Ruijie **Gao**

Student · Computer Systems and Architecture

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"I am not throwing away my shot."

Education

Joint Program by University of Glasgow and UESTC — *Chengdu, Sichuan.China*

B.S. in Electronic Engineering Candidate — *Sep. 2021 - Jun. 2025(expected)*

Relevant Course

- Introductory Programming (Scored a 99)
- Microelectronic Systems (Earned an 85, for course project and presentation)
- Engineering Design and Problem-Solving Practice Problem (On YouTube, provided by CMU)
- Introduction of Computer Systems (On Coursera, provided by Princeton University)
- Algorithm (On YouTube, by official tutorial and this textbook)
- Digital Design and Computer Architecture (On Coursera, provided by UCSD)
- Combinatorics and Probability

Skills

Programming C++, Verilog, Constructing Hardware in a Scala Embedded Language(Chisel), JAVA, Scala

Tools GUN/Linux, CLI Tools, Verilator, Iverilog, Git

Front-end JavaScript, HTML5, Electron, CSS

Languages
- English — Fluent, achieved 321 in GRE
- Mandarin — Native

Course Work/Projects

Risc-v emulator — *Repositories Link* *https://github.com/wuliJerry/ysyx-workbench/tree/master/nemu*

Self Project

- An 64-bit RISC-V IM emulator written in C

Morse-code Decoder — *Repository Link* *https://github.com/wuliJerry/MS-Lab*

Course Project of Microelectronic Systems

- A Morse-decoder implementing embedded C++ based on the STM32 NUCLEO-L432KC develop board and ARM mbed environment

Yosys-Script Language Support — *Project Link* *https://github.com/wuliJerry/Yosys-script*

VS code extension

- A language support extension for Yosys script. Yosys is a framework for RTL synthesis tool.)

Experience

Institute of Computing Technology, Chinese Academy of Sciences — *Beijing, China*

Hardware Engineer — *Aug. 2022, Dec. 2022*

- Use Chisel, a hardware Construct language (HCL), to design and implement a 5-stage pipeline CPU core based on the RISC-V 64IM Instruction Set Architecture (ISA)
- Implement and test the various components of the CPU core, including the instruction decoder, register file, execution units, and memory interface
- Use software tools such as verilator to build a simulation framework for the CPU core, including an interactive shell that allows for single-step execution and monitoring of registers and memory state
- Write and maintain comprehensive documentation for the CPU core and its associated simulation tools

ECE Department, UESTC

Sichuan, China

Teaching Assistant

Sep. 2022 - Dec. 2022

- Assist the instructor in teaching an introductory programming course to freshman students
- Help students understand course materials and concepts through individual and group tutoring sessions, office hours, and other support activities
- Facilitate class discussions and review sessions, and provide additional explanations and examples as needed

Institute of Fundamental and Frontier Sciences, UESTC

Sichuan, China

Research Intern

Feb. 2022 - June. 2022

- Collaborated with a graduate student on a research project involving the construction and testing of transistors using Molybdenum disulfide, graphene, and Boron nitride
- Assisted in the setup and operation of laboratory equipment
- Conducted experiments to measure the flexibility and electrical attributes of the transistor materials
- Collected and analyzed data
- Interpreted results and prepared reports