Jerry (Ruijie) Gao

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Education

University of Glasgow & UESTC   2021/09 – 2025/06 (expect)
B. Sc in Electrical and Electronic Engineering   Chengdu, China
- Teaching Assistant for *Introductory Programming* (2022 Fall)
- Relevant Course (Self-study):
  - Computer Architecture and Engineering   Berkeley CS152/252A
  - Introduction to Computer Systems   CMU 15-213
  - Algorithms I/II   Prof. Robert Sedgewick, Princeton
  - Digital Design & Computer Architecture   Prof. Onur Mutlu, ETH Zürich
  - Circuits and Systems   Prof. Ali Hajimiri, Caltech

Experience

Princeton University   2022/10 – 2023/03
Research Intern   Remote
- **Simulation Acceleration.** Implemented the method of compiler optimization on the synthesis of RTL netlist to generate reduced as well as cycle-accurate RTL code.
- **Experiment.** Compared the simulation time of the original RTL code and the optimized RTL code, and the result shows that the reduced RTL code can save 2x simulation time. Haven tested on multiple designs, including CPU core, deep-learning accelerator, floating point compute unit and general purpose GPU.
- **Assist & Collaborated with** Dr. Yu Zeng
- **Publication.** The result is preparing to submit to *ICCAD, 2023*.

Chinese Academy of Science, "One Core for Life" Project   2022/08 – 2022/10
Hardware Engineer   Remote
- **Designed a RISC-V 64IM CPU core** with 5-stage pipeline and 3 levels of cache, using CHISEL. Fixed bugs in the design and passed all the tests in the RISC-V compliance test suite.
- **Built Simulation Framework** for the core, based on Verilator and C++. Inspired by GEM5, the framework can simulate the core with a core-state monitor and user program.
- **Verified the Design** on ICE40UP5k FPGA, using *icestorm* toolchain.

Institute of Fundamental and Frontier Sciences, UESTC   2022/03 – 2022/07
Research Intern   Chengdu, Sichuan
- **Built a 2-D Material-based Transistor** using PDMS-assisted dry seperation method. The transistor consisted of MoS_2 as the drain, BN as the insulating layer and Graphene as the gate.
- **Measured and Analysed** its electrical properties, including the drain current, the gate voltage and the drain voltage.

Skills

Programming and Platform
- C/C++, GNU/Linux, Scala, Rust, Bash, Java, Windows/WSL, JavaScript, Python,

Hardware Design
- Verilog, Chisel, Vivado HLS
- Vivado, Icestorm, Verilator, Icarus Verilog

Language
- English (GRE 321+4, CET-6 645/710), Chinese (native)

Personal Projects

Yosys-script A Visual Studio Code language support for Yosys script.
NEMU A full-stack RISC-V emulator implemented in C/C++
NeoVim Config My NeoVim config implemented in Lua
Morse-code Decoder A simple morse-code decoder implemented in C++ based on STM32-L432KC