

Jerry (Ruijie) Gao

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Education

University of Glasgow & UESTC

2021/09 – 2025/06 (expected)

B. Sc. in Electrical and Electronic Engineering

Chengdu, China

- Teaching Assistant for *Introductory Programming* (2022 Fall)

- Major GPA: 93.6/100

- Relevant Course (Self-study):

- Computer Architecture and Engineering

Berkeley CS152/252A

- Introduction to Computer Systems

CMU 15-213

- Algorithms I/II

Prof. Robert Sedgewick, Princeton

- Digital Design & Computer Architecture

Prof. Onur Mutlu, ETH Zürich

- Circuits and Systems

Prof. Ali Hajimiri, Caltech

- Introduction to Machine Learning

CMU 10-301/601

Experience

Princeton University

2023/02 – Present

Research Collaboration

Remote

- **Following up** on the [FlashAttention](#), to accelerate the training of Transformers by quantificationally modeling the intra-accelerator data movement and reducing it.

- **Assist & Collaborated with** Dr. [Yu Zeng](#)

Princeton University

2022/10 – 2023/01

Research Collaboration

Remote

- **Simulation Acceleration.** Implemented the method of compiler optimization on the synthesis of RTL netlist to generate reduced as well as cycle-accurate RTL code.

- **Experiment.** Compared the simulation time of the original RTL code and the optimized RTL code, and the result shows that the reduced RTL code can save 2x simulation time. Haven tested on multiple designs, including CPU core, deep-learning accelerator, floating point compute unit, and general purpose GPU.

- **Assist & Collaborated with** Dr. [Yu Zeng](#)

Chinese Academy of Science, “One Core for Life” Project

2022/08 – 2022/10

Hardware Engineer

Remote

- **Designed a RISC-V 64IM CPU core** with 5-stage pipeline and 3 levels of cache, using CHISEL. Fixed bugs in the design and passed all the tests in the RISC-V compliance test suite.

- **Built Simulation Framework** for the core, based on Verilator and C++. Inspired by GEM5, the framework can simulate the core with a core-state monitor and user program.

- **Verified the Design** on ICE40UP5k FPGA, using *icestorm* toolchain.

Institute of Fundamental and Frontier Sciences, UESTC

2022/03 – 2022/07

Research Intern

Chengdu, Sichuan

- **Built a 2-D Material-based Transistor** using the PDMS-assisted dry separation method. The transistor consisted of MoS₂ as the drain, BN as the insulating layer and Graphene as the gate.

- **Measured and Analysed** its electrical properties, including the drain current, the gate voltage, and the drain voltage.

Skills

Programming

- C/C++, Scala, Python, Rust, Bash, Java

- PyTorch, Triton, CUDA

Hardware Design

- Verilog, Chisel, Vivado HLS

- Vivado, Icestorm, Verilator, Icarus Verilog

Platforms and Tools

- GNU/Linux, KVM/QEMU, Windows/WSL2

Language

- English (GRE 321+4, CET-6 645/710), Chinese (native)

Certifications

Machine Learning with Python

2022, Summer

[freeCodeBootcamp](#)

Remote

Personal Projects

Yosys-script A Visual Studio Code language support for Yosys script.

NEMU A full-stack RISC-V emulator implemented in C/C++

NeoVim Config My NeoVim config implemented in Lua