1. Description

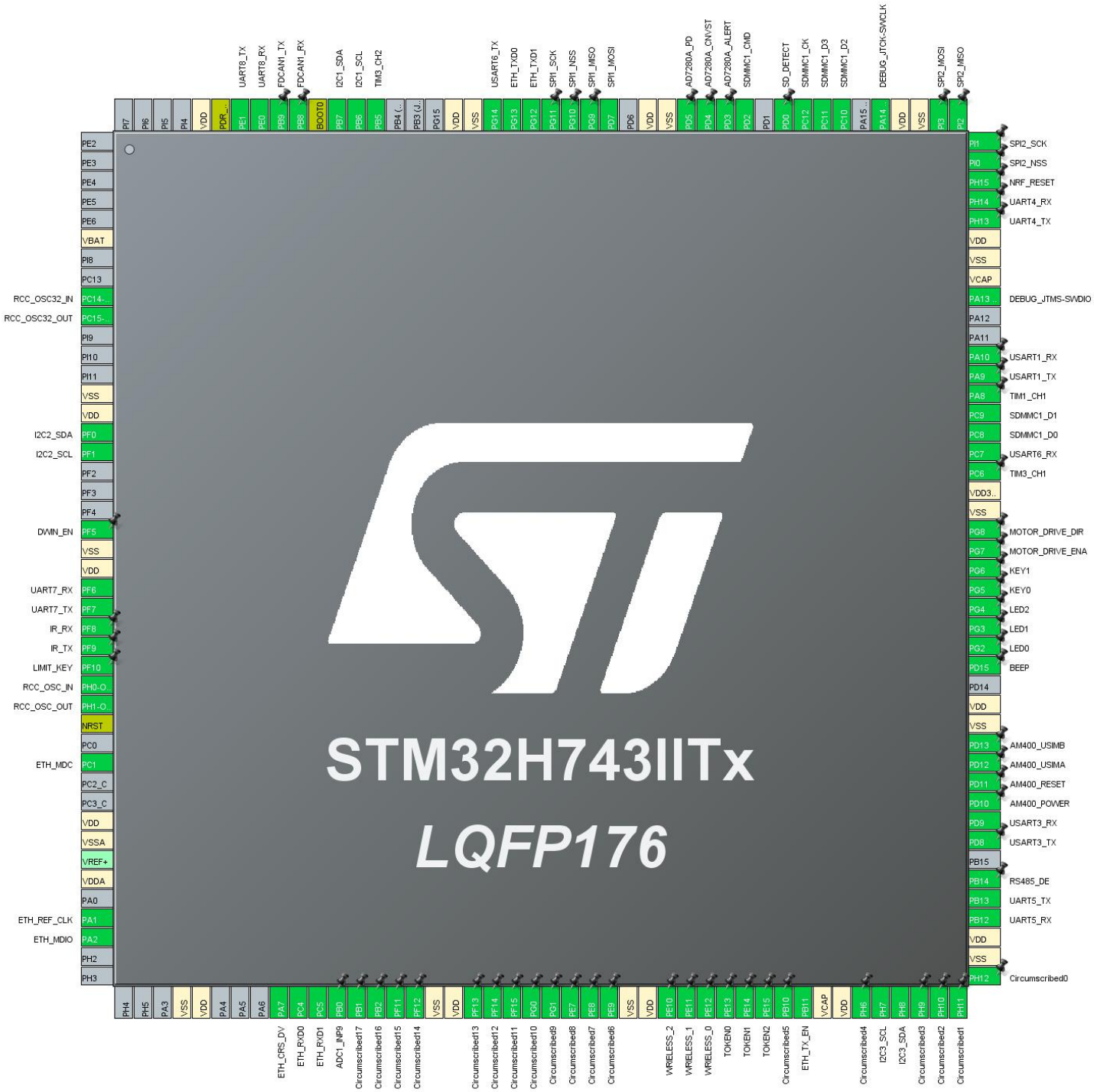
1.1. Project

Project Name	00_H743_Core
Board Name	custom
Generated with:	STM32CubeMX 5.4.0
Date	01/15/2020

1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H743/753
MCU name	STM32H743IITx
MCU Package	LQFP176
MCU Pin number	176

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
9	PC14-OSC32_IN (OSC32_IN)	I/O	RCC_OSC32_IN	
10	PC15-OSC32_OUT (OSC32_OUT)	I/O	RCC_OSC32_OUT	
14	VSS	Power		
15	VDD	Power		
16	PF0	I/O	I2C2_SDA	
17	PF1	I/O	I2C2_SCL	
21	PF5 *	I/O	GPIO_Output	DWIN_EN
22	VSS	Power		
23	VDD	Power		
24	PF6	I/O	UART7_RX	
25	PF7	I/O	UART7_TX	
26	PF8 *	I/O	GPIO_Input	IR_RX
27	PF9 *	I/O	GPIO_Output	IR_TX
28	PF10	I/O	GPIO_EXTI10	LIMIT_KEY
29	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
30	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
31	NRST	Reset		
33	PC1	I/O	ETH_MDC	
36	VDD	Power		
37	VSSA	Power		
39	VDDA	Power		
41	PA1	I/O	ETH_REF_CLK	
42	PA2	I/O	ETH_MDIO	
48	VSS	Power		
49	VDD	Power		
53	PA7	I/O	ETH_CRS_DV	
54	PC4	I/O	ETH_RXD0	
55	PC5	I/O	ETH_RXD1	
56	PB0	I/O	ADC1_INP9	
57	PB1 *	I/O	GPIO_Output	Circumscribed17
58	PB2 *	I/O	GPIO_Output	Circumscribed16
59	PF11 *	I/O	GPIO_Output	Circumscribed15
60	PF12 *	I/O	GPIO_Output	Circumscribed14

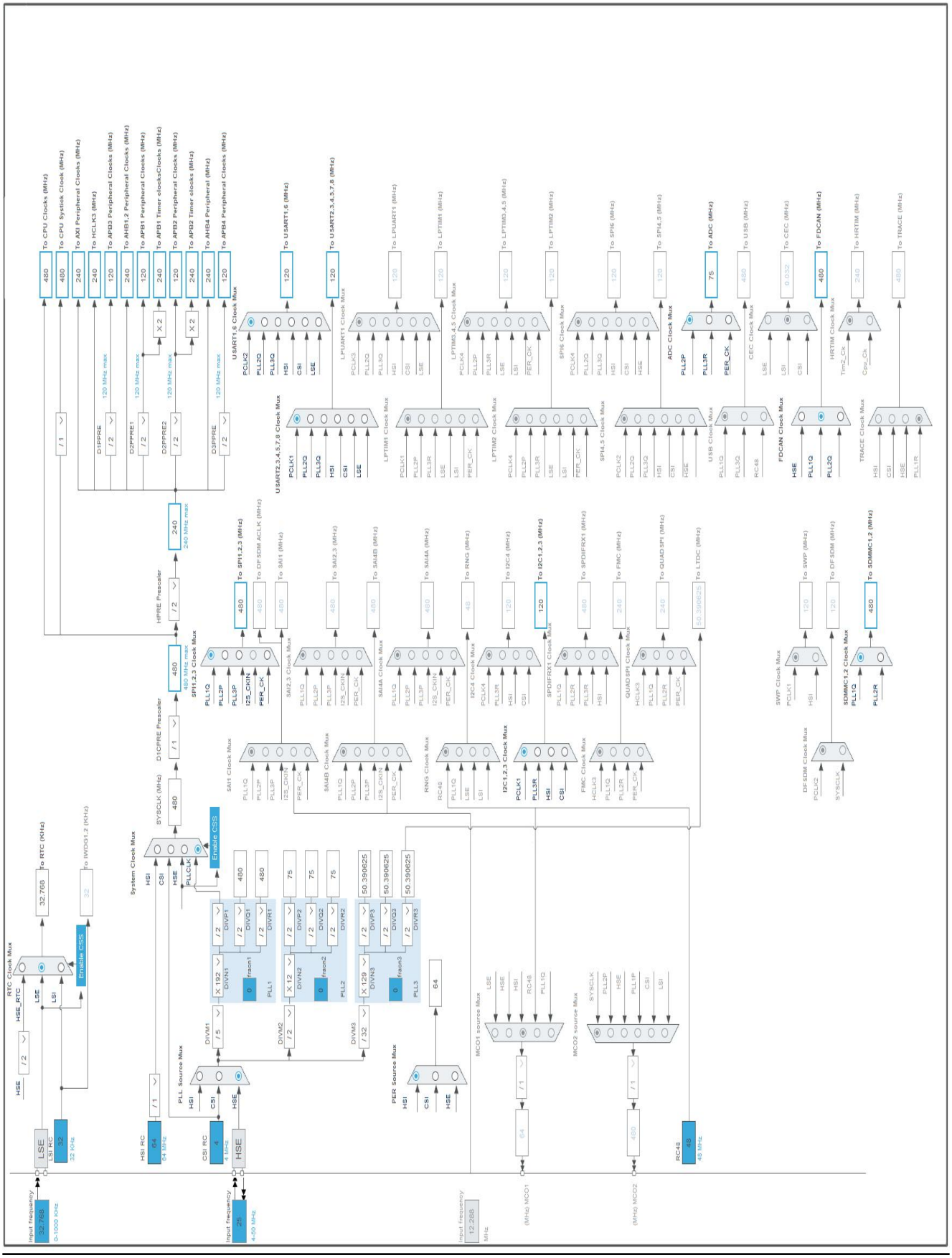
Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
61	VSS	Power		
62	VDD	Power		
63	PF13 *	I/O	GPIO_Output	Circumscribed13
64	PF14 *	I/O	GPIO_Output	Circumscribed12
65	PF15 *	I/O	GPIO_Output	Circumscribed11
66	PG0 *	I/O	GPIO_Output	Circumscribed10
67	PG1 *	I/O	GPIO_Output	Circumscribed9
68	PE7 *	I/O	GPIO_Output	Circumscribed8
69	PE8 *	I/O	GPIO_Output	Circumscribed7
70	PE9 *	I/O	GPIO_Output	Circumscribed6
71	VSS	Power		
72	VDD	Power		
73	PE10 *	I/O	GPIO_Output	WRIELESS_2
74	PE11 *	I/O	GPIO_Output	WRIELESS_1
75	PE12 *	I/O	GPIO_Output	WRIELESS_0
76	PE13 *	I/O	GPIO_Output	TOKEN0
77	PE14 *	I/O	GPIO_Output	TOKEN1
78	PE15 *	I/O	GPIO_Output	TOKEN2
79	PB10 *	I/O	GPIO_Output	Circumscribed5
80	PB11	I/O	ETH_TX_EN	
81	VCAP	Power		
82	VDD	Power		
83	PH6 *	I/O	GPIO_Output	Circumscribed4
84	PH7	I/O	I2C3_SCL	
85	PH8	I/O	I2C3_SDA	
86	PH9 *	I/O	GPIO_Output	Circumscribed3
87	PH10 *	I/O	GPIO_Output	Circumscribed2
88	PH11 *	I/O	GPIO_Output	Circumscribed1
89	PH12 *	I/O	GPIO_Output	Circumscribed0
90	VSS	Power		
91	VDD	Power		
92	PB12	I/O	UART5_RX	
93	PB13	I/O	UART5_TX	
94	PB14 *	I/O	GPIO_Output	RS485_DE
96	PD8	I/O	USART3_TX	
97	PD9	I/O	USART3_RX	
98	PD10 *	I/O	GPIO_Output	AM400_POWER
99	PD11 *	I/O	GPIO_Output	AM400_RESET
100	PD12 *	I/O	GPIO_Output	AM400_USIMA

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
101	PD13 *	I/O	GPIO_Output	AM400_USIMB
102	VSS	Power		
103	VDD	Power		
105	PD15 *	I/O	GPIO_Output	BEEP
106	PG2 *	I/O	GPIO_Output	LED0
107	PG3 *	I/O	GPIO_Output	LED1
108	PG4 *	I/O	GPIO_Output	LED2
109	PG5	I/O	GPIO_EXTI5	KEY0
110	PG6	I/O	GPIO_EXTI6	KEY1
111	PG7 *	I/O	GPIO_Output	MOTOR_DRIVE_ENA
112	PG8 *	I/O	GPIO_Output	MOTOR_DRIVE_DIR
113	VSS	Power		
114	VDD33_USB	Power		
115	PC6	I/O	TIM3_CH1	
116	PC7	I/O	USART6_RX	
117	PC8	I/O	SDMMC1_D0	
118	PC9	I/O	SDMMC1_D1	
119	PA8	I/O	TIM1_CH1	
120	PA9	I/O	USART1_TX	
121	PA10	I/O	USART1_RX	
124	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
125	VCAP	Power		
126	VSS	Power		
127	VDD	Power		
128	PH13	I/O	UART4_TX	
129	PH14	I/O	UART4_RX	
130	PH15 *	I/O	GPIO_Output	NRF_RESET
131	PI0	I/O	SPI2_NSS	
132	PI1	I/O	SPI2_SCK	
133	PI2	I/O	SPI2_MISO	
134	PI3	I/O	SPI2_MOSI	
135	VSS	Power		
136	VDD	Power		
137	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
139	PC10	I/O	SDMMC1_D2	
140	PC11	I/O	SDMMC1_D3	
141	PC12	I/O	SDMMC1_CK	
142	PD0	I/O	GPIO_EXTI0	SD_DETECT
144	PD2	I/O	SDMMC1_CMD	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
145	PD3 *	I/O	GPIO_Output	AD7280A_ALERT
146	PD4 *	I/O	GPIO_Output	AD7280A_CNVST
147	PD5 *	I/O	GPIO_Output	AD7280A_PD
148	VSS	Power		
149	VDD	Power		
151	PD7	I/O	SPI1_MOSI	
152	PG9	I/O	SPI1_MISO	
153	PG10	I/O	SPI1_NSS	
154	PG11	I/O	SPI1_SCK	
155	PG12	I/O	ETH_TXD1	
156	PG13	I/O	ETH_TXD0	
157	PG14	I/O	USART6_TX	
158	VSS	Power		
159	VDD	Power		
163	PB5	I/O	TIM3_CH2	
164	PB6	I/O	I2C1_SCL	
165	PB7	I/O	I2C1_SDA	
166	BOOT0	Boot		
167	PB8	I/O	FDCAN1_RX	
168	PB9	I/O	FDCAN1_TX	
169	PE0	I/O	UART8_RX	
170	PE1	I/O	UART8_TX	
171	PDR_ON	Reset		
172	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	00_H743_Core
Project Folder	D:\03_WorkSpace\03_STM32Cube_HAL\00_H743_Core
Toolchain / IDE	MDK-ARM V5.27
Firmware Package Name and Version	STM32Cube FW_H7 V1.5.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32H7
Line	STM32H743/753
MCU	STM32H743IITx
Datasheet	DS12110_Rev5

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN9

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	Asynchronous clock mode divided by 1
Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Left Bit Shift	No bit shift
Enable Regular Oversampling	Disable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 9
Sampling Time	1.5 Cycles
Offset Number	No offset

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable

Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false

7.2. DEBUG

Debug: Serial Wire

7.3. ETH

Mode: RMII

7.3.1. Parameter Settings:

General : Ethernet Configuration:

Warning	The ETH can work only when RAM is pointing at 0x24000000
Note	PHY Driver must be configured from the LwIP 'Platform Settings' top right tab
Ethernet MAC Address	00:80:E1:00:00:00
Tx Descriptor Length	4
First Tx Descriptor Address	**0x30040060 ***
Rx Descriptor Length	4
First Rx Descriptor Address	**0x30040000 ***
Rx Buffers Address	**0x30040200 ***
Rx Buffers Length	1524

7.4. FDCAN1

Mode: Classic Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Classic mode
Mode	Normal mode
Auto Retransmission	Disable
Transmit Pause	Disable
Protocol Exception	Disable
Nominal Prescaler	1
Nominal Sync Jump Width	1
Nominal Time Seg1	2
Nominal Time Seg2	2
Data Prescaler	1
Data Sync Jump Width	1
Data Time Seg1	1
Data Time Seg2	1
Message Ram Offset	0
Std Filters Nbr	0

Ext Filters Nbr	0
Rx Fifo0 Elmts Nbr	0
Rx Fifo0 Elmt Size	8 bytes data field
Rx Fifo1 Elmts Nbr	0
Rx Fifo1 Elmt Size	8 bytes data field
Rx Buffers Nbr	0
Rx Buffer Size	8 bytes data field
Tx Events Nbr	0
Tx Buffers Nbr	0
Tx Fifo Queue Elmts Nbr	0
Tx Fifo Queue Mode	FIFO mode
Tx Elmt Size	8 bytes data field

7.5. GPIO

7.6. I2C1

I2C: I2C

7.6.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x307075B1 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.7. I2C2

I2C: I2C

7.7.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x307075B1 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.8. I2C3

I2C: I2C

7.8.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x307075B1 ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.9. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : BYPASS Clock Source

7.9.1. Parameter Settings:

SupplySource	PWR_LDO_SUPPLY

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	32

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

PLL range Parameters:

PLL1 clock Input range	Between 4 and 8 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	MEDIUM VCO range

7.10. RTC

mode: Activate Clock Source

7.10.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

7.11. SDMMC1

Mode: SD 4 bits Wide bus

7.11.1. Parameter Settings:

Common SDMMC parameters:

does the board use µSD transceiver	Enabled

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	The hardware control flow is disabled
SDMMC clock divide factor	0

7.12. SPI1

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.12.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**32 ***
Baud Rate	**15.0 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.13. SPI2

Mode: Full-Duplex Master

Hardware NSS Signal: Hardware NSS Output Signal

7.13.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**128 ***
Baud Rate	**3.75 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Output Hardware
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

7.14. SYS

Timebase Source: SysTick

7.15. TIM1

Channel1: PWM Generation CH1

7.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.16. TIM3

Combined Channels: Encoder Mode

7.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.17. UART4

Mode: Asynchronous

7.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.18. UART5

Mode: Asynchronous

7.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable

Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.19. UART7

Mode: Asynchronous

7.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.20. UART8

Mode: Asynchronous

7.20.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200

Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.21. USART1

Mode: Asynchronous

7.21.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.22. USART3

Mode: Asynchronous

7.22.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.23. USART6

Mode: Asynchronous

7.23.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	clock /1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PB0	ADC1_INP9	Analog mode	No pull-up and no pull-down	n/a	
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG12	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
FDCAN1	PB8	FDCAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB9	FDCAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PF1	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C3	PH7	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PH8	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN (OSC32_IN)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PD7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG9	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG10	SPI1_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG11	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PI0	SPI2_NSS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI1	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PI3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART4	PH13	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH14	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART5	PB12	UART5_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB13	UART5_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART7	PF6	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PF7	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART8	PE0	UART8_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE1	UART8_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
USART6	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PG14	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PF5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DWIN_EN
	PF8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IR_RX
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	IR_TX
	PF10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	LIMIT_KEY
	PB1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed17
	PB2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed16

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PF11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed15
	PF12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed14
	PF13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed13
	PF14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed12
	PF15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed11
	PG0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed10
	PG1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed9
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed8
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed7
	PE9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed6
	PE10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WRIELESS_2
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WRIELESS_1
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	WRIELESS_0
	PE13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TOKEN0
	PE14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TOKEN1
	PE15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TOKEN2
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed5
	PH6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed4
	PH9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed3
	PH10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed2
	PH11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed1
	PH12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Circumscribed0
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RS485_DE
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AM400_POWER
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AM400_RESET
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AM400_USIMA
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AM400_USIMB
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	BEEP
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED0
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PG4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PG5	GPIO_EXTI5	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	KEY0
	PG6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	KEY1
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_DRIVE_ENA
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MOTOR_DRIVE_DIR
	PH15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	NRF_RESET
	PD0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	SD_DETECT
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AD7280A_ALERT

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AD7280A_CNVST
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	AD7280A_PD

8.2. DMA configuration

nothing configured in DMA service

8.3. BDMA configuration

nothing configured in DMA service

8.4. MDMA configuration

nothing configured in DMA service

8.5. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line0 interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
FDCAN1 interrupt 0	unused		
FDCAN1 interrupt 1	unused		
EXTI line[9:5] interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
USART1 global interrupt	unused		
USART3 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
SDMMC1 global interrupt	unused		
UART4 global interrupt	unused		
UART5 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 86	unused		
FDCAN calibration unit interrupt	unused		
USART6 global interrupt	unused		
I2C3 event interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
I2C3 error interrupt	unused		
FPU global interrupt	unused		
UART7 global interrupt	unused		
UART8 global interrupt	unused		
HSEM1 global interrupt	unused		

*** User modified value**

9. Software Pack Report