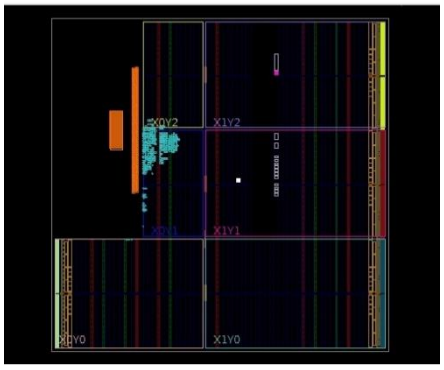
Soc lab 1

系統介紹:此系統結果為輸出乘法表。

透過 10,18 腳位輸入，不斷加 1 的數後。

並於 20 腳位輸出 10 18 腳位相乘結果。



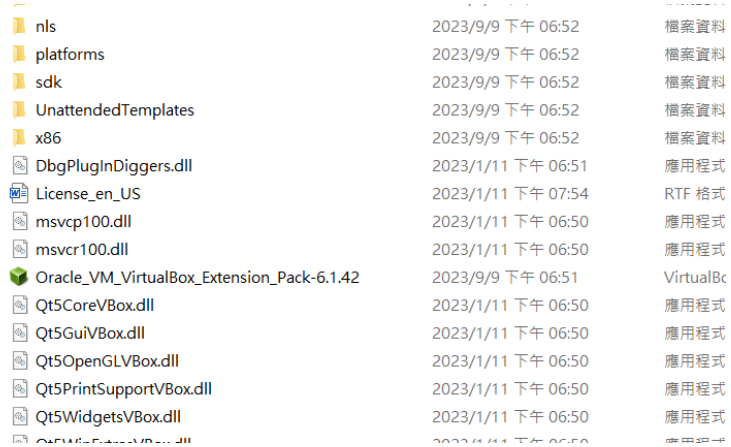
安裝測試:

```
ubuntu@ubuntu2004:~$ vitis

****** Xilinx Vitis Development Environment
****** Vitis v2022.1 (64-bit)
  **** SW Build 3524922 on 2022-04-14-18:00:18
    ** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
```

```
ubuntu@ubuntu2004:~$ vitis_hls

****** Vitis HLS - High-Level Synthesis from C, C++ and OpenCL v2022.1 (64-bit)
  **** SW Build 3526262 on Mon Apr 18 15:47:01 MDT 2022
  **** IP Build 3524634 on Mon Apr 18 20:55:01 MDT 2022
    ** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
```

```
ubuntu@ubuntu2004:~$ vivado

****** Vivado v2022.1 (64-bit)
  **** SW Build 3526262 on Mon Apr 18 15:47:01 MDT 2022
  **** IP Build 3524634 on Mon Apr 18 20:55:01 MDT 2022
    ** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.

start_gui
```

安裝擴充包要放在 C:\Program Files\Oracle\VirtualBo

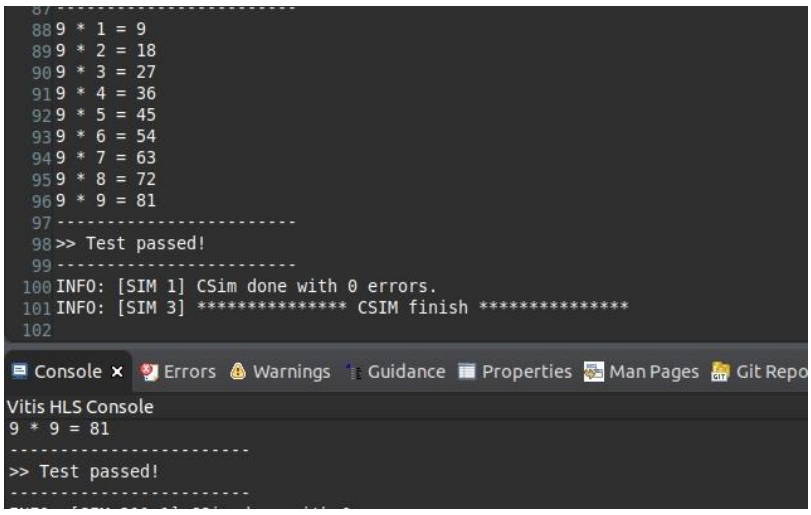


nls	2023/9/9 下午 06:52	檔案資料
platforms	2023/9/9 下午 06:52	檔案資料
sdk	2023/9/9 下午 06:52	檔案資料
UnattendedTemplates	2023/9/9 下午 06:52	檔案資料
x86	2023/9/9 下午 06:52	檔案資料
DbgPlugInDiggers.dll	2023/1/11 下午 06:51	應用程式
License_en_US	2023/1/11 下午 07:54	RTF 格式
msvcp100.dll	2023/1/11 下午 06:50	應用程式
msvcr100.dll	2023/1/11 下午 06:50	應用程式
Oracle_VM_VirtualBox_Extension_Pack-6.1.42	2023/9/9 下午 06:51	VirtualBo
Qt5CoreVBox.dll	2023/1/11 下午 06:50	應用程式
Qt5GuiVBox.dll	2023/1/11 下午 06:50	應用程式
Qt5OpenGLVBox.dll	2023/1/11 下午 06:50	應用程式
Qt5PrintSupportVBox.dll	2023/1/11 下午 06:50	應用程式
Qt5WidgetsVBox.dll	2023/1/11 下午 06:50	應用程式

租借 FPGA 後運算結果

```
Entry: /usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py
System argument(s): 3
Start of "/usr/local/share/pynq-venv/lib/python3.8/site-packages/ipykernel_launcher.py"
-------------------------
1 * 1 = 1
1 * 2 = 2
1 * 3 = 3
1 * 4 = 4
1 * 5 = 5
1 * 6 = 6
1 * 7 = 7
1 * 8 = 8
1 * 9 = 9
-------------------------
2 * 1 = 2
2 * 2 = 4
2 * 3 = 6
2 * 4 = 8
2 * 5 = 10
2 * 6 = 12
2 * 7 = 14
2 * 8 = 16
2 * 9 = 18
-------------------------
3 * 1 = 3
3 * 2 = 6
3 * 3 = 9
3 * 4 = 12
3 * 5 = 15
3 * 6 = 18
3 * 7 = 21
3 * 8 = 24
3 * 9 = 27
-------------------------
4 * 1 = 4
4 * 2 = 8
4 * 3 = 12
4 * 4 = 16
4 * 5 = 20
4 * 6 = 24
4 * 7 = 28
4 * 8 = 32
4 * 9 = 36
-------------------------
```

CSIM 運算後結果。

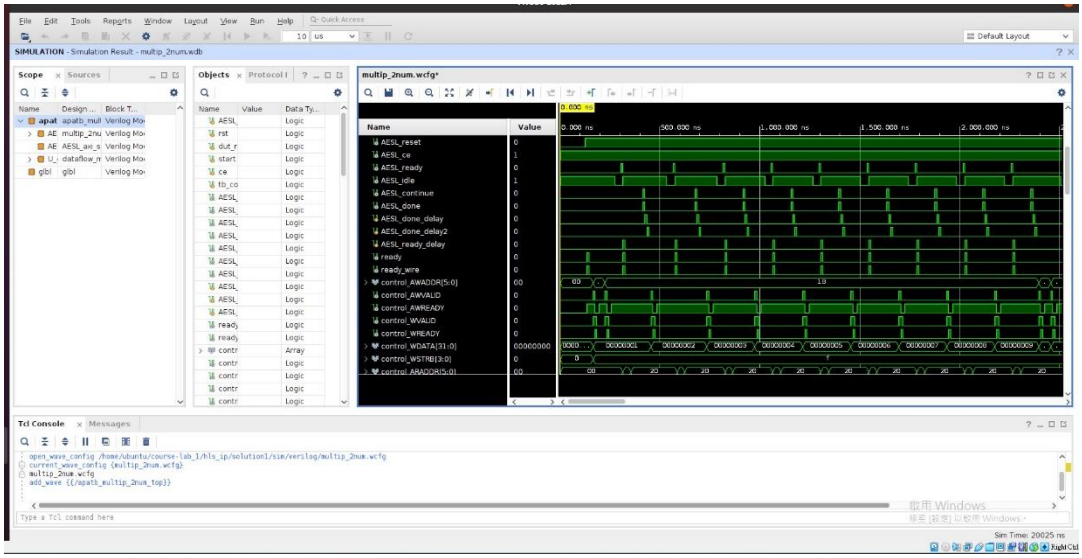


```
88 9 * 1 = 9
89 9 * 2 = 18
90 9 * 3 = 27
91 9 * 4 = 36
92 9 * 5 = 45
93 9 * 6 = 54
94 9 * 7 = 63
95 9 * 8 = 72
96 9 * 9 = 81
97 ------------------------
98 >> Test passed!
99 ------------------------
100 INFO: [SIM 1] CSim done with 0 errors.
101 INFO: [SIM 3] *************** CSIM finish ***************
102
```

Console × Errors Warnings Guidance Properties Man Pages Git Repo

```
Vitis HLS Console
9 * 9 = 81
------------------------
>> Test passed!
------------------------
```

波形圖:


File Edit Tools Reports Window Layout View Run Help
SIMULATION - Simulation Result - multip_2num.wdb
Default Layout
Scope
Sources
Objects
Protocol I
multip_2num.wcfg*
Name
Value
AESL_reset
AESL_ce
AESL_ready
AESL_idle
AESL_continue
AESL_done
AESL_done_delay
AESL_done_delay2
AESL_ready_delay
ready
ready_wire
control_AWADDR[5:0]
control_AWVALID
control_AWREADY
control_WVALID
control_WREADY
control_WDATA[31:0]
control_WSTRB[3:0]
control_ARADDR[5:0]
0.000 ns
500.000 ns
1,000.000 ns
1,500.000 ns
2,000.000 ns
Tcl Console
Messages
open_wave_config /home/ubuntu/course-lab_1/hls_ip/solution1/sim/verilog/multip_2num.wcfg
current_wave_config {multip_2num.wcfg}
multip_2num.wcfg
add_wave {{/apatb_multip_2num_top}}
Type a Tcl command here
Sim Time: 20025 ns