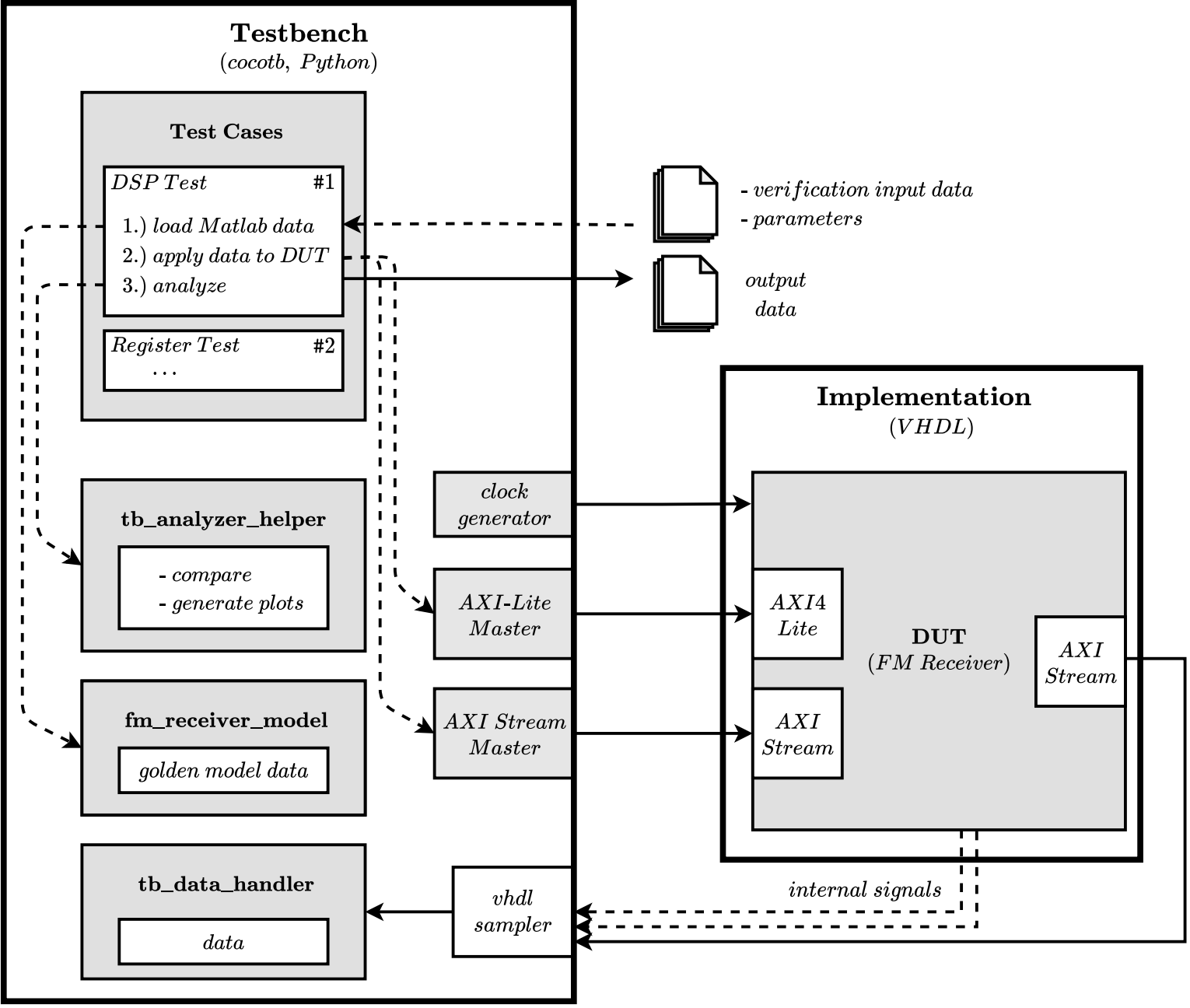
Testbench
(cocotb, Python)
Test Cases
DSP Test #1
1.) load Matlab data
2.) apply data to DUT
3.) analyze
Register Test #2
...
- verification input data
- parameters
output data
Implementation
(VHDL)
tb_analyzer_helper
- compare
- generate plots
fm_receiver_model
golden model data
tb_data_handler
data
clock generator
AXI-Lite Master
AXI Stream Master
vhdl sampler
AXI4 Lite
AXI Stream
DUT
(FM Receiver)
AXI Stream
internal signals