# REALTEK

## RTL8211E-VB-CG
## RTL8211E-VL-CG
## RTL8211EG-VB-CG

# INTEGRATED 10/100/1000M ETHERNET TRANSCEIVER

# DATASHEET
### (CONFIDENTIAL: Development Partners Only)

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## USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

## REVISION HISTORY

| Revision | Release Date | Summary |
|---|---|---|
| 1.0 | 2009/08/31 | First release. |
| 1.1 | 2010/08/13 | Added RTL8211EG-CG product data. |
| 1.2 | 2010/08/16 | Corrected minor typing errors. |
| 1.3 | 2010/12/17 | Added RTL8211E-VL-CG model number. |
|  |  | Revised Table 24 BMCR (Basic Mode Control Register, Address 0x00), page 31. |
|  |  | Revised Table 33 GBCR (1000Base-T Control Register, Address 0x09), page 37. |
|  |  | Revised Table 41 INSR (Interrupt Status Register, Address 0x13), page 42. |
|  |  | Revised Table 57 Power Sequence Parameter, page 55. |
|  |  | Revised Table 63 MDC/MDIO Management Timing Parameters, page 59. |
|  |  | Added section 10.6.2 MII Transmission Cycle Timing, page 60. |
|  |  | Added section 10.6.3 MII Reception Cycle Timing (RTL8211EG-VB Only), page 60. |
|  |  | Revised Table 66 GMII Timing Parameters, page 62. |
|  |  | Revised section 12 Ordering Information, page 68. |
| 1.4 | 2011/05/17 | Revised section 2 Features, page 2. |
|  |  | Revised section 3 System Applications, page 3. |
|  |  | Added section 4 Block Diagram, page 5. |
|  |  | Revised Table 6 Reset, page 11. |
|  |  | Revised Table 10 Power and Ground, page 12. |
|  |  | Added section 7.5 Interrupt, page 15. |
|  |  | Revised section 7.7 Hardware Configuration, page 16. |
|  |  | Revised Figure 7 LED and PHY Address Configuration, page 17. |
|  |  | Revised section 7.9.2 Register Setting, page 18. |
|  |  | Revised section 7.10.4 Management Interface, page 19. |
|  |  | Revised section 7.10.5 Access to Extension Page (ExtPage), page 21. |
|  |  | Added section 7.16 PHY Reset (Hardware Reset), page 29. |
|  |  | Revised Table 24 BMCR (Basic Mode Control Register, Address 0x00), page 31. |
|  |  | Revised Table 38 PHYCR (PHY Specific Control Register, Address 0x10), page 39. |
|  |  | Revised Table 58 Absolute Maximum Ratings, page 56. |
|  |  | Revised Table 59 Recommended Operating Conditions, page 56. |
|  |  | Revised Table 62 DC Characteristics, page 58. |
|  |  | Revised section 10.6.1 MDC/MDIO Timing, page 59. |
|  |  | Revised section 10.6.2 MII Transmission Cycle Timing (RTL8211EG-VB Only), page 60. |
|  |  | Revised Table 68 Ordering Information, page 68. |
| 1.5 | 2011/10/28 | Revised section 4 Block Diagram, page 5. |
|  |  | Revised Table 36 MAADR (MMD Access Address Data Register, Address 0x0E), page 39. |
|  |  | Revised Table 40 INER (Interrupt Enable Register, Address 0x12), page 41. |
|  |  | Revised Table 57 Power Sequence Parameter, page 55. |
|  |  | Revised Table 62 DC Characteristics, page 58. |
|  |  | Revised Table 64 MII Transmission Cycle Timing, page 60. |
|  |  | Revised Table 65 MII Reception Cycle Timing, page 61. |
|  |  | Revised section 10.6.5 RGMII Timing Modes, page 63. |

| Revision | Release Date | Summary |
|----------|--------------|---------|
| 1.6 | 2012/04/03 | Revised Table 21 Register Mapping and Definitions, page 30. |
| | | Added Table 23 ExtPage Register Mapping and Definition, page 31. |
| | | Added Table 43 LDPSR (Link Down Power Saving Register, Address 0x1B), page 42. |
| | | Added Table 44 EPAGSR (Extension Page Select Register, Address 0x1E), page 42. |
| | | Added Table 52 LACR (LED Action Control Register, ExtPage 0x2c, Address 0x1a), page 45. |
| | | Added Table 53 LCR (LED Control Register, ExtPage 0x2c, Address 0x1c), page 45. |
| | | Added Table 54 ACCR (Auto-Crossover Control Register, ExtPage 0x2d, Address 0x18)45, page 45. |
| | | Revised section 11.4 Mechanical Dimensions Notes (RTL8211EG-VB), page 67. |
| 1.7 | 2013/01/07 | Revised section 1 General Description, page 1. |
| | | Revised section 2 Features, page 2. |
| | | Revised section 7.10.4 Management Interface, page 19. |
| | | Revised section 8 Register Descriptions, page 30. |
| | | Added Table 20. Register Access Types, page 30. |
| | | Revised section 9.5 Power Sequence, page 55. |
| | | Revised Table 68. Ordering Information, page 68. |
| 1.8 | 2013/07/10 | Revised section 7.13 LED Configuration, page 27. |
| | | Added Table 55. SCR (SSC Control Register, ExtPage 0xa0, Address 0x1a), page 45. |
| | | Revised section 10.3 Crystal Requirements, page 57. |
| | | Revised section 10.4 Oscillator/External Clock Requirements, page 57. |

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# 1. General Description

The Realtek RTL8211E-VB-CG/RTL8211E-VL-CG/RTL8211EG-VB-CG are highly integrated Ethernet transceivers that comply with 10Base-T, 100Base-TX, and 1000Base-T IEEE 802.3 standards. They provide all the necessary physical layer functions to transmit and receive Ethernet packets over CAT.5 UTP cable.

The RTL8211E-VB(VL)/RTL8211EG-VB uses state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented in the RTL8211E-VB(VL)/RTL8211EG-VB to provide robust transmission and reception capabilities at 10Mbps, 100Mbps, or 1000Mbps.

Data transfer between MAC and PHY is via the Reduced Gigabit Media Independent Interface (RGMII) or Gigabit Media Independent Interface (GMII) for 1000Base-T, 10Base-T, and 100Base-TX. The RTL8211E-VB supports 3.3V or 2.5V signaling for RGMII; the RTL8211EG-VB provides 3.3V or 2.5V signaling for RGMII/GMII, and the RTL8211E-VL supports 1.5/1.8V signaling for RGMII.

# 2.    Features

- 1000Base-T IEEE 802.3ab Compliant

- 100Base-TX IEEE 802.3u Compliant

- 10Base-T IEEE 802.3 Compliant

- Supports RGMII (RTL8211E-VB, RTL8211E-VL, RTL8211EG-VB)

- Supports GMII (RTL8211EG-VB)

- Supports IEEE 802.3az-2010 (Energy Efficient Ethernet)

- Built-in Wake-on-LAN (WOL)

- Supports Interrupt function

- Supports Parallel Detection

- Crossover Detection & Auto-Correction

- Automatic polarity correction

- Supports PHYRSTB core power Turn-Off

- Baseline Wander Correction

- Supports 120m for CAT.5 cable in 1000Base-T

- Supports 3.3V or 2.5V signaling for RGMII (RTL8211E-VB) and RGMII/GMII (RTL8211EG-VB)

- Supports 1.5V and 1.8V signaling for RGMII (RTL8211E-VL)

- Supports 25/50MHz external crystal or OSC

- Provides 125MHz clock source for MAC

- Provides 3 network status LEDs

- Supports Link Down power saving

- Green Ethernet (1000/100Mbps mode only)

- Built-in switching regulator

- Packages
  - 48-pin QFN (RTL8211E-VB, RTL8211E-VL)
  - 64-pin QFN (RTL8211EG-VB)

- 0.11μm process with very low power consumption

# 3. System Applications

- DTV (Digital TV)

- MAU (Media Access Unit)

- CNR (Communication and Network Riser)

- Game Console

- Printer and Office Machine

- DVD Player and Recorder

- Ethernet Hub

- Ethernet Switch

In addition, can be used in any embedded system with an Ethernet MAC that needs a UTP physical connection.

## 3.1. Application Diagram (RTL8211E-VB)
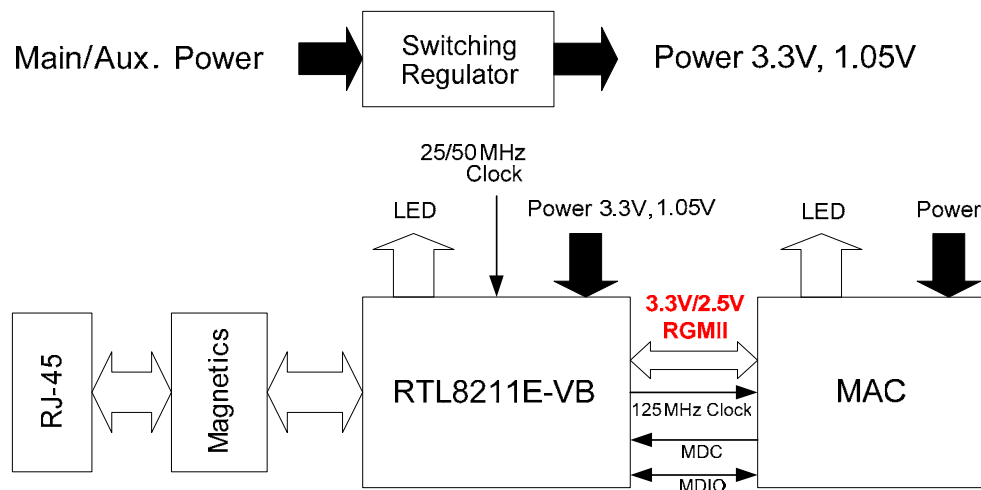


**Figure 1. Application Diagram (RTL8211E-VB)**

## 3.2.   Application Diagram (RTL8211EG-VB)
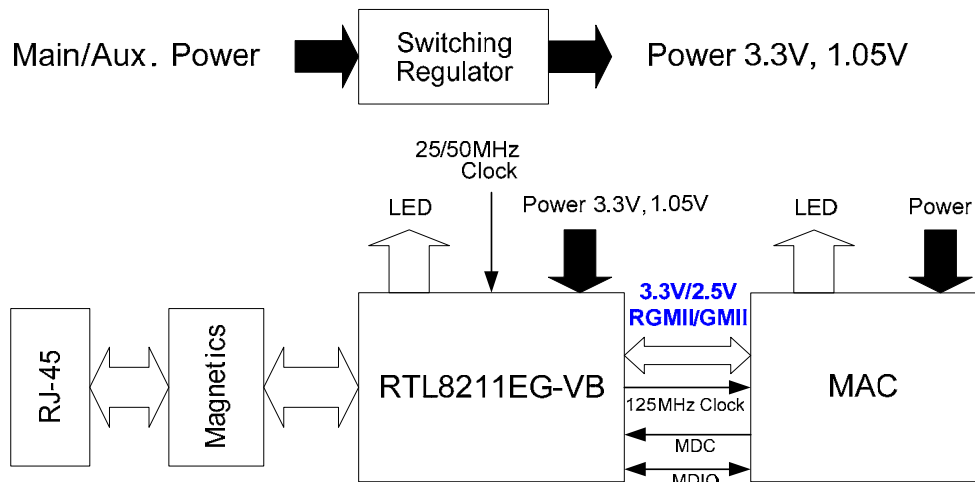


**Figure 2.   Application Diagram (RTL8211EG-VB)**

## 3.3.   Application Diagram (RTL8211E-VL)
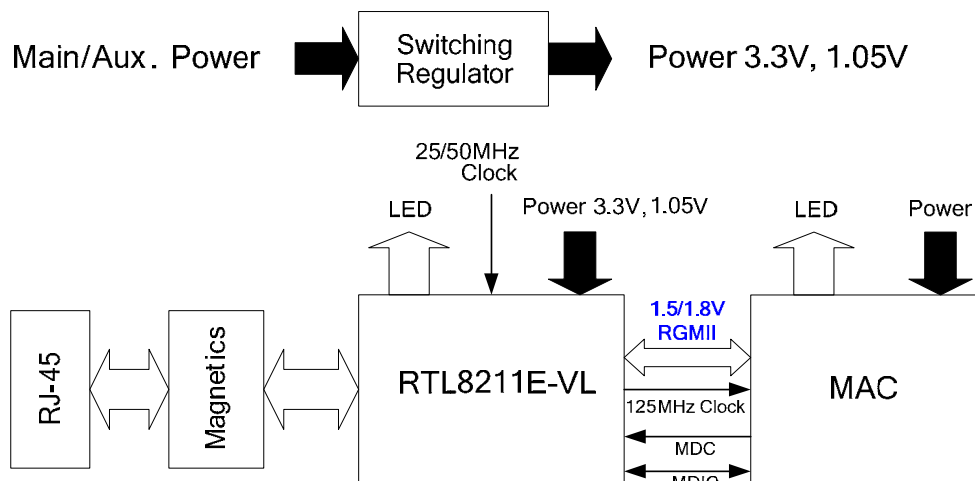


**Figure 3.   Application Diagram (RTL8211EG-VL)**
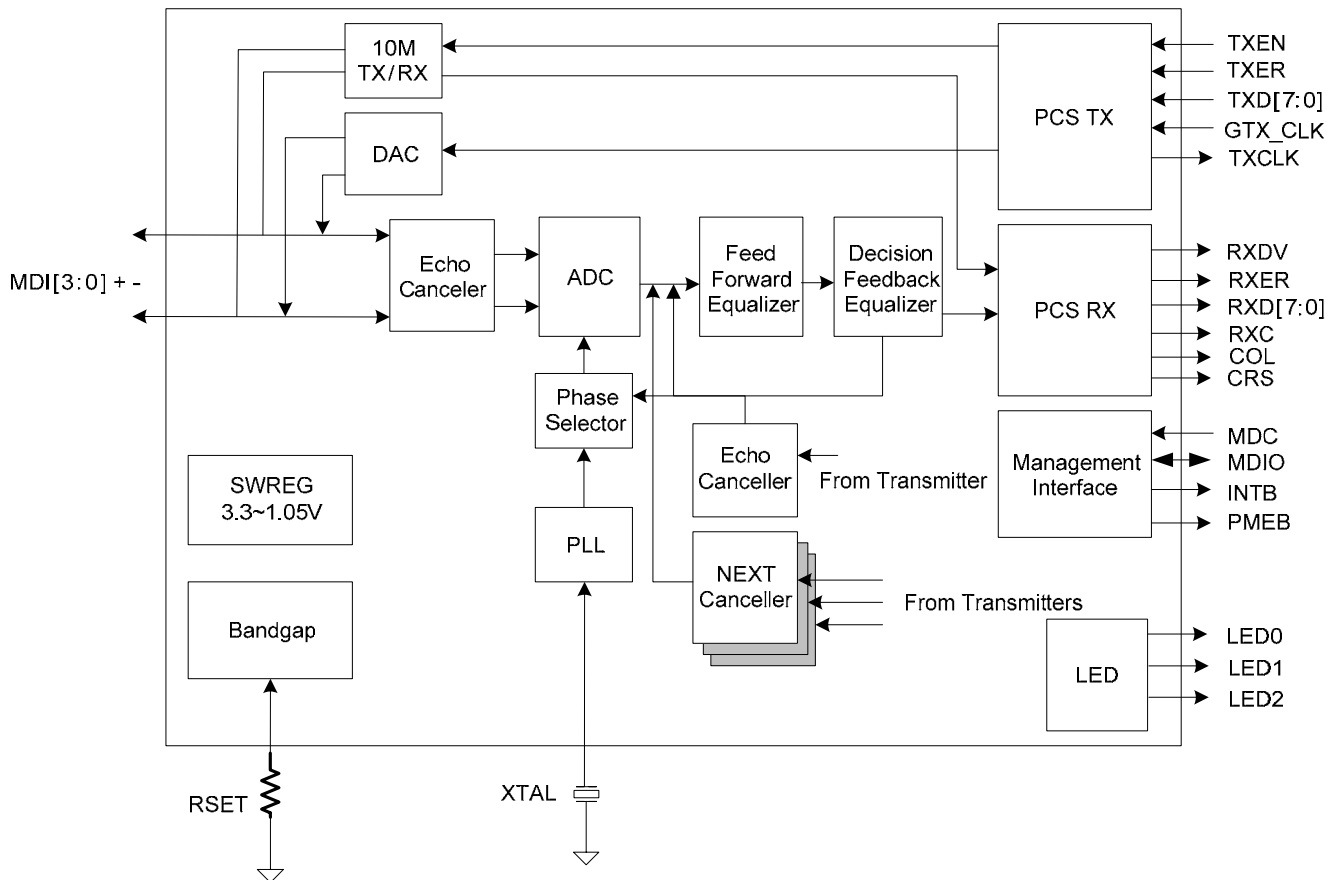
# 4.    Block Diagram



**Figure 4.   Block Diagram**

# 5. Pin Assignments

## 5.1. RTL8211E-VB/RTL8211E-VL Pin Assignments (48-Pin QFN)
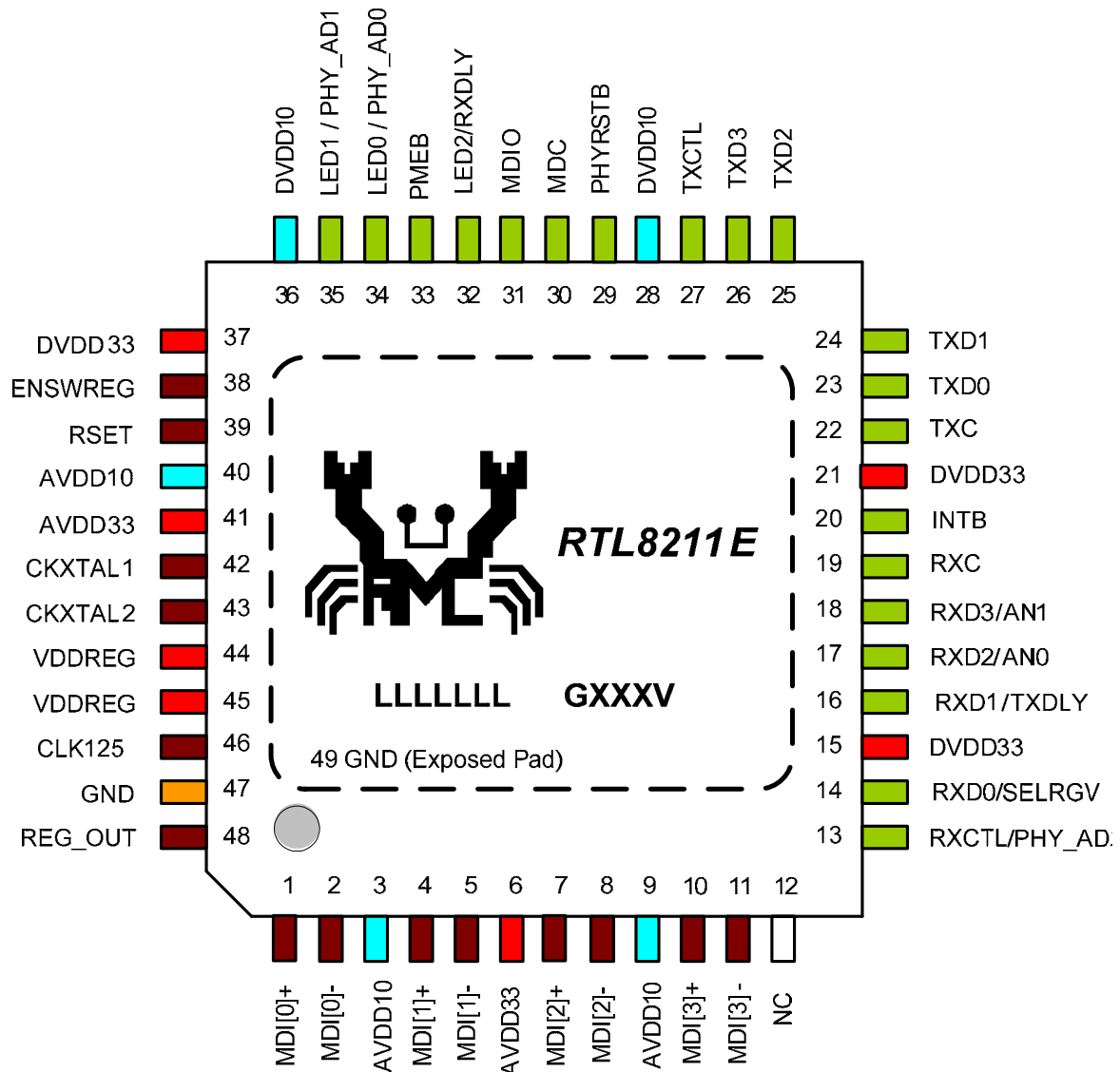


**Figure 5. RTL8211E-VB/RTL8211E-VL Pin Assignments (48-Pin QFN)**

## 5.2. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 5). The version is shown in the location marked 'V'.

# 5.3. RTL8211EG-VB Pin Assignments (64-Pin QFN)
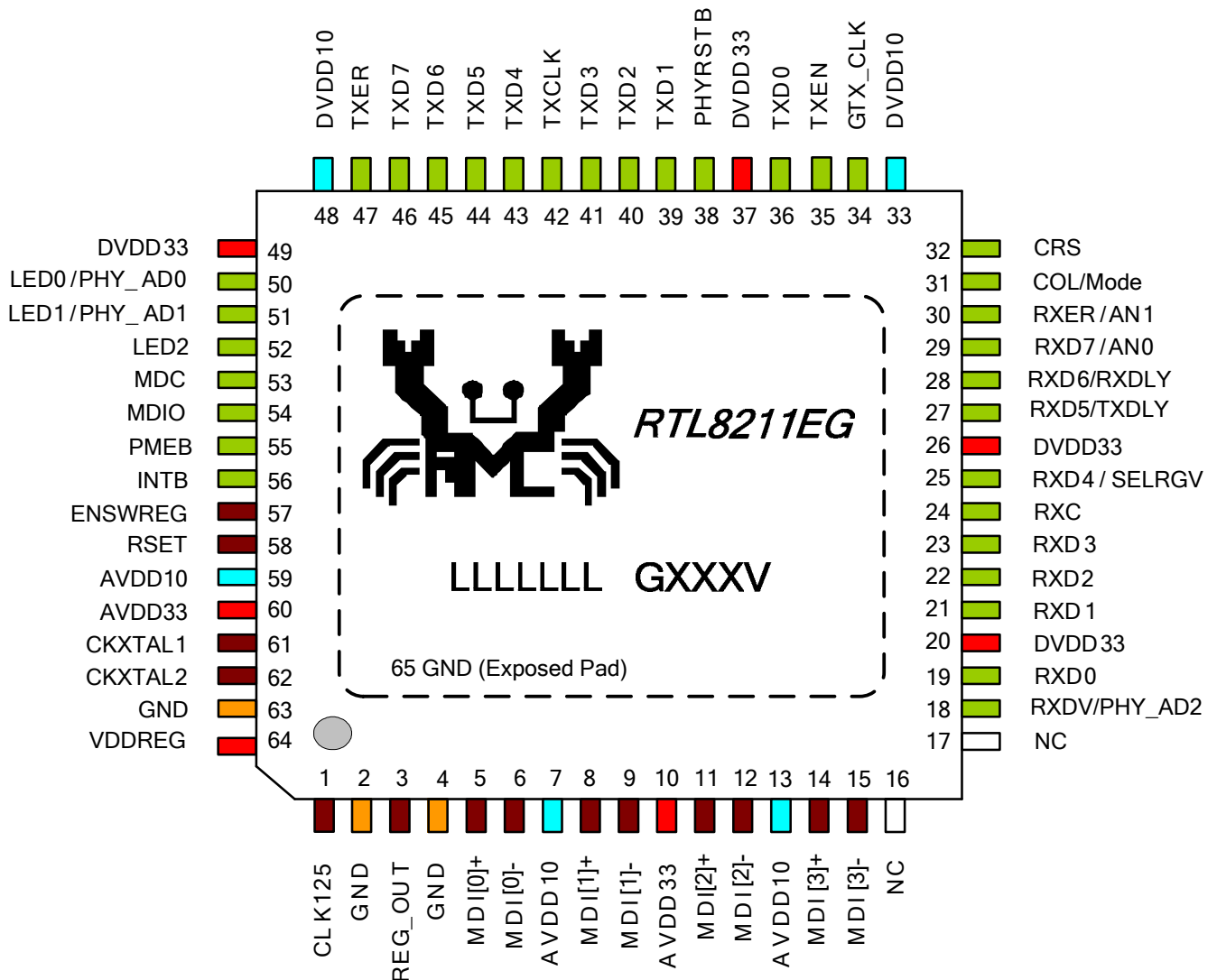


**Figure 6. RTL8211EG-VB Pin Assignments (64-Pin QFN)**

# 5.4. Package Identification

Green package is indicated by the 'G' in GXXXV (Figure 6). The version is shown in the location marked 'V'.

# 6. Pin Descriptions

Some pins have multiple functions. Refer to the Pin Assignments figure on page 6 (RTL8211E-VB/RTL8211E-VL) and page 7 (RTL8211EG-VB) for a graphical representation.

| | | | |
|---|---|---|---|
| I: | Input | LI: | Latched Input During Power up or Reset |
| O: | Output | IO: | Bi-Directional Input and Output |
| P: | Power | PD: | Internal Pull Down During Power On Reset |
| PU: | Internal Pull Up During Power On Reset | OD: | Open Drain |
| G: | Ground | | |

## 6.1. Transceiver Interface

**Table 1. Transceiver Interface**

| Pin No. (48-pin) | Pin No. (64-pin) | Pin Name | Type | Description |
|---|---|---|---|---|
| 1 | 5 | MDI[0]+ | IO | In MDI mode, this is the first pair in 1000Base-T, i.e., the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. |
| 2 | 6 | MDI[0]– | IO | In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. |
| 4 | 8 | MDI[1]+ | IO | In MDI mode, this is the second pair in 1000Base-T, i.e., the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. |
| 5 | 9 | MDI[1]– | IO | In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. |
| 7 | 11 | MDI[2]+ | IO | In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair. |
| 8 | 12 | MDI[2]– | IO | In MDI crossover mode, this pair acts as the BI_DD+/- pair. |
| 10 | 14 | MDI[3]+ | IO | In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair. |
| 11 | 15 | MDI[3]– | IO | In MDI crossover mode, this pair acts as the BI_DC+/- pair. |

## 6.2. Clock

**Table 2. Clock**

| Pin No. (48-pin) | Pin No. (64-pin) | Pin Name | Type | Description |
|---|---|---|---|---|
| 42 | 61 | CKXTAL1 | I | 25/50MHz Crystal Input. If a 25/50MHz oscillator is used, connect CKXTAL1 to the oscillator's output (see section 10.3, page 57 for clock source specifications). |
| 43 | 62 | CKXTAL2 | O | 25/50MHz Crystal Output. Connect to GND if an external 25/50MHz oscillator drives CKXTAL1. |
| 46 | 1 | CLK125 | O/PD | 125MHz Reference Clock Generated from Internal PLL. This pin should be kept floating if the 125MHz clock is not used by MAC. |

*Note: To conduct crystal ppm measurement for models transiting from the RTL8211D to the RTL8211E, the design of the external circuit must be modified, i.e. the output resistor should be connected to CKXTAL1 rather than CKXTAL2.*

## 6.3. RGMII

**Table 3.   RGMII**

| Pin No. (48-pin) | Pin No. (64-pin) | Pin Name | Type (48-pin) | Type (64-pin) | Description |
|---|---|---|---|---|---|
| 22 | - | TXC | I/PU | | The transmit reference clock will be 125MHz, 25MHz, or 2.5MHz depending on speed. |
| - | 34 | GTX_CLK | I | | |
| 23 | 36 | TXD0 | I/PD | | Transmit Data. |
| 24 | 39 | TXD1 | I/PD | | Data is transmitted from MAC to PHY via TXD[3:0]. |
| 25 | 40 | TXD2 | I/PD | | |
| 26 | 41 | TXD3 | I/PU | | |
| 27 | - | TXCTL | I | | Receive Control Signal from the MAC. |
| - | 35 | TXEN | | | |
| 19 | 24 | RXC | O | | The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz, and is derived from the received data stream. |
| 14 | 19 | RXD0 | O/LI/PU | O | Receive Data. |
| 16 | 21 | RXD1 | O/LI/PD | O | Data is transmitted from PHY to MAC via RXD[3:0]. |
| 17 | 22 | RXD2 | O/LI/PU | O | |
| 18 | 23 | RXD3 | O/LI/PU | O | |
| 13 | - | RXCTL | O/LI/PD | | Transmit Control Signal to the MAC. |
| - | 18 | RXDV | | | |
| 16 | 27 | TXDLY | O/LI/PD | | RGMII Transmit Clock Timing Control. 1: Add 2ns delay to TXC for TXD latching |
| 32 | 28 | RXDLY | O/LI/PD | | RGMII Receiver Clock Timing Control. 1: Add 2ns delay to RXC for RXD latching |

## 6.4. GMII (RTL8211EG-VB Only)

**Table 4.   GMII (RTL8211EG-VB Only)**

| Pin No. (48-pin) | Pin No. (64-pin) | Pin Name | Type | Description |
|---|---|---|---|---|
| - | 34 | GTX_CLK | I | The transmit reference clock is 125MHz. |
| - | 42 | TXCLK | O | The transmit reference clock will be 25MHz, or 2.5MHz depending on speed. |
| - | 36 | TXD0 | I | Transmit Data. |
| - | 39 | TXD1 | I | Data is transmitted from MAC to PHY via TXD[7:0]. |
| - | 40 | TXD2 | I | |
| - | 41 | TXD3 | I | |
| - | 43 | TXD4 | I | |
| - | 44 | TXD5 | I | |
| - | 45 | TXD6 | I | |
| - | 46 | TXD7 | I | |
| - | 35 | TXEN | I | Transmit Enable. |

| Pin No. (48-pin) | Pin No. (64-pin) | Pin Name | Type | Description |
|---|---|---|---|---|
| - | 47 | TXER | I | Transmit Error. When both TXER and TXEN are asserted, the transmit error symbol is transmitted onto the cable. When TXER is asserted and TXEN is de-asserted, the carrier extension symbol is transmitted onto the cable. Connect to GND if MAC does not have a TXER pin. |
| - | 24 | RXC | O | The continuous receive reference clock will be 125MHz, 25MHz, or 2.5MHz. It is derived from the received data stream. |
| - | 19 | RXD0 | O | Receive Data. Data is transmitted from PHY to MAC via RXD[7:0]. |
| - | 21 | RXD1 | O | |
| - | 22 | RXD2 | O | |
| - | 23 | RXD3 | O | |
| - | 25 | RXD4 | O/LI/PU | |
| - | 27 | RXD5 | O/LI/PD | |
| - | 28 | RXD6 | O/LI/PD | |
| - | 29 | RXD7 | O/LI/PU | |
| - | 18 | RXDV | O/LI/PD | Receive Data Valid. |
| - | 30 | RXER | O/LI/PU | Receive Error. When both RXER and RXDV are asserted, an error symbol is received from the cable. When RXER is asserted and RXDV is de-asserted, it means false carrier or carrier extension symbol is detected on the cable. |
| - | 31 | COL/Mode | O/LI/PD | Collision In Half Duplex Mode. |
| - | 32 | CRS | O/PD | Carrier Sense. |

# 6.5. Management Interface

**Table 5. Management Interface**

| Pin No. (48-pin) | Pin No. (64-pin) | Pin Name | Type | Description |
|---|---|---|---|---|
| 30 | 53 | MDC | I/PU | Management Data Clock. |
| 31 | 54 | MDIO | IO/PU | Input/Output of Management Data. Pull up 3.3V for 3.3V RGMII (RTL8211E/EG-VB) & GMII (RTL8211EG-VB). Pull up 2.5V for 2.5V RGMII (RTL8211E/EG-VB) & GMII (RTL8211EG-VB). Pull up 1.5/1.8V for 1.5/1.8V RGMII (RTL8211E-VL). |
| 33 | 55 | PMEB | O/OD | Power Management Event (supports 3.3V and 5V pull up). Set low if received a magic packet or wake up frame; active low. This pin will be kept floating if this function is not used. |
| 20 | 56 | INTB | O/OD | Interrupt. Set low if status changed; active low. This pin should be kept floating if this function is not used. |

## 6.6. Reset

**Table 6.   Reset**

| Pin No. (48-pin) | Pin No. (64-pin) | Pin Name | Type | Description |
|---|---|---|---|---|
| 29 | 38 | PHYRSTB | I | Hardware Reset. Active low. For a complete PHY reset, this pin must be asserted low for at least 10ms. All registers will be cleared after a hardware reset. |

## 6.7. Mode Selection

**Table 7.   Mode Selection**

| Pin No. (48-pin) | Pin No. (64-pin) | Pin Name | Type (48-pin) | Type (64-pin) | Description |
|---|---|---|---|---|---|
| 34 | 50 | PHY_AD0 | O/LI/PU | | PHY Address Configuration. |
| 35 | 51 | PHY_AD1 | O/LI/PD | | |
| 13 | 18 | PHY_AD2 | O/LI/PD | | |
| 17 | 29 | AN0 | O/LI/PU | | Auto-Negotiation (NWay) Configuration. |
| 18 | 30 | AN1 | O/LI/PU | | |
| - | 31 | COL/Mode | - | O/LI/PD | RGMII/GMII Mode Configuration. Pull Up for RGMII. Pull Down for GMII. |
| 14 | 25 | SELRGV | O/LI/PU | | Pull Up for 3.3V RGMII (RTL8211E/EG-VB) & GMII (RTL8211EG-VB). Pull Down for 2.5V RGMII (RTL8211E/EG-VB) & GMII (RTL8211EG-VB). Pull Up for 1.5/1.8V RGMII (RTL8211E-VL). *Note: For theRTL8211E-VL, SELRGV should not be Pulled Down.* |

*Note: See section 7.7 Hardware Configuration, page 16 for details.*

## 6.8. LED Default Settings

**Table 8.   LED Default Settings**

| Pin No. (48-pin) | Pin No. (64-pin) | Pin Name | Type | Description |
|---|---|---|---|---|
| 34 | 50 | LED0 | O/LI/PU | Blinking=Transmitting or Receiving. |
| 35 | 51 | LED1 | O/LI/PD | Low=Link Up (Any speed) High=Link Down (Any speed) *Note: High/Low active depends on hardware configuration setting.* |
| 32 | 52 | LED2 | O/LI/PD | No default setting. See Table 19 LED Configuration Table, page 28 for configuration details. |

*Note: See section 7.13 LED Configuration, page 27 for details.*

## 6.9. Regulator and Reference

**Table 9.   Regulator and Reference**

| Pin No. (48-pin) | Pin No. (64-pin) | Pin Name | Type | Description |
|---|---|---|---|---|
| 39 | 58 | RSET | O | Reference. External Resistor Reference. |
| 44, 45 | 64 | VDDREG | P | Analog 3.3V Power Supply for Switching Regulator. |
| 48 | 3 | REG_OUT | O | Switching Regulator 1.05V Output. Connect to a 2.2µH or 4.7µH inductor. |
| 3 | 7 | AVDD10 | P | Feedback Pin for Switching Regulator. |
| 38 | 57 | ENSWREG | I | 3.3V: Enable switching regulator 0V: Disable switching regulator |

## 6.10. Power and Ground

**Table 10. Power and Ground**

| Pin No. (48-pin) | Pin No. (64-pin) | Pin Name | Type | Description |
|---|---|---|---|---|
| 37 | 49 | DVDD33 | P | Digital Power 3.3V. |
| 15, 21 | 20, 26, 37 | DVDD33 | P | Digital IO Power (3.3/2.5/1.8/1.5V) Connect to 3.3V for 3.3V RGMII I/O (RTL8211E/EG-VB) & GMII I/O (RTL8211EG-VB). Connect to 2.5V for 2.5V RGMII I/O (RTL8211E/EG-VB) & GMII I/O (RTL8211EG-VB). Connect to 1.5/1.8V for 1.5/1.8V RGMII I/O (RTL8211E-VL). |
| 28, 36 | 33, 48 | DVDD10 | P | Digital Power. 1.05V. |
| 6, 41 | 10, 60 | AVDD33 | P | Analog Power. 3.3V. |
| 44,45 | 64 | VDDREG | P | Analog 3.3V Power Supply for Switching Regulator. |
| 3, 9, 40 | 7, 13, 59 | AVDD10 | P | Analog Power. 1.05V. |
| 47 | 2, 4, 63 | GND | G | Ground. Exposed Pad (E-Pad) is Analog and Digital Ground (see section 11 Mechanical Dimensions, page 66). |

## 6.11. Not Connected

**Table 11. Not Connected**

| Pin No. (48-pin) | Pin No. (64-pin) | Pin Name | Type | Description |
|---|---|---|---|---|
| 12 | 16, 17 | NC | - | Not Connected. |

# 7. Function Description

## 7.1. Transmitter

### 7.1.1. RGMII/GMII (1000Mbps) Mode

The RTL8211E-VB(VL)/RTL8211EG-VB's PCS layer receives data bytes from the MAC through the RGMII/GMII interface and performs generation of continuous code-groups through 4D-PAM5 coding technology. These code groups are passed through a waveform-shaping filter to minimize EMI effect, and are transmitted onto the 4-pair CAT.5 cable at 125MBaud/s through a D/A converter.

### 7.1.2. MII (100Mbps) Mode

The transmitted 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 25MHz (TXCLK), are converted into 5B symbol code through 4B/5B coding technology, then through scrambling and serializing, are converted to 125MHz NRZ and NRZI signals. The NRZI signals are passed to the MLT3 encoder, then to the D/A converter and transmitted onto the media.

### 7.1.3. MII (10Mbps) Mode

The transmit 4-bit nibbles (TXD[3:0]) from the MAC, clocked at 2.5MHz (TXCLK), are serialized into 10Mbps serial data. The 10Mbps serial data is converted into a Manchester-encoded data stream and is transmitted onto the media by the D/A converter.

## 7.2. Receiver

### 7.2.1. RGMII/GMII (1000Mbps) Mode

Input signals from the media first pass through the on-chip sophisticated hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is processed with state-of-the-art technology, such as adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the RGMII/GMII interface at a clock speed of 125MHz. The Rx MAC retrieves the packet data from the receive RGMII/GMII interface and sends it to the Rx Buffer Manager.

### 7.2.2. MII (100Mbps) Mode

The MLT3 signal is processed with an ADC, equalizer, BLW (Baseline Wander) correction, timing recovery, MLT3 and NRZI decoder, descrambler, 4B/5B decoder, and is then presented to the MII interface in 4-bit-wide nibbles at a clock speed of 25MHz.

## 7.2.3. MII (10Mbps) Mode

The received differential signal is converted into a Manchester-encoded stream. The stream is processed with a Manchester decoder, and is de-serialized into 4-bit-wide nibbles. The 4-bit nibbles are presented to the MII interface at a clock speed of 2.5MHz.

# 7.3. Energy Efficient Ethernet (EEE)

The RTL8211E-VB(VL)/RTL8211EG-VB supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE), at 10Mbps, 100Mbps, and 1000Mbps. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported.

Refer to http://www.ieee802.org/3/az/index.html for more details.

# 7.4. Wake-On-LAN (WOL)

The RTL8211E-VB(VL)/RTL8211EG-VB can monitor the network for a Wakeup Frame or a Magic Packet, and notify the system via the PMEB (Power Management Event; 'B' means low active) pin when such a packet or event occurs. The system can then be restored to a normal state to process incoming jobs. The PMEB pin needs to be connected with a 4.7k-ohm resistor and pulled up to 3.3V or 5V. When the Wakeup Frame or a Magic Packet is sent to the PHY, the PMEB pin will be set low to notify the system to wake up. Refer to the WOL application note for details.

Magic Packet Wakeup occurs only when the following conditions are met:

- The destination address of the received Magic Packet is acceptable to the RTL8211E-VB(VL)/RTL8211EG-VB, e.g., a broadcast, multicast, or unicast packet addressed to the current RTL8211E-VB(VL)/RTL8211EG-VB.

- The received Magic Packet does not contain a CRC error.

- The Magic Packet pattern matches; i.e., 6 * FFh + MISC (can be none) + 16 * DID (Destination ID) in any part of a valid Ethernet packet.

A Wakeup Frame event occurs only when the following conditions are met:

- The destination address of the received Wakeup Frame is acceptable to the RTL8211E-VB(VL)/RTL8211EG-VB, e.g., a broadcast, multicast, or unicast address to the current RTL8211E-VB(VL)/RTL8211EG-VB.

- The received Wakeup Frame does not contain a CRC error.

- The 16-bit CRC* of the received Wakeup Frame matches the 16-bit CRC of the sample Wakeup Frame pattern given by the local machine's OS. Or, the RTL8211E-VB(VL)/RTL8211EG-VB is configured to allow direct packet wakeup, e.g., a broadcast, multicast, or unicast network packet.

*Note: 16-bit CRC: The RTL8211E-VB(VL)/RTL8211EG-VB supports eight long wakeup frames (covering 128 mask bytes from offset 0 to 127 of any incoming network packet). CRC16 polynomial=$x^{16}+x^{12}+x^5+1$.*

# 7.5. Interrupt

Whenever there is a status change on the media detected by the RTL8211E-VB(VL)/RTL8211EG-VB, they will drive the interrupt pin (INTB) low to issue an interrupt event. The MAC senses the status change and accesses the registers (Page 0, Register 19) through the MDC/MDIO interface in response.

Once these status registers (Page 0, Register 19) have been read by the MAC through the MDC/MDIO, the INTB is de-asserted. The RTL8211E-VB(VL)/RTL8211EG-VB interrupt function removes the need for continuous polling through the MDC/MDIO management interface.

# 7.6. MDI Interface

This interface consists of four signal pairs; MDI0, MDI1, MDI2, and MDI3. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors to reduce BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

# 7.7. Hardware Configuration

The operation speed, interface mode, and PHY address can be set by the CONFIG pins. The respective value mapping of CONFIG with the configurable vector is listed in Table 12. To set the CONFIG pins, an external pull-high or pull-low via resistor is required.

**Table 12. CONFIG Pins vs. Configuration Register**

| RTL8211E-VB(VL) Pin | RTL8211EG-VB Pin | Pin Name |
|---|---|---|
| LED0 | LED0 | PHYAD[0] |
| LED1 | LED1 | PHYAD[1] |
| RXCTL | RXDV | PHYAD[2] |
| RXD2 | RXD7 | AN[0] |
| RXD3 | RXER | AN[1] |
| - | COL | Mode |
| LED2 | RXD6 | RX Delay |
| RXD1 | RXD5 | TX Delay |
| RXD0 | RXD4 | SELRGV |

**Table 13. Configuration Register Definitions**

| Configuration | Description |
|---|---|
| PHYAD[2:0] | PHY Address.<br>PHYAD sets the PHY address for the device. The RTL8211E-VB(VL)/RTL8211EG-VB support PHY addresses from 00001 to 00111. PHY address 0 is a broadcast from the MAC; each PHY device should respond.<br>*Note: PHYAD[2:0]=000 can support all PHY addresses. It can automatically remember the first non-zero PHY address.* |
| AN[1:0] | Auto-Negotiation (NWay) Configuration.<br>AN[1:0] controls the Auto-Negotiation speed and duplex settings.<br>00: 10Base-T Full/Half Duplex<br>01: 100Base-TX Half Duplex; 10Base-T Full/Half Duplex<br>10: 100Base-TX Full/Half Duplex; 10Base-T Full/Half Duplex<br>11: NWay. Advertise all capabilities (10/1000Base-T; 100Base-TX Full/Half Duplex) |
| Mode | Interface Mode Select.<br>0: MII/GMII (via 4.7k-ohm to GND)<br>1: RGMII (via 4.7k-ohm to 3.3V)<br>*Note: 'Mode' specifies the RTL8211EG-VB operating mode.* |
| RX Delay | RGMII Transmit Clock Timing Control.<br>1: Add 2ns delay to RXC for RXD latching (via 4.7k-ohm to 3.3V)<br>0: No delay (via 4.7k-ohm to GND) |
| TX Delay | RGMII Transmit Clock Timing Control.<br>1: Add 2ns delay to TXC for TXD latching (via 4.7k-ohm to 3.3V)<br>0: No delay (via 4.7k-ohm to GND) |
| SELRGV | 3.3V or 2.5V RGMII/GMII Selection.<br>1: 3.3V RGMII/GMII (RTL8211E-VB & RTL8211EG-VB)<br>   1.5/1.8V RGMII (RTL8211E-VL)<br>0: 2.5V RGMII/GMII (RTL8211E-VB & RTL8211EG-VB)<br>*Note: For the RTL8211E-VL, SELRGV should not be pulled down.* |

# 7.8. *LED and PHY Address Configuration*

In order to reduce the pin count on the RTL8211E-VB(VL)/RTL8211EG-VB, the LED pins are duplexed with the PHY address pins. As the PHYAD strap options share the LED output pins, the external combinations required for strapping and LED usage must be considered in order to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding PHYAD input upon power-up/reset. For example, as Figure 7 (left-side) shows, if a given PHYAD input is resistively pulled high then the corresponding output will be configured as an active low driver. On the right side, we can see that if a given PHYAD input is resistively pulled low then the corresponding output will be configured as an active high driver. The PHY address configuration pins should not be connected to GND or VCC directly, but must be pulled high or low through a resistor (e.g., 4.7KΩ). If no LED indications are needed, the components of the LED path (LED+510Ω) can be removed.



PHY Address[:]=Logical 1  PHY Address[:]=Logical 0
RXDLY=Logical 1           RXDLY=Logical 0
LED Indication=Active low  LED Indication=Active High
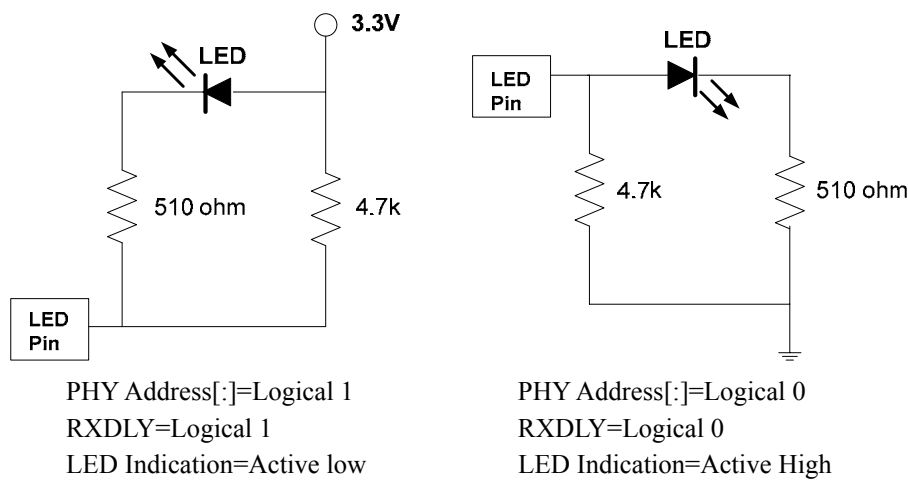
**Figure 7.   LED and PHY Address Configuration**

# 7.9. *Green Ethernet (1000/100Mbps Mode Only)*

## 7.9.1. Cable Length Power Saving

In 1000/100Mbps mode the RTL8211E-VB(VL)/RTL8211EG-VB provides dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides intermediate performance with minimum power consumption.

## 7.9.2. Register Setting

**Follow the register settings below to disable Green Ethernet (Default is 'Enabled')**

Write Reg31, Data=0x0003 (page3)

Write Reg25, Data=0x3246

Write Reg16, Data=0xa87c

Write Reg31, Data=0x0000 (page0)

**Follow the register settings below to enable Green Ethernet (Default is 'Enabled')**

Write Reg31, Data=0x0003 (page3)

Write Reg25, Data=0x3247

Write Reg16, Data=0xac7c

Write Reg31, Data=0x0000 (page0)

# 7.10. MAC/PHY Interface

The RTL8211E-VB/RTL8211E-VL supports industry standards and is suitable for most off-the-shelf MACs with an RGMII interface.

The RTL8211EG-VB supports industry standards and is suitable for most off-the-shelf MACs with GMII and RGMII interfaces.

## 7.10.1. MII

In 100Base-TX and 10Base-T modes (MII mode is selected), TXC and RXC sources are 25MHz and 2.5MHz respectively. TXC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for data transitions.

## 7.10.2. GMII

In 1000Base-T mode (GMII interface is selected), a 125MHz transmit clock is expected on GTX_CLK. RXCLK sources the 125MHz receive clock.

## 7.10.3. RGMII

In 1000Base-T mode (RGMII interface is selected), TXC and RXC sources are 125MHz. TXC will always be generated by the MAC and RXC will always be generated by the PHY. TXD[3:0] and RXD[3:0] signals are used for data transitions on the rising and falling edge of the clock.

## 7.10.4. Management Interface

The management interface provides access to the internal registers through the MDC and MDIO pins as described in IEEE 802.3u section 22. The MDC signal, provided by the MAC, is the management data clock reference to the MDIO signal. The MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC. The MDIO pin needs a 1.5k Ohm pull-up resistor to maintain the MDIO high during idle and turnaround.

Preamble suppression is the default setting of the RTL8211E-VB(VL)/RTL8211EG-VB after power-on. However, there still must be at least one idle bit between operations.

If the MDC clock will be stopped after the read/write operation, the clock must be kept toggling for at least seven clock cycles with the MDIO high before entering the IDLE state.

The RTL8211E-VB(VL)/RTL8211EG-VB can share the same MDIO line. In switch/router applications, each port should be assigned a unique address during the hardware reset sequence, and it can only be addressed via that unique PHY address. For detailed information on the RTL8211E-VB(VL)/ RTL8211EG-VB management registers, see section 8 Register Descriptions, page 30.

**Table 14. Management Frame Format**

| | Management Frame Fields | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **Preamble** | **ST** | **OP** | **PHYAD** | **REGAD** | **TA** | **DATA** | **IDLE** |
| Read | 1…1 | 01 | 10 | AAAAA | RRRRR | Z0 | DDDDDDDDDDDDDDDD | Z |
| Write | 1…1 | 01 | 01 | AAAAA | RRRRR | 10 | DDDDDDDDDDDDDDDD | Z |

**Table 15. Management Frame Description**

| Name | Description |
|---|---|
| Preamble | 32 Contiguous Logical 1's Sent by the MAC on MDIO, along with 32 Corresponding Cycles on MDC. This provides synchronization for the PHY. |
| ST | Start of Frame. Indicated by a 01 pattern. |
| OP | Operation Code. Read: 10 Write: 01 |
| PHYAD | PHY Address. Up to eight PHYs can be connected to one MAC. This 3-bit field selects which PHY the frame is directed to. |
| REGAD | Register Address. This is a 5-bit field that sets which of the 32 registers of the PHY this operation refers to. |
| TA | Turnaround. This is a 2-bit-time spacing between the register address and the data field of a frame to avoid contention during a read transaction. For a read transaction, both the STA and the PHY remain in a high-impedance state for the first bit time of the turnaround. The PHY drives a zero bit during the second bit time of the turnaround of a read transaction. |
| DATA | Data. These are the 16 bits of data. |
| IDLE | Idle Condition. Not truly part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logical '1'. |
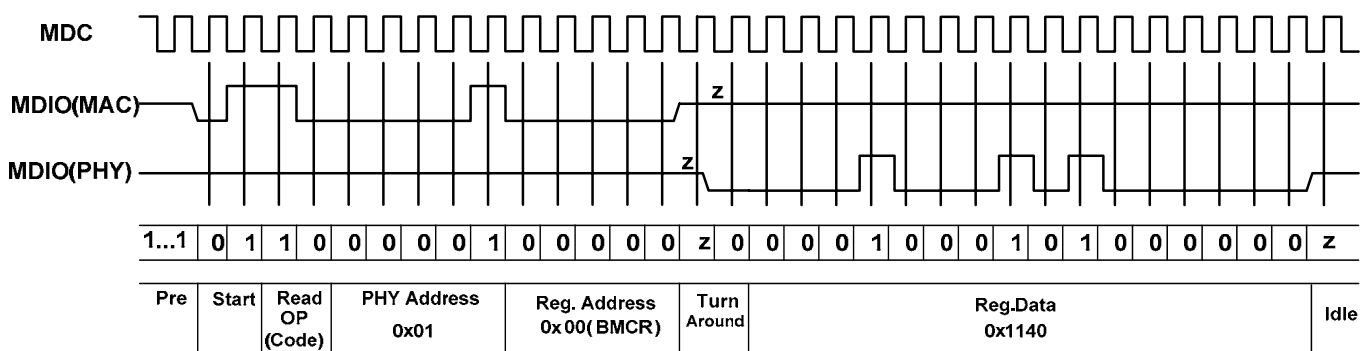


**Figure 8.  MDC/MDIO Read Timing**

| Pre | Start | Write OP (Code) | PHY Address 0x01 | Reg. Address 0x00(BMCR) | Turn Around | Reg. Data 0x1340 | Idle |
|-----|-------|-----------------|------------------|-------------------------|-------------|------------------|------|
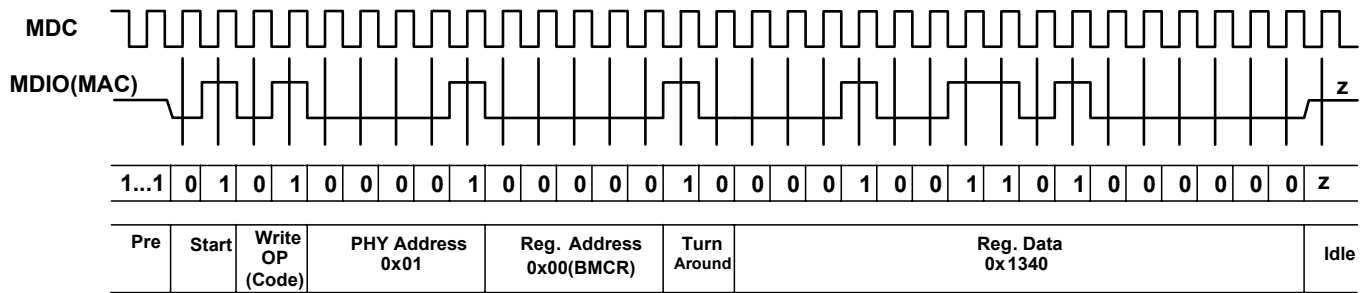
**Figure 9.   MDC/MDIO Write Timing**

# 7.10.5.    Access to Extension Page (ExtPage)

Set MDIO commands as shown below to switch to the Extension Page (ExtPage) 0xXY (in Hex).

1. Write Register 31 Data=0x0007 (set to Extension Page)

2. Write Register 30 Data=0x00XY (Extension Page XY)

3. Write the target Register Data

4. Write Register 31 Data=0x0000 (switch to Page 0)

# 7.10.6.    Access to MDIO Manageable Device (MMD)

The MDIO Manageable Device (MMD) is an extension to the management interface that provides the ability to access more device registers while still retaining logical compatibility with the MDIO interface, defined in section 8.1 Register Mapping and Definitions, page 30. Access to MMD configuration is provided via Registers 13 and 14.

**MMD Read/Write Operation**

1. Write Function field to 00 (address mode) and DEVAD field to the device address value for the desired MMD (Register 13).

2. Write the desired address value to the MMD's address register (Register 14).

3. Write Function field to 01 (data mode; no post increment) and DEVAD field to the same device address for the desired MMD (Register 13).

4. Read: Go to step 5. Write: Go to step 6.

5. Read the content of the selected register in MMD (Register 14).

6. Write the content of the selected register in MMD (Register 14).

# 7.11. Auto-Negotiation

Auto-Negotiation is a mechanism to determine the fastest connection between two link partners. For copper media applications, it was introduced in IEEE 802.3u for Ethernet and Fast Ethernet, and then in IEEE 802.3ab to address extended functions for Gigabit Ethernet. It performs the following:

- Auto-Negotiation Priority Resolution

- Auto-Negotiation Master/Slave Resolution

- Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution

- Crossover Detection & Auto-Correction Resolution

Upon de-assertion of a hardware reset, the RTL8211E-VB(VL)/RTL8211EG-VB can be configured to have auto-negotiation enabled, or be set to operate in 10Base-T, 100Base-TX, or 1000Base-T mode via the CONFIG pins (see section 7.7 Hardware Configuration, page 16).

The auto-negotiation process is initiated automatically upon any of the following:

- Power-up

- Hardware reset

- Software reset (register 0.15)

- Restart auto-negotiation (register 0.9)

- Transition from power down to power up (register 0.11)

- Entering the link fail state

**Table 16. 1000Base-T Base and Next Page Bit Assignments**

| Bit | Name | Bit Description | Register Location |
|-----|------|-----------------|-------------------|
| | | **Base Page** | |
| D15 | NP | Next Page.<br>1: Indicates that Next Pages follow<br>0: Indicates that no Next Pages follow | - |
| D14 | Ack | Acknowledge.<br>1: Indicates that a device has successfully received its link partner's Link Code Word (LCW) | - |
| D13 | RF | Remote Fault.<br>1: Indicates to its link partner that a device has encountered a fault condition | - |
| D[12:5] | A[7:0] | Technology Ability Field.<br>Indicates to its link partner the supported technologies specific to the selector field value. | Register 4.[12:5]<br>Table 28, page 34. |
| D[4:0] | S[4:0] | Selector Field.<br>Always 00001.<br>Indicates to its link partner that it is an IEEE 802.3 device. | Register 4.[4:0]<br>Table 28, page 34. |

| Bit | Name | Bit Description | Register Location |
|---|---|---|---|
| **PAGE 0 (Message Next Page)** | | |
| M15 | NP | Next Page.<br>1: Indicates that Next Pages follow<br>0: Indicates that no Next Pages follow | - |
| M14 | Ack | Acknowledge.<br>1: Indicates that a device has successfully received its link partner's Link Code Word (LCW) | - |
| M13 | MP | Message Page.<br>1: Indicates to its link partner that this is a message page, not an unformatted page. | - |
| M12 | Ack2 | Acknowledge 2.<br>1: Indicates to its link partner that the device has the ability to comply with the message. | - |
| M11 | T | Toggle.<br>Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange. | - |
| M[10:0] | - | 1000Base-T Message Code (Always 8). | - |
| **PAGE 1 (Unformatted Next Page)** | | |
| U15 | NP | Next Page.<br>1: Indicates that Next Pages follow<br>0: Indicates that no Next Pages follow | - |
| U14 | Ack | Acknowledge.<br>1: Indicates that a device has successfully received its link partner's Link Code Word (LCW) | - |
| U13 | MP | Message Page.<br>1: Indicates to its link partner that this is a message page, not an unformatted page. | - |
| U12 | Ack2 | Acknowledge 2.<br>1: Indicates to its link partner that the device has the ability to comply with the message. | - |
| U11 | T | Toggle.<br>Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange. | - |
| U[10:5] | - | Reserved. Transmit as 0 | - |
| U4 | - | 1000Base-T Half Duplex.<br>1: Half duplex          0: No half duplex | - |
| U3 | - | 1000Base-T Full Duplex.<br>1: Full duplex          0: No full duplex | - |
| U2 | - | 1000Base-T Port Type Bit.<br>1: Multi-port device          0: Single-port device | Register 9.10 (GBCR)<br>Table 33, page 37. |
| U1 | - | 1000Base-T Master-Slave Manual Configuration Value.<br>1: Master          0: Slave<br>This bit is ignored if bit 9.12=0 | Register 9.11 (GBCR)<br>Table 33, page 37. |
| U0 | - | 1000Base-T Master-Slave Manual Configuration Enable.<br>1: Manual Configuration Enable<br>This bit is intended to be used for manual selection in Master-Slave mode, and is to be used in conjunction with bit 9.11 | Register 9.12 (GBCR)<br>Table 33, page 37. |

| Bit | Name | Bit Description | Register Location |
|-----|------|----------------|-------------------|
| **PAGE 2 (Unformatted Next Page)** | | | |
| U15 | NP | Next Page.<br>1: Indicates that Next Pages follow<br>0: Indicates that no Next Pages follow | - |
| U14 | Ack | Acknowledge.<br>1: Indicates that a device has successfully received its link partner's Link Code Word (LCW) | - |
| U13 | MP | Message Page.<br>1: Indicates to its link partner that this is a message page, not an unformatted page | - |
| U12 | Ack2 | Acknowledge 2.<br>1: Indicates to its link partner that the device has the ability to comply with the message | - |
| U11 | T | Toggle.<br>Used by the NWay arbitration function to ensure synchronization with its link partner during Next Page exchange. | - |
| U[10:0] | - | 1000Base-T Master-Slave Seed Bit[10:0] | Master-Slave<br>Seed Value SB[10:0] |

# 7.11.1.   Auto-Negotiation Priority Resolution

Upon the start of auto-negotiation, to advertise its capabilities each station transmits a 16-bit packet called a Link Code Word (LCW), within a burst of 17 to 33 Fast Link Pulses (FLP). A device capable of auto-negotiation transmits and receives the FLPs. The receiver must identify three identical LCWs before the information is authenticated and used in the arbitration process. The devices decode the base LCW and select capabilities with the highest common denominator supported by both devices.

To advertise 1000Base-T capability, both link partners, sharing the same link medium, should engage in Next Page (1000Base-T Message Page, Unformatted Page 1, and Unformatted Page 2) exchange.

Auto-negotiation ensures that the highest priority protocol will be selected as the link speed based on the following priorities advertised through the Link Code Word (LCW) exchange. Refer to IEEE 802.3 Clause 28 for detailed information.

1. 1000Base-T Full Duplex (highest priority)

2. 1000Base-T Half Duplex

3. 100Base-TX Full Duplex

4. 100Base-TX Half Duplex

5. 10Base-T Full Duplex

6. 10Base-T Half Duplex (lowest priority)

## 7.11.2.  Auto-Negotiation Master/Slave Resolution

To establish a valid 1000Base-T link, the Master/Slave mode of both link partners should be resolved through the auto-negotiation process:

- Master Priority

  - Multi-port > Single-port
  - Manual > Non-manual

- Determination of Master/Slave configuration from LCW

  - Manual_MASTER=U0*U1
  - Manual_SLAVE=U0*!U1
  - Single-port device=!U0*!U2
  - Multi-port device=!U0*U2
    Where: U0 is bit 0 of the Unformatted Page 1
         U1 is bit 1 of the Unformatted Page 1
         U2 is bit 2 of the Unformatted Page 1

- Where there are two stations with the same configuration, the one with higher Master-Slave seed SB[10:0] in the unformatted page 2 shall become Master.

- Master-Slave configuration process resolution:

  - Successful: Bit 10.15 Master-Slave Configuration Fault is set to logical 0, and bit 10.14 is set to logical 1 for Master resolution, or set to logical 0 for Slave resolution.
  - Unsuccessful: Auto-Negotiation restarts.
  - Fault Detect: Bit 10.15 is set to logical 1 to indicate that a configuration fault has been detected. Auto-Negotiation restarts automatically. This happens when both stations are set to manual Master mode or manual Slave mode, or after seven attempts to configure the Master-Slave relationship through the seed method has failed.

## 7.11.3.  Auto-Negotiation PAUSE/ASYMMETRIC PAUSE Resolution

Auto-negotiation is also used to determine the flow control capability between link partners. Flow control is a mechanism that can force a busy transmitting link partner to stop transmitting in a full duplex environment by sending special MAC control frames. In IEEE 802.3u, a PAUSE control frame had already been defined. However, in IEEE 802.3ab, a new ASY-PAUSE control frame was defined; if the MAC can only generate PAUSE frames but is not able to respond to PAUSE frames generated by the link partner, then it is called ASYMMETRIC PAUSE.

PAUSE/ASYMMETRIC PAUSE capability can be configured by setting the ANAR bits 10 and 11 (Table 28, page 34). Link partner PAUSE capabilities can be determined from ANLPAR bits 10 and 11 (Table 29, page 35). A PHY layer device such as the RTL8211E-VB(VL)/RTL8211EG-VB is not directly involved in PAUSE resolution, but simply advertises and reports PAUSE capabilities during the Auto-Negotiation process. The MAC is responsible for final PAUSE/ASYMMETRIC PAUSE resolution after a link is established, and is responsible for correct flow control actions thereafter.

# 7.12. *Crossover Detection and Auto-Correction*

Ethernet needs a crossover mechanism between both link partners to cross the transmit signal to the receiver when the medium is twisted-pair cable. Crossover Detection & Auto-Correction Configuration eliminates the need for crossover cables between devices, such as two computers connected to each other with a CAT.5 Ethernet cable. The basic concept is to assume the initial default setting is MDI mode, and then check the link status. If no link is established after a certain time, change to MDI Crossover mode and repeat the process until a link is established. An 11-bit pseudo-random timer is applied to decide the mode change time interval.

Crossover Detection & Auto-Correction is not a part of the Auto-Negotiation process, but it utilizes the process to exchange the MDI/MDI Crossover configuration. If the RTL8211E-VB(VL)/RTL8211EG-VB is configured to only operate in 100Base-TX or only in 10Base-T mode, then Auto-Negotiation is disabled only if the Crossover Detection & Auto-Correction function is also disabled. If Crossover Detection & Auto-Correction are enabled, then Auto-Negotiation is enabled and the RTL8211E-VB(VL)/ RTL8211EG-VB advertises only 100Base-TX mode or 10Base-T mode. If the speed of operation is configured manually and Auto-Negotiation is still enabled because the Crossover Detection & Auto-Correction function is enabled, then the duplex advertised is as follows:

1. If CONFIG is set to half duplex, then only half duplex is advertised.

2. If CONFIG is set to full duplex, then both full and half duplex are advertised.

If the user wishes to advertise only full duplex at a particular speed with the Crossover Detection & Auto-Correction function enabled, then Auto-Negotiation should be enabled (register 0.12) with the appropriate advertising capabilities set in registers 4 or 9. The Crossover Detection & Auto-Correction function may be enabled/disabled by setting (register 16.6) manually.

After initial configuration following a hardware reset, Auto-Negotiation can be enabled and disabled via register 0.12, speed via registers 0.13, 0.6, and duplex via register 0.8. The abilities that are advertised can be changed via registers 4 and 9. Changes to registers 0.12, 0.13, 0.6, and 0.8 do not take effect unless at least one of the following events occurs:

- Software reset (register 0.15)

- Restart of Auto-Negotiation (register 0.9)

- Transition from power-down to power-up (register 0.11)

Registers 4 and 9 are internally latched once each time Auto-Negotiation enters the ABILITY DETECT state in the arbitration state machine (IEEE 802.3). Hence a write into register 4 or 9 has no effect once the RTL8211E-VB(VL)/RTL8211EG-VB begins to transmit Fast Link Pulses.

Register 7 is treated in a similar manner as 4 and 9 during additional Next Page exchanges. Once the RTL8211E-VB(VL)/RTL8211EG-VB completes Auto-Negotiation, it updates the various statuses in registers 1, 5, 6, and 10. The speed, duplex, page received, and Auto-Negotiation completed statuses are also available in registers 17 and 19.

# 7.13. LED Configuration

The RTL8211E-VB(VL)/RTL8211EG-VB supports three LED pins, suitable for multiple types of applications that can directly drive the LEDs. The output of these pins is determined by setting the corresponding bits in extension Page44 Register 28 and Register 26. The functionality of the RTL8211E-VB(VL)/RTL8211EG-VB LEDs is shown in Table 17.

**Table 17. LED Default Definitions**

| Pin | Description |
|---|---|
| LED0 | Blinking=Transmitting or Receiving |
| LED1 | Low=Link Up (Any speed) |
| | High=Link Down (Any speed) |
| LED2 | Low=Link Up (Any speed) |
| | High=Link Down (Any speed) |
| | Blinking=Transmitting or Receiving |

*Note 1: When in EEE LED mode (default enabled), blinking duration is 400ms ON and 2 seconds OFF.*

*Note 2: To disable EEE LED mode, set the following registers:*

*a. Write Reg31, Data=0x0005 (page 5).*
*b. Write Reg5, Data=0x8b82.*
*c. Write Reg6, Data=0x052b.*
*d. Write Reg31, Data=0x0000 (page 0).*

The RTL8211E-VB(VL)/RTL8211EG-VB LED pins can be customized from extension Page 44 Register 28 and Register 26. To change the register page, see note (below) and Table 18. There are 16 configuration types (see Table 19, page 28).

*Note: To switch to extension Page44, set Register 31 Data=0x0007 (set to extension page). Set Register 30 Data=0x002c (extension Page44). After LED setting, switch to PHY`s Page0 (Register 31 Data=0000).*

**Table 18. LED Register Table**

| | LINK Speed | | | Active (Tx/Rx) |
|---|---|---|---|---|
| | **10Mbps** | **100Mbps** | **1000Mbps** | |
| LED0 | Reg28 Bit0 | Reg28 Bit1 | Reg28 Bit2 | Reg26 Bit4 |
| LED1 | Reg28 Bit4 | Reg28 Bit5 | Reg28 Bit6 | Reg26 Bit5 |
| LED2 | Reg28 Bit8 | Reg28 Bit9 | Reg28 Bit10 | Reg26 Bit6 |

**Table 19. LED Configuration Table**

| Pin | LINK Bit | | | Active (TX/RX) Bit | Description |
|-----|---|---|---|---|---|
| | 10 | 100 | 1000 | | |
| LED | 0 | 0 | 0 | 0 | N/A |
| | 0 | 0 | 0 | 1 | Active |
| | 0 | 0 | 1 | 0 | Link 1000 |
| | 0 | 0 | 1 | 1 | Link 1000+Active |
| | 0 | 1 | 0 | 0 | Link 100 |
| | 0 | 1 | 0 | 1 | Link 100+Active |
| | 0 | 1 | 1 | 0 | Link 100/1000 |
| | 0 | 1 | 1 | 1 | Link 100/1000+Active |
| | 1 | 0 | 0 | 0 | Link 10 |
| | 1 | 0 | 0 | 1 | Link 10+Active |
| | 1 | 0 | 1 | 0 | Link 10/1000 |
| | 1 | 0 | 1 | 1 | Link 10/1000+Active |
| | 1 | 1 | 0 | 0 | Link 10/100 |
| | 1 | 1 | 0 | 1 | Link 10/100+Active |
| | 1 | 1 | 1 | 0 | Link 10/100/1000 |
| | 1 | 1 | 1 | 1 | Link 10/100/1000+Active |

# 7.14. Polarity Correction

The RTL8211E-VB(VL)/RTL8211EG-VB automatically corrects polarity errors on the receive pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode polarity is irrelevant. In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

## 7.15. *Power*

The RTL8211E-VB(VL)/RTL8211EG-VB implements a voltage regulator to generate operating power. The system vendor needs to supply a 3.3V, 1A steady power source. The RTL8211E-VB(VL)/ RTL8211EG-VB converts the 3.3V steady power source to 1.05V via a switching regulator.

Another possible implementation is to use an external regulator to generate 1.0V. Be sure that the regulator meets the required current rate (0.95V~1.09V).

The RTL8211E-VB(VL)/RTL8211EG-VB implements an option for the RGMII/GMII power pins. The standard I/O voltage of the RGMII/GMII interface is 3.3V, with support for 2.5V to lower EMI. The 2.5V power source for RGMII is from an external regulator.

## 7.16. *PHY Reset (Hardware Reset)*

The RTL8211E-VB(VL)/RTL8211EG-VB has a PHYRSTB pin to reset the chip. For a complete PHY reset, this pin must be asserted low for at least 10ms (Tgap in Figure 10) for the internal regulator. Wait for a further 30ms (for internal circuits settling time) before accessing the PHY register. All registers will return to default values after a hardware reset. Refer to the RTL8211xx-xx_Power_Sequence_App_Note for more detailed information.
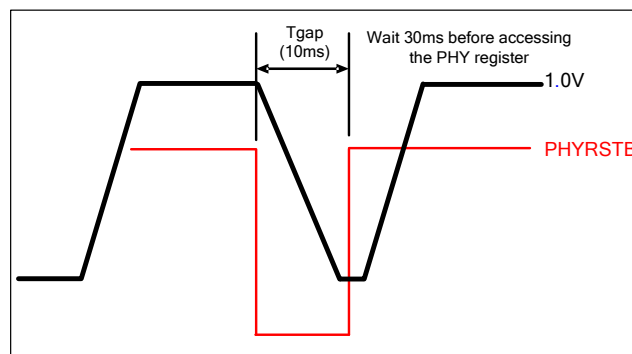


**Figure 10. PHY Reset Timing**

# 8.    Register Descriptions

## 8.1.    Register Mapping and Definitions

**Table 20. Register Access Types**

| Type | Description |
|------|-------------|
| LH | Latch high. If the status is high, this field is set to '1' and remains set. |
| RC | Read-cleared. The register field is cleared after read. |
| RO | Read only. |
| RW | Read and Write |
| SC | Self-cleared. Writing a '1' to this register field causes the function to be activated immediately, and then the field will be automatically cleared to '0' . |

**Table 21. Register Mapping and Definitions**

| Offset | Access | Name | Description |
|--------|--------|------|-------------|
| 0 | RW | BMCR | Basic Mode Control Register. |
| 1 | RO | BMSR | Basic Mode Status Register. |
| 2 | RO | PHYID1 | PHY Identifier Register 1. |
| 3 | RO | PHYID2 | PHY Identifier Register 2. |
| 4 | RW | ANAR | Auto-Negotiation Advertising Register. |
| 5 | RW | ANLPAR | Auto-Negotiation Link Partner Ability Register. |
| 6 | RW | ANER | Auto-Negotiation Expansion Register. |
| 7 | RW | ANNPTR | Auto-Negotiation Next Page Transmit Register. |
| 8 | RW | ANNPRR | Auto-Negotiation Next Page Receive Register. |
| 9 | RW | GBCR | 1000Base-T Control Register. |
| 10 | RO | GBSR | 1000Base-T Status Register. |
| 11~12 | RO | RSVD | Reserved. |
| 13 | WO | MACR | MMD Access Control Register. |
| 14 | RW | MAADR | MMD Access Address Data Register. |
| 15 | RO | GBESR | 1000Base-T Extended Status Register. |
| 16 | RW | PHYCR | PHY Specific Control Register. |
| 17 | RO | PHYSR | PHY Specific Status Register. |
| 18 | RW | INER | Interrupt Enable Register. |
| 19 | RO | INSR | Interrupt Status Register. |
| 20~23 | RW | RSVD | Reserved. |
| 24 | RO | RXERC | Receive Error Counter. |
| 25~26 | RW | RSVD | Reserved. |
| 27 | RO | LDPSR | Link Down Power Saving Register. |
| 28 | RO | RSVD | Reserved. |
| 29 | RW | RSVD | Reserved. |
| 30 | RW | EPAGSR | Extension Page Select Register. |
| 31 | RW | PAGSEL | Page Select Register. |

*Note: To switch to extension Page44, set Register 31 Data=0x0007 (set to extension page). Set Register 30 Data=0x002c (extension Page44). After LED setting, switch to the PHY's Page0 (Register 31 Data=0000).*

## 8.2. MMD Register Mapping and Definition

**Table 22. MMD Register Mapping and Definition**

| Device | Offset | Access | Name | Description |
|--------|--------|--------|--------|-------------|
| 3 | 0 | RW | PC1R | PCS Control 1 Register. |
| 3 | 1 | RW | PS1R | PCS Status 1 Register. |
| 3 | 20 | RO | EEECR | EEE Capability Register. |
| 3 | 22 | RC | EEEWER | EEE Wake Error Register. |
| 7 | 60 | RW | EEEAR | EEE Advertisement Register. |
| 7 | 61 | RO | EEELPAR | EEE Link Partner Ability Register. |

## 8.3. ExtPage Register Mapping and Definition

**Table 23. ExtPage Register Mapping and Definition**

| ExtPage | Offset | Access | Name | Description |
|---------|--------|--------|------|-------------|
| 44 | 26 | RW | LACR | LED Action Control Register. |
| 44 | 28 | RW | LCR | LED Control Register. |
| 45 | 24 | RW | ACCR | Auto-Crossover Control Register. |
| 160 | 26 | RW | SCR | SSC Control Register. |

## 8.4. Register Tables

## 8.4.1. BMCR (Basic Mode Control Register, Address 0x00)

**Table 24. BMCR (Basic Mode Control Register, Address 0x00)**

| Bit | Name | Type | Default | Description |
|-----|------|------|---------|-------------|
| 0.15 | Reset | RW, SC | 0 | Reset.<br>1: PHY reset<br>0: Normal operation<br>Register 0 (BMCR) and register 1 (BMSR) will return to default values after a software reset (set Bit15 to 1).<br>This action may change the internal PHY state and the state of the physical link associated with the PHY. |
| 0.14 | Loopback | RW | 0 | Loopback Mode.<br>1: Enable PCS loopback mode<br>0: Disable PCS loopback mode |

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 0.13 | Speed[0] | RW | 0 | Speed Select Bit 0.<br>In forced mode, i.e., when Auto-Negotiation is disabled, bits 6 and 13 determine device speed selection.<br><table><tr><td>Speed[1]</td><td>Speed[0]</td><td>Speed Enabled</td></tr><tr><td>1</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>Reserved</td></tr><tr><td>0</td><td>1</td><td>100Mbps</td></tr><tr><td>0</td><td>0</td><td>10Mbps</td></tr></table> |
| 0.12 | ANE | RW | 1 | Auto-Negotiation Enable.<br>1: Enable Auto-Negotiation<br>0: Disable Auto-Negotiation |
| 0.11 | PWD | RW | 0 | Power Down.<br>1: Power down (only Management Interface and logic are active; link is down)<br>0: Normal operation |
| 0.10 | Isolate | RW | 0 | Isolate.<br>1: RGMII/GMII interface is isolated; the serial management interface (MDC, MDIO) is still active. When this bit is asserted, the RTL8211E-VB(VL)/RTL8211EG-VB ignores TXD[7:0], and TXCTL inputs, and presents a high impedance on TXC, RXC, RXCTL, RXD[7:0].<br>0: Normal operation |
| 0.9 | Restart_AN | RW, SC | 0 | Restart Auto-Negotiation.<br>1: Restart Auto-Negotiation<br>0: Normal operation |
| 0.8 | Duplex | RW | 1 | Duplex Mode.<br>1: Full Duplex operation<br>0: Half Duplex operation<br>This bit is valid only in force mode, i.e., NWay is disabled. |
| 0.7 | Collision Test | RW | 0 | Collision Test.<br>1: Collision test enabled<br>0: Normal operation |
| 0.6 | Speed[1] | RW | 1 | Speed Select Bit 1.<br>Refer to bit 0.13. |
| 0.5:0 | RSVD | RO | 000000 | Reserved. |

*Note 1: The power-on duplex, speed, and ANE values take on the values set by external pins AN[1:0] on hardware reset only. A write to these registers has no effect unless any one of the following also occurs: Software reset (0.15) is asserted, Restart_AN (0.9) is asserted, or PWD (0.11) transitions from power down to normal operation.*

*Note 2: When the RTL8211E-VB(VL)/RTL8211EG-VB is switched from power down to normal operation, a software reset and restart auto-negotiation is performed, even if bits Reset (0.15) and Restart_AN (0.9) are not set by the user.*

*Note 3: Auto-Negotiation is enabled when speed is set to 1000Base-T. Crossover Detection & Auto-Correction takes precedence over Auto-Negotiation disable (0.12=0). If ANE is disabled, speed and duplex capabilities are advertised by 0.13, 0.6, and 0.8. Otherwise, register 4.8:5 and 9.9:8 take effect.*

*Note 4: Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0.9) is set.*

## 8.4.2. BMSR (Basic Mode Status Register, Address 0x01)

### Table 25. BMSR (Basic Mode Status Register, Address 0x01)

| Bit | Name | Type | Default | Description |
|-----|------|------|---------|-------------|
| 1.15 | 100Base-T4 | RO | 0 | 100Base-T4 Capability.<br>The RTL8211E-VB(VL)/RTL8211EG-VB does not support 100Base-T4 mode. This bit should always be 0. |
| 1.14 | 100Base-TX (full) | RO | 1 | 100Base-TX Full Duplex Capability.<br>1: Device is able to perform 100Base-TX in full duplex mode<br>0: Device is not able to perform 100Base-TX in full duplex mode |
| 1.13 | 100Base-TX (half) | RO | 1 | 100Base-TX Half Duplex Capability.<br>1: Device is able to perform 100Base-TX in half duplex mode<br>0: Device is not able to perform 100Base-TX in half duplex mode |
| 1.12 | 10Base-T (full) | RO | 1 | 10Base-T Full Duplex Capability.<br>1: Device is able to perform 10Base-T in full duplex mode.<br>0: Device is not able to perform 10Base-T in full duplex mode. |
| 1.11 | 10Base-T (half) | RO | 1 | 10Base-T Half Duplex Capability.<br>1: Device is able to perform 10Base-T in half duplex mode<br>0: Device is not able to perform 10Base-T in half duplex mode |
| 1.10 | 10Base-T2 (full) | RO | 0 | 10Base-T2 Full Duplex Capability.<br>The RTL8211E-VB(VL)/RTL8211EG-VB does not support 10Base-T2 mode and this bit should always be 0. |
| 1.9 | 10Base-T2 (half) | RO | 0 | 10Base-T2 Half Duplex Capability.<br>The RTL8211E-VB(VL)/RTL8211EG-VB does not support 10Base-T2 mode. This bit should always be 0. |
| 1.8 | 1000Base-T Extended Status | RO | 1 | 1000Base-T Extended Status Register.<br>1: Device supports Extended Status Register 0x0F (15)<br>0: Device does not support Extended Status Register 0x0F<br>This register is read-only and is always set to 1. |
| 1.7 | RSVD | RO | 0 | Reserved. |
| 1.6 | Preamble Suppression | RO | 1 | Preamble Suppression Capability (Permanently On).<br>The RTL8211E-VB(VL)/RTL8211EG-VB always accepts transactions with preamble suppressed. |
| 1.5 | Auto-Negotiation Complete | RO | 0 | Auto-Negotiation Complete.<br>1: Auto-Negotiation process complete, and contents of registers 5, 6, 8, and 10 are valid<br>0: Auto-Negotiation process not complete |
| 1.4 | Remote Fault | RC, LH | 0 | Remote Fault.<br>1: Remote fault condition detected (cleared on read or by reset). Indication or notification of remote fault from Link Partner<br>0: No remote fault condition detected |
| 1.3 | Auto-Negotiation Ability | RO | 1 | Auto Configured Link.<br>1: Device is able to perform Auto-Negotiation<br>0: Device is not able to perform Auto-Negotiation |

| Bit | Name | Type | Default | Description |
|-----|------|------|---------|-------------|
| 1.2 | Link Status | RO | 0 | Link Status.<br>1: Linked<br>0: Not Linked<br>This register indicates whether the link was lost since the last read. For the current link status, either read this register twice or read register bit 17.10 Link Real Time. |
| 1.1 | Jabber Detect | RC, LH | 0 | Jabber Detect.<br>1: Jabber condition detected<br>0: No Jabber occurred |
| 1.0 | Extended Capability | RO | 1 | 1: Extended register capabilities, always 1 |

## 8.4.3. PHYID1 (PHY Identifier Register 1, Address 0x02)

**Table 26. PHYID1 (PHY Identifier Register 1, Address 0x02)**

| Bit | Name | Type | Default | Description |
|-----|------|------|---------|-------------|
| 2.15:0 | OUI_MSB | RO | 0000000000011100 | Organizationally Unique Identifier Bit 3:18.<br>Always 0000000000011100. |

*Note: Realtek OUI is 0x000732.*

## 8.4.4. PHYID2 (PHY Identifier Register 2, Address 0x03)

**Table 27. PHYID2 (PHY Identifier Register 2, Address 0x03)**

| Bit | Name | Type | Default | Description |
|-----|------|------|---------|-------------|
| 3.15:10 | OUI_LSB | RO | 110010 | Organizationally Unique Identifier Bit 19:24.<br>Always 110010. |
| 3.9:4 | Model Number | RO | 010001 | Manufacture's Model Number |
| 3.3:0 | Revision Number | RO | 0101 | Revision Number |

## 8.4.5. ANAR (Auto-Negotiation Advertising Register, Address 0x04)

**Table 28. ANAR (Auto-Negotiation Advertising Register, Address 0x04)**

| Bit | Name | Type | Default | Description |
|-----|------|------|---------|-------------|
| 4.15 | NextPage | RW | 0 | 1: Additional next pages exchange desired<br>0: No additional next pages exchange desired |
| 4.14 | RSVD | RO | 0 | Reserved. |
| 4.13 | Remote Fault | RW | 0 | 1: Set Remote Fault bit<br>0: No remote fault detected |
| 4.12 | RSVD | RO | 0 | Reserved. |
| 4.11 | Asymmetric PAUSE | RW | 0 | 1: Advertise support of asymmetric pause<br>0: No support of asymmetric pause |

| Bit | Name | Type | Default | Description |
|-----|------|------|---------|-------------|
| 4.10 | PAUSE | RW | 1 | 1: Advertise support of pause frames<br>0: No support of pause frames |
| 4.9 | 100Base-T4 | RO | 0 | 1: 100Base-T4 support<br>0: 100Base-T4 not supported |
| 4.8 | 100Base-TX (Full) | RW | 1 | 1: Advertise support of 100Base-TX full-duplex mode<br>0: Not advertised |
| 4.7 | 100Base-TX (Half) | RW | 1 | 1: Advertise support of 100Base-TX half-duplex mode<br>0: Not advertised |
| 4.6 | 10Base-T (Full) | RW | 1 | 1: Advertise support of 10Base-TX full-duplex mode<br>0: Not advertised |
| 4.5 | 10Base-T (Half) | RW | 1 | 1: Advertise support of 10Base-TX half-duplex mode<br>0: Not advertised |
| 4.4:0 | Selector Field | RO | 00001 | Indicates the RTL8211E-VB(VL)/RTL8211EG-VB supports IEEE 802.3 |

*Note 1: The setting of Register 4 has no effect unless NWay is restarted or the link goes down.*

*Note 2: If 1000Base-T is advertised, then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed.*

## 8.4.6. ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)

**Table 29. ANLPAR (Auto-Negotiation Link Partner Ability Register, Address 0x05)**

| Bit | Name | Type | Default | Description |
|-----|------|------|---------|-------------|
| 5.15 | Next Page | RO | 0 | Next Page Indication.<br>Received Code Word Bit 15. |
| 5.14 | ACK | RO | 0 | Acknowledge.<br>Received Code Word Bit 14. |
| 5.13 | Remote Fault | RO | 0 | Remote Fault indicated by Link Partner.<br>Received Code Word Bit 13. |
| 5.12 | RSVD | RO | 0 | Reserved. |
| 5.11:5 | Technology Ability Field | RO | 00000000 | Received Code Word Bit 12:5. |
| 5.4:0 | Selector Field | RO | 00000 | Received Code Word Bit 4:0. |

*Note: Register 5 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.*

## 8.4.7. ANER (Auto-Negotiation Expansion Register, Address 0x06)

**Table 30. ANER (Auto-Negotiation Expansion Register, Address 0x06)**

| Bit | Name | Type | Default | Description |
|------|------|------|---------|-------------|
| 6.15:5 | RSVD | RO | 0x000 | Reserved. |
| 6.4 | Parallel Detection Fault | RC, LH | 0 | 1: A fault has been detected via the Parallel Detection function<br>0: A fault has not been detected via the Parallel Detection function |
| 6.3 | Link Partner Next Page Able | RO | 0 | 1: Link Partner supports Next Page exchange<br>0: Link Partner does not support Next Page exchange |
| 6.2 | Local Next Page Able | RO | 1 | 1: Local Device is able to send Next Page<br>Always 1. |
| 6.1 | Page Received | RC, LH | 0 | 1: A New Page (new LCW) has been received<br>0: A New Page has not been received |
| 6.0 | Link Partner Auto-Negotiation capable | RO | 0 | 1: Link Partner supports Auto-Negotiation<br>0: Link Partner does not support Auto-Negotiation |

*Note: Register 6 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.*

## 8.4.8. ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)

**Table 31. ANNPTR (Auto-Negotiation Next Page Transmit Register, Address 0x07)**

| Bit | Name | Type | Default | Description |
|------|------|------|---------|-------------|
| 7.15 | Next Page | RW | 0 | Next Page Indication.<br>0: No more next pages to send<br>1: More next pages to send<br>Transmit Code Word Bit 15. |
| 7.14 | RSVD | RO | 0 | Transmit Code Word Bit 14. |
| 7.13 | Message Page | RW | 1 | Message Page.<br>0: Unformatted Page<br>1: Message Page<br>Transmit Code Word Bit 13. |
| 7.12 | Acknowledge 2 | RW | 0 | Acknowledge2.<br>0: Local device has no ability to comply with the message received<br>1: Local device has the ability to comply with the message received<br>Transmit Code Word Bit 12. |
| 7.11 | Toggle | RO | 0 | Toggle Bit.<br>Transmit Code Word Bit 11. |
| 7.10:0 | Message/Unformatted Field | RW | 0x001 | Content of Message/Unformatted Page.<br>Transmit Code Word Bit 10:0. |

## 8.4.9. ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)

**Table 32. ANNPRR (Auto-Negotiation Next Page Receive Register, Address 0x08)**

| Bit | Name | Type | Default | Description |
|------|------|------|---------|-------------|
| 8.15 | Next Page | RO | 0 | Received Link Code Word Bit 15. |
| 8.14 | Acknowledge | RO | 0 | Received Link Code Word Bit 14. |
| 8.13 | Message Page | RO | 0 | Received Link Code Word Bit 13. |
| 8.12 | Acknowledge 2 | RO | 0 | Received Link Code Word Bit 12. |
| 8.11 | Toggle | RO | 0 | Received Link Code Word Bit 11. |
| 8.10:0 | Message/Unformatted Field | RO | 0x00 | Received Link Code Word Bit 10:0. |

*Note: Register 8 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.*

## 8.4.10. GBCR (1000Base-T Control Register, Address 0x09)

**Table 33. GBCR (1000Base-T Control Register, Address 0x09)**

| Bit | Name | Type | Default | Description |
|------|------|------|---------|-------------|
| 9.15:13 | Test Mode | RW | 0 | Test Mode Select.<br>000: Normal Mode<br>001: Test Mode 1 – Transmit Jitter Test<br>010: Test Mode 2 – Transmit Jitter Test (MASTER mode)<br>011: Test Mode 3 – Transmit Jitter Test (SLAVE mode)<br>100: Test Mode 4 – Transmit Distortion Test<br>101, 110, 111: Reserved |
| 9.12 | MASTER/SLAVE Manual Configuration Enable | RW | 0 | Enable Manual Master/Slave Configuration.<br>1: Manual MASTER/SLAVE configuration<br>0: Automatic MASTER/SLAVE |
| 9.11 | MASTER/SLAVE Configuration Value | RW | 0 | Advertise Master/Slave Configuration Value.<br>1: Manual configure as MASTER<br>0: Manual configure as SLAVE |
| 9.10 | Port Type | RW | 0 | Advertise Device Type Preference.<br>1: Prefer multi-port device (MASTER)<br>0: Prefer single port device (SLAVE) |
| 9.9 | 1000Base-T Full Duplex | RW | 1 | Advertise 1000Base-T Full-Duplex Capability.<br>1: Advertise<br>0: Do not advertise |
| 9.8 | RSVD | RW | 0 | Reserved. |
| 9.7:0 | RSVD | RO | 0 | Reserved. |

*Note 1: Values set in register 9.12:9 have no effect unless Auto-Negotiation is restarted (Reg0.9) or the link goes down.*
*Note 2: Bits 9.11 and 9.10 are ignored when bit 9.12=0.*

## 8.4.11. GBSR (1000Base-T Status Register, Address 0x0A)

**Table 34. GBSR (1000Base-T Status Register, Address 0x0A)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 10.15 | MASTER/SLAVE Configuration Fault | RO, RC, LH | 0 | Master/Slave Manual Configuration Fault Detected.<br>1: MASTER/SLAVE configuration fault detected<br>0: No MASTER/SLAVE configuration fault detected |
| 10.14 | MASTER/SLAVE Configuration Resolution | RO | 0 | Master/Slave Configuration Result.<br>1: Local PHY configuration resolved to MASTER<br>0: Local PHY configuration resolved to SLAVE |
| 10.13 | Local Receiver Status | RO | 0 | Local Receiver Status.<br>1: Local Receiver OK<br>0: Local Receiver Not OK |
| 10.12 | Remote Receiver Status | RO | 0 | Remote Receiver Status.<br>1: Remote Receiver OK<br>0: Remote Receiver Not OK |
| 10.11 | Link Partner 1000Base-T Full Duplex Capability | RO | 0 | Link Partner 1000Base-T Full Duplex Capability.<br>1: Link Partner is capable of 1000Base-T full duplex<br>0: Link Partner is not capable of 1000Base-T full duplex |
| 10.10 | Link Partner 1000Base-T Half Duplex Capability | RO | 0 | Link Partner 1000Base-T Half Duplex Capability.<br>1: Link Partner is capable of 1000Base-T half duplex<br>0: Link Partner is not capable of 1000Base-T half duplex |
| 10.9:8 | RSVD | RO | 00 | Reserved. |
| 10.7:0 | Idle Error Count | RO, RC | 0x00 | MSB of Idle Error Counter.<br>The counter stops automatically when it reaches 0xff. |

*Note 1: Values set in register 10.11:10 are not valid until register 6.1 is set to 1.*

*Note 2: Register 10 is not valid until the Auto-Negotiation complete bit 1.5 indicates completed.*

## 8.4.12. MACR (MMD Access Control Register, Address 0x0D)

**Table 35. MACR (MMD Access Control Register, Address 0x0D)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 13.15:14 | Function | WO | 0 | 00: Address<br>01: Data with no post increment<br>10: Data with post increment on reads and writes<br>11: Data with post increment on writes only |
| 13.13:5 | RSVD | RO | 000000000 | Reserved. |
| 13.4:0 | DEVAD | WO | 0 | Device Address. |

*Note 1: This register is used in conjunction with the MAADR (Register 14) to provide access to the MMD address space.*

*Note 2: If the MAADR accesses for address (Function=00), then it is directed to the address register within the MMD associated with the value in the DEVAD field.*

*Note 3: If the MAADR accesses for data (Function≠00), both the DEVAD field and MMD's address register direct the MAADR data accesses to the appropriate registers within the MMD.*

## 8.4.13. MAADR (MMD Access Address Data Register, Address 0x0E)

**Table 36. MAADR (MMD Access Address Data Register, Address 0x0E)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 14.15:0 | Address Data | RW | 0x0000 | 13.15:14 = 00<br>→ MMD DEVAD's address register<br>13.15:14 = 01, 10, or 11<br>→ MMD DEVAD's data register as indicated by the contents of its address register |

*Note: This register is used in conjunction with the MACR (Register 13; Table 35) to provide access to the MMD address space.*

## 8.4.14. GBESR (1000Base-T Extended Status Register, Address 0x0F)

**Table 37. GBESR (1000Base-T Extended Status Register, Address 0x0F)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 15.15 | 1000Base-X FD | RO | 0 | 0: Not 1000Base-X full duplex capable |
| 15.14 | 1000Base-X HD | RO | 0 | 0: Not 1000Base-X half duplex capable |
| 15.13 | 1000Base-T FD | RO | 1 | 1: 1000Base-T full duplex capable |
| 15.12 | 1000Base-T HD | RO | 1 | 1: 1000Base-T half duplex capable |
| 15.11:0 | RSVD | RO | 0x000 | Reserved. |

## 8.4.15. PHYCR (PHY Specific Control Register, Address 0x10)

**Table 38. PHYCR (PHY Specific Control Register, Address 0x10)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 16.15 | Disable RXC | RW | 0 | Disable RXC Clock Output. |
| 16.14:12 | Select FPR Fail | RW | 000 | Select Signal for 'LPRFAIL' (10M Link Pulse Receive Status). |
| 16.11 | Assert CRS on Transmit | RW | 1 (GMII)<br>0 (RGMII) | 1: Assert CRS on transmit<br>0: Never assert CRS on transmit |
| 16.10:8 | RSVD | RW | 001 | Reserved. |
| 16.7 | RSVD | RW | 0 | Reserved. |
| 16.6 | Enable Crossover | RW | 1 | 1: Enable Auto-crossover mechanism<br>After setting MDI/MDIX, perform a PHY reset (register0, bit[15]=1) |
| 16.5 | MDI Mode | RW | 1 | Used to Determine MDI/MDIX Mode when Auto-Crossover is Disabled.<br>*Note:*<br>*Method 1 (Set Reg16.6=0 to disable auto crossover)*<br>*0: MDI mode*<br>*1: MDIX mode*<br>*Method 2 (Set ExtPage45_24.5=1 to disable auto-crossover)*<br>*0: MDIX mode*<br>*1: MDI mode* |

| Bit | Name | Type | Default | Description | |
|------|------|------|---------|-------------|---|
| 16.4 | Disable CLK125 | RW | 0 | 1: CLK125 remains at logic Low<br>0: CLK125 Toggling Enabled | |
| 16.3:1 | RSVD | RW | 111 | Reserved. | |
| 16.0 | Disable Jabber | RW | 0 | 1: Disable jabber function | 0: Enable jabber function |

*Note 1: There are two methods to disable auto-crossover and force MDI or MDIX mode.*
*Method 1:*
*Step 1: Set Enable Crossover Reg16 bit[6]=0 (Disables auto-crossover) and set MDI Reg16 bit[5]=1 (MDIX) or 0 (MDI).*
*Step 2: Set PHY reset Reg0 bit[15]=1.*
*Method 2:*
*Set Disable Crossover ExtPage45 Reg24, bit[5]=1 (Disables auto-crossover) and set MDI Reg16, bit[5]=1 (MDI) or 0 (MDIX).*

*Note 2: To write ExtPage 45_Reg.24 bit[5]=1:*
*a. Write Reg31, Data=0x0007 (page 7).*
*b. Write Reg30, Data=0x002d (Extension page 45).*
*c. Write Reg24, bit[5]=1.*


# 8.4.16.   PHYSR (PHY Specific Status Register, Address 0x11)

**Table 39. PHYSR (PHY Specific Status Register, Address 0x11)**

| Bit | Name | Type | Default | Description | |
|------|------|------|---------|-------------|---|
| 17.15:14 | Speed | RO | 01 | Link Speed.<br>11: Reserved | 10: 1000Mbps |
| | | | | 01: 100Mbps | 00: 10Mbps |
| 17.13 | Duplex | RO | 0 | Full/Half Duplex Mode.<br>1: Full duplex | 0: Half duplex |
| 17.12 | Page Received | RC, LH | 0 | New Page Received.<br>1: Page received | 0: Page not received |
| 17.11 | Speed and Duplex Resolved | RO | 0 | Speed and Duplex Mode Resolved.<br>1: Resolved | 0: Not resolved |
| 17.10 | Link (Real Time) | RO | 0 | Real Time Link Status.<br>1: Link OK | 0: Link not OK |
| 17.9:7 | RSVD | RO | 000 | Reserved. | |
| 17.6 | MDI Crossover Status | RO | 0 | MDI/MDI Crossover Status.<br>1: MDI Crossover | 0: MDI |
| 17.5:2 | RSVD | RW | 0000 | Reserved. | |
| 17.1 | pre_linkok | RO | 0 | Reflects Local Receiver is OK.<br>0: Receiver is not OK<br>1: Receiver is OK | |
| 17.0 | Jabber (Real Time) | RO | 0 | Real Time Jabber Indication.<br>1: Jabber indication | 0: No jabber indication |

## 8.4.17. INER (Interrupt Enable Register, Address 0x12)

**Table 40. INER (Interrupt Enable Register, Address 0x12)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 18.15 | Auto-Negotiation Error Interrupt | RW | 1 | 1: Interrupt Enable      0: Interrupt Disable<br>Setting this bit to 0 only masks an auto-negotiation error interrupt event in the INTB pin.<br>Reg19 Bit15 (section 8.4.18, page 42) always reflects the auto-negotiation error interrupt behavior. |
| 18.14:13 | RSVD | RW | 00 | Reserved. |
| 18.12 | Page Received Interrupt | RW | 1 | 1: Interrupt Enable      0: Interrupt Disable<br>Setting this bit to 0 only masks a page received interrupt event in the INTB pin.<br>Reg19 Bit12 (section 8.4.18, page 42) always reflects the page received interrupt behavior. |
| 18.11 | Auto-Negotiation Completed Interrupt | RW | 1 | 1: Interrupt Enable      0: Interrupt Disable<br>Setting this bit to 0 only masks an auto-negotiation completed interrupt event in the INTB pin.<br>Reg19 Bit11 (section 8.4.18, page 42) always reflects the auto-negotiation completed interrupt behavior. |
| 18.10 | Link Status Change Interrupt | RW | 1 | 1: Interrupt Enable      0: Interrupt Disable<br>Setting this bit to 0 only masks a link status change interrupt event in the INTB pin.<br>Reg19 Bit10 (section 8.4.18, page 42) always reflects the link change interrupt behavior. |
| 18.9 | Symbol Error Interrupt | RW | 1 | 1: Interrupt Enable      0: Interrupt Disable<br>Setting this bit to 0 only masks a symbol error interrupt event in the INTB pin.<br>Reg19 Bit9 (section 8.4.18, page 42) always reflects the symbol error interrupt behavior. |
| 18.8 | False Carrier Interrupt | RW | 1 | 1: Interrupt Enable      0: Interrupt Disable<br>Setting this bit to 0 only masks a false carrier interrupt event in the INTB pin.<br>Reg19 Bit8 (section 8.4.18, page 42) always reflects the false carrier interrupt behavior. |
| 18.7:1 | RSVD | RW | 0000000 | Reserved. |
| 18.0 | Jabber Interrupt | RW | 1 | 1: Interrupt Enable      0: Interrupt Disable<br>Setting this bit to 0 only masks a jabber interrupt event in the INTB pin.<br>Reg19 Bit0 (section 8.4.18, page 42) always reflects the jabber interrupt behavior. |

## 8.4.18.    INSR (Interrupt Status Register, Address 0x13)

**Table 41. INSR (Interrupt Status Register, Address 0x13)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 19.15 | Auto-Negotiation Error | RC, LH | 0 | 1: Auto-Negotiation Error   0: No Auto-Negotiation Error |
| 19.14:13 | RSVD | RC, LH | 00 | Reserved. |
| 19.12 | Page Received | RC, LH | 0 | 1: Page (a new LCW) received<br>0: Page not received |
| 19.11 | Auto-Negotiation Completed | RC, LH | 0 | 1: Auto-Negotiation completed<br>0: Auto-Negotiation not completed |
| 19.10 | Link Status Change | RC, LH | 0 | 1: Link status changed       0: Link status not changed |
| 19.9 | Symbol Error | RC, LH | 0 | 1: Symbol error detected      0: No symbol error detected |
| 19.8 | False Carrier | RC, LH | 0 | 1: False carrier       0: No false carrier detected |
| 19.7:1 | RSVD | RO | 0000000 | Reserved. |
| 19.0 | Jabber | RC, LH | 0 | 1: Jabber detected       0: No jabber detected |

## 8.4.19.    RXERC (Receive Error Counter, Address 0x18)

**Table 42. RXERC (Receive Error Counter, Address 0x18)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 24.15:0 | Receive Error Count | RC | 0x0000 | Receive Error Count. |

*Note: The RXERC register is read-cleared after a read.*

## 8.4.20.    LDPSR (Link Down Power Saving Register, Address 0x1B)

**Table 43. LDPSR (Link Down Power Saving Register, Address 0x1B)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 27.15:1 | RSVD | RO | 0 | Reserved. |
| 27.0 | Power Save Mode | RO | 0 | Link Down Power Saving Mode.<br>1: Reflects local device enters Link Down Power Saving Mode, i.e., cable not plugged in (will be reflected after 3 sec)<br>0: With cable plugged in (will be reflected 21ms after plugging in) |

## 8.4.21.    EPAGSR (Extension Page Select Register, Address 0x1E)

**Table 44. EPAGSR (Extension Page Select Register, Address 0x1E)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 30.15:8 | RSVD | RW | 0 | Reserved. |
| 30.7:0 | ExtPageSel | RW | 0x00 | Extension Page Select (in HEX). |

*Note: This register is used in conjunction with the PAGSEL (Register 31) to provide access to the Extension Page space. Values in this register are valid only if 31.2:0 (PageSel)=111.*

## 8.4.22. PAGSEL (Page Select Register, Address 0x1F)

**Table 45. PAGSEL (Page Select Register, Address 0x1F)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 31.15:3 | RSVD | RW | 0 | Reserved. |
| 31.2:0 | PageSel | RW | 000 | Page Select Signal.<br>000: Page 0 (default page)      001: Page 1<br>010: Page 2      011: Page 3<br>100: Page 4      101: Page 5<br>110: Page 6      111: Extension page |

## 8.4.23. PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)

**Table 46. PC1R (PCS Control 1 Register, MMD Device 3, Address 0x00)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 3.0.15:11 | RSVD | RW | 0 | Reserved. |
| 3.0.10 | Clock Stop Enable | RW | 0 | 1: PHY stops RXC in LPI<br>0: RXC not stoppable |
| 3.0.9:0 | RSVD | RW | 0 | Reserved. |

## 8.4.24. PS1R (PCS Status1 Register, MMD Device 3, Address 0x01)

**Table 47. PS1R (PCS Status 1 Register, MMD Device 3, Address 0x01)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 3.1.15:12 | RSVD | RO | 0 | Reserved. |
| 3.1.11 | TX LPI Received | RO, LH | 0 | 1: TX PCS has received LPI<br>0: LPI not received |
| 3.1.10 | RX LPI Received | RO,LH | 0 | 1: RX PCS has received LPI<br>0: LPI not received |
| 3.19 | TX LPI Indication | RO | 0 | 1: TX PCS is currently receiving LPI<br>0: TX PCS is not currently receiving LPI |
| 3.1.8 | RX LPI Indication | RO | 0 | 1: RX PCS is currently receiving LPI<br>0: RX PCS is not currently receiving LPI |
| 3.1.7 | RSVD | RO | 0 | Reserved. |
| 3.1.6 | Clock Stop Capable | RO | 1 | 1: MAC stops TXC in LPI<br>0: TXC not stoppable |
| 3.1.5:0 | RSVD | RO | 0 | Reserved. |

## 8.4.25. EEECR (EEE Capability Register, MMD Device 3, Address 0x14)

**Table 48. EEECR (EEE Capability Register, MMD Device 3, Address 0x14)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 3.20.15:3 | RSVD | RO | 0 | Reserved. |
| 3.20.2 | 1000BASE-T EEE | RO | 1 | 1: EEE is supported for 1000Base-T EEE<br>0: EEE is not supported for 1000Base-T EEE |
| 3.20.1 | 100BASE-TX EEE | RO | 1 | 1: EEE is supported for 100Base-TX EEE<br>0: EEE is not supported for 100Base-TX EEE |
| 3.20.0 | RSVD | RO | 0 | Reserved. |

## 8.4.26. EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)

**Table 49. EEEWER (EEE Wake Error Register, MMD Device 3, Address 0x16)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 3.22.15:0 | EEE Wake Error Counter | RC | 0 | Used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. |

## 8.4.27. EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3c)

**Table 50. EEEAR (EEE Advertisement Register, MMD Device 7, Address 0x3c)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 7.60.15:3 | RSVD | RW | 0 | Reserved. |
| 7.60.2 | 1000BASE-T EEE | RW | 1 | Advertise 1000Base-T EEE Capability.<br>1: Advertise          0: Do not advertise |
| 7.60.1 | 100BASE-TX EEE | RW | 1 | Advertise 100Base-TX EEE Capability.<br>1: Advertise          0: Do not advertise |
| 7.60.0 | RSVD | RW | 0 | Reserved. |

## 8.4.28. EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3d)

**Table 51. EEELPAR (EEE Link Partner Ability Register, MMD Device 7, Address 0x3d)**

| Bit | Name | Type | Default | Description |
|---|---|---|---|---|
| 7.61.15:3 | RSVD | RO | 0 | Reserved. |
| 7.61.2 | LP 1000BASE-T EEE | RO | 0 | 1: Link Partner is capable of 1000Base-T EEE<br>0: Link Partner is not capable of 1000Base-T EEE |
| 7.61.1 | LP 100BASE-TX EEE | RO | 0 | 1: Link Partner is capable of 100Base-TX EEE<br>0: Link Partner is not capable of 100Base-TX EEE |
| 7.61.0 | RSVD | RO | 0 | Reserved. |

## 8.4.29. LACR (LED Action Control Register, ExtPage 0x2c, Address 0x1a)

**Table 52. LACR (LED Action Control Register, ExtPage 0x2c, Address 0x1a)**

| Bit | Name | Type | Default | Description |
|-----|------|------|---------|-------------|
| 15:7 | RSVD | RO | 0 | Reserved. |
| 6:4 | LEDActCtrl | RW | 101 | LED Blink Mode Setting.<br>1: Blinking mode<br>0: Steady mode |
| 3:0 | RSVD | RO | 0 | Reserved. |

*Note: This register is used in conjunction with the LED Control Register (ExtPage 44, Register 28).*

## 8.4.30. LCR (LED Control Register, ExtPage 0x2c, Address 0x1c)

**Table 53. LCR (LED Control Register, ExtPage 0x2c, Address 0x1c)**

| Bit | Name | Type | Default | Description |
|-----|------|------|---------|-------------|
| 15:11 | RSVD | RO | 0 | Reserved. |
| 10:8 | LED2 Control | RW | 111 | LED2 Control Bits. |
| 7 | RSVD | RO | 0 | Reserved. |
| 6:4 | LED1 Control | RW | 111 | LED1 Control Bits. |
| 3 | RSVD | RO | 0 | Reserved. |
| 2:0 | LED0 Control | RW | 000 | LED0 Control Bits. |

*Note: This register is used in conjunction with the LED Action Control Register (ExtPage 44, Register 26).*

## 8.4.31. ACCR (Auto-Crossover Control Register, ExtPage 0x2d, Address 0x18)

**Table 54. ACCR (Auto-Crossover Control Register, ExtPage 0x2d, Address 0x18)**

| Bit | Name | Type | Default | Description |
|-----|------|------|---------|-------------|
| 15:6 | RSVD | RO | 0 | Reserved. |
| 5 | Disable Crossover | RW | 0 | 1: Disable Auto-crossover and determine MDI/MDIX mode via bit 16.5. |
| 4:0 | RSVD | RO | 0 | Reserved. |

## 8.4.32. SCR (SSC Control Register, ExtPage 0xa0, Address 0x1a)

**Table 55. SCR (SSC Control Register, ExtPage 0xa0, Address 0x1a)**

| Bit | Name | Type | Default | Description |
|-----|------|------|---------|-------------|
| 15:3 | RSVD | RO | 0 | Reserved. |
| 2 | Disable RXC SSC | RW | 1 | 1: Disable Spread-Spectrum Clocking (SSC) on RXC. |
| 1:0 | RSVD | RO | 0 | Reserved. |

# 9. Switching Regulator

The RTL8211E-VB(VL)/RTL8211EG-VB incorporates a state-of-the-art switching regulator that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. The switching regulator 1.05V output pin (REG_OUT) should be connected only to DVDD10 and AVDD10 (do not provide this power source to other devices).

## 9.1. PCB Layout

- The input 3.3V power trace connected to VDDREG must be wider than 40 mils

- The bulk de-coupling capacitors (Cin1 and Cin2) must be placed within 200 mils (0.5cm) of VDDREG to prevent input voltage overshoot

- The output power trace out of REG_OUT must be wider than 60 mils

- Lx (2.2µH/4.7µH) must be kept within 200 mils (0.5cm) of REG_OUT

- Cout1 and Cout2 must be kept within 200 mils (0.5cm) of Lx to ensure stable output power and better power efficiency

- For switching regulator stability, the capacitor Cout1 and Cout2 must be a ceramic (X5R) capacitor. Cin1 and Cin2 are recommended to be ceramic capacitors

- Place Lx and Cin1 on the same layer as the RTL8211E-VB(VL)/RTL8211EG-VB. Do not use vias on VDDREG and REG_OUT traces

*Note: Violation of the above rules will damage the IC.*
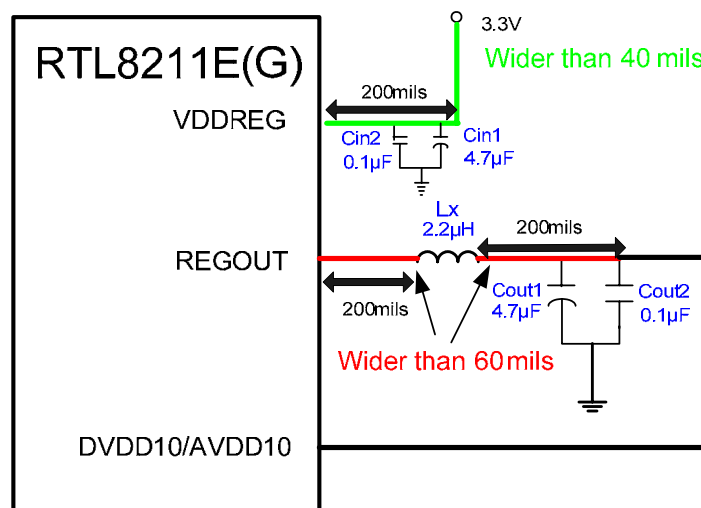
**Figure 11. Switching Regulator**

# 9.2.  Inductor and Capacitor Parts List

**Table 56. Inductor and Capacitor Parts List**

| Inductor Type | Inductance | Max IDC (mA) | Variation | Output Ripple (mV) |
|---|---|---|---|---|
| GLK2510P-2R2M | 2.2µH | 1000 | ≤ 20% | (See Figure 15, Figure 16) |
| GLK2510P-4R7M | 4.7µH | 750 | ≤ 20% | (See Figure 17, Figure 18) |
| GTSD32P-2R2M | 2.2µH | 1500 | ≤ 20% | (See Figure 19) |

*Note 1: The ESR is equivalent to RDC or DCR. Lower ESR inductor values will promote a higher-efficiency switching regulator.*

*Note 2: The power inductor used by the switching regulator must be able to withstand 600mA of current.*

*Note 3: Typically, if the power inductor's ESR at 1MHz is below 0.8Ω, the switching regulator efficiency will be above 75%. However the actual switching regulator efficiency should be measured according to the method described in section 9.4 Efficiency Measurement, page 54.*

*Note 4: If the inductor does not meet this requirement, it may damage the switching regulator.*

| Capacitor Type | Capacitance | ESR at 1MHz (mΩ) | Output Ripple (mV) |
|---|---|---|---|
| 4.7µF 0805 X5R TDK | 4.838 | 40.28 | (See Figure 15, Figure 17) |
| 10µF 0603 X5R YAGEO | 11.956 | 58.29 | (See Figure 16, Figure 18) |

*Note: Capacitors (Cin1 & Cin2) must be ceramic due to their low ESR value. Lower ESR values will yield lower output voltage ripple.*

## 9.3. Measurement Criteria

In order for the switching regulator to operate properly, the input and output voltage measurement criteria must be met. From the input side, the voltage overshoot cannot exceed 4V; otherwise the chip may be damaged. Note that the voltage signal must be measured directly at the VDDREG pin, not at the capacitor. In order to reduce the input voltage overshoot, the Cin1 and Cin2 must be placed close to the VDDREG pin. The following figures show what a good input voltage and a bad one look like.
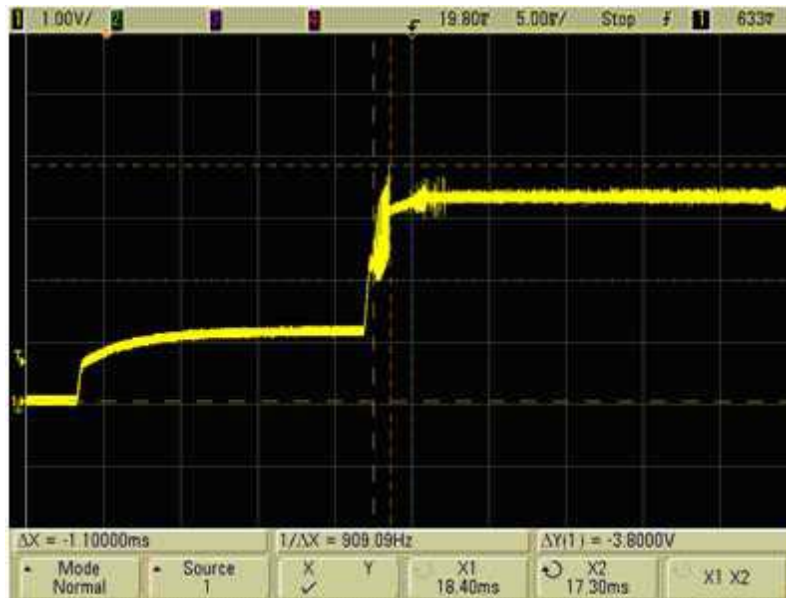


**Figure 12. Input Voltage Overshoot <4V (Good)**



**Figure 13. Input Voltage Overshoot >4V (Bad)**

From the output side measured at the REG_OUT pin, the voltage ripple must be within 100mV peak-to-peak. Choosing different types and values of input and output capacitor (Cin1, Cin2; Cout1, Cout2) and power inductor (Lx) will seriously affect the efficiency and output voltage ripple of switching regulators. The following figures show the effects of different types of capacitors on the switching regulator's output voltage.

The blue square wave signal (top row) is measured at the output of the REG_OUT pin before the power inductor (Lx). The yellow signal (second row) is measured after the power inductor (Lx), and shows there is a voltage ripple. The green signal (lower row) is the current. Data in the following figures was measured at gigabit speed.



**Figure 14. Ceramic 10µF 0603 (X5R) (Good)**



**Figure 15. L=GLK2510P-2R2M, C=Ceramic 4.7µF 0805 X5R TDK (Ripple 12.4mV)**
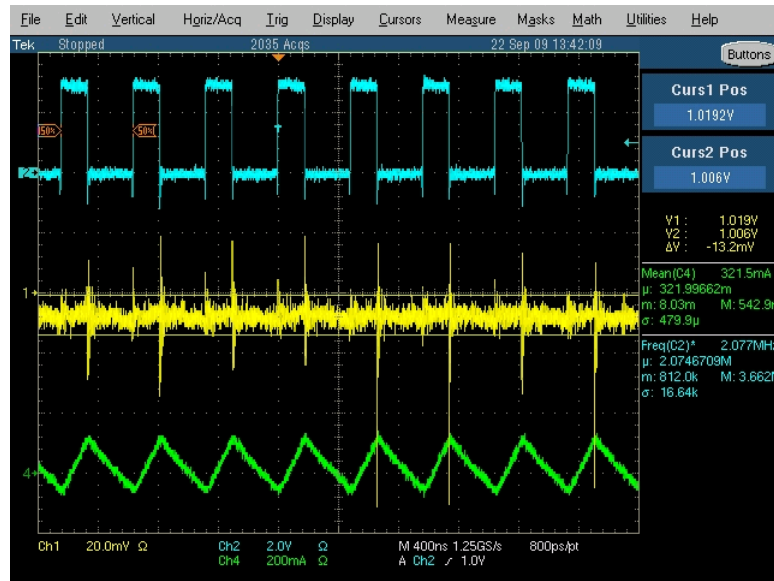
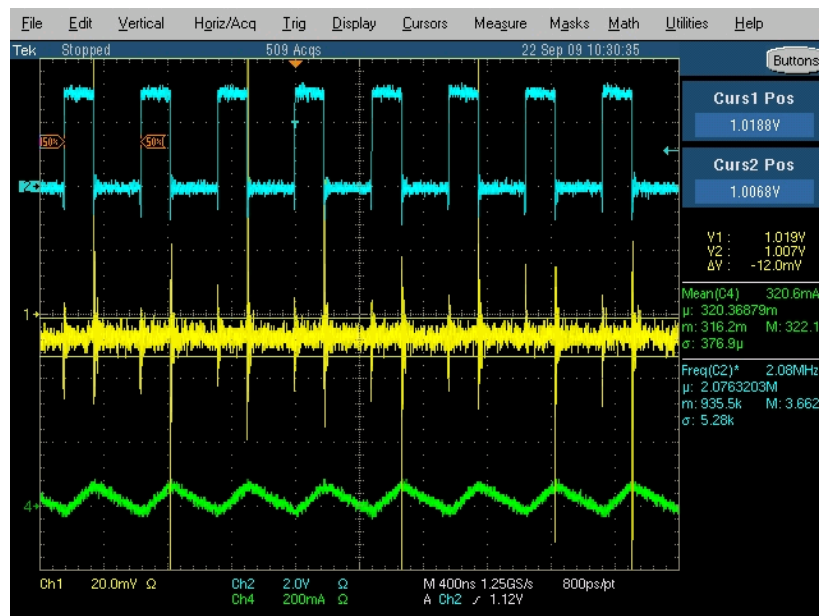**Figure 16. L=GLK2510P-2R2M, C=Ceramic 10µF 0603 X5R YAGEO (Ripple 13.2mV)**



**Figure 17. L=GLK2510P-4R7M, C=Ceramic 4.7µF 0805 X5R TDK (Ripple 12mV)**

**Figure 18. L=GLK2510P-4R7M, C=Ceramic 10μF 0603 X5R YAGEO (Ripple 11.2mV)**



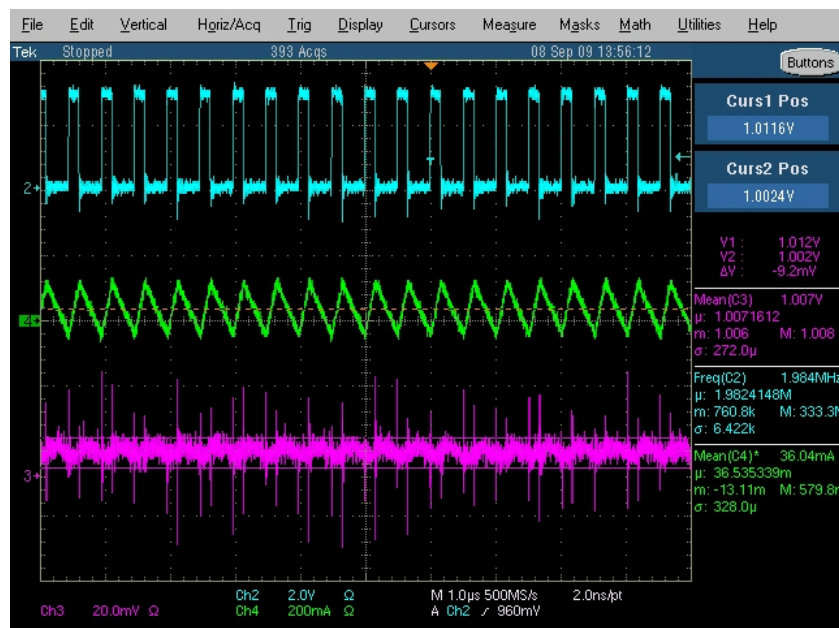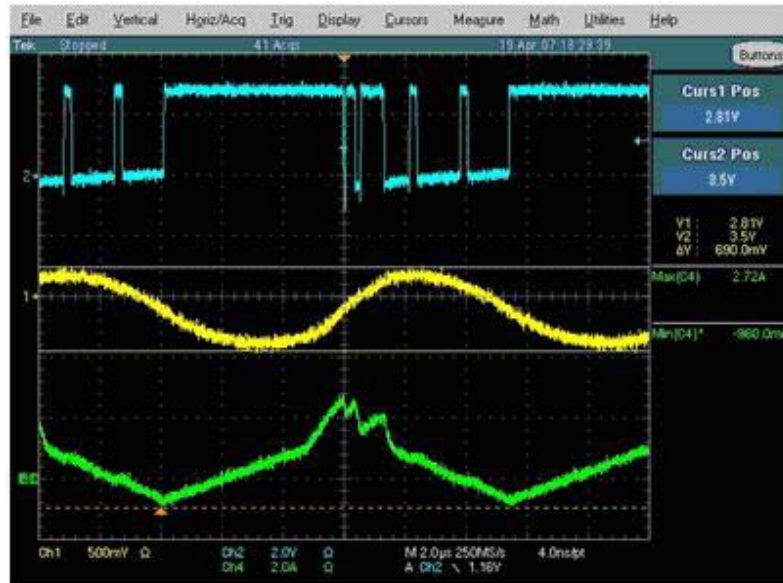**Figure 19. L=GTSD32P-2R2M, C=Ceramic 4.7μF 0805 X5R TDK (Ripple 9.2mV)**

**Figure 20. Ceramic 10µF (Y5V) (Bad)**

A ceramic 10µF (X5R) will have a lower voltage ripple compared to an electrolytic 100µF. The key to choosing a proper output capacitor is to choose the lowest ESR to reduce the output voltage ripple. Choosing a ceramic 10µF (Y5V) in this case will cause malfunction of the switching regulator. Placing several Electrolytic capacitors in parallel will help lower the output voltage ripple.



**Figure 21. Electrolytic 100µF (Ripple Too High)**

The following figures show how different inductors affect the REG_OUT output waveform. The typical waveform should look like Figure 22, which has a square waveform with a dip at the falling edge and the rising edge. If the inductor is not carefully chosen, the waveform may look like Figure 23, where the waveform looks like a distorted square. This will cause insufficient current supply and will undermine the stability of the system at gigabit speed. Data in the following figures was measured at gigabit speed
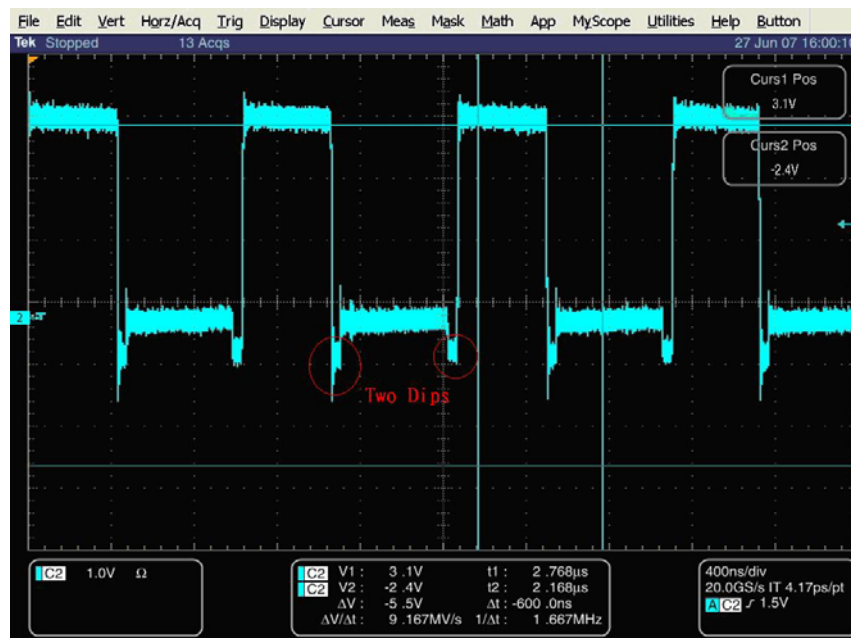


**Figure 22. GTSD32P-2R2M (Good)**
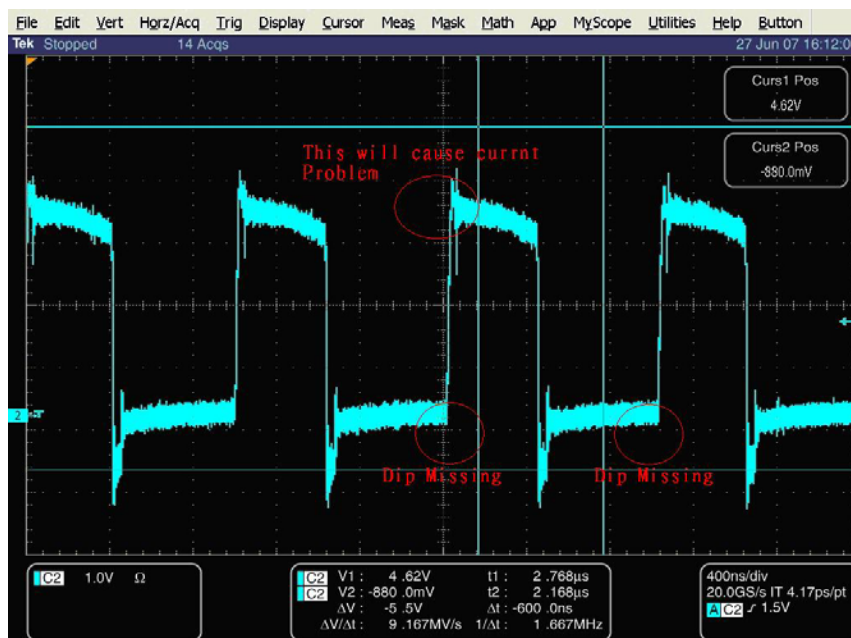


**Figure 23. 1µH Bead (Bad)**

## 9.4. Efficiency Measurement

The efficiency of the switching regulator is designed to be above 75% in gigabit traffic mode. It is very important to choose a suitable inductor before Gerber certification, as the Inductor ESR value will affect the efficiency of the switching regulator. An inductor with a lower ESR value will result in a higher-efficiency switching regulator.

The efficiency of the switching regulator is easily measured using the following method.

Figure 24 shows two checkpoints, checkpoint A (CP_A) and checkpoint B (CP_B). The switching regulator input current (Icpa) should be measured at CP_A, and the switching regulator output current (Icpb) should be measured at CP_B.

To determine efficiency, apply the following formula:

Efficiency = Vcpb*Icpb / Vcpa*Icpa

Where Vcpb is 1.05V; Vcpa is 3.3V. The measurements should be performed in gigabit traffic mode.

For example: The inductor used in the evaluation board is a GOTREND GTSD32-4R7M:

- The ESR value @ 1MHz is approximately 0.712ohm

- The measured Icpa is 101mA at CP_A

- The measured Icpb is 263mA at CP_B

These values are measured in gigabit traffic mode, so the efficiency of the GOTREND GTSD32-4R7M can be calculated as follows:

Efficiency = (1.05V*263mA) / (3.3V*101mA) = 0.823 = 82.3%.

We strongly recommend that when choosing an inductor for the switching regulator, the efficiency should be measured, and that the inductor should yield an efficiency rating higher than 75%. If the efficiency does not meet this requirement, there may be risk to the switching regulator reliability in the long run.
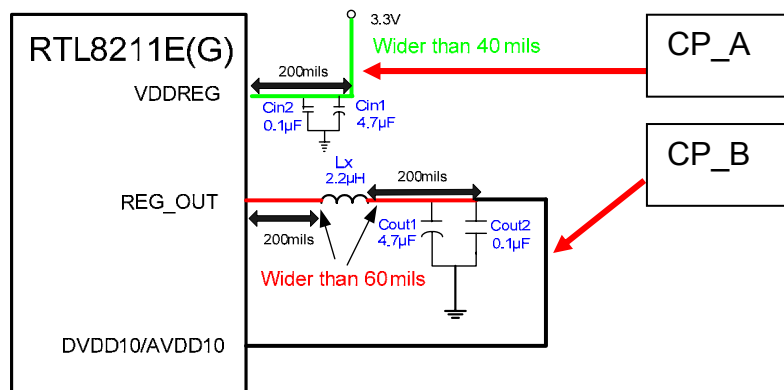


**Figure 24. Switching Regulator Efficiency Measurement Checkpoint**

## 9.5. Power Sequence
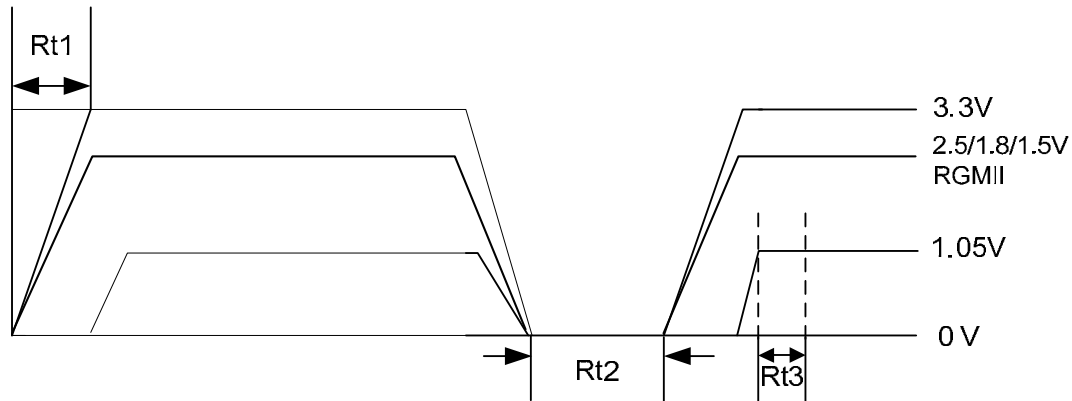


**Figure 25. Power Sequence**

**Table 57. Power Sequence Parameters**

| Symbol | Description | Min | Typical | Max | Units |
|--------|-------------|-----|---------|-----|-------|
| Rt1 | 3.3V Rise Time | 0.5* | - | 100 | ms |
| Rt1 | 2.5/1.8/1.5V RGMII Rise Time | - | - | 100 | ms |
| Rt2 | 3.3V Off Time | 100 | - | - | ms |
| Rt3 | Core Logic Ready Time | 20 | - | - | ms |

*Note 1: The RTL8211E-VB(VL)/RTL8211EG-VB does not support fast 3.3V rising. The 3.3V rise time should be controlled over 0.5ms.*

*\* A 3.3V rise time between 0.1ms to 0.5ms is conditionally permitted only if the system 3.3V power budget is sufficient to ensure that 3.3V Overcurrent Protection (OCP) will NOT be triggered during the power-on procedure. If the rise time is less than 0.1ms, it will induce a peak voltage in VDDREG which may cause permanent damage to the switching regulator.*

*Note 2: If there is any action that involves consecutive ON/OFF toggling of the switching-regulator source (3.3V), the design must make sure the OFF state of both the switching-regulator source (3.3V) and output (1.05V) reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 100ms.*

*Note 3: When using an external oscillator or clock source, on stopping the clock source the RTL8211E-VB(VL)/RTL8211EG-VB must also be powered off.*

*Note 4: 2.5V (or 1.8/1.5V) RGMII power should be risen simultaneously or slightly earlier than 3.3V power. Rising 2.5V (or 1.8/1.5V) power later than 3.3V power may lead to errors.*

# 10.   Characteristics

## *10.1. Absolute Maximum Ratings*

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

**Table 58. Absolute Maximum Ratings**

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| VDD33, AVDD33 | Supply Voltage 3.3V | -0.4 | 3.7 | V |
| AVDD10, DVDD10 | Supply Voltage 1.05V | -0.1 | 1.26 | V |
| 2.5V RGMII/GMII | Supply Voltage 2.5V | -0.2 | 2.8 | V |
| 1.8V RGMII | Supply Voltage 1.8V | -0.2 | 2.3 | V |
| 1.5V RGMII | Supply Voltage 1.5V | -0.2 | 2.0 | V |
| DCinput | Input Voltage | -0.5 | Corresponding Supply Voltage + 0.5 | V |
| DCoutput | Output Voltage | -0.3 | Corresponding Supply Voltage + 0.5 | V |
| NA | Storage Temperature | -55 | +125 | °C |

*Note: Refer to the most updated schematic circuit for correct configuration.*

## *10.2. Recommended Operating Conditions*

**Table 59. Recommended Operating Conditions**

| Description | Pins | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Supply Voltage VDD | DVDD33, AVDD33 | 2.97 | 3.3 | 3.63 | V |
|  | AVDD10, DVDD10 | 0.95 | 1.05 | 1.09 | V |
|  | 2.5V RGMII/GMII | 2.4 | 2.5 | 2.62 | V |
|  | 1.8V RGMII | 1.5 | 1.8 | 2.2 | V |
|  | 1.5V RGMII | 1.43 | 1.5 | 1.9 | V |
| Ambient Operating Temperature $T_A$ | - | 0 | - | 70 | °C |
| Maximum Junction Temperature | - | - | - | 125 | °C |

# 10.3. Crystal Requirements

**Table 60. Crystal Requirements**

| Symbol | Description/Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $F_{ref}$ | Parallel Resonant Crystal Reference Frequency, Fundamental Mode, AT-Cut Type. | - | 25 | - | MHz |
| $F_{ref}$ Tolerance | Parallel Resonant Crystal Frequency Tolerance, Fundamental Mode, AT-Cut Type. $T_a$=0°C~70°C. | -50 | - | +50 | ppm |
| $F_{ref}$ Duty Cycle | Reference Clock Input Duty Cycle. | 40 | - | 60 | % |
| ESR | Equivalent Series Resistance. | - | - | 30 | Ω |
| DL | Drive Level. | - | - | 0.5 | mW |
| Jitter | Broadband Peak-to-Peak Jitter1, 2 | - | - | 200 | ps |
| $V_{ih\_CKXTAL}$ | Crystal Output High Level | 1.4 | - | - | V |
| $V_{il\_CKXTAL}$ | Crystal Output Low Level | - | - | 0.4 | V |

*Note 1: 25KHz to 25MHz RMS < 3ps.*

*Note 2: Broadband RMS < 9ps.*

*Note 3: Fref Tolerance +/- 50ppm including effects of first year aging, external crystal capacitors, and PCB layout.*

# 10.4. Oscillator/External Clock Requirements

**Table 61. Oscillator/External Clock Requirements**

| Parameter | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Frequency | - | - | 25/50 | - | MHz |
| Frequency Tolerance | Ta=0°C~70°C | -50 | - | 50 | ppm |
| Duty Cycle | - | 40 | - | 60 | % |
| Broadband Peak-to-Peak Jitter [1,2] | - | - | - | 200 | ps |
| Vpeak-to-peak | - | 3.15 | 3.3 | 3.45 | V |
| Rise Time (10%~90%) | - | - | - | 10 | ns |
| Fall Time (10%~90%) | - | - | - | 10 | ns |
| Operating Temperature Range | - | 0 | - | 70 | °C |

*Note 1: 25KHz to 25MHz RMS < 3ps.*

*Note 2: Broadband RMS < 9ps.*

*Note 3: $F_{ref}$ Tolerance +/- 50ppm including effects of first year aging, external crystal capacitors, and PCB layout.*

## 10.5. DC Characteristics

**Table 62. DC Characteristics**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| VDD33, AVDD33 | 3.3V Supply Voltage | - | 2.97 | 3.3 | 3.63 | V |
| 1. MDIO (Table 5, page 8)<br>2. RGMII/GMII I/O (Table 3, page 9/Table 4,page 9) | 2.5V RGMII/GMII Supply Voltage | - | 2.37 | 2.5 | 2.62 | V |
| 1. MDIO (Table 5, page 8)<br>2. RGMII I/O (Table 3, page 9) | 1.5V RGMII Supply Voltage | - | 1.43V | 1.5V | 1.9V | V |
| 1. MDIO (Table 5, page 8)<br>2. RGMII I/O (Table 3, page 9) | 1.8V RGMII Supply Voltage | - | 1.5V | 1.8V | 2.2V | V |
| DVDD10, AVDD10 | 1.05V Supply Voltage | - | 0.95 | 1.05 | 1.09 | V |
| Voh (3.3V) | Minimum High Level Output Voltage | - | 0.9*VDD33 | - | VDD33 + 0.3 | V |
| Voh (2.5V) | Minimum High Level Output Voltage | - | 0.9*VDD25 | - | VDD25 + 0.3 | V |
| Voh (1.8V) | Minimum High Level Output Voltage | - | 0.9*VDD18 | - | VDD18 + 0.3 | V |
| Voh (1.5V) | Minimum High Level Output Voltage | - | 0.9*VDD15 | - | VDD15 + 0.3 | V |
| Vol (3.3V) | Maximum Low Level Output Voltage | - | -0.3 | - | 0.1*VDD33 | V |
| Vol (2.5V) | Maximum Low Level Output Voltage | - | -0.3 | - | 0.1*VDD25 | V |
| Vol (1.8V) | Maximum Low Level Output Voltage | - | -0.3 | - | 0.1*VDD18 | V |
| Vol (1.5V) | Maximum Low Level Output Voltage | - | -0.3 | - | 0.1*VDD15 | V |
| Vih (3.3V) | Minimum High Level Input Voltage | - | 1.8 | - | - | V |
| Vil (3.3V) | Maximum Low Level Input Voltage | - | - | - | 0.9 | V |
| Vih (2.5V) | Minimum High Level Input Voltage | - | 1.7 | - | - | V |
| Vil (2.5V) | Maximum Low Level Input Voltage | - | - | - | 0.7 | V |
| Vih (1.8V) | Minimum High Level Input Voltage | - | 1.2 | - | - | V |
| Vil (1.8V) | Maximum Low Level Input Voltage | - | - | - | 0.5 | V |
| Vih (1.5V) | Minimum High Level Input Voltage | - | 1.0 | - | - | V |
| Vil (1.5V) | Maximum Low Level Input Voltage | - | - | - | 0.3 | V |
| Iin | Input Current | Vin=VDD33 or GND | 0 | - | 0.5 | μA |

*Note: Pins not mentioned above remain at 3.3V.*

# 10.6. AC Characteristics

## 10.6.1. MDC/MDIO Timing
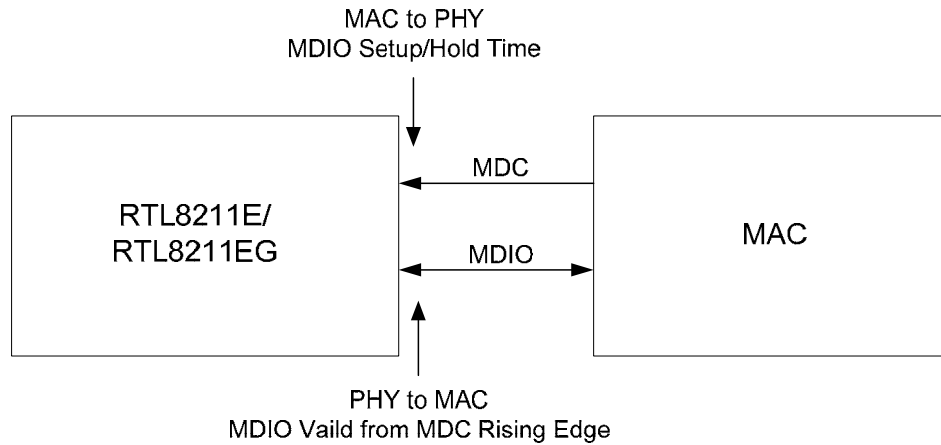


**Figure 26. MDC/MDIO Setup, Hold Time, and Valid from MDC Rising Edge Time Definitions**

**MDC/MDIO Timing – Management Port**
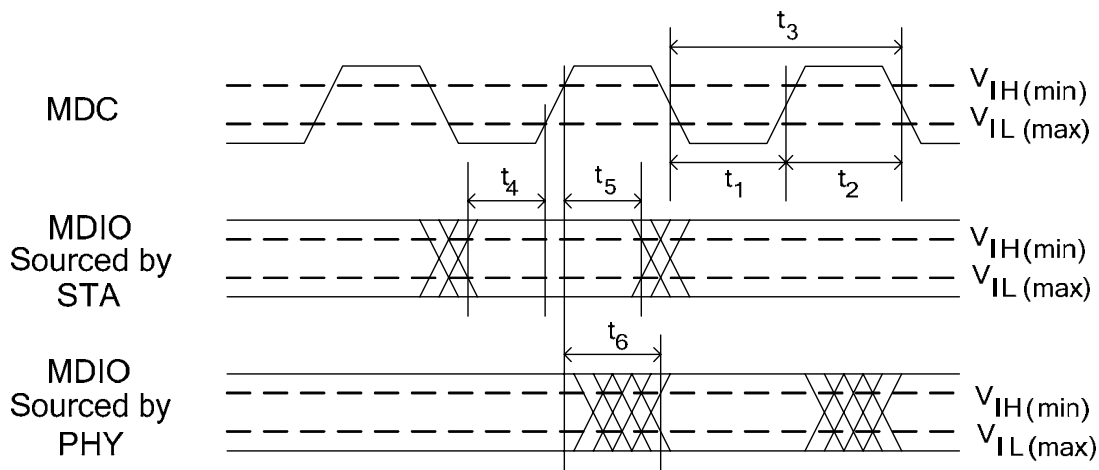


**Figure 27. MDC/MDIO Management Timing Parameters**

**Table 63. MDC/MDIO Management Timing Parameters**

| Symbol | Description | Minimum | Maximum | Unit |
|--------|-------------|---------|---------|------|
| $t_1$ | MDC High Pulse Width | 160 | - | ns |
| $t_2$ | MDC Low Pulse Width | 160 | - | ns |
| $t_3$ | MDC Period | 400 | - | ns |
| $t_4$ | MDIO Setup to MDC Rising Edge | 10 | - | ns |
| $t_5$ | MDIO Hold Time from MDC Rising Edge | 10 | - | ns |
| $t_6$ | MDIO Valid from MDC Rising Edge | 0 | 300 | ns |

## 10.6.2. MII Transmission Cycle Timing (RTL8211EG-VB Only)
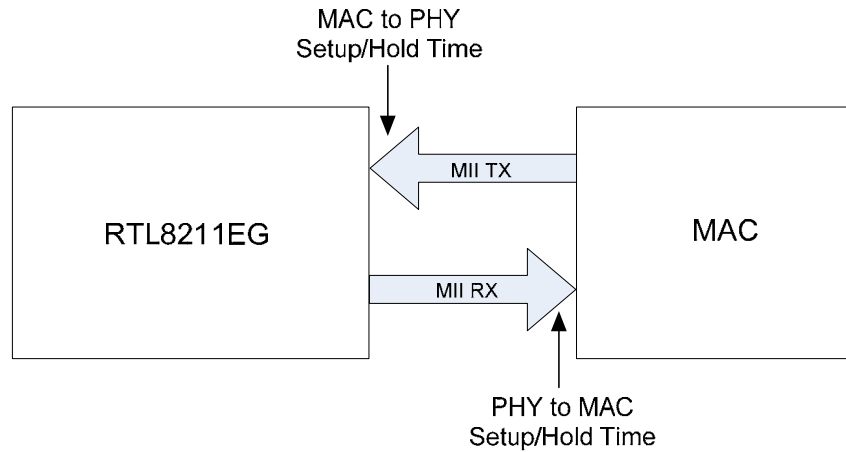
Figure 28. MII Interface Setup/Hold Time Definitions

Figure 29 show an example of a packet transfer from MAC to PHY on the MII interface.
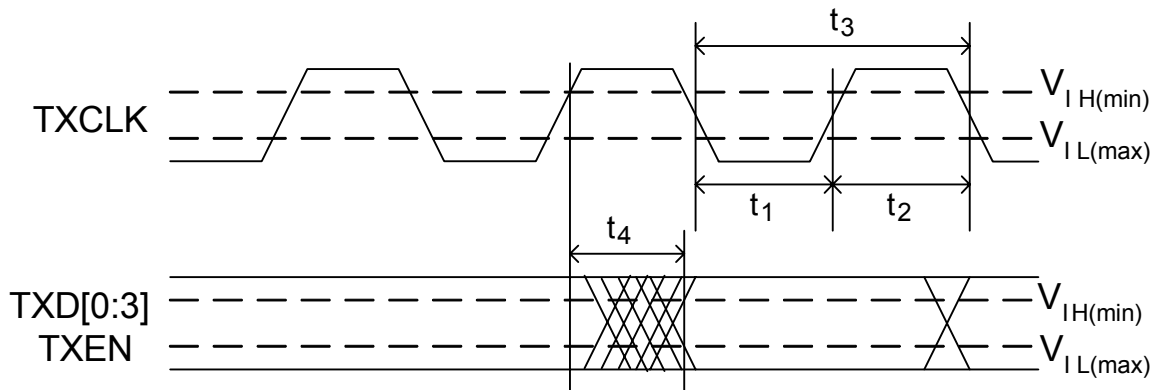
Figure 29. MII Transmission Cycle Timing

**Table 64. MII Transmission Cycle Timing**

| Symbol | Description | | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $t_1, t_2$ | TXCLK Duty Cycle | 100Mbps | 40 | 50 | 60 | % |
| | | 10Mbps | 40 | 50 | 60 | % |
| $t_3$ | TXCLK Period | 100Mbps | - | 40 | - | ns |
| | | 10Mbps | - | 400 | - | ns |
| $t_4$ | TXEN, TXD[0:3] | 100Mbps | 0 | - | 25 | ns |
| | Hold After TXCLK Rising Edge | 10Mbps | 0 | - | 25 | ns |

## 10.6.3. MII Reception Cycle Timing (RTL8211EG-VB Only)

Figure 30 show an example of a packet transfer from PHY to MAC on the MII interface.
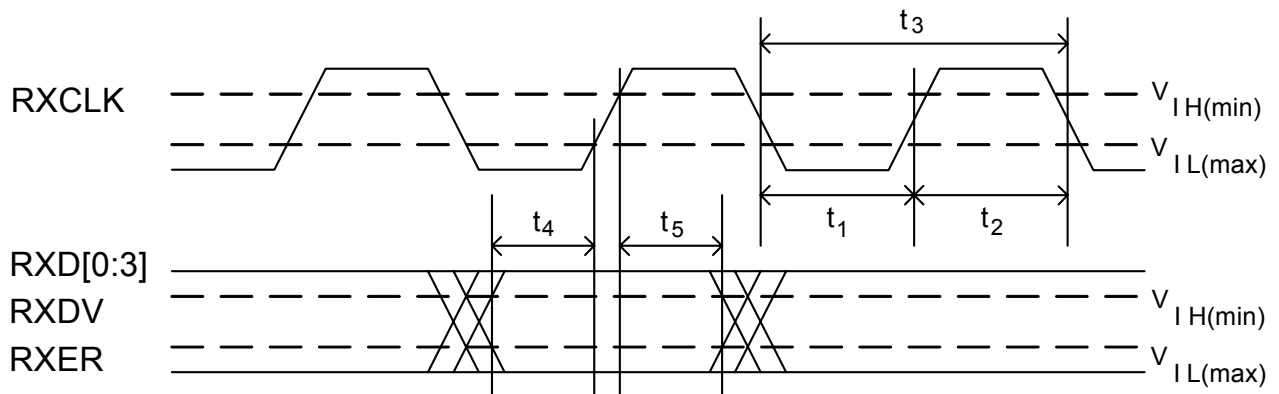


**Figure 30. MII Reception Cycle Timing**

**Table 65. MII Reception Cycle Timing**

| Symbol | Description | | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $t_1, t_2$ | RXCLK Duty Cycle | 100Mbps | 40 | 50 | 60 | % |
| | | 10Mbps | 40 | 50 | 60 | % |
| $t_3$ | RXCLK Period | 100Mbps | - | 40 | - | ns |
| | | 10Mbps | - | 400 | - | ns |
| $t_4$ | RXER, RXDV, RXD[0:3] Setup to RXCLK Rising Edge | 100Mbps | 10 | - | - | ns |
| | | 10Mbps | 10 | - | - | ns |
| $t_5$ | RXER, RXDV, RXD[0:3] Hold After RXCLK Rising Edge | 100Mbps | 10 | - | - | ns |
| | | 10Mbps | 10 | - | - | ns |

## 10.6.4.   GMII Timing Modes (RTL8211EG-VB Only)
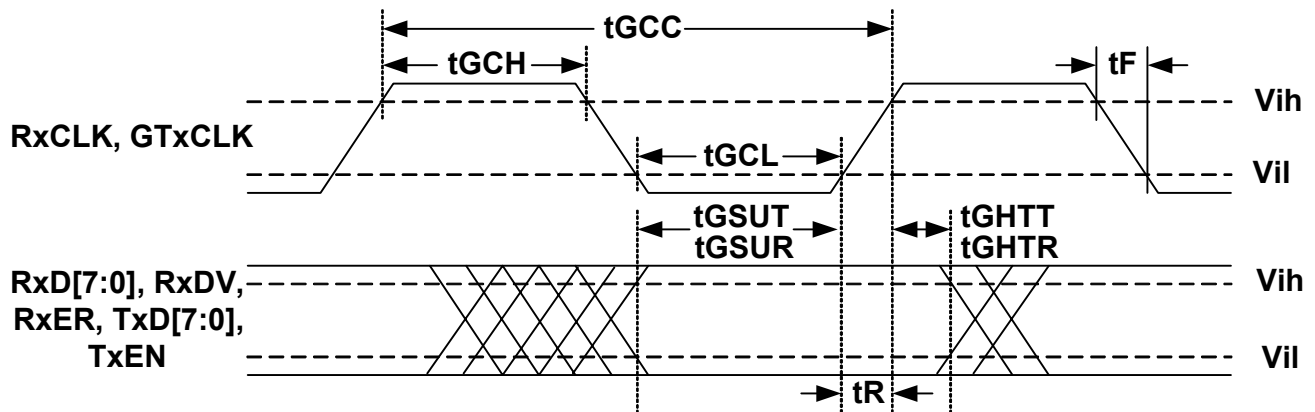


**Figure 31. GMII Timing**

**Table 66. GMII Timing Parameters**

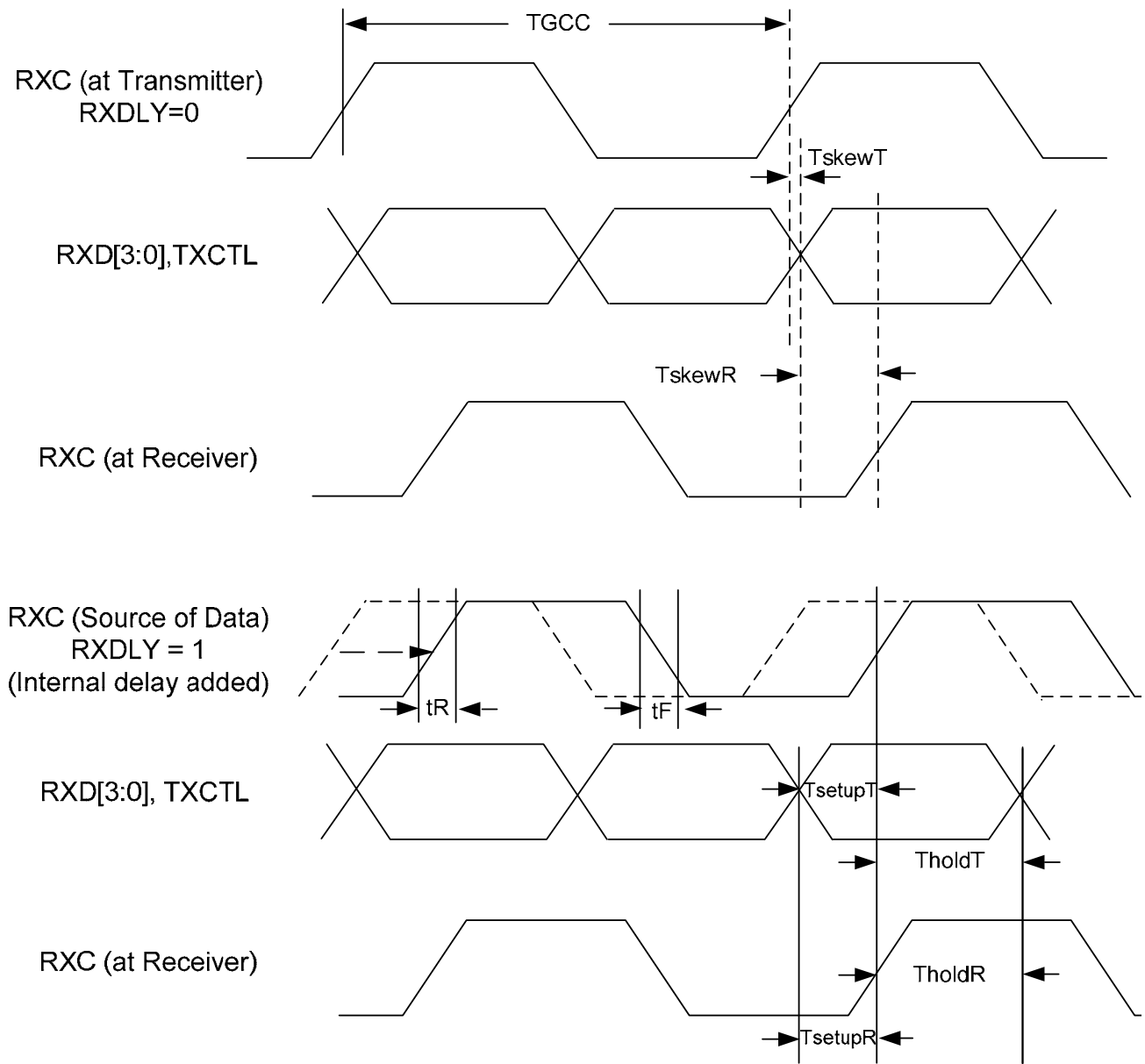| Symbol | Description | Min | Typical | Max | Units |
|--------|-------------|-----|---------|-----|-------|
| tGCC | RxCLK Cycle Time | 7.5 | 8 | 8.5 | ns |
| tGCH | GTxCLK, RxCLK High Time | 2.5 | - | - | ns |
| tGCL | GTxCLK, RxCLK Low Time | 2.5 | - | - | ns |
| tR | GTxCLK, RxCLK Rise Time | - | - | 1 | ns |
| tF | GTxCLK, RxCLK Fall Time | - | - | 1 | ns |
| tGSUT | RxD, RxDV, RxER Setup to $\uparrow$ of RxCLK | 2.5 | - | - | ns |
| tGHTT | RxD, RxDV, RxER Hold from $\uparrow$ of RxCLK | 0.5 | - | - | ns |
| tGSUR | TxD, TxEN Setup to $\uparrow$ of GTxCLK | 2 | - | - | ns |
| tGHTR | TxD, TxEN Hold from $\uparrow$ of GTxCLK | 0 | - | - | ns |

## 10.6.5.    RGMII Timing Modes

Timing for this interface will be such that the clock and data are generated simultaneously by the source of the signals and therefore skew between the clock and data is critical to proper operation.

Figure 32 shows the effect of adding an internal delay to TXC when in RGMII mode.
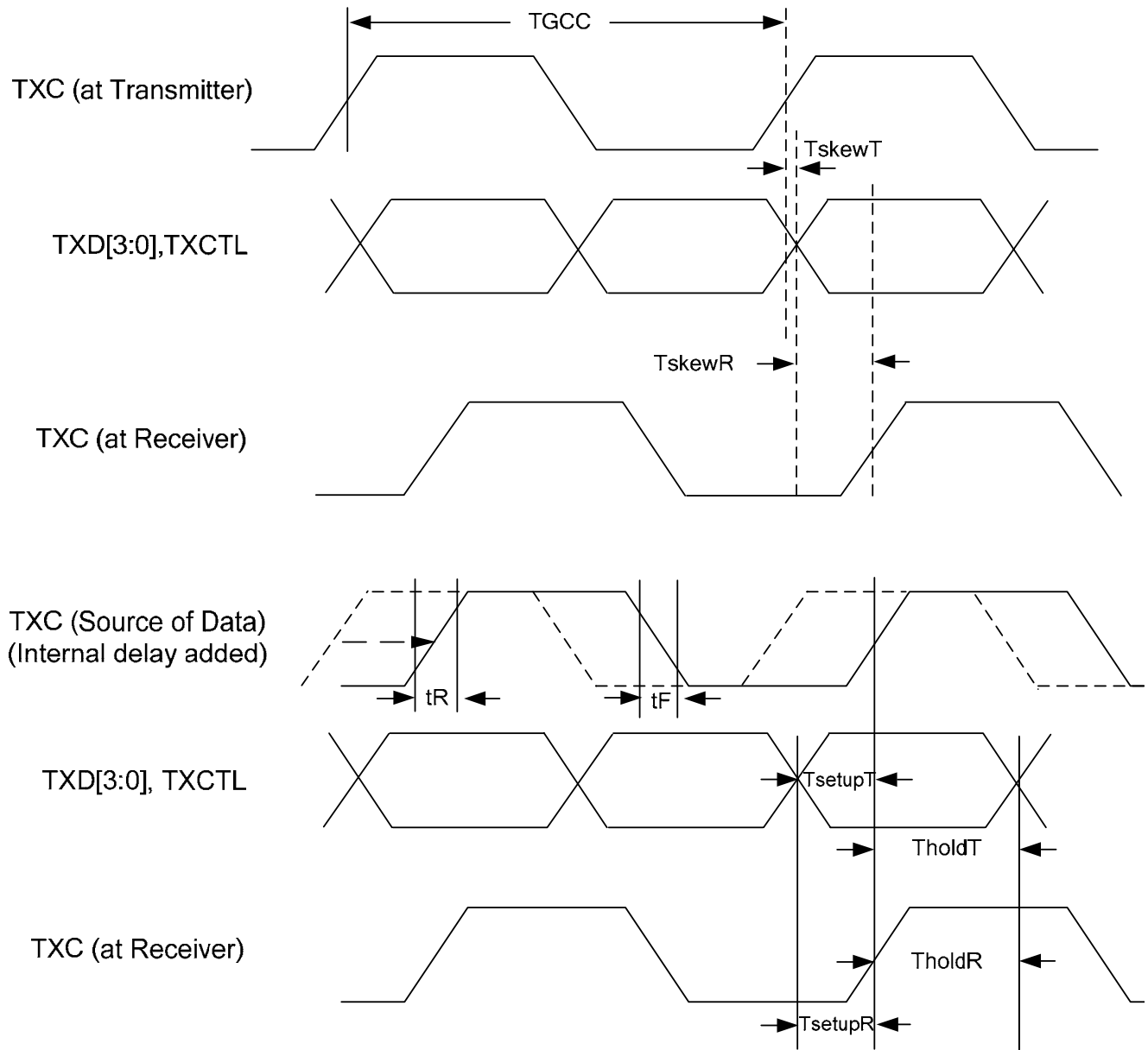


**Figure 32. RGMII Timing Modes (For TXC)**

Figure 33 shows the effect of adding an internal delay to the RXC flow when in RGMII mode.



**Figure 33. RGMII Timing Modes (For RXC)**

**Table 67. RGMII Timing Parameters**

| Symbol | Description | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| TGCC | Clock Cycle Duration (1000Mbps) | 7.2 | 8 | 8.8 | ns |
|  | Clock Cycle Duration (100Mbps) | 36 | 40 | 44 | ns |
|  | Clock Cycle Duration (10Mbps) | 360 | 400 | 440 | ns |
| Duty_G | Duty Cycle for 1000 | 45 | 50 | 55 | % |
| Duty_T | Duty Cycle for 10/100 | 40 | 50 | 60 | % |
| tR | RXC Rise Time (20%~80%) | - | - | 0.75 | ns |
| tF | RXC Fall Time (20%~80%) | - | - | 0.75 | ns |
| TsetupT | Data to Clock Output Setup (at transmitter integrated delay) | 1.2 | 2 | - | ns |
| TholdT | Data to Clock Output Hold (at transmitter integrated delay) | 1.2 | 2 | - | ns |
| TsetupR | Data to Clock Input Setup (at receiver integrated delay) | 1.0 | 2 | - | ns |
| TholdR | Data to Clock Input Hold (at receiver integrated delay) | 1.0 | 2 | - | ns |
| TskewT | Data to Clock Output Skew (at transmitter) | -0.5 | 0 | 0.5 | ns |
| TskewR | Data to Clock Input Skew (at receiver)<br><br>This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns will be added to the associated clock signal. | 1 | 1.8 | 2.6 | ns |

# 11. Mechanical Dimensions

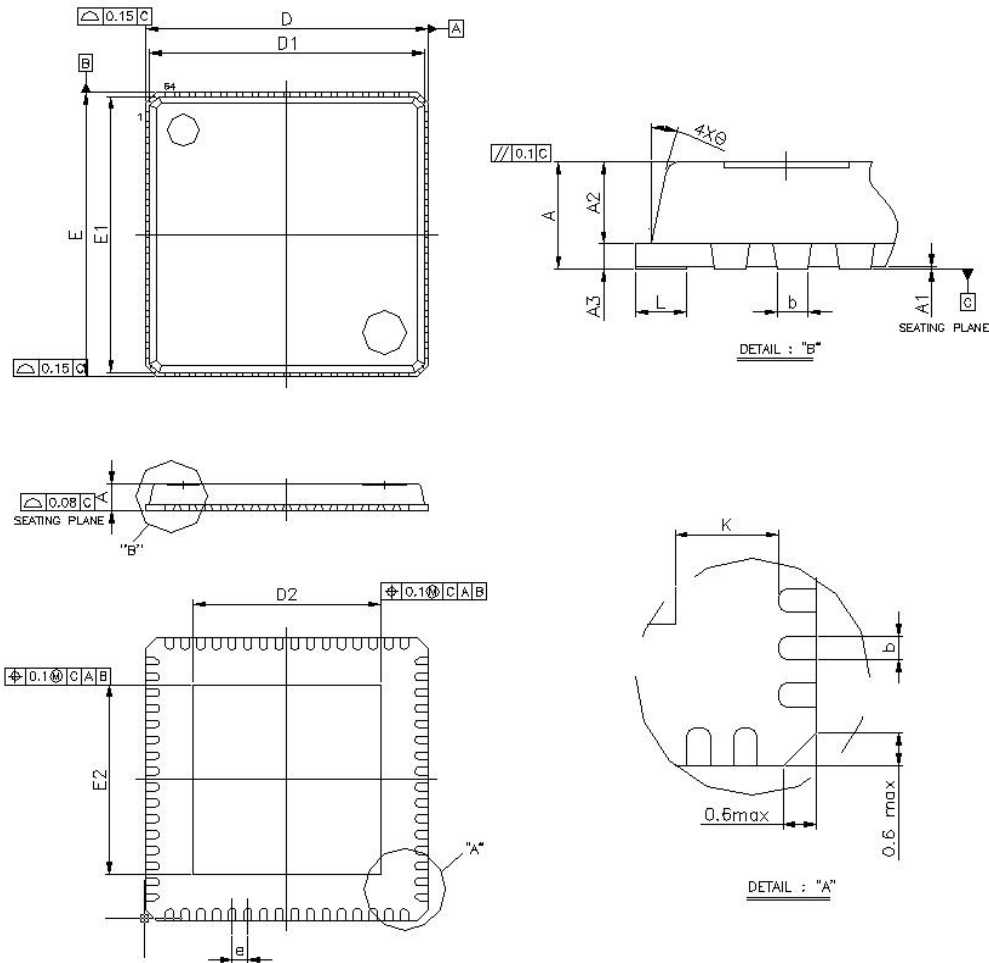## 11.1. RTL8211E-VB/RTL8211E-VL Mechanical Dimensions (48-Pin QFN)
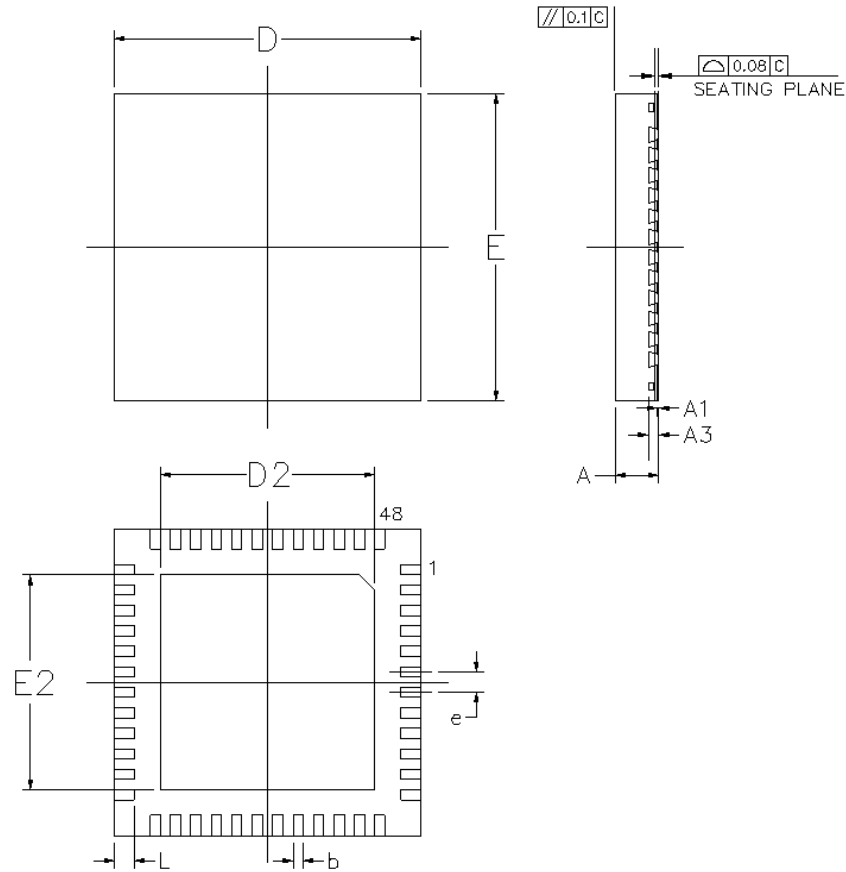


## 11.2. Mechanical Dimensions Notes (RTL8211E-VB/RTL8211E-VL)

| Symbol | Dimension in mm | | | Dimension in inch | | |
|--------|-----|-----|-----|-----|-----|-----|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.75 | 0.85 | 1.00 | 0.030 | 0.034 | 0.039 |
| $A_1$ | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| $A_3$ | 0.20REF | | | 0.008REF | | |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| D/E | 6.00BSC | | | 0.236BSC | | |
| D2/E2 | 4.15 | 4.4 | 4.65 | 0.163 | 0.173 | 0.183 |
| e | 0.40BSC | | | 0.016BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |

*Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).*
*Note 2: REFERENCE DOCUMENT: JEDEC MO-220.*

## 11.3. RTL8211EG-VB Mechanical Dimensions (64-Pin QFN)



## 11.4. Mechanical Dimensions Notes (RTL8211EG-VB)

| Symbol | Dimension in mm | | | Dimension in inch | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| A | 0.75 | 0.85 | 1.00 | 0.030 | 0.034 | 0.039 |
| $A_1$ | 0.00 | 0.02 | 0.05 | 0.000 | 0.001 | 0.002 |
| $A_2$ | 0.55 | 0.65 | 0.80 | 0.022 | 0.026 | 0.032 |
| $A_3$ | 0.20REF | | | 0.008REF | | |
| b | 0.18 | 0.25 | 0.30 | 0.007 | 0.010 | 0.012 |
| D/E | 9.00BSC | | | 0.354BSC | | |
| $D_1/E_1$ | 8.75BSC | | | 0.344BSC | | |
| $D_2/E_2$ | 3.55 | 3.80 | 4.05 | 0.140 | 0.150 | 0.160 |
| e | 0.50BSC | | | 0.020BSC | | |
| L | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| θ | 0º | - | 14º | 0º | - | 14º |

*Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).*
*Note 2: REFERENCE DOCUMENT: JEDEC MO-220.*

# 12. Ordering Information

**Table 68. Ordering Information**

| Part Number | Package | Status |
|---|---|---|
| RTL8211E-VB-CG | 48-Pin QFN with 'Green' Package (Supports 3.3V or 2.5V signaling for RGMII) | MP |
| RTL8211E-VL-CG | 48-Pin QFN with 'Green' Package (Supports 1.5/1.8V RGMII) | MP |
| RTL8211EG-VB-CG | 64-Pin QFN with 'Green' Package (Supports 3.3V or 2.5V signaling for RGMII/GMII) | MP |

*Note: See page 6 (RTL8211E-VB/RTL8211E-VL) & 7 (RTL8211EG-VB) for package identification.*