ZXIC

ZX2AA500

Data Sheet

0.35

深圳市中兴微电子技术有限公司

修改记录

文件编号	版本号	拟制人/修改人	拟制/修改日期	更改理由	主要更改内容（写要点即可）
	V0.1	丁己善	2015-07-09	创建	
	V0.2	丁己善	2015-07-10		增加 PIN 电压域
	V0.21	丁己善	2015-07-14		填写管脚分配列表
	V0.22	丁己善	2015-07-22		增加功耗
	V0.23	丁己善	2015-07-27		修改电口、buck 外围电路，增加 LED 外围电路
	V0.24	丁己善	2015-07-29		修改电口外围电路
	V0.25	丁己善	2015-07-31		PIN53 需增加测试点
	V0.26	丁己善	2015-08-27		根据评审意见修改，增加 RGMII 接口时序和寄存器说明
	V0.27	丁己善	2015-11-25		增加 PHY 地址说明、寄存器配置注意事项和直流特性
	V0.28	丁己善	2015-12-09		增加 BUCK 和 LDO 输入电压说明
	V0.29	丁己善	2015-12-25		AVDD33 电源分类说明
	V0.30	丁己善	2016-01-14		修改电源设计要求
	V0.31	丁己善	2016-01-19		增加环境温度
	V0.32	丁己善	2016-03-23		修改 PHY Identifier Register 初值
	V0.33	丁己善	2016-03-29		修改 model number 读写属性
	V0.34	叶联渲	2016-04-13		更新框图，更新功能点描述，更新部分寄存器描述
	V0.35	丁己善	2016-07-26		修改水印
注 1：每次更改归档文件（指归档到事业部或公司档案室的文件）时，需填写此表。					
注 2：文件第一次归档时，"更改理由"、"主要更改内容"栏写"无"。					

目　录

第1章. 概述

ZX2AA500 芯片实现 GE 以太网的数据信号向物理层转换的功能，完成 802.3 定义的 10M/100M/1000M PHY 的基本功能和扩展功能。本芯片采用单端口设计，提供 10/100/1000 BASE-T 接口，同时可以通过 RGMII 接口连接三速以太网 MAC。

1.1 特性

ZX2AA500 的主要特性如下：

- 支持RGMII-COPPER的工作模式，MAC通过RGMII接口连接本芯片，本芯片在媒体侧支持10BASE-T/100BASE-TX/1000BASE-T接口

- 三速电口可通过自协商或手工配置，配置为10/100/1000三种速率、全双工/半双工及主从模式（主从模式仅限于1000BASE-T）

- 支持10BASE-T电口，在使用非屏蔽五类线时，传输距离不小于100米

- 支持100BASE-TX电口，在使用非屏蔽五类线时，传输距离不小于100米

- 支持1000BASE-T电口，在使用非屏蔽五类线时，传输距离不小于100米

- 支持EEE功能

- 支持MDI/MDIX自交叉功能和网线的差分线对极性翻转功能

- 支持MDI线序翻转功能，方便PCB走线

- RGMII接口支持RGMII V2.0规范，提供正常模式和延时模式

- RGMII接口驱动能力可调

- 提供MDIO接口用于CPU访问

- 支持IEEE 1149.1 JTAG功能

- 56pin VQFN封装，外形封装7mm x 7mm

1.2 应用场景

本芯片适用于 RGMII-COPPER 的场景，通过 RGMII 接口连接到 MAC,通过 COPPER 接口连接媒体侧。本芯片支持 10/100/1000BASE-T 三速，提供自协商和手工配置两种模式。
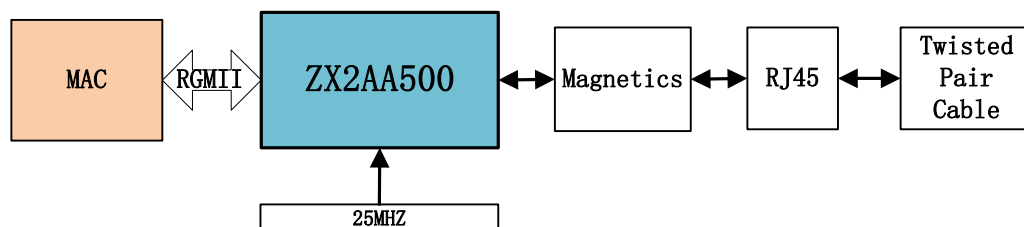
图 1-1 ZX2AA500 适用场景
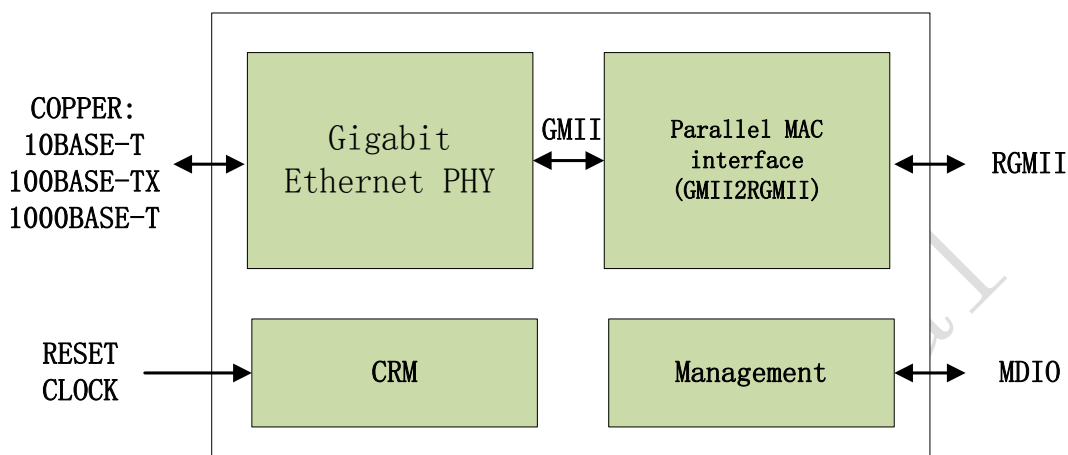
第2章. 功能简介

本芯片的功能框图如下图所示：

图 2-1 系统功能框图

本芯片主要由 GE PHY 模块、GMII/RGMII 接口转换模块、寄存器管理模块、时钟复位模块组成。

发送方向上，本芯片首先从 MAC 接收 RGMII 数据，进行双沿采样和位宽扩展，转换为 GMII 数据，之后将数据转换为 10M/100M/1000M 的标准电口数据发送出去。

接收方向上，本芯片首先接收 10M/100M/1000M 的标准电口数据，转换为 GMII 数据，之后进行采样和位宽压缩，转换为 RGMII 数据，通过 RGMII 接口发送到 MAC。

本芯片还对外提供 MDIO 配置接口/LED 状态显示接口/中断接口/测试接口等。

第3章. 接口说明

3.1 属性说明

本章表格中管脚方向和属性说明缩写如表 3-1 所示:

表 3-1 管脚属性说明

属性缩写	属性说明
I	Input
O	Output
IO	Bi-Directional Input and Output
PU	Internal Pull Up During Power On Reset
PD	Internal Pull Down During Power On Reset
P	Power
G	Ground

3.2 时钟复位接口

表 3-2 时钟复位接口列表

信号名称	数量	管脚编号	方向	电压域	电平标准	上下拉	说明
CLKSEL	1	6	I	VDD3P3	LVCMOS	PD	clock select 0: CMOS 25M clock 1: 25MHZ Crystal Oscillator input,
CLK25	1	31	I	VDD3P3	LVCMOS		CMOS 25M clock
CKXTAL1	1	45	I	AVDD33_OSC			25MHZ Crystal Oscillator input.
CKXTAL2	1	44	O	AVDD33_OSC			25MHZ Crystal Oscillator output.
CLK125	1	9	O	VDD3P3	LVCMOS		125MHz Reference Clock Generated from Internal PLL. This pin should be kept floating if the 125MHz clock is not used by MAC.
PHYRSTB	1	25	I	VDD3P3	LVCMOS		Hardware Reset. Active low. For a complete PHY reset, this pin must be asserted low for at least 10ms. All registers will be cleared after a hardware reset.

本芯片接收来自晶体或时钟源的 25MHz 参考时钟;时钟接法见下表; CLK125 为芯片输出的参考时钟,如果不使用必须板级浮空。

表 3-3 时钟接口列表

CLKSEL	CLK25	CKXTAL1	CKXTAL2	备注
0	接时钟源	接 0	板级浮空	
1	接 0	接晶体	接晶体	
		接时钟源	板级浮空	时钟源电压幅值要求不大于 1.5Vpp，时钟源与 CKXTAL1 之间需要交流耦合 1uF 电容

　　本芯片通过异步复位管脚实现芯片复位，对应管脚为 PHYRSTB。单端输入时，为保证芯片稳定和正常工作，在复位撤销之前，时钟 CLK25 必须保证稳定输入 100 周期以上。晶体输入时，复位释放 15ms CPU 才可通过 MDIO 访问。

3.3　媒体接口

表 3-4 媒体接口列表

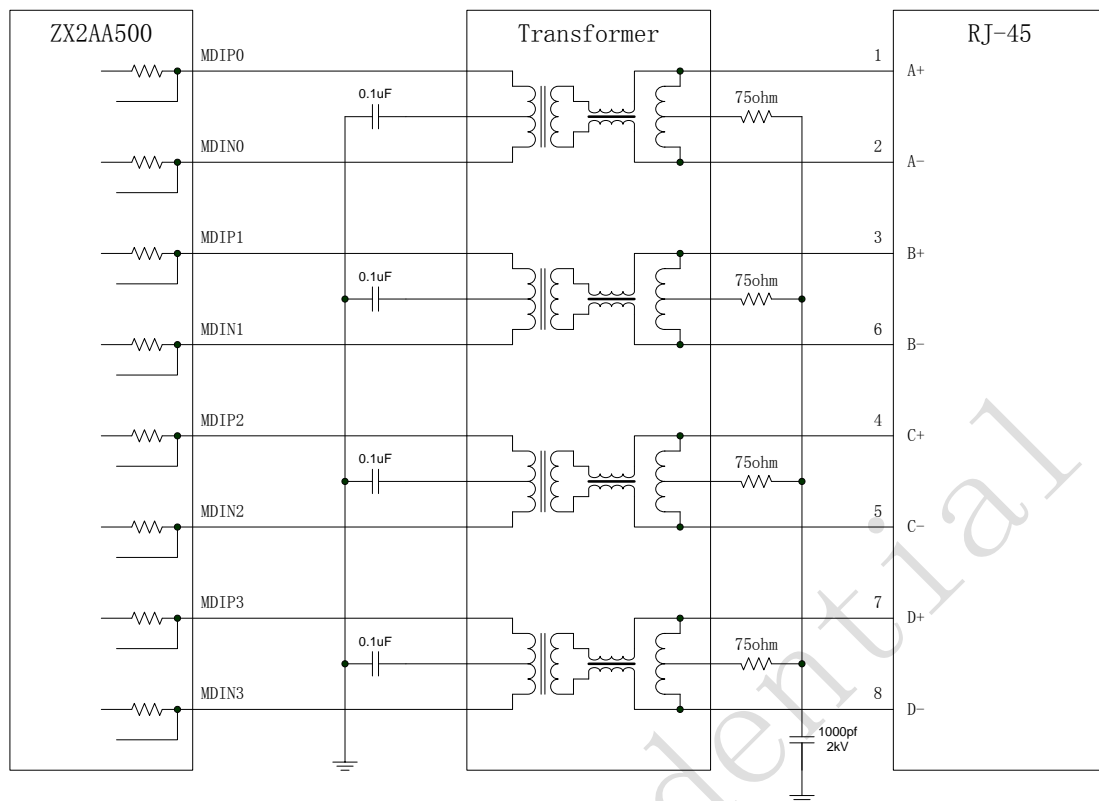| 信号名称	数量	管脚编号	方向	电压域	电平标准	说明
MDIP[0]	1	2	IO	AVDD33_AFE	模拟	Meida Dependent Interface[0]
MDIN[0]	1	1	IO	AVDD33_AFE	模拟	Meida Dependent Interface[0]
MDIP[1]	1	55	IO	AVDD33_AFE	模拟	Meida Dependent Interface[1]
MDIN[1]	1	54	IO	AVDD33_AFE	模拟	Meida Dependent Interface[1]
MDIP[2]	1	52	IO	AVDD33_AFE	模拟	Meida Dependent Interface[2]
MDIN[2]	1	51	IO	AVDD33_AFE	模拟	Meida Dependent Interface[2]
MDIP[3]	1	49	IO	AVDD33_AFE	模拟	Meida Dependent Interface[3]
MDIN[3]	1	48	IO	AVDD33_AFE	模拟	Meida Dependent Interface[3]

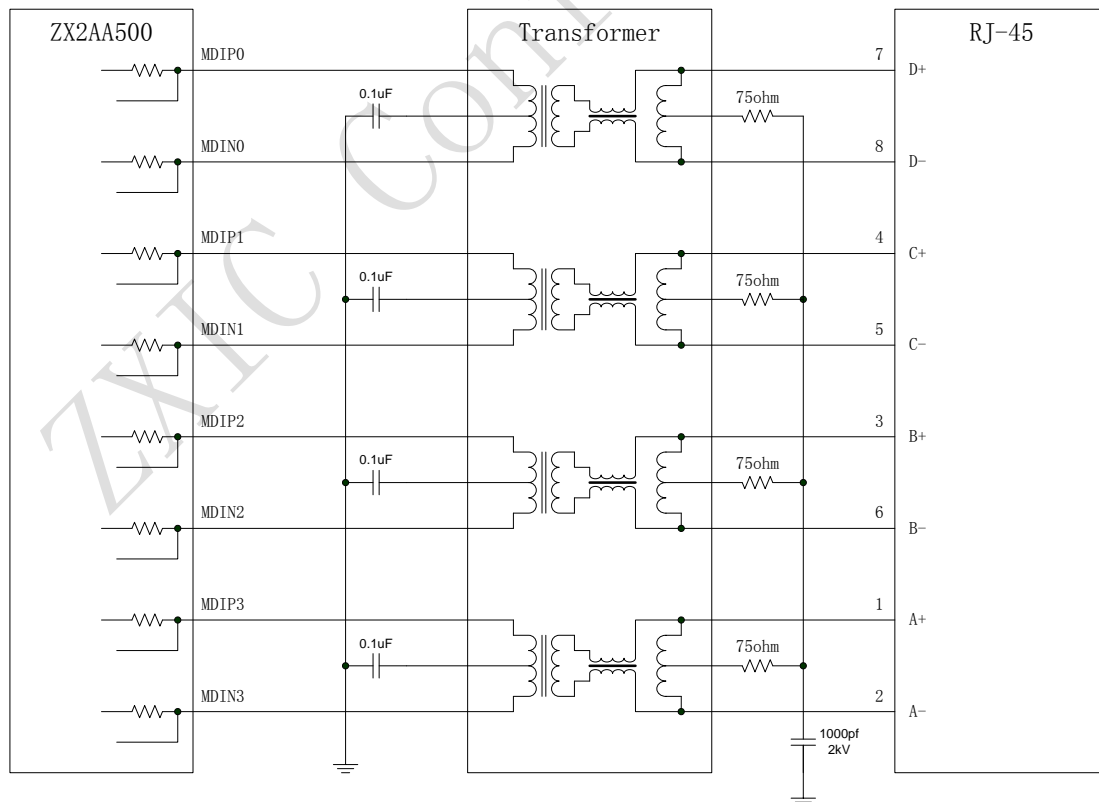　　媒体接口的单板设计可参考图 3-1 或图 3-2。

图 3-1 媒体接口外围电路（线序不翻转）

图 3-2 媒体接口外围电路（线序翻转）

3.4 RGMII 接口

表 3-5 RGMII 接口列表

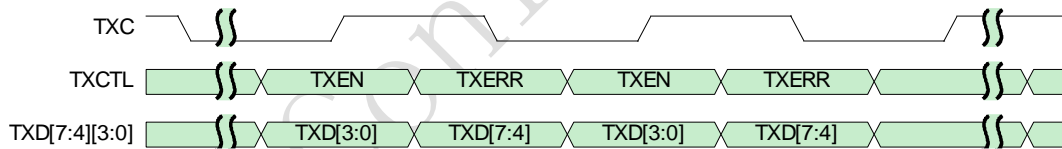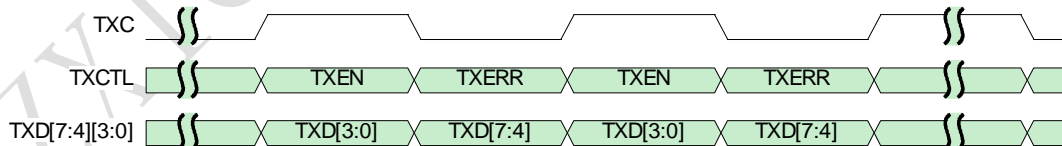| 信号名称	数量	管脚编号	方向	电压域	电平标准	上下拉	说明
TXC	1	19	I	VDD3P3	LVCMOS	PU	RGMII transmit clock，2.5MHz/25MHz/125MHz
TXCTL	1	24	I	VDD3P3	LVCMOS		RGMII transmit control.
TXD0	1	20	I	VDD3P3	LVCMOS	PD	RGMII transmit data input
TXD1	1	21	I	VDD3P3	LVCMOS	PD	RGMII transmit data input
TXD2	1	22	I	VDD3P3	LVCMOS	PD	RGMII transmit data input
TXD3	1	23	I	VDD3P3	LVCMOS	PU	RGMII transmit data input
RXC	1	16	O	VDD3P3	LVCMOS		RGMII receive clock，2.5MHz/25MHz /125MHz
RXCTL	1	11	O	VDD3P3	LVCMOS		RGMII receive control.
RXD0	1	12	O	VDD3P3	LVCMOS		RGMII receive data output
RXD1	1	13	O	VDD3P3	LVCMOS		RGMII receive data output
RXD2	1	14	O	VDD3P3	LVCMOS		RGMII receive data output
RXD3	1	15	O	VDD3P3	LVCMOS		RGMII receive data output

图 3-3 RGMII TX 接口时序（正常模式）

图 3-4 RGMII TX 接口时序（延时模式）
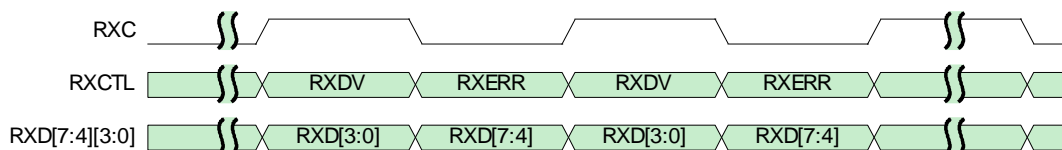
图 3-5 RGMII RX 接口时序（正常模式）
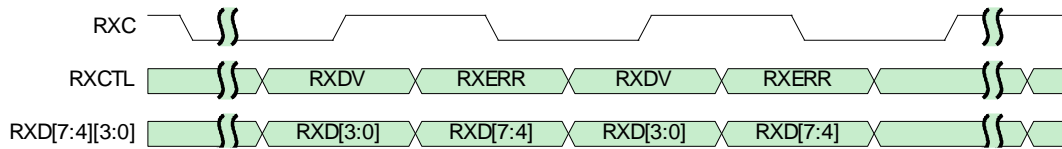
图 3-6 RGMII RX接口时序（延时模式）

3.5 MDIO 接口

表 3-6 MDIO 接口列表

信号名称	数量	管脚编号	方向	电压域	电平标准	上下拉	说明
MDC	1	26	I	VDD3P3	LVCMOS	PU	management Interface clock
MDIO	1	27	IO	VDD3P3	LVCMOS	PU	management interface IO

本芯片通过 MDIO 接口访问和配置芯片内部寄存器，MDIO 接口遵循 IEEE 802.3 第 22 节，MDC 时钟最高频率为 12.5MHz。

PHY 地址高两位为 0，低 3 位与 LED 管脚复用，PHY 地址范围为 0xo 至 0x7，详见 3.6.

3.6 LED/PHY 地址接口

表 3-7 LED/PHY 地址接口列表

信号名称	数量	管脚编号	方向	电压域	电平标准	上下拉	说明
LED0/PHY_AD0	1	29	IO	VDD3P3	LVCMOS	PU	Low=Link Up (Any speed) High=Link Down (Any speed) PHY Address Configuration.
LED1/PHY_AD1	1	30	IO	VDD3P3	LVCMOS	PD	Low=Link Up (Any speed) High=Link Down (Any speed) PHY Address Configuration.
LED2/PHY_AD2	1	28	IO	VDD3P3	LVCMOS	PD	Low=Link Up (Any speed) High=Link Down (Any speed) PHY Address Configuration.

LED0 默认 10M、100M 或 1000M 建立连接前长灭，建立连接后长亮，收发数据时闪烁；
LED1 默认 100M 建立连接前长灭，建立连接后长亮；LED2 默认 1000M 建立连接前长灭，
建立连接后长亮。

LED 外围电路如下图，LED 端口极性可自动调整，如上拉，低表示点亮；如下拉，高表示点亮。如果使用管脚内部默认上下来，下图中 4.7k 电阻可不使用。

PHY Address[:]=Logic 1
LED indication =active low

PHY Address[:]=Logic 0
LED indication =active high
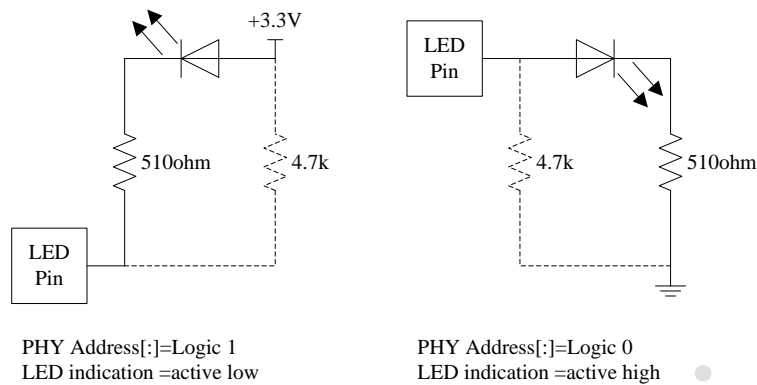
图 3-7 LED 外围电路

3.7 其它接口

表 3-8 其它接口列表

信号名称	数量	管脚编号	方向	电压域	电平标准	上下拉	说明
INTB	1	18	O	VDD3P3	LVCMOS		Interrupt. Set low if status changed; active low. This pin should be kept floating if this function is not used.
RSET	1	4	IO	AVDD33_COM	模拟		Resistor Reference,3.01k 1% res to GND
SVR_CTRL	1	38	I	AVDD33_REG	LVCMOS33		0V: Enable switching regulator 3.3V: Disable switching regulator
AFE_TST_P	1	46	IO	AVDD33_AFE	模拟		analog test pin
AFE_TST_N	1	47	IO	AVDD33_AFE	模拟		analog test pin
TX_TCLK	1	10	O	VDD3P3	LVCMOS		IEEE transmit test clock

管脚 RSET 为模拟参考电阻接口，通过 3.01k 1%精度电阻接地，PCB 布局时外接电阻尽量离 RSET 近，走线尽量粗短。

如果使用内部 3.3V 转 0.9V 电源转换器，SVR_CTRL 外接地；如果不使用内部 3.3V 转 0.9V 电源转换器，SVR_CTRL 外接 3.3V。

管脚 AFE_TST_P/AFE_TST_N 为模拟输出测试管脚，板级增加测试点。

3.8 JTAG 及 DFT 接口

表 3-9 JTAG 及 DFT 接口列表

信号名称	数量	管脚编号	方向	电压域	电平标准	上下拉	说明
TEST_MODE	1	7	I	VDD3P3	LVCMOS	PD	test mode
TRST	1	34	IO	VDD3P3	LVCMOS	PD	JTAG reset
TMS	1	36	IO	VDD3P3	LVCMOS	PD	JTAG mode
TCK	1	33	IO	VDD3P3	LVCMOS	PD	JTAG clock
TDI	1	37	IO	VDD3P3	LVCMOS	PD	JTAG data input
TDO	1	35	IO	VDD3P3	LVCMOS		JTAG data output

管脚 TEST_MODE 接地；管脚 TRST/TMS/TCK/TDI 在芯片内部已做下拉处理，板级可浮空，保险起见，板级也可下拉；管脚 TDO 需浮空。

3.9 电源和地接口

表 3-10 电源和地接口列表

名称	数量	管脚编号	电压(V)	说明
AVDD33_AFE	2	50,56	3.3	AFE 模拟电源。
AVDD33_COM	1	3	3.3	AFE COMMON 模拟电源。
AVDD33_LDO	1	41	3.3	LDO 输入电压
AVDD33_OSC	1	43	3.3	Crystal oscillator 模拟电源，LDO 模拟电源
VDD3P3	3	5,17,32	3.3	IO 数字电源
AVDD33_REG	1	40	3.3	Regulator 电源
REG_OUT	1	39	0.9	regulator 输出电压
DVDD	1	42	0.9	数字核电压
GND	1	EPAD	0	地

如果使用内部 3.3V 转 0.9V 电源转换器，REG_OUT 与 DVDD 通过电感板级互联，见下图；如果不使用内部 3.3V 转 0.9V 电源转换器，REG_OUT 板级浮空，DVDD 外接 0.9V 数字电源。
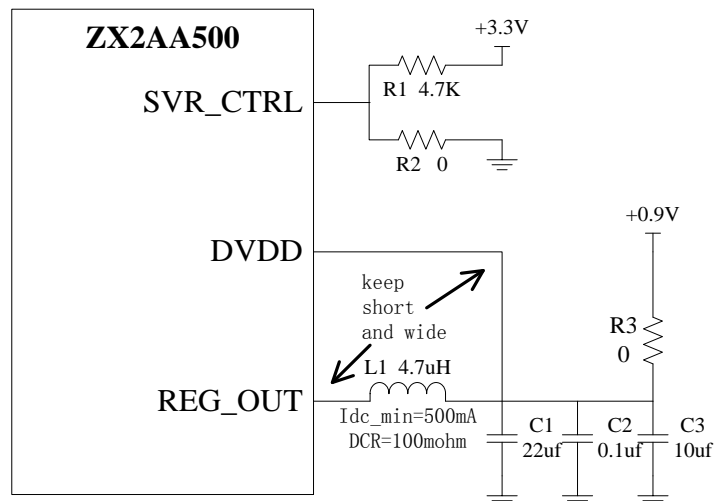
图 3-8 电源外围电路

表 3-11 DVDD power options

Internal SVR	External Power
L1: STUFF	L1: NO STUFF
R3: NO STUFF	R3: STUFF
R1: NO STUFF	R1: STUFF
R2: STUFF	R2: NO STUFF

第4章. 管脚说明

4.1 管脚布局
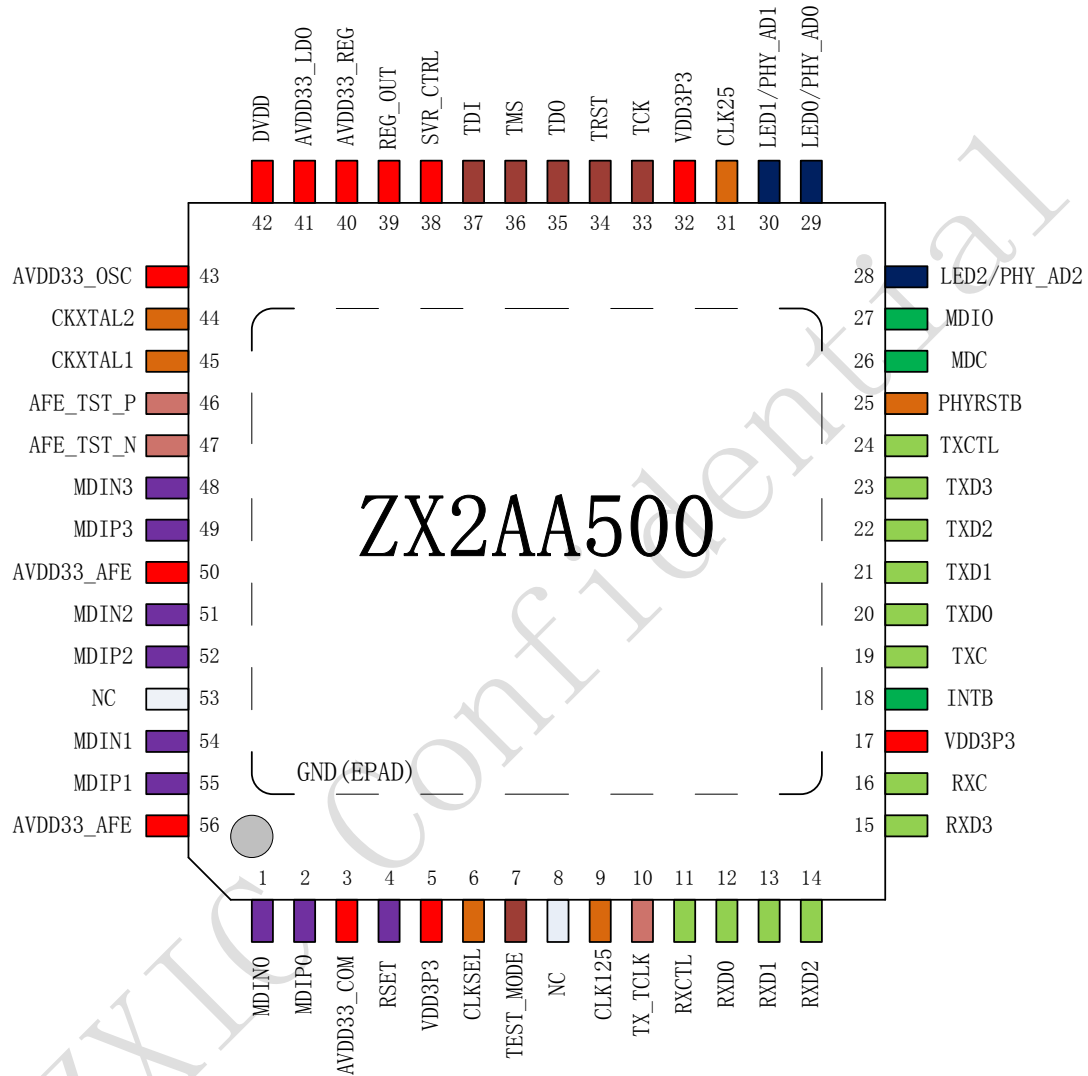
图 4-1 管脚布局

4.2 管脚分配

表 4-1 管脚分配列表

管脚	数量	管脚编号（数量大于 1 的从 MSB 开始）
AFE_TST_N	1	47
AFE_TST_P	1	46
AVDD33_AFE	2	50,56
AVDD33_COM	1	3

管脚	数量	管脚编号（数量大于 1 的从 MSB 开始）
AVDD33_LDO	1	41
AVDD33_OSC	1	43
AVDD33_REG	1	40
CLK125	1	9
CLK25	1	31
CLKSEL	1	6
CKXTAL1	1	45
CKXTAL2	1	44
DVDD	1	42
GND	1	EPAD
INTB	1	18
LED0/PHY_AD0	1	29
LED1/PHY_AD1	1	30
LED2/PHY_AD2	1	28
MDC	1	26
MDIN[0]	1	1
MDIP[0]	1	2
MDIN[1]	1	54
MDIP[1]	1	55
MDIN[2]	1	51
MDIP[2]	1	52
MDIN[3]	1	48
MDIP[3]	1	49
MDIO	1	27
NC	2	8,53
PHYRSTB	1	25
REG_OUT	1	39
RSET	1	4
RXC	1	16
RXCTL	1	11
RXD0	1	12
RXD1	1	13
RXD2	1	14
RXD3	1	15
SVR_CTRL	1	38
TCK	1	33
TDI	1	37
TDO	1	35
TEST_MODE	1	7
TMS	1	36
TRST	1	34
TXC	1	19
TXCTL	1	24
TXD0	1	20
TXD1	1	21
TXD2	1	22

管脚	数量	管脚编号（数量大于1的从 MSB 开始）
TXD3	1	23
TX_TCLK	1	10
VDD3P3	3	5,17,32

注：PIN 53 管脚 NC 为备用测试管脚，需增加测试点。

第5章. 寄存器说明

5.1 术语、首字母和缩略语

本文描述的 ZX2AA500 使用到的相关术语、首字母和缩略语见下表。

表 5-1 术语、首字母缩写和缩略语说明

	缩写	描述
寄存器类型	R	只读。表示寄存器对象（整个寄存器或部分字段）只能由CPU读取，不能被写入。如果向此类寄存器执行写入操作，那么寄存器的值保持不变。
	RW	可读可写。表示寄存器对象（整个寄存器或部分字段）可以被CPU读取或写入。
	RC	读清除。表示寄存器对象（整个寄存器或部分字段）在被CPU读取之后会自动置零。
	RSV	保留位。对应的bit位没有使用，做为保留位使用。
模块名称	ZGPHY	Zxic Gigabit Ethemet PHY子系统
	MGN	配置管理子系统

5.2 寄存器编址总列表

下表列出了寄存器的编址范围。

表 5-2 寄存器编址总列表

编号	子系统名称	开始地址	结束地址	备注
1	ZGPHY	0x00	0x1D	PAGE0
2	ZGPHY	0x1F	0x1F	PAGE0
3	MGN	0x10	0x1D	PAGE1
4	MGN	0x1E	0x1E	PAGE 寄存器

5.3 寄存器功能/配置

表 5-3 Page Address-Page Any,Address 30

位号	字段名称	类型	功能和描述	初始值
15:8	RSV	R	Reserved	0x0
7:0	mdio_page	RW	页寄存器： page=0，访问 zgphy 寄存器 page=1，访问 rgmii、led 配置、gephy 接口配置寄存器	0x0

注意：配置页寄存器为非 0 时，配置完该页相关寄存器后必须配置页寄存器为 0。

表 5-4 Control Register-Page 0,Address 0

位号	字段名称	类型	功能和描述	初始值
15	Reset	RW	1 = PHY reset. 0 = Normal operation. The TruePHY Quintus core automatically clears the reset bit upon completion of the reset sequence. The TruePHY Quintus core sets this bit to 1 during reset.	0x0
14	Loopback	RW	1 = Enables loopback. 0 = Disables loopback. This is the master enable for digital and analog loopback as the standard defines. The loopback control register (address 19) determines the exact type of loopback.	0x0
13	Speed Selection (LSB)	RW	Use this bit and bit 6 (MSB) to configure the link manually. 11 = Reserved. 10 = 1000 Mbits/s. 01 = 100 Mbits/s. 00 = 10 Mbits/s. Setting these bits has no effect unless bit 0.12 is 0. These bits are also used by the PHY to report the technology negotiated in the event of an auto-negotiated or parallel detected link. They become valid once Autonegotiation Complete is asserted.	0x0
12	Autonegotiation Enable	RW	1 = Enables autonegotiation process. 0 = Disables autonegotiation process. When this bit is 0, the determination of link configuration is manual.	0x1
11	Powerdown	RW	1 = Software powerdown. 0 = Normal operation. A configuration input sets the default value of this bit.	0x0
10	Isolate	RW	1 = Isolates PHY from MII. 0 = Normal operation. Setting this bit isolates the PHY from the MII interface or GMII interface.	0x0
9	Restart Autonegotiation	RW	1 = Restarts autonegotiation process. 0 = Normal operation. This bit automatically clears when autonegotiation	0x0

<以上所有信息均为深圳市中兴微电子技术有限公司所有，不得外传>
20

			restarts.	
8	Duplex Mode	RW	1 = Full duplex. 0 = Half duplex. Use this bit to configure the link manually. Setting this bit has no effect unless bit 0.12, is 0. This bit is also used by the PHY to report the technology negotiated in the event of an auto-negotiated or parallel detected link. The bit becomes valid once Autonegotiation Complete is asserted.	0x0
7	Collision Test	RW	1 = Enables IEEE 22.2.4.1.9 collision test. 0 = Disables collision test.	0x0
6	Speed Selection (MSB)	RW	See bit 13.	0x1
5	Unidirectional Enable	R	0 = Enable transmit from media independent interface only when the PHY has determined that a valid link has been established. The PHY does not have the ability to transmit data from the MII regardless of whether or not it has determined that a valid link has been established. This register bit is always 0.	0x0
4:0	RSV	R	Reserved	

表 5-5 Status Register-Page 0,Address 1

位号	字段名称	类型	功能和描述	初始值
15	100BASE-T4	R	0 = Not 100BASE-T4 capable. The TruePHY Quintus core does not support 100BASE-T4 or 100BASE-T2; therefore, this register bit is always 0.	0x0
14	100BASE-X Full Duplex	R	1 = 100BASE-X full-duplex capable. 0 = Not 100BASE-X full-duplex capable.	0x1
13	100BASE-X Half Duplex	R	1 = 100BASE-X half-duplex capable. 0 = Not 100BASE-X half-duplex capable.	0x1
12	10BASE-T Full Duplex	R	1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.	0x1
11	10BASE-T Half Duplex	R	1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.	0x1
10	100BASE-T2 Full Duplex	R	0 = Not 100BASE-T2 full-duplex capable. The TruePHY Quintus core does not support 100BASE-T4 or 100BASE-T2; therefore, this register bit is always 0.	0x0

9	100BASE-T2 Half Duplex	R	0 = Not 100BASE-T2 half-duplex capable. The TruePHY Quintus core does not support 100BASE-T4 or 100BASE-T2; therefore, this register bit is always 0.	0x0
8	Extended Status	R	Extended status information in register 15.	0x1
7	Unidirectional Ability	R	0 = PHY able to transmit from media independent interface only when the PHY has determined that a valid link has been established. The PHY does not have the ability to transmit data from the MII regardless of whether or not it has determined that a valid link has been established, this register bit is always 0.	0x0
6	MF Preamble Suppression	R	Preamble suppressed MFs accepted. The first frame following a reset must have a preamble. Note that the first management frame after a H/W or S/W reset must have a full preamble so as to allow the PHY to synchronize to the station management.	0x1
5	Autonegotiation Complete	R	1 = Autonegotiation process complete. 0 = Autonegotiation process not complete. Upon completion of autonegotiation, this bit becomes 1.	0x0
4	Remote Fault	R	1 = Remote fault detected. 0 = No remote fault detected. This bit indicates the detection of a remote fault. When set, it remains set until it is cleared by reading register 1 via the MI or by PHY reset.	0x0
3	Autonegotiation Ability	R	1 = Autonegotiation capable. 0 = Not autonegotiation capable.	0x1
2	Link Status	R	1 = Link is up. 0 = Link is down. This bit indicates the establishment of a valid link. When this bit clears due to link failure, this bit remains inactive until register 1 is read via the MI.	0x0
1	Jabber Detect	R	1 = Jabber condition detected. 0 = No jabber condition detected.	0x0
0	Extended Capability	R	1 = Extended register capabilities. Indicates that the PHY provides an extended set of capabilities that can be accessed through the extended register set. For a PHY that incorporates a GMII/RGMII, the extended register set consists of all management registers except registers 0, 1, and 15. This register bit is always 1.	0x1

表 5-6 PHY Identifier Register 1-Page 0, Address 2

位号	字段名称	类型	功能和描述	初始值
15:0	PHY Identifier Bits 3:18	R	Organizationally unique identifier (OUI), bits 3:18. The default value is 00-05-3D.	0x0381

表 5-7 PHY Identifier Register 2-Page 0, Address 3

位号	字段名称	类型	功能和描述	初始值
15:10	PHY Identifier Bits 19:24	R	Organizationally unique identifier (OUI), bits 19:24. The default value is 00-05-3D.	0x17
9:4	Model Number	R	Model number. The CORE_OP_CFG pins set the values of this bit.	0x1
3:0	Revision Number	R	Revision number. The CORE_OP_CFG pins set the values of this bit.	0x1

表 5-8 Autonegotiation Advertisement Register-Page 0, Address 4

位号	字段名称	类型	功能和描述	初始值
15	Next Page	RW	1 = Advertise next page ability supported. 0 = Advertise next page ability not supported.	0x0
14	RSV	R	Reserved	
13	Remote Fault	RW	1 = Advertises remote fault detected. 0 = Advertises no remote fault detected.	0x0
12	RSV	R	Reserved	
11	Asymmetric Pause	RW	1 = Advertises asymmetric pause ability. 0 = Advertises no asymmetric pause ability.	0x0
10	Pause Capable	RW	1 = Full-duplex pause operation capable. 0 = Not pause operation capable.	0x0
9	100BASE-T4 Capability	R	0 = Not 100BASE-T4 capable. The TruePHY Quintus core does not support 100BASE-T4; therefore, this register bit is always 0..	0x0
8	100BASE-TX Full-Duplex Capable	RW	1 = 100BASE-TX full-duplex capable. 0 = Not 100BASE-TX full-duplex capable.	0x1
7	100BASE-TX Half-Duplex Capable	RW	1 = 100BASE-TX half-duplex capable. 0 = Not 100BASE-TX half-duplex capable.	0x1
6	10BASE-T Full-Duplex Capable	RW	1 = 10BASE-T full-duplex capable. 0 = Not 10BASE-T full-duplex capable.	0x1
5	10BASE-T Half-Duplex Capable	RW	1 = 10BASE-T half-duplex capable. 0 = Not 10BASE-T half-duplex capable.	0x1
4:0	Selector Field	RW	The selector field advertisement register indicates	00001

| | | | how the advertised technology abilities should be interpreted.
00001 = IEEE 802.3 CSMA/CD. | |

Note: Any write to this register prior to the completion of autonegotiation is followed by a restart of autonegotiation. Also note that this register is not updated following autonegotiation.

表 5-9 Autonegotiation Link Partner Ability Register-Page 0,Address 5

位号	字段名称	类型	功能和描述	初始值
15	Next page	R	1 = Link partner has next page ability. 0 = Link partner does not have next page ability.	0x0
14	Acknowledge	R	1 = Link partner has received link code word. 0 = Link partner has not received link code word. of this bit.	0x0
13	Remote Fault	R	1 = Link partner has detected remote fault. 0 = Link partner has not detected remote fault.	0x0
12	RSV	R	Reserved	
11	Asymmetric Pause	R	1 = Link partner desired asymmetric pause. 0 = Link partner does not desire asymmetric pause.	0x0
10	Pause Capable	R	1 = Link partner is capable of full-duplex pause operation. 0 = Link partner is not capable of full-duplex pause operation.	0x0
9	100BASE-T4 Capability	R	1 = Link partner is 100BASE-T4 capable. 0 = Link partner is not 100BASE-T4 capable.	0x0
8	100BASE-TX Full-Duplex Capable	R	1 = Link partner is 100BASE-TX full-duplex capable. 0 = Link partner is not 100BASE-TX full-duplex capable.	0x0
7	100BASE-TX Half-Duplex Capable	R	1 = Link partner is 100BASE-TX half-duplex capable. 0 = Link partner is not 100BASE-TX half-duplex capable.	0x0
6	10BASE-T Full-Duplex Capable	R	1 = Link partner is 10BASE-T full-duplex capable. 0 = Link partner is not 10BASE-T full-duplex capable.	0x0
5	10BASE-T Half-Duplex Capable	R	1 = Link partner is 10BASE-T half-duplex capable. 0 = Link partner is not 10BASE-T half-duplex capable.	0x0
4:0	Protocol Selector Field	R	Link partner protocol selector field. 00001 = IEEE 802.3 CSMA/CD.	0x0

表 5-10 Autonegotiation Expansion Register-Page 0,Address 6

位号	字段名称	类型	功能和描述	初始值
15:7	RSV	R	Reserved	
6	Receive Next Page Location Able	R	1 = Received Next Page storage location is specified by bit (6.5). Next pages are always stored in register address 8. This register bit is always 1.	0x1
5	Remote Fault	R	Received Next Page Storage Location 1 = Next pages are stored in register address 8 Next pages are always stored in register address 8. This register bit is always 1.	0x1
4	Parallel Detection Fault	R	1 = Parallel link fault detected. 0 = Parallel link fault not detected.	0x0
3	Link Partner Next Page Ability	R	1 = Link partner has next page capability. 0 = Link partner does not have next page capability.	0x0
2	Next Page Capability	R	1 = Local device has next page capability. 0= Local device does not have next page capability.	0x1
1	Page Received	R	1 = New page has been received from link partner. 0 = New page has not been received.	0x0
0	Link Partner Auto-negotiation Ability	R	1 = Link partner has autonegotiation capability. 0 = Link partner does not have autonegotiation capability.	0x0

表 5-11 Autonegotiation Next Page Transmit Register-Page 0,Address 7

位号	字段名称	类型	功能和描述	初始值
15	Next Page	RW	1 = Additional next pages follow. 0 = Sending last next page.	0x0
14	RSV	R	Reserved	
13	Message Page	RW	1 = Formatted page. 0 = Unformatted page.	0x1
12	Acknowledge 2	RW	1 = Complies with message. 0 = Cannot comply with message.	0x0
11	Toggle	R	1 = Previous value of transmitted link code word was logic zero. 0 = Previous value of transmitted link code word was logic one. This ensures that two consecutive next pages cannot be identical.	0x0
10:0	Message/ Unformatted Code Field	RW	Next page message code or unformatted data.	0x1

表 5-12 Link Partner Next Page Register-Page 0, Address 8

位号	字段名称	类型	功能和描述	初始值
15	Next Page	R	1 = Additional next pages follow. 0 = Sending last next page.	0x0
14	Acknowledge	R	1 = Acknowledge. 0 = No acknowledge.	0x0
13	Message Page	R	1 = Formatted page. 0 = Unformatted page. If this bit is set it indicates that the link partner next page contains a predefined message code.	0x0
12	Acknowledge 2	R	1 = Complies with message. 0 = Cannot comply with message.	0x0
11	Toggle	R	1 = Previous value of transmitted link code word was logic zero. 0 = Previous value of transmitted link code word was logic one. This ensures that two consecutive next pages cannot be identical.	0x0
10:0	Message/ Unformatted Code Field	RW	Next page message code or unformatted data.	0x0

表 5-13 1000BASE-T Control Register-Page 0, Address 9

位号	字段名称	类型	功能和描述	初始值
15:13	Test Mode	RW	The test mode register allows the test modes specified in clause 40.6.1.1.2 of std 802.3 to be enabled. 000 = Normal mode. 001 = Test mode 1 – transmit waveform test. 010 = Test mode 2 – master transmit jitter test. 011 = Test mode 3 – slave transmit jitter test. 100 = Test mode 4 – transmit distortion test. 101 = Reserved. 110 = Reserved. 111 = Reserved.	000
12	Master/Slave Configuration Enable	RW	1 = Enables master/slave configuration. 0 = Automatic master/slave configuration.	0x0
11	Master/Slave Configuration Value	RW	1 = Configures PHY as master. 0 = Configures PHY as slave. Setting this bit has no effect unless bit 9.12 is 1.	0x0
10	Port Type	RW	1 = Multiport device (prefers master).	0x0

			0 = Single-port device (prefers slave).	
9	Advertise 1000BASE-T Full-duplex Capability	RW	1 = Advertises 1000BASE-T full-duplex capability. 0 = Advertises no 1000BASE-T full-duplex capability.	0x1
8	Advertise 1000BASE-T Half-duplex Capability	RW	1 = Advertises 1000BASE-T half-duplex capability. 0 = Advertises no 1000BASE-T half-duplex capability.	0x0
7:0	RSV	R	Reserved	

表 5-14 1000BASE-T Status Register-Page 0,Address 10

位号	字段名称	类型	功能和描述	初始值
15	Master/ Slave Configuration Fault	R	1 = Master/slave configuration fault detected. 0 = No master/slave configuration fault detected. When set, this bit remains set until the following actions clear it: Read of register 10 via the MI. Reset. Completion of autonegotiation. Enabling of autonegotiation.	0x0
14	Master/Slave Configuration Resolution	R	Master/Slave Configuration Resolution 1 = Local PHY resolved to master. 0 = Local PHY resolved to slave. This bit is not valid when bit 15 is set to 1.	0x0
13	Local Receiver Status	R	1 = Local receiver OK. 0 = Local receiver not OK. The local receiver status bit reads as 1'b1 when the loc_rcvr_status variable specified in clause 40.4.5.1 of std 802.3 is OK.	0x0
12	Remote Receiver Status	R	1 = Remote receiver OK. 0 = Remote receiver not OK.	0x0
11	Link Partner 1000BASE-T Full-duplex Capability	R	1 = Link partner is capable of 1000BASE-T full duplex. 0 = Link partner not 1000BASE-T full-duplex capable.	0x0
10	Link Partner 1000BASE-T Half-duplex Capability	R	1 = Link partner is 1000BASE-T half-duplex capable. 0 = Link partner not 1000BASE-T half-duplex capable.	0x0
9:8	RSV	R	Reserved	
7:0	Idle Error Count	R	MSB of idle error count.	0x0

| | | | These bits contain a cumulative count of the errors detected when the receiver gets idles and both the local and remote receiver statuses are OK. In the event of overflow, the TruePHY Quintus core holds the count at 255. Reading this register through the MI resets the count to 0. A hardware or software reset also resets the count to 0. | |

表 5-15 Extended Status Register-Page 0, Address 15

位号	字段名称	类型	功能和描述	初始值
15	1000BASE-X Full-duplex	R	0 = Not 1000BASE-X full-duplex capable. The TruePHY Quintus core does not support 1000BASE-X; therefore, this register bit is always 0.	0x0
14	1000BASE-X Half-duplex	R	0 = Not 1000BASE-X half-duplex capable. The TruePHY Quintus core does not support 1000BASE-X; therefore, this register bit is always 0.	0x0
13	1000BASE-T Full-duplex	R	1 = 1000BASE-T full-duplex capable. 0 = Not 1000BASE-T full-duplex capable.	0x1
12	1000BASE-T Half-duplex	R	1 = 1000BASE-T half-duplex capable. 0 = Not 1000BASE-T half-duplex capable.	0x1
11:0	RSV	R	Reserved	

表 5-16 EMI Address Register-Page 0, Address 16

位号	字段名称	类型	功能和描述	初始值
15:0	EMI Address	RW	16-bit address of EMI register. To access an EMI register, the 16-bit address of the EMI register is written into the EMI address register, address 16 and value of the EMI register may be read or written using the EMI data register, address 17.	0x0

表 5-17 EMI Data Register-Page 0, Address 17

位号	字段名称	类型	功能和描述	初始值
15:0	EMI Data	RW	16-bit data value of the EMI register. To access an EMI register, the 16-bit address of the EMI register is written into the EMI address register, address 16 and value of the EMI register	0x0

			may be read or written using the EMI data register, address 17.	

表 5-18 PHY Control Register 2-Page 0,Address 18

位号	字段名称	类型	功能和描述	初始值
15	Resolve MDI/ MDI-X before Forced Speed	RW	1 = Resolves MDI/MDI-X configuration before forcing speed. 0 = Does not resolve MDI/MDI-X configuration before forcing speed. This register bit has no effect when Automatic MDI/MDI-X is clear as the MDI/MDI-X configuration is deemed to be resolved in this case. It is not recommended to clear this bit unless you fully understand how forced speeds are handled in the IEEE standard.	0x1
14	Count False Carrier Events	RW	1 = Rx error counter counts false carrier events. 0 = Rx error counter does not count false carrier events. Count symbol errors (18.13) and count false carrier events (18.14) control the type of errors that the Rx error counter (20.15:0) counts for non-collision packets.	0x0
13	Count Symbol Errors	RW	1 = Rx error counter counts symbol errors. 0 = Rx error counter counts CRC errors. Count symbol errors (18.13) and count false carrier events (18.14) control the type of errors that the Rx error counter (20.15:0) counts for non-collision packets.	0x0
12	RSV	R	Reserved	
11	Manual MDI Pair Flip	RW	1 = Reversed MDI pair order 0 = Normal MDI pair order The manual MDI flip register allows the order of the PHY dimensions to be reversed in order to accommodate alternative board layouts.	0x0
10	Automatic MDI/MDI-X	RW	1 = Enables automatic MDI/MDI-X detection. 0 = Disables automatic MDI/MDI-X detection.	0x1
9	MDI/MDI-X Configuration	RW	1 = Manual MDI-X configuration. 0 = Manual MDI configuration.	0x0
8:3	RSV	R	Reserved	
2	Enable Diagnostics	RW	1 = Enables diagnostics. 0 = Disables diagnostics.	0x0
1:0	RSV	R	Reserved	

表 5-19 Loopback Control Register-Page 0, Address 19

位号	字段名称	类型	功能和描述	初始值
15	MII	RW	1 = MII loopback selected. 0 = MII loopback not selected.	0x0
14:13	RSV	R	Reserved	
12	All Digital	RW	1 = All digital loopback selected. 0 = All digital loopback not selected.	0x1
11:10	RSV	R	Reserved	
9	Remote	RW	1 = Remote loopback enabled. 0 = Remote loopback disabled. If the Rx Suppression bit (19.8) is clear then the PHY will also pass any data that it receives on to the ASIC core. If the Rx Suppression bit is set then the PHY will not send any data to the ASIC core.	0x0
8	Rx Suppression	RW	1 = Suppress Rx data during loopback. 0 = Forward Rx data during loopback.	0x0
7	External Cable	RW	1 = External cable loopback enabled. 0 = External cable loopback disabled.	0x0
6	Tx Suppression	RW	1 = Suppress Tx during all digital loopback. 0 = Do not suppress Tx during all digital loop back. This bit has no effect if all digital loopback is not enabled.	0x1
5:1	RSV	R	Reserved	
0	Force Link Status	RW	1 = Force link status okay in MII loopback. 2 = Force link status not okay in MII loopback. Use this bit to force link status okay during MII loopback. In MII loopback, the link status bit is not set unless using force link status. In all other loopback modes, the link status bit is set when the link comes up.	0x1

表 5-20 RX Error Counter Register-Page 0, Address 20

位号	字段名称	类型	功能和描述	初始值
15:0	Rx Error Counter	R	16-bit Rx error counter. Reference bits 18.13 and 8.14 for error type descriptions. This register is clear-on-read.	0x0

表 5-21 Management Interface (MI) Control Register-Page 0, Address 21

位号	字段名称	类型	功能和描述	初始值

15:4	RSV	R	Reserved	0x0
3	Energy-Detect Powerdown Enable	RW	1 = Enables energy-detect powerdown. 0 = Disables energy-detect powerdown.	0x0
2	Energy-Detect Powerdown Transmit Enable	RW	1 = Enables NLP transmission during energy-detect powerdown. 0 = Disables NLP transmission during energy-detect powerdown. If enabled it allows the PHY to occasionally transmit a single pulse on both dimension 0 and dimension 1 while it is in energy detect powerdown. The idea is to avoid the lock-up condition that could otherwise arise if the PHYs at either end of a link were both in energy detect powerdown.	0x1
1:0	RSV	R	Reserved	

表 5-22 PHY Configuration Register-Page 0, Address 22

位号	字段名称	类型	功能和描述	初始值
15	CRS Transmit Enable	RW	1 = Enables CRS on transmit in half-duplex mode. 0 = Disables CRS on transmit.	0x0
14:12	RSV	R	Reserved	
11:10	Automatic Speed Downshift Mode	RW	00 = Disables automatic speed downshift. 01 = 10BASE-T downshift enabled. 10 = 100BASE-TX downshift enabled. 11 = 100BASE-TX and 10BASE-T enabled. If automatic speed downshift is active and the PHY fails to autonegotiate at 1000BASE-T, the PHY falls back to attempt a connection at 100BASE-TX and, subsequently, 10BASE-T. This cycle repeats. If the link breaks at any speed, the PHY restarts this process by reattempting connection at the highest possible speed (e.g., 1000BASE-T).	0x3
9:8	RSV	R	Reserved	
7	Alternate Next-Page	RW	1 = Enables manual control of 1000BASE-T next pages only. 0 = Normal operation of 1000BASE-T next page exchange	0x0
6	Group MDIO Mode Enable	RW	1 = Enables group MDIO mode. 0 = Disable Group MDIO mode. When this bit is set, the PHY processes MDIO accesses to the group address 31 as if they are accesses to its own PHY address.	0x0

5	Transmit Clock Enable	RW	1 = Enables output of mixer clock (transmit clock in 1000BASE-T). 0 = Disables output. When this bit is set, the transmit test clock is available on pin TX_TCLK.	0x0
4:0	RSV	R	Reserved	

表 5-23 PHY Control Register-Page 0, Address 23

位号	字段名称	类型	功能和描述	初始值
15:14	RSV	R	Reserved	
13	LNK_EN	RW	1 = Enables linking. 0 = Disables linking. When this bit is set, the PHY attempts to establish a link with a remote partner and monitors the MDI for link pulses. When this bit is cleared, the PHY takes down any active link, goes into standby, and does not respond to link pulses from a remote link partner.	0x1
12:10	Link Attempts Before Automatic Speed Downshift	RW	000 = 1. 001 = 2. 010 = 3. 011 = 4. 100 = 5. 101 = 6. 110 = 7. 111 = 8	0x4
9:8	RSV	R	Reserved	
7	Link Partner Detected	R	1 = Link partner detected. 0 = Link partner not detected When linking is disabled, the PHY automatically monitors for the appearance of a link partner and sets this bit if it detects a link partner. Clearing LNK_EN (23.13 = 0) disables linking.	0x0
6	Jabber Enable (10BASE-T)	RW	1 = Disables jabber. 0 = Normal operation.	0x1
5	SQE Test Enable (10BASE-T)	RW	1 = Enables the 10BASE-T signal quality error message (SQE) test function. 0 = Disables the 10BASE-T SQE test function.	0x0
4	10BASE-T MAU Loopback Enable	RW	1 = Enables MAU loopback function (half-duplex only). 0 = Disables MAU loopback function.	0x0
3:2	10BASE-T Preamble Length	RW	00 = 10BASE-T preamble length of 0 octets in the received frames sent over the MII. 01 = 10BASE-T preamble length of 1 octets. 10 = 10BASE-T preamble length of 2 octets. 11 = 10BASE-T preamble length of 7 octets.	10
1	RSV	R	Reserved	
0	Force Interrupt	RW	1 = Asserts MDINT pin. 0 = Deasserts MDIN pin.	0x0

表 5-24 Interrupt Mask Register-Page 0, Address 24

位号	字段名称	类型	功能和描述	初始值
15:10	RSV	R	Reserved	
9	MDIO Sync Lost	RW	1 = Enables interrupt. 0 = Disables interrupt.	0x0
8	Autonegotiation Status Change	RW	1 = Enables interrupt. 0 = Disables interrupt.	0x0
7	CRC Errors	RW	1 = Enables interrupt. 0 = Disables interrupt.	0x0
6	Next Page Received	RW	1 = Enables interrupt. 0 = Disables interrupt.	0x0
5	Idle Error Counter Full	RW	1 = Enables interrupt. 0 = Disables interrupt.	0x0
4	FIFO Overflow/ Underflow	RW	1 = Enables interrupt. 0 = Disables interrupt.	0x0
3	Receive Status Change	RW	1 = Enables interrupt. 0 = Disables interrupt.	0x0
2	Link Status Change	RW	1 = Enables interrupt. 0 = Disables interrupt.	0x0
1	Automatic Speed Downshift	RW	1 = Enables interrupt. 0 = Disables interrupt.	0x0
0	Hardware Interrupt Enable	RW	1 = Enables interrupt. 0 = Disables interrupt.	0x0

表 5-25 Interrupt Status Register-Page 0, Address 25

位号	字段名称	类型	功能和描述	初始值
15:10	RSV	R	Reserved	
9	MDIO Sync Lost	R	1 = Event has occurred. 0 = Event has not occurred. When suppressing the MF preamble suppression (MI register address 1, bit6), the PHY can lose synchronization if there is a glitch at the interface. The PHY can recover when a single frame with a preamble is sent to it. The MDIO sync lost interrupt can be used to detect loss of synchronization and, thus, enable recovery.	0x0
8	Autonegotiation Status Change	R	1 = Event has occurred. 0 = Event has not occurred.	0x0
7	CRC Errors	R	1 = Event has occurred. 0 = Event has not occurred.	0x0

6	Next Page Received	R	1 = Event has occurred. 0 = Event has not occurred.	0x0
5	Idle Error Counter Full	R	1 = Event has occurred. 0 = Event has not occurred.	0x0
4	FIFO Overflow/ Underflow	R	1 = Event has occurred. 0 = Event has not occurred.	0x0
3	Receive Status Change	R	1 = Event has occurred. 0 = Event has not occurred.	0x0
2	Link Status Change	R	1 = Event has occurred. 0 = Event has not occurred.	0x0
1	Automatic Speed Downshift	R	1 = Event has occurred. 0 = Event has not occurred.	0x0
0	Hardware Interrupt Enable	R	1 = Event has occurred. 0 = Event has not occurred. Only enabled interrupts contribute to the generation of MII Interrupt Pending. When the Hardware Interrupt Enable register bit (24.0) is set the hardware interrupt pin (MDINT) asserts (active-high) if Interrupt Pending is set.	0x0

表 5-26 PHY Status Register-Page 0, Address 26

位号	字段名称	类型	功能和描述	初始值
15	PHY in Standby Mode	R	1 = PHY in standby mode. 0 = PHY not in standby mode. This bit indicates that the PHY is in standby mode The PHY enters standby mode when LNK_EN is cleared (23.13 = 0) and exits standby mode and attempts to autonegotiate a link when LNK_EN is set (23.13 = 1).	0x0
14:13	Autonegotiation Fault Status	R	11 = Reserved. 10 = Master/slave autonegotiation fault. 01 = Parallel detect autonegotiation fault. 00 = No autonegotiation fault.	0x0
12	Autonegotiation Status	R	1 = Autonegotiation is complete. 0 = Autonegotiation not complete.	0x0
11	Pair Swap on Pairs A and B	R	1 = Pairs A and B are swapped. 0 = Pairs A and B are not swapped.	0x0
10	Polarity Status	R	1 = Polarity is inverted (10BASE-T only). 0 = Polarity is normal (10BASE-T only).	0x0
9:8	Speed Status	R	11 = Undetermined. 10 = 1000BASE-T. 01 = 100BASE-TX.	11

位号	字段名称	类型	功能和描述	初始值
			00 = 10BASE-T	
7	Duplex Status	R	1 = Full duplex. 0 = Half duplex.	0x0
6	Link Status	R	1 = Link is up. 0 = Link is down.	0x0
5	Transmit Status	R	1 = PHY is transmitting a packet. 0 = PHY is not transmitting a packet.	0x0
4	Receive Status	R	1 = PHY is receiving a packet. 0 = PHY is not receiving a packet.	0x0
3	Collision Status	R	1 = Collision is occurring. 0 = Collision not occurring.	0x0
2	Autonegotiation Enabled	R	1 = Both partners have autonegotiation enabled. 0 = Both partners do not have autonegotiation enabled.	0x0
1	Link partner advertised PAUSE	R	1 = Link partner advertised PAUSE. 0 = Link partner did not advertised PAUSE.	0x0
0	Link partner advertised Asym metric PAUSE	R	1 = Link partner advertised Asymmetric PAUSE. 0 = Link partner did not advertised Asymmetric PAUSE.	0x0

表 5-27 LED Control Register-Page 0, Address 27

位号	字段名称	类型	功能和描述	初始值
15	Two-Color Mode LED_100/LED_10	RW	1 = Two-color mode for LED_100 and LED_10. 0 = Normal mode for LED_100 and LED_10. If two-color mode is active for pair LED_100 and LED_10, the signal output for LED_100 equals (LED_100 AND).For the case where LED_100 and LED_10 are not mutually exclusive (e.g., duplex and collision), this mode can simplify the external circuitry because it ensures either LED_100 or LED_10 is on, and not both at the same time. The same rule applies to pair LED_LNK/ACT and LED_1000.	0x0
14	Two-Color Mode LED_LNK/ACT / LED_1000	RW	1 = Two-color mode for LED_LNK/ACT and LED_1000. 0 = Normal mode for LED_LNK/ACT and LED_1000. The same rule applies to pair LED_LNK/ACT and LED_1000 as described for pair LED_100 and LED_10 above.	0x0
13	LED_10 Extended Modes	RW	1 = Extended modes for LED_10. 0 = Standard modes for LED_10.	0x0

12	LED_100 Extended Modes	RW	1 = Extended modes for LED_100. 0 = Standard modes for LED_100.	0x0
11	LED_1000 Extended Modes	RW	1 = Extended modes for LED_1000. 0 = Standard modes for LED_1000.	0x0
10	LED_LNK/ACT Extended Modes	RW	1 = Extended modes for LED_LNK/ACT. 0 = Standard modes for LED_LNK/ACT.	0x0
9:8	RSV	R	Reserved	
7:4	LED Blink Pattern Pause	RW	LED blink pattern pause cycles.	0x0
3:2	LED Pulse Duration	RW	00 = Stretch LED events to 32ms. 01 = Stretch LED events to 64 ms. 10 = Stretch LED events to 104 ms. 11 = Reserved. Program the pulse duration for the setting 27.3:2 = 11 in the range 0 ms to 2 s, in steps of 4 ms using the extended register set.	0x0
1	LED Output Disable	RW	1 = Disables LED outputs. 0 = Enables LED outputs. The LED_CFG pins at reset set the default value of this bit.	0x1
0	Pulse Stretch 0	RW	1 = Enable pulse stretching of LED functions: transmit activity, receive activity, and collision. 0 = Disable pulse stretching of LED functions: transmit activity, receive activity, and collision.	0x1

表 5-28 LED Control Register 2-Page 0, Address 28

位号	字段名称	类型	功能和描述	初始值
15:12	LED_10	RW	In accordance with bits 3:0.	0x2
11:8	LED_100	RW	In accordance with bits 3:0.	0x1
7:4	LED_1000	RW	In accordance with bits 3:0.	0x0
3:0	LED_LNK/ACT	RW	Standard modes 0000 = 1000BASE-T. 0001 = 100BASE-TX. 0010 = 10BASE-T. 0011 = 1000BASE-T on, 100BASE-TX blink. 0100 = Link established. 0101 = Transmit. 0110 = Receive. 0111 = Transmit or receive activity. 1000 = Full duplex. 1001 = Collision. 1010 = Link established (on) and activity (blink). 1011 = Link established (on) and receive (blink).	0xa

1100 = Full duplex (on) and collision (blink).

1101 = Blink. 1110 = On. 1111 = Off.

Extended modes

0000 = 10BASE-T or 100BASE-TX.

0001 = 100BASE-TX or 1000BASE-T.

0010 = 10BASE-T (on) and activity (blink).

0011 = 100BASE-TX (on) and activity (blink).

0100 = 1000BASE-T (on) and activity (blink).

0101 = 10BASE-T or 100BASE-TX (on) and activity (blink).

0110 = 100BASE-TX or 1000BASE-T (on) and activity (blink).

0111 = 10BASE-T or 1000BASE-T.

1000 = 10BASE-T or 1000BASE-T (on) and activity (blink).

1xxx = Reserved.

表 5-29 LED Control Register 3-Page 0, Address 29

位号	字段名称	类型	功能和描述	初始值
15:14	LED Blink Pattern Address	RW	Select LED blink pattern register set. 00 = Select register set for LED_LNK/ACT. 01 = Select register set for LED_1000. 10 = Select register set for LED_100. 11 = Select register set for LED_10.	0x0
13:8	LED Blink Pattern Frequency	RW	LED blink pattern clock frequency divide ratio. The default pattern is a 512-ms blink.	0x1F
7:0	LED Blink Pattern	RW	LED blink pattern. The default pattern is a 512-ms blink.	0x55

表 5-30 Diagnostics Status Register (Link Analysis)-Page 0, Address 31

位号	字段名称	类型	功能和描述	初始值
15	RSV	R	Reserved	
14	Pair Swap on Pairs C and D	R	1 = Pairs C and D are swapped (1000BASE-T only). 0 = Pairs C and D are not swapped (1000BASE-T only). When setting this bit, the PHY detects the crossover of the received pair 2 (RJ-45 pins 4 and 5) and pair 3 (RJ-45 pins 7 and 8).	0x0
13	Polarity on Pair D	R	1 = Polarity on pair D is inverted (1000BASE-T only).	0x0

			0 = Polarity on pair D is normal (1000BASE-T only).	
12	Polarity on Pair C	R	1 = Polarity on pair C is inverted (1000BASE-T only). 0 = Polarity on pair C is normal (1000BASE-T only).	0x0
11	Polarity on Pair B	R	1 = Polarity on pair B is inverted (10BASE-T or 1000BASE-T). 0 = Polarity on pair B is normal (10BASE-T or 1000BASE-T).	0x0
10	Polarity on Pair A	R	1 = Polarity on pair A is inverted (10BASE-T or 1000BASE-T). 0 = Polarity on pair A is normal (10BASE-T or 1000BASE-T).	0x0
9:1	RSV	R	Reserved	
0	Excessive Pair Skew	R	1 = Excessive pair skew (1000BASE-T only). 0 = Not excessive pair skew (1000BASE-T only). Detect excessive pair skew in 1000BASE-T by detecting no scrambler acquisition and no establishment of a 1000BASE-T link. In this case, the PHY usually reverts to 100BASE-TX or 10BASE-T. Other scrambler acquisition errors can be mistaken as excessive pair skew.	0x0

表 5-31 Soft Reset Register-Page 1, Address 16

位号	字段名称	类型	功能和描述	初始值
15:2	RSV	R	Reserved	0x0
1	zgphy_soft_rstn	RW	zgphy 软复位，低有效	0x1
0	RSV	R	Reserved	0x1

表 5-32 Rgmii config Register-Page 1, Address 17

位号	字段名称	类型	功能和描述	初始值
15:4	RSV	R	Reserved	0x0
3	rgmii_isolate_en	RW	rgmii 接口 isolate 使能，1：isolate，0：normal	0x0
2	rgmii_tx_clk_delay_en	RW	rgmii tx clock 延时使能，1 延时 1.5~2ns，0 不延时	0x1
1	rgmii_rx_clk_delay_en	RW	rgmii rx clock 延时使能，1 延时 1.5~2ns，0 不延时	0x1
0	RSV	R	Reserved	0x1

表 5-33 LED Manual Config Register-Page 1, Address 27

位号	字段名称	类型	功能和描述	初始值
15:6	RSV	R	Reserved	0x0
5:3	manual_cfg_en	RW	分别配置 led0/led1/led2 是否使用手动配置	0x0
2:0	manual_cfg	RW	分别配置 led0/led1/led2 使用手动配置的值，0：表示 led 高点亮，1：表示 led 低点亮	0x0

表 5-34 LED Control register-Page 1, Address 28

位号	字段名称	类型	功能和描述	初始值
15:12	RSV	R	Reserved	0x0
11:9	led_act_ctrl	RW	分别配置 led_act 到 led0/led1/led2 的连接，为 1 表示连接上	0x1
8:6	led2_ctrl	RW	分别配置 led2 到 led10/led100/led1000 的连接，为 1 表示连接上	0x4
5:3	led1_ctrl	RW	分别配置 led1 到 led10/led100/led1000 的连接，为 1 表示连接上	0x2
2:0	led0_ctrl	RW	分别配置 led0 到 led10/led100/led1000 的连接，为 1 表示连接上	0x0

第6章. 电气特性

6.1 电源需求

芯片工作需要的电源种类如表 3-10 所示，以下分别对各个电源进行描述。

6.1.1 数字电源 VDD3P3 设计要求

数字电源 VDD3P3 网络和其他电源网络需要磁珠隔离，电源管脚旁边放置 0.1uF 电容。

6.1.2 模拟电源 AVDD33_AFE 设计要求

模拟电源 AVDD33_AFE 网络和数字电源 VDD3P3 网络需要磁珠隔离，管脚旁边放置 0.1uF 电容。

6.1.3 模拟电源 AVDD33_COM 设计要求

模拟电源 AVDD33_COM 网络和数字电源 VDD3P3 网络需要磁珠隔离，管脚旁边放置 0.1uF 电容；AVDD33_COM 要求较高，尽量避免干扰。

6.1.4 模拟电源 AVDD33_LDO 设计要求

模拟电源 AVDD33_LDO 网络和数字电源 VDD3P3 网络需要磁珠隔离， AVDD33 管脚旁边放置 10uF 和 0.1uF 电容。

6.1.5 模拟电源 AVDD33_OSC 设计要求

模拟电源 AVDD33_OSC 网络和数字电源 VDD3P3 网络需要磁珠隔离，管脚旁边放置 0.1uF 电容。

6.1.6 电源 AVDD33_REG 设计要求

AVDD33_REG 为 buck 电源，会产生干扰，管脚旁边需放置 22uF 和 0.1uF 电容。

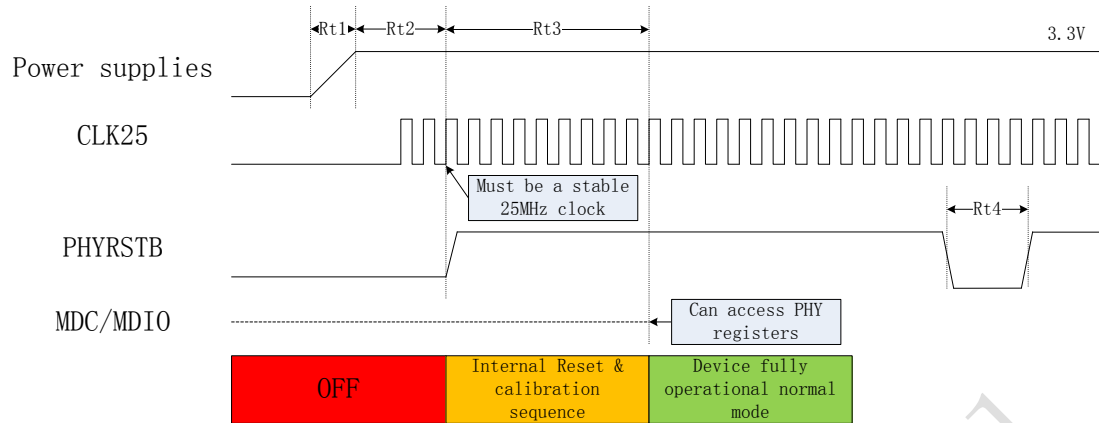### 6.1.7 核电源 DVDD 设计要求

电源管脚旁边放置 0.1uF 电容。

6.2 上电顺序

<以上所有信息均为深圳市中兴微电子技术有限公司所有，不得外传>

图 6-1 上电顺序

表 6-1 上电顺序参数

Symbol	Description	Min	Typical	Max	Units
Rt1	3.3V rise time	0.01	–	2	ms
Rt2	Reset time	10	–	–	ms
Rt3	Internal reset & calibration time	22	–	–	ms
Rt4	Reset time when normal mode	20	–	–	us

注：AVDD33_AFE/AVDD33_COM/ AVDD33_LDO/ AVDD33_OSC/AVDD33_REG 和 VDD3P3 同时上电，DVDD 如果外接 0.9V 数字电源，上电时间晚于其他电源。

6.3 电源参数

芯片正常工作时电源和温度参数如下表所示。

表 6-2 芯片电源参数

电源名称	最小	典型	最大	误差	单位
AVDD33_AFE	3.135	3.3	3.465	5%	V
AVDD33_COM	3.135	3.3	3.465	5%	V
AVDD33_LDO	3.135	3.3	3.465	5%	V
AVDD33_OSC	3.135	3.3	3.465	5%	V
AVDD33_REG	3.135	3.3	3.465	5%	V

<以上所有信息均为深圳市中兴微电子技术有限公司所有，不得外传>

DVDD	0.855	0.9	0.945	5%	V
VDD3P3	3.135	3.3	3.465	5%	V
结温范围	-40		125		℃
环境温度	-40		70		℃
注：电压指芯片管脚处					

6.4 功耗

芯片工作时各个电源最大电流和功耗如表 6-3 和表 6-4 所示。

表 6-3 芯片功耗参数（DVDD 使用内部电源）

电源名称	典型电压(V)	最大电流(mA)	峰值电流(mA)	功耗(W)
AVDD33	3.3	114.8	114.8	0.379
VDD3P3	3.3	38.9	38.9	0.129
Total				0.508

表 6-4 芯片功耗参数（DVDD 使用外部电源）

电源名称	典型电压(V)	最大电流(mA)	峰值电流(mA)	功耗(W)
AVDD33	3.3	99.3	99.3	0.328
VDD3P3	3.3	43.5	43.5	0.144
DVDD	0.9	46	46	0.042
Total				0.514

6.5 直流特性

表 6-5 直流特性

Parameter	Symbol	Minimum	Maximum	Units	Conditions
Input High	Vih	2.0	VDD3P3+0.3	V	
Input Low	Vil	-0.3	0.8	V	
Output High	Voh	2.4	VDD3P3	V	
Output Low	Vol	0	0.4	V	
Input Hystersis	Hys	300		mV	
Input Leakage	IZ	-	10	uA	OE=0, PAD from 0 to VDD3P3.

6.6 交流特性

6.7 ESD 指标

芯片各项 ESD 指标如下表所示。

表 6-6 芯片 ESD 参数

参数	最大值(V)
Human Body Model (HBM) per EIA	±2000 V

第7章. 封装特性

7.1 封装机械特性

本芯片采用 7x7 mm² VQFN 封装，包含 57 个管脚，最小管脚距离 0.4mm，芯片封装机械特性如图 7-1 和图 7-2 所示。

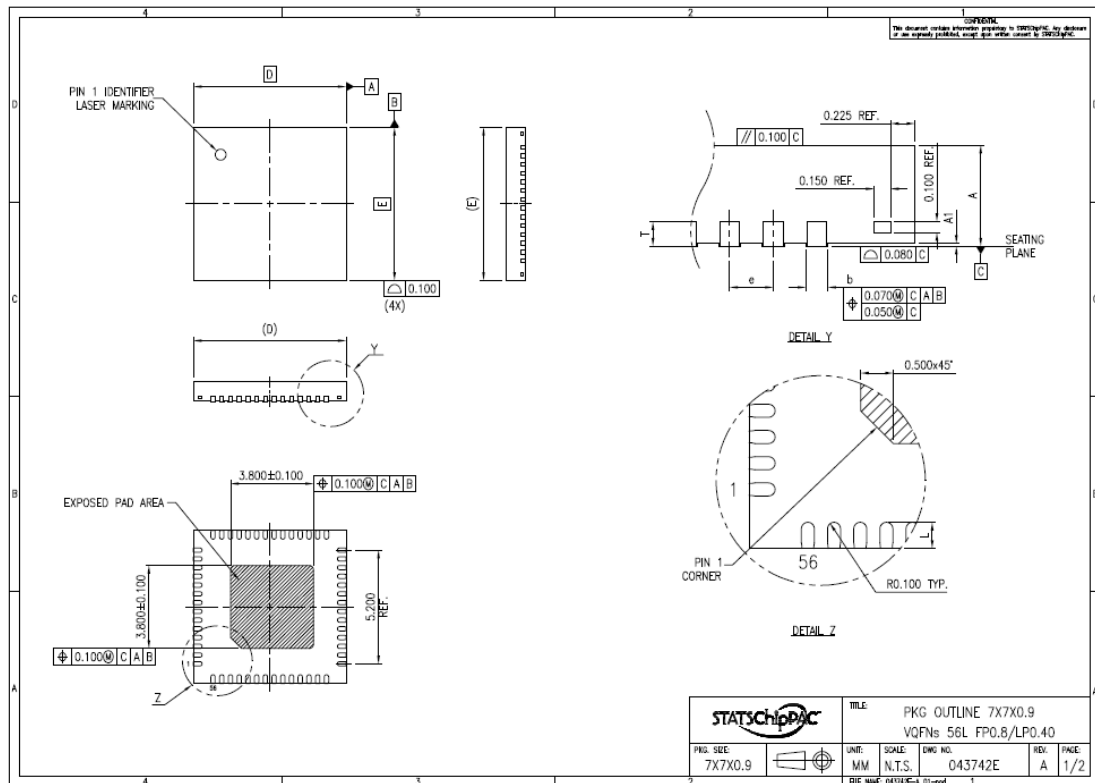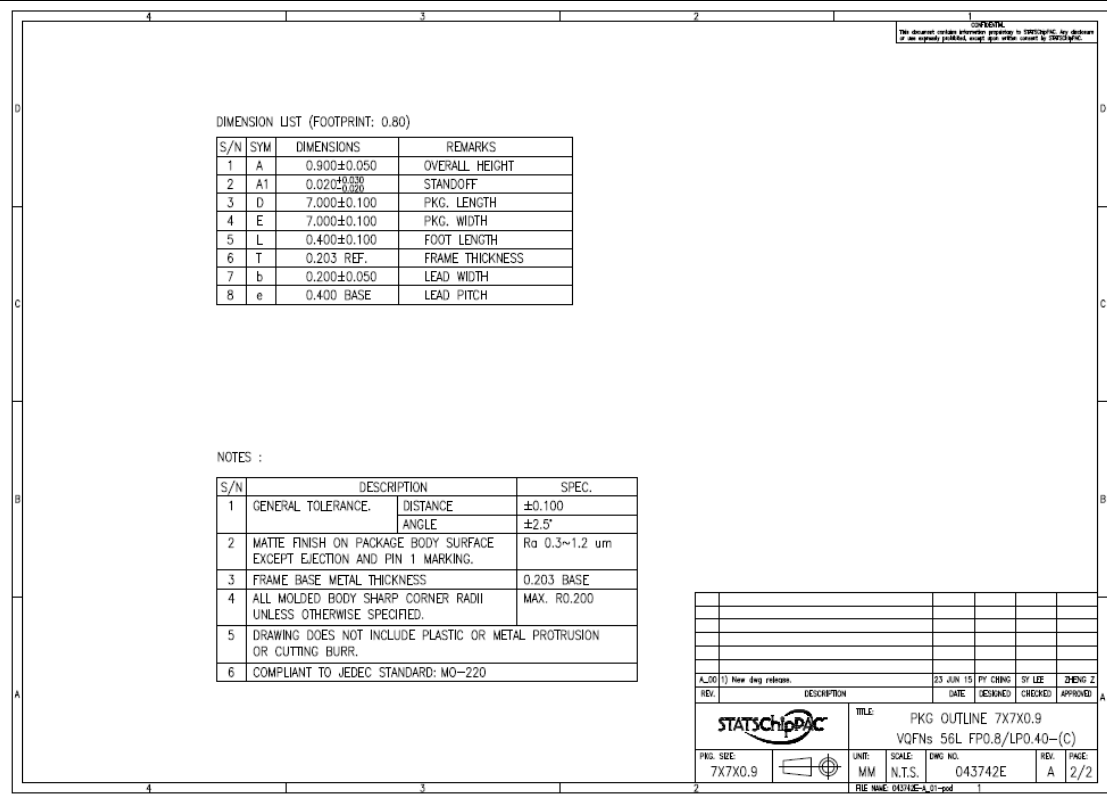图 7-1 芯片封装机械特性

图 7-2 芯片封装参数

7.2 封装热特性

芯片封装热特性为 35℃/W。

7.3 封装承压特性

芯片承压特性如下表所示。

表 7-1 封装承压特性

承压大小	单位
25	PSI(Pounds per square inch)