



# REALTEK

## ALC5651

Ultra-Low Power Two-Channel Audio CODEC

with SounzReal™ Digital Sound Effect  
for Mobile Devices

## LAYOUT GUIDE

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## **Introduction**

To ensure maximum performance from the ALC5651 codec, proper component placement and routing are very important. This document includes properly isolating the digital circuitry and analog circuitry.

The effects of ground and supply plane geometry, decoupling/bypassing/filtering capacitors placement priorities, LINK signals, analog power supplies, and analog ground planes.

## ***The layout design of Ground and Supply plane Geometry***

Figure.1 shows a top view layout of ground plane for ALC5651 codec. This layout separates the analog and digital ground planes with a 60 to 100 mils gap. The moat helps to isolate noisy digital circuitry from quiet analog audio circuitry. *The digital and analog ground planes are tied together at one point (Ferrite Bead).* This will be the "drawbridge" that goes across the moat. Similarly, NO SIGNALS WHATEVER are permitted to cross the moat (to do so creates a "slot antenna" radiator which will hammer your PCB layout with crosstalk, and create huge amounts of EMI, totally defeating your purpose). ALC5651 also supports a charge pump capless headphone output. It is better to connect a clear ground for charge pump. So, connect CPVREF to AGND is the better choice.

For a layout that helps to reduce noise, separate analog and digital ground planes should be provided, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. In addition to ground planes scheme, digital and analog power supply planes should be partitioned directly over their respective ground planes. Placing analog power coincident with analog ground, and digital power coincident with digital ground (as Figure.2 – right separation). If any portions of analog and digital plane overlap, the distributed capacitance (result from power plane reference to ground plane or signal plane reference to ground plane) between the overlapping portions will couple digital noise into the analog circuitry. This defeats the purpose of isolated plane(as Figure.2 – wrong separation). The power and ground planes should be separated by approximately 40mils for the four layer PCB design. Using power and ground planes forming a natural, high capacitive, bypass capacitor to reduce overall PCB noise.

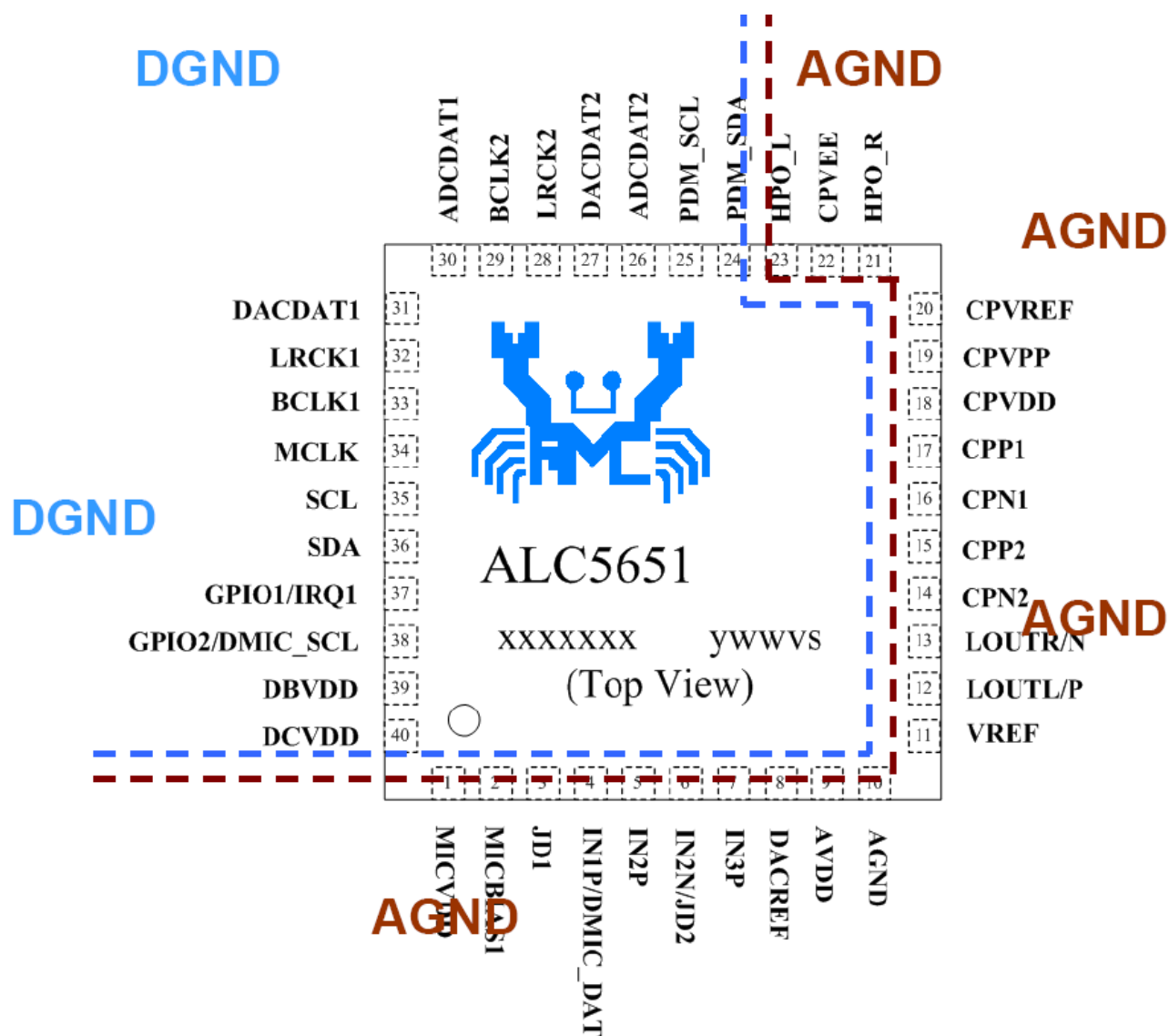
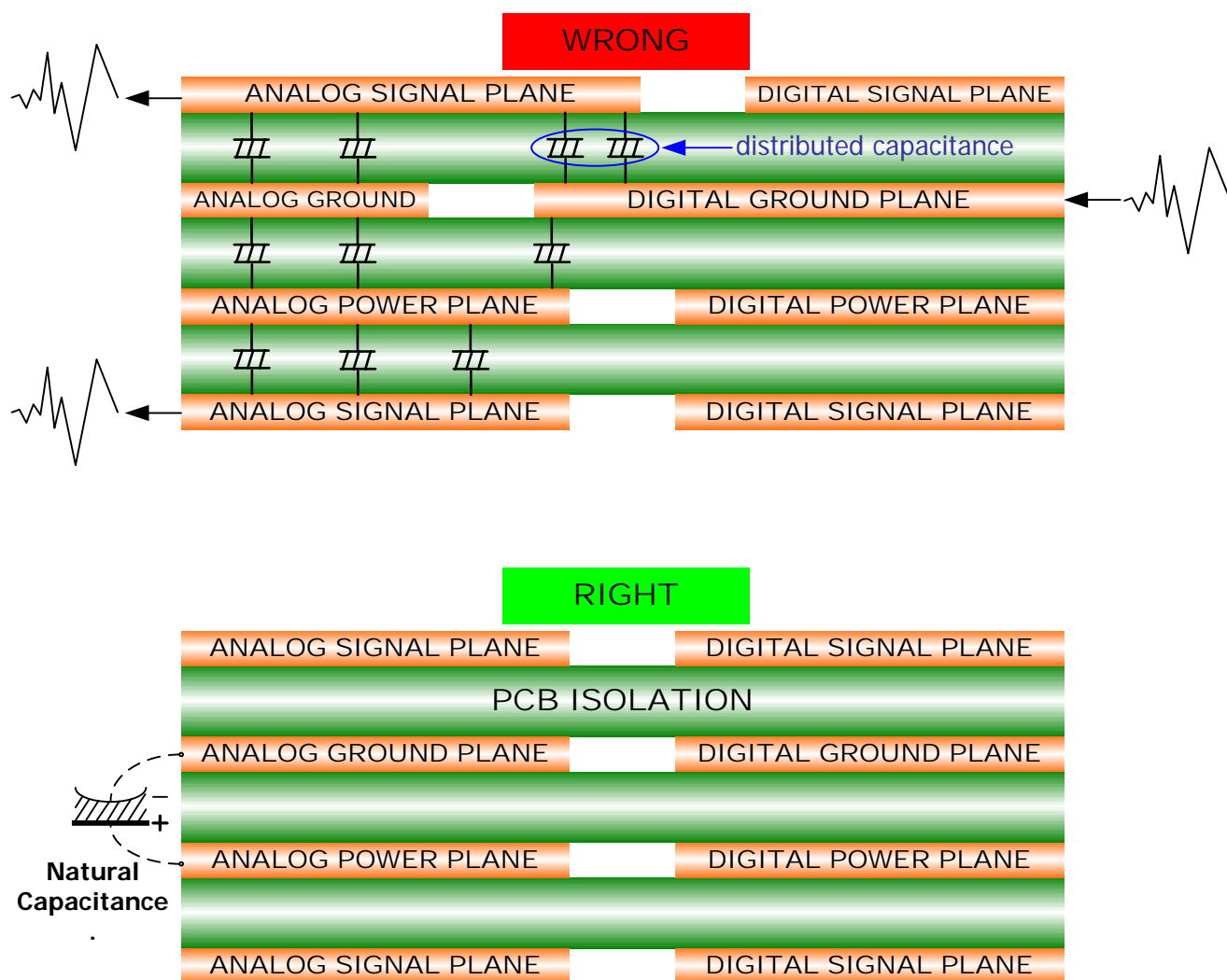


Figure1. ALC5651 ground plane Layout Guide



**Figure2. Side view of PCB, the right separation of analog and digital plane.**

## ***Decoupling and bypassing capacitors***

Bypass capacitors on the PCB are used to short digital noise into ground. Commonly, codec generates noise when its internal digital circuitry turns currents on and off. These current changes arise in the power and ground pins for the related section of the codec. The goal is to force AC currents to flow in the shortest possible loop from the supply pin through the bypass cap and back into the codec through the nearby ground pin. A bypassing circuit is supposed to be a low lead inductance between the codec and the bypass capacitors when in the operating frequency of the codec. The longer the trace – the greater the inductance. To avoid long-trace inductance effects, use the shortest possible traces for bypass capacitors, with wide traces to reduce impedance. For best performance, use supply bypass leads of less than one-half inch.

In Table1, it shows the priorities of Realtek series codec capacitor placement

1. Pins with a first – “A” priority components placed around the codec are the bypass caps, which are located as close as possible to the power supply pins. The capacitors must have low inductance and low equivalent series resistance (ESR). AVDD and DVDD are suggested to connect to 1uF and 0.1uF ceramics. CPVDD is suggested to connect to 2.2uF and 0.1uF ceramics .
2. The filter capacitors with “B” priority stabilize the reference voltage for internal Ops should be placed close to codec. A good reference voltage is relative to good analog performance.
3. These decoupling capacitors (“C” priority) should be close to the codec pins, or positioned for the shortest connections to pins, with wide traces to reduce impedance. The Table 1 also point out the distribution of codec capacitor locations and placement priorities.

Table 1.Realtek series **codec** capacitor placement priorities

Signal Description	Package Pins	Priority of Close Proximity to DAC Pin Placement of Filter and Decoupling Capacitors
Digital Supply Voltage , +1.8DBVDD	39	A
Digital Supply Voltage , +1.2DCVDD	40	A
Analog Supply Voltage, +1.8AVDD	9,8	A
Charge pump amp CPVDD , +1.8V	18	A
MICVDD,+3.3V	1	B
Voltage Reference Filter(V <sub>REF</sub> )	11	B
Analog Signal Inputs & Output(Decouple)	4~7,12~17,19,22	C

## The trace routing

### I. Power Input trace

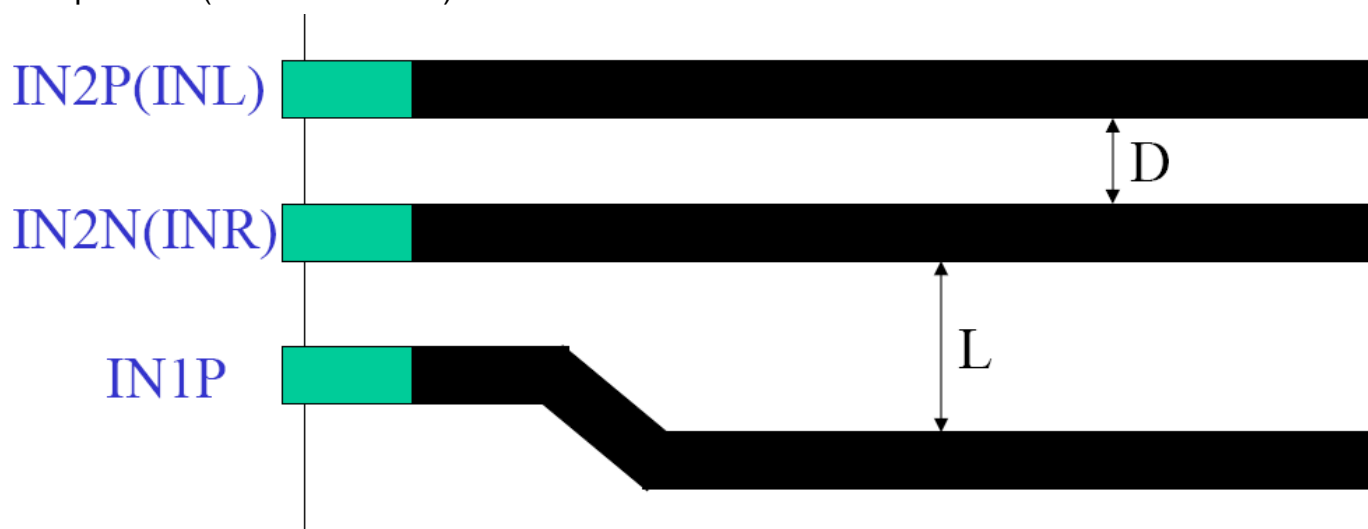
For the better loading ,the power traces width are better to correspond to the suggestion as below:

1. AVDD,DBVDD,CPVDD  $\geq 15$ mils

### II. Analog Input & Output signal trace

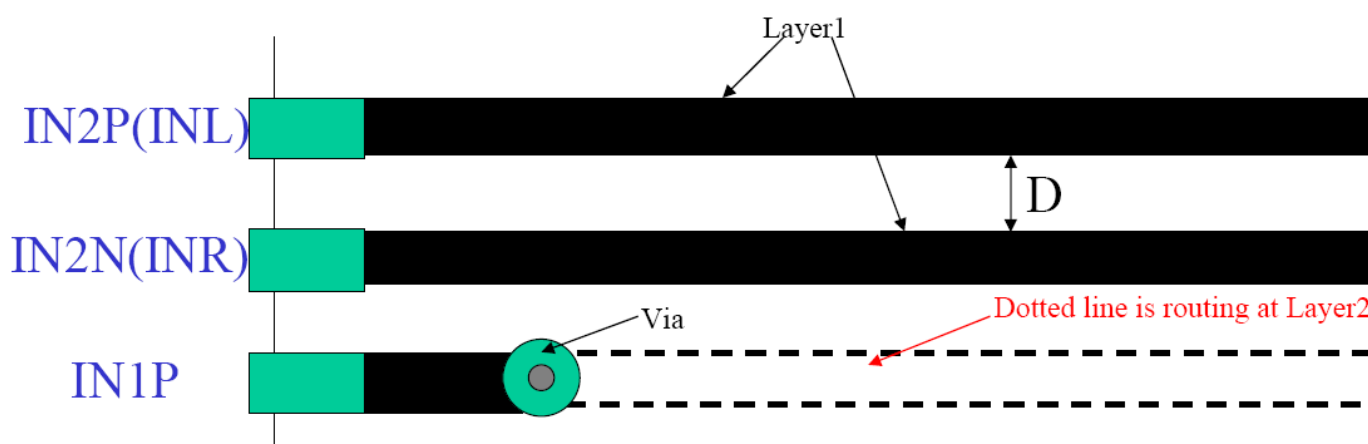
For reaching the best audio quality, some guideline should be obeyed.

1. To avoid a cross-talk issue result from having no enough space between channels or input/output traces. The cross-talk may affect the performance of analog signal, especially the mic1 and mic2. In Figure 3, the isolation between IN2P/N(INL/R) and IN1P are routing as wider as possible (L at least 60mils).



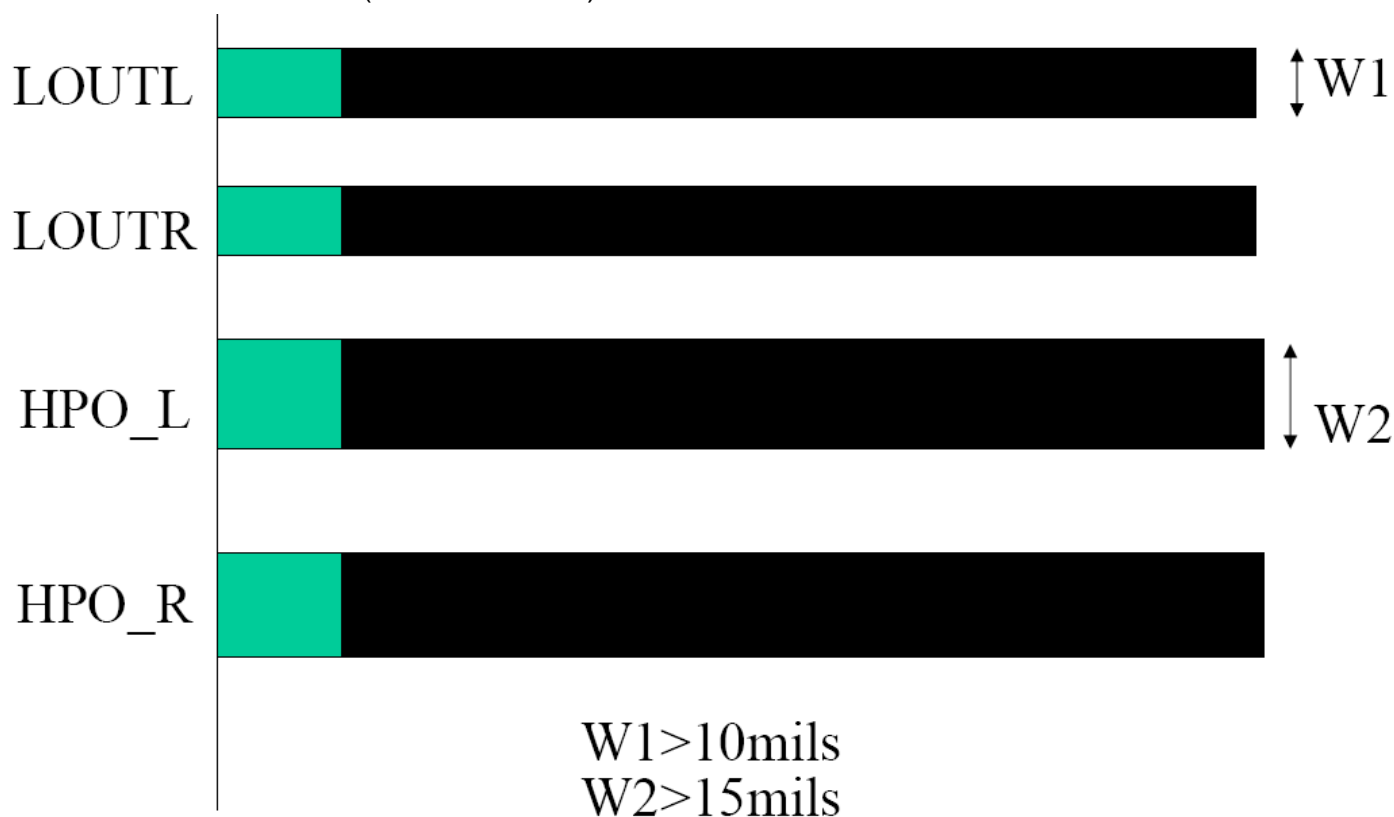
**Figure3.**The routing for analog input( $L > 60$ mils ,  $D \leq 10$ mils)

2. The IN1 and IN2 microphone input signals are more sensitive than the other signals. These two signals may route to the other layer if possible, and we can see that in Figure 4. In Figure 4, IN2(used as linein) input signal are routing on layer1. But IN1 microphone input are routing on layer2 between codec and phone jack input.

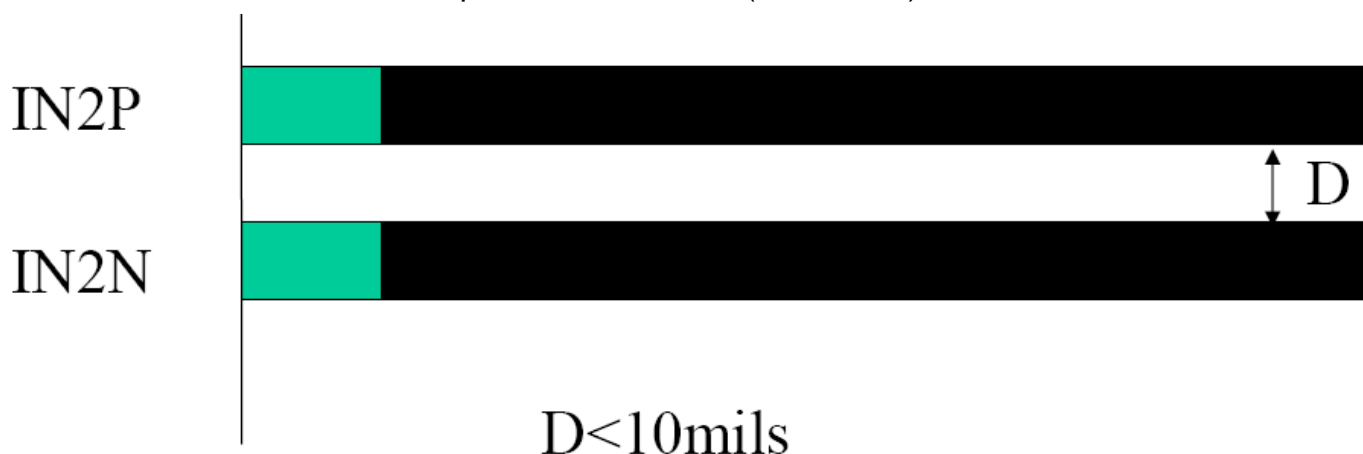


**Figure4.**The special routing for mic input signal( $D \leq 10$ mils)

- For better audio performance, analog input&output traces width should be as wide as possible.  
 IN1P, IN2P/IN2N ,IN3P >10 mils (15mils is better)  
 LOU TL/ LOU TR >10mils (15mils is better)  
 HPO\_L/HPO\_R > 15mils (20mils is better)



- The signal length from codec to input/output connector should be as short as possible.
- The trace length difference between differential signal(ex:IN2P/N ) should be kept as small as possible.(better within 1 inch)
- The width between differential pair should be small( $D \leq 10\text{mils}$ )



#### 7. The digital microphone clock (CLK) Trace

The digital microphone is not sensitive to the ground plane. The normal operation clock of digital microphone is around 1MHz to 3MHz bit rate, a long trace causes a slow rising time that makes CLK waveform is deformed, or different of trace length between CLK and DATA signal cause skew variation, both will influence digital microphone performance. The CLK and DATA signals should be routed by using **at least 5-mil width of trace and 5-mil space between each other, and keep both traces have the same length.**

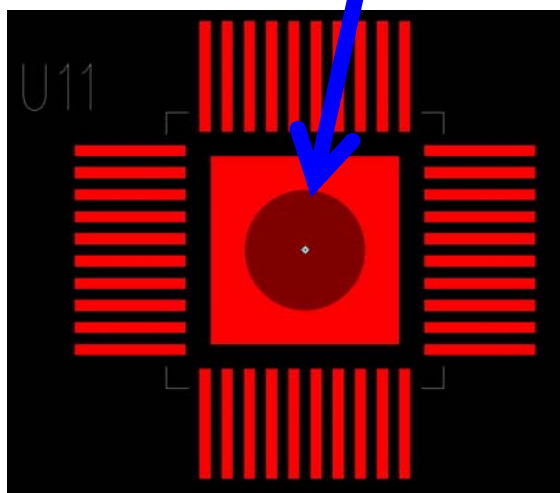
8. The space between each trace should better to be filled with copper which connect to analog ground.



- *QFN40 footprint layout*

The layout of PCB footprint for ALC5651 ( QFN40 ) can be seen in Figure 5. Note that the digital ground pad in the center is important. It makes codec to have better performance.

***Digital Ground Pad***



**Figure5.ALC5640 PCB footprint**