High-Performance Application Processor with Dual-Cluster Architecture

- 64bit Big-Little architecture with Dual-Core Cortex-A72 and Quad-Core Cortex-A53
- Powerful 3D GPU processor with OpenGL ES3.1, OpenCL2.0 and DirectX12
- Multi-format video decoder up to 4Kx2K@60fps, including H.264/H.265/VP9
- Total hardware-based security solution , including HDCP2.2
- The first worldwide SoC with embedded full Type-C interface
- High-integration SoC, more competitive Bom Cost

Overview

RK3399 is a high performance application processor for PC, mobile phone, high-end tablet and TV-Box. Especially it is one of current leading solution for chromebook, multi-OS PC and 4Kx2K TV-Box.

Integrate 64bit Big-Little architecture with Dual-Core Cortex-A72 and Quad-Core Cortex-A53. Special architecture based on CCI-Kipling will achieve memory coherency between 2 clusters to decrease the DDR access power and improve the system performance. More than 32bits address will support up to 8GB access space.

Currently, latest generation and most powerful GPU Mali-T9xx is embedded to support smoothly high-resolution (3840x2160) display and mainstream game. Support OpenGL ES1.1/2.0/3.0/3.1, OpenCL1.2/2.0, DirectX11.1/12 etc.

Full-format video decoder, including 4Kx2K H.264/H.265/VP9 decoder.

Lots of high-performance interface to get very flexible solution, such as multi-pipe display with dual-channel MIPI-DSI, eDP1.3, HDMI2.0, DP1.2, dual-channel MIPI-CSI2 interface with 13MP dual-pipe ISP embedded.

Fully-integrated hardware-based security solution will provide HDCP2.x for miracast and all kinds of DRM solution based on different OS.

Dual-Channel 64bits DDR3/DDR3L/LPDDR3/LPDDR4 provide demand memory bandwidths for high-performance and high-resolution application.

Convenient and high-speed communication with peripheral equipment by USB3 Type-C interface and PCIe2.1 interface etc. Rich low speed interface to decrease bom cost.

Features

CPU

64bit Big-Little Dual-Cluster core architecture
Dual-Core Cortex-A72 as big core cluster with maximum 2.0GHz
Quad-Core Cortex-A53 as little core cluster with maximum 1.5GHz
Separately Integrated Neon and FPU per CPU
48KB/32KB L1 ICache/DCache per Cortex-A72 CPU
32KB/32KB L1 ICache/DCache per Cortex-A53 CPU
Unified 1MB L2 Cache for Dual-Core Cortex-A72
Unified 512KB L2 Cache for Quad-Core Cortex-A53
CCI-Kipling to get memory coherency between 2 clusters
LPAE (Large Physical Address Extensions) , Support up to 8GB address space
Virtualization Extensions Support
DVFS separately for big core cluster and little core cluster

GPU

3D GPU
Quad-Core Mali-T9 series with maximum 650MHz
Leading graphics performance: 520M Tri-rate, 2.6G pixel-rate,93.6 GFLOPS
Architected for GPU computing
Adaptive Scalable Texture Compression

Support OpenGL ES1.1/2.0/3.0/3.1, OpenCL1.2/2.0, Directx11.1/12

DVFS support

2D GPU

Multi-Core architecture with maximum 500MHz

Up to 8Kx8K input and 4Kx4K output

High-quality image scale up/down

Dither operation

Image rotation with 90/180/270 degree or x/y-mirror

BitBLT, Alpha Blending, Raster Operation

VPU

Video Decoder

Support MPEG-2, MPEG-4, AVS, VC-1, VP8, MVC with up to 1080p@60fps

Support H.264 with up to 4Kx2K@30fps

Support H.265 with up to 4Kx2K@60fps

Support VP9 with up to 4Kx2K@60fps

Support 8bits/10bits H.264 decoder

Support 8bits/10bits H.265 decoder

High-quality deinterleave

Video Encoder

Support H.264,VP8,MVC with up to 1080p@30fps

Video Interface

Video Input

Dual-channel input for front and rear camera

Dual-channel MIPI-CSI2 interface with 4-lane per channel, 1.5Gbps/lane

8/10/12 bits standard DVP interface

Maximum 13Mpixel ISP, Dual-pipe

Video display

Dual-panel display with 2 separately interface

Maximum resolution is 4096x2048 and 2560x1600 for different channel

CABC support to decrease interface power

Write-back function for miracast display or dual panel

Frame Buffer Compression support

Dual channel MIPI-DSI, 4 lanes per channel, maximum 1.5Gbps per lane

HDMI2.0, support maximum 4Kx2K@60fps, HDCP2.x

DP1.2, 4-lanes, support maximum 4Kx2K@60fps, HDCP2.x

eDP1.3, 4-lanes, support maximum 2.7Gbps per lane, PSR support

Memory Interface

eMMC Interface

Compatible with eMMC5.1 standard

8bits data width

Support HS400 mode with 400MB/s data rate

DDR interface

Dual channel 64bits interface,16bits/32bits per channel

Support DDR3/DDR3L/LPDDR3/LPDDR4

Up to 2133Mbps

Hardware-based DDR frequency scaling

DVFS support

Rich Connectivity

2 SD/MMC/SDIO interface, compatible with SD3.0,SDIO3.0 and MMC4.5

One 8-channels I2S/PCM interface to support both 8-ch TX and 8-ch RX

One 2-channels I2S/PCM interface

One 8-channels SPDIF interface

Two USB2.0 Host

Two USB3.0 OTG, compatible with USB2.0 OTG

Two USB3.0/DP1.2 type-C interface

One PCIe2.1 interface, 4-lanes, 5Gbps per lane, support endpoint and root complex

One high-speed inter chip interface with 480Mbps data rate

100M/1000M RMII/RGMII Ethernet interface

5 UART, 6 SPI (master or slave), 9 I2C(up to 4Mbps), 4 PWM

Others

Standalone crypto and decrypto, compatible with AES 256bits/DES/3DES/SHA-1/ SHA-256/MD5/160bits PRNG/PKA 2048bits

Full hardware-based security solution, including secure boot/debug, DRM based on different OS and HDCP2.x

Embedded Cortex-M0 cpu to do low power management

3 watchdog, 26 timer, 2 mailbox, 5 PVTM

4 channels SAR-ADC

Temperature Sensor to support better temperature control inside chip

Package Type

TBD

SoC Diagram