MP2143

3A, 5.5V, 1.2MHz, 40µA I_Q, COT Synchronous Step Down Switcher

The Future of Analog IC Technology®

DESCRIPTION

The MP2143 is a monolithic, step-down, switch-mode converter with internal power MOSFETs. It can achieve up to 3A continuous output current from a 2.5V–to-5.5V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.6V.

Constant-on-time control provides fast transient response and eases loop stabilization. Fault-condition protections includes cycle-by-cycle current limiting and thermal shutdown.

The MP2143 is available in small TSOT23-8 package and requires only a minimal number of readily-available standard external components.

The MP2143 is ideal for a wide range of applications including high-performance DSPs, FPGAs, smartphones, portable instruments, and DVD drivers.

FEATURES

- Wide 2.5V-to-5.5V Operating Input Range
- Output Voltage as Low as 0.6V
- 100% Duty Cycle in Dropout
- Up to 3A Output Current
- Low I_Q: 40µA
- 80mΩ and 40mΩ Internal Power MOSFET Switches
- Default 1.2MHz Switching Frequency
- EN and Power-Good for Power Sequencing
- Cycle-by-Cycle Over-Current Protection
- Auto Discharge at Power Off
- Short-Circuit Protect with Hiccup Mode
- Stable with Low-ESR Output Ceramic Capacitors
- Available in a TSOT23-8 Package

APPLICATIONS

- Low Voltage (<5V) I/O System Power
- Handheld/Battery-powered Systems
- Wireless/Networking Cards

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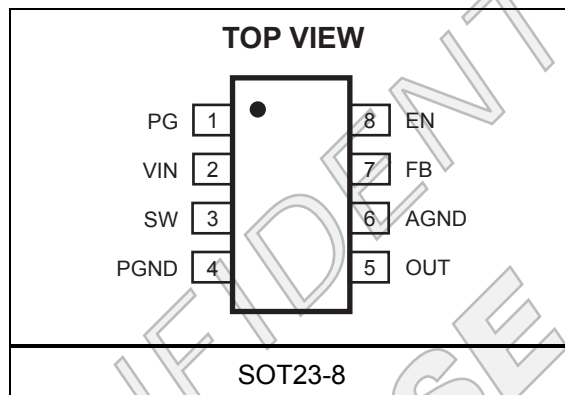
TYPICAL APPLICATION

Efficiency
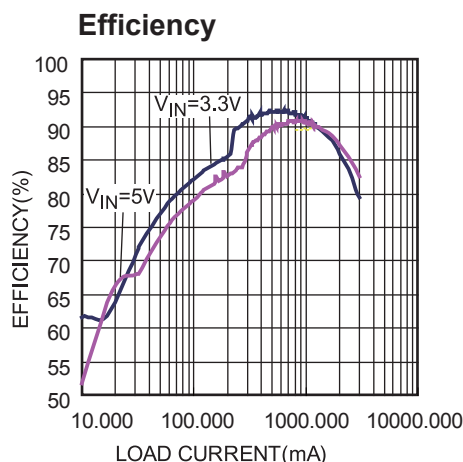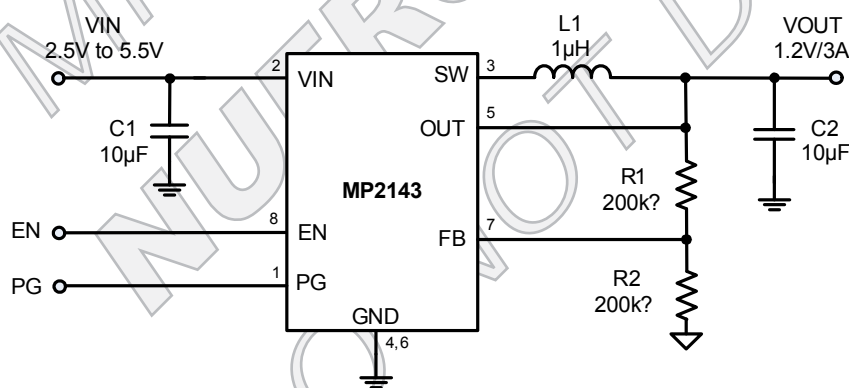
ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2143DJ	TSOT23-8	ACE

* For Tape & Reel, add suffix –Z (e.g. MP2143DJ–Z);
For RoHS compliant packaging, add suffix –LF (e.g. MP2143DJ–LF–Z)

PACKAGE REFERENCE

TOP VIEW

PG	1	8 EN
VIN	2	7 FB
SW	3	6 AGND
PGND	4	5 OUT

SOT23-8

ABSOLUTE MAXIMUM RATINGS [1]

Supply Voltage V$_{IN}$ 6V
V$_{SW}$ .... (-3V for < 5ns) to (V$_{IN}$+0.3V)
All Other Pins ....-0.3V to +6 V
Junction Temperature ....150°C
Lead Temperature ....260°C
Continuous Power Dissipation (T$_A$ = 25°C) [2]
.... 1.25W
Storage Temperature............... -65°C to +150°C

Recommended Operating Conditions [3]

Supply Voltage V$_{IN}$ ....2.5V to 5.5V
Output Voltage V$_{OUT}$................ 0.6V to V$_{IN}$ -0.5V
Operating Junction Temp. (T$_J$). -40°C to +125°C

Thermal Resistance [4]   θ$_{JA}$ θ$_{JC}$

TSOT23-8 .... 100 ..... 55... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T$_J$ (MAX), the junction-to-ambient thermal resistance θ$_{JA}$, and the ambient temperature T$_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P$_D$ (MAX) = (T$_J$ (MAX)-T$_A$)/θ$_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS [5]

V$_{IN}$ = 5V, T$_A$ = 25°C, unless otherwise noted.

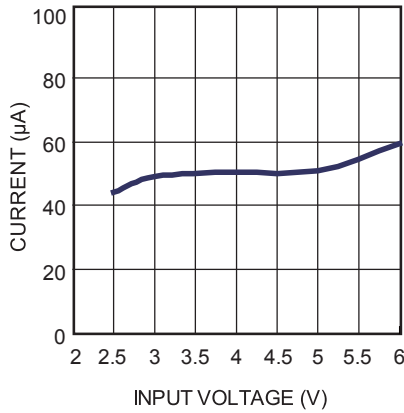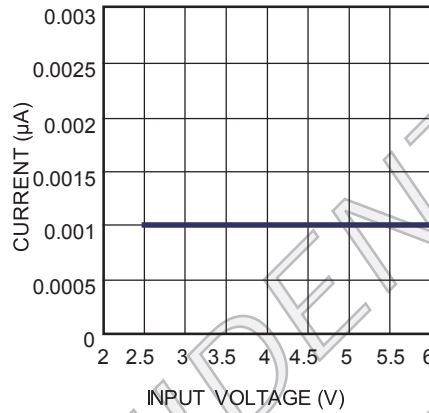| Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V$_{FB}$	2.5V ≤ V$_{IN}$ ≤ 5.5V	-1.5%	0.600	+1.5%	V/%
		T$_A$=-40°C to +85°C	-2%		+2%	
Feedback Current	I$_{FB}$	V$_{FB}$ = 0.63V		10		nA
PFET Switch ON Resistance	R$_{DSON\_P}$			80		mΩ
NFET Switch ON Resistance	R$_{DSON\_N}$			40		mΩ
Switch Leakage		V$_{EN}$ = 0V, V$_{IN}$ = 5V V$_{SW}$ = 0V and 5V		0.1	2	µA
PFET Current Limit			4.2	4.8		A
NFET Switch Sinking Current	I$_{NSW}$	V$_{OUT}$=1.2V, V$_{FB}$=0.7V		100		µA
ON Time	t$_{ON}$	V$_{IN}$=5V, V$_{OUT}$=1.2V		200		nS
		V$_{IN}$=3.6V, V$_{OUT}$=1.2V		277		
Switching frequency	f$_s$	V$_{IN}$=5V, V$_{OUT}$=1.2V, I$_{OUT}$=1A	-20%	1200	+20%	kHz
		T$_A$=-40°C to +85°C	-25%	1200	+25%	kHz
Minimum OFF Time	t$_{MIN-OFF}$			50		ns
Soft-Start Time	t$_{SS-ON}$			1.3		ms
Soft-Stop Time	t$_{SS-OFF}$			1		ms
Power-Good Upper Trip Threshold	PG$_H$	FB voltage respect to the regulation		+10%		%
Power-Good Lower Trip Threshold	PG$_L$			-10%		%
Power-Good Delay	PG$_D$			110		µs
Power-Good Sink Current Capability	V$_{PG-L}$	Sink 1mA			0.4	V
Power-Good Logic High Voltage	V$_{PG-H}$	V$_{IN}$=5V, V$_{FB}$=0.6V	4.9			V
Power-Good Internal Pull-Up Resistor	R$_{PG}$			500		kΩ
Under-Voltage Lockout Threshold Rising			2.2	2.3	2.4	V
Under-Voltage Lockout Threshold Hysteresis				300		mV
EN Input Logic Low Voltage					0.4	V
EN Input Logic High Voltage			1.2			V
EN Input Current		V$_{EN}$=2V		2		µA
		V$_{EN}$=0V		0.1		µA
Supply Current (Shutdown)		V$_{EN}$=0V		0.1		µA
Supply Current (Quiescent)		V$_{EN}$=2V, V$_{FB}$=0.63V, V$_{IN}$=3.6V		40		µA
Thermal Shutdown				150		°C
Thermal Hysteresis				30		°C

Notes:
5) Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

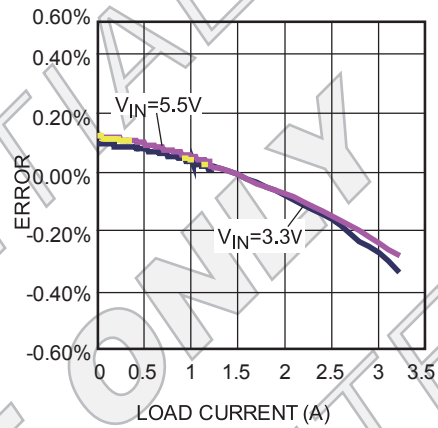V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, C_{OUT}=22µF, T_A = 25°C, unless otherwise noted.

MP2143 Rev. 1.01
2/29/2012
Preliminary Specifications Subject to Change
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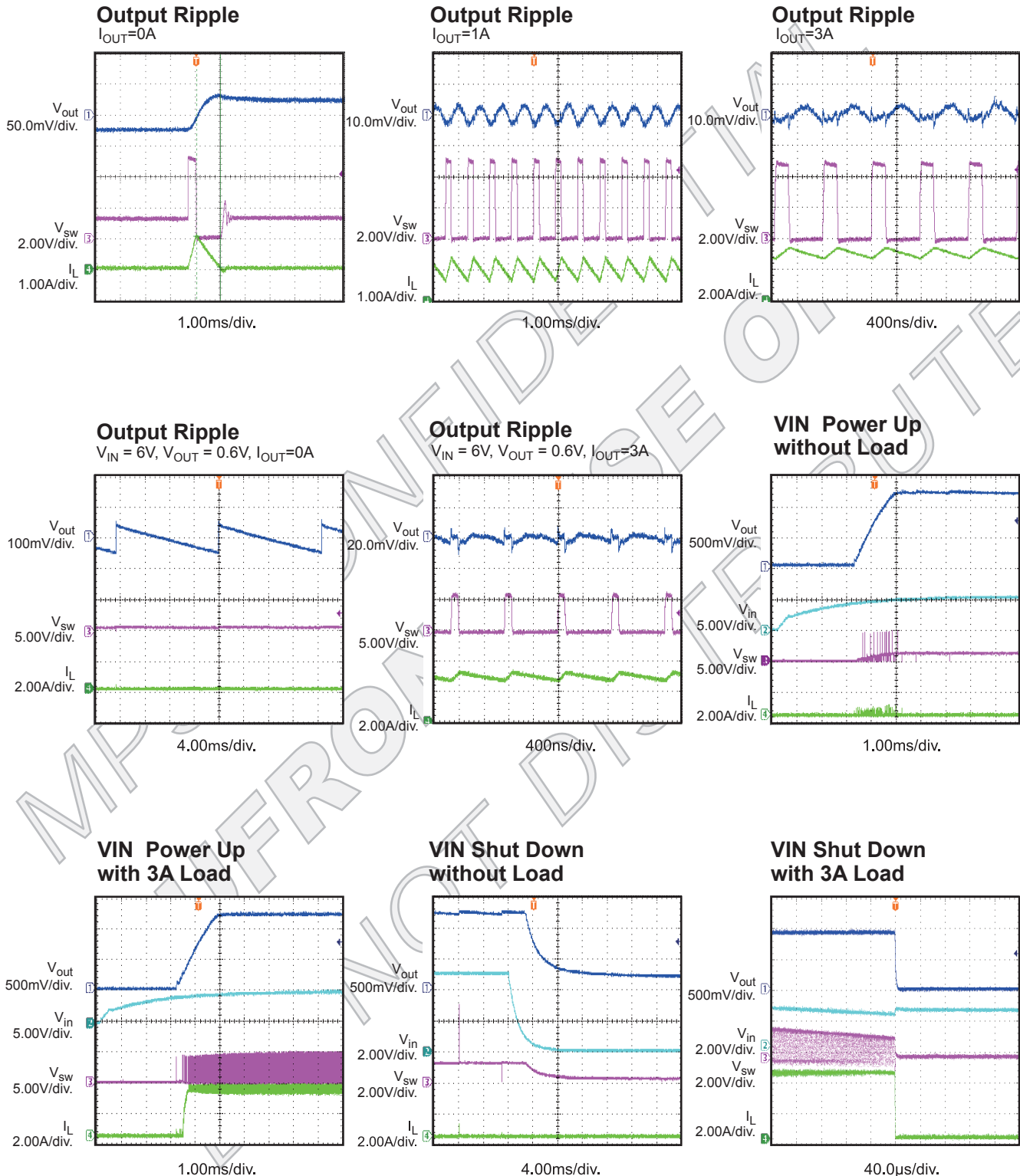© 2012 MPS. All Rights Reserved.
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, C_{OUT}=22µF, T_A = 25°C, unless otherwise noted

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.TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V$_{IN}$ = 5V, V$_{OUT}$ = 1.2V, L = 1.0µH, C$_{OUT}$=22µF, T$_A$ = 25°C, unless otherwise noted.

EN Start Up without Load

EN Start Up with 3A Load

EN Shut Down without Load

EN Shut Down with 3A Load

Power Good On without Load

Power Good On with 3A Load

Power Good Off without Load

Power Good Off with 3A Load

Load Transient Response

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, C_{OUT}=22µF, T_A = 25°C, unless otherwise noted.

Short Circuit Entry
V_{IN}= 6V

Short Circuit
V_{IN}= 6V

Short Circuit Recovery
V_{IN}= 6V
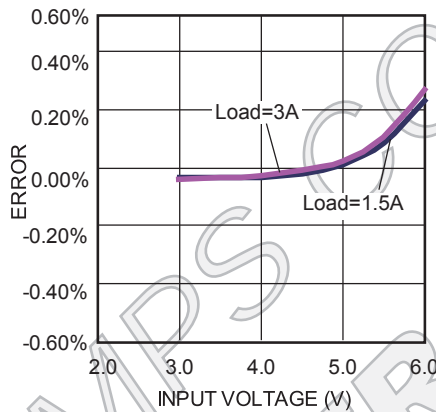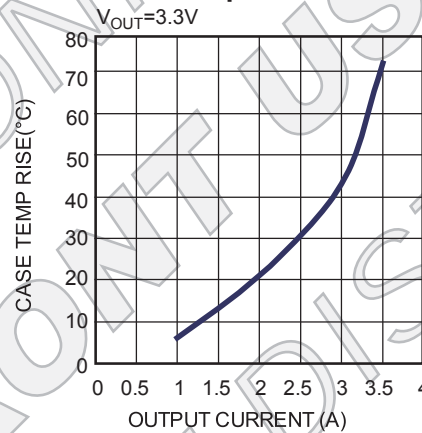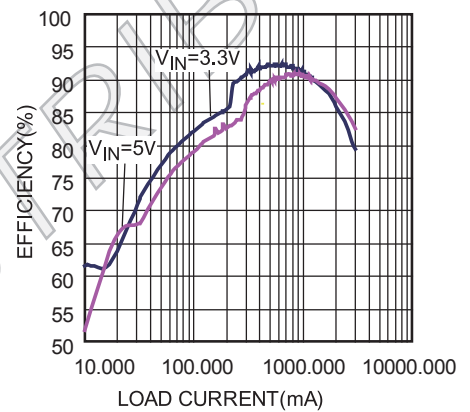
PIN FUNCTIONS

| TSOT23 Pin #	Name	Description
1	PG	Power-Good Indicator. The pin output is an open drain that connects to VIN by an internal pull-up resistor. PG is pulled up to VIN when the FB voltage is within 10% of the regulation level. If FB voltage is out of that regulation range, it is LOW.
2	VIN	Supply Voltage. The MP2143 operates from a 2.5V-to-5.5V unregulated input. C1 prevents large voltage spikes from appearing at the input.
3	SW	Switch Output
4	PGND	Power Ground
5	OUT	Input Sense. For output voltage feedback
6	AGND	Analog ground. Reference for the internal control circuit.
7	FB	Feedback pin. Connect an external resistor divider from the output to GND to set the output voltage.
8	EN	On/Off Control

FUNCTIONAL BLOCK DIAGRAM
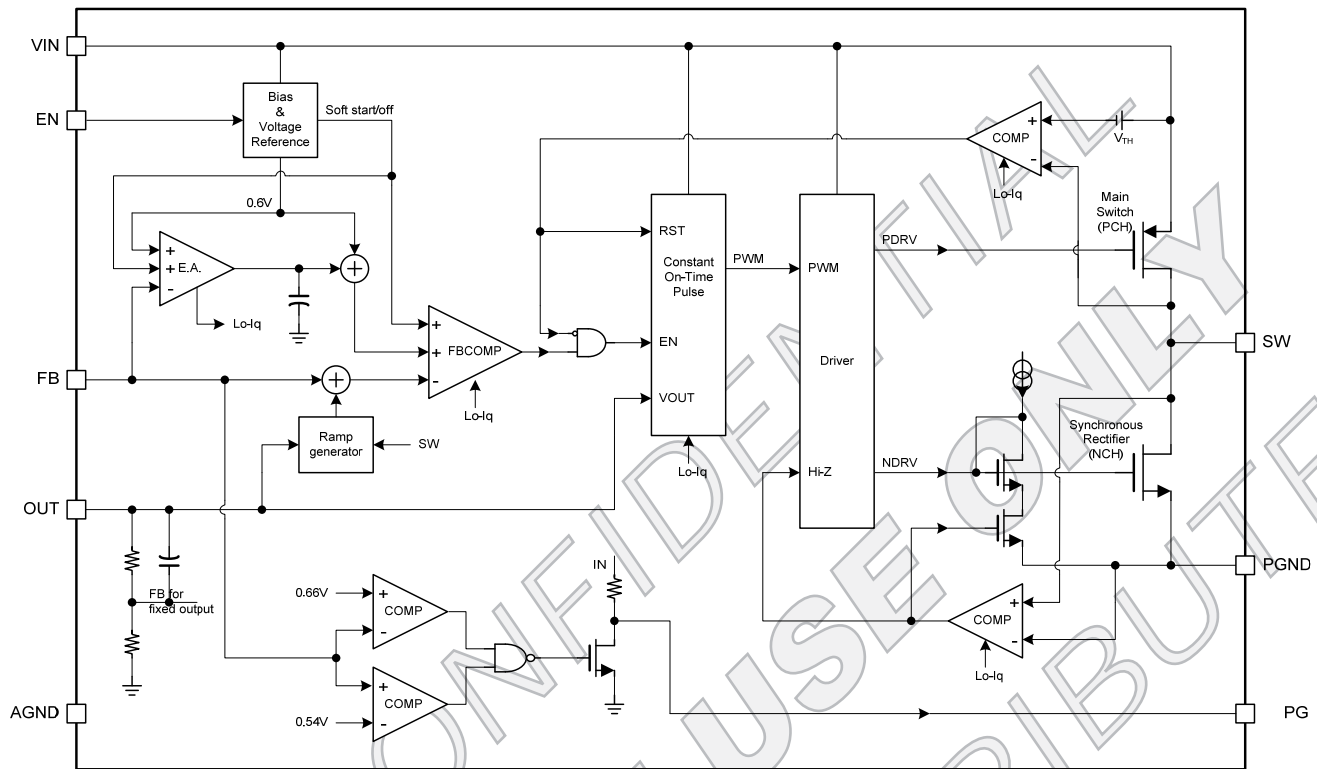
Figure 1: Functional Block Diagram

OPERATION

The MP2143 uses constant on-time control with input-voltage feed-forward to stabilize the switching frequency over its full input range. At light load, the MP2143 employs a proprietary control over the low-side MOSFET (LS-FET) and inductor current to eliminate ringing on switching node and to improve efficiency.

Constant On-Time Control

When compared to fixed-frequency PWM control, constant on-time control offers a simpler control loop and faster transient response. By using input-voltage feed-forward, the MP2143 maintains a nearly constant switching frequency across the entire input and output voltage range. The switching pulse ON time can be estimated as:

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 0.833\mu s$$

To prevent inductor current runaway during the load transient, the MP2143 has a fixed minimum OFF time of 50ns. However, this minimum OFF time limit does not affect the operation of the MP2143 in steady state in any way.

Light Load Operation

In light load condition, the MP2143 uses a proprietary control scheme to save power and improve efficiency: It gradually ramps down the LS-FET current to its minimum instead of turning off the LS-FET immediately when the inductor current starts to reverse. The gradual current drop avoids ringing at the switching node that always occurs in discontinuous conduction mode (DCM) operation.

Enable

When the input voltage exceeds the under-voltage lockout (UVLO) threshold—typically 2.3V—the MP2143 is enabled by pulling the EN pin above 1.2V. Leaving the EN pin floating or

grounded will disable the MP2143. There is an internal 1MΩ resistor from the EN pin to ground.

Soft-Start/Stop

MP2143 has a built-in soft-start that ramps up the output voltage at a constant slew rate that avoids overshooting at startup. The soft-start time is typically about 1ms. When disabled, the MP2143 ramps down the internal reference voltage to allow the load to linearly discharge the output.

Power GOOD Indictor

MP2143 has an open drain with 500kΩ pull-up resistor pin for power good (PG) indication. When the FB pin is within ±10% of regulation voltage (0.6V), the PG pin is pulled up to VIN by the internal resistor. If the FB pin voltage is outside the ±10% window, the PG pin is pulled to ground by an internal MOSFET. The MOSFET has a maximum R$_{dson}$ of less than 100Ω.

Current limit

The MP2143 has a 4.8A current limit for the high side switch (HS-FET). When the HS-FET hits its current limit, the MP2143 enters hiccup mode until the current drops to prevent the inductor current from building and possibly damaging the components.

Short Circuit and Recovery

The MP2143 also enters short-circuit protection (SCP) mode when it hits the current limit, and tries to recover from the short circuit by entering hiccup mode. In SCP, the MP2143 disables the output power stage, discharges a soft-start capacitor, and then enacts a soft-start procedure. If the short-circuit condition still holds after soft-start ends, the MP2143 repeats this operation until the short circuit ceases and output rises back to regulation level.

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

The external resistor divider sets the output voltage (see the Typical Application schematic on page 1). The feedback resistor R1 must account for both stability and dynamic response, and thus can not be too large or too small. Choose an R1 value between 120kΩ and 200kΩ. R2 is then given by:

$$R2 = \frac{R1}{\dfrac{V_{out}}{0.6} - 1}$$

The feedback circuit is shown as Figure 2.
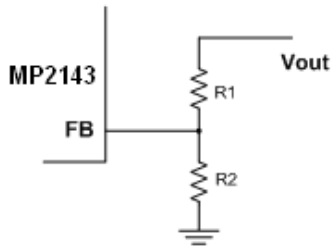
Figure 2: Feedback Network

Table 1 lists the recommended resistors values for common output voltages.

Table 1: Resistor Values for Common Output Voltages

V$_{OUT}$ (V)	R1 (kΩ)	R2 (kΩ)
1.0	200(1%)	300(1%)
1.2	200(1%)	200(1%)
1.8	200(1%)	100(1%)
2.5	200(1%)	63.2(1%)
3.3	200(1%)	44.2(1%)

Selecting the Inductor

A 0.82μH to 4.7μH inductor is recommended for most applications. For highest efficiency, chose an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose an inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR values and small temperature coefficients. For most applications, a 10μF capacitor is sufficient. For higher output voltage, use 47μF to improve system stability.

Since the input capacitor absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at VIN = 2V$_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, use a small high-quality ceramic capacitor (0.1μF), placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the output DC voltage. Use ceramic capacitors. Low-ESR capacitors keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L$_1$ is the inductor value and R$_{ESR}$ is the equivalent series resistance of the output capacitor.

Using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system.

PCB Recommendation of MP2143

Proper layout of the switching power supplies is very important, and sometimes critical for proper operation. For high-frequency switching converters, poor layout could lead to poor line or load regulation and stability issues.

The high current paths (GND, IN, and SW) should be placed very close to the device using short, direct, and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.
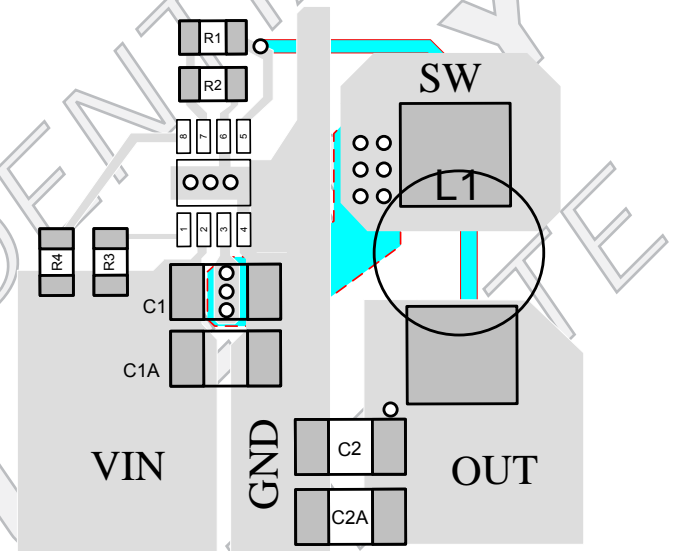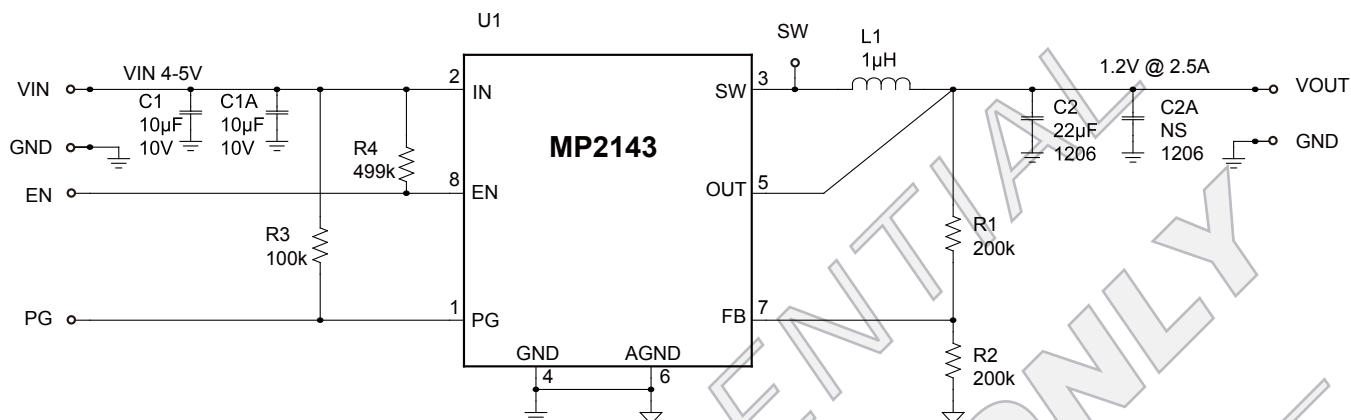
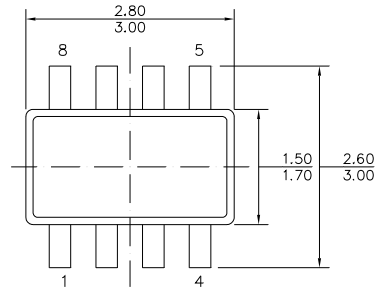

Figure 3: Layout Recommendation 1
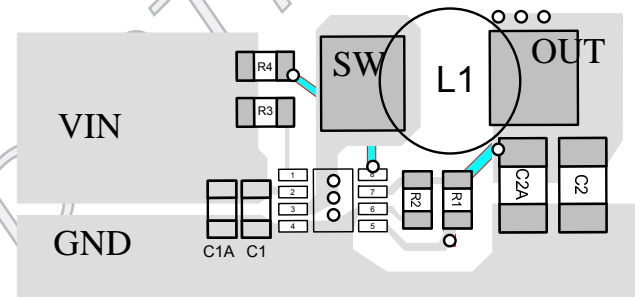
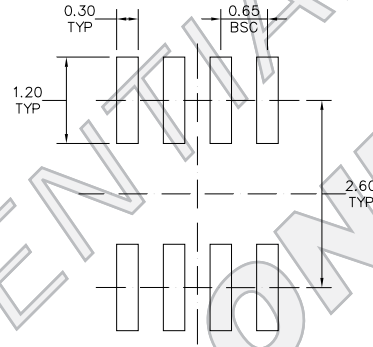**Figure 4: Layout Recommendation 2**

TYPICAL APPLICATION CIRCUITS

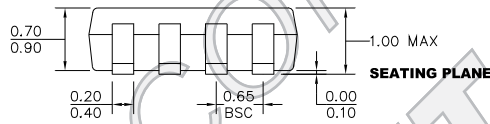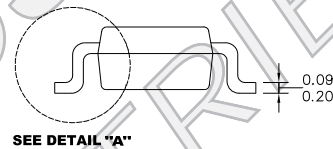**Figure 5: MP2143 Typical Application Circuit**

PACKAGE INFORMATION

TOP VIEW

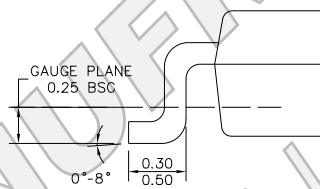**RECOMMENDED LAND PATTERN**

FRONT VIEW

SIDE VIEW

DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.