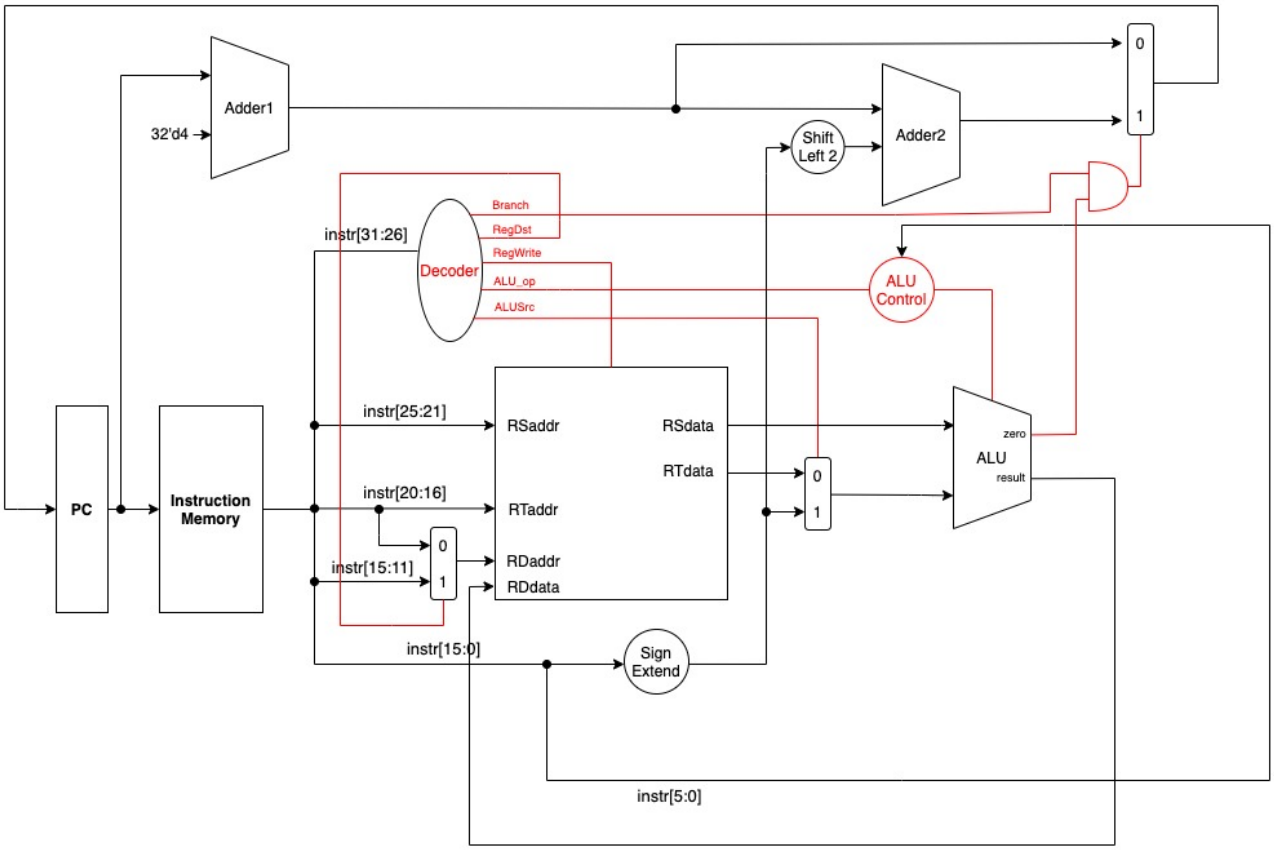
0716050 吳泓毅

Report

Computer Organization Lab 2

Architecture Diagram



Module Description

- ProgramCounter:
  To determine the output of PC by reset while reaching the edges of the clock

- Simple_Single_CPU:
  To determine the I/Os of each modules and construct a model

- Adder:
  To add up two inputs; here is to generate a new PC

- Instr_Memory:
  To obtain an instruction from the instruction memory

- Decoder:
  To determine the controls by instruction op code

- Reg_File:
  To deal with the input datum: output the data from the register or write something into RD

- ALU_Ctrl:
  To determine ALU controls by ALU_ops and functs if the ALU_op represents R-type

- ALU:
  To determine the operations under ALU with ALU controls

- MUX_2to1:
  To determine the output by certain input controls

- Sign_Extend:
  To extend a 16 bit number with the leading digit to a 32 bit number

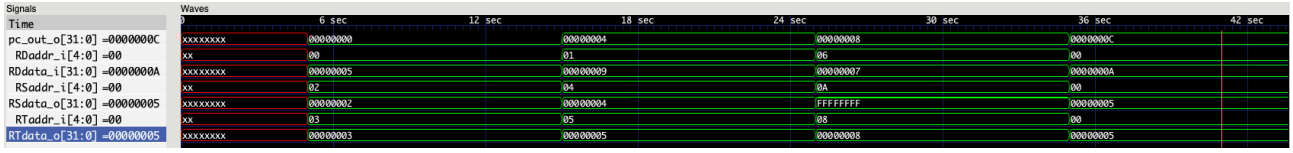
- Shift_Left_Two_32:
  To make the number 4 times, to turn the number in terms of instructions into the one in terms of bytes

- TestBench:
  To test the program with some case datum

Waveform

R-type

- addu



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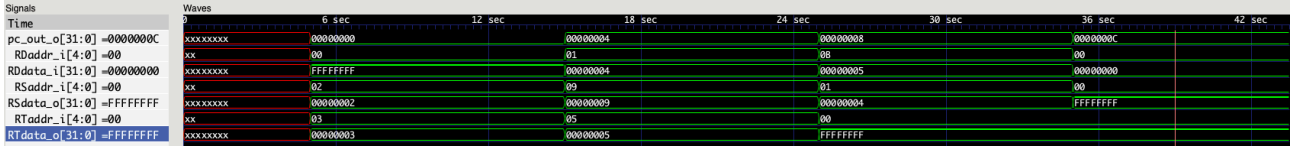

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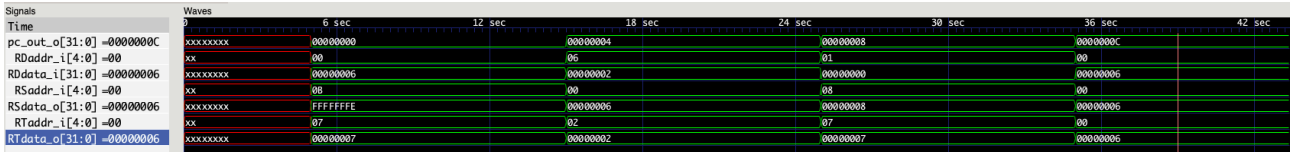

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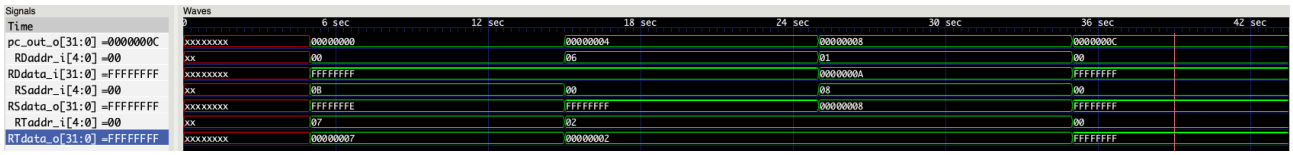

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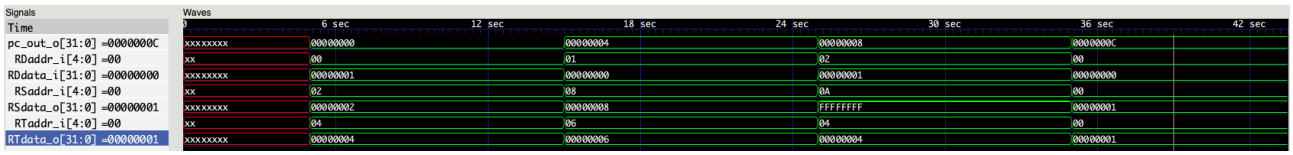

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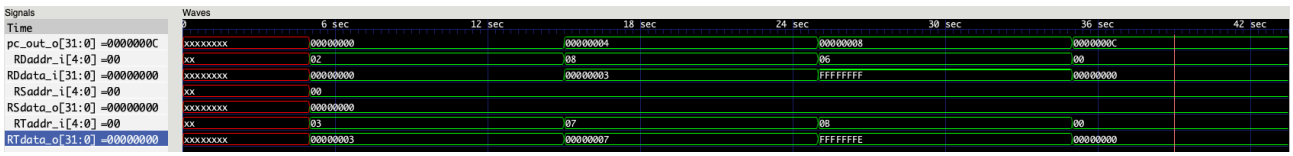

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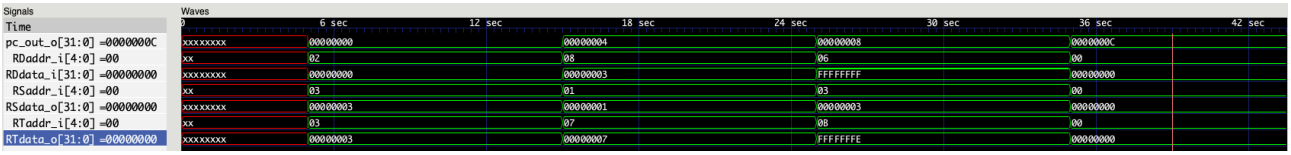
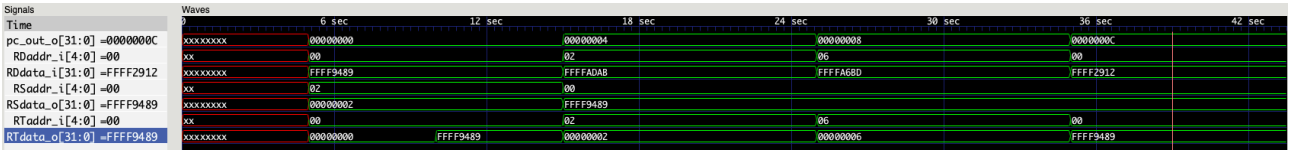


I-type

- addi



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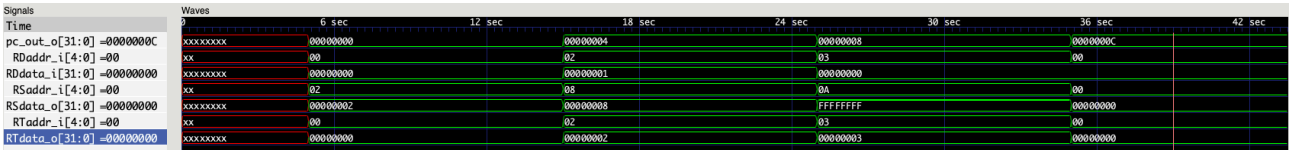

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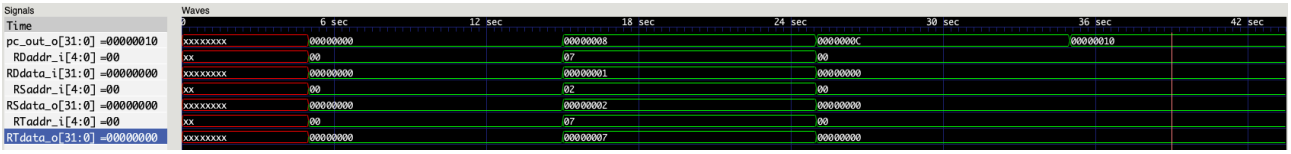

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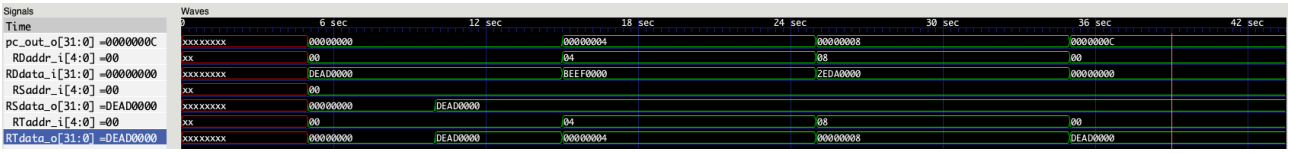

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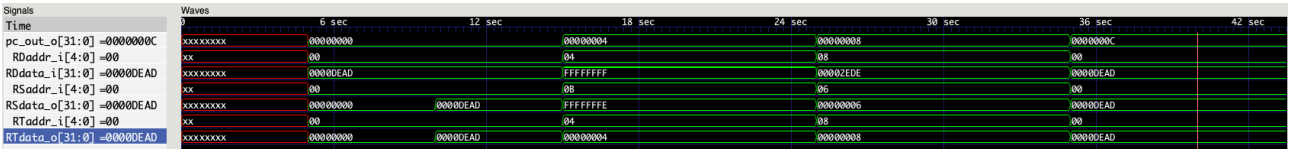

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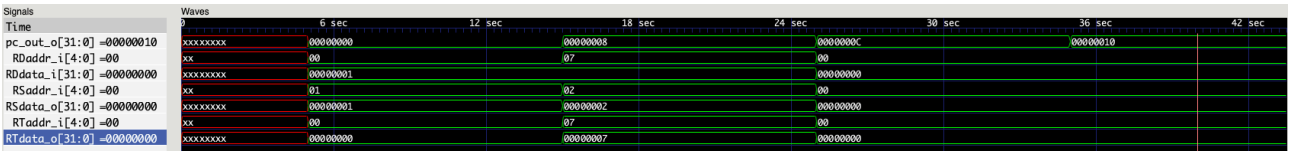

Questions

- What is the difference between "input [15:0] input_0" and "input [0:15] input_0" inside the module?

  Way it uses the LSB and the MSB

- What is the meaning of "always" block in Verilog?
  Used to describe events that should happen under certain conditions

- What are the advantages and disadvantages of port connection by order and port connection by name in Verilog?
  - Connection by order
    - Advantages:
      - More simplified
    - Disadvantages:
      - Easily cause an error due to unawareness of wrong order
  - Connection by name
    - Advantages:
      - Reduce the risk of an inadvertent error because a net was connected to the wrong port
      - Better document the intent of the design
    - Disadvantages:
      - Too verbose

Contribution

- ALU module, ALU_Ctrl module, Simple_Single_CPU module, Adder module
- test case generation
- draw the architecture diagram

However, we debug together, which includes bugs in ALU, ALU_Ctrl.

Discussions

這次的作業雖然繁瑣，sra和一些sign的問題也困擾了我們很久，再來是debug底到快崩潰，但是這次Lab也讓我更徹底了解整個CPU的運作流程，等於是再複習了一次期中考的內容，希望之後的Lab也能繼續像這次一樣令我收穫滿滿。另外隊友很讚，非常棒。