

# WUXI LI

Staff Software Engineer ◊ Vivado Implementation Team ◊ Xilinx  
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## RESEARCH INTERESTS

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Design automation and optimization for VLSI

## EXPERIENCE

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<b>AMD (Xilinx), San Jose, CA</b> Member of Technical Staff (MTS) Software Engineer, Vivado Placement Team	<i>Feb. 2022 – Present</i>
<b>Xilinx, San Jose, CA</b> Staff Software Engineer, Vivado Placement Team	<i>Aug. 2019 – Feb. 2022</i>
<b>Xilinx, San Jose, CA</b> Software Development Intern, Vivado Implementation Team	<i>May 2018 – Aug. 2018</i>
<b>Cadence Design System, Austin, TX</b> Software Development Intern, Clocking Team	<i>May 2016 – Dec. 2016</i>
<b>Apple, Austin, TX</b> Hardware Design Intern, SoC Clocking Team	<i>Jan. 2015 – Dec. 2015</i>
<b>Apple, Cupertino, CA</b> Hardware Design Intern, SoC Methodology Team	<i>Sep. 2014 – Dec. 2014</i>
<b>ARM, Austin, TX</b> Hardware Design Intern, Memory Team	<i>May 2014 – Aug. 2014</i>

## EDUCATION

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<b>University of Texas at Austin, TX</b> Ph.D., Department of Electrical and Computer Engineering Dissertation: Placement Algorithms for Large-Scale Heterogeneous FPGAs Advisor: David Z. Pan (GPA 4.0/4.0)	<i>Jan. 2016 – Aug. 2019</i>
<b>University of Texas at Austin, TX</b> M.S., Department of Electrical and Computer Engineering (GPA 4.0/4.0)	<i>Aug. 2013 – Dec. 2015</i>
<b>Shanghai Jiao Tong University, Shanghai, China</b> B.S. with Highest Honors, Department of Microelectronics (GPA 90.1/100)	<i>Sep. 2009 – Jul. 2013</i>

## PUBLICATIONS

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### Journal Articles

- [J8] Yibai Meng, **Wuxi Li**, Yibo Lin, David Z. Pan, “[elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2021.
- [J7] Yibo Lin, Zixuan Jiang, Jiaqi Gu, **Wuxi Li**, Shounak Dhar, Haoxing Ren, Bruce Khailany, David Z. Pan, “[DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2020. (**Best Paper Award**)
- [J6] Yibo Lin, **Wuxi Li**, Jiaqi Gu, Haoxing Ren, Bruce Khailany, David Z. Pan, “[ABCDPlace: Accelerated Batch-based Concurrent Detailed Placement on Multi-threaded CPUs and GPUs](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2020.

- [J5] **Wuxi Li**, David Z. Pan, “[A New Paradigm for FPGA Placement without Explicit Packing](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2018.
- [J4] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, David Z. Pan, “[A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2018.
- [J3] **Wuxi Li**, Yibo Lin, Meng Li, Shounak Dhar, David Z. Pan, “[UTPlaceF 2.0: A High-Performance Clock-Aware FPGA Placement Engine](#)”, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2018. (**1st-Place Award of ISPD 2017 Contest**)
- [J2] **Wuxi Li**, Shounak Dhar, David Z. Pan, “[UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing](#)”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2017.
- [J1] **Wuxi Li**, Hang Yuan, Wei Xu, Kunling Geng, Guoxing Wang, “[An Optimization Procedure for Coil Design in a Dual Band Wireless Power and Data Transmission System](#)”, ECS Transactions (ECST), 2013.

### Conference Papers

- [C12] Donghao Fang, Boyang Zhang, Hailiang Hu, **Wuxi Li**, Bo Yuan, Jiang Hu, “[Global Placement Exploiting Soft 2D Regularity](#)”, ACM International Symposium on Physical Design, 2022.
- [C11] Jiaqi Gu, Zheng Zhao, Chenghao Feng, **Wuxi Li**, Ray T. Chen, David Z. Pan, “[FLOPS: Efficient On-Chip Learning for Optical Neural Networks Through Stochastic Zeroth-Order Optimization](#)”, ACM/IEEE Design Automation Conference (DAC), 2020.
- [C10] Mohamed B. Alawieh, **Wuxi Li**, Yibo Lin, Love Singhal, Mahesh Iyer, David Z. Pan, “[High-Definition Routing Congestion Prediction for Large-Scale FPGAs](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2020.
- [C9] Mingjie Liu, **Wuxi Li**, Keren Zhu, Biying Xu, Yibo Lin, Linxiao Shen, Xiyuan Tang, Nan Sun, David Z. Pan, “[S3DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2020.
- [C8] **Wuxi Li**, Yibo Lin, David Z. Pan, “[elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2019. (**Best-in-Track Paper**)
- [C7] Yibo Lin, Shounak Dhar, **Wuxi Li**, Haoxing Ren, Brucek Khailany, David Z. Pan, “[DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement](#)”, ACM/IEEE Design Automation Conference (DAC), 2019. (**Best Paper Award**)
- [C6] **Wuxi Li**, Stephen Yang, Mehrdad E. Dehkordi, David Z. Pan, “[Simultaneous Placement and Clock Tree Construction for Modern FPGAs](#)”, ACM International Symposium on Field-Programmable Gate Arrays (FPGA), 2019.
- [C5] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, David Z. Pan, “[A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion](#)”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2018.
- [C4] **Wuxi Li**, Meng Li, Jiajun Wang, David Z. Pan, “[UTPlaceF 3.0: A Parallelization Framework for Modern FPGA Global Placement](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2017. (**Invited Paper**)
- [C3] Wei Ye, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, Yiwei Fu, Yongsheng Sun, Canhui Zhan, David Z. Pan, “[Placement Mitigation Techniques for Power Grid Electromigration](#)”, IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2017.
- [C2] **Wuxi Li**, Shounak Dhar, David Z. Pan, “[UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing](#)”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2016. (**Invited Paper, 1st-Place Award of ISPD 2016 Contest**)
- [C1] Wei Xu, Xiyun Li, **Wuxi Li**, Hang Yuan, Guoxing Wang, “[Live demonstration: An Optimization Software and a Design Case of a Novel Dual Band Wireless Power and Data Transmission System](#)”, IEEE International Symposium on Circuits and Systems (ISCAS), 2014.

## PATENT

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- [P1] **Wuxi Li**, Mehrdad Eslami Dehkordi, Xiaojian Yang, “[Clock tree routing in programmable logic device](#)”, US Patent 10,860,765.

## PROFESSIONAL SERVICE

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### TPC Member

- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2023.
- ACM/IEEE Design Automation Conference (DAC), 2022.
- ACM International Symposium on Physical Design (ISPD), 2022.
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2022.

### Session (Co-)Chair

- Session “Learn about advanced placement algorithms for hyperscaler chips!”, DAC, 2022.
- Session “Advances in VLSI Routing”, ASPDAC, 2022.
- Session “Optimization Attacks Routing Challenges”, ICCAD, 2019.

### Journal Reviewer

- IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transaction on Very Large Scale Integration Systems (TVLSI)
- Integration, the VLSI Journal (Integration)
- Journal of Parallel and Distributed Computing (JPDC)

### Conference Reviewer

- ACM/IEEE Design Automation Conference (DAC)
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
- IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC)
- ACM International Symposium on Physical Design (ISPD)
- ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)

## AWARDS AND HONORS

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Best Paper Award	TCAD	2021
Best Paper Award	DAC	2019
Silver Medal at ACM/SIGDA Student Research Competition	ACM/SIGDA	2018
George J. Heuer, Jr. Ph.D. Endowed Graduate Fellowship Fund	UT Austin	2018
3rd-Place Winner of Intern Showcase Presentation	Xilinx	2018
1st-Place Winner of Clock-Aware FPGA Placement Contest	ISPD	2017
1st-Place Winner of Routability-Driven FPGA Placement Contest	ISPD	2016
Graduation with Highest Honors, College Graduate Excellence Award of Shanghai	SJTU	2013
Excellent Bachelor Dissertation Award (Top 39/3900+)	SJTU	2013
Toshiba Electronics Scholarship	SJTU	2012

## SKILLS

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### Programming Languages

C/C++, L<sup>A</sup>T<sub>E</sub>X, Perl, Python, Verilog

### Operating Systems

Linux/UNIX

### EDA Tools

Cadence Virtuoso, Synopsys Design Compiler, Synopsys IC Compiler, Synopsys PrimeTime