

YIBO LIN

PhD student ◇ Department of Electrical & Computer Engineering
University of Texas at Austin, Austin, TX 78712 ◇ University of Texas at Austin
1600 Wickersham Lane apt 3089, Austin, TX 78741, USA ◇ Phone: +1 512-605-7126
yibolin@utexas.edu ◇ www.cerc.utexas.edu/~yibolin

RESEARCH INTERESTS

Design automation and optimization for VLSI

EDUCATION

- | | |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|
| University of Texas at Austin, TX
Ph.D., Department of Electrical and Computer Engineering
Dissertation: Placement Algorithms for Large-Scale Heterogeneous FPGAs
Advisor: David Z. Pan
(GPA 4.0/4.0) | <i>Jan. 2016 – Aug. 2019</i> |
| University of Texas at Austin, TX
M.S., Department of Electrical and Computer Engineering
(GPA 4.0/4.0) | <i>Aug. 2013 – Dec. 2015</i> |
| Shanghai Jiao Tong University, Shanghai, China
B.S. with Highest Honors, Department of Microelectronics
(GPA 90.1/100) | <i>Sep. 2009 – Jul. 2013</i> |

EXPERIENCE

- | | |
|--------------------------------------------------------------------------------------------|------------------------------|
| AMD (Xilinx), San Jose, CA
Principal Software Engineer, Vivado Placement Team | <i>Jul. 2024 – Present</i> |
| AMD (Xilinx), San Jose, CA
Senior Staff Software Engineer, Vivado Placement Team | <i>Jul. 2022 – Jun. 2024</i> |
| AMD (Xilinx), San Jose, CA
Staff Software Engineer, Vivado Placement Team | <i>Aug. 2019 – Jun. 2022</i> |
| Xilinx, San Jose, CA
Software Development Intern, Vivado Placement Team | <i>May 2018 – Aug. 2018</i> |
| Cadence Design System, Austin, TX
Software Development Intern, Clocking Team | <i>May 2016 – Dec. 2016</i> |
| Apple, Austin, TX
Hardware Design Intern, SoC Clocking Team | <i>Jan. 2015 – Dec. 2015</i> |
| Apple, Cupertino, CA
Hardware Design Intern, SoC Methodology Team | <i>Sep. 2014 – Dec. 2014</i> |
| ARM, Austin, TX
Hardware Design Intern, Memory Team | <i>May 2014 – Aug. 2014</i> |

PUBLICATIONS

Journal Articles

- [J9] Licheng Guo, Pongstorn Maidee, Yun Zhou, Chris Lavin, Eddie Hung, **Wuxi Li**, Jason Lau, Weikang Qiao, Yuze Chi, Linghao Song, Yuanlong Xiao, Alireza Kaviani, Zhiru Zhang, Jason Cong, “RapidStream 2.0: Automated Parallel Implementation of Latency Insensitive FPGA Designs Through Partial Reconfiguration”, ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2023.
- [J8] Yibai Meng, **Wuxi Li**, Yibo Lin, David Z. Pan, “elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2021.

- [J7] Yibo Lin, Zixuan Jiang, Jiaqi Gu, **Wuxi Li**, Shounak Dhar, Haoxing Ren, Brucek Khailany, David Z. Pan, “DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2020. (**Best Paper Award**)
- [J6] Yibo Lin, **Wuxi Li**, Jiaqi Gu, Haoxing Ren, Brucek Khailany, David Z. Pan, “ABCDPlace: Accelerated Batch-based Concurrent Detailed Placement on Multi-threaded CPUs and GPUs”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2020.
- [J5] **Wuxi Li**, David Z. Pan, “A New Paradigm for FPGA Placement without Explicit Packing”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2018.
- [J4] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, David Z. Pan, “A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2018.
- [J3] **Wuxi Li**, Yibo Lin, Meng Li, Shounak Dhar, David Z. Pan, “UTPlaceF 2.0: A High-Performance Clock-Aware FPGA Placement Engine”, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2018. (**1st-Place Award of ISPD 2017 Contest**)
- [J2] **Wuxi Li**, Shounak Dhar, David Z. Pan, “UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2017.
- [J1] **Wuxi Li**, Hang Yuan, Wei Xu, Kunling Geng, Guoxing Wang, “An Optimization Procedure for Coil Design in a Dual Band Wireless Power and Data Transmission System”, ECS Transactions (ECST), 2013.

Conference Papers

- [C16] **Wuxi Li**, Yuji Kukimoto, Gregory Servel, Ismail Bustany, Mehrdad E. Dehkordi, “Calibration-Based Differentiable Timing Optimization in Non-linear Global Placement”, ACM International Symposium on Physical Design (ISPD), 2024.
- [C15] Hailiang Hu, Donghao Fang, **Wuxi Li**, Bo Yuan, Jiang Hu, “Systolic Array Placement on FPGAs”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2023.
- [C14] Ismail Bustany, Grigor Gasparyan, Amit Gupta, Andrew B. Kahng, Meghraj Kalase, **Wuxi Li**, Bodhisatta Pramanik, “The 2023 MLCAD FPGA Macro Placement Benchmark Design Suite and Contest Results”, ACM/IEEE Workshop on Machine Learning for CAD (MLCAD), 2023.
- [C13] Zizheng Guo, Zuodong Zhang, Xun Jiang, **Wuxi Li**, Yibo Lin, Runsheng Wang, Ru Huang, “General-Purpose Gate-Level Simulation with Partition-Agnostic Parallelism”, ACM/IEEE Design Automation Conference (DAC), 2023.
- [C12] Donghao Fang, Boyang Zhang, Hailiang Hu, **Wuxi Li**, Bo Yuan, Jiang Hu, “Global Placement Exploiting Soft 2D Regularity”, ACM International Symposium on Physical Design (ISPD), 2022.
- [C11] Jiaqi Gu, Zheng Zhao, Chenghao Feng, **Wuxi Li**, Ray T. Chen, David Z. Pan, “FLOPS: Efficient On-Chip Learning for Optical Neural Networks Through Stochastic Zeroth-Order Optimization”, ACM/IEEE Design Automation Conference (DAC), 2020.
- [C10] Mohamed B. Alawieh, **Wuxi Li**, Yibo Lin, Love Singhal, Mahesh Iyer, David Z. Pan, “High-Definition Routing Congestion Prediction for Large-Scale FPGAs”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2020.
- [C9] Mingjie Liu, **Wuxi Li**, Keren Zhu, Biying Xu, Yibo Lin, Linxiao Shen, Xiyuan Tang, Nan Sun, David Z. Pan, “S3DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2020.
- [C8] **Wuxi Li**, Yibo Lin, David Z. Pan, “elfPlace: Electrostatics-based Placement for Large-Scale Heterogeneous FPGAs”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2019. (**Best-in-Track Paper**)
- [C7] Yibo Lin, Shounak Dhar, **Wuxi Li**, Haoxing Ren, Brucek Khailany, David Z. Pan, “DREAMPlace: Deep Learning Toolkit-Enabled GPU Acceleration for Modern VLSI Placement”, ACM/IEEE Design Automation Conference (DAC), 2019. (**Best Paper Award**)

- [C6] **Wuxi Li**, Stephen Yang, Mehrdad E. Dehkordi, David Z. Pan, “Simultaneous Placement and Clock Tree Construction for Modern FPGAs”, ACM International Symposium on Field-Programmable Gate Arrays (FPGA), 2019.
- [C5] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, David Z. Pan, “A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2018.
- [C4] **Wuxi Li**, Meng Li, Jiajun Wang, David Z. Pan, “UTPlaceF 3.0: A Parallelization Framework for Modern FPGA Global Placement”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2017. (**Invited Paper**)
- [C3] Wei Ye, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, Yiwei Fu, Yongsheng Sun, Canhui Zhan, David Z. Pan, “Placement Mitigation Techniques for Power Grid Electromigration”, IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2017.
- [C2] **Wuxi Li**, Shounak Dhar, David Z. Pan, “UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2016. (**Invited Paper, 1st-Place Award of ISPD 2016 Contest**)
- [C1] Wei Xu, Xiyan Li, **Wuxi Li**, Hang Yuan, Guoxing Wang, “Live demonstration: An Optimization Software and a Design Case of a Novel Dual Band Wireless Power and Data Transmission System”, IEEE International Symposium on Circuits and Systems (ISCAS), 2014.

RELATED COURSES

• EE382M: VLSI I	<i>Prof. Michael Orshansky</i>
• EE382N: Computer Architecture	<i>Prof. Aater Suleman</i>
• EE382V: Optimization Issues in VLSI CAD	<i>Prof. David Pan</i>
• EE382M: VLSI II	<i>Prof. Jacob Abraham</i>
• EE380L: Engineer Programming Languages	<i>Prof. Craig Chase</i>
• EE382V: VLSI Physical Design Automation	<i>Prof. David Pan</i>
• EE382N: High-Speed Computer Arithmetic	<i>Prof. Earl Swartzlander</i>
• EE382M: Verification of Digital Systems	<i>Dr. Jayanta Bhadra</i>
• INF385M: Database Management	<i>Dr. Stan Gunn</i>
• INF385T: Metadata Generation/Interface for Massive Dataset	<i>Prof. Unmil Karadkar</i>
• EE380N: Optimization in Engineering Systems	<i>Prof. Ross Baldick</i>
• CS383C: Numerical Analysis: Linear Algebra	<i>Prof. George Biros</i>

SKILLS

Programming Languages

C/C++, L^AT_EX, Perl, Python, Verilog

Operating Systems

Linux/UNIX

EDA Tools

Cadence Virtuoso, Synopsys Design Compiler, Synopsys IC Compiler, Synopsys PrimeTime

AWARDS AND HONORS

Outstanding TPC Member	DAC	2024
Best Paper Award	TCAD	2021
Best Paper Award	DAC	2019
Silver Medal at ACM/SIGDA Student Research Competition	ACM/SIGDA	2018
George J. Heuer, Jr. Ph.D. Endowed Graduate Fellowship Fund	UT Austin	2018
3rd-Place Winner of Intern Showcase Presentation	Xilinx	2018

1st-Place Winner of Clock-Aware FPGA Placement Contest	ISPD	2017
1st-Place Winner of Routability-Driven FPGA Placement Contest	ISPD	2016
Graduation with Highest Honors, College Graduate Excellence Award of Shanghai	SJTU	2013
Excellent Bachelor Dissertation Award (Top 39/3900+)	SJTU	2013