

# YIBO LIN

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## RESEARCH INTERESTS

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Design automation for VLSI

## EDUCATION

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| <b>University of Texas at Austin, TX, US</b><br>Ph.D. student, Department of Electrical and Computer Engineering<br>Advisor: David Z. Pan<br>(GPA 4.0/4.0) | <i>Jan. 2016 – Present</i>   |
| <b>University of Texas at Austin, TX, US</b><br>M.S., Department of Electrical and Computer Engineering<br>(GPA 4.0/4.0)                                   | <i>Aug. 2013 – Dec. 2015</i> |
| <b>Shanghai Jiao Tong University, Shanghai, China</b><br>B.S., Department of Microelectronics<br>(GPA 90.1/100)                                            | <i>Sep. 2009 – Jul. 2013</i> |

## EXPERIENCE

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| <b>Xilinx Inc., San Jose, CA</b><br><i>Software Development Intern, Vivado Implementation Team</i>                                                                                                                                                                                                                                                                                                         | <i>May 2018 – Aug. 2018</i>  |
| <b>Cadence Design System, Austin, TX</b><br><i>Software Development Intern, Clocking Team</i>                                                                                                                                                                                                                                                                                                              | <i>May 2016 – Dec. 2016</i>  |
| <b>Apple Inc., Austin, TX</b><br><i>Hardware Design Intern, SoC Clocking Team</i>                                                                                                                                                                                                                                                                                                                          | <i>Jan. 2015 – Dec. 2015</i> |
| <b>Apple Inc., Cupertino, CA</b><br><i>Hardware Design Intern, SoC Methodology Team</i>                                                                                                                                                                                                                                                                                                                    | <i>Sep. 2014 – Dec. 2014</i> |
| <b>ARM Inc., Austin, TX</b><br><i>Hardware Design Intern, Memory Team</i>                                                                                                                                                                                                                                                                                                                                  | <i>May 2014 – Aug. 2014</i>  |
| <b>ECE Department, University of Texas at Austin, Austin, TX</b><br><i>Graduate Student</i> <ul style="list-style-type: none"><li>· Research Assistant</li><li>· Teaching Assistant of VLSI-II, Spring 2016 and 2017</li><li>· Simultaneous FPGA placement and packing</li><li>· FPGA placement parallelization</li><li>· Clock-aware FPGA placement</li><li>· Routability-driven FPGA placement</li></ul> | <i>Aug. 2013 – Present</i>   |

## PUBLICATIONS

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### Journal Articles

- [J5] **Wuxi Li**, David Z. Pan, “A New Paradigm for FPGA Placement without Explicit Packing”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2018. (**Accepted**)
- [J4] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, David Z. Pan, “A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2018. (**Accepted**)

- [J3] **Wuxi Li**, Yibo Lin, Meng Li, Shounak Dhar, David Z. Pan, “UTPlaceF 2.0: A High-Performance Clock-Aware FPGA Placement Engine”, ACM Transactions on Design Automation of Electronic Systems (TODAES), 2018. (**1st-Place Award of ISPD 2017 Contest**)
- [J2] **Wuxi Li**, Shounak Dhar, David Z. Pan, “UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing”, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2017.
- [J1] **Wuxi Li**, Hang Yuan, Wei Xu, Kunling Geng, Guoxing Wang, “An Optimization Procedure for Coil Design in a Dual Band Wireless Power and Data Transmission System”, ECS Transactions (ECST), 2013.

#### Conference Papers

- [C5] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, David Z. Pan, “A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion”, IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2018.
- [C4] **Wuxi Li**, Meng Li, Jiajun Wang, David Z. Pan, “UTPlaceF 3.0: A Parallelization Framework for Modern FPGA Global Placement”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2017. (**Invited Paper**)
- [C3] Wei Ye, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, Yiwei Fu, Yongsheng Sun, Canhui Zhan, David Z. Pan, “Placement Mitigation Techniques for Power Grid Electromigration”, IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2017.
- [C2] **Wuxi Li**, Shounak Dhar, David Z. Pan, “UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing”, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2016. (**Invited Paper, 1st-Place Award of ISPD 2016 Contest**)
- [C1] Wei Xu, Xiyang Li, **Wuxi Li**, Hang Yuan, Guoxing Wang, “Live demonstration: An Optimization Software and a Design Case of a Novel Dual Band Wireless Power and Data Transmission System”, IEEE International Symposium on Circuits and Systems (ISCAS), 2014.

#### RELATED COURSES

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• EE382M: VLSI I	<i>Prof. Michael Orshansky</i>
• EE382N: Computer Architecture	<i>Prof. Aater Suleman</i>
• EE382V: Optimization Issues in VLSI CAD	<i>Prof. David Pan</i>
• EE382M: VLSI II	<i>Prof. Jacob Abraham</i>
• EE380L: Engineer Programming Languages	<i>Prof. Craig Chase</i>
• EE382V: VLSI Physical Design Automation	<i>Prof. David Pan</i>
• EE382N: High-Speed Computer Arithmetic	<i>Prof. Earl Swartzlander</i>
• EE382M: Verification of Digital Systems	<i>Dr. Jayanta Bhadra</i>
• INF385M: Database Management	<i>Dr. Stan Gunn</i>
• INF385T: Metadata Generation/Interface for Massive Dataset	<i>Prof. Unmil Karadkar</i>
• EE380N: Optimization in Engineering Systems	<i>Prof. Ross Baldick</i>
• CS383C: Numerical Analysis: Linear Algebra	<i>Prof. George Biros</i>

#### SKILLS

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##### Programming Languages

C/C++, Perl, Python, Verilog

##### EDA Tools

Cadence Virtuoso, Synopsys Design Compiler, Synopsys IC Compiler, Synopsys PrimeTime

#### AWARDS AND HONORS

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Silver Medal at ACM/SIGDA Student Research Competition	ACM/SIGDA	2018
George J. Heuer, Jr. Ph.D. Endowed Graduate Fellowship Fund	UT-Austin	2018
3rd-Place Winner of Intern Showcase Presentation	Xilinx	2018
1st-Place Winner of Clock-Aware FPGA Placement Contest	ISPD	2017
1st-Place Winner of Routability-Driven FPGA Placement Contest	ISPD	2016
Graduation with Honor, College Graduate Excellence Award of Shanghai	SJTU	2013
Excellent Bachelor Dissertation Award (Top 39/3900+)	SJTU	2013
Toshiba Electronics Scholarship	SJTU	2012