WUXI LI

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Ph.D. Student ◇ Department of Eletrical and Computer Engineering

RESEARCH INTERESTS

Design automation for VLSI

EDUCATION

University of Texas at Austin, TX, US *Jan. 2016 – Present*
Ph.D. student, Department of Electrical and Computer Engineering
Advisor: David Z. Pan
(GPA 4.0/4.0)

University of Texas at Austin, TX, US *Aug. 2013 – Dec. 2015*
M.S., Department of Electrical and Computer Engineering
(GPA 4.0/4.0)

Shanghai Jiao Tong University, Shanghai, China *Sep. 2009 – Jul. 2013*
B.S., Department of Microelectronics
(GPA 90.1/100)

EXPERIENCE

Xilinx Inc., San Jose, CA *May 2018 – Aug. 2018*
Software Development Intern, Vivado Implementation Team

Cadence Design System, Austin, TX *May 2016 – Dec. 2016*
Software Development Intern, Clocking Team

Apple Inc., Austin, TX *Jan. 2015 – Dec. 2015*
Hardware Design Intern, SoC Clocking Team

Apple Inc., Cupertino, CA *Sep. 2014 – Dec. 2014*
Hardware Design Intern, SoC Methodology Team

ARM Inc., Austin, TX *May 2013 – Aug. 2014*
Hardware Design Intern, Memory Team

ECE Department, University of Texas at Austin, Austin, TX *Aug. 2013 – Present*
Graduate Student
· Research Assistant
· Teaching Assistant of VLSI-II, Spring 2016 and 2017
· Simultaneous FPGA placement and packing
· FPGA placement parallelization
· Clock-aware FPGA placement
· Routability-driven FPGA placement

PUBLICATIONS

Journal Articles

[J4] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, David Z. Pan, "A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2018.

[J3] **Wuxi Li**, Yibo Lin, Meng Li, Shounak Dhar, David Z. Pan, "UTPlaceF 2.0: A High-Performance Clock-Aware FPGA Placement Engine", ACM Transactions on Design Automation of Electronic Systems (TODAES), 2018. (**1st-Place Award of ISPD 2017 Contest**)

[J2] **Wuxi Li**, Shounak Dhar, David Z. Pan, "UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2017.

[J1] **Wuxi Li**, Hang Yuan, Wei Xu, Kunling Geng, Guoxing Wang, "An Optimization Procedure for Coil Design in a Dual Band Wireless Power and Data Transmission System", ECS Transactions (ECST), 2013.

Conference Papers

[C5] Meng Li, Bei Yu, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, David Z. Pan, "A Practical Split Manufacturing Framework for Trojan Prevention via Simultaneous Wire Lifting and Cell Insertion", IEEE/ACM Asia and South Pacific Design Automation Conference (ASPDAC), 2018.

[C4] **Wuxi Li**, Meng Li, Jiajun Wang, David Z. Pan, "UTPlaceF 3.0: A Parallelization Framework for Modern FPGA Global Placement", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2017. (**Invited Paper**)

[C3] Wei Ye, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, Yiwei Fu, Yongsheng Sun, Canhui Zhan, David Z. Pan, "Placement Mitigation Techniques for Power Grid Electromigration", IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2017.

[C2] **Wuxi Li**, Shounak Dhar, David Z. Pan, "UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2016. (**Invited Paper, 1st-Place Award of ISPD 2016 Contest**)

[C1] Wei Xu, Xiyan Li, **Wuxi Li**, Hang Yuan, Guoxing Wang, "Live demonstration: An Optimization Software and a Design Case of a Novel Dual Band Wireless Power and Data Transmission System", IEEE International Symposium on Circuits and Systems (ISCAS), 2014.

RELATED COURSES

- EE382M: VLSI I — *Prof. Michael Orshansky*
- EE382N: Computer Architecture — *Prof. Aater Suleman*
- EE382V: Optimization Issues in VLSI CAD — *Prof. David Pan*
- EE382M: VLSI II — *Prof. Jacob Abraham*
- EE380L: Engineer Programming Languages — *Prof. Craig Chase*
- EE382V: VLSI Physical Design Automation — *Prof. David Pan*
- EE382N: High-Speed Computer Arithmetic — *Prof. Earl Swartzlander*
- EE382M: Verification of Digital Systems — *Dr. Jayanta Bhadra*
- INF385M: Database Management — *Dr. Stan Gunn*
- INF385T: Metadata Generation/Interface for Massive Dataset — *Prof. Unmil Karadkar*
- EE380N: Optimization in Engineering Systems — *Prof. Ross Baldick*
- CS383C: Numerical Analysis: Linear Algebra — *Prof. George Biros*

SKILLS

Programming Languages
C/C++, Perl, Python, Verilog

EDA Tools
Cadence Virtuoso, Synopsys Design Compiler, Synopsys IC Compiler, Synopsys PrimeTime

AWARDS AND HONORS

1st-Place Winner of Clock-Aware FPGA Placement Contest	ISPD	2017
1st-Place Winner of Routability-Driven FPGA Placement Contest	ISPD	2016
A. Richard Newton Young Student Fellow	DAC	2016
Graduation with Honor, College Graduate Excellence Award of Shanghai	Shanghai Jiao Tong University	2013

Excellent Bachelor Dissertation Award (Top 39/3900+) Shanghai Jiao Tong University 2013
Toshiba Electronics Scholarship Shanghai Jiao Tong University 2012