

WUXI LI

University of Texas at Austin ◊ Austin, TX 78712

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RESEARCH INTERESTS

Physical design automation for VLSI

EDUCATION

University of Texas at Austin, TX

Jan. 2016 - Present

Ph.D. student, Department of Electrical and Computer Engineering

Advisor: David Z. Pan

GPA: 4.0/4.0

University of Texas at Austin, TX

Aug. 2013 - Dec. 2015

M.S., Department of Electrical and Computer Engineering

GPA: 4.0/4.0

Shanghai Jiao Tong University, Shanghai, China

Sep. 2009 - Jul. 2013

B.S., School of Microelectronics

GPA: 90.1/100.0

EXPERIENCE

Cadence Design System

May 2016 - Dec. 2016

Software Development Intern

Austin, TX

- Fast buffer insertion

Apple Inc.

Sep. 2014 - Dec. 2015

Physical Design Intern

Cupertino, CA & Austin, TX

- Low-power flip-flop design
- Static timing analysis

ARM Inc.

May. 2014 - Aug. 2014

Memory Design Intern

Austin, TX

- Fast memory leakage measurement

ECE Department, University of Texas at Austin

Aug. 2013 - Present

Graduate Student

Austin, TX

- Research Assistant
- Teaching Assistant of VLSI-II, Spring 2017
- Teaching Assistant of VLSI-II, Spring 2016

PUBLICATION

Journal Papers

- [J2] **Wuxi Li**, Shounak Dhar, and David Z. Pan, "UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2017. (accepted)

- [J1] **Wuxi Li**, Hang Yuan, Wei Xu, Kunling Geng, Guoxing Wang, "An Optimization Procedure for Coil Design in a Dual Band Wireless Power and Data Transmission System", ECS Transactions (ECST), 2013.

Conference Papers

- [C3] Wei Ye, Yibo Lin, Xiaoqing Xu, **Wuxi Li**, Yiwei Fu, Yongsheng Sun, Canhui Zhan and David Z. Pan, "Placement Mitigation Techniques for Power Grid Electromigration", IEEE International Symposium on Low Power Electronics and Design (ISLPED), Taipei, Jul. 24-26, 2017.
- [C2] **Wuxi Li**, Shounak Dhah, and David Z. Pan, "UTPlaceF: A Routability-Driven FPGA Placer with Physical and Congestion Aware Packing", IEEE/ACM International Conference on Computer-Aided Design (ICCAD), 2016. (**Invited Paper, 1st-Place Winner of ISPD'16 Contest**)
- [C1] Wei Xu, Xiyan Li, **Wuxi Li**, Hang Yuan, Guoxing Wang, "Live demonstration: An Optimization Software and a Design Case of a Novel Dual Band Wireless Power and Data Transmission System", IEEE International Symposium on Circuits and Systems (ISCAS), 2014.

COURSES

VLSI I	Prof. Michael Orshansky
Computer Architecture	Prof. Aater Suleman
Optimization Issues in VLSI CAD	Prof. David Pan
VLSI II	Prof. Jacob Abraham
Engineering Programming Languages	Prof. Craig Chase
Verification of Digital Systems	Dr. Jay Bhadra
VLSI Physical Design Automation	Prof. David Pan
Database Management	Dr. Stan Gunn
High-Speed Computer Arithmetic	Prof. Earl Swartzlander
Metadata Generation/Interface and mass Datasets	Prof. Unmil Karadkar
Optimization in Engineering Systems	Prof. Ross Baldick

SKILLS

Programming Languages

C/C++, Perl, Python, Verilog

EDA Tools

Cadence Virtuoso, Synopsys Design Compiler, Synopsys IC Compiler, Synopsys PrimeTime

HONORS AND AWARDS

1st-Place Winner of Clock-Aware FPGA Placement Contest	ISPD	2017
A. Richard Newton Young Student Fellow	DAC	2016
1st-Place Winner of Routability-Driven FPGA Placement Contest	ISPD	2016
Graduation with Honor, College Graduate Excellence Award of Shanghai	SJTU	2013
Excellent Bachelor Dissertation Award (Top 39/3900+)	SJTU	2013
Toshiba Electronics Scholarship	SJTU	2012
Academic Excellence Scholarship	SJTU	2011
Academic Excellence Scholarship	SJTU	2010