

# **C**ommunication

*MIAT-C3X FPGA Development Board*

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浯陽科技有限公司



**CSIE MIAT Lab.**  
*National Central University*

# Outline

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- ☐ Part I
  - Design Consideration
  - Buadrate Generator
  - Transmitter
- ☐ Part II
  - Receiver
- ☐ Part III
  - Time for Questions
- ☐ Part IV
  - Project Architecture
  - QuartusII Setting

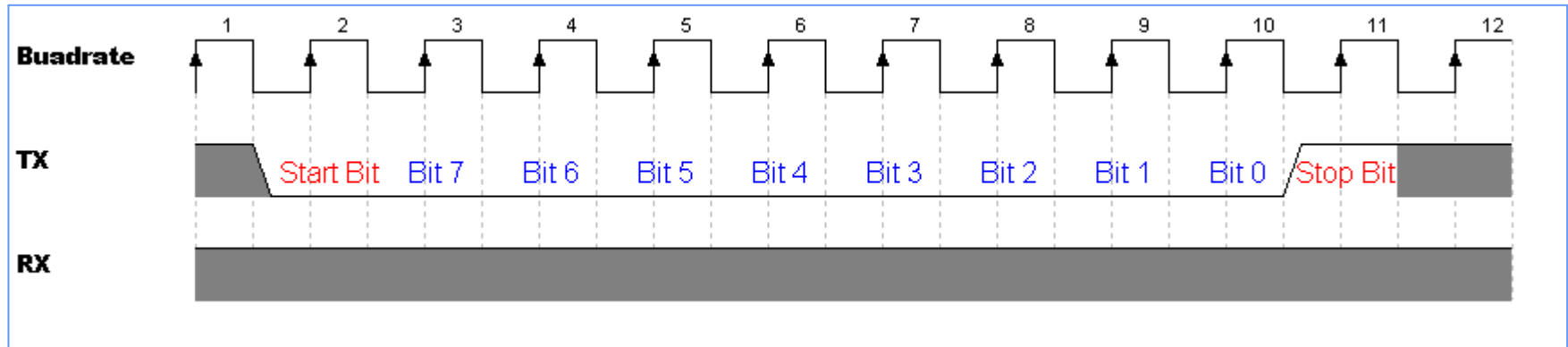
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Part – I

# UART TRANSMITTER DESIGN

# Transmitter – UART Communication Protocol

## □ UART Transmitter Protocol - Waveform



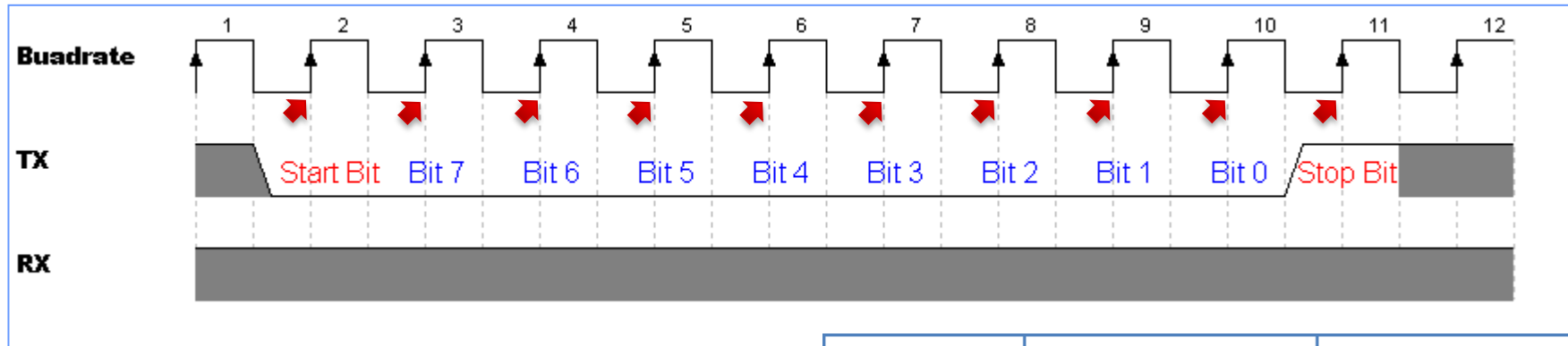
## □ Transmit from the last bit of the byte

■ 0x55(01010101<sub>2</sub>)



# Transmitter – Design Consideration

## □ Timing Diagram



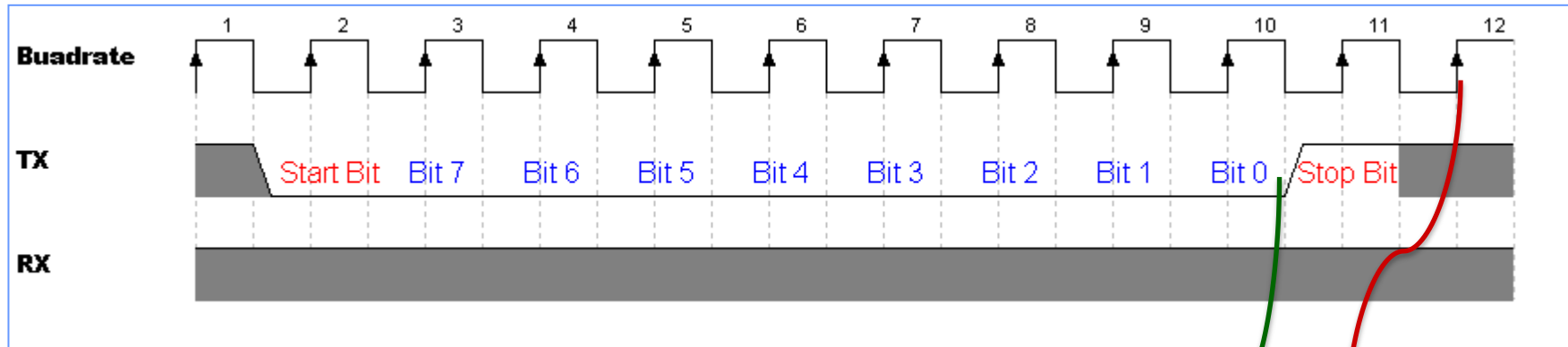
## □ Describe TX **behavior**

- **Serially**, shift 10 bits
- Hold a bit during a period

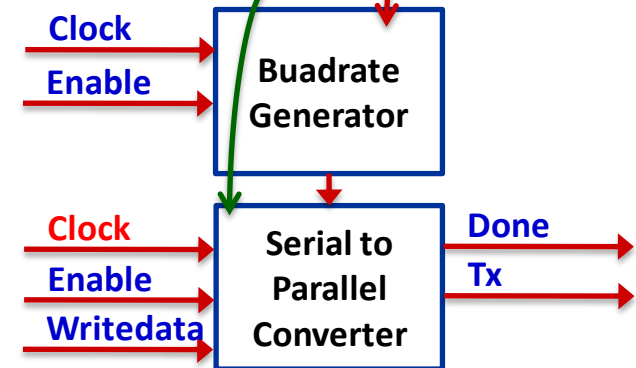
<u>Buadrate</u>	One Packet <sup>+</sup> Transmission Time	One Bit <sup>+</sup> Transmission Time
1200 bps	8330 us	833 us
2400 bps	4160 us	416 us
4800 bps	2080 us	208 us
9600 bps	1040 us	104 us
19200 bps	520 us	52 us
38400 bps	260 us	26 us
57600 bps	170 us	17 us
115200 bps	80 us	8 us

# Transmitter – Design Entity

## □ Timing Diagram

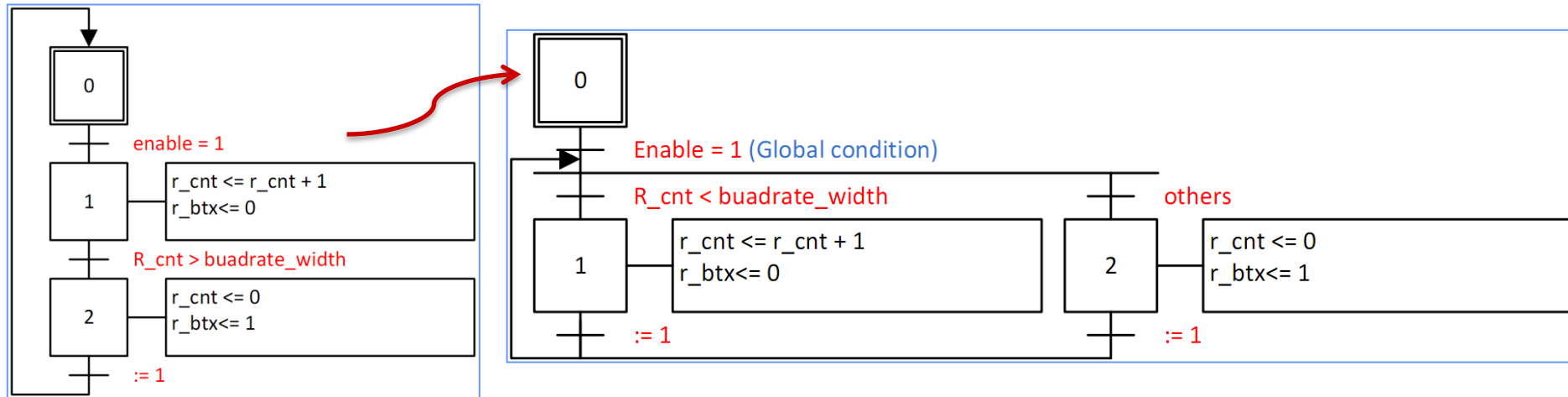


- Buadrate Generator Module
  - Compute period width
  - Output work signal
- Serial to Parallel Converter Module
  - Shift bit

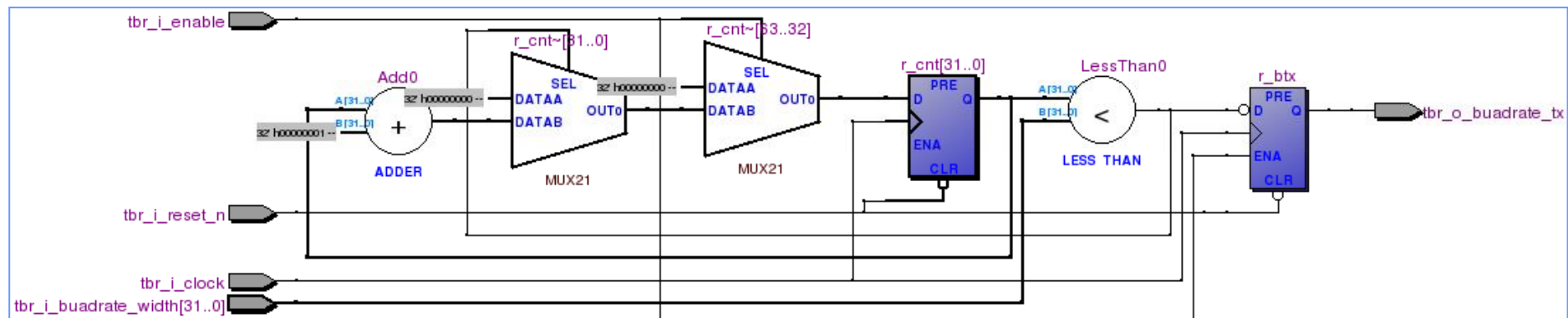


# Buadrate Gen. – Design Entity

## Behavior

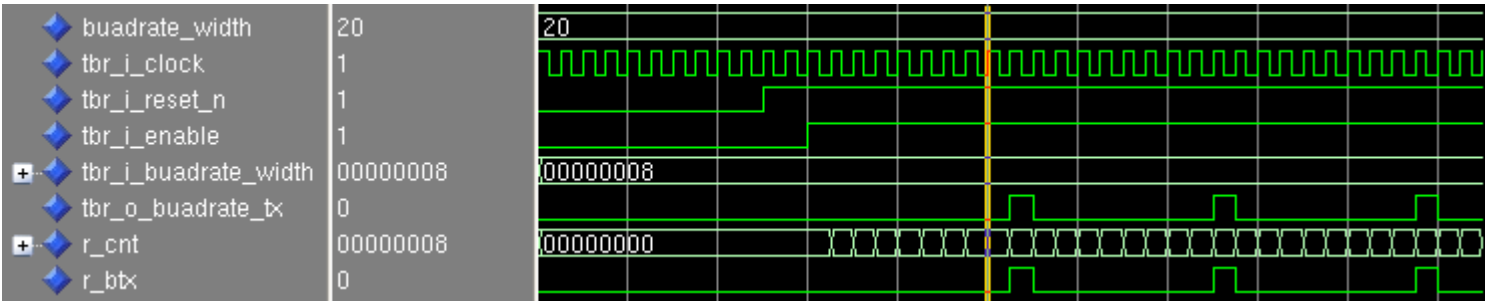


## RTL Viewer



# Exercise I – Buadrate Generator

- ☐ Design a Buadrate Generator Module
  - ☒ Generate a reference signal can be programmed period
- ☐ Simulate Result





# Exercise I – Buadrate Generator, Cont.

## ❑ Counter Bit Width

### ■ 32-bit Timing analyzer report

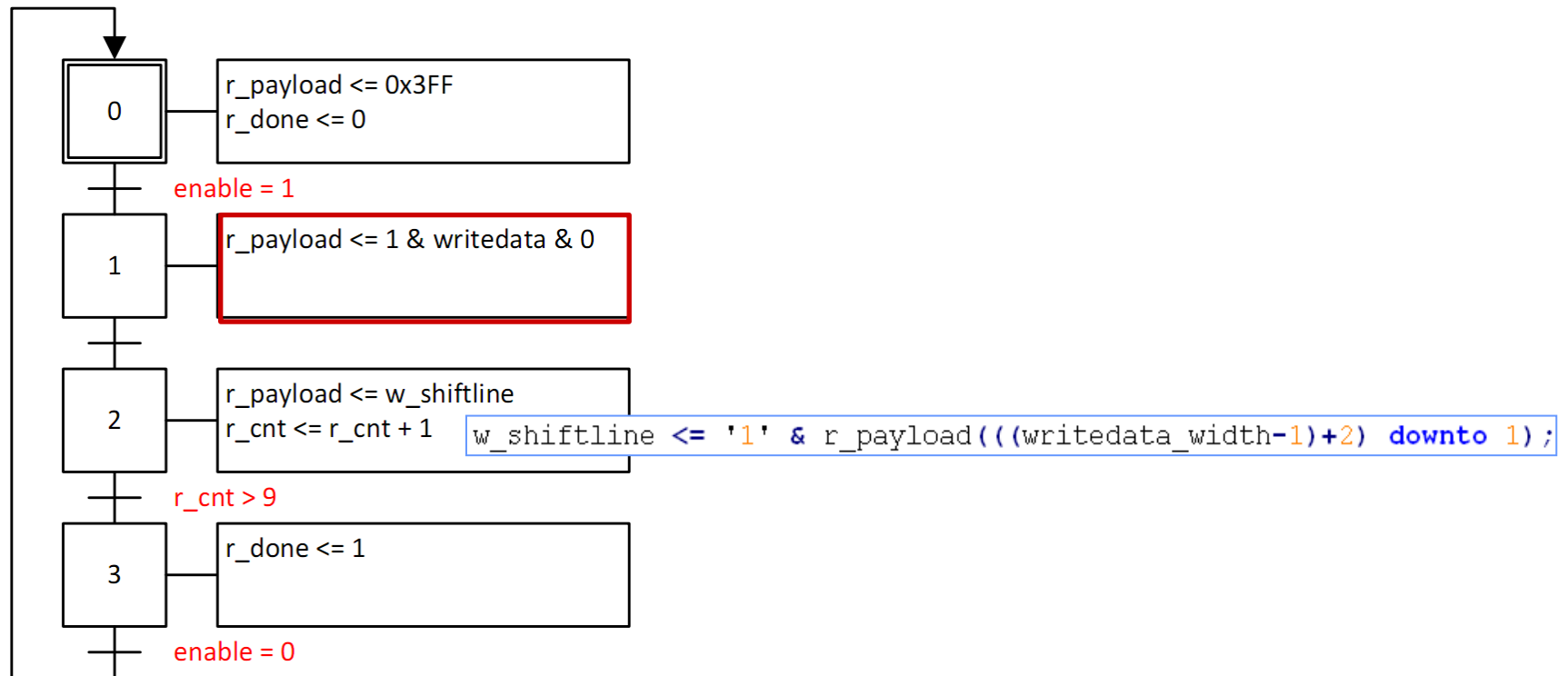
Timing Analyzer Summary						
	Type	Slack	Required Time	Actual Time	From	To
1	Worst-case tsu	N/A	None	7.844 ns	tbr_i_buadrate_width[4]	r_cnt[0]
2	Worst-case tco	N/A	None	6.872 ns	r_btx	tbr_o_buadrate_tx
3	Worst-case th	N/A	None	0.138 ns	tbr_i_enable	r_btx
4	Clock Setup: 'tbr_i_clock'	N/A	None	147.51 MHz ( period = 6.779 ns )	r_cnt[0]	r_cnt[0]
5	Total number of failed paths					

### ■ 8-bit Timing analyzer report

Timing Analyzer Summary						
	Type	Slack	Required Time	Actual Time	From	To
1	Worst-case tsu	N/A	None	5.188 ns	tbr_i_buadrate_width[2]	r_cnt[0]
2	Worst-case tco	N/A	None	7.959 ns	r_btx	tbr_o_buadrate_tx
3	Worst-case th	N/A	None	0.559 ns	tbr_i_enable	r_btx
4	Clock Setup: 'tbr_i_clock'	N/A	None	243.66 MHz ( period = 4.104 ns )	r_cnt[0]	r_cnt[0]
5	Total number of failed paths					

# PS Converter – Design Entity

## □ Behavior



# PS Converter – Synthesis Report

## □ Timing Report

### Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To
1	Worst-case tsu	N/A	None	3.101 ns	tx_i_writedata[2]	r_payload[3]
2	Worst-case tco	N/A	None	8.288 ns	r_payload[0]	tx_o_tx
3	Worst-case th	N/A	None	0.969 ns	tx_i_writedata[0]	r_payload[1]
4	Clock Setup: 'tx_i_clock'	N/A	None	Restricted to 250.00 MHz ( period = 4.000 ns )	m_state[0]	r_payload[7]
5	Total number of failed paths					

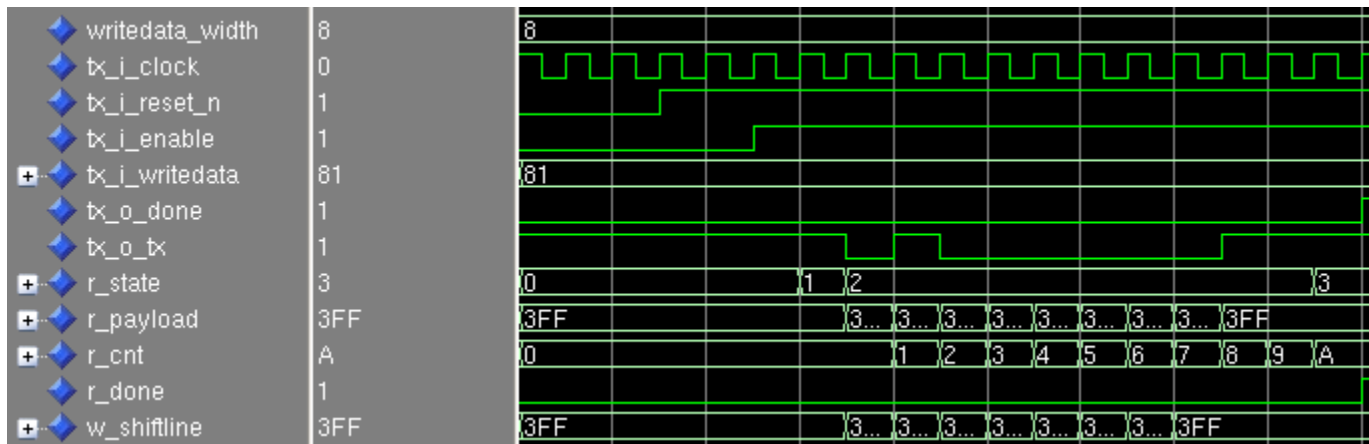
## □ Synthesis Report

### Flow Summary

Flow Status	Successful - Fri Jul 16 20:28:04 2010
Quartus II Version	10.0 Build 218 06/27/2010 SJ Full Version
Revision Name	miatc3x
Top-level Entity Name	transmitter
Family	Cyclone III
Device	EP3C25F256C8
Timing Models	Final
Met timing requirements	Yes
[-] Total logic elements	18 / 24,624 ( < 1 % )
Total combinational functions	18 / 24,624 ( < 1 % )
Dedicated logic registers	16 / 24,624 ( < 1 % )
Total registers	16
Total pins	13 / 157 ( 8 % )
Total virtual pins	0
Total memory bits	0 / 608,256 ( 0 % )
Embedded Multiplier 9-bit elements	0 / 132 ( 0 % )
Total PLLs	0 / 4 ( 0 % )

# Exercise II – PS Converter

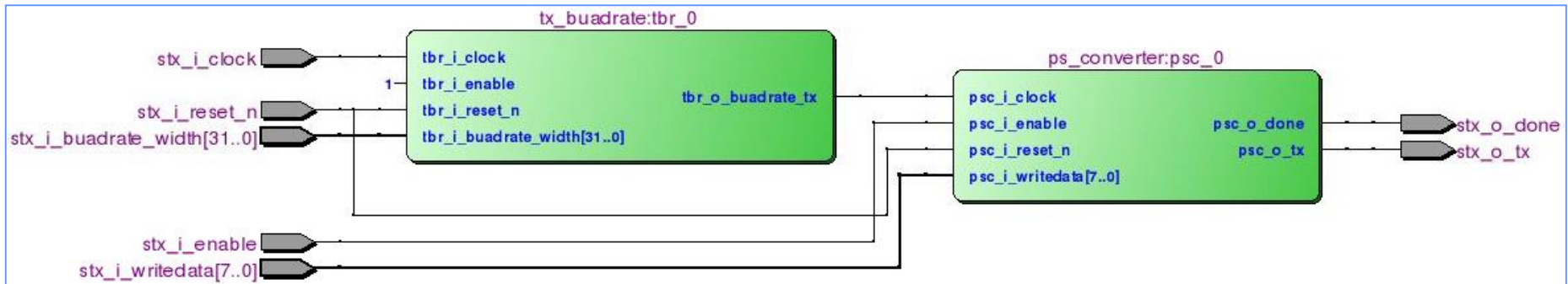
- ☐ Design a Parallel to Serial Converter
  - ☒ A shift controller
- ☐ Simulate



[Project Name] /uart\_divider2

# Exercise III – Serial Transmitter

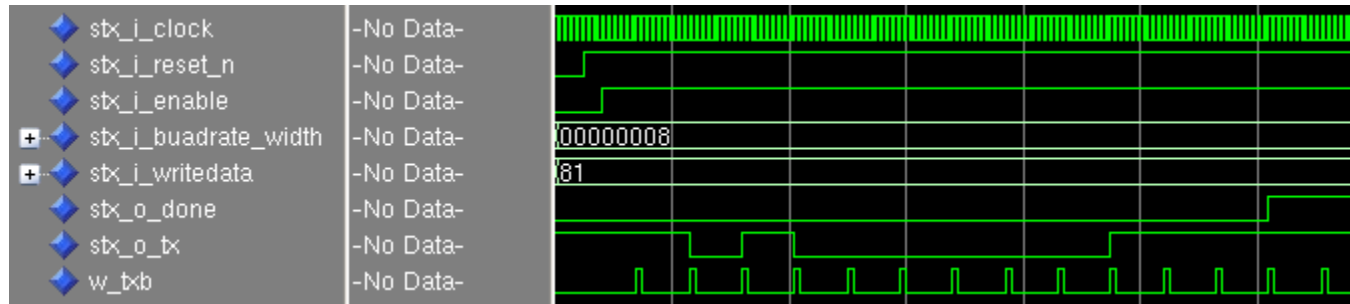
- Integrate Modules
  - Buadrate Generator
  - Parallel to Serial Converter
  - Use the reference signal to trigger the PX Converter



[Project Name] /uart\_divider2

# Exercise III – Serial Transmitter

## ☐ Simulate



## ☐ Issue

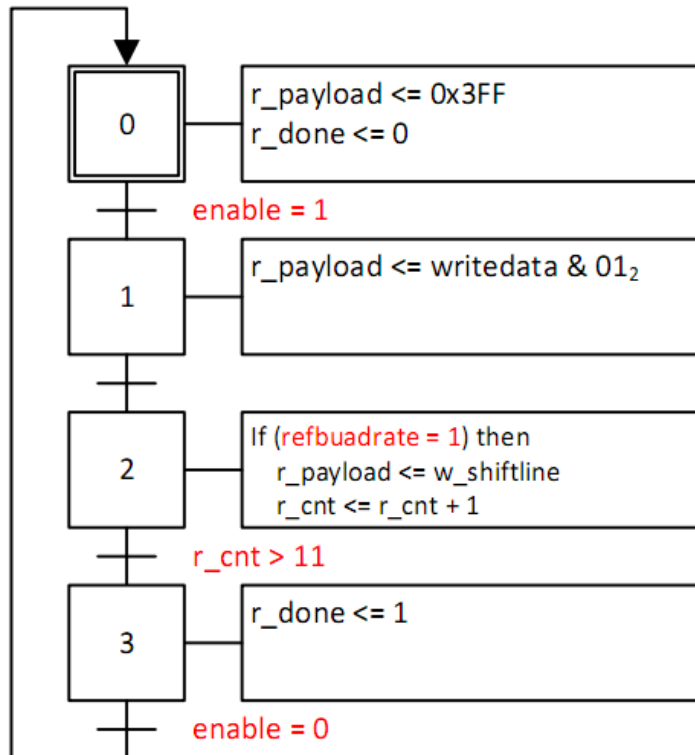


**Warning:** Found 1 node(s) in clock paths which may be acting as ripple and/or gated clocks  
 -- node(s) analyzed as buffer(s) resulting in clock skew

**Info:** Detected ripple clock "tx\_buadrate:tbr\_0|r\_btx" as buffer

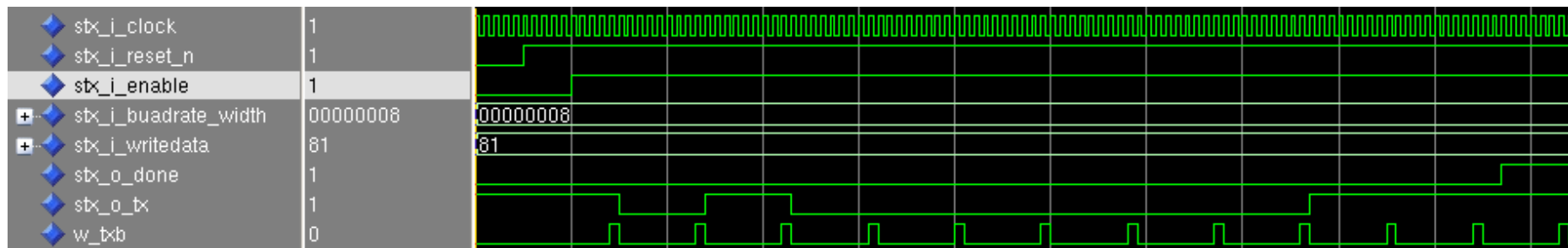
# Modified Serial Transmitter

## □ Behavior

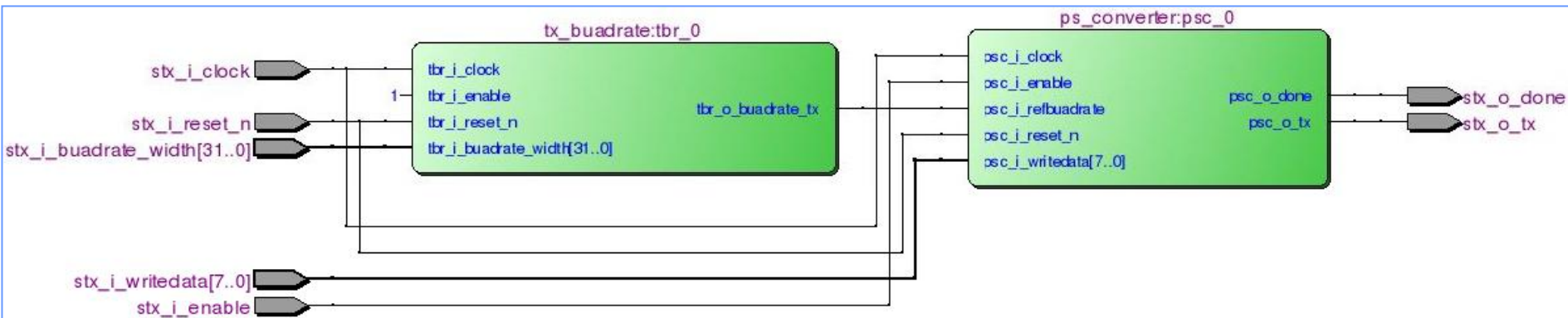


# Exercise VI – Modified Serial Transmitter

- ☐ Modified ripple clock issue
  - ☒ Modified reference signal approach
- ☐ Simulate



- ☐ RTL Viewer



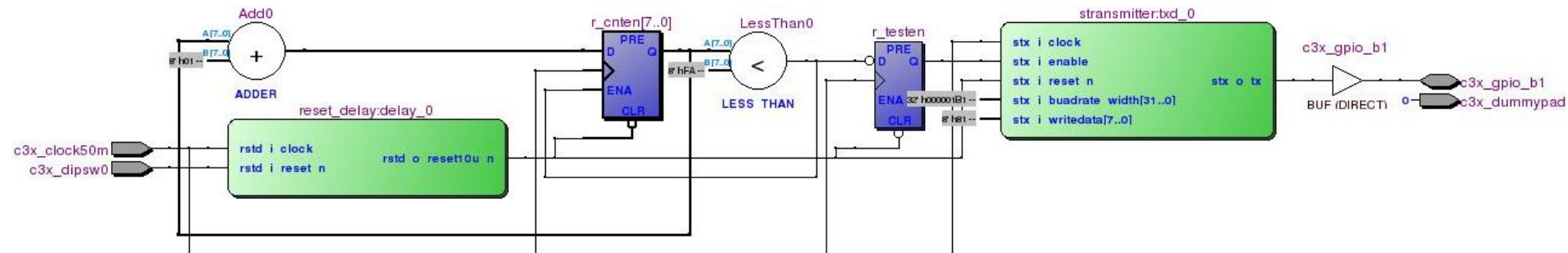
[Project Name] /uart\_para1



# Exercise V – Porting Serial Transmitter

## □ Porting Serial Transmitter to MIATC3X Board

- Reset synchronous issue
- IO mapping
- Top controller



## □ PC Client

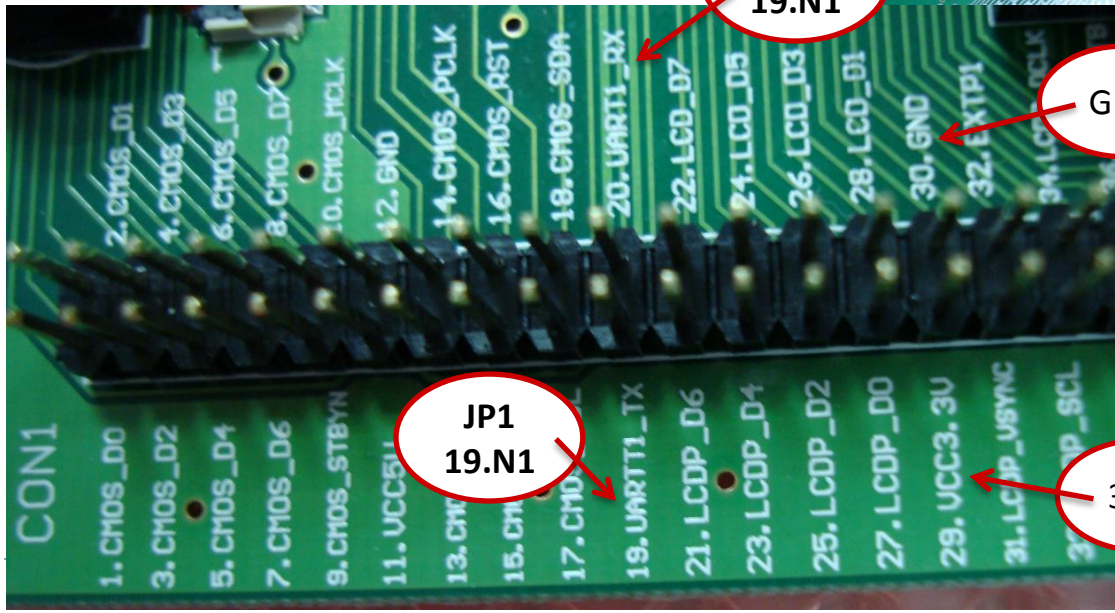
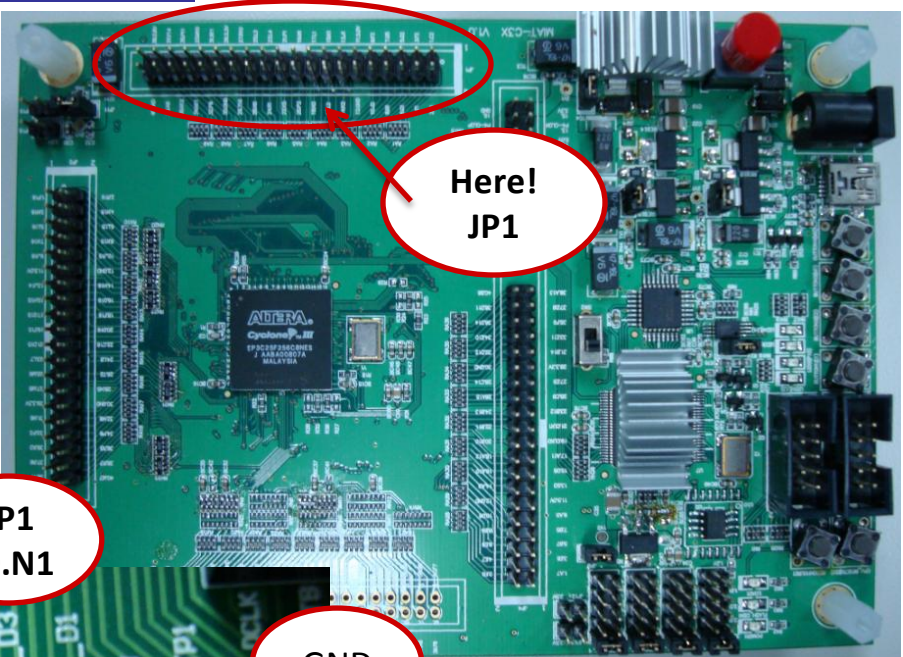


[Project Name] /uart\_para2

# MIATC3X Board PIN MAPPING

## Mapping Table

HDL Name	Pin Mapping	Description
c3x_clock50m	E16	miatc3x onboard
c3x_clock24m		miatc3x onboard
c3x_dipsw0	E1	miatc3x onboard
c3x_dipsw1	E2	miatc3x onboard
c3x_dipsw2		miatc3x onboard
c3x_dipsw3		miatc3x onboard
c3x_gpio_b1[0]	C2	miatc3x-JP1 1.C2
c3x_gpio_b1[16]	N1	miatc3x-JP1 19.N1
c3x_gpio_b1[17]	P2	miatc3x-JP1 20.P2



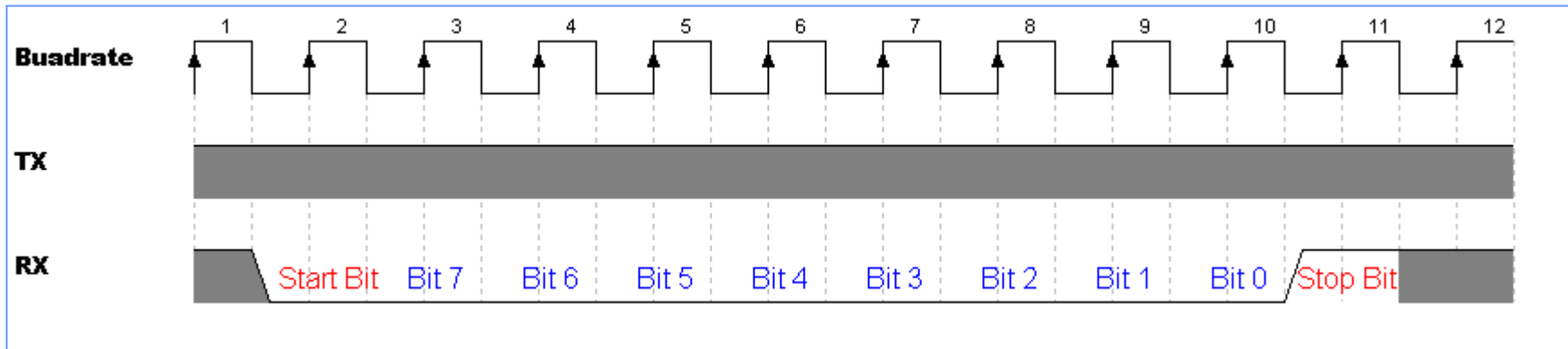
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Part – II

# UART RECEIVER DESIGN

# UART Communication Protocol – Receiver

## □ UART Receiver Protocol

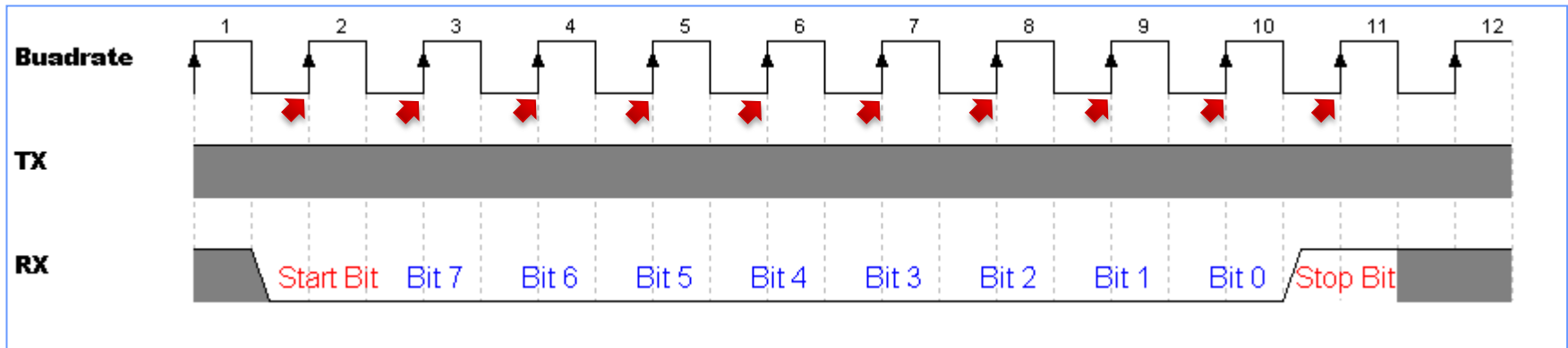


## □ Rx Signal

- Wait Start Bit
- Fetch Data Bit
- Detect Stop Bit

# Receiver – Design Consideration

## □ UART Receiver Protocol

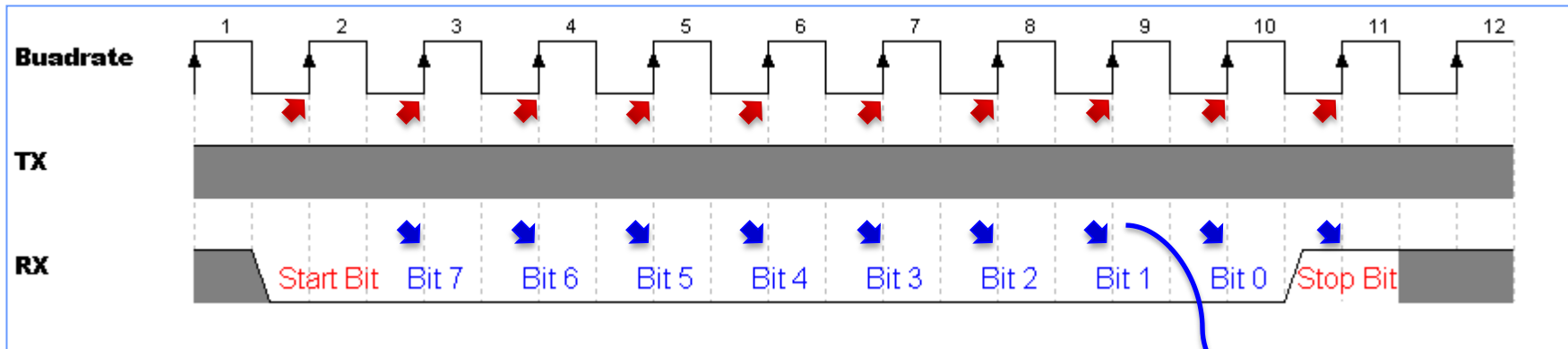


## □ Detect RX Bit

- Signal phase shift
- Error stop bit

# Receiver – Design Consideration, Cont.

## □ Timing Diagram

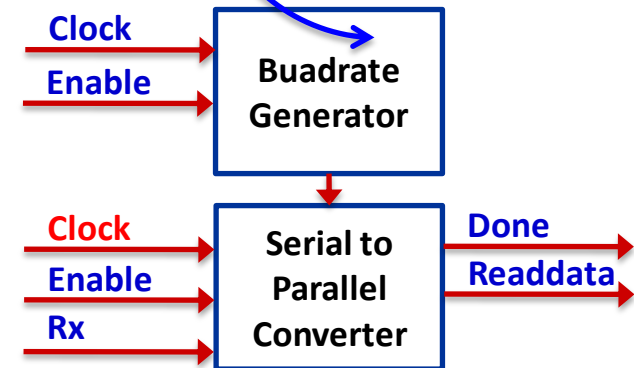


## □ Buadrate Generator

- Over Sampling
- Phase Shift
- Programmable

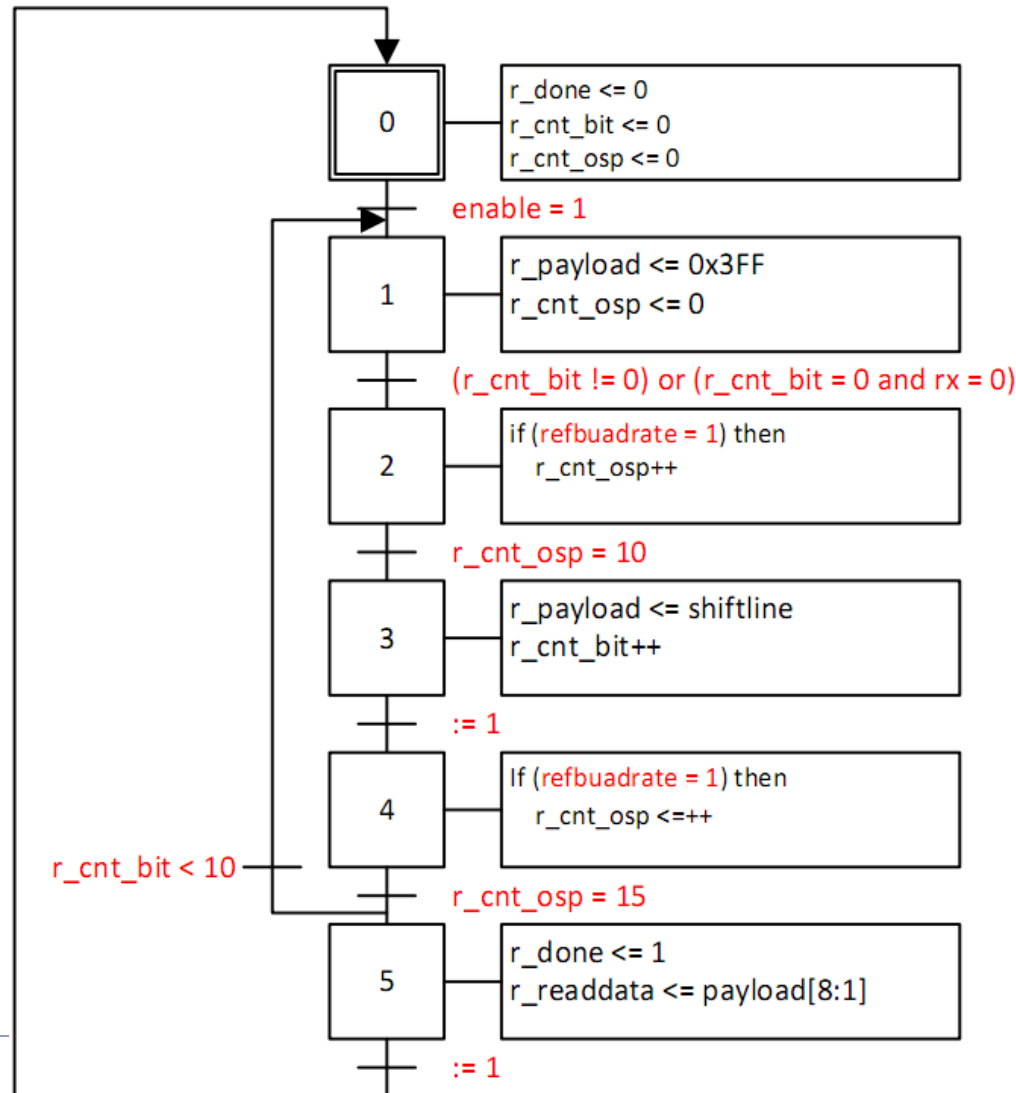
## □ SP Converter

- Fetch Data Bit



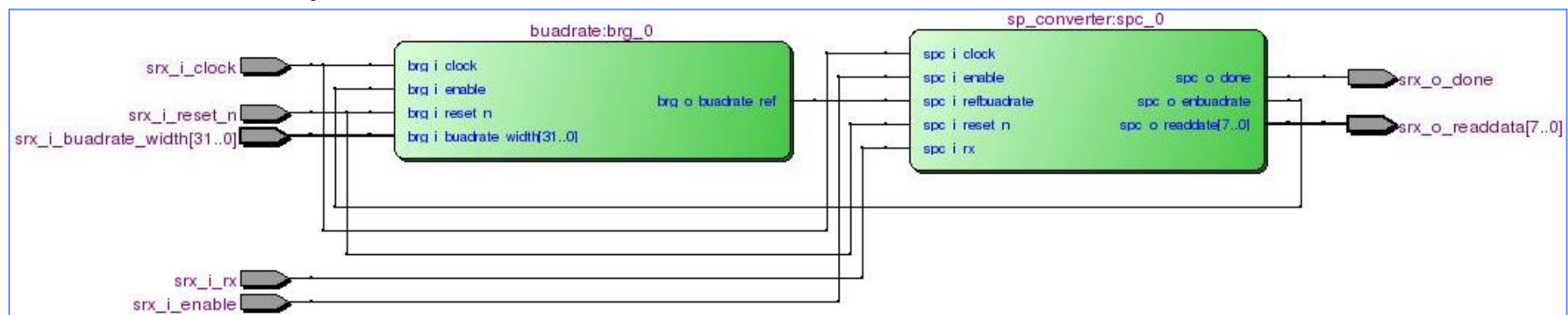
# Receiver – Design Entity

## □ Behavior



# Exercise VI – Serial Receiver

- Design Serial Receiver
  - Reuse Baudrate Generator
  - Implement Serial to Parallel Converter

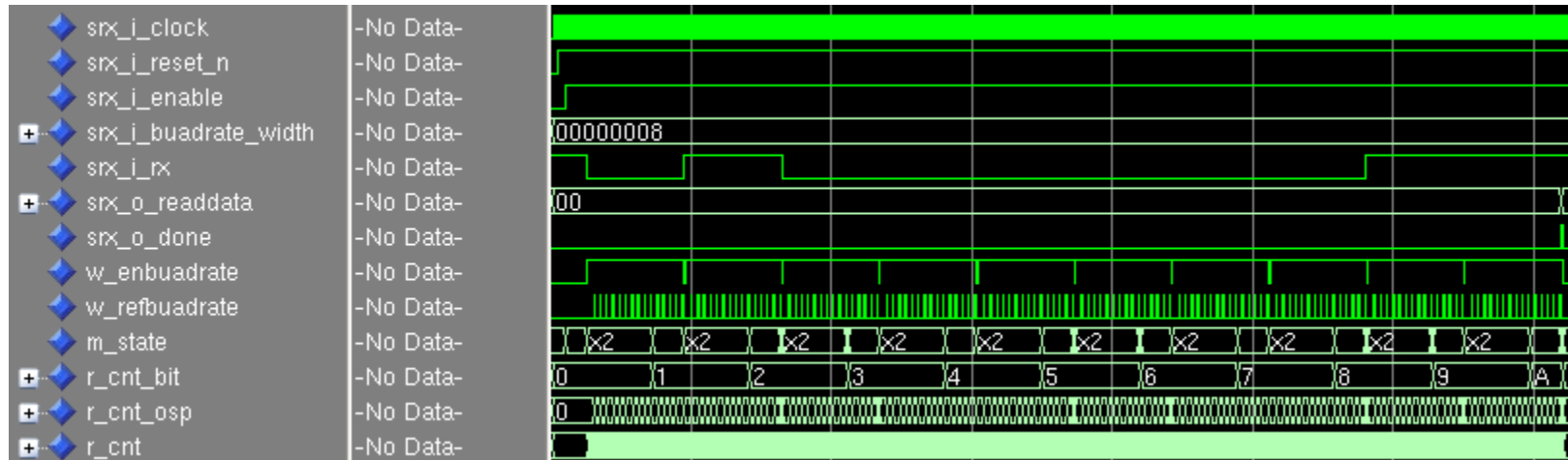


[Project Name] /uart\_receiver1



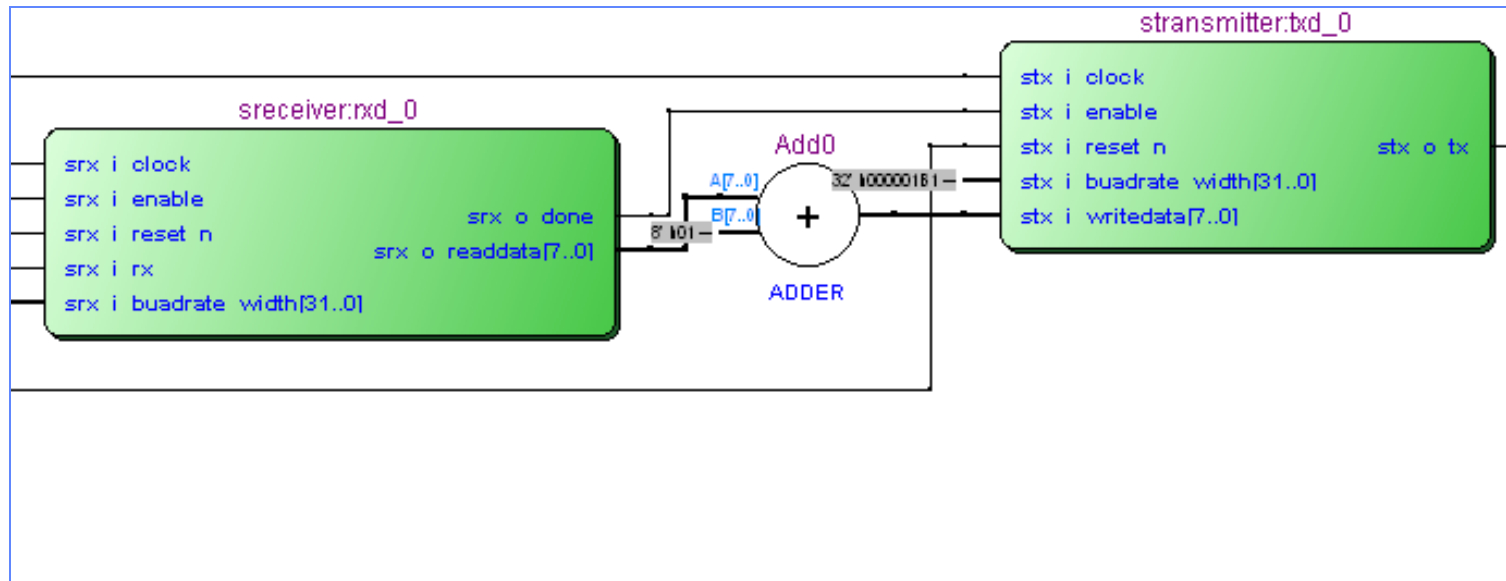
# Exercise VI – Serial Receiver, Cont.

## □ Simulate



# Exercise VII – Receiver and Transmitter

- Receive and transmit
  - Receive a value
  - Return it +1

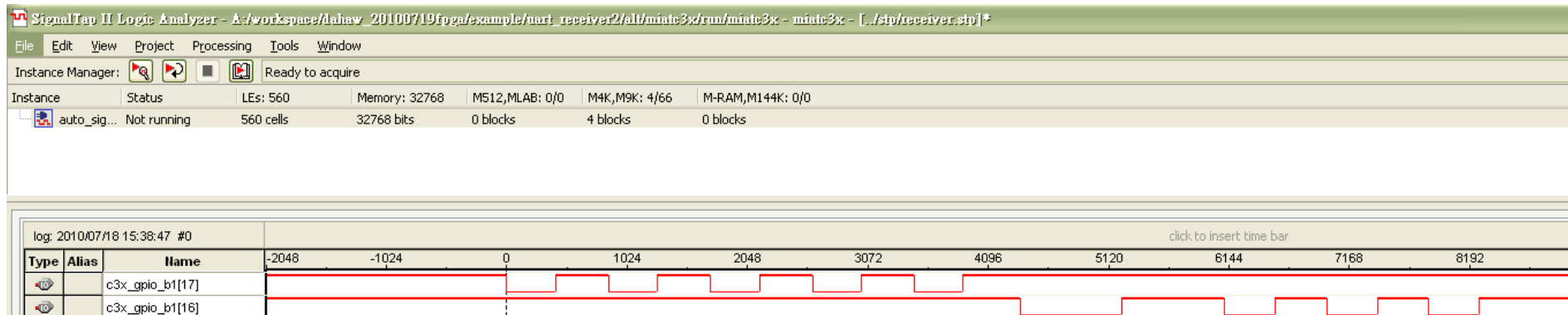


[Project Name] /uart\_receiver2

# Exercise VII – Receiver and Transmitter, Cont.

□ Monitor internal signal

■ SignalTapII



□ Client



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Part – III

# TIME FOR QUESTION

***Note:***

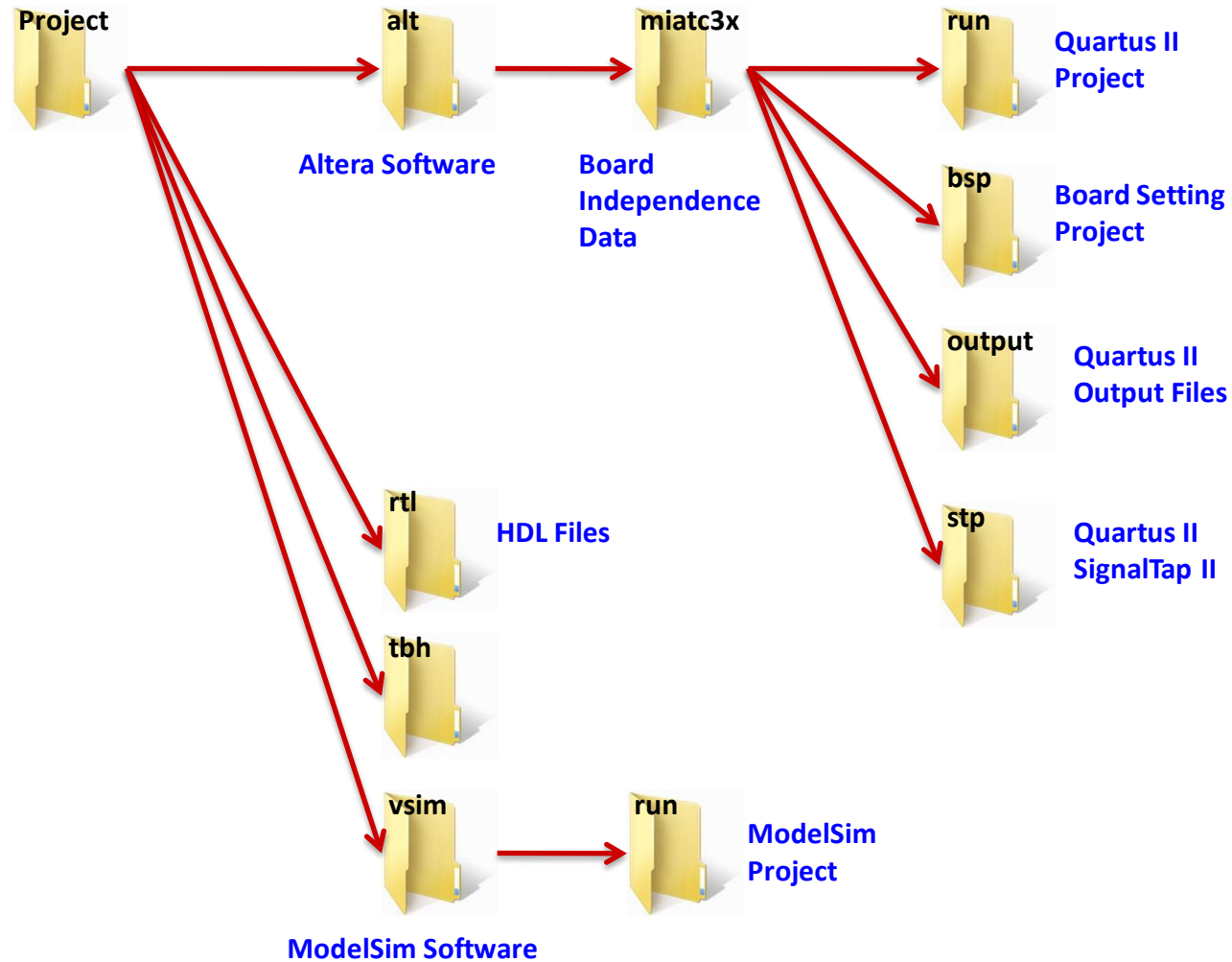
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Part – IV

# APPENDIX

# Project Architecture



## QuartusII Project Setting

## New Project Wizard

### Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

**Device family**

Family: Cyclone III

Devices: All

**Target device**

☐ Auto device selected by the Filter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

**Show in 'Available devices' list**

Package: FBGA

Pin count: 256

Speed grade: 8

☒ Show advanced devices

☐ HardCopy compatible only

**Available devices:**

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit
EP3C5F256C8	1.2V	5136	183	423936	46
EP3C10F256C8	1.2V	10320	183	423936	46
EP3C16F256C8	1.2V	15408	169	516096	112
EP3C25F256C8	1.2V	24624	157	608256	132

**Companion device**

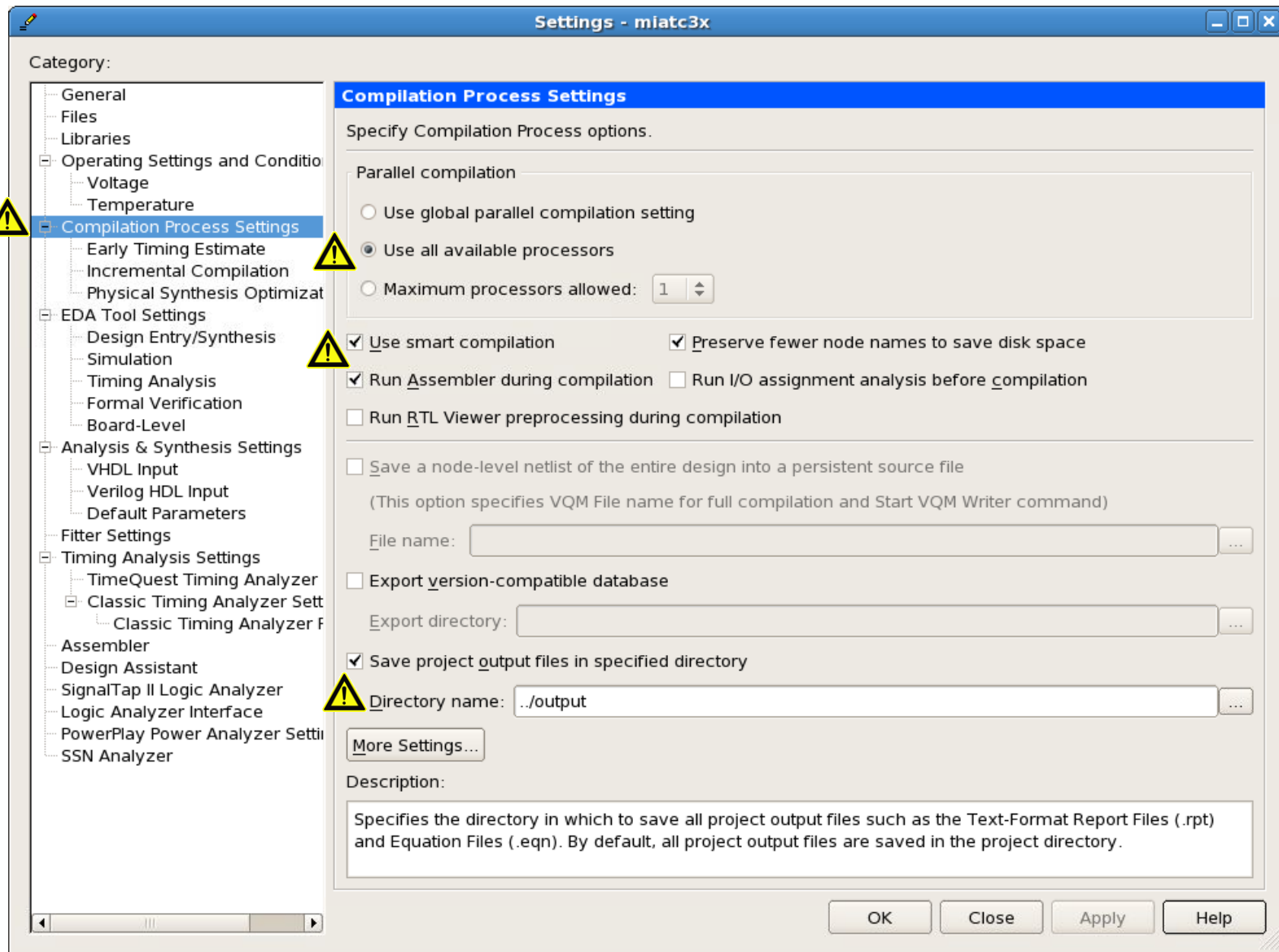
HardCopy:  

☐ Limit DSP & RAM to HardCopy device resources

< Back
Next >
Finish
Cancel



# QuartusII Project Setting, Cont.



**Settings - miatc3x**

Category:

- General
- Files
- Libraries
- Operating Settings and Conditions
  - Voltage
  - Temperature
- Compilation Process Settings**
  - Early Timing Estimate
  - Incremental Compilation
  - Physical Synthesis Optimization
- EDA Tool Settings
  - Design Entry/Synthesis
  - Simulation
  - Timing Analysis
  - Formal Verification
  - Board-Level
- Analysis & Synthesis Settings
  - VHDL Input
  - Verilog HDL Input
  - Default Parameters
- Fitter Settings
- Timing Analysis Settings
  - TimeQuest Timing Analyzer
  - Classic Timing Analyzer Settings
    - Classic Timing Analyzer Settings
- Assembler
- Design Assistant
- SignalTap II Logic Analyzer
- Logic Analyzer Interface
- PowerPlay Power Analyzer Settings
- SSN Analyzer

**Compilation Process Settings**

Specify Compilation Process options.

Parallel compilation

☐ Use global parallel compilation setting

☒ Use all available processors

☐ Maximum processors allowed:

☒ Use smart compilation ☒ Preserve fewer node names to save disk space

☒ Run Assembler during compilation ☐ Run I/O assignment analysis before compilation

☐ Run RTL Viewer preprocessing during compilation

☐ Save a node-level netlist of the entire design into a persistent source file

(This option specifies VQM File name for full compilation and Start VQM Writer command)

File name:

☐ Export version-compatible database

Export directory:

☒ Save project output files in specified directory

☒ Directory name:

[More Settings...](#)

Description:

Specifies the directory in which to save all project output files such as the Text-Format Report Files (.rpt) and Equation Files (.eqn). By default, all project output files are saved in the project directory.

OK Close Apply Help

# QuartusII Project Setting, Cont.

Category:

- General
- Files
- Libraries
- Operating Settings and Condition
  - Voltage
  - Temperature
- Compilation Process Settings
  - Early Timing Estimate
  - Incremental Compilation
  - Physical Synthesis Optimizat
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  - Timing Analysis
  - Formal Verification
  - Board-Level
- Analysis & Synthesis Settings
  - VHDL Input
  - Verilog HDL Input
  - Default Parameters
- Fitter Settings
- Timing Analysis Settings
  - TimeQuest Timing Analyzer
  - Classic Timing Analyzer Sett
    - Classic Timing Analyzer f
- Assembler
- Design Assistant
- SignalTap II Logic Analyzer
- Logic Analyzer Interface
- PowerPlay Power Analyzer Setti
- SSN Analyzer

Timing Analysis Settings

Specify whether to use the TimeQuest Timing Analyzer or the Classic Timing Analyzer as the default timing analysis tool. The TimeQuest Timing Analyzer requires a Synopsys Design Constraints File containing timing constraints or exceptions.

Timing analysis processing

☐ Use TimeQuest Timing Analyzer during compilation
☒ Use Classic Timing Analyzer during compilation

(The Classic Timing Analyzer will not be available in a future release of the Quartus II software. Use the TimeQuest Timing Analyzer to run timing analysis on your design. Convert all the project settings and the timing constraints to TimeQuest Timing Analyzer equivalents.)

Description:

Specifies whether you want to use the TimeQuest Timing Analyzer or the Classic Timing Analyzer as the default timing analysis tool. The TimeQuest analyzer requires a Synopsys Design Constraints File (SDC) containing timing constraints or exceptions.

OK

Close

Apply

Help