HDL Name	Pin Mapping	Description	STM32F103	IOB
c3x_clock50m	E16	miatc3x onboard		
c3x_dipsw0	E1	miatc3x onboard		
c3x_gpio_b1[0]	C2	miatc3x-JP1 1.C2	PA9	19. UART1_TX
c3x_gpio_b1[1]	D1	miatc3x-JP1 2.D1	PG10	
c3x_gpio_b1[2]	F2	miatc3x-JP1 3.F2	PD4	
c3x_gpio_b1[3]	F1	miatc3x-JP1 4.F1	PD5	
c3x_gpio_b1[4]	G2	miatc3x-JP1 5.G2	PE0	
c3x_gpio_b1[5]	G1	miatc3x-JP1 6.G1	PE1	
c3x_gpio_b1[6]	G5	miatc3x-JP1 7.G5	PD14	
c3x_gpio_b1[7]	B1	miatc3x-JP1 8.B1	PD15	
c3x_gpio_b1[8]	F3	miatc3x-JP1 9.F3	PD0	
c3x_gpio_b1[9]	J2	miatc3x-JP1 10.J2	PD1	
c3x_gpio_b1[10]	J1	miatc3x-JP1 13.J1	PE7	
c3x_gpio_b1[11]	K2	miatc3x-JP1 14.K2	PE8	
c3x_gpio_b1[12]	K1	miatc3x-JP1 15.K1	PE9	
c3x_gpio_b1[13]	L2	miatc3x-JP1 16.L2	PE10	
c3x_gpio_b1[14]	L1	miatc3x-JP1 17.L1	PE11	
c3x_gpio_b1[15]	N2	miatc3x-JP1 18.N2	PE12	
c3x_gpio_b1[16]	N1	miatc3x-JP1 19.N1	PE13	
c3x_gpio_b1[17]	P2	miatc3x-JP1 20.P2	PE14	
c3x_gpio_b1[18]	P1	miatc3x-JP1 21.P1	PE15	
c3x_gpio_b1[19]	K5	miatc3x-JP1 22.K5	PD8	
c3x_gpio_b1[20]	L4	miatc3x-JP1 23.L4	PD9	
c3x_gpio_b1[21]	R1	miatc3x-JP1 24.R1	PD10	
c3x_gpio_b1[22]	L3	miatc3x-JP1 25.L3	PF0	
c3x_gpio_b1[23]	N9	miatc3x-JP1 26.N9	PF1	
c3x_gpio_b1[24]	R10	miatc3x-JP1 27.R10	PF2	
c3x_gpio_b1[25]	T10	miatc3x-JP1 28.T10	PF3	
c3x_gpio_b1[26]	R11	miatc3x-JP1 31.R11	PF4	
c3x_gpio_b1[27]	P9	miatc3x-JP1 32.P9	PF5	
c3x_gpio_b1[28]	M10	miatc3x-JP1 33.M10	PF12	
c3x_gpio_b1[29]	N11	miatc3x-JP1 34.N11	PF13	
c3x_gpio_b1[30]	P11	miatc3x-JP1 35.P11	PF14	
c3x_gpio_b1[31]	N12	miatc3x-JP1 36.N12	PF15	
c3x_gpio_b1[32]	F14	miatc3x-JP1 37.F14	PG0	
c3x_gpio_b1[33]	A6	miatc3x-JP1 38.A6	PG1	