HDL Name	Pin Mapping	Description
c3x_clock50m	E16	miatc3x onboard
c3x_clock24m		miatc3x onboard
c3x_dipsw0	E1	miatc3x onboard
c3x_dipsw1	E2	miatc3x onboard
c3x_dipsw2		miatc3x onboard
c3x_dipsw3		miatc3x onboard
c3x_gpio_b1[0]	C2	miatc3x-JP1 1.C2
c3x_gpio_b1[1]	D1	miatc3x-JP1 2.D1
c3x_gpio_b1[2]	F2	miatc3x-JP1 3.F2
c3x_gpio_b1[3]	F1	miatc3x-JP1 4.F1
c3x_gpio_b1[4]	G2	miatc3x-JP1 5.G2
c3x_gpio_b1[5]	G1	miatc3x-JP1 6.G1
c3x_gpio_b1[6]	G5	miatc3x-JP1 7.G5
c3x_gpio_b1[7]	B1	miatc3x-JP1 8.B1
c3x_gpio_b1[8]	F3	miatc3x-JP1 9.F3
c3x_gpio_b1[9]	J2	miatc3x-JP1 10.J2
c3x_gpio_b1[10]	J1	miatc3x-JP1 13.J1
c3x_gpio_b1[11]	K2	miatc3x-JP1 14.K2
c3x_gpio_b1[12]	K1	miatc3x-JP1 15.K1
c3x_gpio_b1[13]	L2	miatc3x-JP1 16.L2
c3x_gpio_b1[14]	L1	miatc3x-JP1 17.L1
c3x_gpio_b1[15]	N2	miatc3x-JP1 18.N2
c3x_gpio_b1[16]	N1	miatc3x-JP1 19.N1
c3x_gpio_b1[17]	P2	miatc3x-JP1 20.P2
c3x_gpio_b1[18]	P1	miatc3x-JP1 21.P1
c3x_gpio_b1[19]	K5	miatc3x-JP1 22.K5
c3x_gpio_b1[20]	L4	miatc3x-JP1 23.L4
c3x_gpio_b1[21]	R1	miatc3x-JP1 24.R1
c3x_gpio_b1[22]	L3	miatc3x-JP1 25.L3
c3x_gpio_b1[23]	N9	miatc3x-JP1 26.N9
c3x_gpio_b1[24]	R10	miatc3x-JP1 27.R10
c3x_gpio_b1[25]	T10	miatc3x-JP1 28.T10
c3x_gpio_b1[26]	R11	miatc3x-JP1 31.R11
c3x_gpio_b1[27]	P9	miatc3x-JP1 32.P9
c3x_gpio_b1[28]	M10	miatc3x-JP1 33.M10
c3x_gpio_b1[29]	N11	miatc3x-JP1 34.N11
c3x_gpio_b1[30]	P11	miatc3x-JP1 35.P11
c3x_gpio_b1[31]	N12	miatc3x-JP1 36.N12
c3x_gpio_b1[32]	F14	miatc3x-JP1 37.F14
c3x_gpio_b1[33]	A6	miatc3x-JP1 38.A6