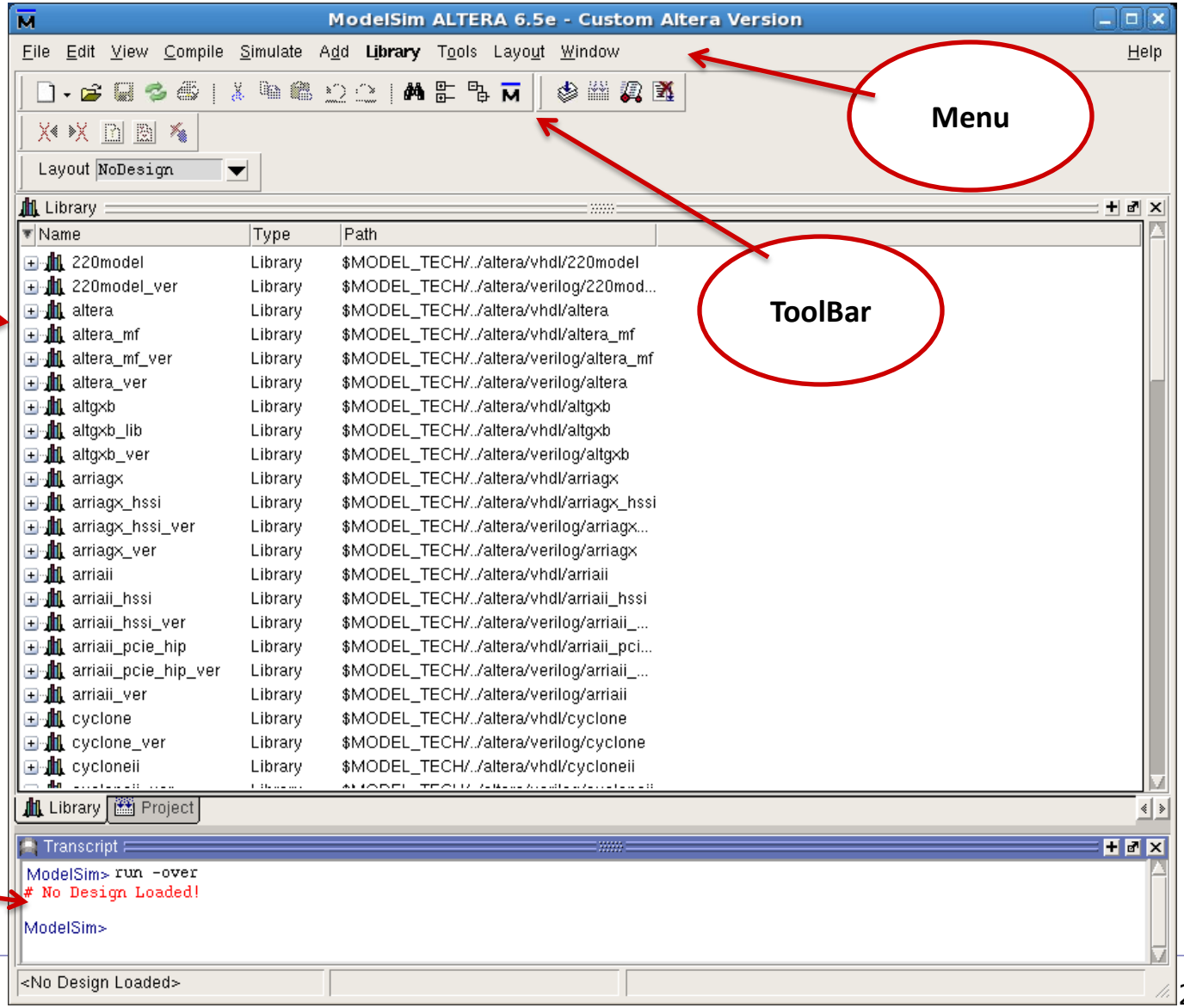
Simple
ModelSim Starter Guide

MIAT-C3X FPGA Development Board

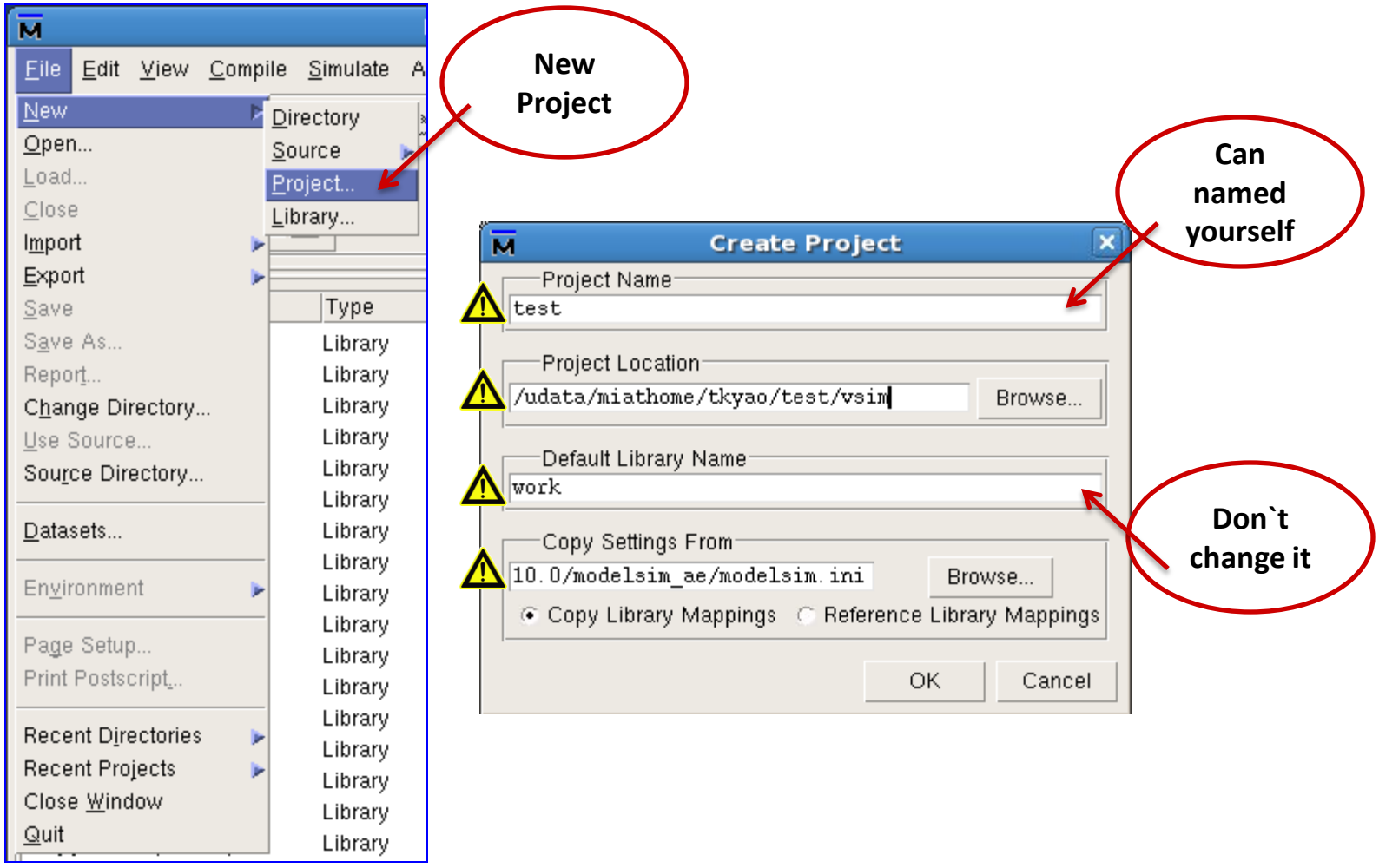
浯陽科技有限公司

CSIE MIAT Lab.
National Central University

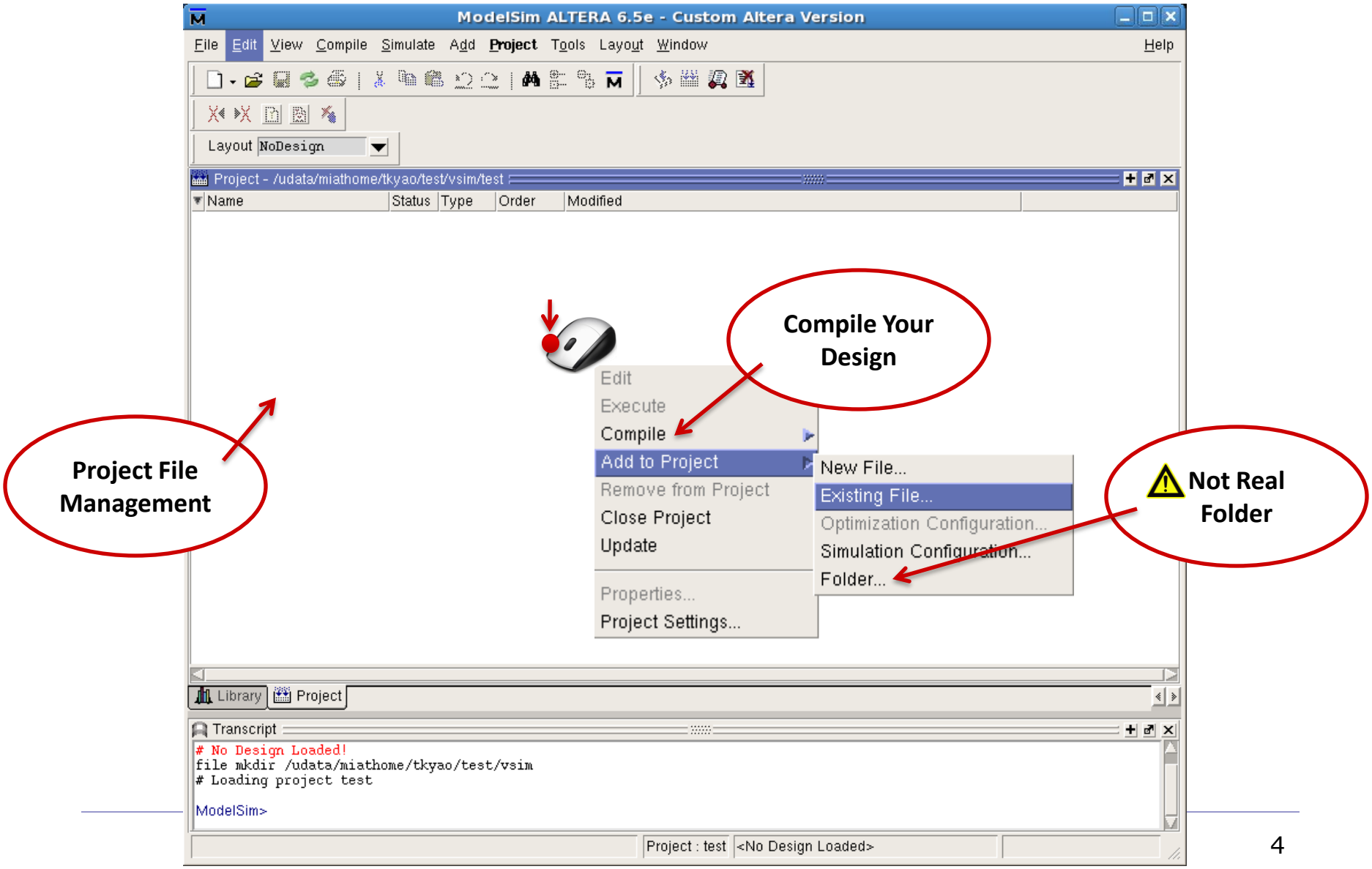
Main Windows



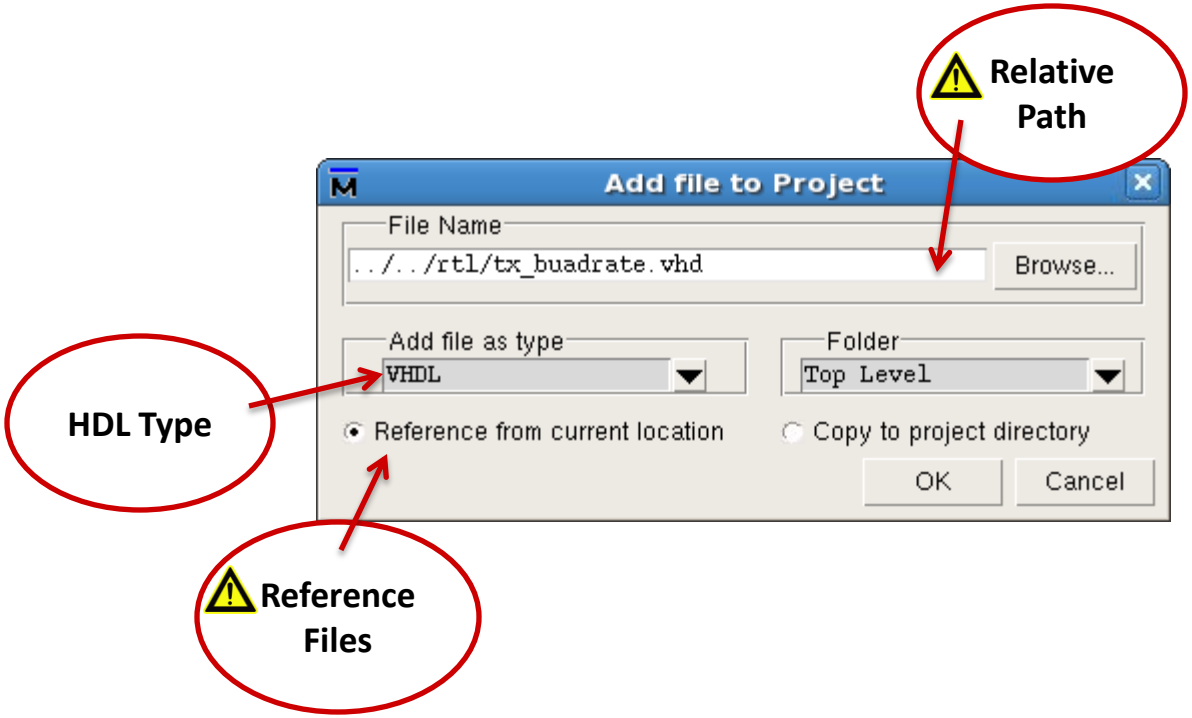
New Project


File
Edit
View
Compile
Simulate
New
Open...
Load...
Close
Import
Export
Save
Save As...
Report...
Change Directory...
Use Source...
Source Directory...
Datasets...
Environment
Page Setup...
Print Postscript...
Recent Directories
Recent Projects
Close Window
Quit
Directory
Source
Project...
Library...
Type
Library
New Project
Create Project
Project Name
test
Project Location
/udata/miathome/tkyao/test/vsim
Browse...
Default Library Name
work
Copy Settings From
10.0/modelsim_ae/modelsim.ini
Browse...
Copy Library Mappings
Reference Library Mappings
OK
Cancel
Can named yourself
Don`t change it

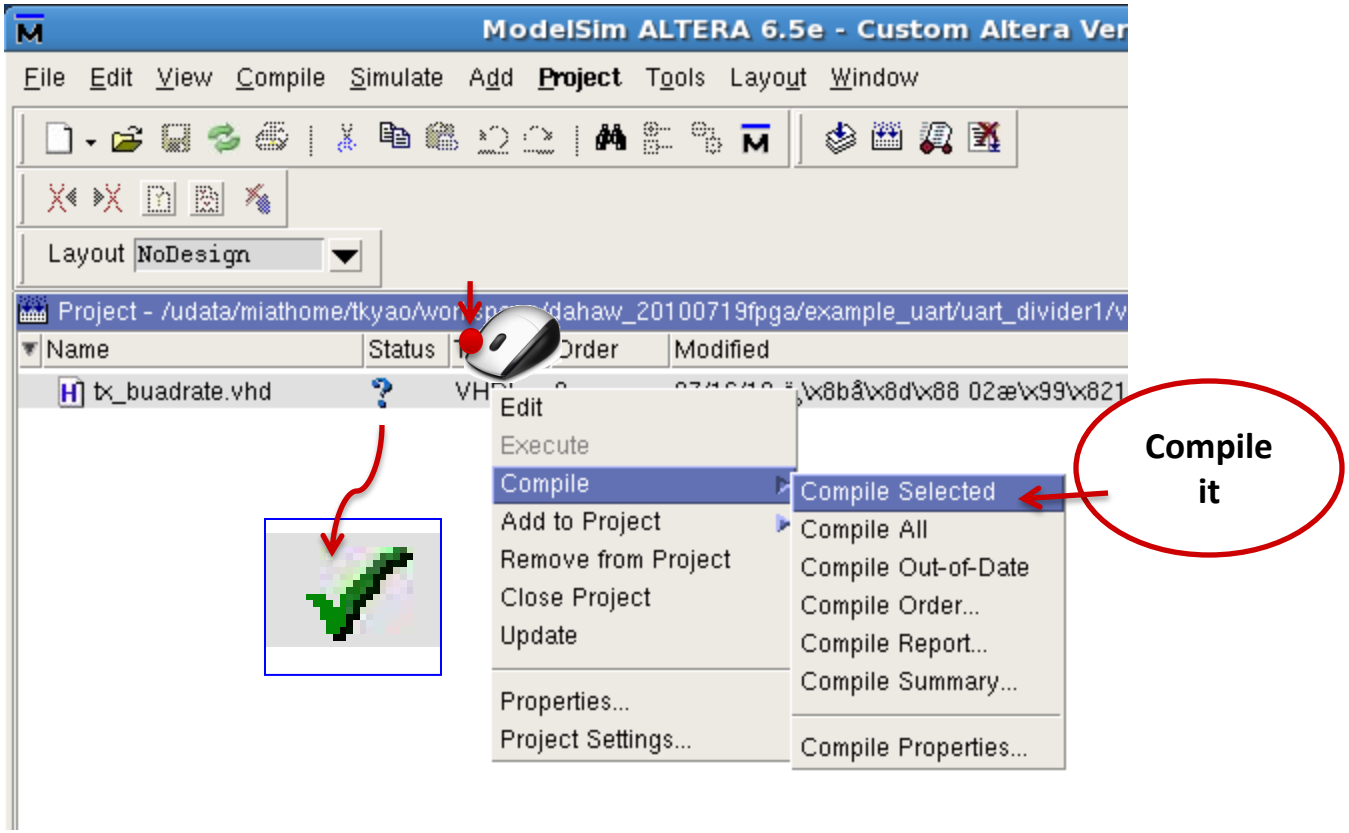
New Project, Cont. 1



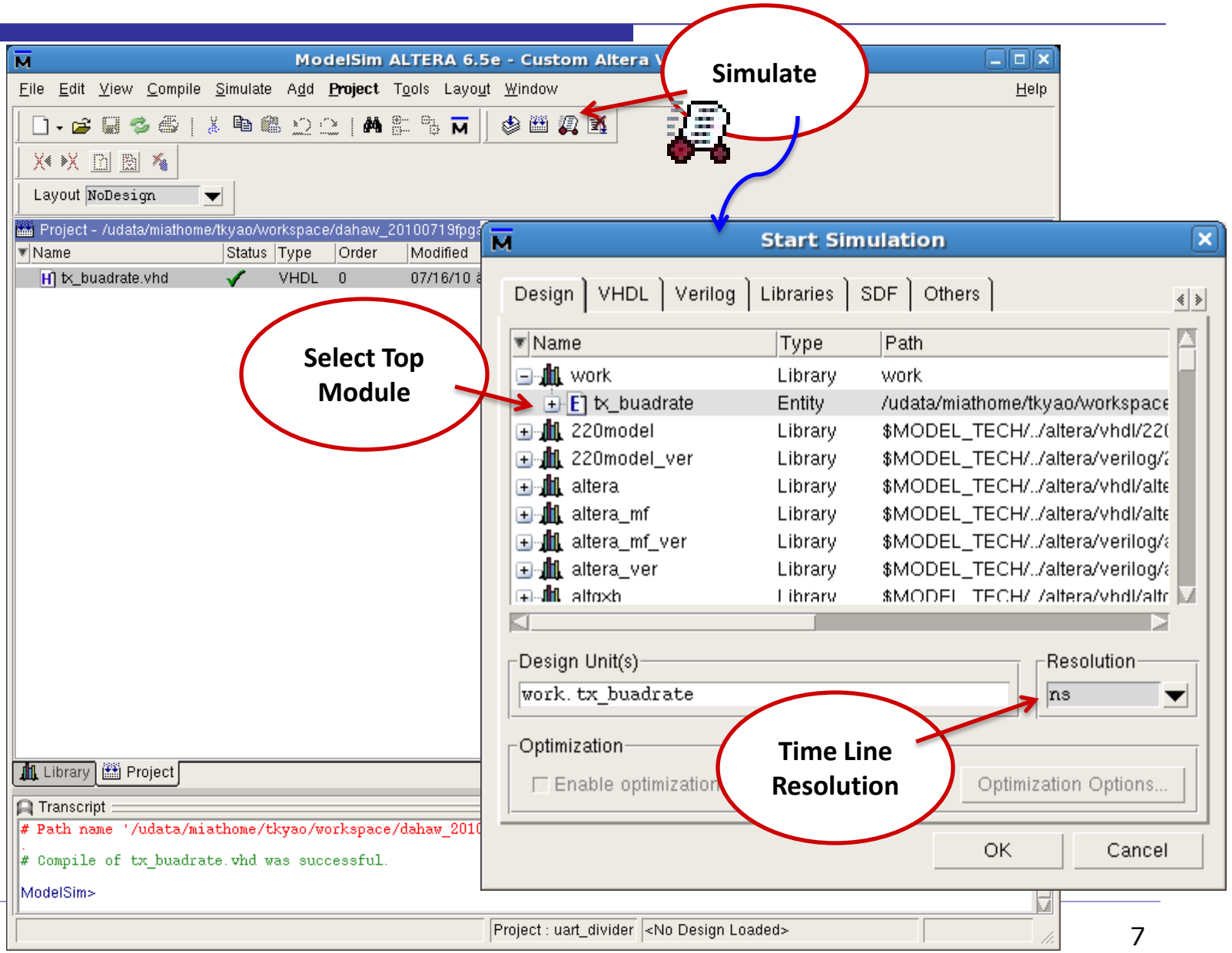
New Project, Cont. 2



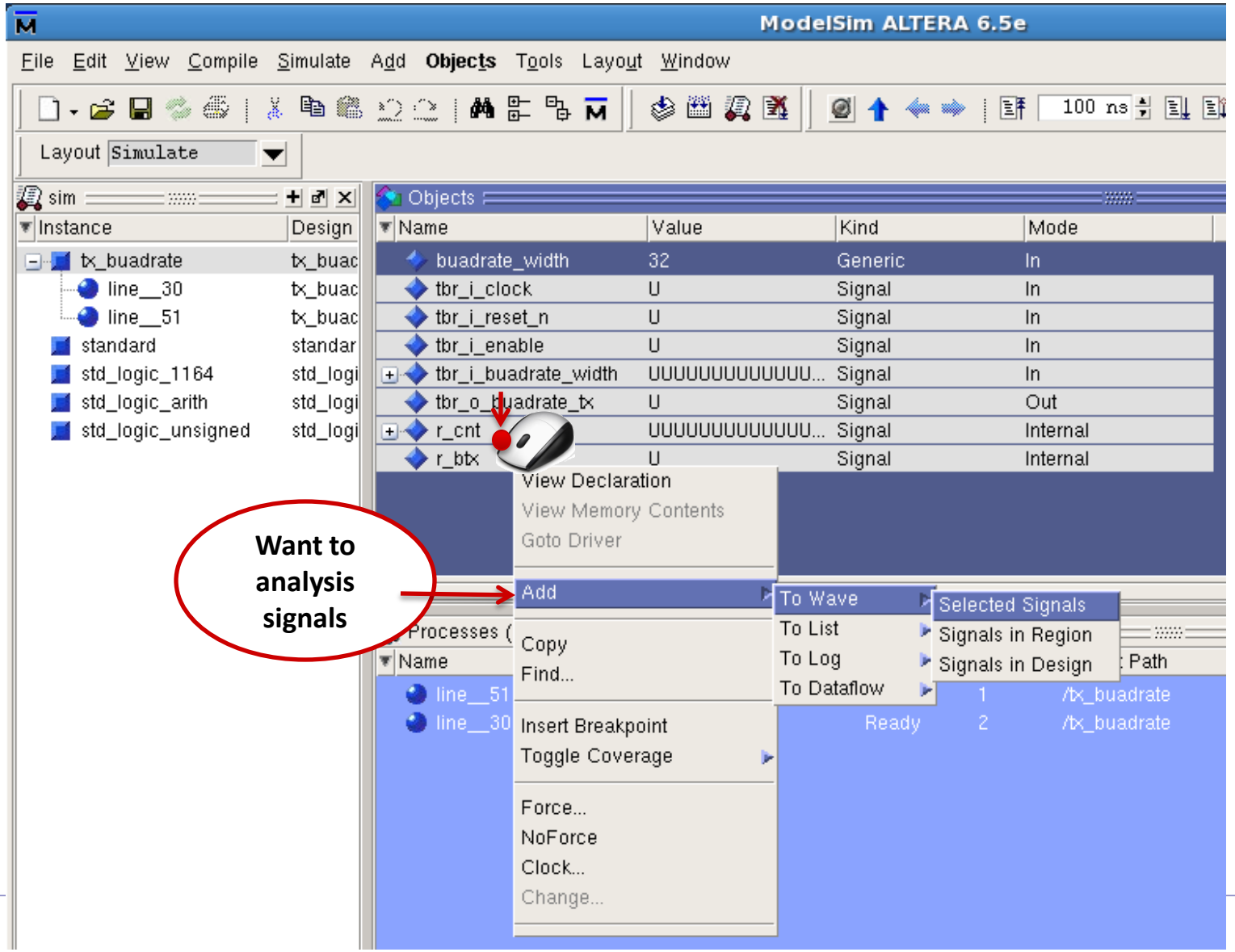
New Project, Cont. 2



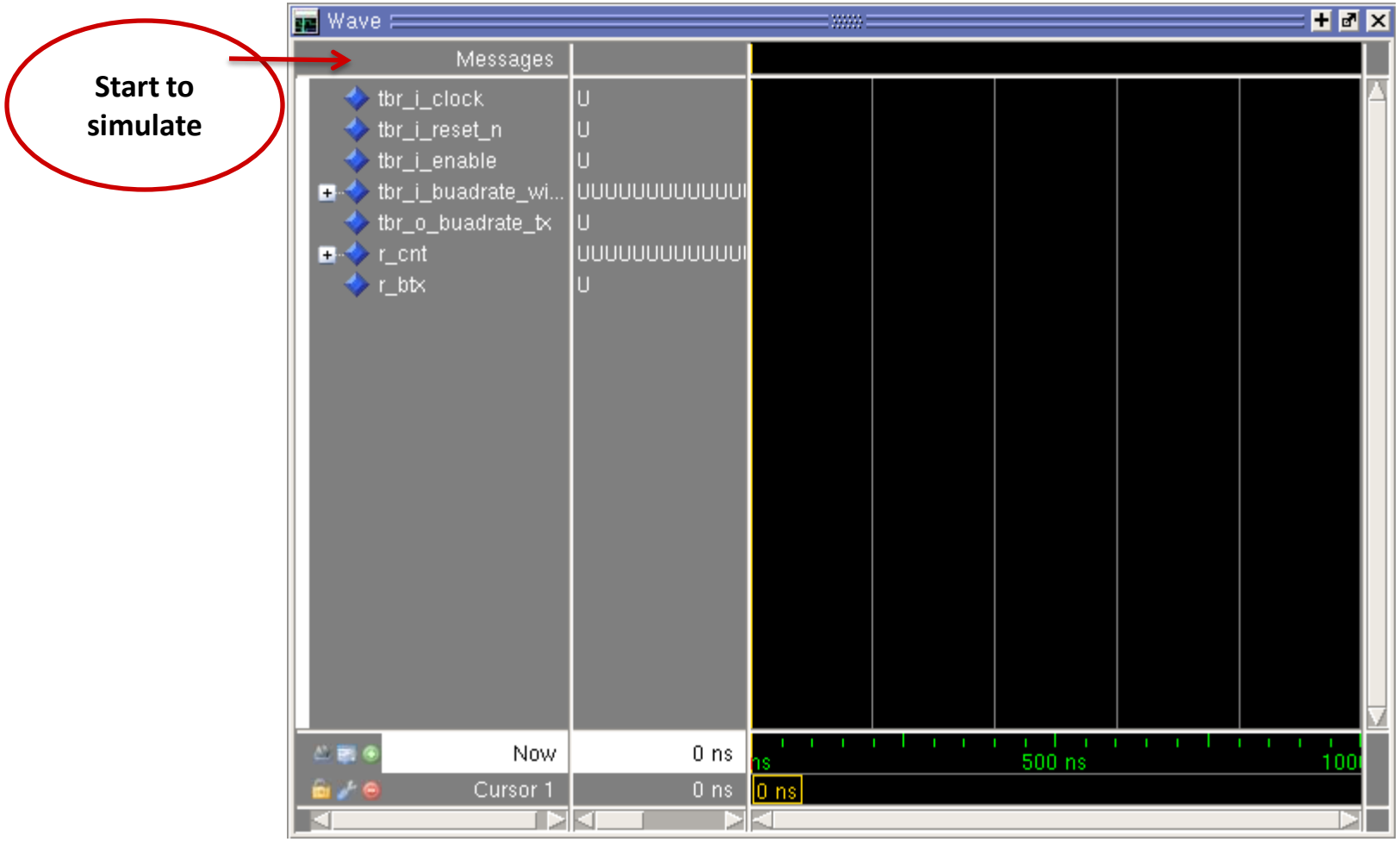
Simulation


Simulate
ModelSim ALTERA 6.5e - Custom Altera V
File Edit View Compile Simulate Add Project Tools Layout Window Help
Layout NoDesign
Project - /udata/miathome/tkyao/workspace/dahaw_20100719fpga
Name Status Type Order Modified
tx_buadrate.vhd VHDL 0 07/16/10
Start Simulation
Design VHDL Verilog Libraries SDF Others
Name Type Path
work Library work
tx_buadrate Entity /udata/miathome/tkyao/workspace
220model Library $MODEL_TECH/../altera/vhdl/220
220model_ver Library $MODEL_TECH/../altera/verilog/
altera Library $MODEL_TECH/../altera/vhdl/alte
altera_mf Library $MODEL_TECH/../altera/vhdl/alte
altera_mf_ver Library $MODEL_TECH/../altera/verilog/
altera_ver Library $MODEL_TECH/../altera/verilog/
Select Top Module
Design Unit(s)
work. tx_buadrate
Resolution
ns
Optimization
Enable optimization
Optimization Options...
Time Line Resolution
OK
Cancel
Library Project
Transcript
Path name '/udata/miathome/tkyao/workspace/dahaw_2010
Compile of tx_buadrate.vhd was successful.
ModelSim>
Project : uart_divider
<No Design Loaded>

Simulation, Cont. 1



Simulation, Cont. 2



Note