MIAT-C3X-EVB

軟硬體實驗模組與開發流程介紹

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Platform	■ MIAT_C3X ■ MIAT_IOB
Peripheral	Key Switch, LED
Author	■ WU-YANG Technology Co., Ltd.

Outline

- MIAT_C3X實驗板
  - 主要功能介紹
  - 硬體環境設定
- MIAT_IOB實驗板
  - 各個週邊模組功能介紹
- 開發流程介紹
  - 以基本I/O驅動為例
  - 硬體電路配置
  - Quartus II軟體基本使用方法介紹
- 開發流程練習

MIAT_C3X實驗板主要功能介紹

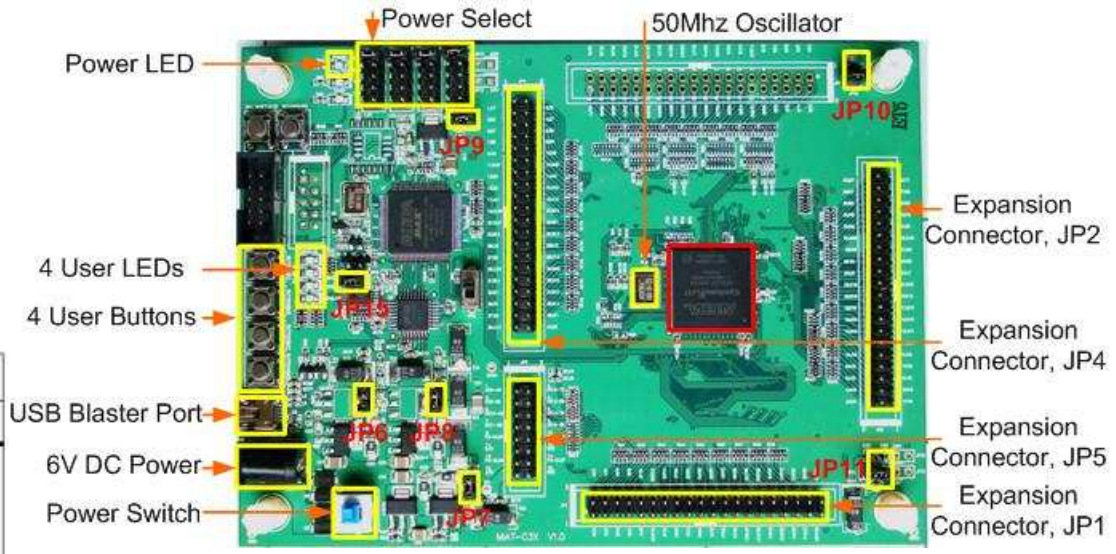
- FPGA編號Altera Cyclone III EP3C25
  - 24,624 Logic Elements
  - 594(66x9) Kbits Memory
  - 66 Multipliers
  - 4 PLLs
  - 20 Global Clock Networks
  - 156 I/O Pin Counts

Table 1–6. Cyclone III FPGA I/O Standards Support *Note (1)*

Type	I/O Standard
Single-Ended I/O	• LVTTL • LVCMOS • SSTL • HSTL • PCI • PCI-X
Differential I/O	• SSTL • HSTL • LVPECL • BLVDS • LVDS • mini-LVDS • RSDS • PPDS

Note to Table 1–6:
(1) PCI Express and Serial Rapid I/O can be supported using an external PHY device.

  - Support Memory Types
    - DDR, DDR2, SDRAM
    - Data Rates up to 400 Mbps
  - FBGA 256



MIAT_C3X正面

MIAT_C3X實驗板主要功能介紹

- FPGA內部可合成記憶體之規格

Table 4–1. Summary of M9K Memory Features (Part 1 of 2)

Feature	M9K Blocks
Maximum performance	315 MHz
Total RAM bits (including parity bits)	9,216
Configurations (depth × width)	8192 × 1 4096 × 2 2048 × 4 1024 × 8 1024 × 9 512 × 16 512 × 18 256 × 32 256 × 36
Parity bits	✓
Byte enable	✓
Packed mode	✓
Address clock enable	✓
Single-port mode	✓
Simple dual-port mode	✓
True dual-port mode	✓

MIAT_C3X實驗板主要功能介紹

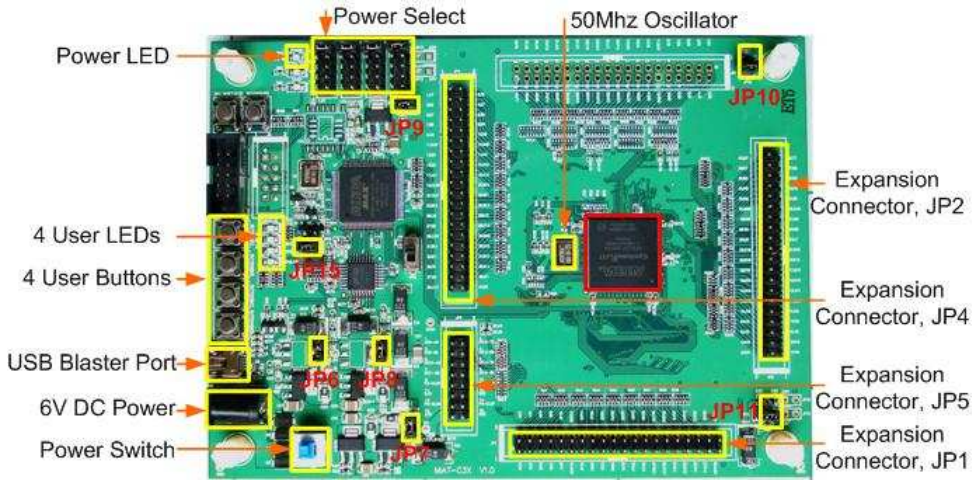
- FPGA內部可合成記憶體之規格

Table 4–1. Summary of M9K Memory Features (Part 2 of 2)

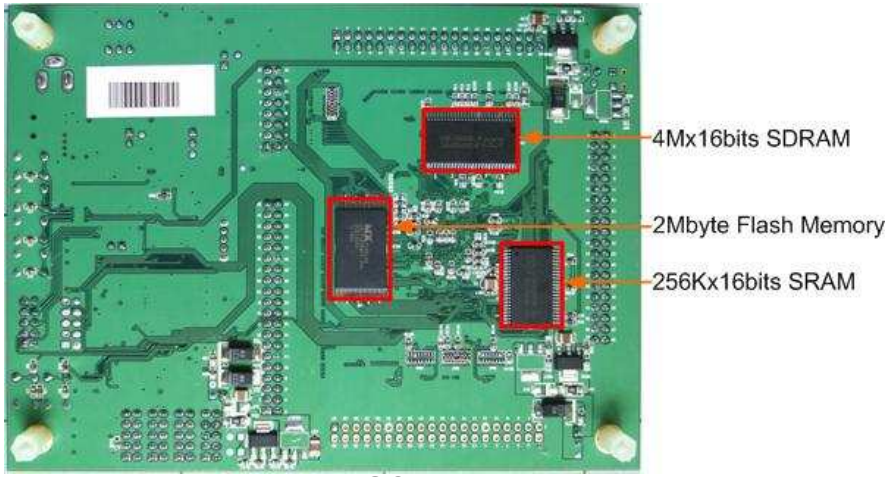
Feature	M9K Blocks
Embedded shift register mode *(1)*	✓
ROM mode	✓
FIFO buffer *(1)*	✓
Simple dual-port mixed width support	✓
True dual-port mixed width support *(2)*	✓
Memory initialization file (**.mif**)	✓
Mixed-clock mode	✓
Power-up condition	Outputs cleared
Register asynchronous clears	Read address registers and output registers only
Latch asynchronous clears	Output latches only
Write/Read operation triggering	Write and Read: Rising clock edges
Same-port read-during-write	Outputs set to “Old Data” or “New Data”
Mixed-port read-during-write	Outputs set to “Old Data” or “Don’t Care”

MIAT_C3X實驗板主要功能介紹

- 50Mhz Oscillator
- 可由USB介面燒錄電路
- 4個使用者測試 LED
- 4個使用者測試按鈕開關
- 核心晶片之I/O接腳以2.54mm間距的2x20PIN排針連接，可彈性擴充週邊。
- I/O接腳邏輯電位可調(1.2V, 1.8V, 2.5V, 2.8V, 3.3V)。
- 外部記憶體
  - 4Mx16bits SDRAM
  - 2Mbyte Flash Memory
  - 256Kx16bits SRAM
- 電源DC6V
- 尺寸：150x110mm



MIAT_C3X正面

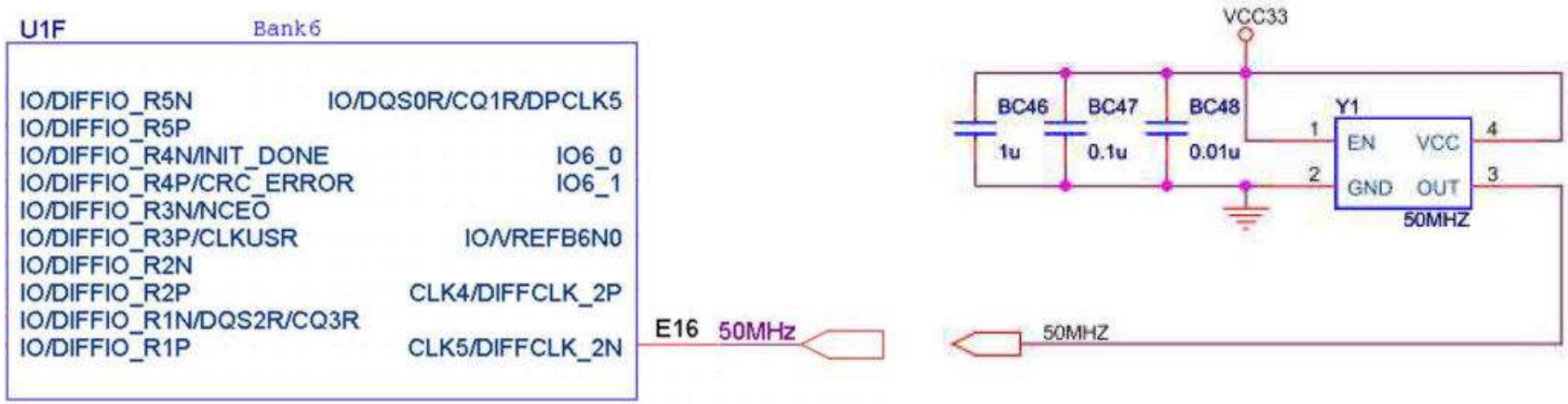


MIAT_C3X反面

MIAT_C3X實驗板主要功能介紹

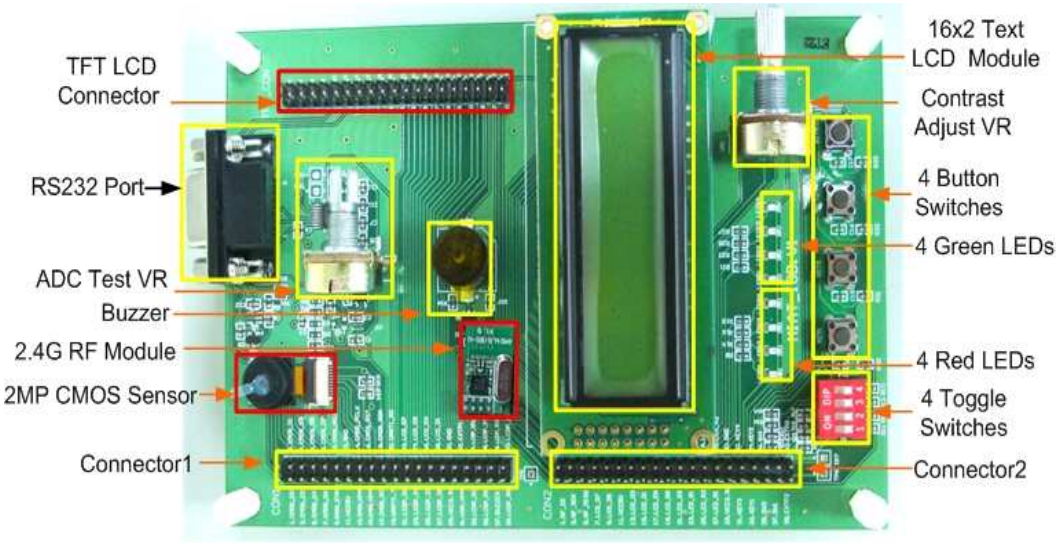
石英晶體振盪器

Signal Name	FPGA Pin Name	Bank No.
50MHz	E16	B6



MIAT_IOB實驗週邊功能介紹

- 2MPixels CMOS Sensor模組
- 2.4G RF模組
- 2x16文字型LCD模組
  (含明暗度調整電阻)
- RS232介面
- AD轉換測試模組
- 蜂鳴器
- 4個紅色LED
- 4個綠色LED
- 4個按鈕開關
- 4 P指撥開關
- TFT LCD 2.54mm連接器
- 尺寸：145x103mm



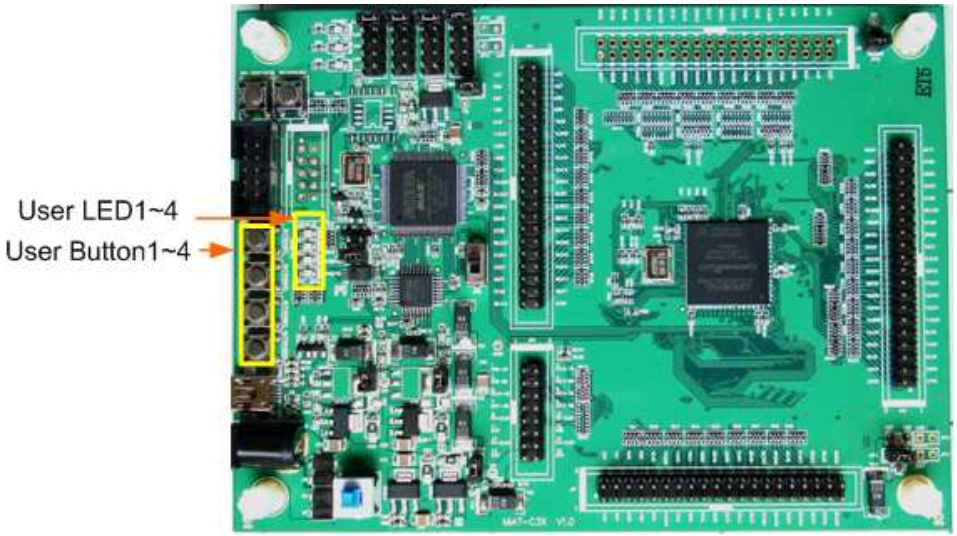
開發流程介紹－以基本I/O驅動為例

- 實驗目的

  學習如何連接與操作簡單的輸入與輸出的元件到FPGA 晶片，其中輸入元件為MIAT_C3X實驗板上的開關Button1~4，輸出元件為LED1~4。

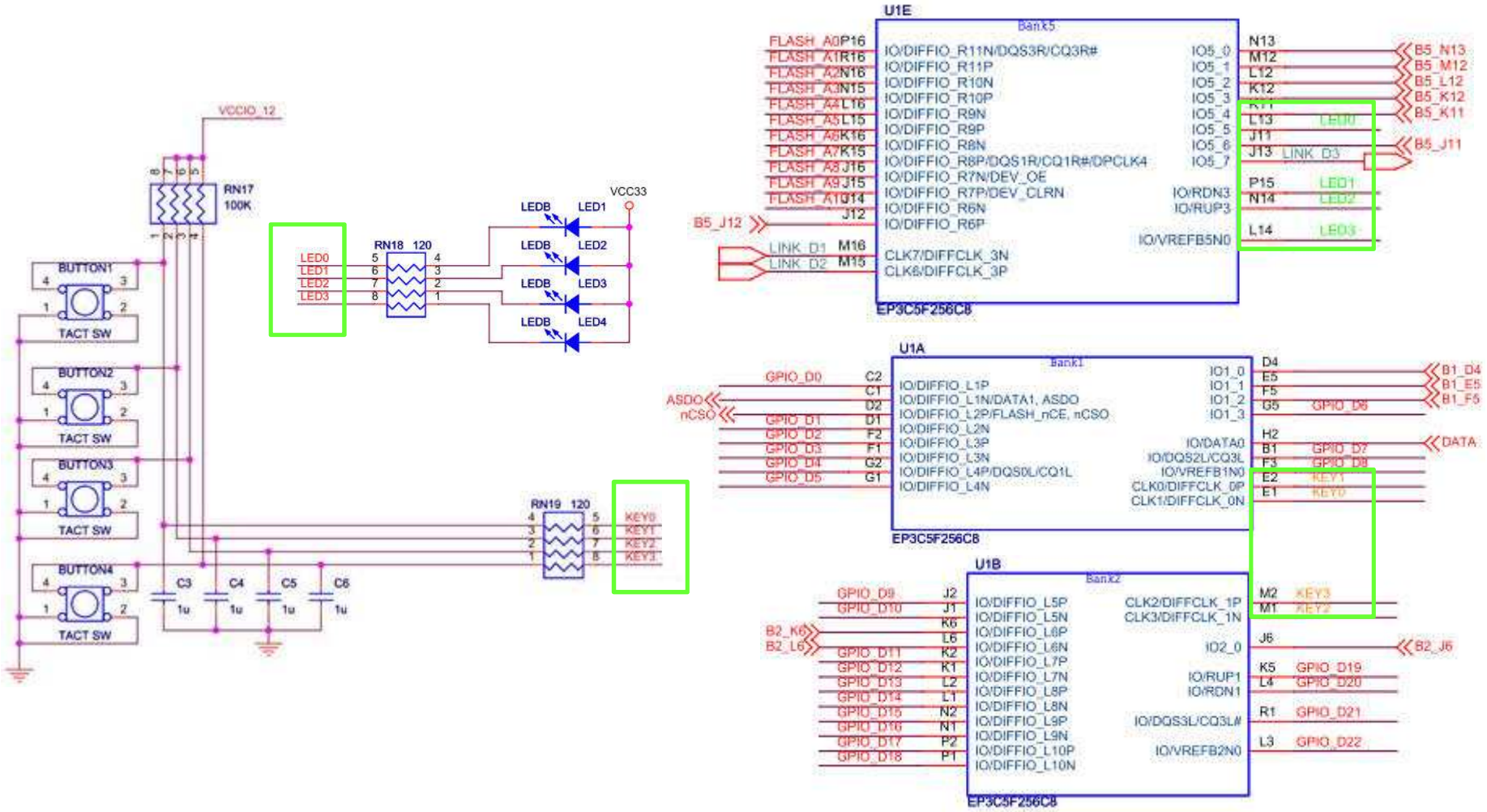
- 實驗原理

  範例一、根據開關、LED 電路圖與FPGA 腳位對照表使用提示的VHDL 程式碼將開關與LED 做連接的動作，當開關Button按下時相對應的LED被點亮，反之LED熄滅。



FPGA Pin Name	I/O assignment
PIN_E1	User Botton1
PIN_E2	User Botton2
PIN_M1	User Botton3
PIN_M2	User Botton4
PIN_L13	User LED1
PIN_P15	User LED2
PIN_N14	User LED3
PIN_L14	User LED4

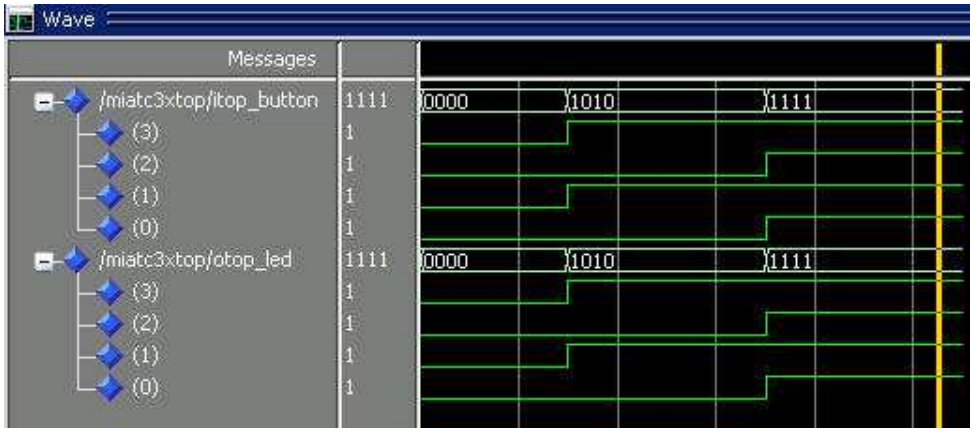
基本I/O驅動範例


U1E
Bank5
FLASH_A0 P16
FLASH_A1 R16
FLASH_A2 N16
FLASH_A3 N15
FLASH_A4 L16
FLASH_A5 L15
FLASH_A6 K16
FLASH_A7 K15
FLASH_A8 J16
FLASH_A9 J15
FLASH_A10 J14
B5_J12
J12
IO/DIFFIO_R11N/DQS3R/CQ3R#
IO/DIFFIO_R11P
IO/DIFFIO_R10N
IO/DIFFIO_R10P
IO/DIFFIO_R9N
IO/DIFFIO_R9P
IO/DIFFIO_R8N
IO/DIFFIO_R8P/DQS1R/CQ1R#/DPCLK4
IO/DIFFIO_R7N/DEV_OE
IO/DIFFIO_R7P/DEV_CLRN
IO/DIFFIO_R6N
IO/DIFFIO_R6P
LINK_D1 M16
LINK_D2 M15
CLK7/DIFFCLK_3N
CLK6/DIFFCLK_3P
IO/VREFB5N0
IO/RDN3
IO/RUP3
IO5_0 N13
IO5_1 M12
IO5_2 L12
IO5_3 K12
IO5_4 L13
IO5_5 J11
IO5_6 J13
IO5_7
B5_N13
B5_M12
B5_L12
B5_K12
B5_K11
B5_J11
LED0
LINK_D3
P15 LED1
N14 LED2
L14 LED3
EP3C5F256C8
U1A
Bank1
GPIO_D0 C2
ASDO C1
nCSO D2
GPIO_D1 D1
GPIO_D2 F2
GPIO_D3 F1
GPIO_D4 G2
GPIO_D5 G1
IO/DIFFIO_L1P
IO/DIFFIO_L1N/DATA1, ASDO
IO/DIFFIO_L2P/FLASH_nCE, nCSO
IO/DIFFIO_L2N
IO/DIFFIO_L3P
IO/DIFFIO_L3N
IO/DIFFIO_L4P/DQS0L/CQ1L
IO/DIFFIO_L4N
IO/DATA0
IO/DQS2L/CQ3L
IO/VREFB1N0
CLK0/DIFFCLK_0P
CLK1/DIFFCLK_0N
IO1_0 D4
IO1_1 E5
IO1_2 F5
IO1_3 G5
H2
B1
F3
E2
E1
B1_D4
B1_E5
B1_F5
GPIO_D6
GPIO_D7
GPIO_D8
KEY1
KEY0
DATA
EP3C5F256C8
U1B
Bank2
GPIO_D9 J2
GPIO_D10 J1
K6
L6
GPIO_D11 K2
GPIO_D12 K1
GPIO_D13 L2
GPIO_D14 L1
GPIO_D15 N2
GPIO_D16 N1
GPIO_D17 P2
GPIO_D18 P1
B2_K6
B2_L6
IO/DIFFIO_L5P
IO/DIFFIO_L5N
IO/DIFFIO_L6P
IO/DIFFIO_L6N
IO/DIFFIO_L7P
IO/DIFFIO_L7N
IO/DIFFIO_L8P
IO/DIFFIO_L8N
IO/DIFFIO_L9P
IO/DIFFIO_L9N
IO/DIFFIO_L10P
IO/DIFFIO_L10N
CLK2/DIFFCLK_1P
CLK3/DIFFCLK_1N
IO2_0
IO/RUP1
IO/RDN1
IO/DQS3L/CQ3L#
IO/VREFB2N0
M2 KEY3
M1 KEY2
J6
K5 GPIO_D19
L4 GPIO_D20
R1 GPIO_D21
L3 GPIO_D22
B2_J6
EP3C5F256C8
VCCIO_12
RN17
100K
BUTTON1
BUTTON2
BUTTON3
BUTTON4
TACT SW
C3 1u
C4 1u
C5 1u
C6 1u
LED0
LED1
LED2
LED3
RN18 120
VCC33
LEDB LED1
LEDB LED2
LEDB LED3
LEDB LED4
RN19 120
KEY0
KEY1
KEY2
KEY3

基本I/O驅動範例

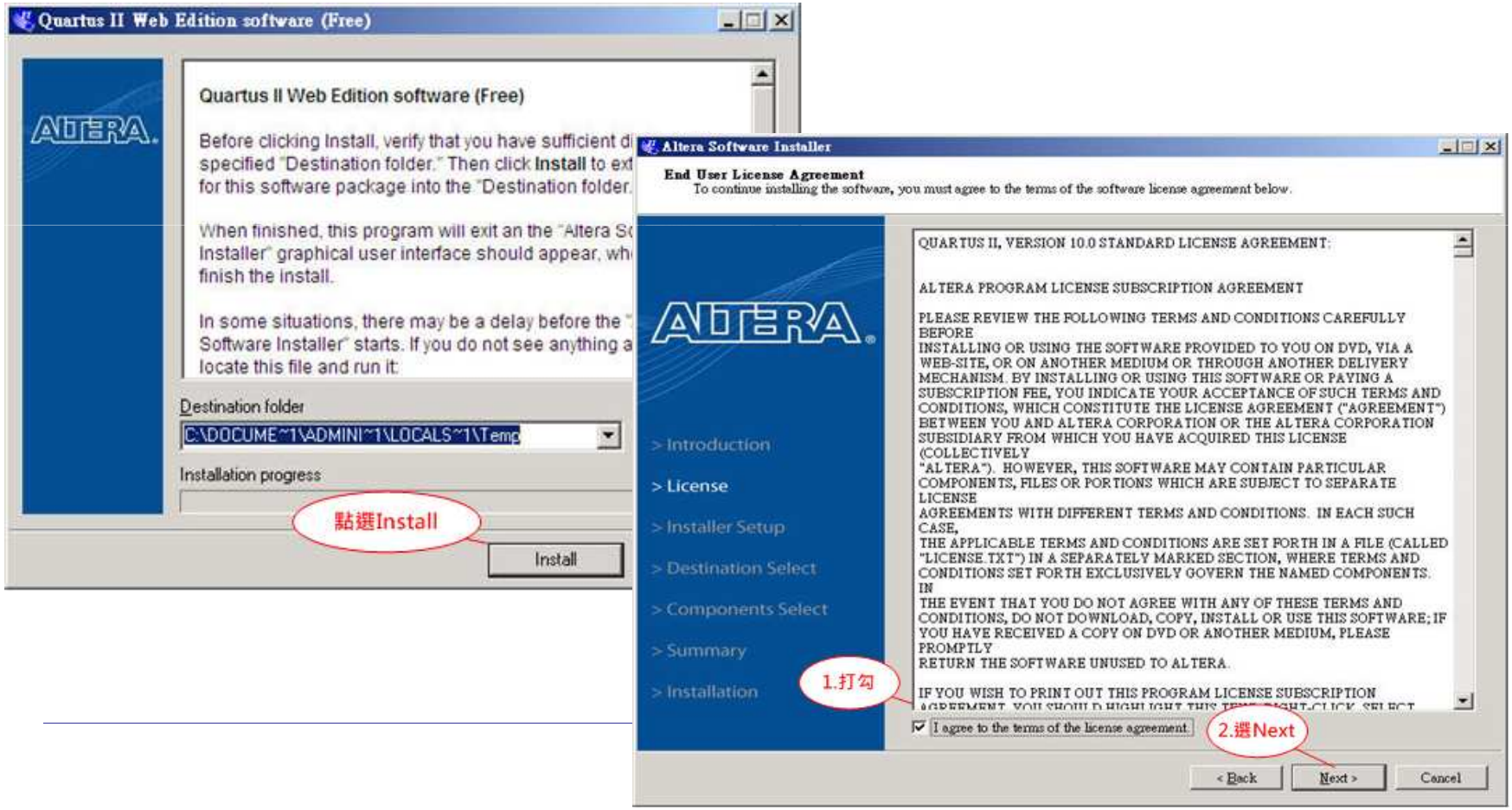
提示的VHDL程式碼(檔案路徑CDROM\MIAT_C3X_EVB_Demonstrations\TESTIO1)

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
library work;
entity MIATC3XTOP is
port(
        …
        -- Push Button 1~4
        iTOP_BUTTON : in  std_logic_vector(3 downto 0); -- Push Button

        -- LED 1~4
        oTOP_LED : out std_logic_vector(3 downto 0);      -- LED 4 Bits
        …
);
end MIATC3XTOP;
architecture RTL of MIATC3XTOP is
begin

    oTOP_LED <= iTOP_BUTTON;
--   oTOP_LED(3) <= iTOP_BUTTON(3);
--   oTOP_LED(2 downto 0) <= iTOP_BUTTON(2 downto 0);

end RTL;
```



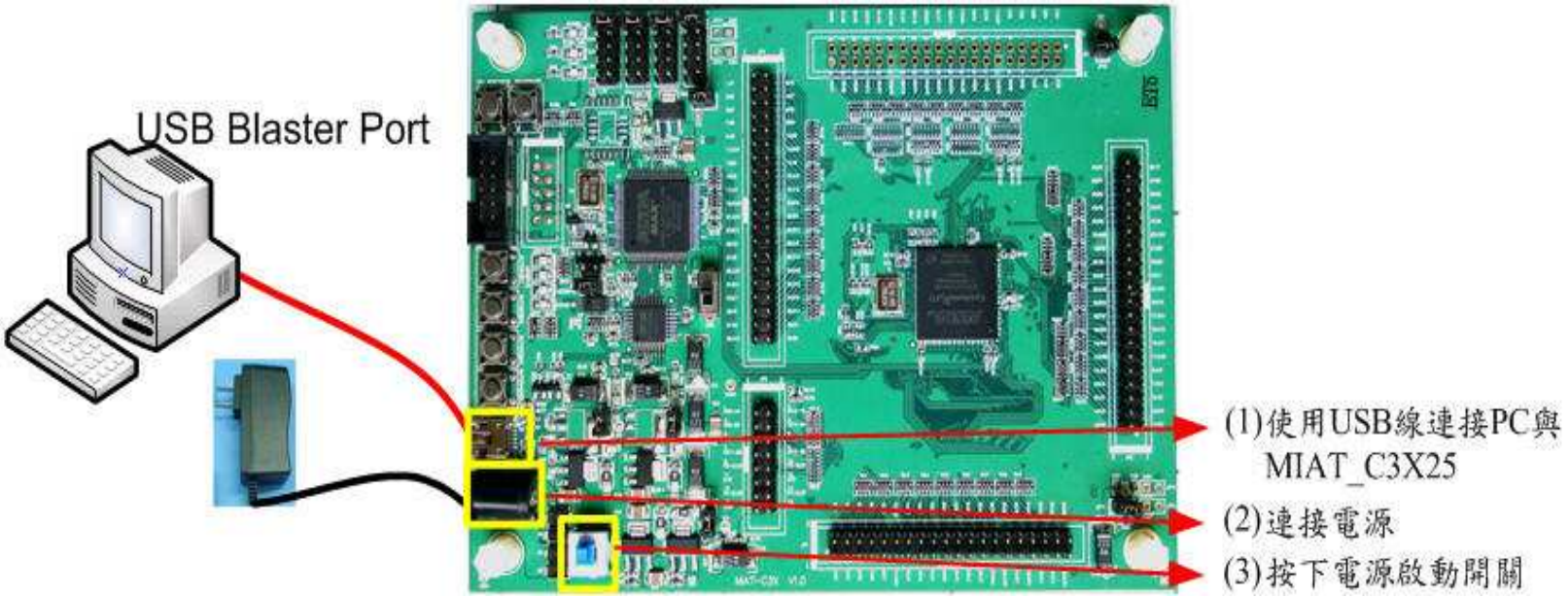
QuartusII軟體安裝

- 安裝10.0_quartus_free_windows.exe，此檔案的目錄位置在光碟內的“\Altera\”，安裝過程注意下列畫面，其他選Next與OK即可完成安裝。



MIAT_C3X實驗板安裝

- 步驟一、將實驗板連接PC

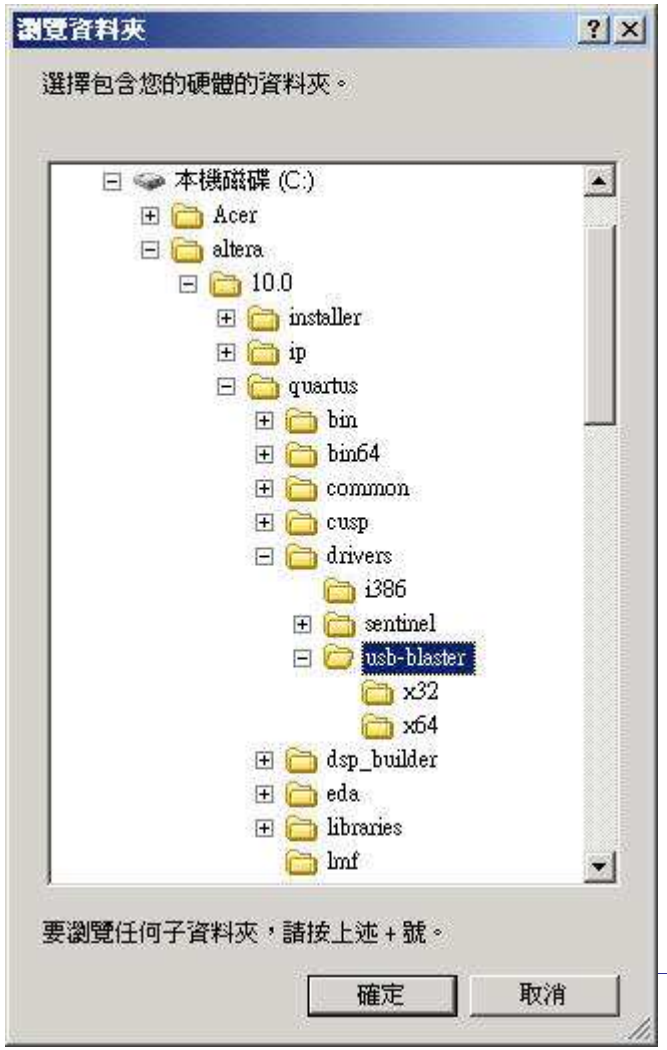


MIAT_C3X實驗板安裝

- 步驟二、驅動程式安裝，當實驗板第一次連接PC時，需安裝USB Blaster驅動程式，驅動程式目錄為C:\altera\10.0\quartus\drivers\usb-blaster 。

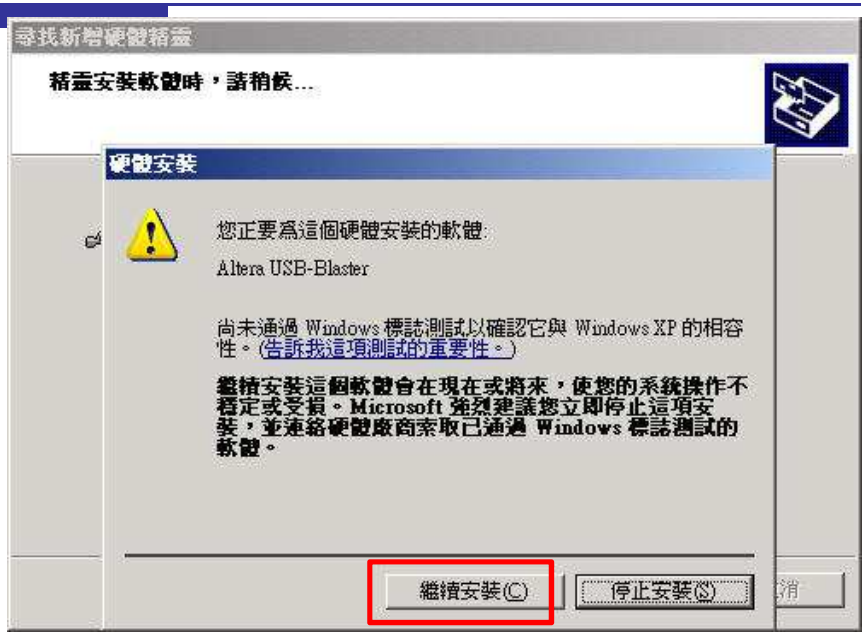
MIAT_C3X實驗板安裝

- 步驟二、驅動程式安裝



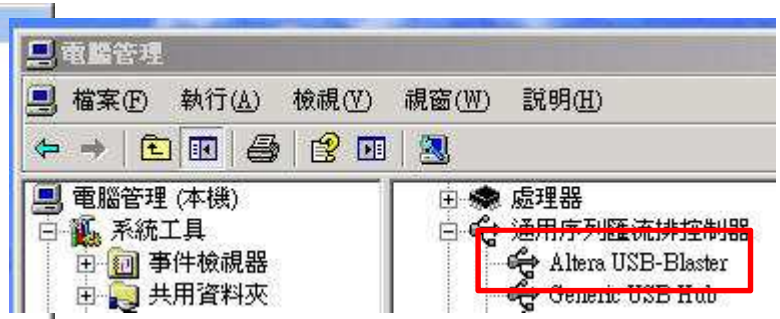
MIAT_C3X實驗板安裝

- 步驟二、驅動程式安裝



MIAT_C3X實驗板安裝

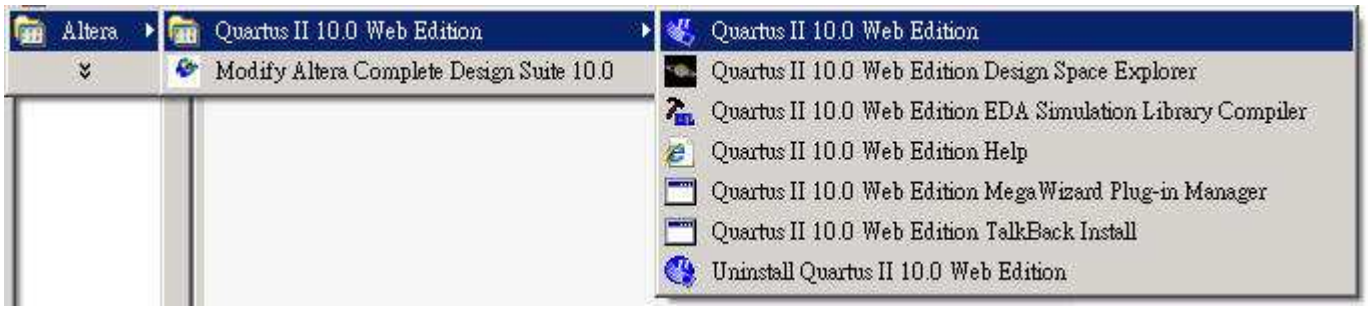
- 步驟二、驅動程式安裝



QuartusII軟體使用方法

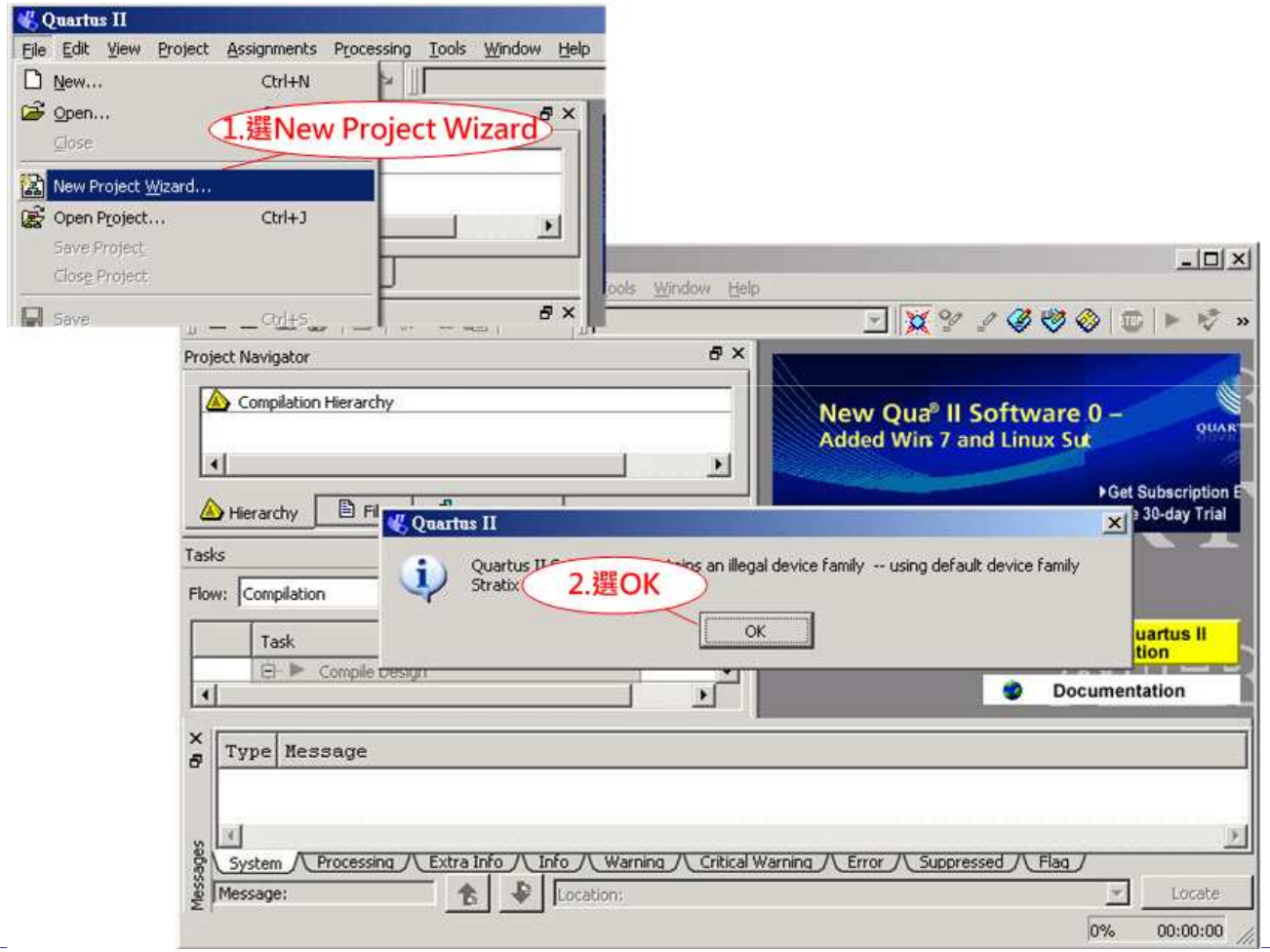
- 假設使用者已安裝QuartusII軟體工具，在此以TESTIO1為範例，目錄於CDROM\MIAT_C3X_EVB_Demonstrations\TESTIO1 ，設定步驟如下：
- 步驟一、 在\D:建立專案目錄並複製MIATC3XTOP.vhd檔案，如下圖

- 步驟二、執行Quartus II



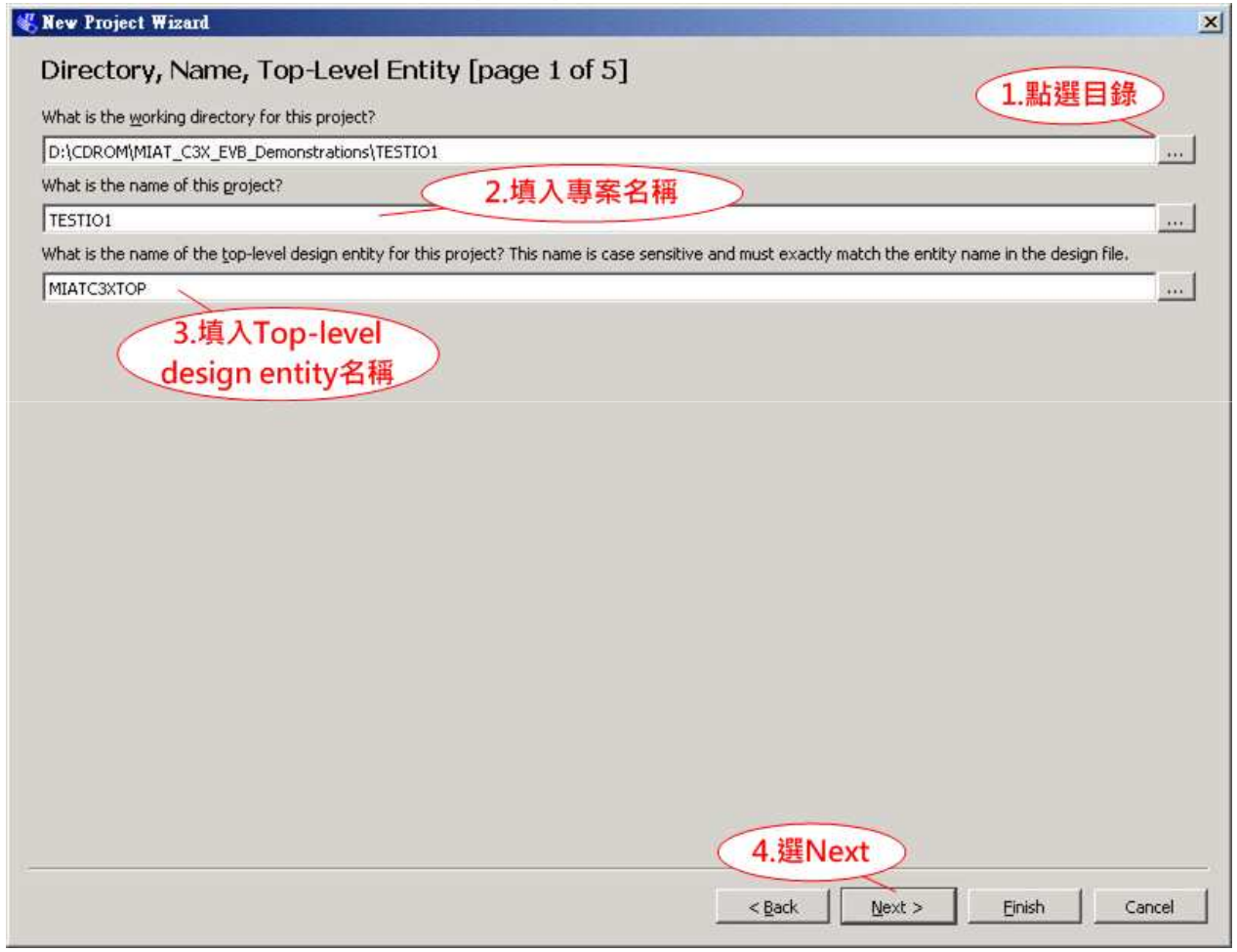
QuartusII軟體使用方法

- 步驟三、建立專案檔(1/6)

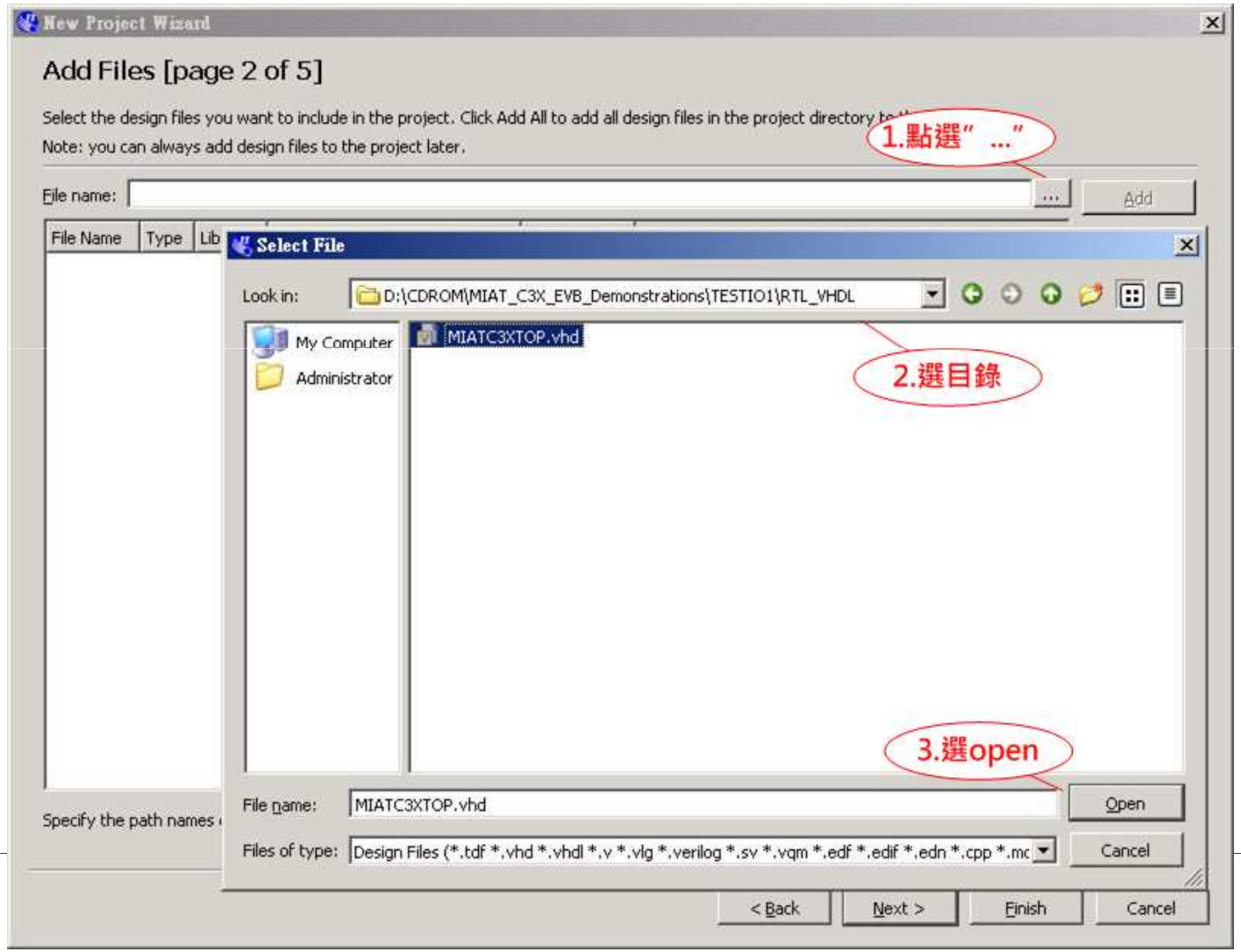


QuartusII軟體使用方法

- 步驟三、建立專案檔(2/6)

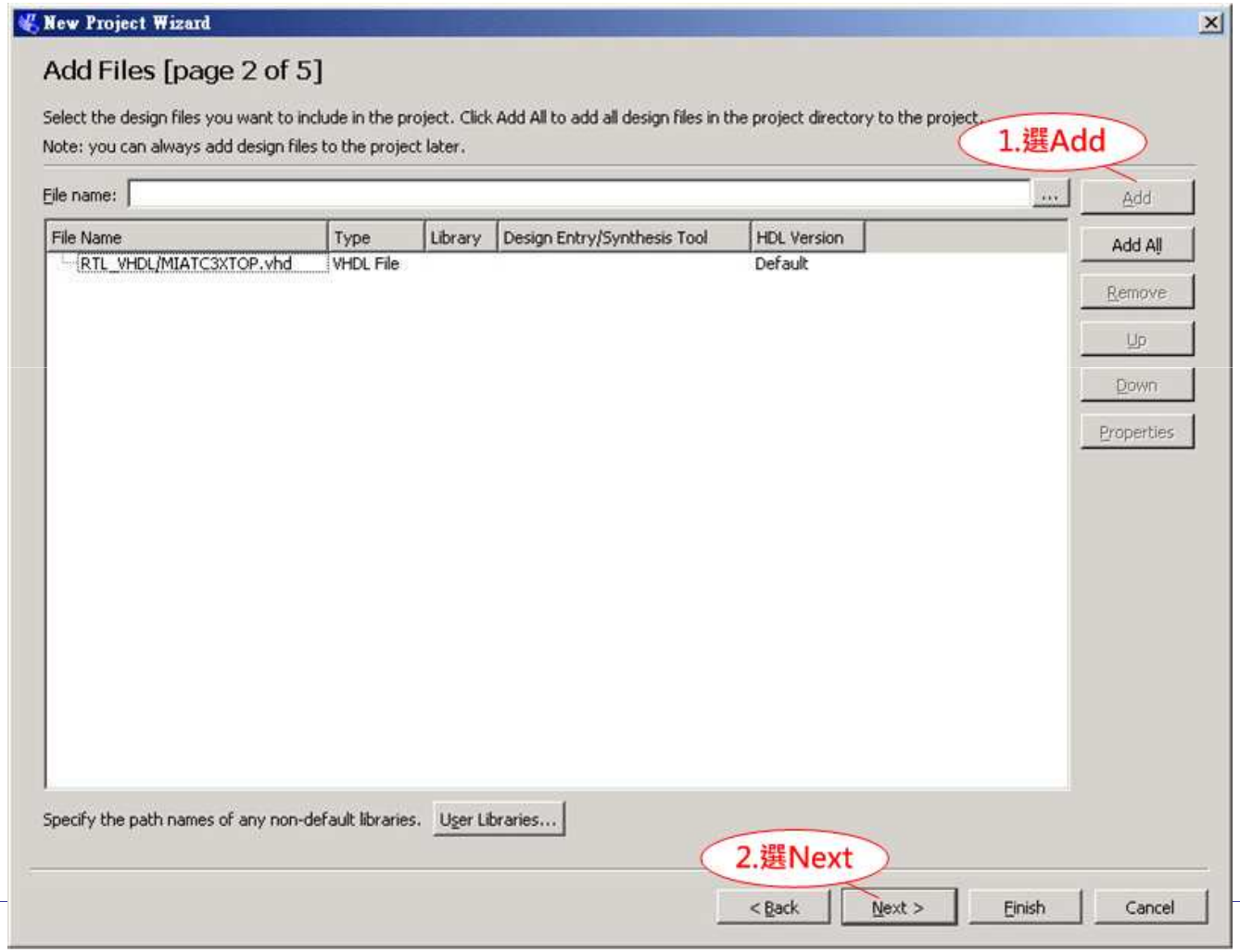


步驟三、建立專案檔(3/6)


New Project Wizard
Add Files [page 2 of 5]
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to
Note: you can always add design files to the project later.
1.點選" ..."
File name:
...
Add
File Name
Type
Lib
Select File
Look in:
D:\CDROM\MIAT_C3X_EVB_Demonstrations\TESTIO1\RTL_VHDL
My Computer
Administrator
MIATC3XTOP.vhd
2.選目錄
3.選open
File name:
MIATC3XTOP.vhd
Open
Files of type:
Design Files (*.tdf *.vhd *.vhdl *.v *.vlg *.verilog *.sv *.vqm *.edf *.edif *.edn *.cpp *.mc
Cancel
Specify the path names
< Back
Next >
Finish
Cancel

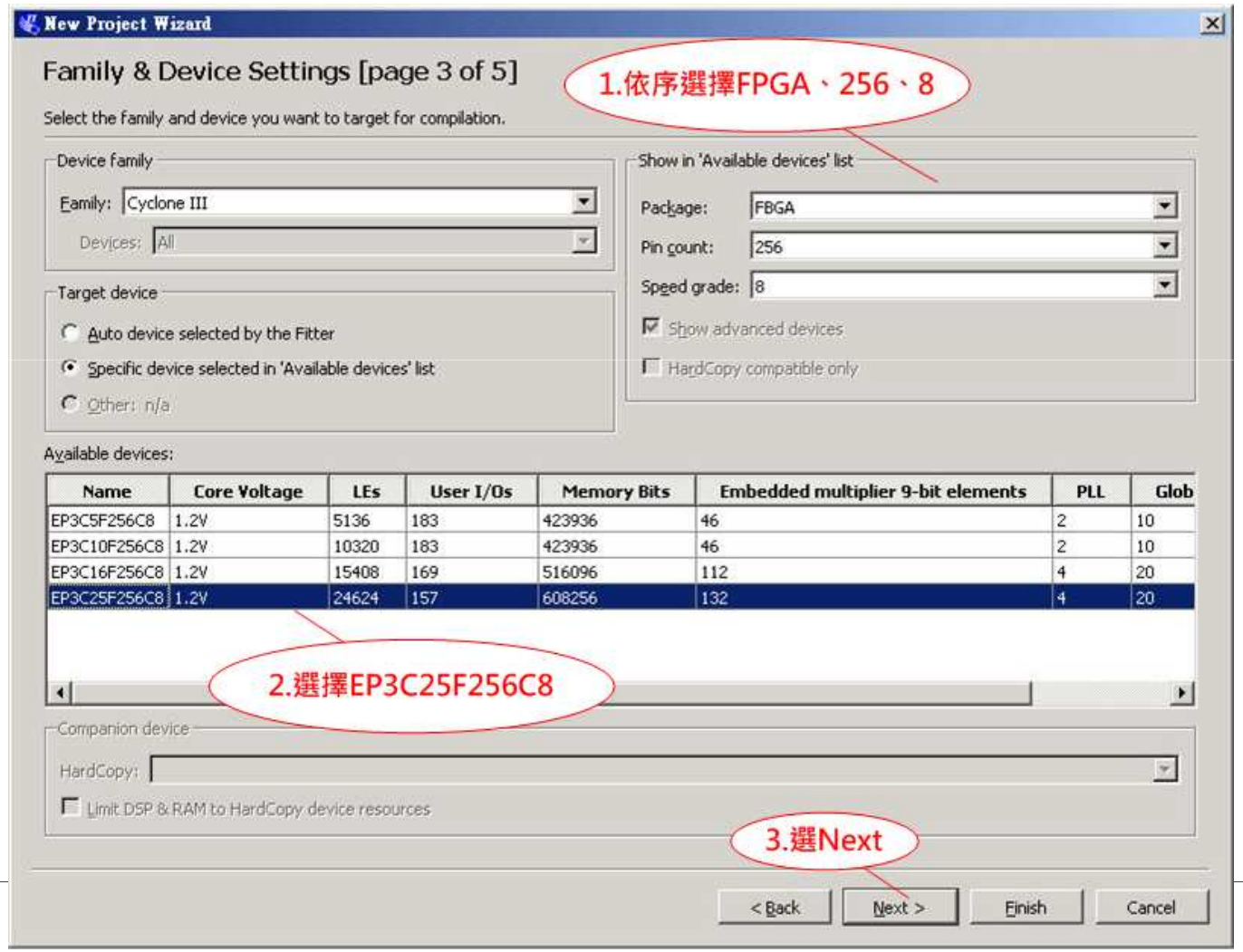
QuartusII軟體使用方法

- 步驟三、建立專案檔(4/6)



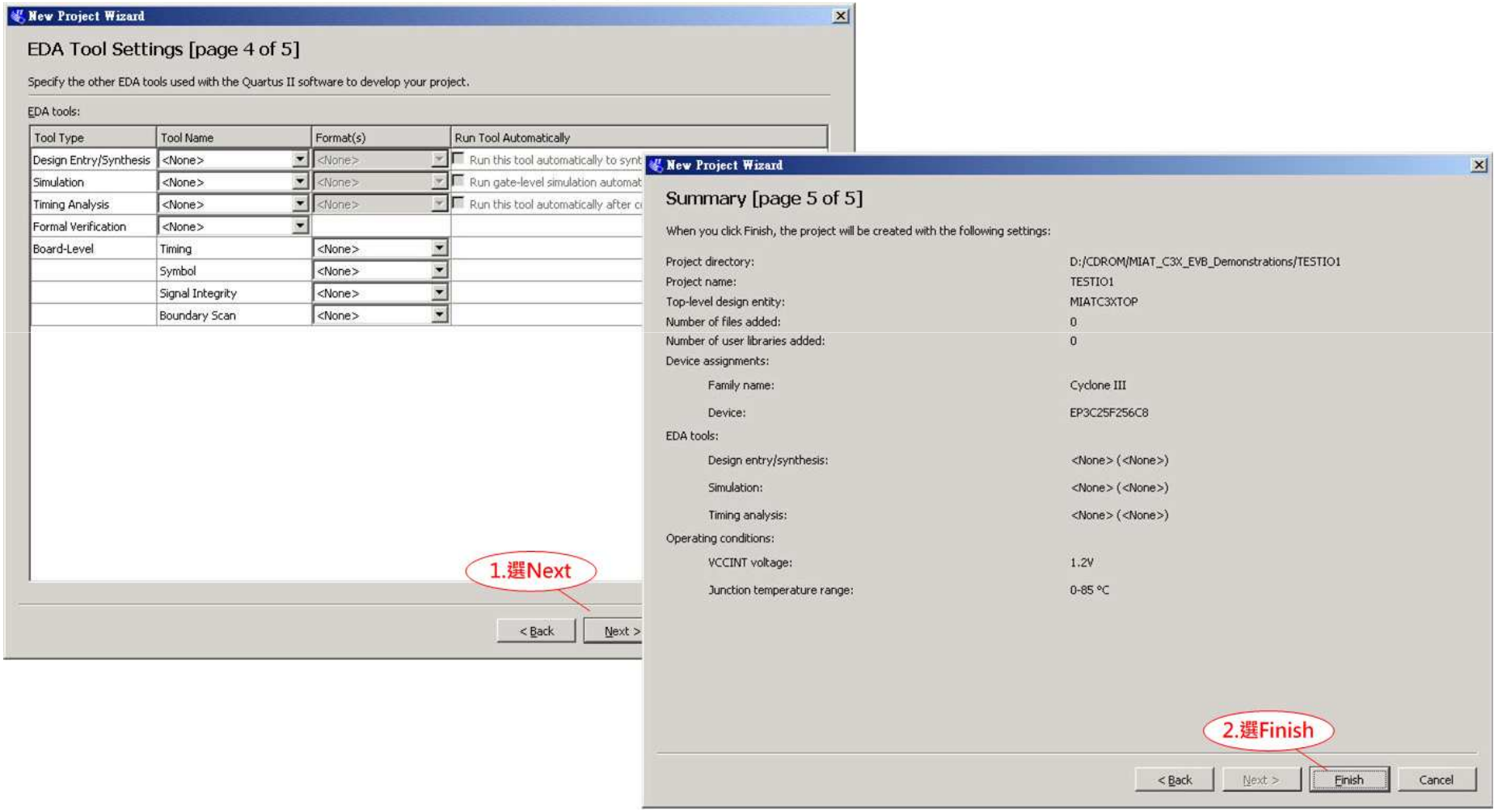
QuartusII軟體使用方法

- 步驟三、建立專案檔(5/6)



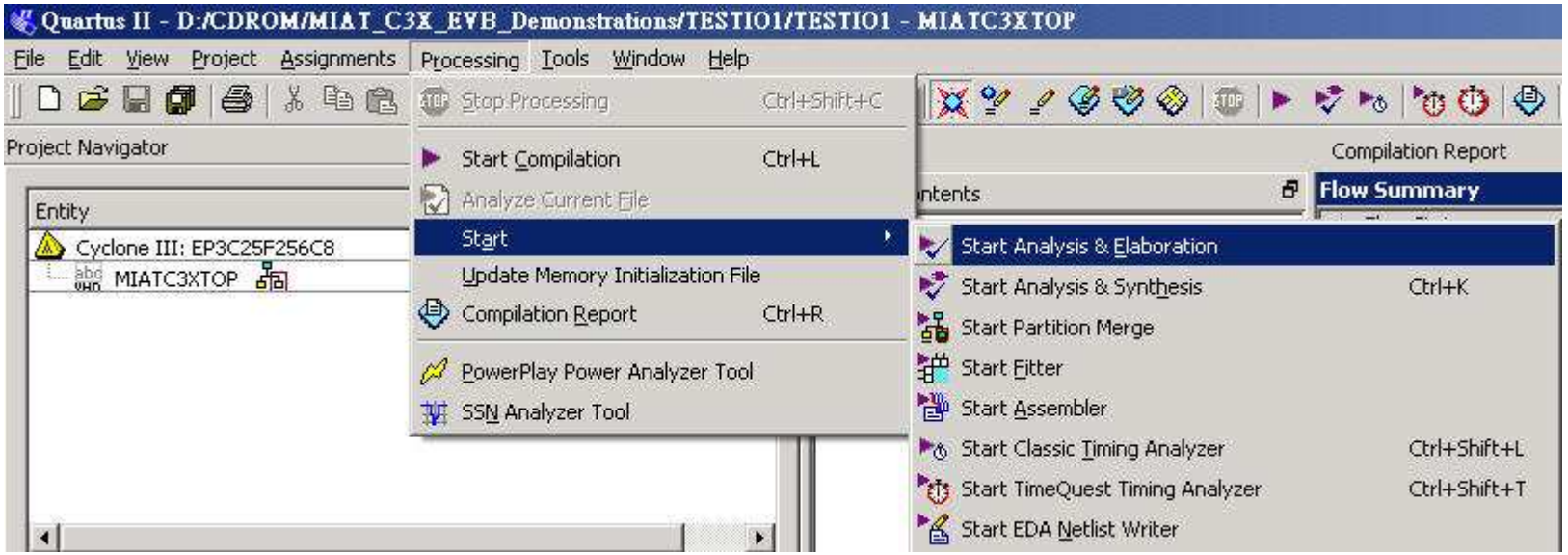
QuartusII軟體使用方法

- 步驟三、建立專案檔(6/6)



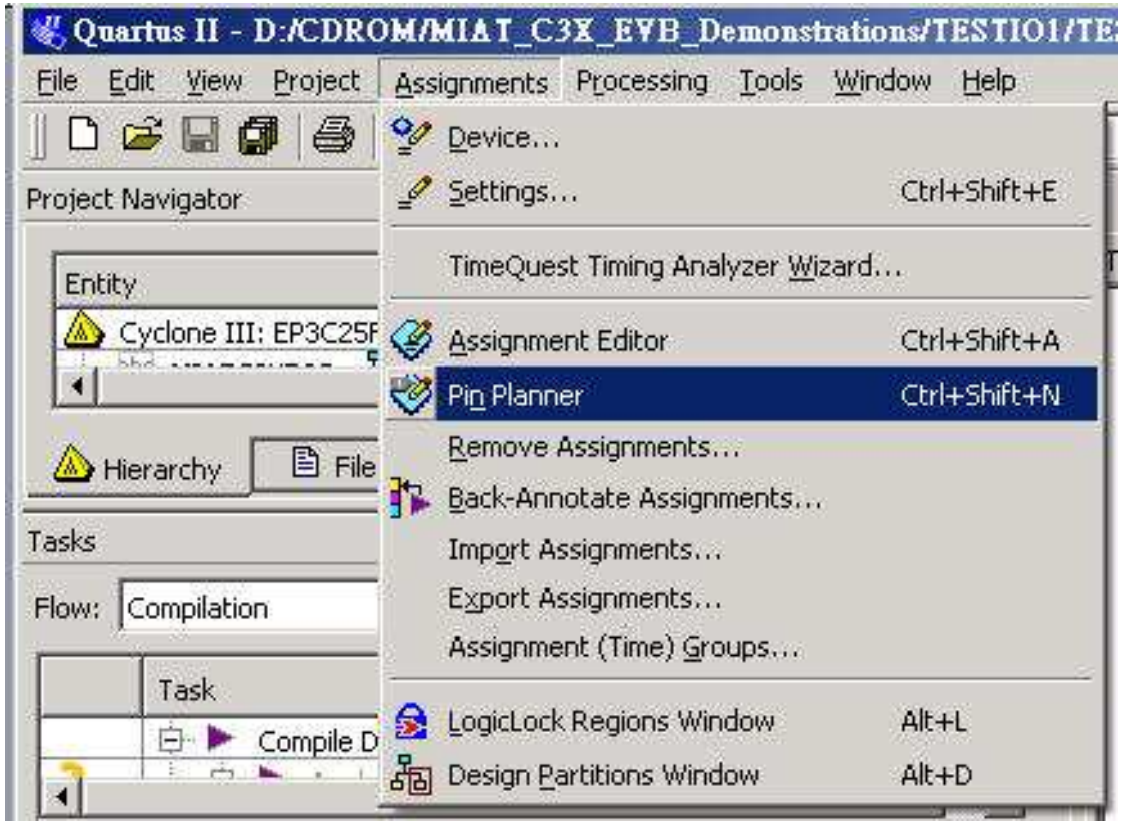
QuartusII軟體使用方法

- 步驟四、執行Analysis & Elaboration



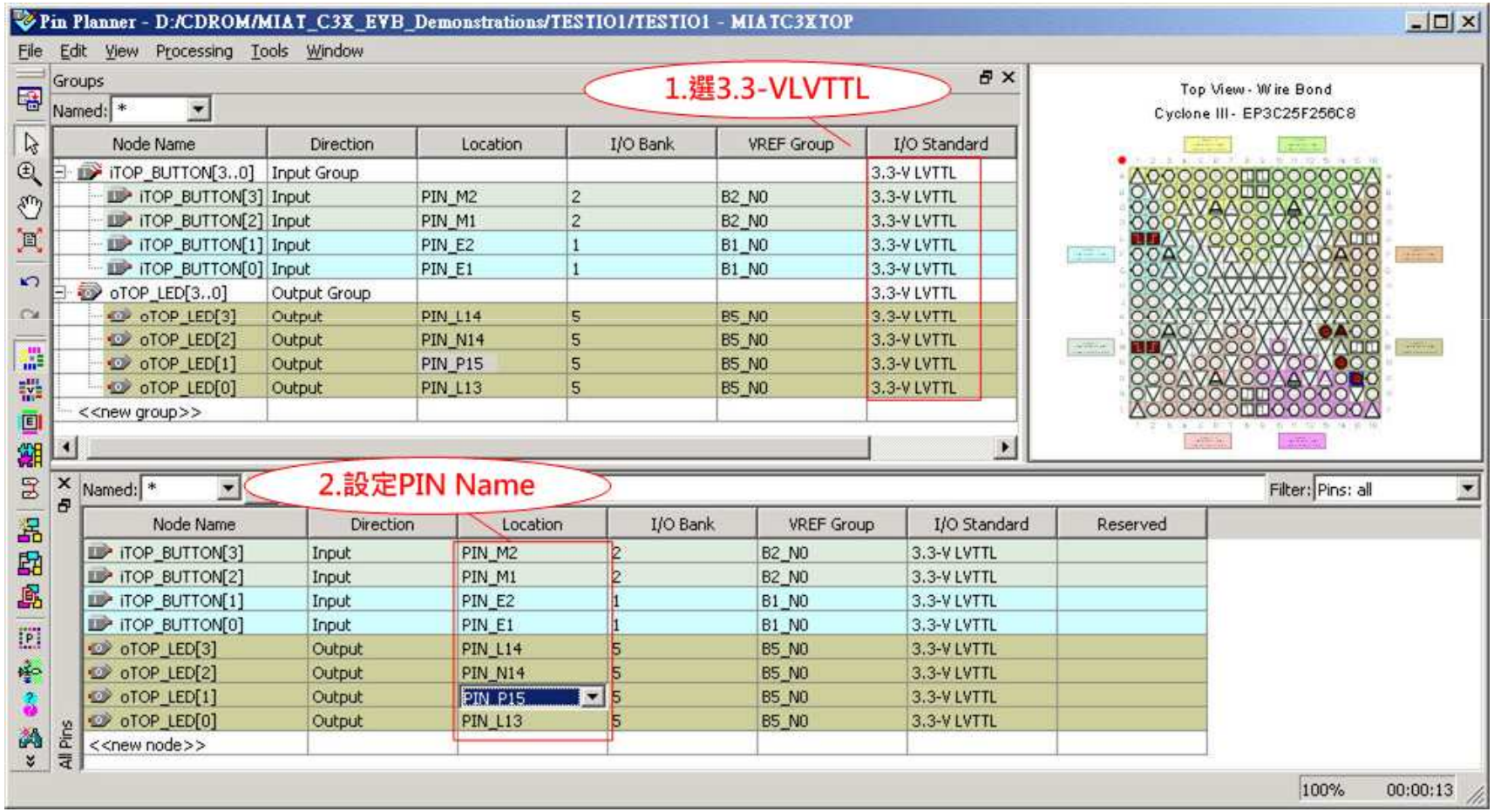
QuartusII軟體使用方法

- 步驟五、執行Pin Planner



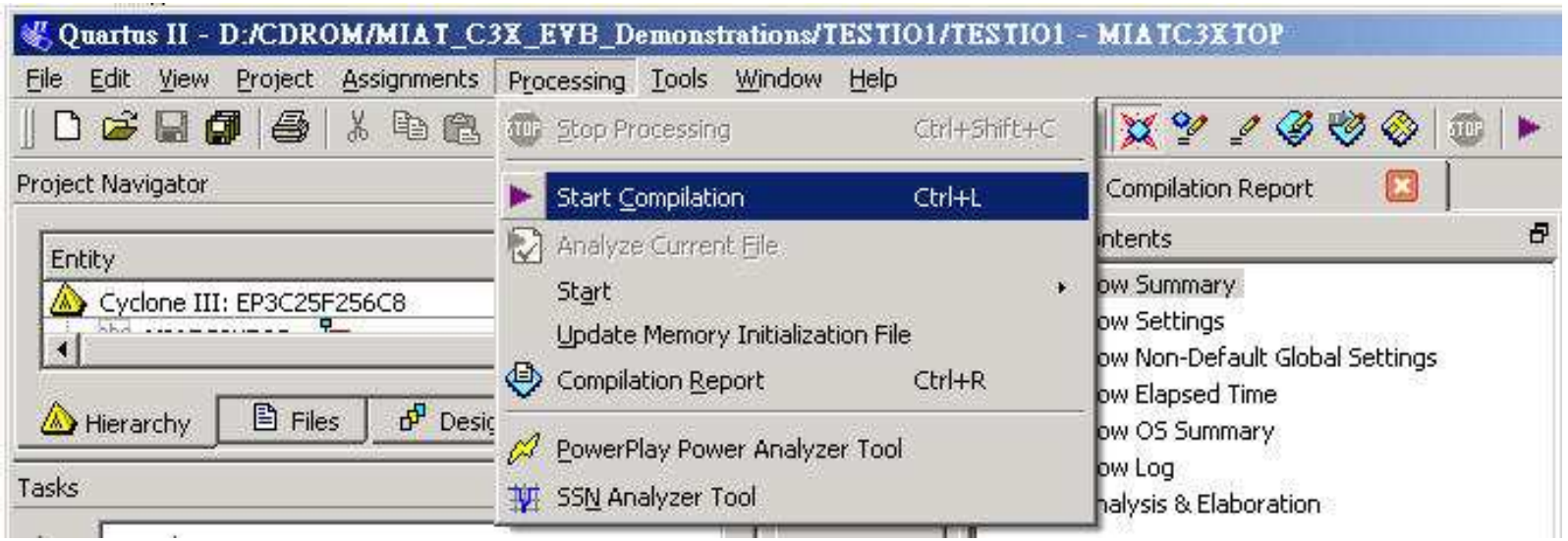
QuartusII軟體使用方法

- 步驟五、執行Pin Planner



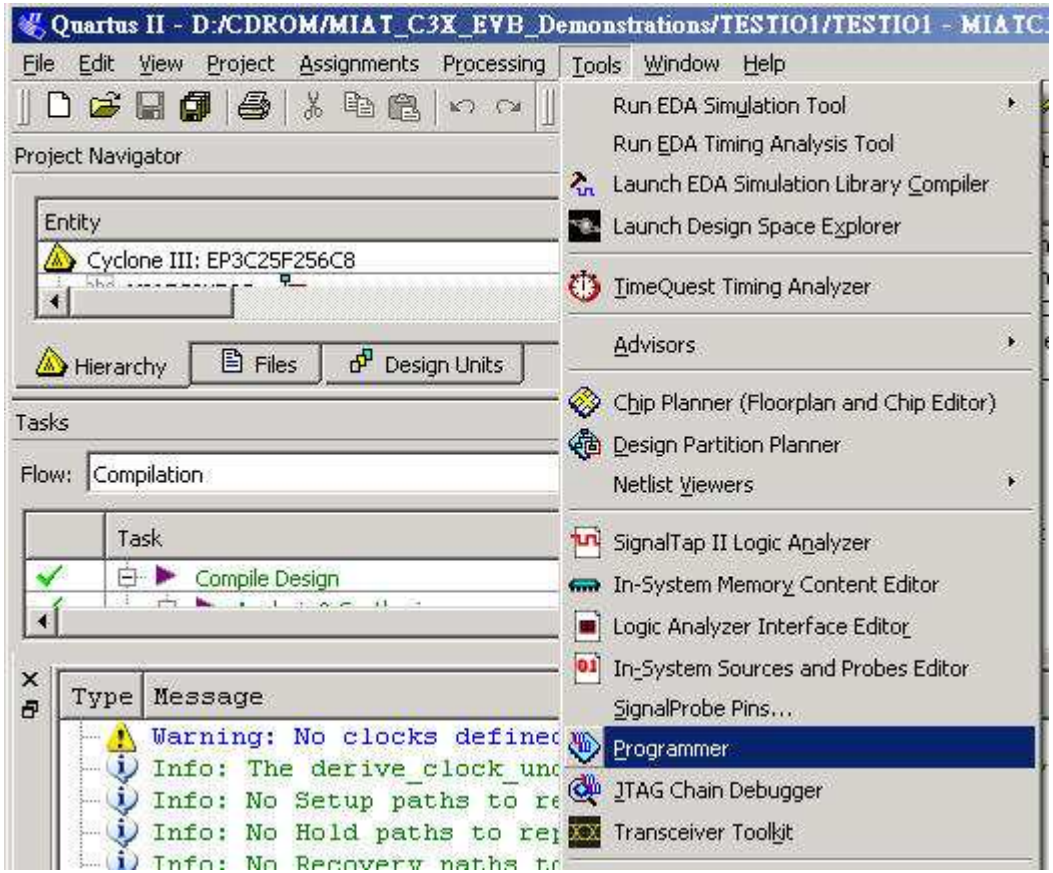
QuartusII軟體使用方法

- 步驟六、執行Start Compilation



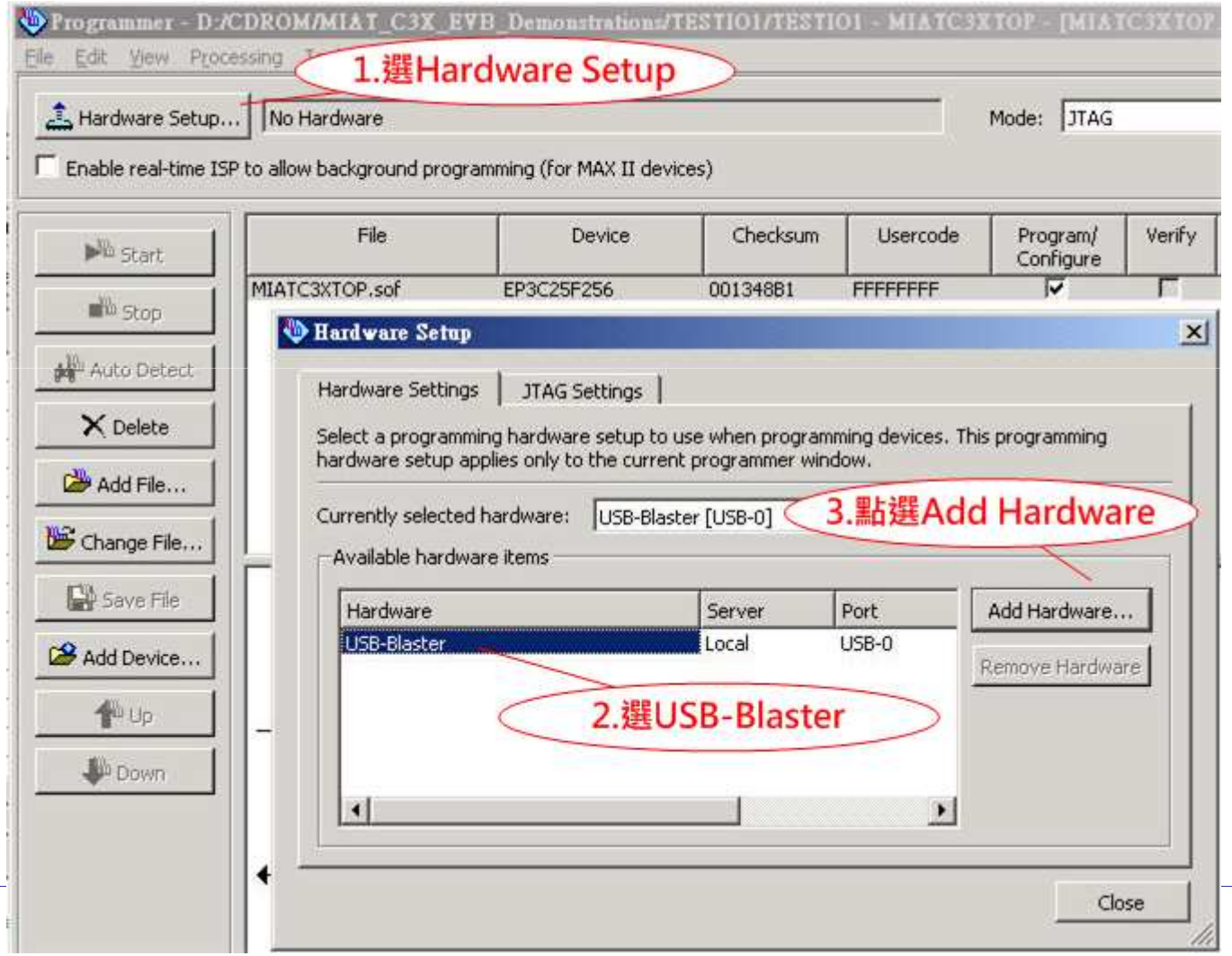
QuartusII軟體使用方法

- 步驟七、執行Programmer



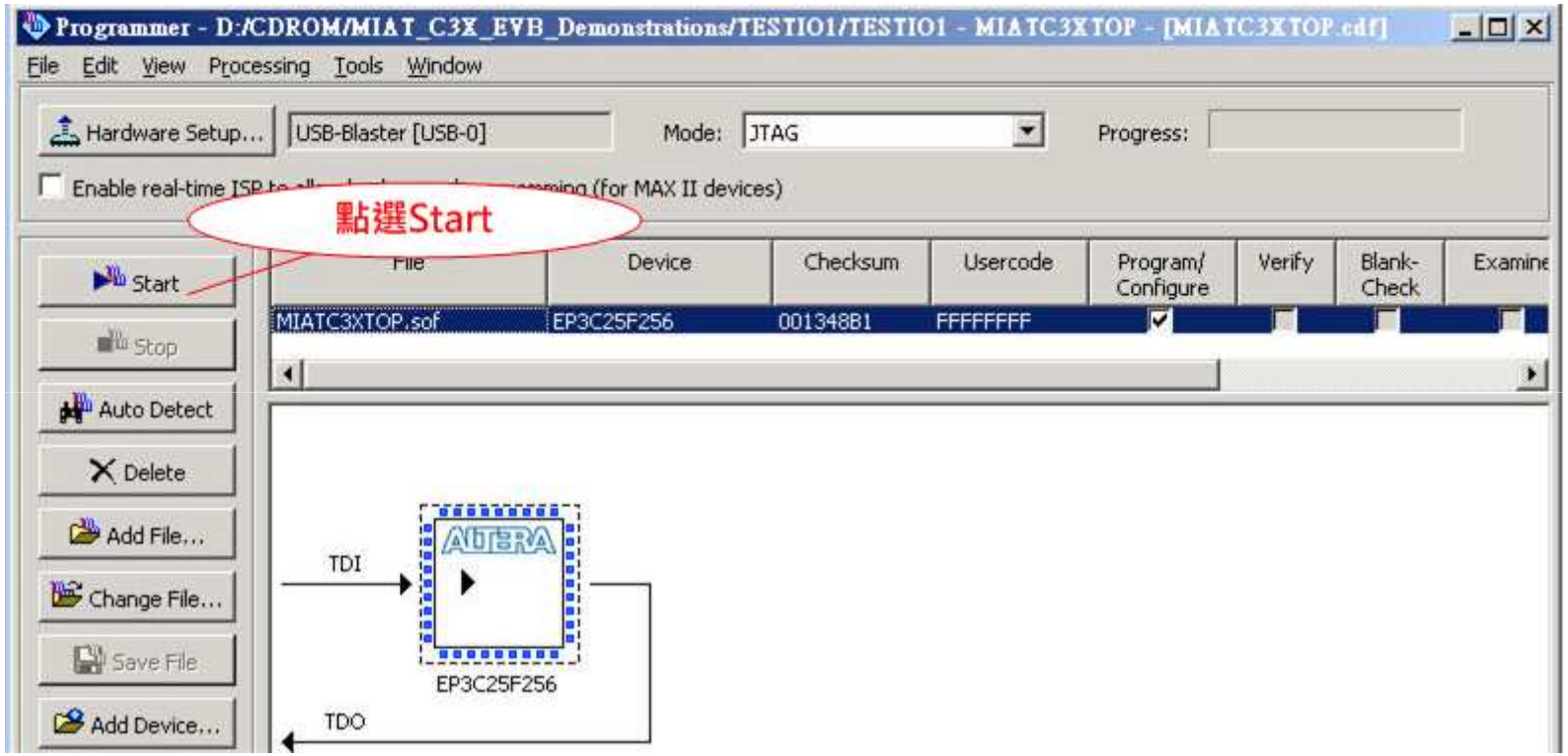
QuartusII軟體使用方法

- 步驟七、執行Programmer

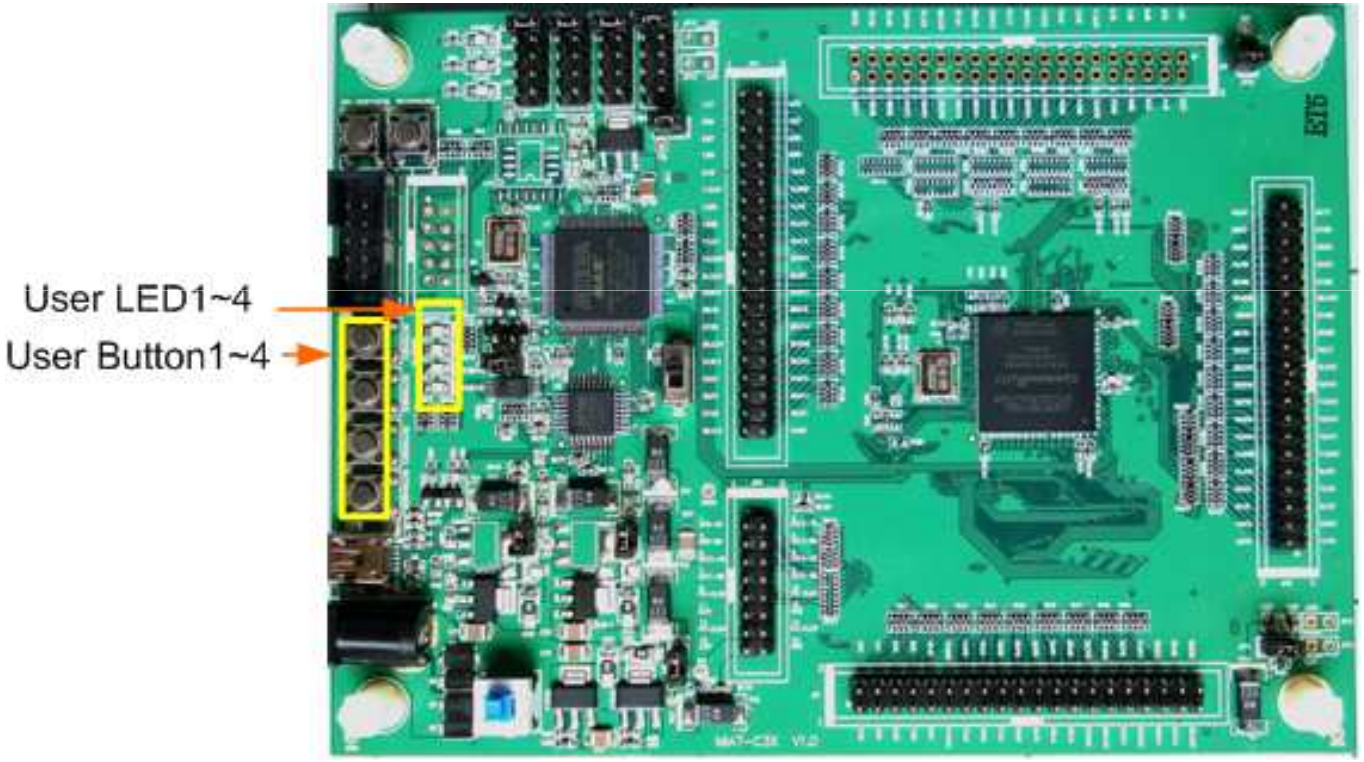


QuartusII軟體使用方法

- 步驟七、執行Programmer



- 步驟八、測試實驗板之Button與LED動作是否正確，當開關Button按下時相對應的LED被點亮，反之LED熄滅。



練習一、開發流程練習

- 步驟一、修改程式碼如下

```
begin

    --oTOP_LED <= iTOP_BUTTON;
    oTOP_LED(3) <= iTOP_BUTTON(3);
    oTOP_LED(2 downto 0)<= iTOP_BUTTON(2 downto 0);

end RTL;
```

步驟二、重新編譯與燒錄至實驗板後重新執行，觀察是否為預期之結果。

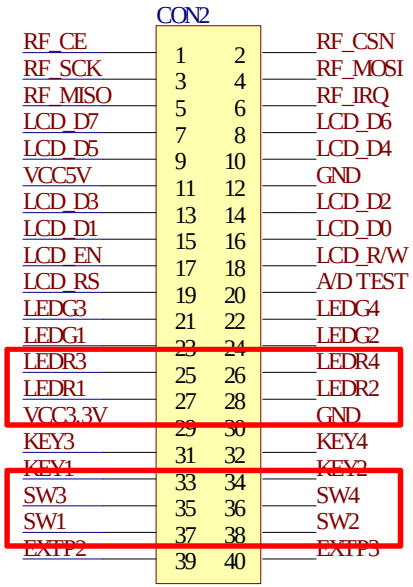
練習二、電路設計修改

- 步驟一、硬體電路配置

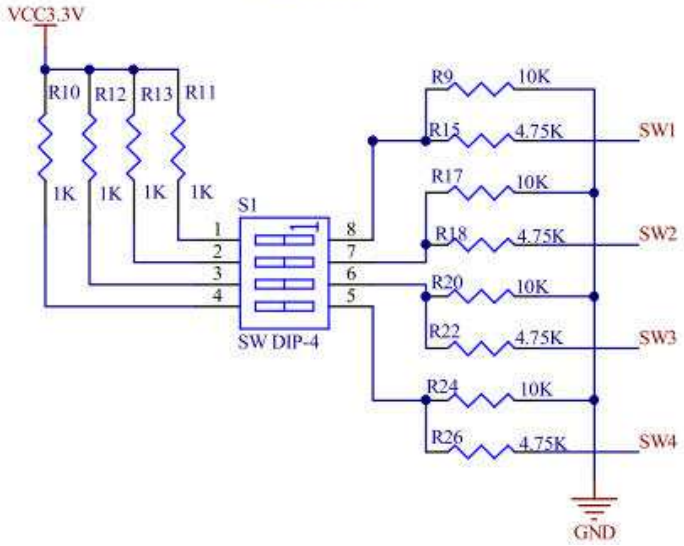
  將練習一之Button1~4與LED1~4改由IOB子板之周邊I/O電路SW1~4與LEDR1~4取代。使用SW控制LEDR之閃爍功能。

- MIAT_IOB之SW與LED之電路圖

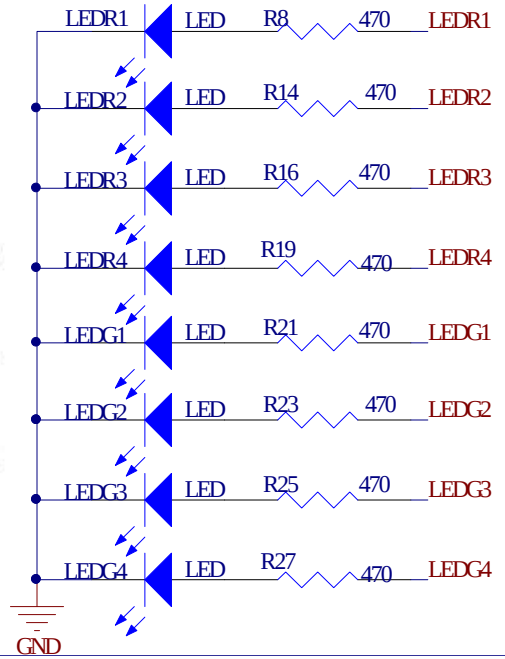
CONNECTOR2



SWITCH

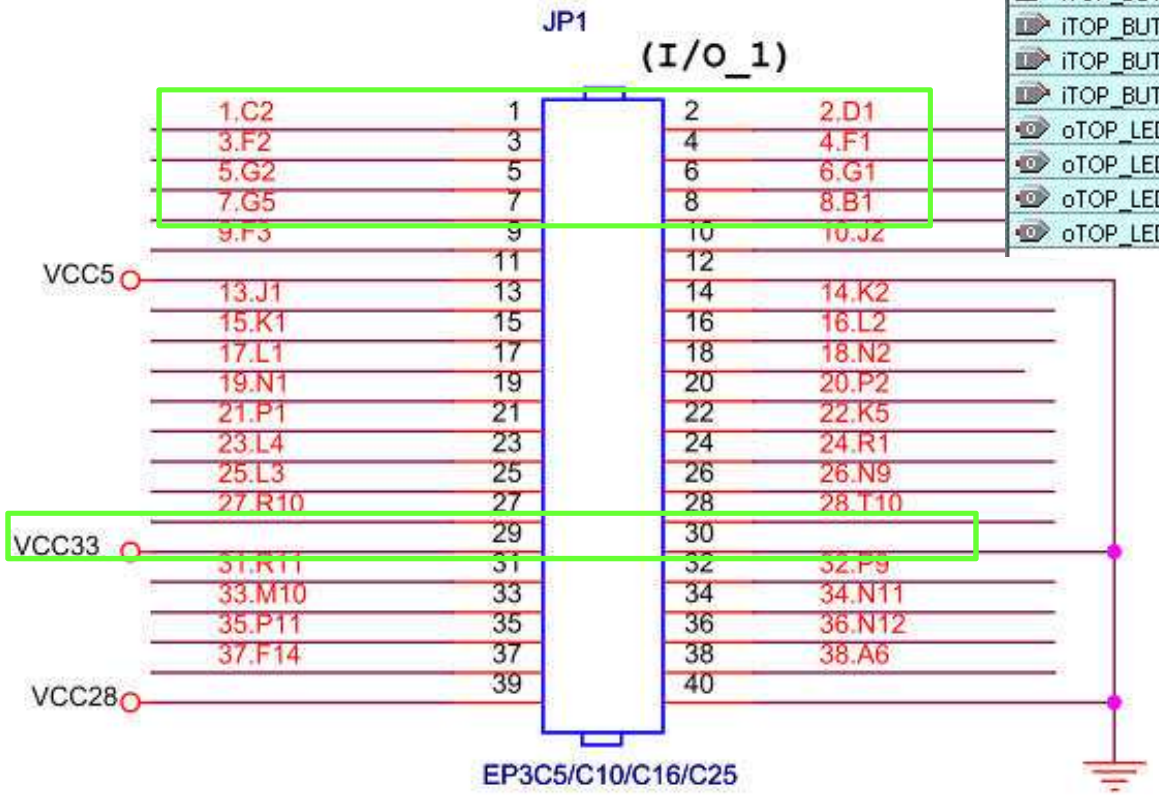


LED



練習二、電路設計修改

- MIAT_C3X 之JP1電路圖

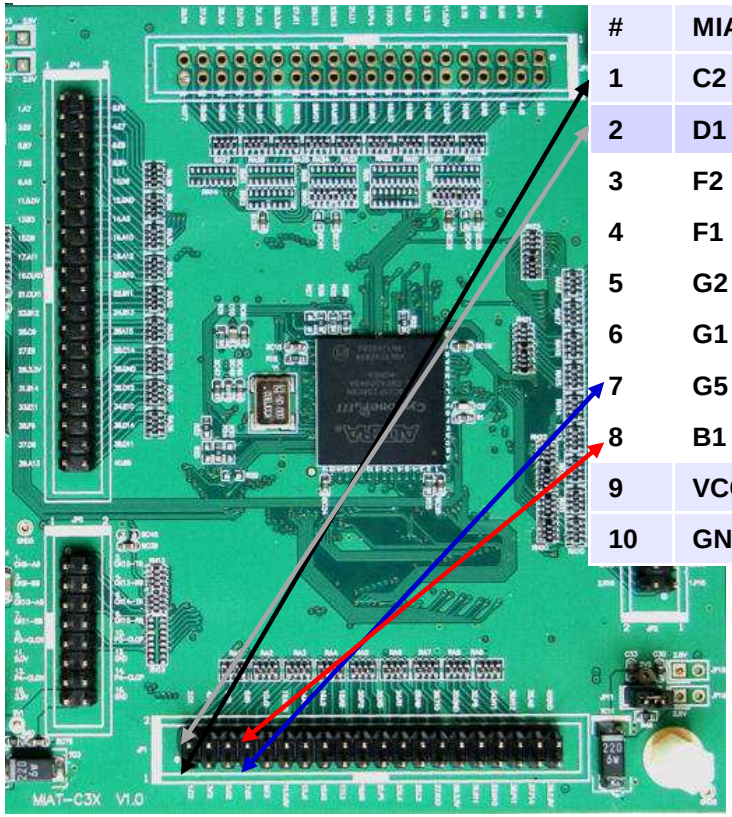


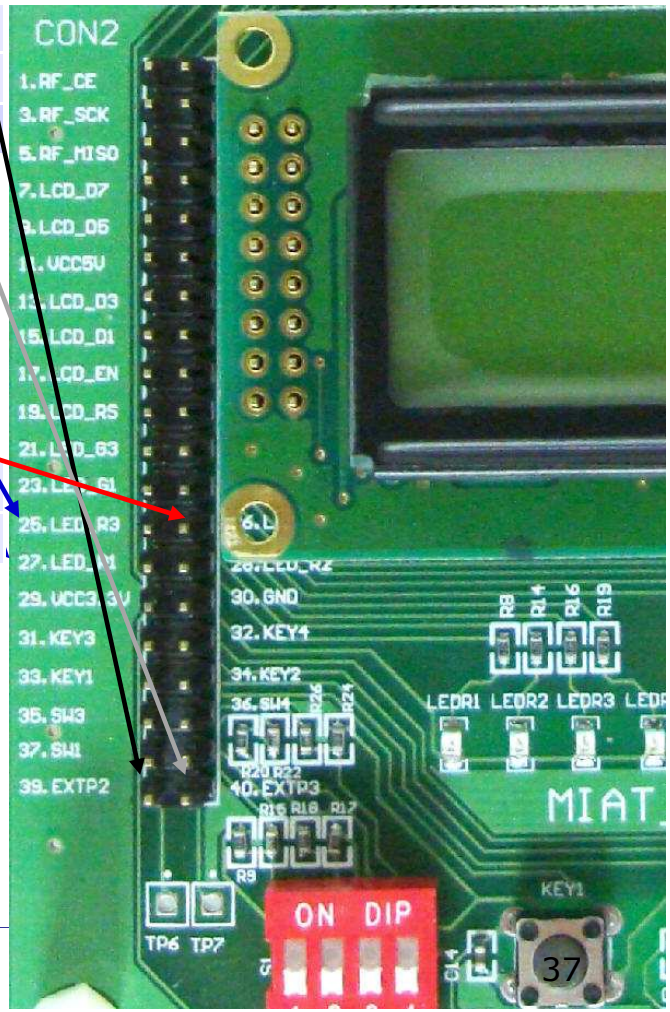
Node Name	Direction	Location
iTOP_BUTTON[3]	Input	PIN_F1
iTOP_BUTTON[2]	Input	PIN_F2
iTOP_BUTTON[1]	Input	PIN_D1
iTOP_BUTTON[0]	Input	PIN_C2
oTOP_LED[3]	Output	PIN_B1
oTOP_LED[2]	Output	PIN_G5
oTOP_LED[1]	Output	PIN_G1
oTOP_LED[0]	Output	PIN_G2

練習二、電路設計修改

- 線路連接

MIAT_C3X	Pin Mapping		MIAT_IOB
	#	MIAT_C3X	MIAT_IOB
	1	C2 (JP1.1)	SW1 (CON2.37)
	2	D1 (JP1.2)	SW2 (2.38)
	3	F2 (JP1.3)	SW3 (2.35)
	4	F1 (JP1.4)	SW4 (2.36)
	5	G2 (JP1.5)	LEDR1 (2.27)
	6	G1 (JP1.6)	LEDR2 (2.28)
	7	G5 (JP1.7)	LEDR3 (2.25)
	8	B1 (JP1.8)	LEDR4 (2.26)
	9	VCC3.3 (JP1.29)	VCC3.3 (2.29)
	10	GND(JP1.30)	GND(2.30)





Q & A

WU-YANG

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