

MIAT-C3X-EVB

軟硬體實驗模組與開發流程介紹

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Declared Version

Training Only

Declare

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Document Title	MIAT-C3X-EVB軟硬體實驗模組與開發流程介紹
Exercise Time	-----
Platform	■ MIAT_C3X ■ MIAT_IOB
Peripheral	Key Switch, LED
Author	■ WU-YANG Technology Co., Ltd.



Outline

- MIAT_C3X實驗板
 - 主要功能介紹
 - 硬體環境設定
- MIAT_IOB實驗板
 - 各個週邊模組功能介紹
- 開發流程介紹
 - 以基本I/O驅動為例
 - 硬體電路配置
 - Quartus II軟體基本使用方法介紹
- 開發流程練習



MIAT_C3X實驗板主要功能介紹

□ FPGA編號Altera Cyclone III EP3C25

- 24,624 Logic Elements
- 594(66x9) Kbits Memory
- 66 Multipliers
- 4 PLLs
- 20 Global Clock Networks
- 156 I/O Pin Counts

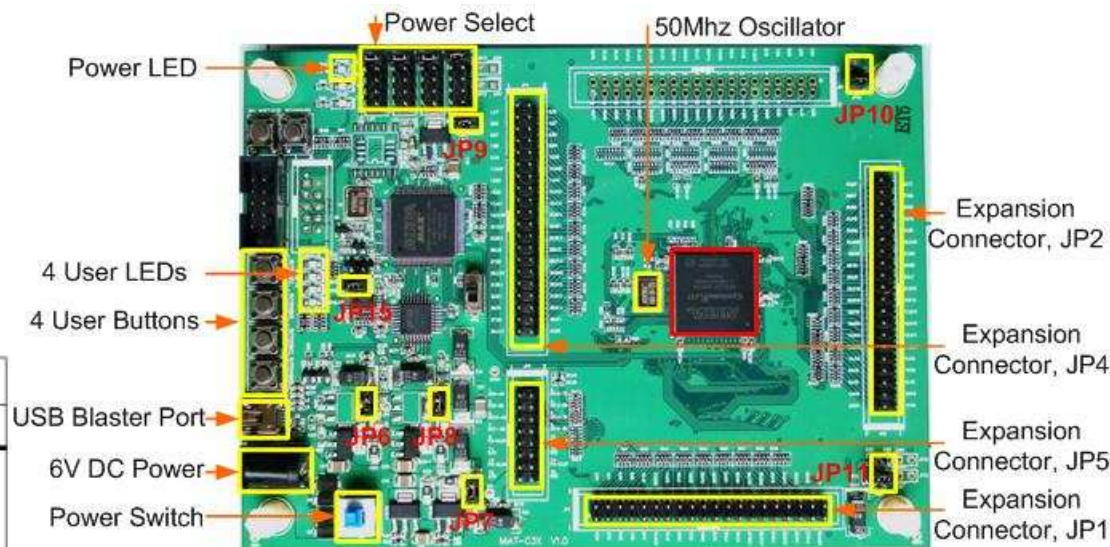
Table 1-6. Cyclone III FPGA I/O Standards Support *Note (1)*

Type	I/O Standard
Single-Ended I/O	<ul style="list-style-type: none">• LVTTTL• LVCMOS• SSTL• HSTL• PCI• PCI-X
Differential I/O	<ul style="list-style-type: none">• SSTL• HSTL• LVPECL• BLVDS• LVDS• mini-LVDS• RSDS• PPDS

Note to Table 1-6:

(1) PCI Express and Serial Rapid I/O can be supported using an external PHY device.

- Support Memory Types
 - DDR, DDR2, SDRAM
 - Data Rates up to 400 Mbps
- FBGA 256



MIAT_C3X正面



MIAT_C3X實驗板主要功能介紹

□ FPGA內部可合成記憶體之規格

Table 4–1. Summary of M9K Memory Features (Part 1 of 2)

Feature	M9K Blocks
Maximum performance	315 MHz
Total RAM bits (including parity bits)	9,216
Configurations (depth × width)	8192 × 1 4096 × 2 2048 × 4 1024 × 8 1024 × 9 512 × 16 512 × 18 256 × 32 256 × 36
Parity bits	✓
Byte enable	✓
Packed mode	✓
Address clock enable	✓
Single-port mode	✓
Simple dual-port mode	✓
True dual-port mode	✓



MIAT_C3X實驗板主要功能介紹

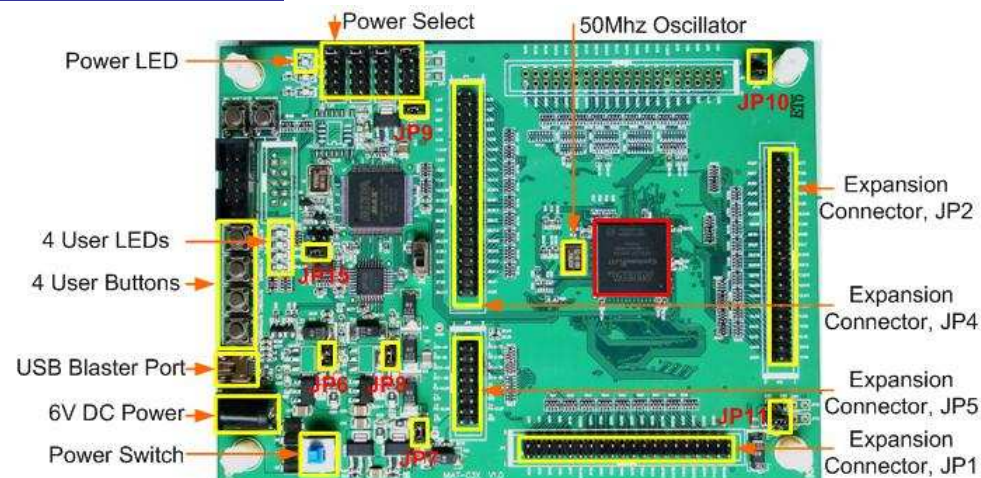
□ FPGA內部可合成記憶體之規格

Table 4-1. Summary of M9K Memory Features (Part 2 of 2)	
Feature	M9K Blocks
Embedded shift register mode (1)	✓
ROM mode	✓
FIFO buffer (1)	✓
Simple dual-port mixed width support	✓
True dual-port mixed width support (2)	✓
Memory initialization file (.mif)	✓
Mixed-clock mode	✓
Power-up condition	Outputs cleared
Register asynchronous clears	Read address registers and output registers only
Latch asynchronous clears	Output latches only
Write/Read operation triggering	Write and Read: Rising clock edges
Same-port read-during-write	Outputs set to "Old Data" or "New Data"
Mixed-port read-during-write	Outputs set to "Old Data" or "Don't Care"

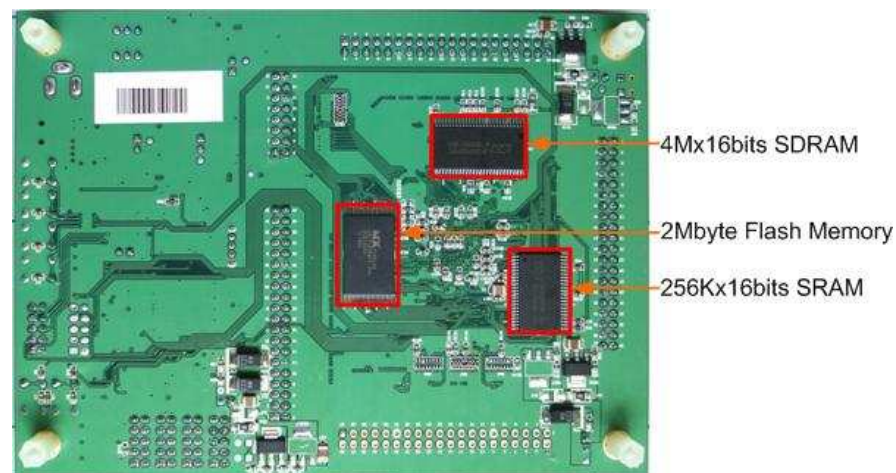


MIAT_C3X實驗板主要功能介紹

- 50Mhz Oscillator
- 可由USB介面燒錄電路
- 4個使用者測試 LED
- 4個使用者測試按鈕開關
- 核心晶片之I/O接腳以2.54mm間距的2x20PIN排針連接，可彈性擴充週邊。
- I/O接腳邏輯電位可調(1.2V, 1.8V, 2.5V, 2.8V, 3.3V)。
- 外部記憶體
 - 4Mx16bits SDRAM
 - 2Mbyte Flash Memory
 - 256Kx16bits SRAM
- 電源DC6V
- 尺寸：150x110mm



MIAT_C3X正面



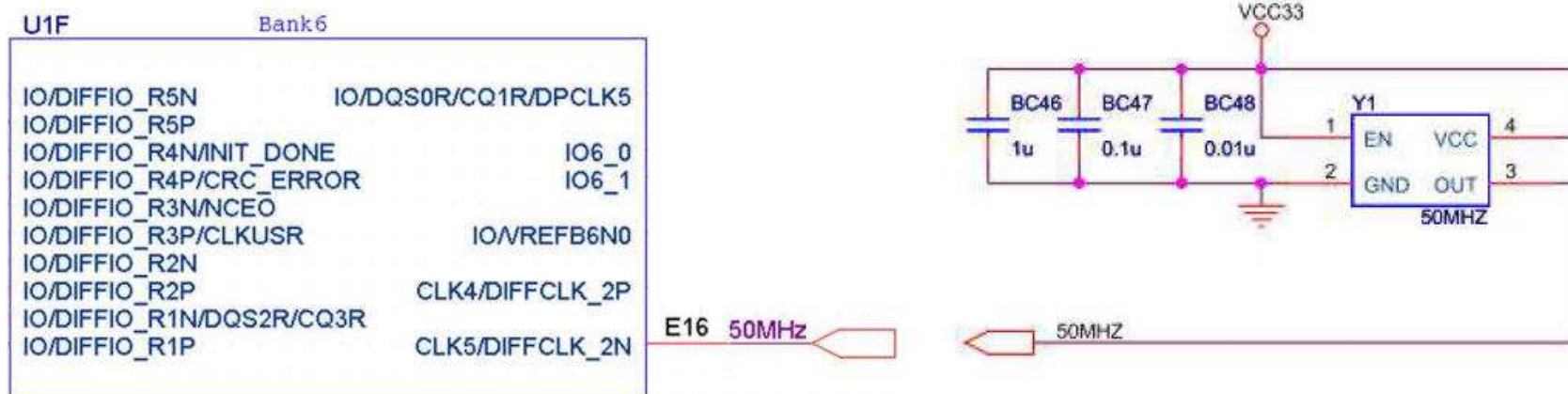
MIAT_C3X反面



MIAT_C3X實驗板主要功能介紹

石英晶體振盪器

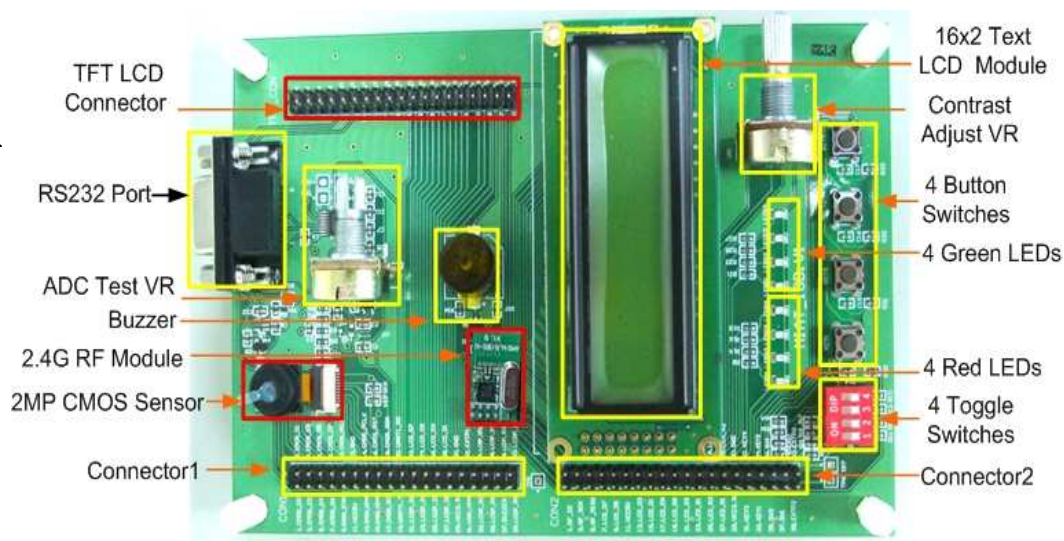
Signal Name	FPGA Pin Name	Bank No.
50MHz	E16	B6





MIAT_IOB實驗週邊功能介紹

- ❑ 2MPixels CMOS Sensor模組
- ❑ 2.4G RF模組
- ❑ 2x16文字型LCD模組
(含明暗度調整電阻)
- ❑ RS232介面
- ❑ AD轉換測試模組
- ❑ 蜂鳴器
- ❑ 4個紅色LED
- ❑ 4個綠色LED
- ❑ 4個按鈕開關
- ❑ 4 P指撥開關
- ❑ TFT LCD 2.54mm連接器
- ❑ 尺寸：145x103mm





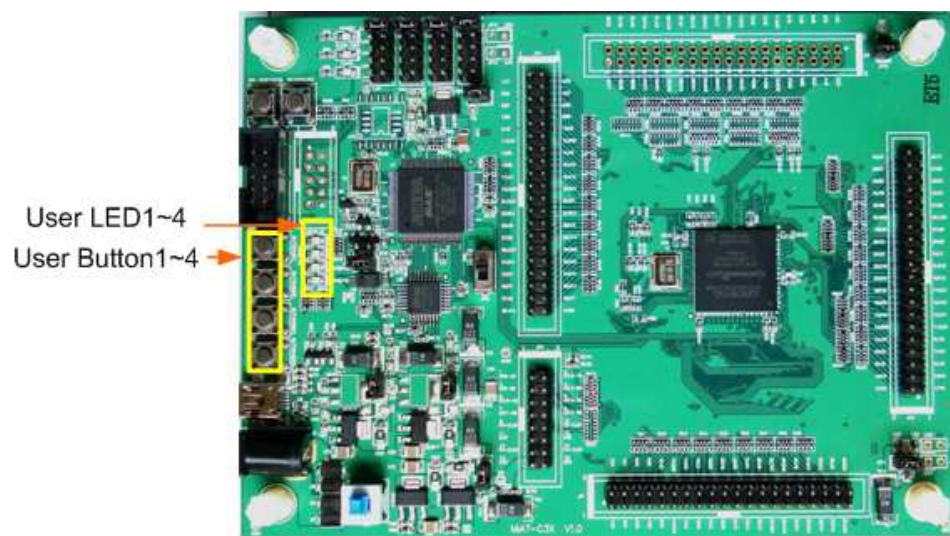
開發流程介紹－以基本I/O驅動為例

□ 實驗目的

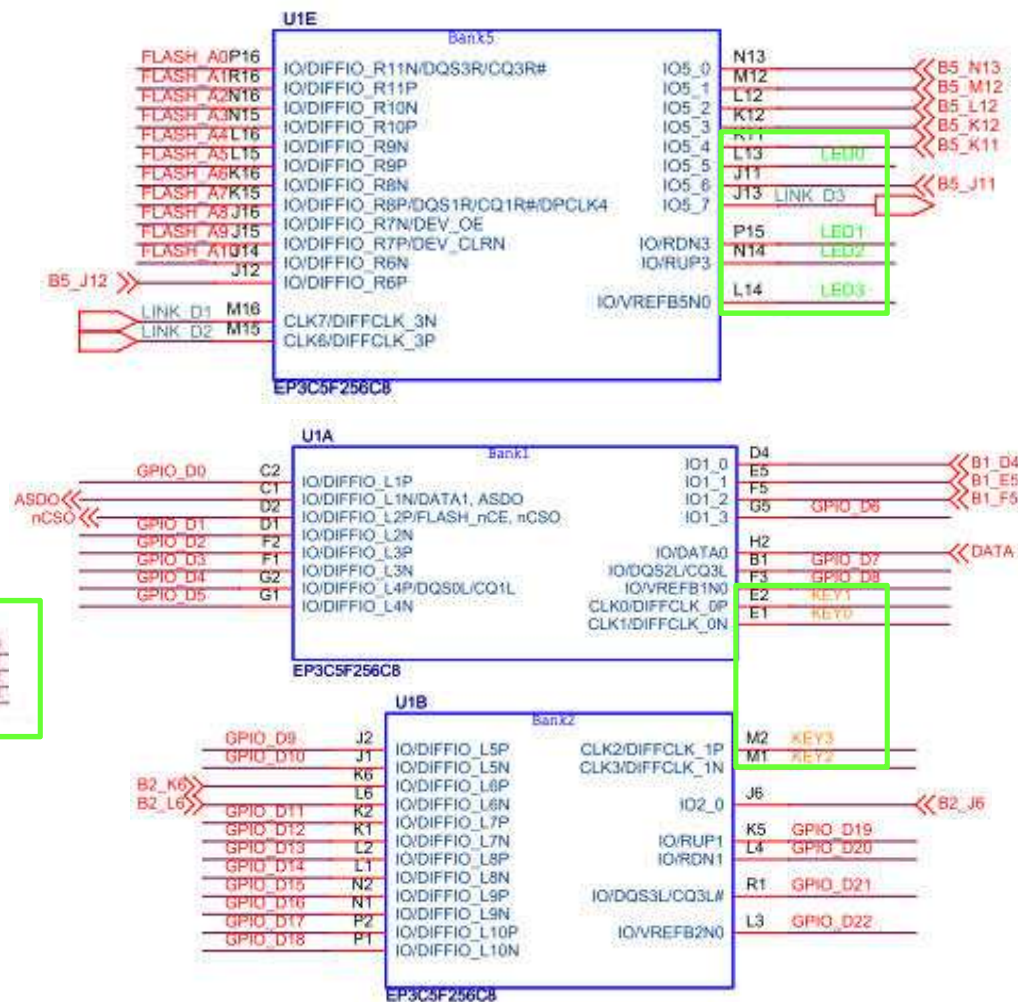
學習如何連接與操作簡單的輸入與輸出的元件到FPGA 晶片，其中輸入元件為MIAT_C3X實驗板上的開關Button1~4，輸出元件為LED1~4。

□ 實驗原理

範例一、根據開關、LED 電路圖與FPGA 腳位對照表使用提示的VHDL 程式碼將開關與LED 做連接的動作，當開關Button按下時相對應的LED 被點亮，反之LED熄滅。



FPGA Pin Name	I/O assignment
PIN_E1	User Botton1
PIN_E2	User Botton2
PIN_M1	User Botton3
PIN_M2	User Botton4
PIN_L13	User LED1
PIN_P15	User LED2
PIN_N14	User LED3
PIN_L14	User LED4





基本I/O驅動範例

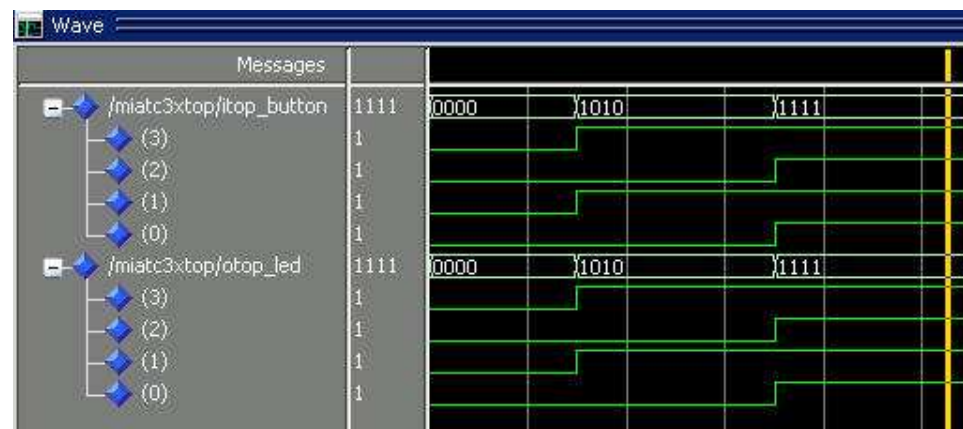
提示的VHDL程式碼(檔案路徑CDROM\MIAT_C3X_EVB_Demonstrations\TESTIO1)

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
library work;
entity MIATC3XTOP is
port(
    ...
    -- Push Button 1~4
    iTOP_BUTTON : in  std_logic_vector(3 downto 0); -- Push Button

    -- LED 1~4
    oTOP_LED : out std_logic_vector(3 downto 0);    -- LED 4 Bits
    ...
);
end MIATC3XTOP;
architecture RTL of MIATC3XTOP is
begin

    oTOP_LED <= iTOP_BUTTON;
    -- oTOP_LED(3) <= iTOP_BUTTON(3);
    -- oTOP_LED(2 downto 0) <= iTOP_BUTTON(2 downto 0);

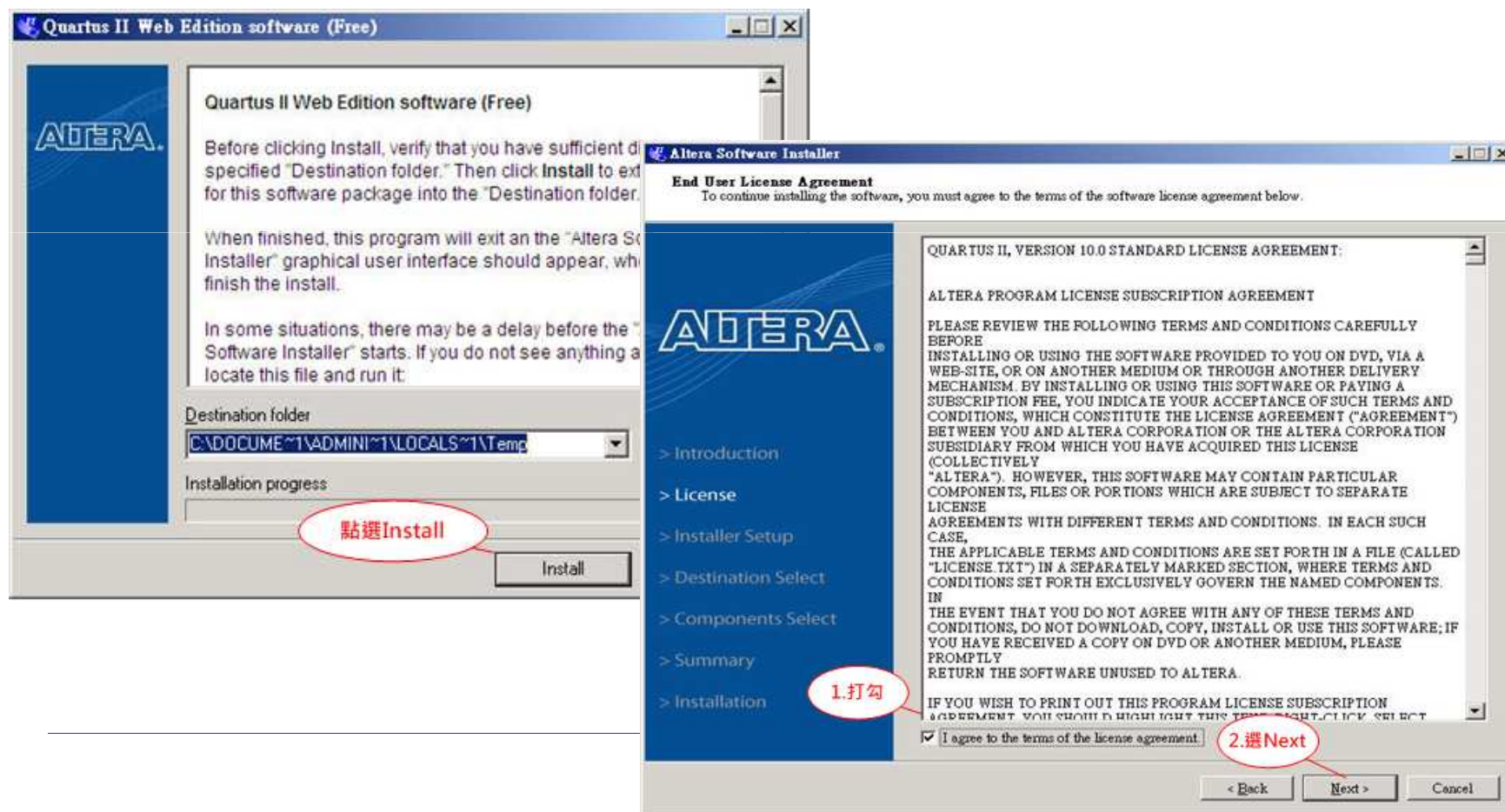
end RTL;
```





QuartusII軟體安裝

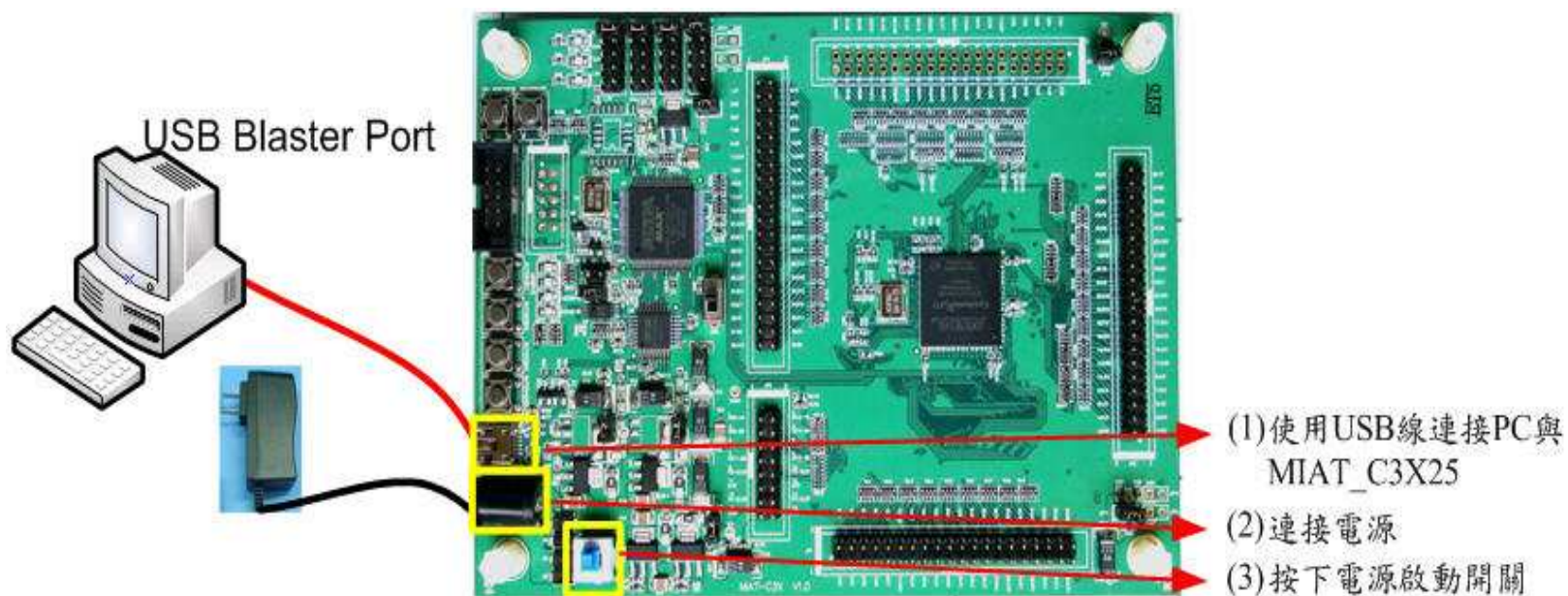
- ❑ 安裝10.0_quartus_free_windows.exe，此檔案的目錄位置在光碟內的“\Altera\”，安裝過程注意下列畫面，其他選Next與OK即可完成安裝。





MIAT_C3X實驗板安裝

□ 步驟一、將實驗板連接PC





MIAT_C3X實驗板安裝

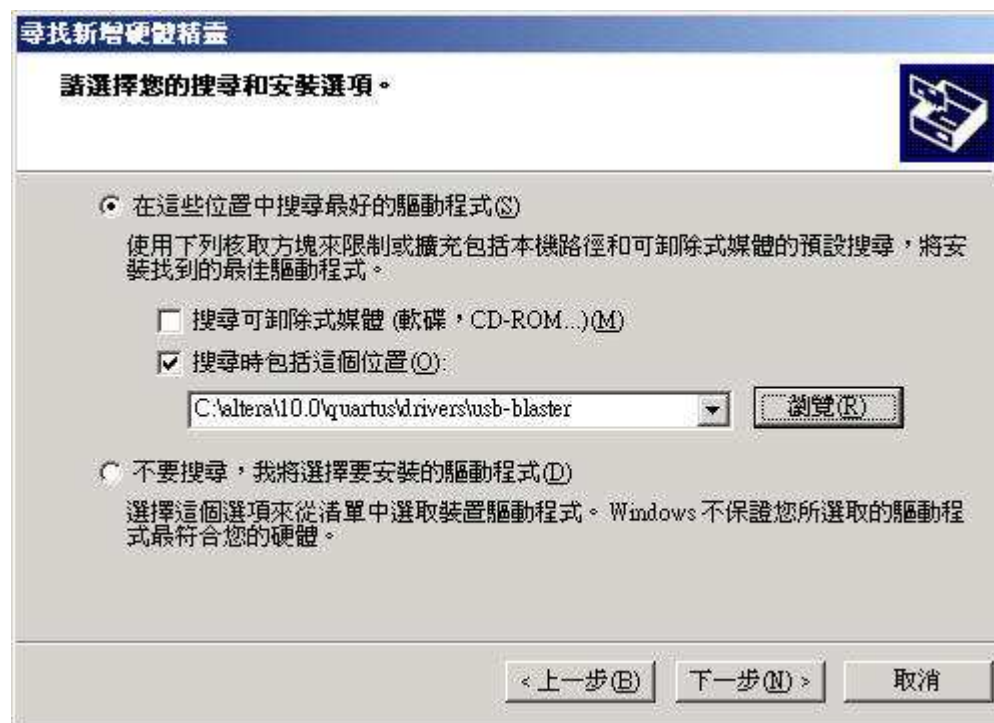
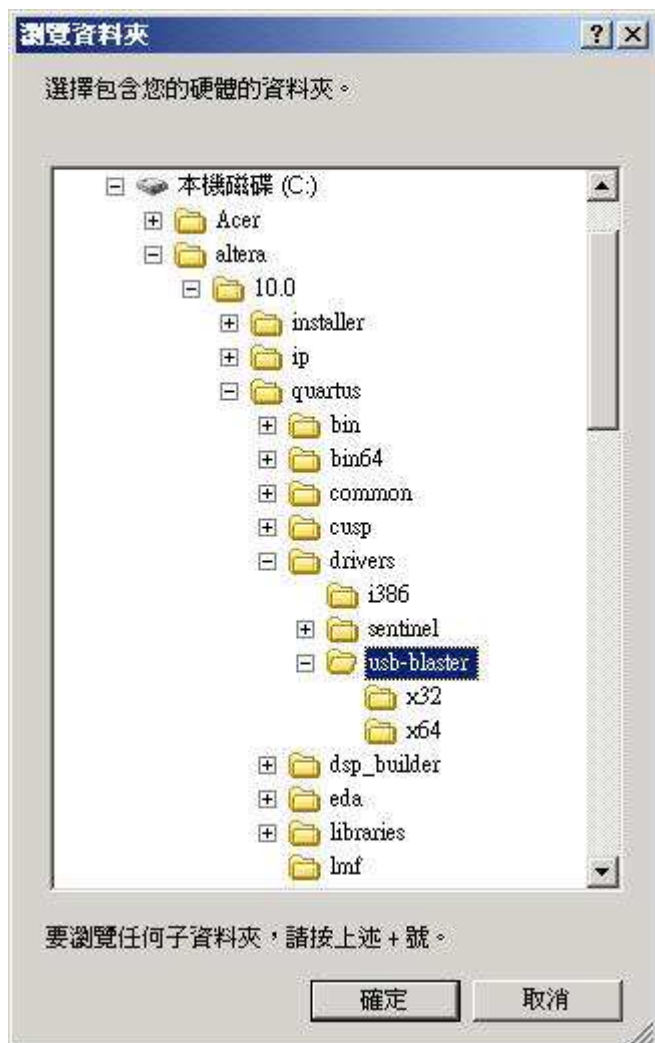
- ❑ 步驟二、驅動程式安裝，當實驗板第一次連接PC時，需安裝USB Blaster驅動程式，驅動程式目錄為C:\altera\10.0\quartus\drivers\usb-blaster。





MIAT_C3X實驗板安裝

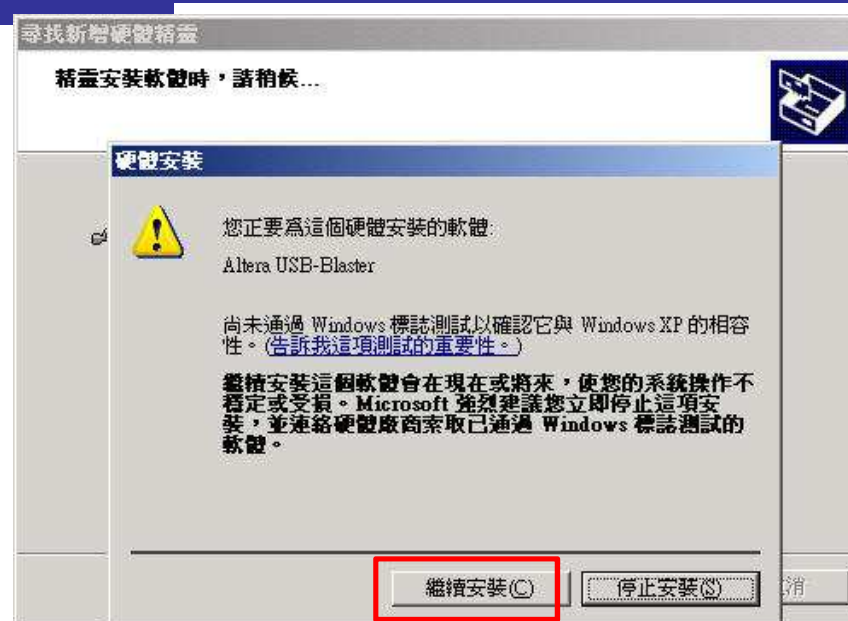
❑ 步驟二、驅動程式安裝





MIAT_C3X實驗板安裝

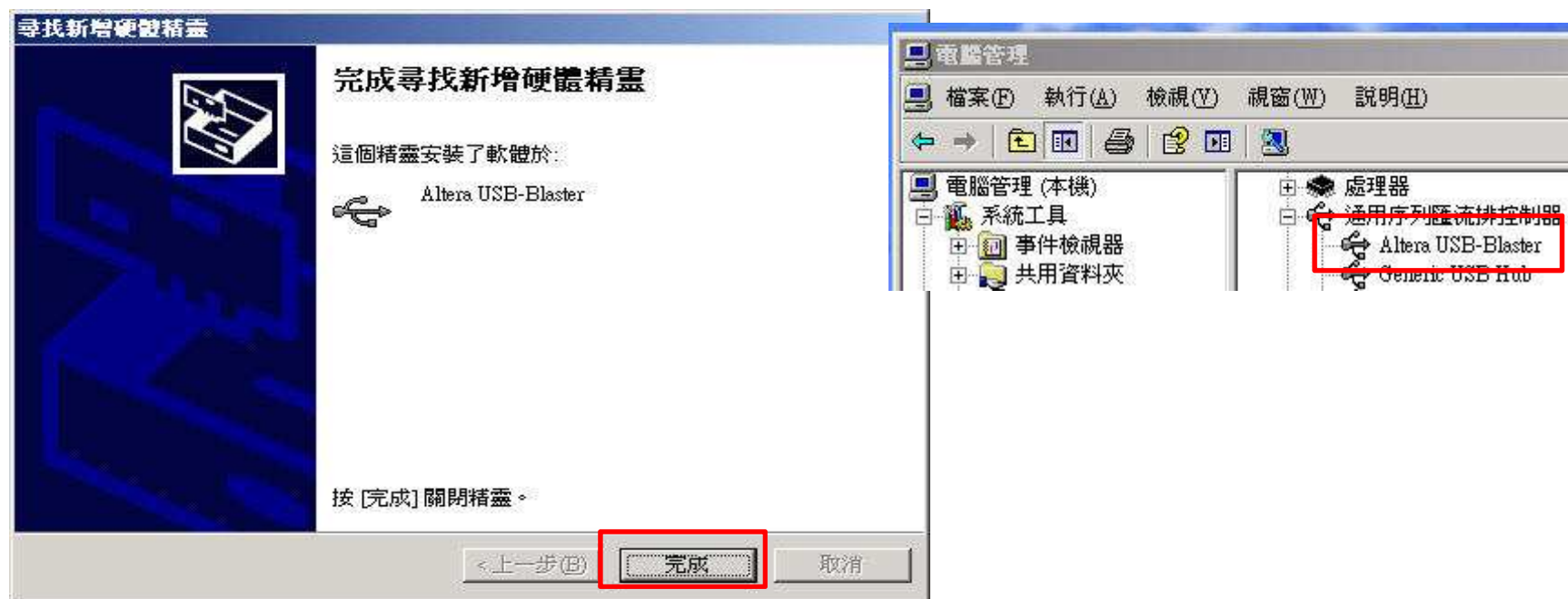
□ 步驟二、驅動程式安裝





MIAT_C3X實驗板安裝

❑ 步驟二、驅動程式安裝





QuartusII軟體使用方法

- 假設使用者已安裝QuartusII軟體工具，在此以TESTIO1為範例，目錄於CDROM\MIAT_C3X_EVB_Demonstrations\TESTIO1，設定步驟如下：
- 步驟一、在\D:建立專案目錄並複製MIATC3XTOP.vhd檔案，如下圖



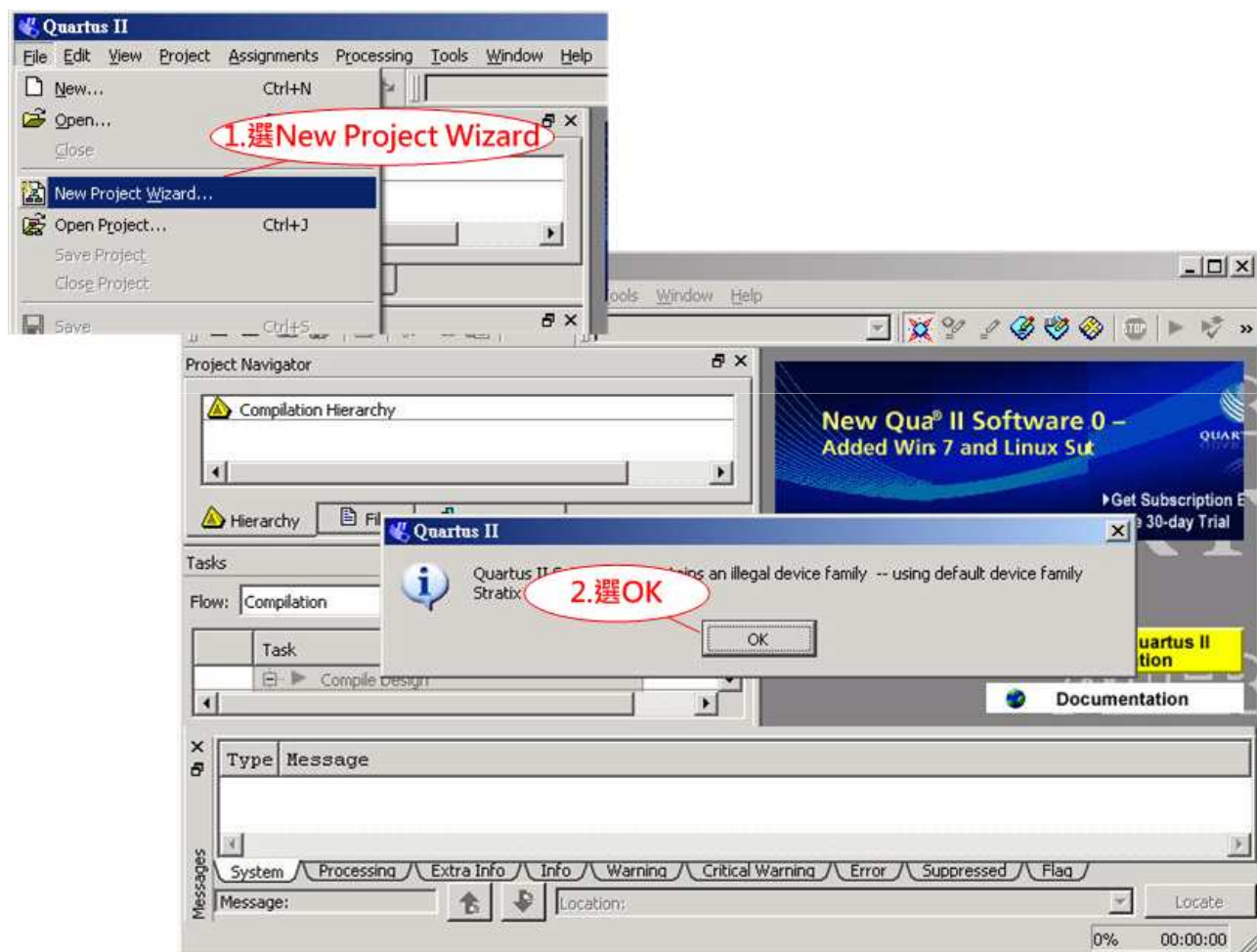
- 步驟二、執行Quartus II





Quartus II 軟體使用方法

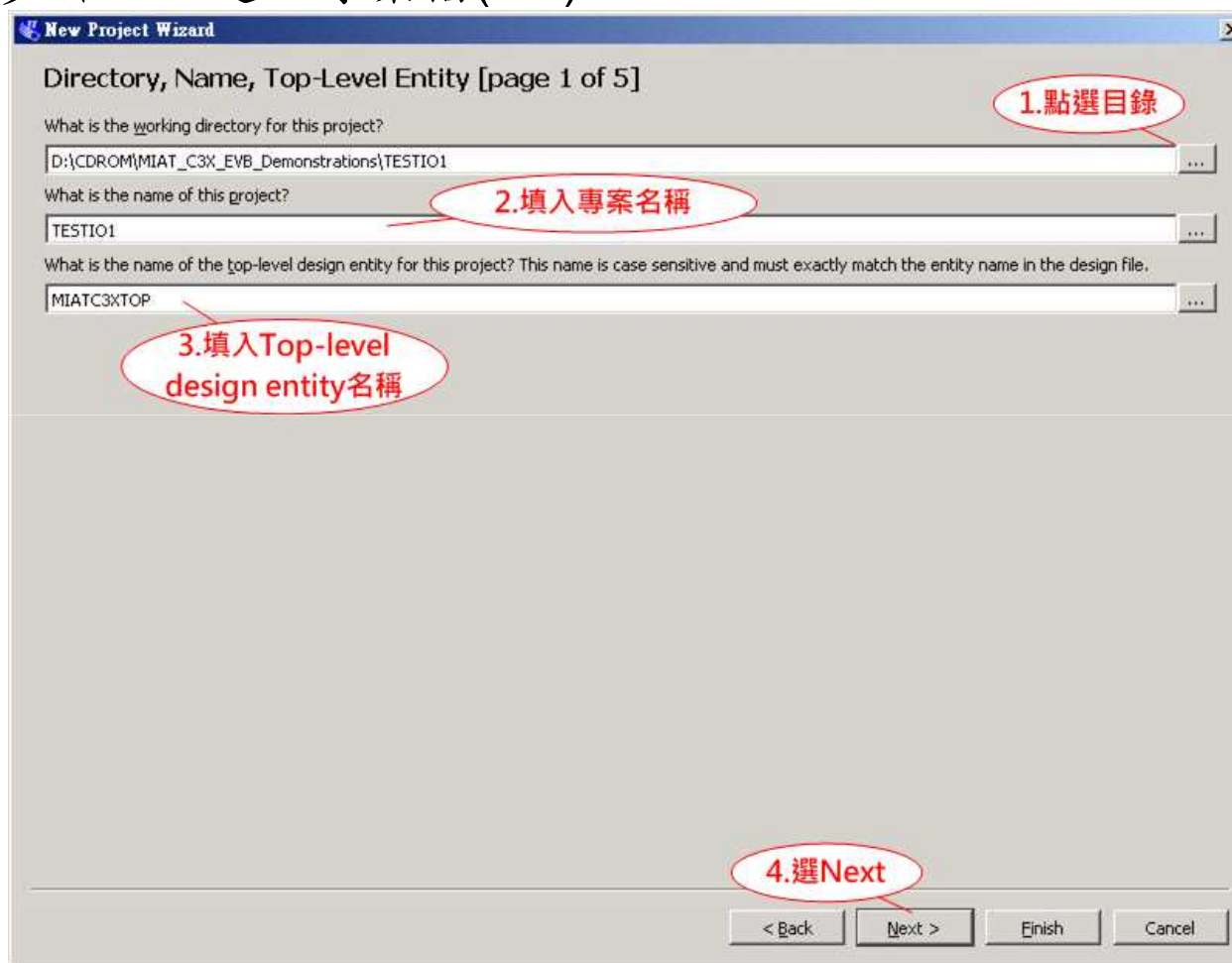
□ 步驟三、建立專案檔(1/6)





QuartusII軟體使用方法

□ 步驟三、建立專案檔(2/6)



The image shows the 'New Project Wizard' dialog box in Quartus II, specifically the 'Directory, Name, Top-Level Entity' page (page 1 of 5). The dialog box contains three text input fields and a set of navigation buttons at the bottom. Red callout boxes with numbers 1 through 4 point to specific elements: 1. '點選目錄' (Click directory) points to the first text field containing 'D:\CDROM\MIAT_C3X_EVB_Demonstrations\TESTIO1'. 2. '填入專案名稱' (Enter project name) points to the second text field containing 'TESTIO1'. 3. '填入Top-level design entity名稱' (Enter top-level design entity name) points to the third text field containing 'MIATC3XTOP'. 4. '選Next' (Select Next) points to the 'Next >' button. The buttons at the bottom are '< Back', 'Next >', 'Finish', and 'Cancel'.

Directory, Name, Top-Level Entity [page 1 of 5]

What is the working directory for this project?

D:\CDROM\MIAT_C3X_EVB_Demonstrations\TESTIO1

What is the name of this project?

TESTIO1

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

MIATC3XTOP

1. 點選目錄

2. 填入專案名稱

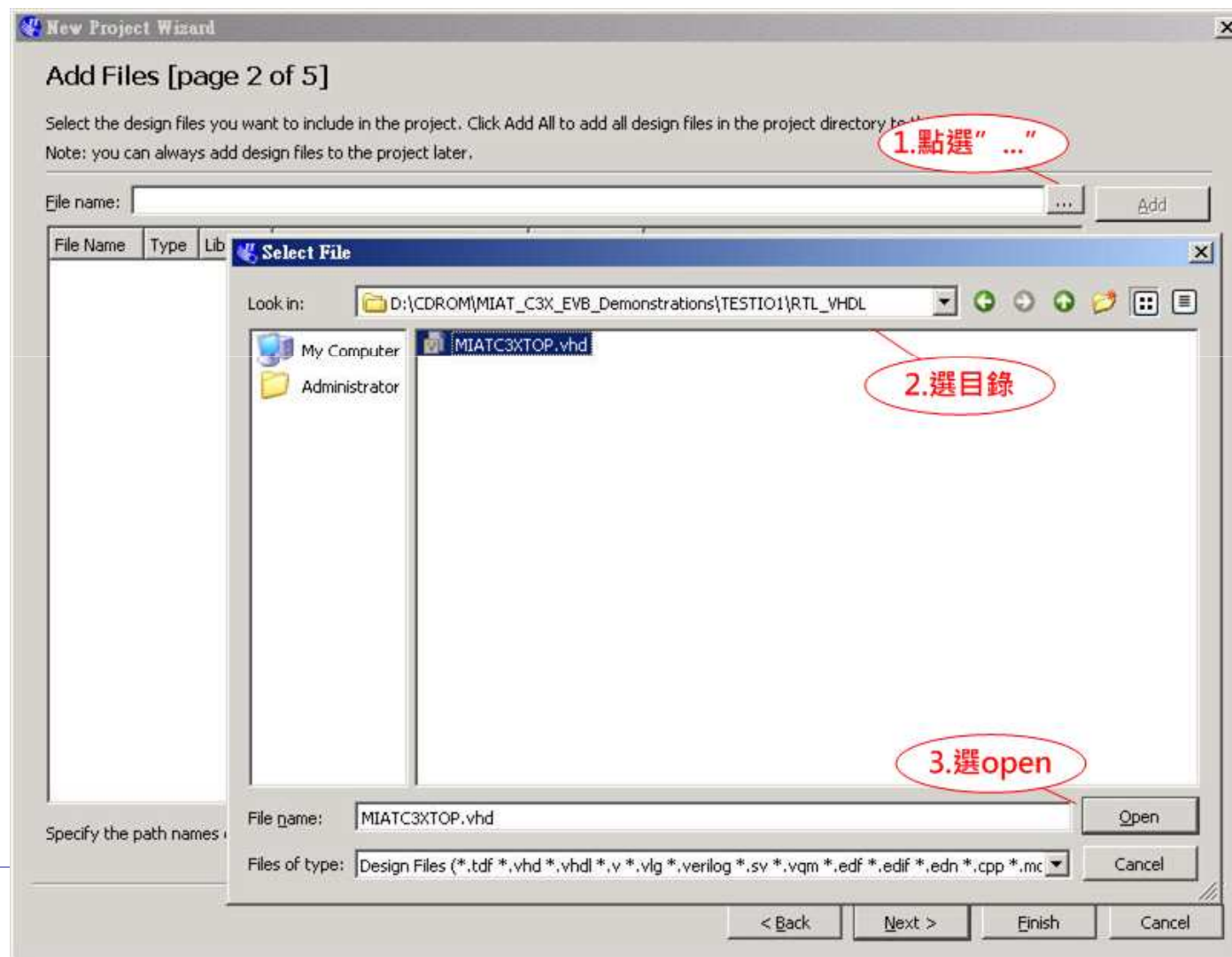
3. 填入Top-level design entity名稱

4. 選Next

< Back Next > Finish Cancel



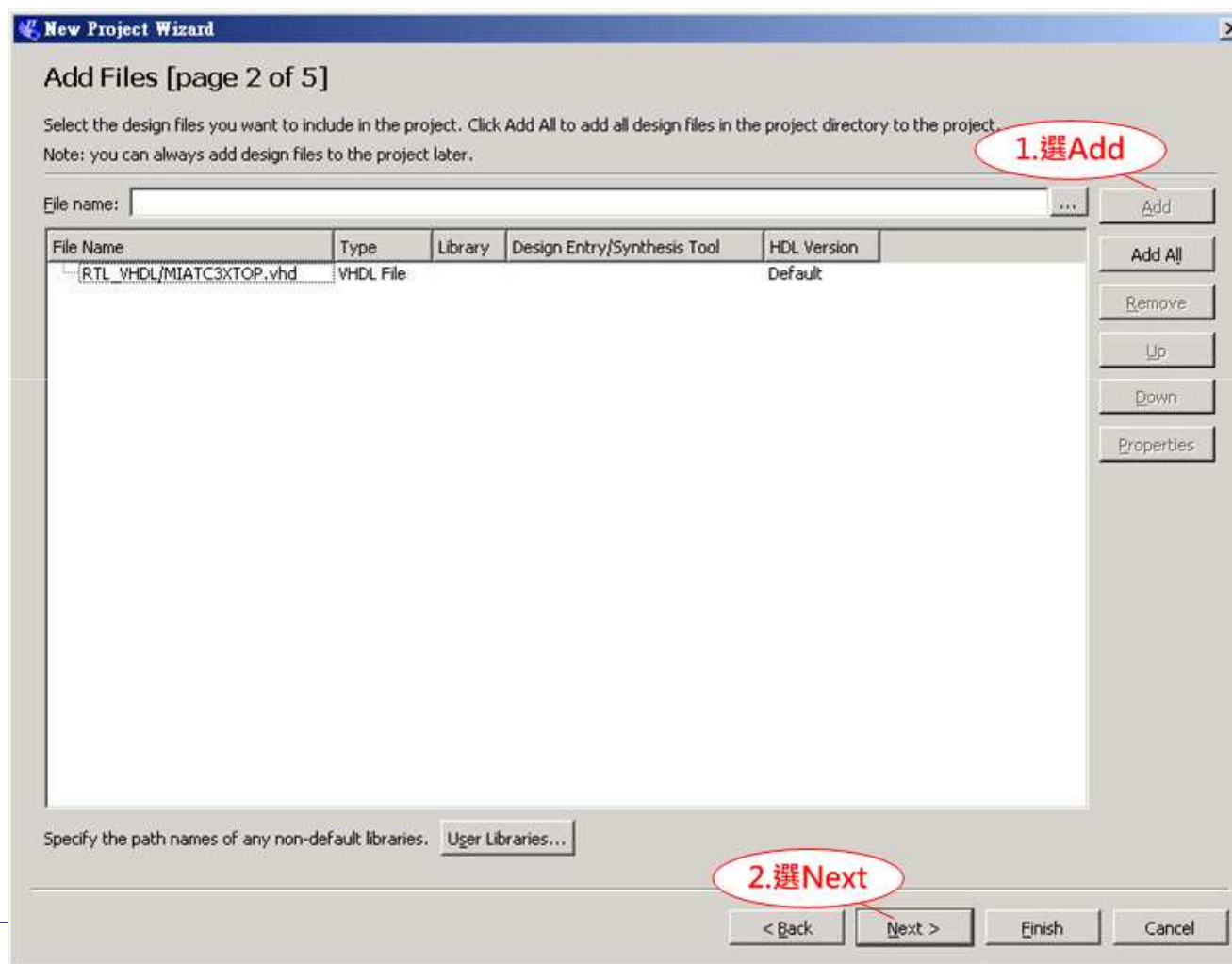
□ 步驟三、建立專案檔(3/6)





QuartusII軟體使用方法

□ 步驟三、建立專案檔(4/6)





QuartusII軟體使用方法

□ 步驟三、建立專案檔(5/6)

New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family

Family: Cyclone III

Devices: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: FBGA

Pin count: 256

Speed grade: 8

☒ Show advanced devices

☐ HardCopy compatible only

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	Glob
EP3C5F256C8	1.2V	5136	183	423936	46	2	10
EP3C10F256C8	1.2V	10320	183	423936	46	2	10
EP3C16F256C8	1.2V	15408	169	516096	112	4	20
EP3C25F256C8	1.2V	24624	157	608256	132	4	20

Companion device

HardCopy:

☐ Limit DSP & RAM to HardCopy device resources

< Back Next > Finish Cancel

1.依序選擇FPGA、256、8

2.選擇EP3C25F256C8

3.選Next



QuartusII軟體使用方法

❑ 步驟三、建立專案檔(6/6)

New Project Wizard

EDA Tool Settings [page 4 of 5]

Specify the other EDA tools used with the Quartus II software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize
Simulation	<None>	<None>	<input type="checkbox"/> Run gate-level simulation automatically
Timing Analysis	<None>	<None>	<input type="checkbox"/> Run this tool automatically after synthesis
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

1. 選Next

< Back Next >

New Project Wizard

Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory: D:/CDROM/MIAT_C3X_EVB_Demonstrations/TESTIO1

Project name: TESTIO1

Top-level design entity: MIATC3XTOP

Number of files added: 0

Number of user libraries added: 0

Device assignments:

Family name: Cyclone III

Device: EP3C25F256C8

EDA tools:

Design entry/synthesis: <None> (<None>)

Simulation: <None> (<None>)

Timing analysis: <None> (<None>)

Operating conditions:

VCCINT voltage: 1.2V

Junction temperature range: 0-85 °C

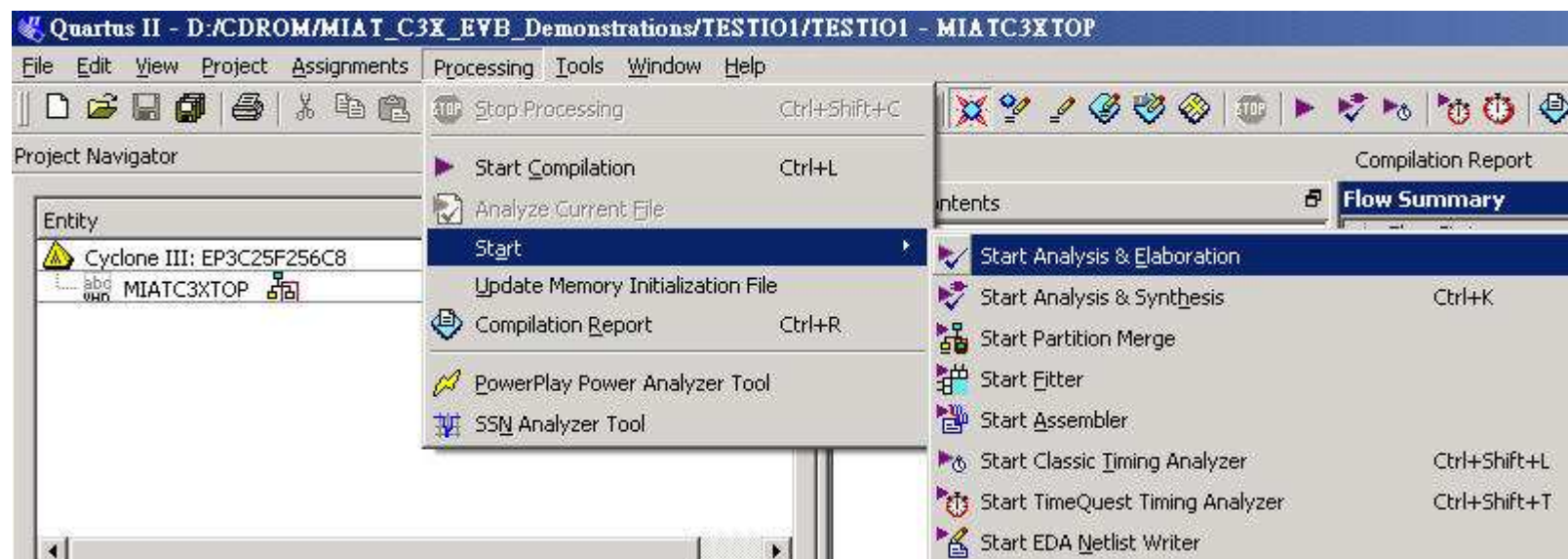
2. 選Finish

< Back Next > Finish Cancel



QuartusII軟體使用方法

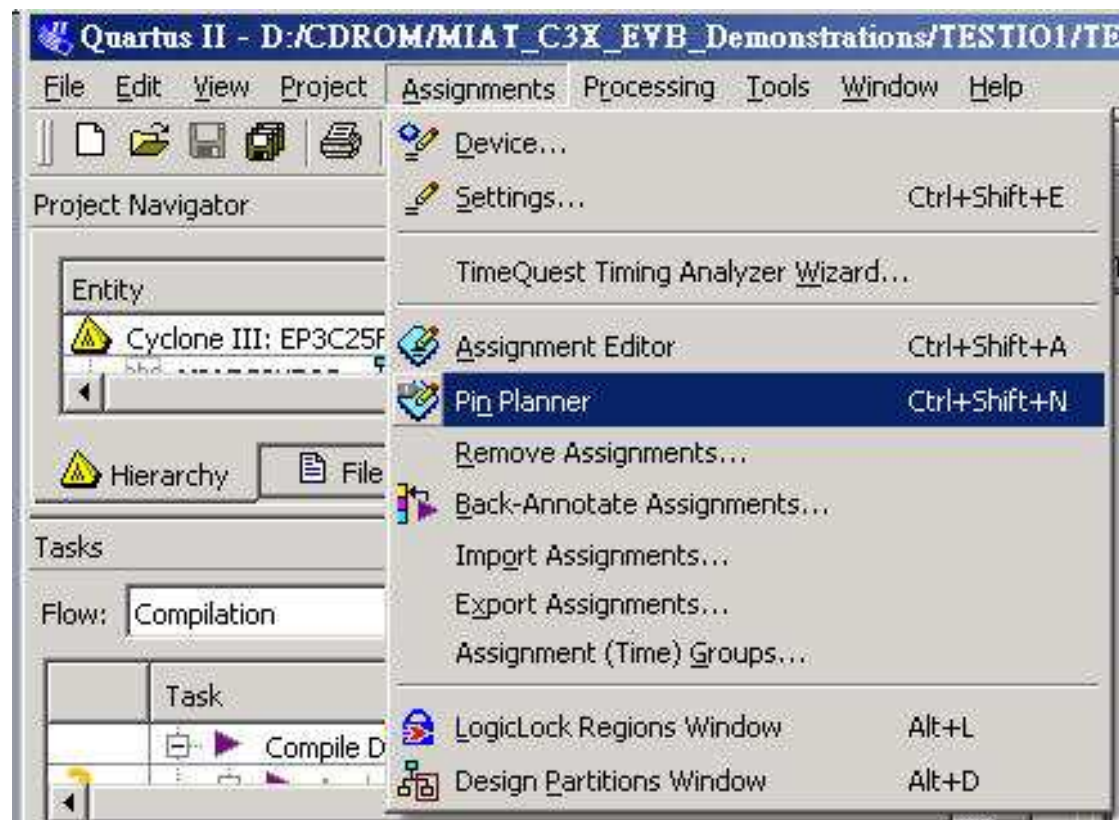
□ 步驟四、執行Analysis & Elaboration





QuartusII軟體使用方法

□ 步驟五、執行Pin Planner





QuartusII軟體使用方法

□ 步驟五、執行Pin Planner

Pin Planner - D:\CDROM\MIAT_C3X_EVB_Demonstrations\TESTIO1\TESTIO1 - MIATC3X.TOP

File Edit View Processing Tools Window

Groups

Named: *

1. 選3.3-VLVTTL

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard
ITOP_BUTTON[3..0]	Input Group				3.3-V LVTTTL
ITOP_BUTTON[3]	Input	PIN_M2	2	B2_N0	3.3-V LVTTTL
ITOP_BUTTON[2]	Input	PIN_M1	2	B2_N0	3.3-V LVTTTL
ITOP_BUTTON[1]	Input	PIN_E2	1	B1_N0	3.3-V LVTTTL
ITOP_BUTTON[0]	Input	PIN_E1	1	B1_N0	3.3-V LVTTTL
oTOP_LED[3..0]	Output Group				3.3-V LVTTTL
oTOP_LED[3]	Output	PIN_L14	5	B5_N0	3.3-V LVTTTL
oTOP_LED[2]	Output	PIN_N14	5	B5_N0	3.3-V LVTTTL
oTOP_LED[1]	Output	PIN_P15	5	B5_N0	3.3-V LVTTTL
oTOP_LED[0]	Output	PIN_L13	5	B5_N0	3.3-V LVTTTL
<<new group>>					

Top View - Wire Bond
Cyclone III - EP3C25F256C8

2. 設定PIN Name

Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
ITOP_BUTTON[3]	Input	PIN_M2	2	B2_N0	3.3-V LVTTTL	
ITOP_BUTTON[2]	Input	PIN_M1	2	B2_N0	3.3-V LVTTTL	
ITOP_BUTTON[1]	Input	PIN_E2	1	B1_N0	3.3-V LVTTTL	
ITOP_BUTTON[0]	Input	PIN_E1	1	B1_N0	3.3-V LVTTTL	
oTOP_LED[3]	Output	PIN_L14	5	B5_N0	3.3-V LVTTTL	
oTOP_LED[2]	Output	PIN_N14	5	B5_N0	3.3-V LVTTTL	
oTOP_LED[1]	Output	PIN_P15	5	B5_N0	3.3-V LVTTTL	
oTOP_LED[0]	Output	PIN_L13	5	B5_N0	3.3-V LVTTTL	
<<new node>>						

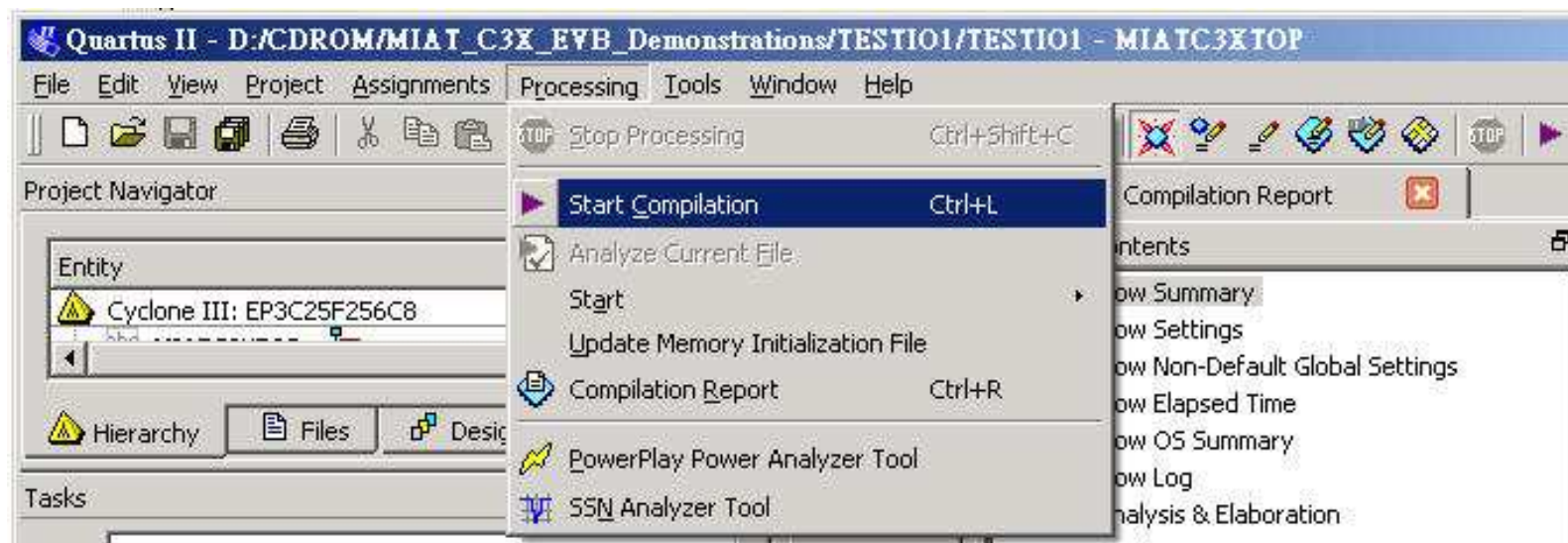
Filter: Pins: all

100% 00:00:13



QuartusII軟體使用方法

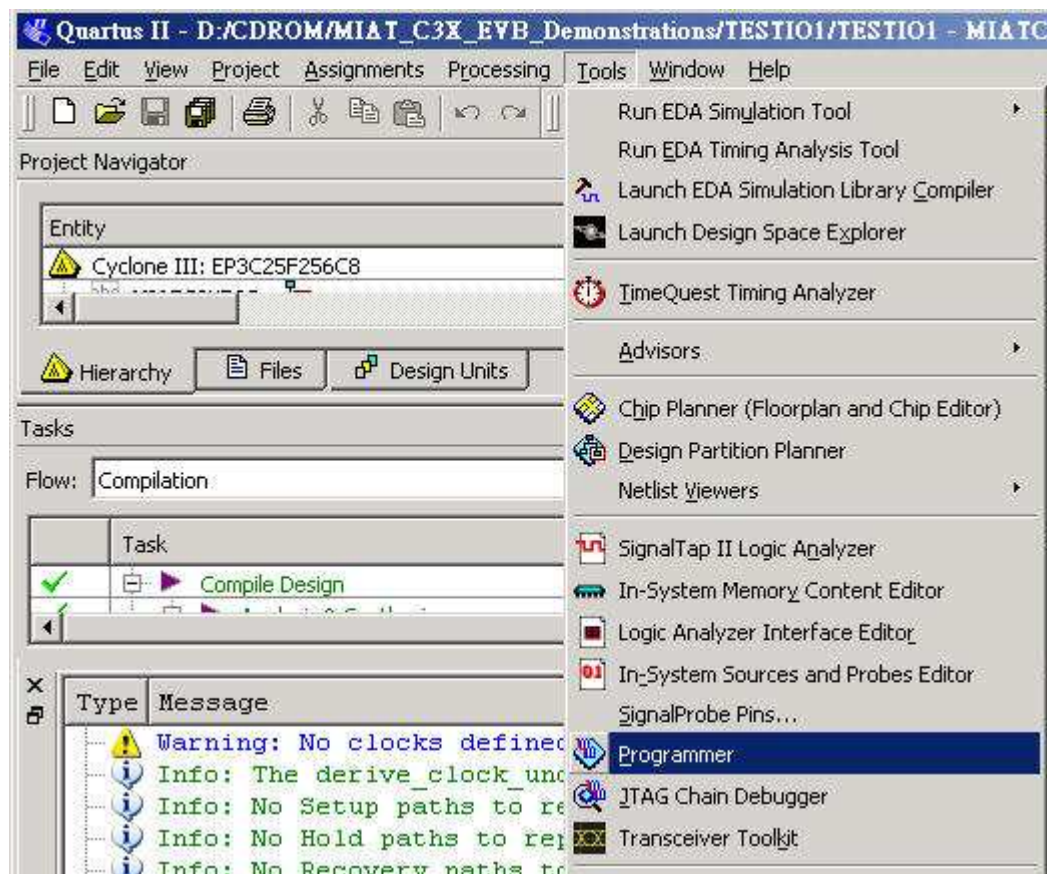
□ 步驟六、執行Start Compilation





QuartusII軟體使用方法

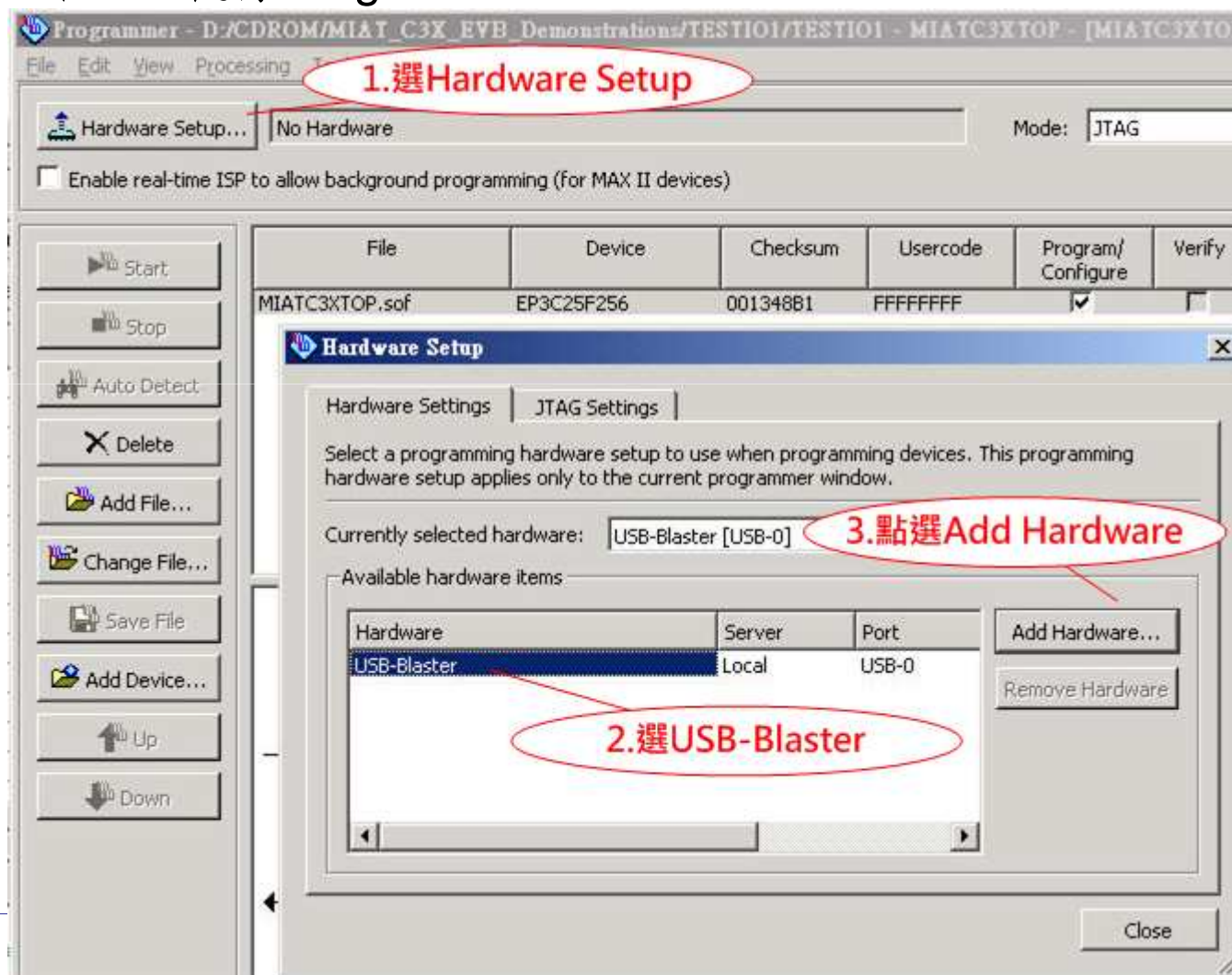
❑ 步驟七、執行Programmer





QuartusII軟體使用方法

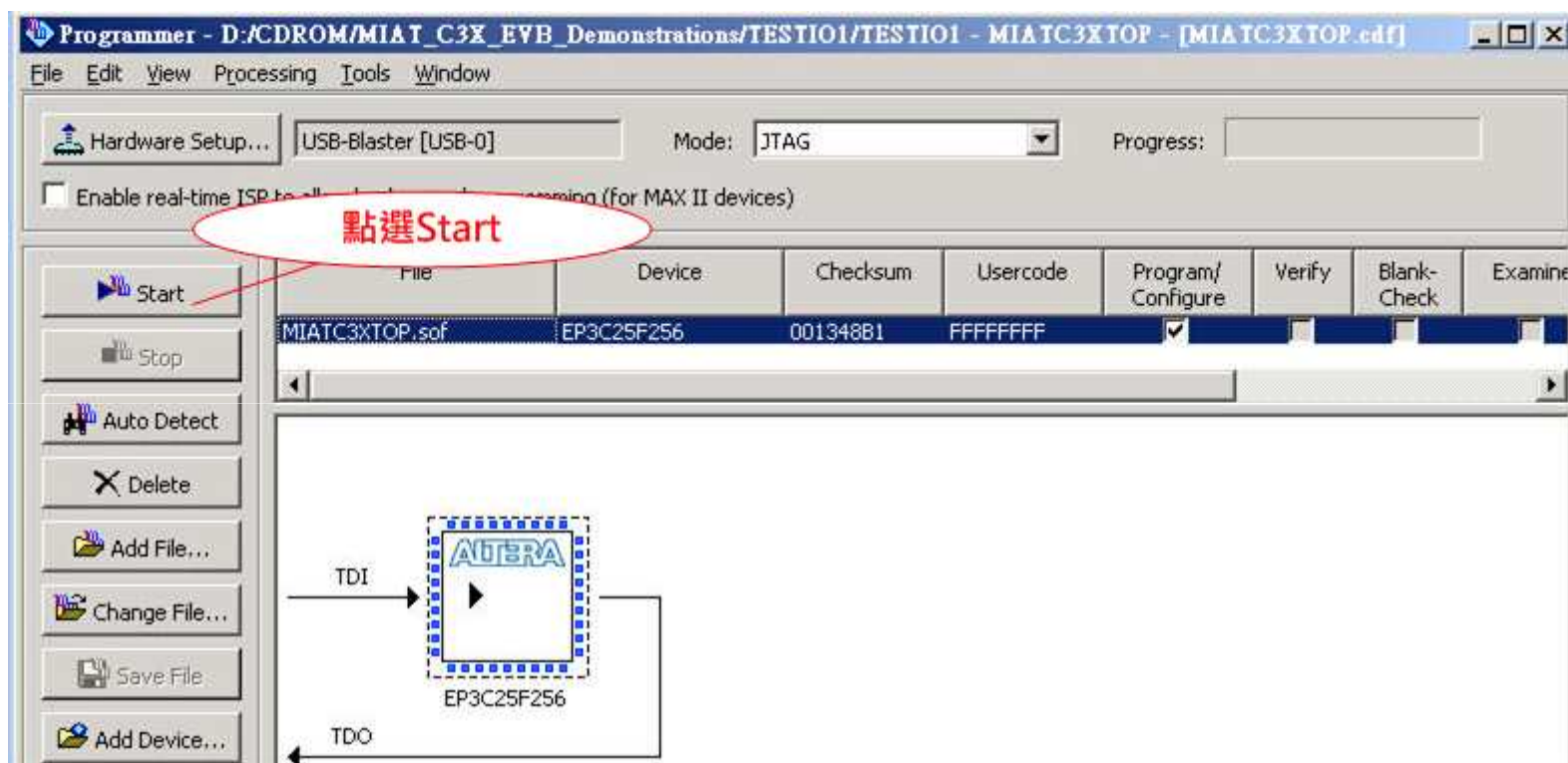
□ 步驟七、執行Programmer





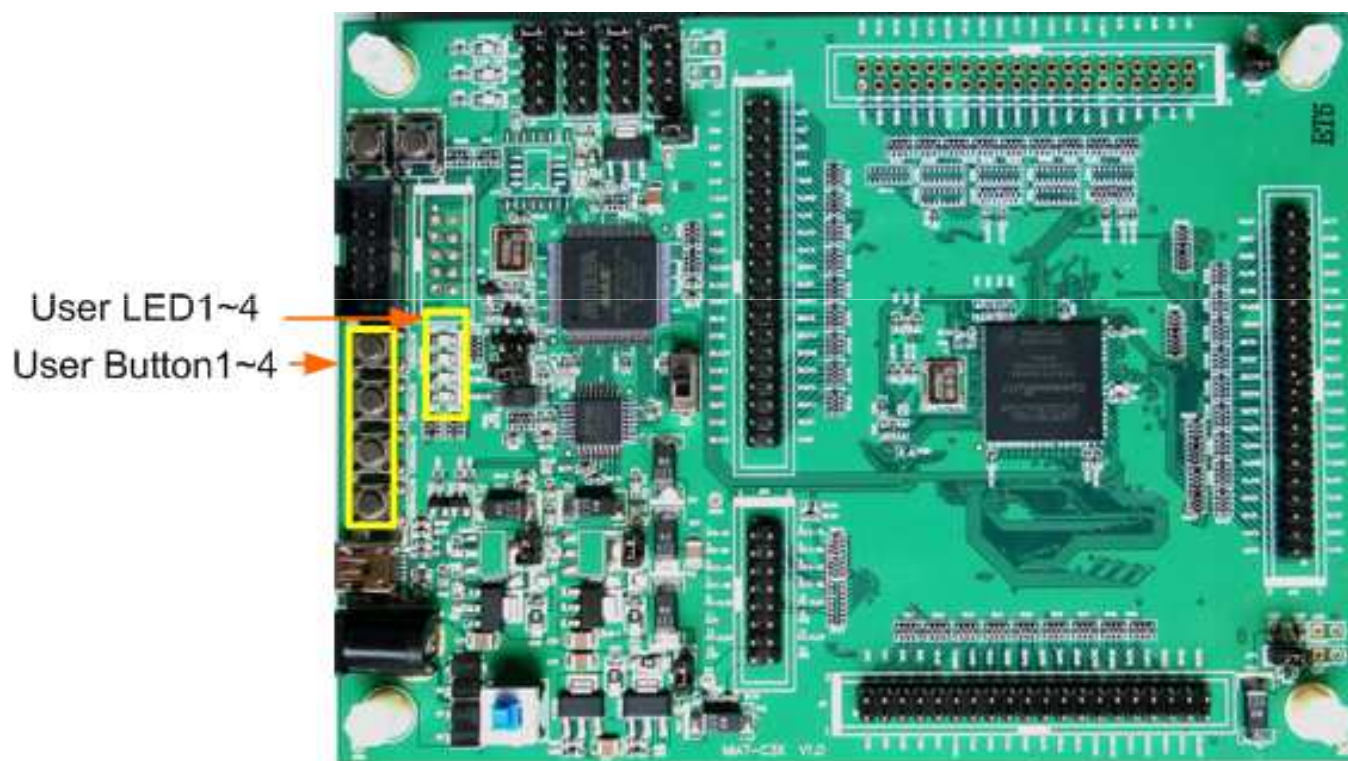
QuartusII軟體使用方法

□ 步驟七、執行Programmer





- ❑ 步驟八、測試實驗板之Button與LED動作是否正確，當開關Button按下時相對應的LED被點亮，反之LED熄滅。





練習一、開發流程練習

□ 步驟一、修改程式碼如下

begin

```
--oTOP_LED <= iTOP_BUTTON;
```

```
oTOP_LED(3) <= iTOP_BUTTON(3);
```

```
oTOP_LED(2 downto 0) <= iTOP_BUTTON(2 downto 0);
```

end RTL;

步驟二、重新編譯與燒錄至實驗板後重新執行，觀察是否為預期之結果。

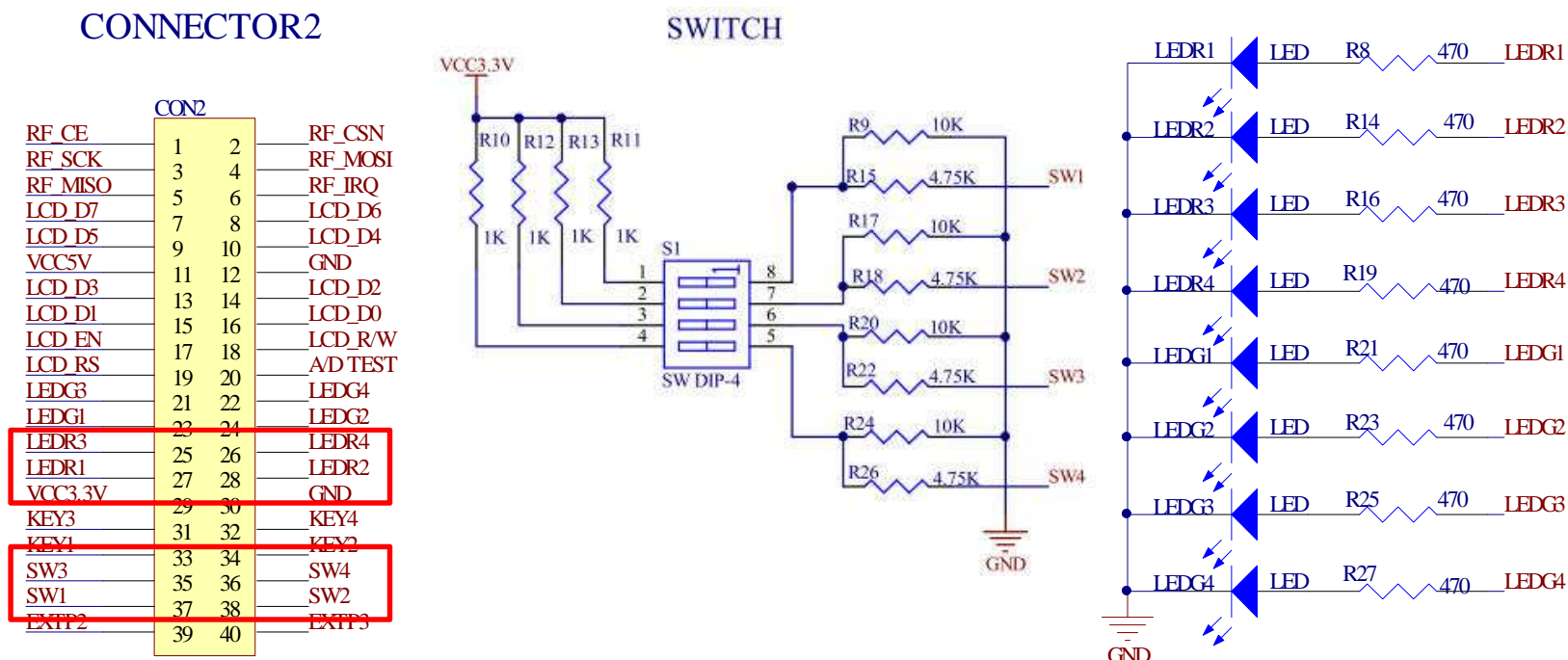


練習二、電路設計修改

□ 步驟一、硬體電路配置

將練習一之Button1~4與LED1~4改由IOB子板之周邊I/O電路
SW1~4與LEDR1~4取代。使用SW控制LEDR之閃爍功能。

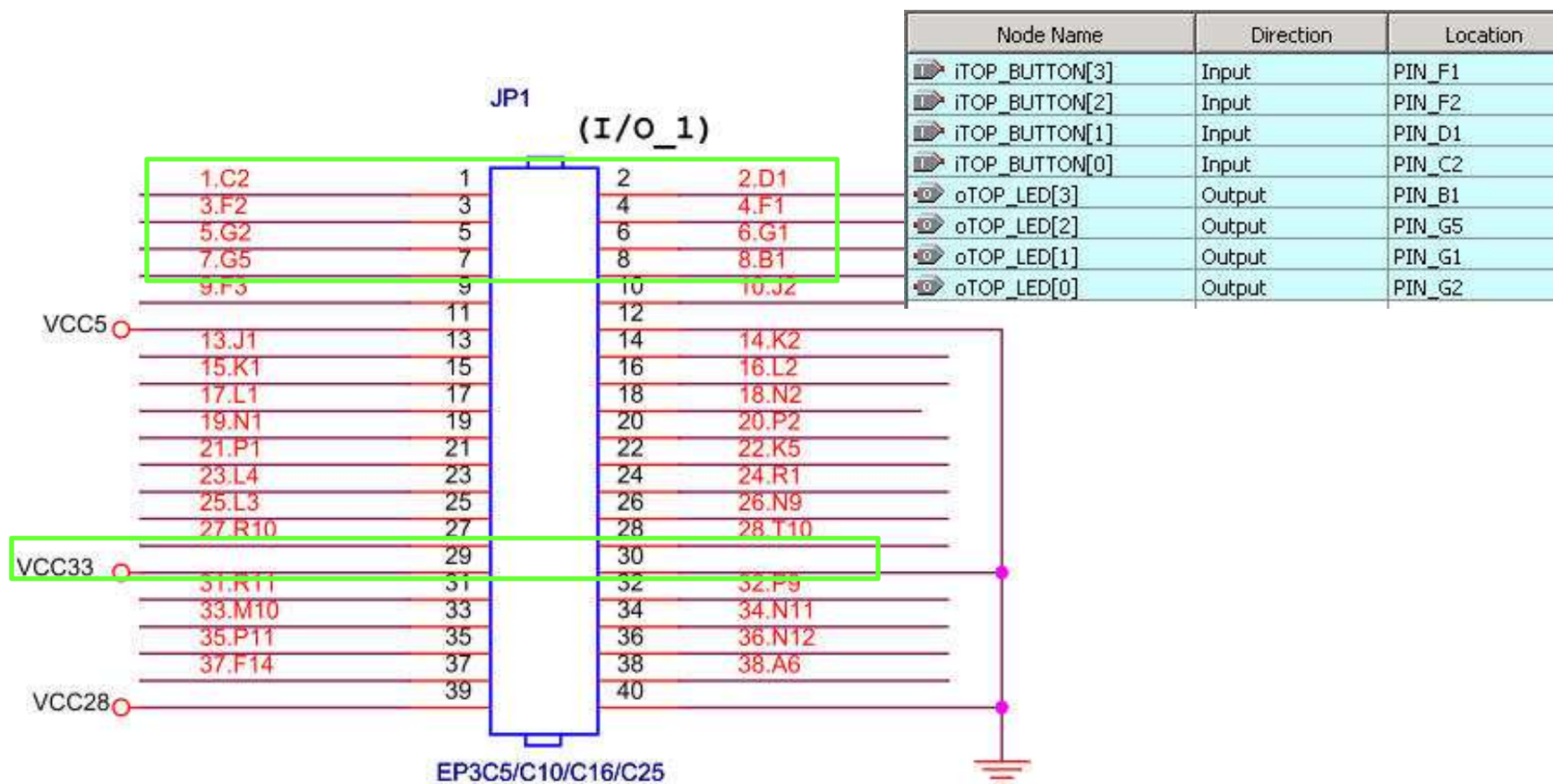
□ MIAT_IOB之SW與LED之電路圖





練習二、電路設計修改

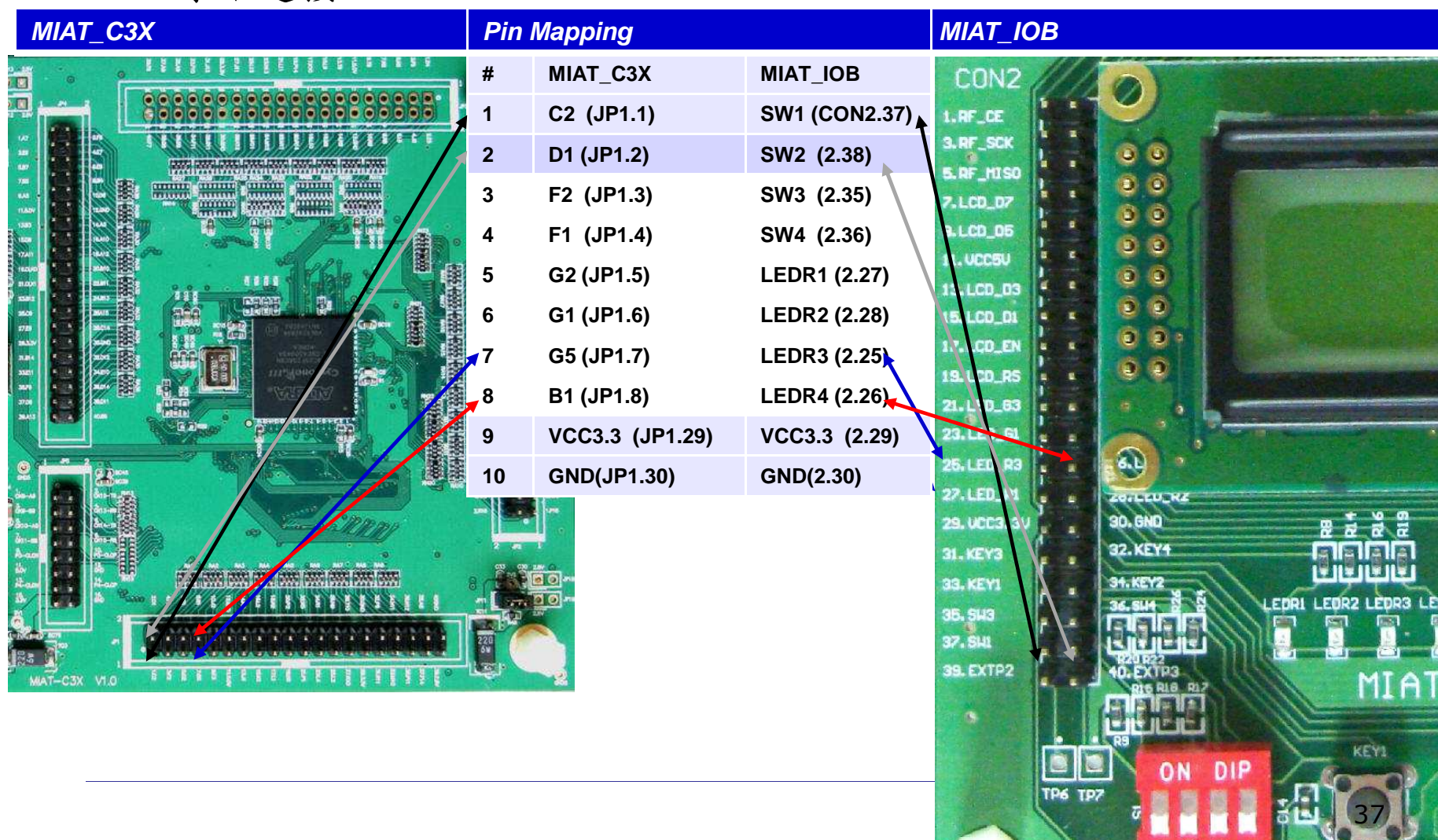
□ MIAT_C3X 之JP1電路圖





練習二、電路設計修改

□ 線路連接



Q & A



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