ARM Cortex-M3之架構與原理介紹

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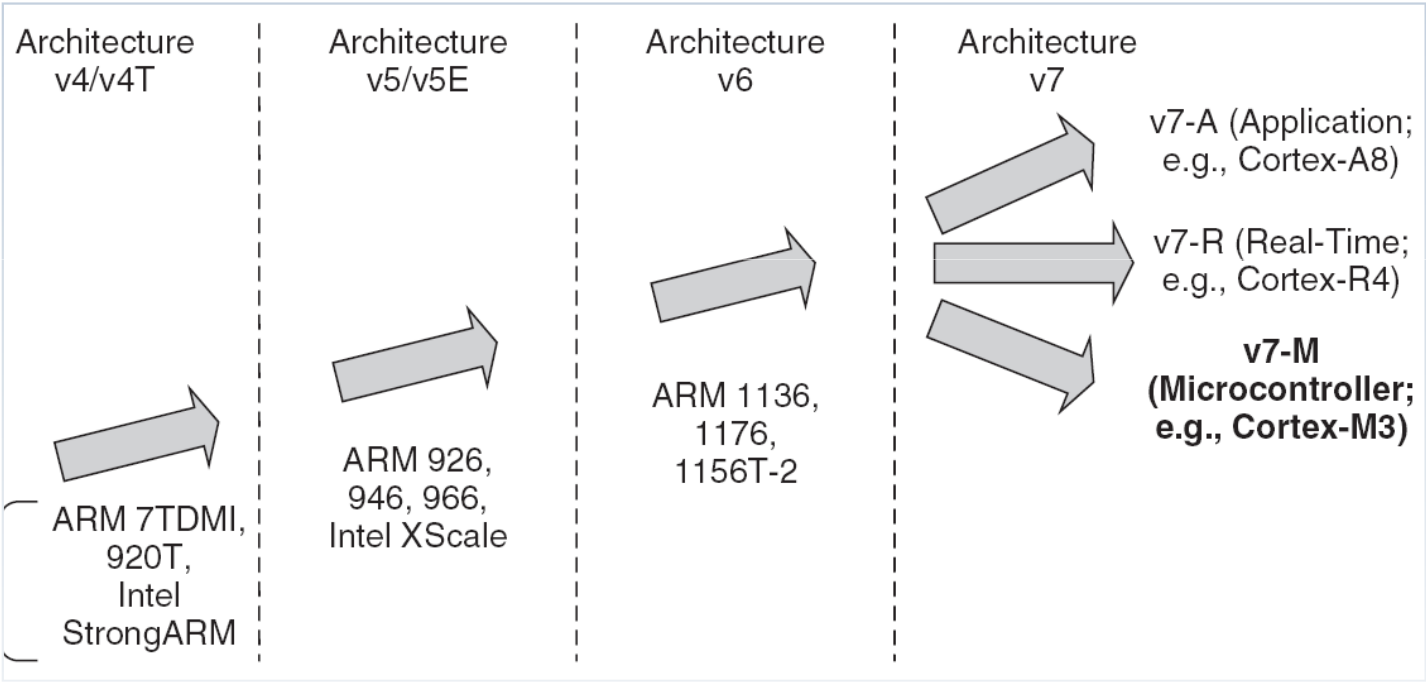
Outline

- ARM 處理器簡介
- ARM Cortex-M3處理器架構與原理介紹
- ARM Cortex-M3處理器之應用

ARM 處理器簡介

- ARM是Advanced RISC Machine的縮寫，意為高級精簡指令集計算機。是一個32位元精簡指令集（RISC）處理器架構，主要設計目標為低耗電、低成本與高效能的特性，其廣泛地使用在許多嵌入式系統設計。



Evolution of ARM Architecture

ARM 處理器簡介

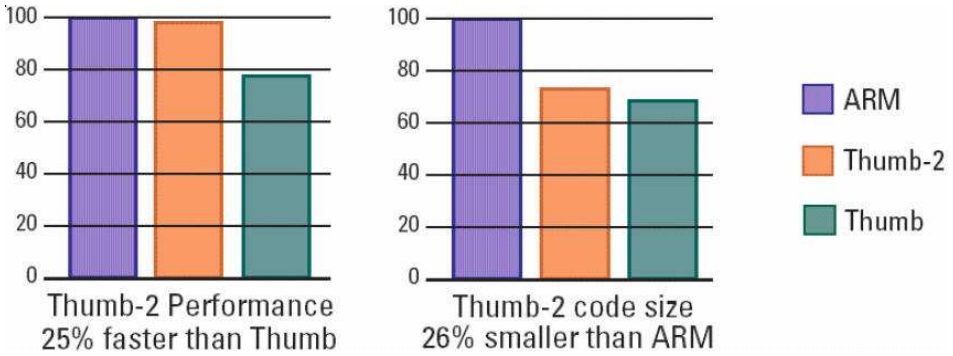
Family	Architecture Version	Example Core	Feature	Clock Rate	MIPS / MHz	Application
ARM7TDMI	ARMv4T	ARM7TDMI(-S)	3-stage pipeline, Thumb	66~80MHz	0.9MIPS	Nintendo DS, iPod, Lego NXT,Samsung S3C4510B
ARM9E	ARMv5TEJ	ARM926EJ-S	5-stage pipeline,Thumb, Jazelle DBX, Enhanced DSP instructions	200MHz	1.1MIPS	Texas Instruments OMAP1710, Qualcomm MSM6100,Samsung S3C2412
ARM11	ARMv6	ARM1136J(F)-S	8-stage pipeline, SIMD, Thumb, Jazelle DBX, (VFP)	450~665MHz	2.1MIPS	Texas Instruments OMAP2420,2430, Qualcomm MSM7201A, 7200A
Cortex	ARMv7-A	Cortex-A8	Application profile, VFP, NEON, Jazelle RCT, Thumb-2, 13-stage superscalar pipeline	600MHz~1 GHz	2.0DMIPS	Texas Instruments OMAP3xxx series
Cortex	ARMv7-M	Cortex-M3	3-stage pipeline, Microcontroller profile, Thumb-2.	72~100MHz	1.25DMIPS	Luminary Micro microcontroller family, ST Microelectronics STM32, NXP Semiconductors LPC1700

ARM 處理器簡介

- ARM7TDMI-S and Cortex-M3 comparison (100MHz frequency on TSMC 0.18G)

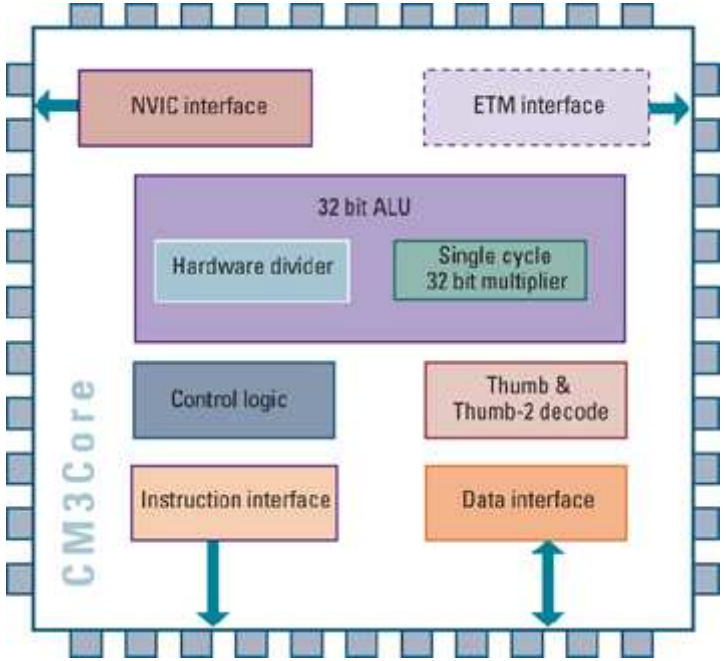
Features	ARM7TDMI-S	Cortex-M3
Architecture	ARMv4T (von Neumann)	ARMv7-M (Harvard)
ISA Support	Thumb / ARM	Thumb / Thumb-2
Pipeline	3-Stage	3-Stage + branch speculation
Interrupts	FIQ / IRQ	NMI + 1 to 240 Physical Interrupts
Interrupt Latency	24-42 Cycles	12 Cycles
Sleep Modes	None	Integrated
Memory Protection	None	8 region Memory Protection Unit
Dhrystone	0.95 DMIPS/MHz (ARM mode)	1.25 DMIPS/MHz
Power Consumption	0.28mW/MHz	0.19mW/MHz
Area	0.62mm2 (Core Only)	0.86mm2 (Core & Peripherals)*

- Thumb-2 技術首見於 ARM1156 核心，並於2003年發表。Thumb-2 擴充了受限的 16-bit Thumb 指令集，以額外的 32-bit 指令讓指令集的使用更廣泛。因此 Thumb-2 的預期目標是要達到近乎 Thumb 的編碼密度，但能表現出近乎 ARM 指令集在 32-bit 記憶體下的效能。



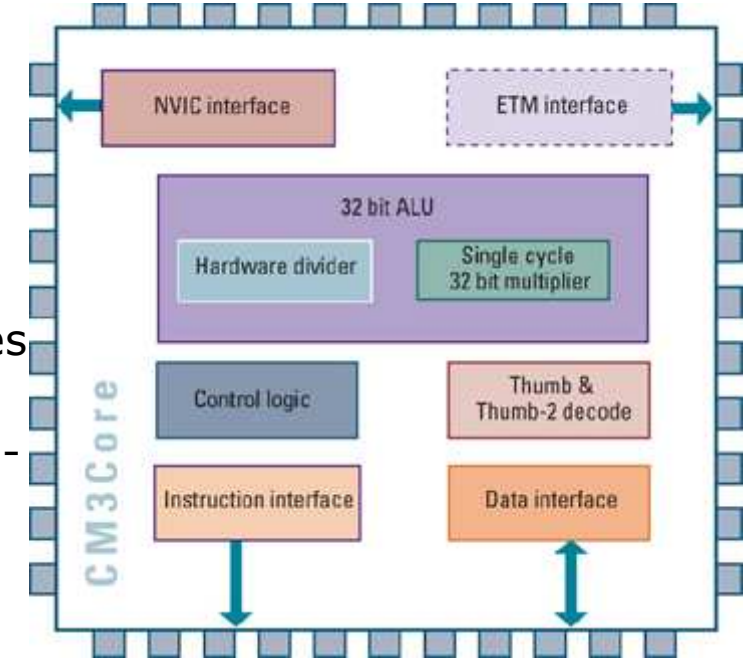
ARM Cortex-M3架構

- ARMv7-M architecture
  - Optimized for microcontroller and low-cost applications
- Harvard architecture
  - separate instruction and data buses
- RISC(Reduced Instruction Set Computing)
- Many operations in parallel
- 3 stages pipelined with branch speculation:
  - Instruction Fetch, Instruction Decode and Instruction Execute



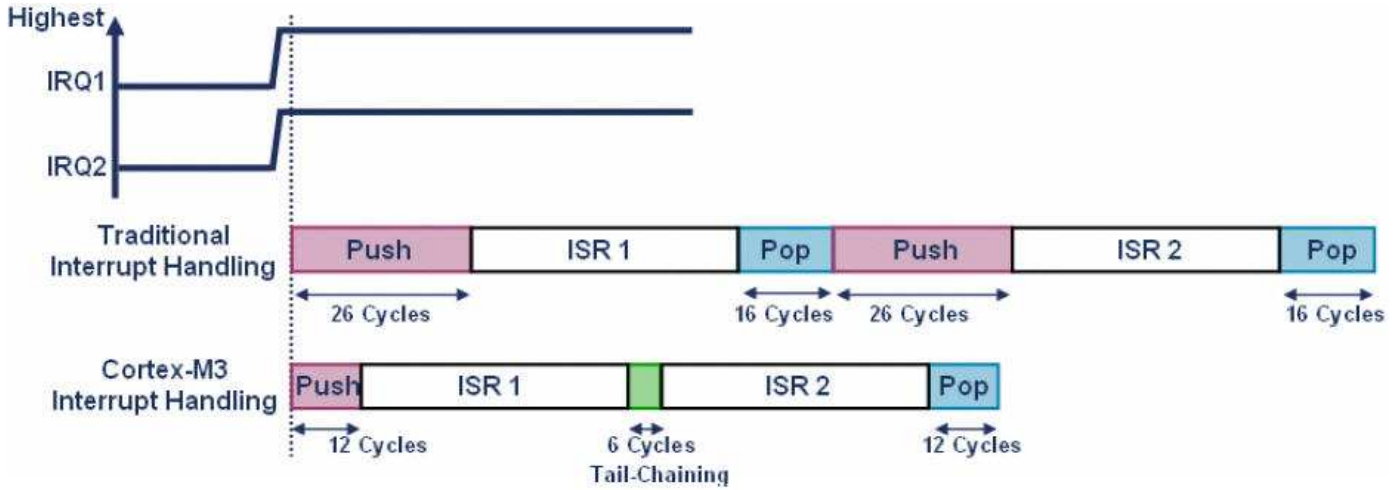
ARM Cortex-M3架構

- Nested Vectored Interrupt Controller (NVIC)
  - Configurable from 1-240 physical interrupts; up to 256 levels of priority
  - Non-Maskable Interrupt (NMI) enables critical interrupt capabilities
  - Low latency through tail chaining, late arrival service & stack pop pre-emption
  - Nesting (stacking) of interrupts
  - Dynamic interrupt reprioritization
- Single cycle multiply and hardware divide instructions
  - 32-bit multiplication in a single cycle
  - Signed and unsigned divide operations between 2 and 12 cycles



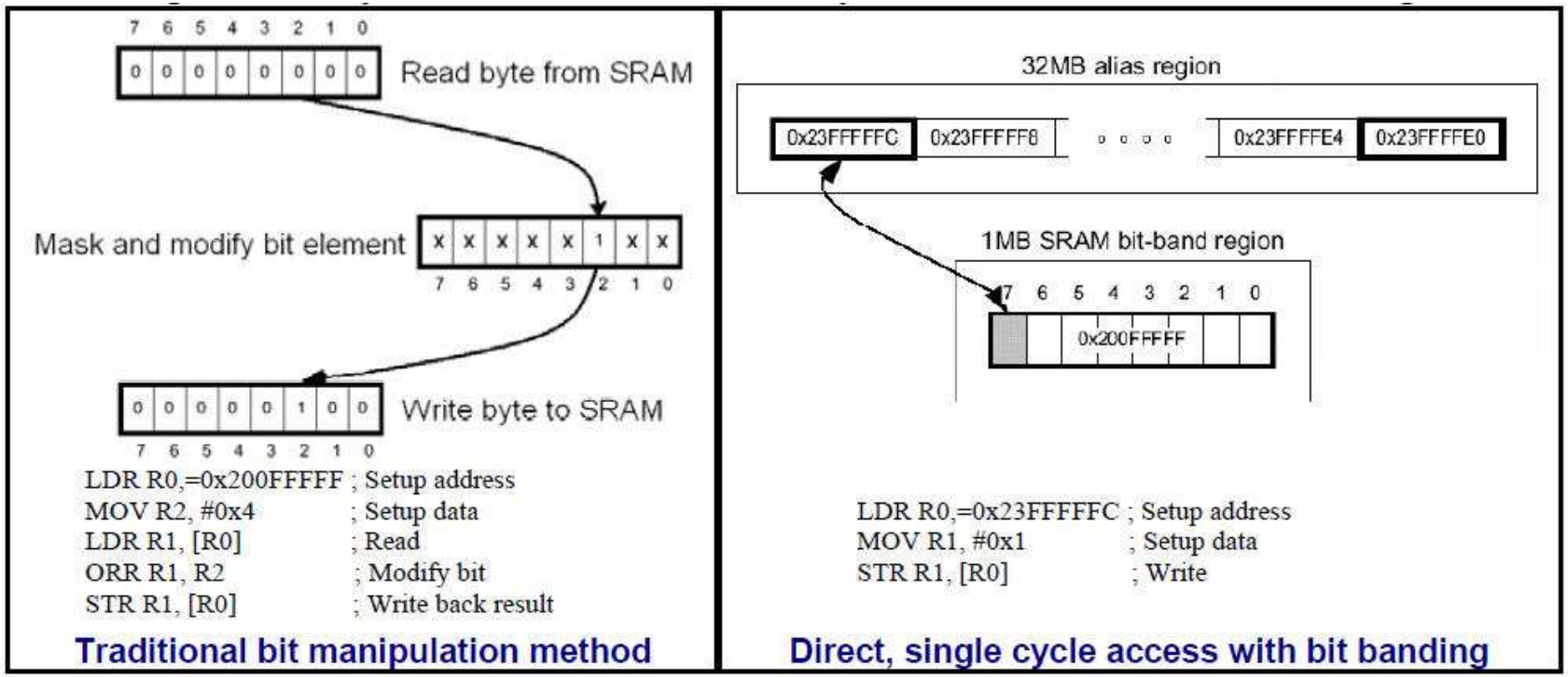
The Nested Vectored Interrupt Controller (NVIC)

- By handling the stack operations in hardware, the Cortex-M3 processor removes the need to write assembler wrappers that are required to perform stack manipulation for traditional C-based interrupt service routines, making application development significantly easier.
- Tail chaining achieves much lower latency by replacing serial stack pop and push actions that normally take over 30 clock cycles with a simple 6 cycle instruction fetch.



Bit banding

- The Cortex-M3 processor enables direct access to single bits of data in simple systems by implementing a technique called bit-banding.



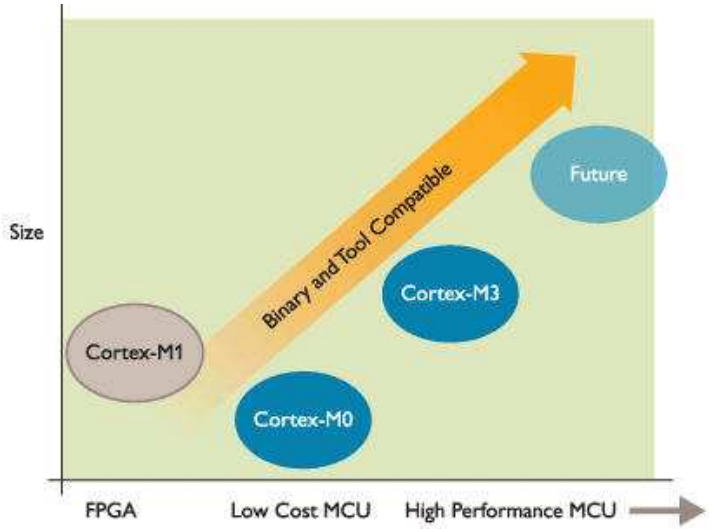
Bit banding

- bit_word_addr = bit_band_base + (byte_offset x 32) + (bit_number × 4)
- where:
  - bit_word_addr is the address of the word in the alias memory region that maps to the targeted bit.
  - bit_band_base is the starting address of the alias region
  - byte_offset is the number of the byte in the bit-band region that contains the targeted bit
  - bit_number is the bit position (0-7) of the targeted bit.
- Example:
  - The following example shows how to map bit 7 of the byte located at SRAM address 0x200FFFFF in the alias region:0x23FFFFFC = 0x22000000 + (0xFFFFF *32) + (7*4).
  - Writing to address 0x23FFFFFC has the same effect as a read-modify-write operation on bit 7 of the byte at SRAM address 0x200FFFFF.

ARM Cortex-M3處理器之應用

The Cortex-M3 processor offers an excellent balance of architectural features, high performance and low costs, making it a very attractive choice for a broad range of applications, including:

- Microcontrollers
  - 32-bit performance at 8-bit costs
- Wireless networking (inc Bluetooth, ZigBee and others)
  - Low power operation and integrated sleep modes supporting complex stacks
- Automotive and industrial control systems
  - Secure, reliable and deterministic operation
- White goods
  - High performance maths for complex motor algorithm support
- Electronic toys
  - Low cost implementations for next generation intelligent toys



參考資料

- http://www.arm.com/
- http://en.wikipedia.org/wiki/ARM_architecture

Q & A

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