PCA8539

100 x 18 Chip-On-Glass LCD dot matrix driver

Rev. 0.04 — 29 August 2013 **Objective data sheet**

1. General description

The PCA8539 is a fully featured Liquid Crystal Display (LCD)[1] driver, specifically designed for high-contrast Vertical Alignment (VA) LCD with multiplex rates up to 1:18. It generates the drive signals for multiplexed LCD containing up to 18 backplanes, 100 segments, and up to 1800 elements. The PCA8539 features an internal charge pump with internal capacitors for on-chip generation of the LCD driving voltage. To ensure an optimal and stable contrast over the full temperature range, the PCA8539 offers a programmable temperature compensation of the LCD supply voltage. The PCA8539 can be easily connected to a microcontroller by either the two-line I^{2}C-bus or a four-line bidirectional SPI-bus.

For a selection of NXP LCD segment drivers, see Table 46 on page 80.

2. Features and benefits

- AEC Q100 grade 2 compliant for automotive applications
- Single-chip LCD controller and driver
- 100 segments and 18 backplanes allowing to drive any graphic with up to 1800 elements
- On-chip:
  - Configurable 4, 3, or 2 times voltage multiplier generating LCD supply voltage, independent of V_{DD}, programmable by instruction (external supply also possible)
  - Integrated temperature sensor with temperature readout
  - Temperature compensation of on-chip generated VLCDOUT. Selectable linear temperature compensation of V_{LCD}
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible)
- Readout of RAM and registers possible
- Diagnostic features:
  - Checksum on I^{2}C and SPI bus
- Frame frequency: programmable from 45 Hz to 360 Hz
- 2960-bit RAM for storage (1800 bit for display data)
- Two-line I^{2}C-bus interface or four-line SPI bus
- Multiplex drive mode 1:18 and 1:12
- Inversion modes
  - n-line (n = 1 to 7) inversion
  - Frame inversion

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 20.

- Large supply voltage range: V_{DD1}: 2.5 V to 5.5 V (chip can be driven with battery cells)
- Analog supply voltage V_{DD2}: 2.5 V to 5.5 V
- LCD supply voltage V_{LCD}: 4 V to 16 V
- Very low current consumption (20 µA to 200 µA):
  - Power-down mode: < 2 µA

3. Applications

- Automotive
  - Instrument clusters
  - Climate control display
  - Car entertainment
  - Car radio
- Industrial
  - Medical and health care
  - Measuring equipment
  - Machine control systems
  - Information boards
  - General-purpose display modules
- Consumer
  - White goods
  - Home entertainment

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA8539DUG	bare die	244 bumps	PCA8539DUG

4.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCA8539DUG/DA	935301519033	PCA8539DUG/DAZ	1	chips with bumps in tray

5. Marking

Each die has a laser marking on the rear side. The format is LLLLLLLWWXXXXXX having the following meaning:

LLLLLLL - lot number

WW - wafer number

XXXXXX - die identification number

6. Block diagram

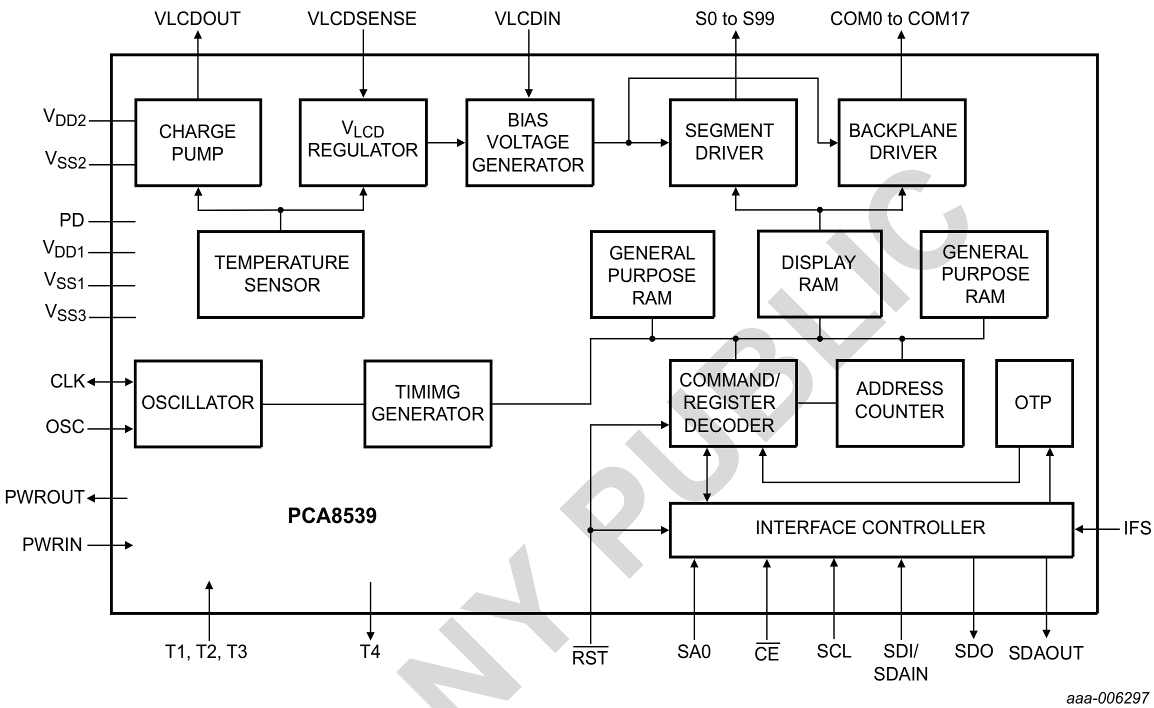


Fig 1. Block diagram of PCA8539

7. Pinning information

7.1 Pinning

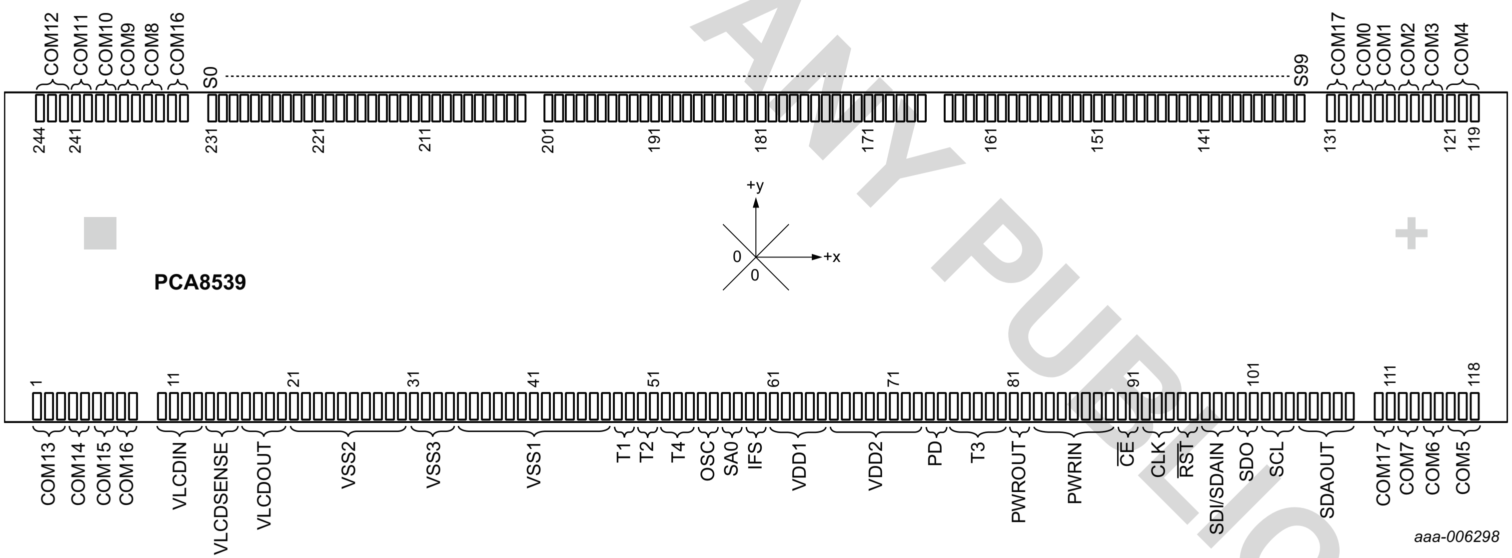


Fig 2. Pin configuration for PCA8539DUG

7.2 Pin description

Table 3. Pin description of PCA8539DUG

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description
Backplane output pins			
COM13	1 to 3	output	LCD backplane
COM14	4, 5		
COM15	6, 7		
COM16	8, 9, 232, 233		
COM17	110, 111, 130, 131		
COM7	112, 113		
COM6	114, 115		
COM5	116 to 118		
COM4	119 to 121		
COM3	122, 123		
COM2	124, 125		
COM1	126, 127		
COM0	128, 129		
COM8	234, 235		
COM9	236, 237		
COM10	238, 239		
COM11	240, 241		
COM12	242 to 244		
Segment output pins			
S99 to S0	132 to 231	output	LCD segment driver output
V_{LCD} pins			
VLCDIN	10 to 13	supply	V_{LCD} input
VLCDSENSE	14 to 16	input	V_{LCD} regulation input
VLCDOUT	17 to 20	output	V_{LCD} output
Supply pins			
VSS2[1]	21 to 30	supply	ground supply
VSS3[1]	31 to 34		
VSS1[1]	35 to 47		
VDD1	61 to 65	supply	supply voltage 1
VDD2	66 to 73	supply	supply voltage 2
PWROUT	81, 82	output	regulated voltage output; must be connected to PWRIN
PWRIN	83 to 89	input	regulated voltage input; must be connected to PWROUT
Test pins			
T1	48, 49	input	not accessible; must be connected to V_{SS1}
T2	50, 51		
T4	52 to 54	output	not accessible; must be left open

Table 3. Pin description of PCA8539DUG *…continued*

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description	
T3	76 to 80	input	not accessible; must be connected to PWROUT	
Oscillator, synchronization, and reset pins				
OSC[2]	55, 56	input	clock (internal/external) selector	
PD	74, 75	input	power-down mode select • for normal operation, pin PD must be LOW • for power-down mode, pin PD must be HIGH	
CLK	92 to 94	input/output	internal oscillator output, external oscillator input	
$\overline{\text{RST}}$	95, 96	input	active LOW reset input	
Bus-related pins				
			SPI-bus	**I²C-bus**
SA0	57, 58	input	unused; • connect to V_{SS1}	slave address selector; • connect to V_{SS1} for logic 0 • connect to V_{DD1} for logic 1
IFS	59, 60	input	interface selector input • connect to V_{SS1}	interface selector input • connect to V_{DD1}
$\overline{\text{CE}}$	90, 91	input	chip enable input (active LOW)	unused • connect to V_{DD1}
SDI/SDAIN	97 to 99	input	SPI-bus data input	I²C-bus serial data input
SDO	100, 101	output	SPI serial data output	unused • must be left open
SCL	102 to 104	input	serial clock input	serial clock input
SDAOUT	105 to 109	output	unused • must be connected to V_{SS1}	serial data output

[1] The substrate (rear side of the die) is at V_{SS1} potential and must not be connected.

[2] If pin OSC is tied to V_{SS1}, CLK is the output pin of the internal oscillator. If pin OSC is tied to V_{DD1}, CLK is the input pin for the external oscillator.

8. Functional description

8.1 Commands of PCA8539

The commands defined in Table 5 control the PCA8539.

The sequence to execute a command is like shown in Table 4:

Table 4. Command execution sequence

Bus	Byte 1	Byte 2	Byte 3
I^2C	slave address[1] + R/W̄[2]	CO + RS[1:0][3]	command
SPI	R/W̄[2] + subaddress[4]	CO + RS[1:0][3]	command

[1] More about the slave address, see Section 9.2.7.

[2] See Section 9.2.7 and Section 9.3.1.

[3] See Section 9.1.

[4] More about the subaddress, see Section 9.3.1.

Remark: Any other combinations of operation code bits that are not mentioned in this document can lead to undesired operation modes of PCA8539.

Table 5. Commands of PCA8539

Bit positions labeled as - are not implemented have to be always written with 0.

Command name	R/W̄	Command select RS[1:0]		Bits 7	6	5	4	3	2	1	0	Reference
General control commands												
Initialize	0	0	0	0	0	0	0	0	0	0	1	Section 8.1.1.1
Clear_reset_flag	0	0	0	0	0	0	1	1	1	1	1	Section 8.1.1.2
OTP_refresh	0	0	0	0	0	0	0	0	0	1	0	Section 8.1.1.3
Clock_out_ctrl	0	0	0	0	0	1	0	0	0	0	COE	Section 8.1.1.4
Read_reg_select	0	0	0	0	0	0	0	0	1	XC	SO	Section 8.1.1.5
Read_status_reg	1	0	0	TD[7:0]								Section 8.1.1.6
				CS[7:0]								
				Status_Register_1 to Status_Register_9								
Graphic_mode_cfg	0	0	0	0	1	0	1	0	GMX	-	-	Section 8.1.1.7
Sel_mem_bank	0	0	0	0	0	0	1	0	SMB[2:0]			Section 8.1.1.8
Set_mem_addr	0	0	0	1	ADD[6:0]							Section 8.1.1.9
Read_data	1	0	1	RD[7:0]								Section 8.1.1.10
				0	0	0	RD[4:0]					
Write_data	0	0	1	WD[7:0]								Section 8.1.1.11
				0	0	0	WD[4:0]					
Display control commands												
Entry_mode_set	0	1	0	0	0	1	0	1	0	I_D	-	Section 8.1.2.1
Inversion_mode	0	1	0	0	1	0	0	0	INV[2:0]			Section 8.1.2.2
Frame_frequency	0	1	0	1	0	0	FF[4:0]					Section 8.1.2.3
Display_control	0	1	0	0	0	1	0	0	D	-	-	Section 8.1.2.4

Table 5. Commands of PCA8539 *...continued*

Bit positions labeled as - are not implemented have to be always written with 0.

Command name	R/$\overline{W}$	Command select		Bits								Reference
		RS[1:0]		7	6	5	4	3	2	1	0	
Display_config	0	1	0	0	0	0	0	0	1	P	-	Section 8.1.2.5
Charge pump and LCD bias control commands												
Charge_pump_ctrl	0	1	1	1	0	0	0	0	CPE	CPC[1:0]		Section 8.1.3.1
Set_VLCD	0	1	1	1	0	1	VLCD[8:4]					Section 8.1.3.2
	0	1	1	1	0	0	1	VLCD[3:0]				
Temperature compensation control commands												
Temperature_ctrl	0	1	1	0	0	0	0	0	TCE	TMF	TME	Section 8.1.4.1
TC_slope	0	1	1	0	0	0	0	1	TSA[2:0]			Section 8.1.4.2
	0	1	1	0	0	0	1	0	TSB[2:0]			
	0	1	1	0	0	0	1	1	TSC[2:0]			
	0	1	1	0	0	1	0	0	TSD[2:0]			

8.1.1 General control commands

8.1.1.1 Command: Initialize

This command generates a chip-wide reset by setting all command registers to their default values. It must be sent to the PCA8539 after power-on. For further information, see Section 8.2.1 on page 22.

Table 6. Initialize - Initialize command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00000001	**initialize**

8.1.1.2 Command: Clear_reset_flag

The Clear_reset_flag command clears the reset flag CRF, see Table 11 on page 11.

Table 7. Clear_reset_flag - Clear_reset_flag command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00011111	**clear reset status flag**

8.1.1.3 Command: OTP_refresh

In order to achieve the specified accuracy of the V_{LCD}, the frame frequency, and the temperature measurement, each IC is calibrated during production. These calibration values are stored in One Time Programmable (OTP) cells. Their content is loaded into the associated registers every time when the Initialize command or the OTP_refresh command is sent. This command takes approximately 10 ms to finish.

Table 8. OTP_refresh - OTP_refresh command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 0	-	00000010	**refresh register settings from OTP**

8.1.1.4 Command: Clock_out_ctrl

When pin CLK is configured as an output pin, the Clock_out_ctrl command enables or disables the clock output on pin CLK.

Table 9. Clock_out_ctrl - CLK pin input/output switch command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 1	-	0010000	fixed value
0	COE		**CLK** pin setting
		0[1]	clock signal not available on pin CLK; pin CLK is in 3-state
		1	clock signal available on pin CLK

[1] Default value.

For lower power consumption, the clock is only active when display (see Table 21), charge pump (see Table 23), or temperature measurement (see Table 25) is enabled.

8.1.1.5 Command: Read_reg_select

The Read_reg_select command allows choosing to read out the temperature or the status registers Checksum to Status_Register_9 of the device (see Table 11).

Table 10. Read_reg_select - select registers for readout command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 2	-	000001	fixed value
1	XC		**checksum mode setting**
		0[1]	XOR checksum
		1	CRC-8 checksum
0	SO		**readout select**
		0[1]	temperature
		1	status registers

[1] Default value.

8.1.1.6 Command: Read_status_reg

With the Read_status_reg command the temperature, checksum, and the status registers can be read out. The behavior of the Read_status_reg command is controlled by the SO bit of the Read_reg_select command (see Table 10).

Table 11. Read_status_reg - readout register command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	1	fixed value
-	RS[1:0]	00	fixed value
Temperature readout if SO = 0 (see Table 10)			
7 to 0	TD[7:0]	00000000 to 11111111[1]	**temperature readout**
Status readout if SO = 1 (see Table 10)			
Checksum			
7 to 0	CS[7:0]	00000000[1] to 11111111	**checksum result** from RAM writing with checksum mode set by bit XC (see Table 10)
Status_Register_1			
7	-	0	fixed value
6	GMX		**multiplex drive mode setting status**
5, 4	-	00	fixed value
3	I_D	see Table 17	**address stepping select status**
2 to 0	-	000	fixed value
Status_Register_2			
7 to 5	INV[2:0]	see Table 18	**inversion mode setting status**
4 to 0	FF[4:0]	see Table 20	**frame frequency setting status**
Status_Register_3			
7	D	see Table 21	**display setting status**
6 to 2	-	00000	fixed value
1	P	see Table 22	**display segment setting status**
0	-	0	fixed value
Status_Register_4			
7 to 5	-	000	fixed value
4	CPE	see Table 23	**charge pump setting status**
3	-	0	fixed value
2, 1	CPC[1:0]	see Table 23	**charge pump voltage multiplier setting status**
0	VLCD8	see Table 24	**V_{LCD} values setting**
Status_Register_5			
7 to 0	VLCD[7:0]	see Table 24	**V_{LCD} values setting**
Status_Register_6			
7	TCE	see Table 25	**temperature compensation setting status**
6	TMF		**temperature measurement filter setting status**
5 to 3	TSA[2:0]	see Table 26	**temperature compensation slope A setting status**
2 to 0	TSB[2:0]		**temperature compensation slope B setting status**
Status_Register_7			
7	TME	see Table 25	**temperature measurement setting status**

Table 11. Read_status_reg - readout register command bit description *…continued*

Bit	Symbol	Value	Description
6 to 4	TSC[2:0]	see Table 26	**temperature compensation slope C setting status**
3 to 1	TSD[2:0]		**temperature compensation slope D setting status**
0	-	0	fixed value
Status_Register_8			
7 to 0	-	00000000	fixed value
Status_Register_9			
7 to 3	-	00000	fixed value
2	QPR		**charge pump charge status**
		0	charge pump has not reached programmed value
		1	charge pump has reached programmed value
1	CRF		**reset flag status** the reset flag is set whenever a reset occurs; it should be cleared for reset monitoring (see Table 7)
		0	no reset has occurred since the reset flag register was cleared last time
		1[1]	reset has occurred since the reset flag register was cleared last time
0	COE	see Table 9	**CLK pin setting status**

[1] Start-up value.

8.1.1.7 Command: Graphic_mode_cfg

The Graphic_mode_cfg command allows setting the multiplex drive mode.

Table 12. Graphic_mode_cfg - graphic mode command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 3	-	01010	fixed value
2	GMX		**multiplex drive mode setting**
		0	1:18 multiplex drive mode
		1[1]	1:12 multiplex drive mode
1, 0	-	- -[2]	not implemented

[1] Default value.

[2] Not implemented, have to be always written with 0.

8.1.1.8 Command: Sel_mem_bank

The Sel_mem_bank command determines which RAM to access.

Table 13. Sel_mem_bank - RAM access configuration command

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7 to 3	-	00010	fixed value
2 to 0	SMB[2:0]		**RAM access select**
		000[1]	general-purpose RAM 1 is selected
		001	display data RAM bank 1 is selected
		010	display data RAM bank 2 is selected
		011	display data RAM bank 3 is selected
		100	general-purpose RAM 2 is selected
		101 to 111	not implemented

[1] Default value.

8.1.1.9 Command: Set_mem_addr

The Set_mem_addr command allows setting the RAM address in the address counter to access. The Sel_mem_bank command (see Section 8.1.1.8) determines whether to access the display RAM or the general-purpose RAM.

Table 14. Set_mem_addr - memory address command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	00	fixed value
7	-	1	fixed value
6 to 0	ADD[6:0]	0000000[1] to 1111111	**RAM address**

[1] Default value.

8.1.1.10 Command: Read_data

The Read_data command reads binary 8-bit data from the display RAM or general-purpose RAM.

Table 15. Read_data - data read bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	1	fixed value
-	RS[1:0]	01	fixed value
General-purpose RAM 1			
7 to 0	RD[7:0]	00000000 to 11111111	**read data from general-purpose RAM 1**
Display RAM bank 1 to 3, general-purpose RAM 2			
7 to 5	-	000	fixed value
4 to 0	RD[4:0]	00000 to 11111	**read data from display RAM bank 1 to 3 and general-purpose RAM 2**

The Sel_mem_bank command (see Section 8.1.1.8) determines whether to read from the display RAM or general-purpose RAM. After reading, the address counter automatically increments or decrements by 1 in accordance with the setting of bit I_D of the Entry_mode_set command (see Section 8.1.2.1).

Only bit 4 to bit 0 of the display RAM or the general-purpose RAM 2 data are valid. Bit 7 to bit 5 are set logic 0.

8.1.1.11 Command: Write_data

The Write_data command writes binary 8-bit data to the display RAM or general-purpose RAM.

Table 16. Write_data - data write bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	01	fixed value
General-purpose RAM 1			
7 to 0	WD[7:0]	00000000 to 11111111	**write data to general-purpose RAM 1**
display RAM bank 1 to 3, general-purpose RAM 2			
7 to 5	-	000	not implemented
4 to 0	WD[4:0]	00000 to 11111	**write data to the display RAM bank 1 to 3 and general-purpose RAM 2**

The Sel_mem_bank command (see Section 8.1.1.8) determines whether to write data into the display RAM or general-purpose RAM. After writing, the address counter automatically increments or decrements by 1 in accordance with the setting of bit I_D of the Entry_mode_set command (see Section 8.1.2.1).

Only bit 4 to bit 0 of the display RAM or the general-purpose RAM 2 data are valid. Bit 7 to bit 5 are not implemented and should always be logic 0.

8.1.2 Display control commands

8.1.2.1 Command: Entry_mode_set

The Entry_mode_set command sets the address stepping.

Table 17. Entry_mode_set - entry mode bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 2	-	001010	fixed value
1	I_D		**address stepping select**
		0	display RAM or general-purpose RAM address decrements by 1
		1[1]	display RAM or general-purpose RAM address increments by 1
0	-	-[2]	not implemented

[1] Default value.

[2] Not implemented, have to be always written with 0.

Bit I_D: When bit I_D = 1, the display RAM or general-purpose RAM address increments by 1 when data is written into or read from the display RAM or general-purpose RAM.

When bit I_D = 0 the display RAM or general-purpose RAM address decrements by 1 when data is written into or read from the display RAM or general-purpose RAM.

8.1.2.2 Command: Inversion_mode

The Inversion_mode command allows changing the drive scheme inversion mode.

The waveforms used to drive LC displays (see Figure 24 and Figure 25) inherently produce a DC voltage across the display cell. The PCA8539 compensates for the DC voltage by inverting the waveforms on alternate frames or alternate lines. The choice of the compensation method is determined with INV[2:0] in Table 18.

Table 18. Inversion_mode - inversion mode command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	01000	fixed value
2 to 0	INV[2:0]		**inversion mode setting**
		000[1]	frame inversion mode
		001	1-line inversion mode
		010	2-line inversion mode
		011	3-line inversion mode
		100	4-line inversion mode
		101	5-line inversion mode
		110	6-line inversion mode
		111	7-line inversion mode

[1] Default value.

Line inversion mode (driving scheme A): In line inversion mode, the DC value is compensated every n^{th} line. Changing the inversion mode to line inversion mode reduces the possibility for flickering but increases the power consumption.

Frame inversion mode (driving scheme B): In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption, therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined, however since the switching frequency is reduced there is the possibility for flicker to occur.

8.1.2.3 Command: Frame_frequency

With this command, the clock and frame frequency can be programmed when using the internal clock.

Table 19. Frame-frequency - frame frequency select command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 5	-	100	fixed value
4 to 0	FF[4:0]	see Table 20	**frame frequency setting**

The duty cycle depends on the frequency chosen (see Table 20).

The Frame_frequency command allows configuring the frame frequency and the clock frequency. The default frame frequency of 80 Hz is factory calibrated.

Table 20. Clock and frame frequency values

Duty cycle definition: % HIGH-level time : % LOW-level time.

FF[4:0]	Frame frequency (Hz)	Clock frequency (Hz)	Typical duty cycle (%)
00000	45	36000	50 : 50
00001	50	39724	44 : 56
00010	55	44308	38 : 62
00011	60	48000	33 : 67
00100	65	52364	27 : 73
00101	70	54857	23 : 77
00110	75	60632	15 : 85
00111[1]	80	64000	11 : 89
01000	85	67765	5 : 95
01001	90	72000	50 : 50
01010	95	76800	46 : 54
01011	100	82286	42 : 58
01100	110	88615	38 : 62
01101	120	96000	33 : 67
01110	130	104727	27 : 73
01111	145	115200	20 : 80
10000	160	128000	11 : 89
10001	180	144000	50 : 50
10010	210	164571	42 : 58
10011	240	192000	33 : 67
10100	290	230400	20 : 80
10101 to 11111	360	288000	50 : 50

[1] Default value.

8.1.2.4 Command: Display_control

With the Display_control command, the display can be switched on or off.

Table 21. Display_control - Display control bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 3	-	00100	fixed value
2	D		**display setting**
		0[1]	display is off
		1	display is on
1, 0	-	- -[2]	not implemented

[1] Default value.

[2] Not implemented, have to be always written with 0.

8.1.2.5 Command: Display_config

The Display_config command allows setting how the data is displayed.

Table 22. Display_config - display configuration bit description

Bit	Symbol	Value	Description
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	10	fixed value
7 to 2	-	000001	fixed value
1	P		**display segment setting**
		0[1]	segment data: left to right; segment data is displayed from segment 0 to segment 99
		1	segment data: right to left; segment data is displayed from segment 99 to segment 0
0	-	-[2]	fixed value

[1] Default value.

[2] Not implemented, have to be always written with 0.

Bit P: The P bit is used to flip the display left to right by mirroring the segment data.

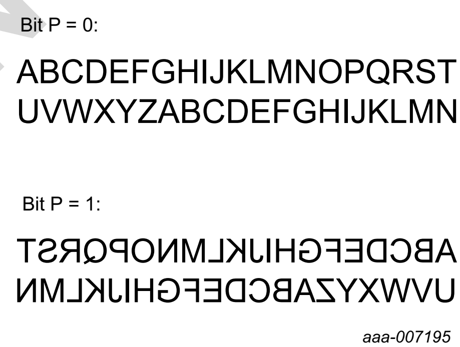


Fig 3. Illustration of the display configuration bit P

8.1.3 Charge pump and LCD bias control commands

8.1.3.1 Command: Charge_pump_ctrl

The Charge_pump_ctrl command enables or disables the internal V_{LCD} generation and controls the charge pump voltage multiplier setting.

Table 23. Charge_pump_ctrl - charge pump control command bit description

Bit	Symbol	Binary value	Description
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	11	fixed value
7 to 4	-	1000	fixed value
3	CPE		**charge pump setting**
		0[1]	charge pump disabled; no internal V_{LCD} generation; external supply of V_{LCD}
		1	charge pump enabled
2 to 0	CPC[2:0]		**charge pump voltage multiplier setting**
		00[1]	$V_{LCD} = 2 \times V_{DD2}$
		01	$V_{LCD} = 3 \times V_{DD2}$
		10	$V_{LCD} = 4 \times V_{DD2}$
		11	$V_{LCD} = V_{DD2}$ (direct mode)

[1] Default value.

8.1.3.2 Command: Set_VLCD

The Set_VLCD command allows programming the V_{LCD} value. The generated V_{LCD} is independent of the power supply, allowing battery operation of the PCA8539.

Table 24. Set_VLCD - Set-V_{LCD} command bit description

Bit	Symbol	Value	Description
The 5 MSB of VLCD			
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	11	fixed value
7 to 5	-	101	fixed value
4 to 0	VLCD[8:4]	00000[1] to 11111	**V_{LCD} value**
The 4 LSB of VLCD			
-	$R/\overline{W}$	0	fixed value
-	RS[1:0]	11	fixed value
7 to 4	-	1001	fixed value
3 to 0	VLCD[3:0]	0000[1] to 1111	**V_{LCD} value**

[1] Default value.

8.1.4 Temperature compensation control commands

8.1.4.1 Command: Temperature_ctrl

The Temperature_ctrl command enables or disables the temperature measurement block and the temperature compensation of V_{LCD} (see Section 8.4.5).

Table 25. Temperature_ctrl - temperature measurement control command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	11	fixed value
7 to 3	-	00000	fixed value
2	TCE		**temperature compensation setting**
		0[1]	temperature compensation of V_{LCD} disabled
		1	temperature compensation of V_{LCD} enabled
1	TMF		**temperature measurement filter** setting
		0[1]	digital temperature filter disabled[2]
		1	digital temperature filter enabled
0	TME		**temperature measurement setting**
		0[1]	temperature measurement disabled; no temperature readout possible
		1	temperature measurement enabled; temperature readout possible

[1] Default value.

[2] The unfiltered digital value of TD[7:0] is immediately available for the readout and V_{LCD} compensation.

8.1.4.2 Command: TC_slope

The TC_slope command allows setting the temperature coefficients of V_{LCD} corresponding to 4 temperature intervals.

Table 26. TC_slope - V_{LCD} temperature compensation slope command bit description

Bit	Symbol	Value	Description
-	R/$\overline{W}$	0	fixed value
-	RS[1:0]	11	fixed value
TC-slope-A			
7 to 3	-	00001	fixed value
2 to 0	TSA[2:0]	000[1] to 111	**temperature factor A setting**[2]
TC-slope-B			
7 to 3	-	00010	fixed value
2 to 0	TSB[2:0]	000[1] to 111	**temperature factor B setting**[2]
TC-slope-C			
7 to 3	-	00011	fixed value
2 to 0	TSC[2:0]	000[1] to 111	**temperature factor C setting**[2]
TC-slope-D			
7 to 3	-	00100	fixed value
2 to 0	TSD[2:0]	000[1] to 111	**temperature factor D setting**[2]

[1] Default value.

[2] See Table 28 on page 37.

8.2 Start-up and shut-down

8.2.1 Initialization

The first command sent to the device after power-on or a reset by using the $\overline{RST}$ pin must be the Initialize command (see Section 8.1.1.1 on page 9).

The Initialize command resets the PCA8539 to the following starting conditions:

1. All backplane and segment driver outputs are set to V_{SS1}.
2. Selected drive mode is 1:18 multiplex driving mode.
3. The address counter is cleared (set logic 0).
4. Temperature measurement is disabled.
5. Temperature filter is disabled.
6. The internal V_{LCD} voltage generation is disabled. The charge pump is switched off.
7. The V_{LCD} temperature compensation is disabled.
8. The display is disabled.

The reset state is as shown in Table 27.

Table 27. Reset state of PCA8539

Command name	Bits							
	7	6	5	4	3	2	1	0
General control commands								
Clock_out_ctrl	0	0	1	0	0	0	0	0
Read_reg_select	0	0	0	0	0	1	0	0
Graphic_mode_cfg	0	0	0	0	1	0	0	0
Sel_mem_bank	0	0	0	1	0	0	0	0
Set_mem_addr	1	0	0	0	0	0	0	0
Display control commands								
Entry_mode_set	0	0	1	0	1	0	1	0
Inversion_mode	0	1	0	0	0	0	0	0
Frame_frequency	1	0	0	0	0	1	1	1
Display_control	0	0	1	0	0	0	0	0
Display_config	0	0	0	0	0	1	0	0
Charge pump and LCD bias control commands								
Charge_pump_ctrl	1	0	0	0	0	0	0	0
Set_VLCD	1	0	1	0	0	0	0	0
	1	0	0	1	0	0	0	0
Temperature compensation control commands								
Temperature_ctrl	0	0	0	0	0	0	0	0
TC_slope	0	0	0	0	1	0	0	0
	0	0	0	1	0	0	0	0
	0	0	0	1	1	0	0	0
	0	0	1	0	0	0	0	0

Remarks:

1. Do not transfer data for at least 1 ms after a power-on.
2. After power-on and before enabling the display, the display RAM content must be brought to a defined status by writing meaningful display content (for example, a graphic) otherwise unwanted display artifacts may appear on the display.

8.2.2 Reset pin function

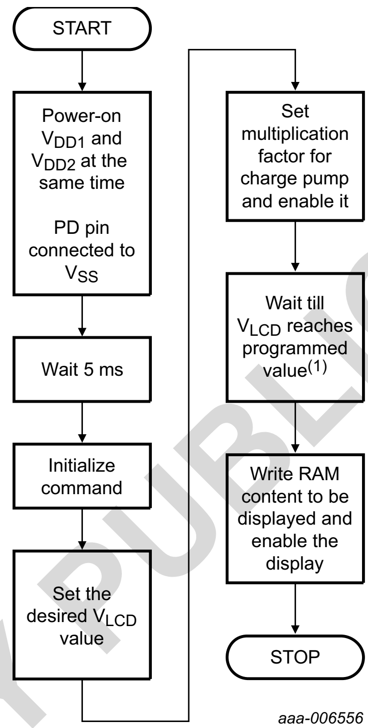
The reset pin ($\overline{RST}$) of the PCA8539 resets all the registers to their default state. The reset state is given in Table 27. The RAM contents remain unchanged. After the reset signal is released, the Initialize command must be sent to complete the initialization of the chip.

8.2.3 Power-down pin function

When connected to V_{DD1}, the internal circuits are switched off, leaving only 2 μA (typical) as an overall current consumption. When connected to V_{SS1}, the PCA8539 runs or starts up to normal mode again. For the start-up and power-down sequences, see Section 8.2.4 and Section 8.2.5.

8.2.4 Recommended start-up sequences

This section describes how to proceed with the initialization of the chip in different application modes.



(1) The QPR flag (see Table 11) indicates if the programmed LCD voltage value was reached. The latency time depends on the external capacitor on the V_{LCD} pins. For a capacitor of 100 nF a delay of 50 ms to 60 ms is expected.

Fig 4. Recommended start-up sequence when using the internal charge pump and the internal clock signal

When using the internal V_{LCD} generation, the display must not be enabled before the generation of V_{LCD} with the internal charge pump is completed. Otherwise unwanted display artifacts may appear on the display.

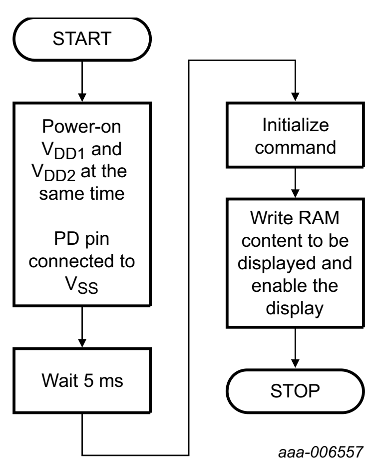
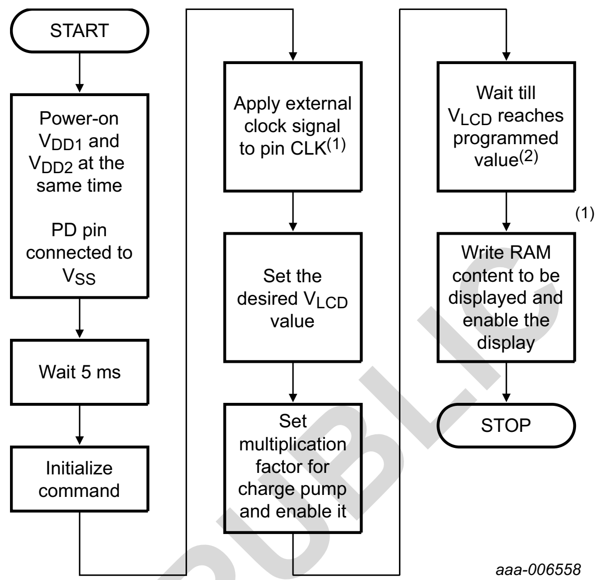


Fig 5. Recommended start-up sequence when using an externally supplied V_{LCD} and the internal clock signal



(1) Alternatively, the external clock signal can be applied after the generation of the V_{LCD} voltage.

(2) The QPR flag (see Table 11) indicates if the programmed LCD voltage value was reached. The latency time depends on the external capacitor on the V_{LCD} pins. For a capacitor of 100 nF a delay of 50 ms to 60 ms is expected.

Fig 6. Recommended start-up sequence when using the internal charge pump and an external clock signal

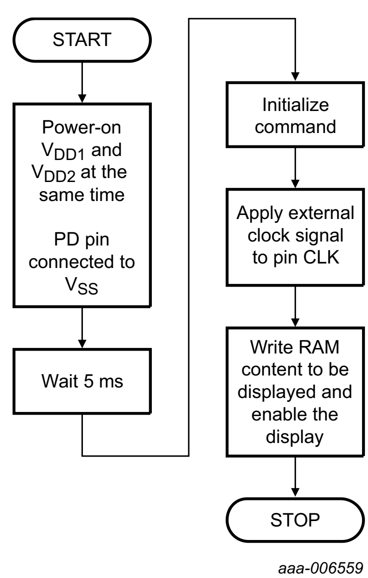
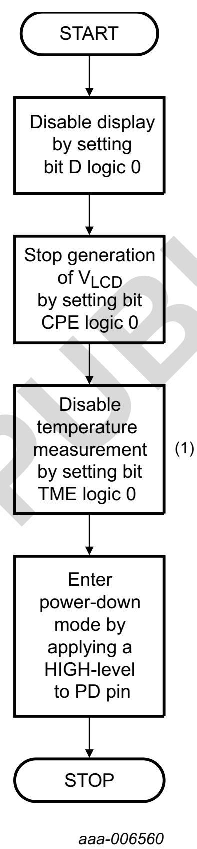


Fig 7. Recommended start-up sequence when using an externally supplied V_{LCD} and an external clock signal

8.2.5 Recommended power-down sequences

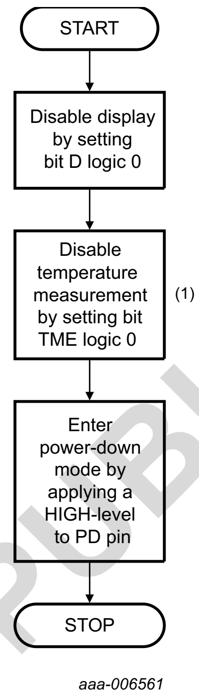
With the following sequences, the PCA8539 can be set to a state of minimum power consumption, called power-down mode.



(1) If previously enabled.

Remark: When bits D (Table 21 on page 17), CPE (Table 23 on page 19), and TME (Table 25 on page 20) are logic 0, the internal clock signal is switched off.

Fig 8. Recommended power-down sequence for minimum power-down current when using the internal charge pump and the internal clock signal



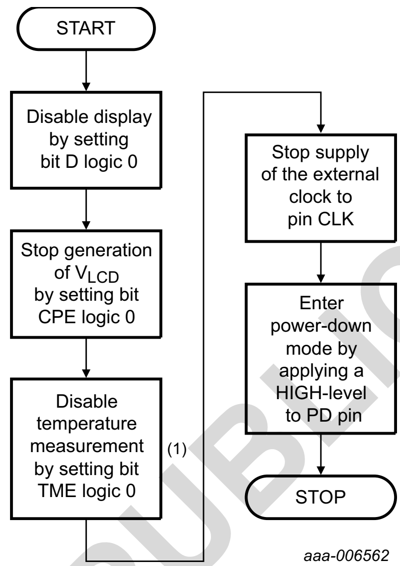
(1) If previously enabled.

Remark: When bits D (Table 21 on page 17), CPE (Table 23 on page 19), and TME (Table 25 on page 20) are logic 0, the internal clock signal is switched off.

Fig 9. Recommended power-down sequence when using an externally supplied V_{LCD} and the internal clock signal

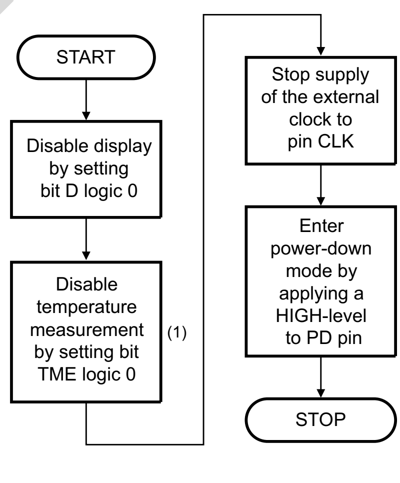
The chip can be put into power-down mode by applying a HIGH-level to pin PD. In power-down mode, all static currents are switched off (no internal oscillator, no bias level generation and all LCD outputs are internally connected to V_{SS}).

During power-down, information in the RAM and the chip state are not preserved. Instruction execution during power-down is not possible.



(1) If previously enabled.

Fig 10. Recommended power-down sequence when using the internal charge pump and an external clock signal



(1) If previously enabled.

Fig 11. Recommended power-down sequence when using an externally supplied V_{LCD} and an external clock signal

Remarks:

1. It is necessary to run the power-down sequence before removing the supplies. Depending on the application, care must be taken that no other signals are present at the chip input or output pins when removing the supplies (refer to Section 10 on page 59). Otherwise this may cause unwanted display artifacts. Uncontrolled removal of supply voltages does not damage the PCA8539.

2. Static voltages across the liquid crystal display can build up when the external LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD1} and V_{DD2}) is off, or the other way round. This may cause unwanted display artifacts. To avoid such artifacts, external V_{LCD}, V_{DD1}, and V_{DD2} must be applied or removed together.
3. A clock signal must always be supplied to the device when the device is active. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. Disable the display first and then remove the clock signal afterwards.

8.3 Possible display configurations

The PCA8539 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD dot-matrix displays (see Figure 12).

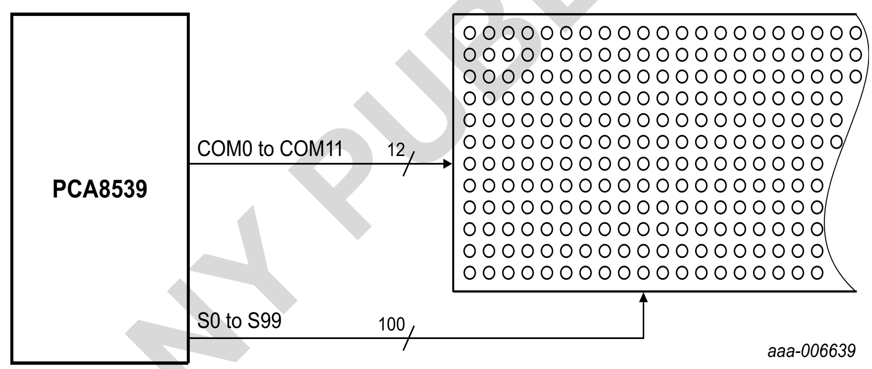


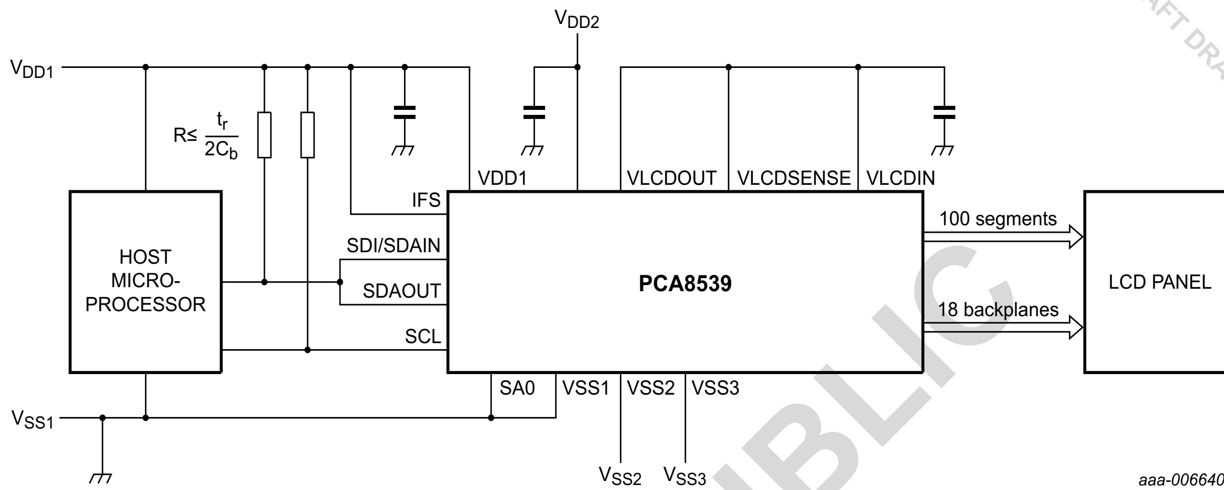
Fig 12. PCA8539 connected to a dot-matrix LCD (multiplex drive mode 1:12)

The host microcontroller maintains the communication channel with the PCA8539. The only other connections required to complete the system are the power supplies (VDD1, VDD2 and VSS1 to VSS3), the V_{LCD} pins (VLCDOUT, VLCDSENSE, VLCDIN), the external capacitors, and the LCD panel selected for the application. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally.

External capacitors of 100 nF minimum are required on each of the pins VDD1 and VDD2. VDD1 and VDD2 can be connected to the same power supply. In this case, a capacitor of 300 nF minimum is required.

VSS1 to VSS3 can be connected to the same ground supply.

The VLCD pins (VLCDOUT, VLCDSENSE, VLCDIN) can be connected, whether V_{LCD} is generated internally or supplied from external. An external capacitor of 300 nF minimum is recommended for VLCD. For high display loads, 1 μF is suggested.

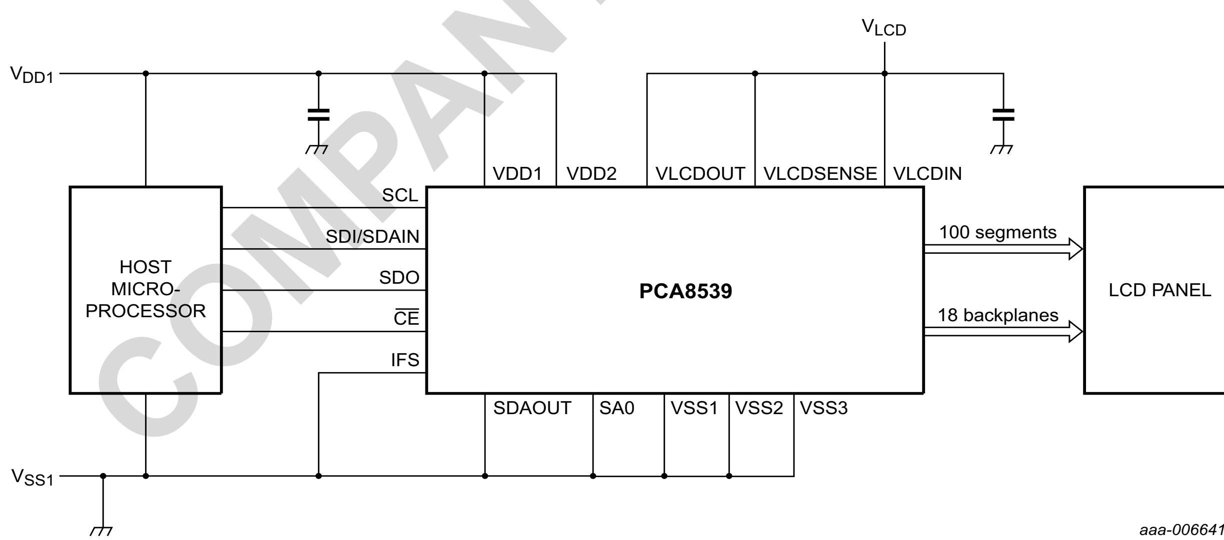


V_{DD1} and V_{DD2} from 2.5 V to 5.5 V. Values for t_r and C_b, see Table 40.

V_{DD1} and V_{DD2} can be connected to the same power supply.

V_{SS1} to V_{SS3} can be connected to the same ground supply.

Fig 13. Typical system configuration if using the internal V_{LCD} generation and I²C-bus



V_{DD1} and V_{DD2} from 2.5 V to 5.5 V.

Fig 14. Typical system configuration if using the external V_{LCD} and SPI-bus

8.4 LCD voltage

8.4.1 V_{LCD} pins

The PCA8539 has 3 V_{LCD} pins:

VLCDIN — V_{LCD} supply input

VLCDOUT — V_{LCD} voltage output

VLCDSENSE — V_{LCD} regulation circuitry input

The V_{LCD} voltage can be generated on-chip or externally supplied.

8.4.2 External V_{LCD} supply

When the external V_{LCD} supply is selected, the V_{LCD} voltage must be supplied to the pin VLCDIN. The pins VLCDOUT and VLCDSENSE can be left unconnected or alternatively connected to VLCDIN. The V_{LCD} voltage is available at the row and column drives of the device through the chosen bias system.

The internal charge pump must not be enabled, otherwise high internal currents may flow as well as high currents via pin VDD2 and pin VLCDOUT. No internal temperature compensation occurs on the externally supplied V_{LCD} even if bit TCE is set logic 1 (see Section 8.1.4.1). Also programming VLCD[8:0] has no effect on the externally supplied V_{LCD}.

8.4.3 Internal V_{LCD} generation

When the internal V_{LCD} generation is selected, the V_{LCD} voltage is available on pin VLCDOUT. The pins VLCDIN and VLCDSENSE must be connected to the pin VLCDOUT.

The Charge_pump_ctrl command (see Table 23 on page 19) controls the charge pump. It can be enabled with the CPE bit. The multiplier setting can be configured with the CPC[1:0] bits. The charge pump can generate a V_{LCD} up to $4 \times V_{DD2}$.

8.4.3.1 V_{LCD} programming

V_{LCD} can be programmed with the bit-field VLCD[8:0]. The final value of V_{LCD} is a combination of the programmed VLCD[8:0] value and in addition the output of the temperature compensation block. The system is exemplified in Figure 15.

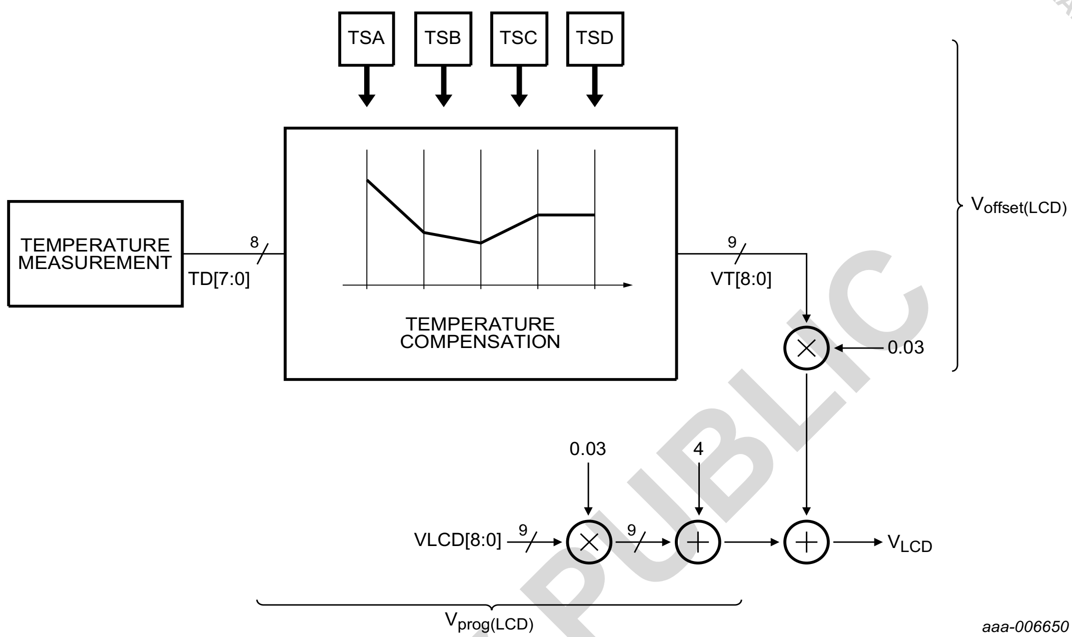


Fig 15. V_{LCD} generation including temperature compensation

Equation 1 to Equation 3 exemplify the V_{LCD} generation with temperature compensation.

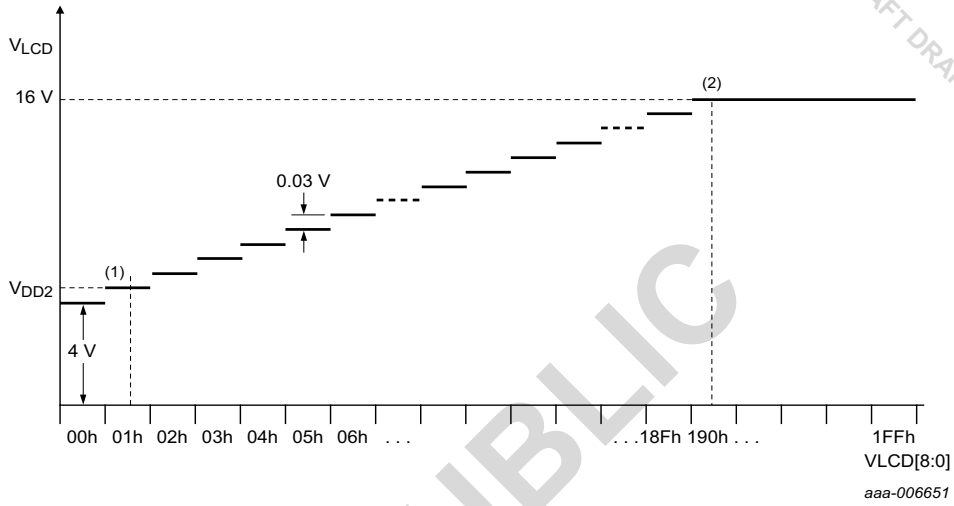
$$V_{prog(LCD)} = VLCD \times 0.03\ V + 4\ V \quad (1)$$

$$V_{offset(LCD)} = VT \times 0.03\ V \quad (2)$$

$$V_{LCD} = V_{prog(LCD)} + V_{offset(LCD)} = VLCD \times 0.03\ V + 4\ V + VT \times 0.03\ V \quad (3)$$

1. VLCD is the decimal value of the programmed VLCD factor (VLCD[8:0]).
2. VT is the binary value of the programmed temperature compensating factor (VT[8:0]) of the temperature compensation block. The temperature compensation block provides the value which is a two's complement with the value of 0h at 20 °C.

Figure 16 shows how the V_{LCD} changes with the programmed value of VLCD[8:0].



(1) VLCD[8:0] must be set so that $V_{LCD} > V_{DD2}$.

(2) Automatic limitation for $V_{LCD} > 16$ V.

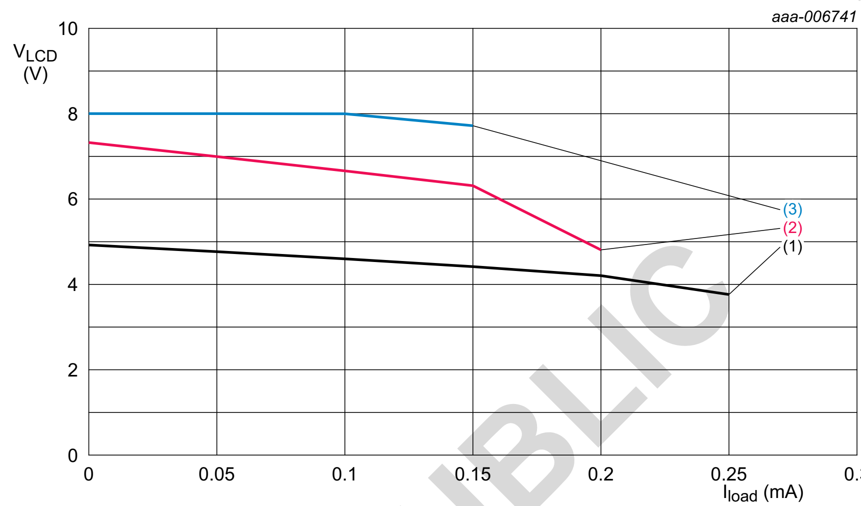
Fig 16. V_{LCD} programming of PCA8539 (assuming VT[8:0] = 0h)

Remarks:

1. VLCD[8:0] has to be set to such a value that the resultant V_{LCD}, including the temperature compensation, is higher than V_{DD2}.
2. The programmable range of VLCD[8:0] is from 0h to 1FFh. This would allow achieving a V_{LCD} of higher voltages but the PCA8539 has a built-in automatic limitation set to 16 V.

8.4.4 V_{LCD} drive capability

Figure 17 to Figure 19 illustrate the drive capability of the internal charge pump for various conditions. V_{LCD} is internally limited to 16 V.



Conditions: V_{DD2} = 2.5 V; V_{LCD} = 8 V; T_{amb} = 25 °C; $R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 50 Ω.

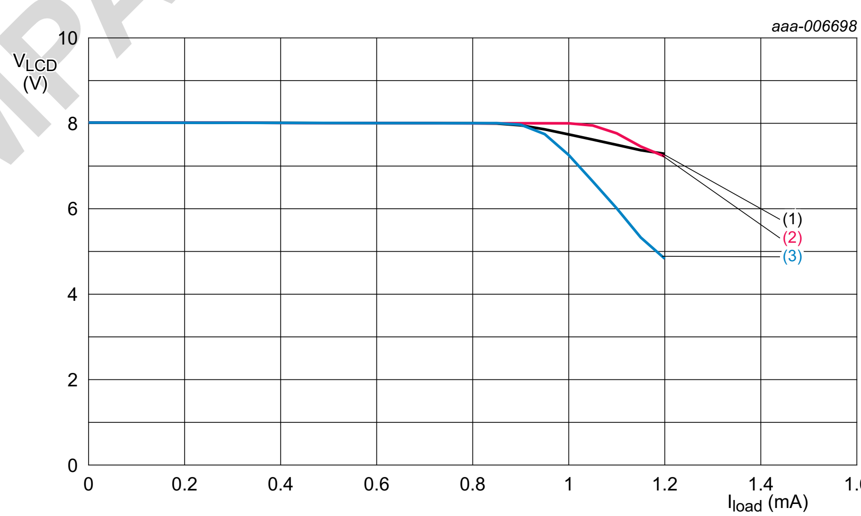
(1) $V_{LCD} = 2 \times V_{DD2}$.

(2) $V_{LCD} = 3 \times V_{DD2}$.

(3) $V_{LCD} = 4 \times V_{DD2}$.

I_{load} is the overall current sink of the column and row outputs depending on the display, plus the on-chip V_{LCD} current consumption.

Fig 17. V_{LCD} with respect to I_{load} at V_{DD2} = 2.5 V



Conditions: V_{DD2} = 5 V; V_{LCD} = 8 V; T_{amb} = 25 °C; $R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 50 Ω.

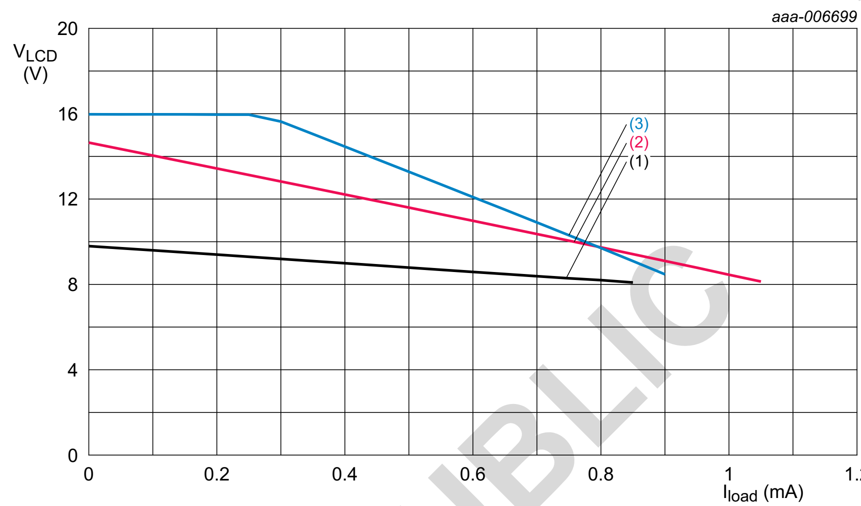
(1) $V_{LCD} = 2 \times V_{DD2}$.

(2) $V_{LCD} = 3 \times V_{DD2}$.

(3) $V_{LCD} = 4 \times V_{DD2}$.

I_{load} is the overall current sink of the column and row outputs depending on the display, plus the on-chip V_{LCD} current consumption.

Fig 18. V_{LCD} with respect to I_{load} at V_{DD2} = 5 V



Conditions: V_{DD2} = 5 V; V_{LCD} = 16 V; T_{amb} = 25 °C; $R_{ITO(VSS2)}$, $R_{ITO(VDD2)}$, $R_{ITO(VLCDOUT)}$ = 50 Ω.

(1) $V_{LCD} = 2 \times V_{DD2}$.

(2) $V_{LCD} = 3 \times V_{DD2}$.

(3) $V_{LCD} = 4 \times V_{DD2}$.

I_{load} is the overall current sink of the column and row outputs depending on the display, plus the on-chip V_{LCD} current consumption.

Fig 19. V_{LCD} with respect to I_{load} at V_{DD2} = 5 V

8.4.5 Temperature measurement and temperature compensation of V_{LCD}

8.4.5.1 Temperature readout

The PCA8539 has a built-in temperature sensor which provides an 8-bit digital value (TD[7:0]) of the ambient temperature. This value can be read by command (see Section 8.1.1.5 on page 10). The actual temperature is determined from TD[7:0] using Equation 4.

$$T(°C) = 0.6275 \times TD - 40 \quad (4)$$

TD[7:0] = FFh means that no temperature readout is available or was performed. FFh is the default value after initialization. The measurement needs about 8 ms to complete. It is repeated periodically every second as long as bit TME is set logic 1 (see Table 25 on page 20).

Due to the nature of a temperature sensor, oscillations may occur. To avoid this, a filter has been implemented in PCA8539. A control bit, TMF, is implemented to enable or disable the digital temperature filter (see Table 25 on page 20). The system is exemplified in Figure 20.

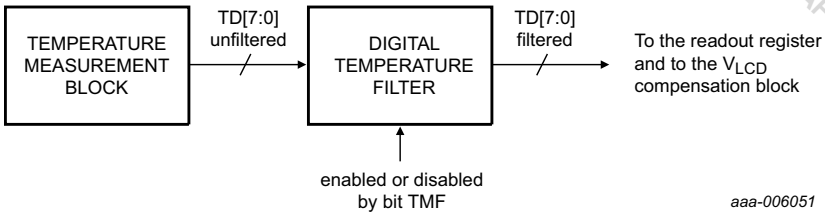
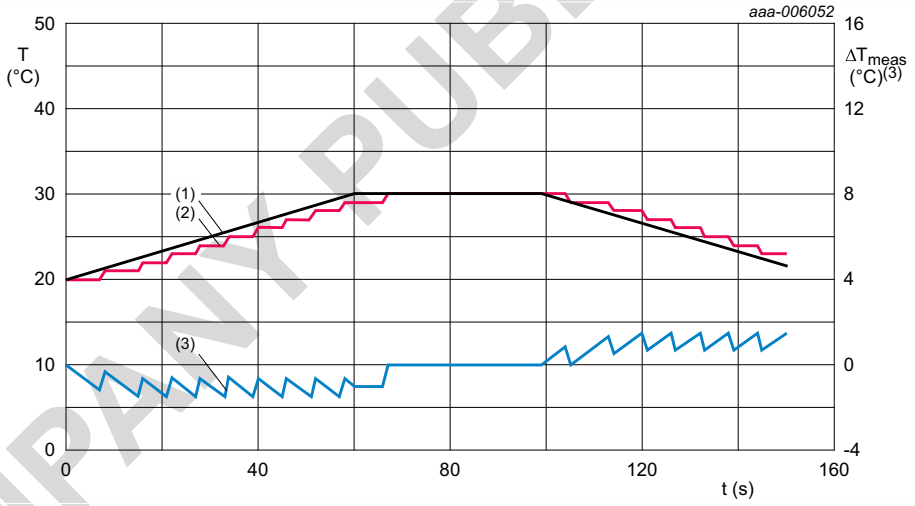


Fig 20. Temperature measurement block with digital temperature filter

The digital temperature filter introduces a certain delay in the measurement of the temperature. This behavior is illustrated in Figure 21.



(1) Environment temperature, T1 (°C).

(2) Measured temperature, T2 (°C).

(3) Measurement temperature variation, ΔT_{meas} = T2 − T1.

Fig 21. Temperature measurement delay

8.4.5.2 Temperature adjustment of the V_{LCD}

Due to the temperature dependency of the liquid crystal viscosity, the LCD supply voltage may have to be adjusted at different temperatures to maintain optimal contrast. The temperature characteristics of the liquid are provided by the LCD manufacturer. The slope has to be set to compensate for the liquid behavior. Internal temperature compensation can be enabled via bit TCE (see Table 25 on page 20).

The ambient temperature range is split up into 4 regions (see Figure 22) and to each a different temperature coefficient can be applied.

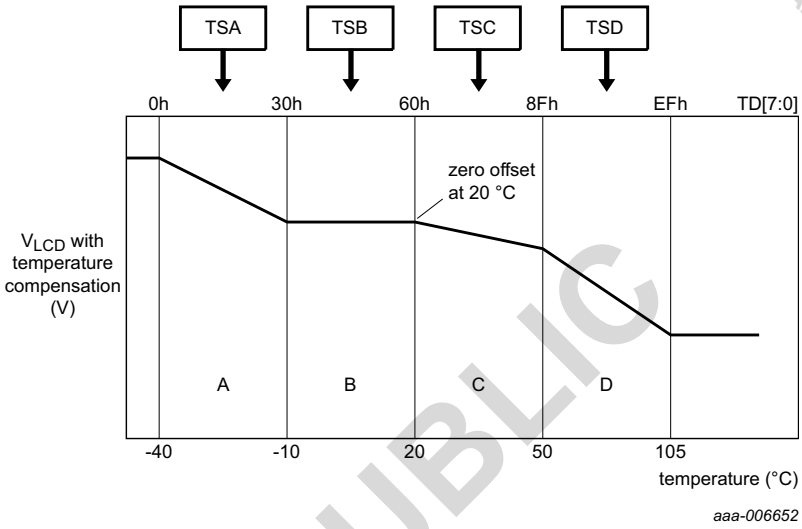


Fig 22. Example of segmented temperature coefficients

The temperature coefficients can be selected from a choice of eight different slopes. Each one of theses coefficients is independently selected via the TC_slope command (see Section 8.1.4.2 on page 21).

Table 28. Temperature coefficients

TSA[2:0] to TSD[2:0] value	Slope factor (mV/°C)	Temperature factor TSA to TSD[1]
000[2]	0	0.000
001	–6	–0.125
010	–12	–0.250
011	–24	–0.500
100	–60	–1.250
101	+6	+0.125
110	+12	+0.250
111	+24	+0.500

[1] The relationship between the temperature coefficients TSA to TSD and the slope factor is derived from Equation 5. where LSB of VLCD[8:0] ≅ 30 mV.

[2] Default value.

$$TSn = \frac{0.6275(°C)}{30\ (mV)} \times slope\ factor\ (mV/°C) \quad (5)$$

The value of the temperature compensated factor VT[8:0] is calculated according to Table 29.

Table 29. Calculation of the temperature compensating factor VT

Temperature range (°C)	Decimal value of TD[7:0]	Equations of factor VT
$T \leq -40\ °C$	0	$VT = -48 \times TSB - 48 \times TSA$
$-40°C < T \leq -10\ °C$	0 to 48	$VT = -48 \times TSB - (48 - TD[7:0]) \times TSA$
$-10\ °C < T \leq 20\ °C$	49 to 96	$VT = -(96 - TD[7:0]) \times TSB$
$20\ °C < T \leq 50\ °C$	97 to 143	$VT = (TD[7:0] - 96) \times TSC$
$50\ °C < T < 105\ °C$	144 to 230	$VT = 47 \times TSC + (TD[7:0] - 143) \times TSD$
$105\ °C \leq T$ [1]	231	$VT = 47 \times TSC + 88 \times TSD$

[1] No temperature compensation is possible above 105 °C. Above this value, the system maintains the compensation value from 105 °C.

8.4.5.3 Example calculation of $V_{offset(LCD)}$

Assumed that T_{amb} = –8 °C

1. Choose a temperature factor from Table 28, for example TSB[2:0] = 001, which gives a temperature factor of –0.125.
2. Calculate the decimal value of TD[7:0] with Equation 4:

$$TD = \frac{-8 + 40}{0.6275} \approx 51 .$$

3. Calculate the temperature compensating factor VT with the appropriate equation from Table 29:

$$VT = -(96 - 51) \times -0.125 = 5.625 .$$

4. Calculate $V_{offset(LCD)}$ with Equation 2:

$$V_{offset(LCD)} = 5.625 \times 0.03\ V = 0.169\ V .$$

8.4.6 LCD bias voltage generator

The intermediate bias voltages for the LCD are generated on-chip. This removes the need for an external resistive bias chain and significantly reduces the system current consumption. The optimum value of V_{LCD} depends on the multiplex rate, the LCD threshold voltage (V_{th}) and the number of bias levels.

The intermediate bias levels for the different multiplex rates are shown in Table 30. These bias levels are automatically set to the given values when switching to the corresponding multiplex rate.

Table 30. Bias levels as a function of multiplex rate

Multiplex rate	LCD bias configuration	Bias voltages					
		V_1	V_2	V_3	V_4	V_5	V_6
1:18	¼	V_{LCD}	$\frac{3}{4}V_{LCD}$	$\frac{1}{2}V_{LCD}$	$\frac{1}{2}V_{LCD}$	$\frac{1}{4}V_{LCD}$	V_{SS}
1:12	¼	V_{LCD}	$\frac{3}{4}V_{LCD}$	$\frac{1}{2}V_{LCD}$	$\frac{1}{2}V_{LCD}$	$\frac{1}{4}V_{LCD}$	V_{SS}

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 6 and the RMS off-state voltage ($V_{off(RMS)}$) with Equation 7:

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1 + a)^2}} \quad (6)$$

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1 + a)^2}} \quad (7)$$

where the values of a are

a = 3 for ¼ bias

and the values for n are

n = 12 for 1:12 multiplex rate

n = 18 for 1:18 multiplex rate.

Discrimination (D) is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 8. Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a+1)^2 + (n-1)}{(a-1)^2 + (n-1)}} \quad (8)$$

Remark:

- Row and column outputs comprise a series resistance R_o (see Table 38).
- V_{LCD} is sometimes referred as the LCD operating voltage.

8.4.6.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel is switched on or off, determines the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 23. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (9)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (10)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a (see Equation 6), n (see Equation 8), and the V_{LCD} voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named V_{th}. $V_{th(on)}$ is sometimes named saturation voltage V_{sat}.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

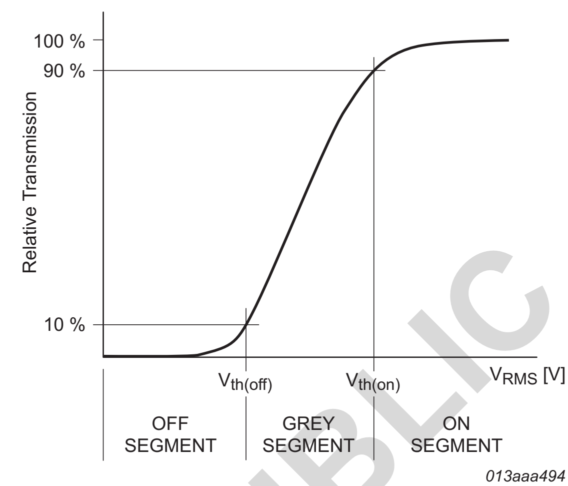
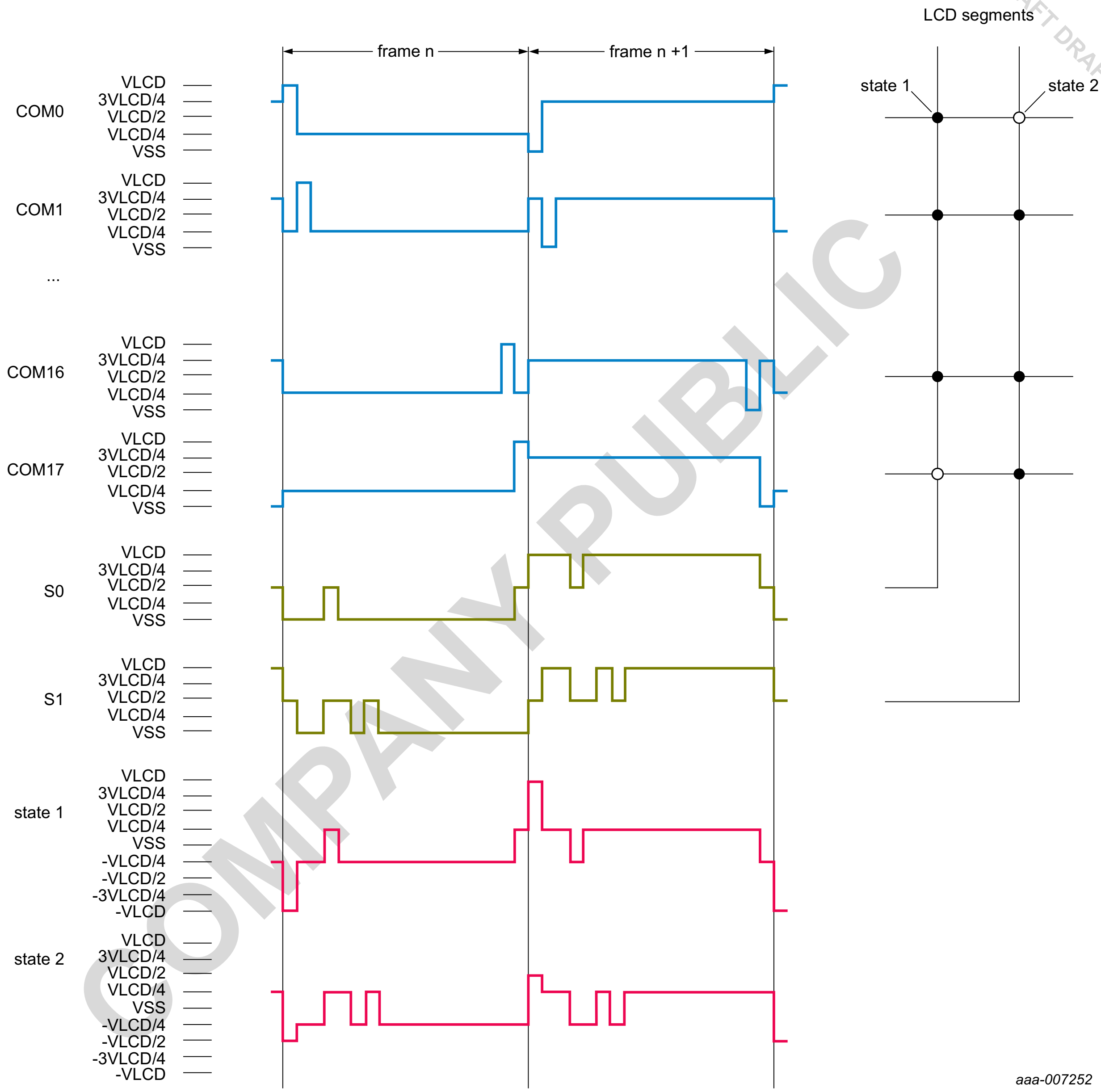


Fig 23. Electro-optical characteristic: relative transmission curve of the liquid

8.4.7 LCD drive mode waveforms

The PCA8539 contains 18 backplane and 100 segment drivers, which drive the appropriate LCD bias voltages in sequence to the display and in accordance with the data to be displayed. Unused outputs should be left open.

The bias voltages and the timing are automatically selected when the number of lines in the display is selected. Figure 24 and Figure 25 show typical waveforms.



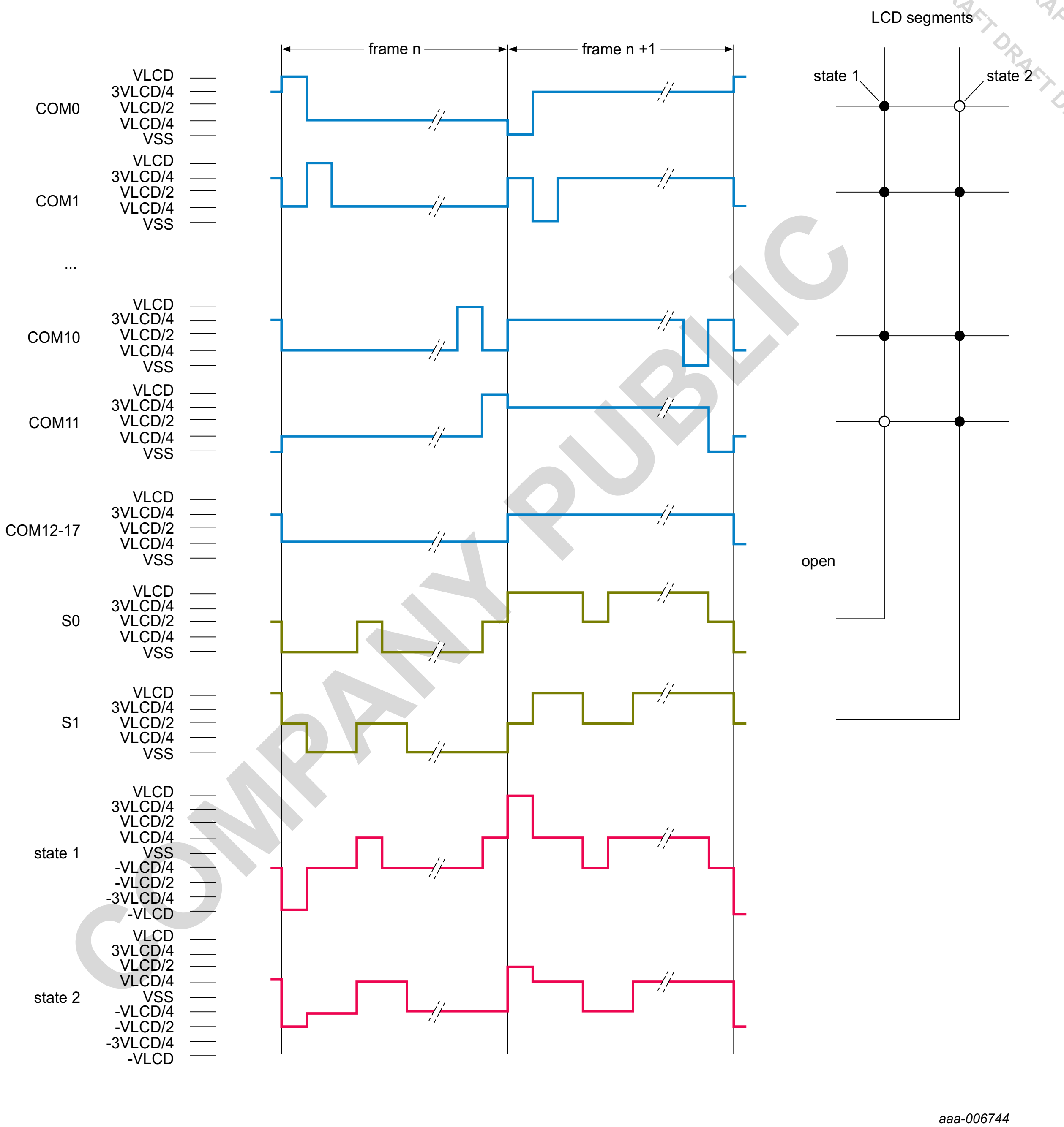
State(n) marks intersection(COM(x),S(n)) of LCD element(x,n).

$V_{state(n)}(t) = V_{S(n)}(t) - V_{COM(x)}(t)$.

$V_{state1}(t) = V_{S0}(t) - V_{COM0}(t)$.

$V_{state2}(t) = V_{S1}(t) - V_{COM0}(t)$.

Fig 24. Waveforms for the 1:18 multiplex drive mode. 5 bias levels, character mode, frame inversion mode



State(n) marks intersection(COM(x),S(n)) of LCD element(x,n).

$V_{state(n)}(t) = V_{S(n)}(t) - V_{COM(x)}(t)$.

$V_{state1}(t) = V_{S0}(t) - V_{COM0}(t)$.

$V_{state2}(t) = V_{S1}(t) - V_{COM0}(t)$.

Fig 25. Waveforms for the 1:12 multiplex drive mode, 5 bias levels, character mode, R8 to R15 and R17 open, frame inversion mode

8.5 Display RAM and general-purpose RAM

The PCA8539 has a display RAM and two general-purpose RAM. The RAM access is exemplified in Figure 26.

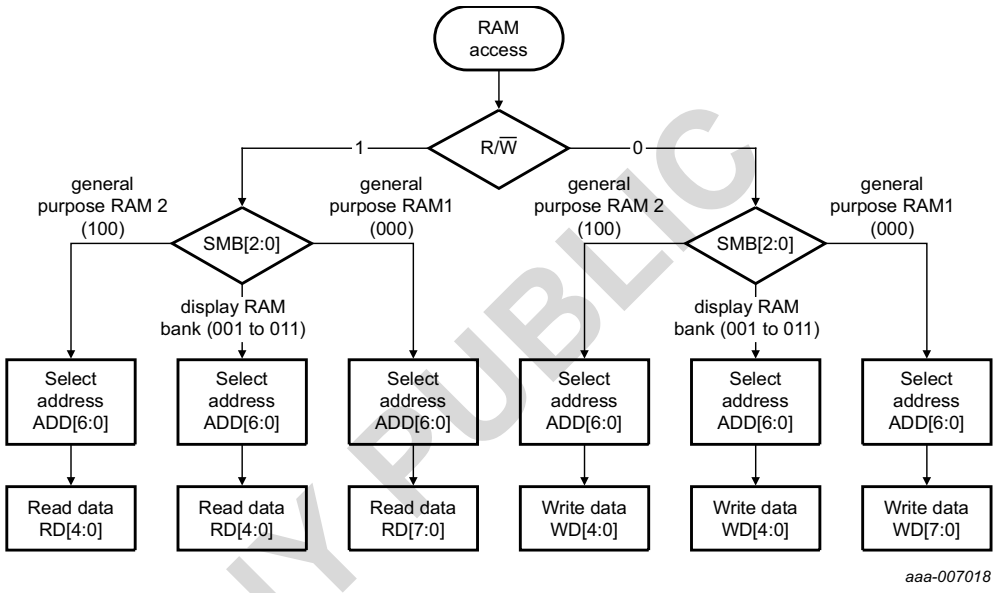


Fig 26. RAM access flowchart

8.5.1 Checksum

In order to detect transmission failures for RAM content transfers, the PCA8539 has a checksum calculator providing an XOR or CRC-8 checksum. The checksum calculator can be configured with bit XC of the Read_reg_select command (see Section 8.1.1.5). The checksum result can be read out with the Read_status_reg command (see Section 8.1.1.6).

The checksum results are:

- when XC = 0 (XOR checksum)
  - The checksum is the result of the XOR operation on the values loaded with the Write_data command and the previous register content.
  - The checksum result is reset when the bits of the command select RS[1:0] or R/$\overline{W}$ are changed.
- when XC = 1 (CRC-8 checksum)
  - The checksum is the result of the CRC-8 operation on the values loaded with the Write_data command and the previous register content. The polynomial used is $x^8 + x^5 + x^4 + 1$.
  - The checksum result is reset when the bits of the command select RS[1:0] or R/$\overline{W}$ are changed.

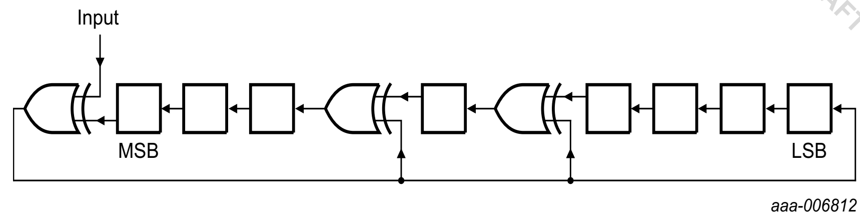


Fig 27. Logic diagram of the CRC8 generator

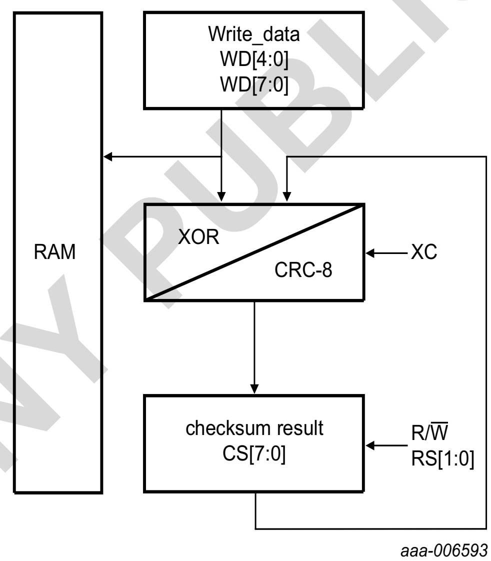


Fig 28. Checksum generation

8.5.2 Display RAM and multiplex drive modes

The display RAM is a static 100 × 18-bit RAM which stores LCD data. Logic 1 in the RAM bit map indicates the on-state, logic 0 the off-state of the corresponding LCD element. There is a one-to-one correspondence between the bits in the display RAM bitmap (Table 31) and the LCD elements.

The display RAM bitmap (Table 31) shows that the display RAM is organized in three RAM banks. The access to the RAM banks is controlled by SMB[2:0] (see Table 13). Row 0 to row 17 in the display RAM bitmap correspond with the backplane outputs COM0 to COM17, and column 0 to column 99 correspond with the segment outputs S0 to S99.

Table 31. Display RAM bitmap

RAM bank	RAM bank select	RAM address	Row (Back-plane)	Column (segment)					RAM bank	RAM bank select	RAM address	Row (Back-plane)	Column (segment)				
				Bit									Bit				
	SMB[2:0]	ADD[6:0]		4	3	2	1	0		SMB[2:0]	ADD[6:0]		4	3	2	1	0
1	001	0h	0	0	1	2	3	4	2	010	34h	9	0	1	2	3	4
		1h		5	6	7	8	9			35h		5	6	7	8	9
		2h		10	11	12	13	14			36h		10	11	12	13	14
		3h		15	16	17	18	19			37h		15	16	17	18	19
		4h		20	21	22	23	24			38h		20	21	22	23	24
		5h		25	26	27	28	29			39h		25	26	27	28	29
		6h		30	31	32	33	34			3Ah		30	31	32	33	34
		7h		35	36	37	38	39			3Bh		35	36	37	38	39
		8h		40	41	42	43	44			3Ch		40	41	42	43	44
		9h		45	46	47	48	49			3Dh		45	46	47	48	49
		Ah		50	51	52	53	54			3Eh		50	51	52	53	54
		Bh		55	56	57	58	59			3Fh		55	56	57	58	59
		Ch		60	61	62	63	64			40h		60	61	62	63	64
		Dh		65	66	67	68	69			41h		65	66	67	68	69
		Eh		70	71	72	73	74			42h		70	71	72	73	74
		Fh		75	76	77	78	79			43h		75	76	77	78	79
		10h		80	81	82	83	84			44h		80	81	82	83	84
		11h		85	86	87	88	89			45h		85	86	87	88	89
		12h		90	91	92	93	94			46h		90	91	92	93	94
		13h		95	96	97	98	99			47h		95	96	97	98	99
		14h	1	0	1	2	3	4			48h	10	0	1	2	3	4
		15h		5	6	7	8	9			49h		5	6	7	8	9
		16h		10	11	12	13	14			4Ah		10	11	12	13	14
		17h		15	16	17	18	19			4Bh		15	16	17	18	19
		18h		20	21	22	23	24			4Ch		20	21	22	23	24
		19h		25	26	27	28	29			4Dh		25	26	27	28	29
		1Ah		30	31	32	33	34			4Eh		30	31	32	33	34
		1Bh		35	36	37	38	39			4Fh		35	36	37	38	39
		1Ch		40	41	42	43	44			50h		40	41	42	43	44
		1Dh		45	46	47	48	49			51h		45	46	47	48	49
		1Eh		50	51	52	53	54			52h		50	51	52	53	54
		1Fh		55	56	57	58	59			53h		55	56	57	58	59
		20h		60	61	62	63	64			54h		60	61	62	63	64
		21h		65	66	67	68	69			55h		65	66	67	68	69
		22h		70	71	72	73	74			56h		70	71	72	73	74
		23h		75	76	77	78	79			57h		75	76	77	78	79

Table 31. Display RAM bitmap *…continued*

RAM bank	RAM bank select	RAM address	Row (Back-plane)	Column (segment) Bit					RAM bank	RAM bank select	RAM address	Row (Back-plane)	Column (segment) Bit				
	SMB[2:0]	ADD[6:0]		4	3	2	1	0		SMB[2:0]	ADD[6:0]		4	3	2	1	0
1	001	24h	1	80	81	82	83	84	2	010	58h	10	80	81	82	83	84
		25h		85	86	87	88	89			59h		85	86	87	88	89
		26h		90	91	92	93	94			5Ah		90	91	92	93	94
		27h		95	96	97	98	99			5Bh		95	96	97	98	99
		28h	2	0	1	2	3	4			5Ch	11	0	1	2	3	4
		29h		5	6	7	8	9			5Dh		5	6	7	8	9
		2Ah		10	11	12	13	14			5Eh		10	11	12	13	14
		2Bh		15	16	17	18	19			5Fh		15	16	17	18	19
		2Ch		20	21	22	23	24			60h		20	21	22	23	24
		2Dh		25	26	27	28	29			61h		25	26	27	28	29
		2Eh		30	31	32	33	34			62h		30	31	32	33	34
		2Fh		35	36	37	38	39			63h		35	36	37	38	39
		30h		40	41	42	43	44			64h		40	41	42	43	44
		31h		45	46	47	48	49			65h		45	46	47	48	49
		32h		50	51	52	53	54			66h		50	51	52	53	54
		33h		55	56	57	58	59			67h		55	56	57	58	59
		34h		60	61	62	63	64			68h		60	61	62	63	64
		35h		65	66	67	68	69			69h		65	66	67	68	69
		36h		70	71	72	73	74			6Ah		70	71	72	73	74
		37h		75	76	77	78	79			6Bh		75	76	77	78	79
		38h		80	81	82	83	84			6Ch		80	81	82	83	84
		39h		85	86	87	88	89			6Dh		85	86	87	88	89
		3Ah		90	91	92	93	94			6Eh		90	91	92	93	94
		3Bh		95	96	97	98	99			6Fh		95	96	97	98	99
		3Ch	3	0	1	2	3	4			70h	12	0	1	2	3	4
		3Dh		5	6	7	8	9			71h		5	6	7	8	9
		3Eh		10	11	12	13	14			72h		10	11	12	13	14
		3Fh		15	16	17	18	19			73h		15	16	17	18	19
		40h		20	21	22	23	24			74h		20	21	22	23	24
		41h		25	26	27	28	29			75h		25	26	27	28	29
		42h		30	31	32	33	34			76h		30	31	32	33	34
		43h		35	36	37	38	39			77h		35	36	37	38	39
		44h		40	41	42	43	44			78h		40	41	42	43	44
		45h		45	46	47	48	49			79h		45	46	47	48	49
		46h		50	51	52	53	54			7Ah		50	51	52	53	54
		47h		55	56	57	58	59			7Bh		55	56	57	58	59
		48h		60	61	62	63	64			7Ch		60	61	62	63	64
		49h		65	66	67	68	69			7Dh		65	66	67	68	69

Table 31. Display RAM bitmap *…continued*

RAM bank	RAM bank select	RAM address	Row (Back-plane)	Column (segment) Bit					RAM bank	RAM bank select	RAM address	Row (Back-plane)	Column (segment) Bit				
	SMB[2:0]	ADD[6:0]		4	3	2	1	0		SMB[2:0]	ADD[6:0]		4	3	2	1	0
1	001	4Ah	3	70	71	72	73	74	2	010	7Eh	12	70	71	72	73	74
		4Bh		75	76	77	78	79			7Fh		75	76	77	78	79
		4Ch		80	81	82	83	84	3	011	0h		80	81	82	83	84
		4Dh		85	86	87	88	89			1h		85	86	87	88	89
		4Eh		90	91	92	93	94			2h		90	91	92	93	94
		4Fh		95	96	97	98	99			3h		95	96	97	98	99
		50h	4	0	1	2	3	4			4h	13	0	1	2	3	4
		51h		5	6	7	8	9			5h		5	6	7	8	9
		52h		10	11	12	13	14			6h		10	11	12	13	14
		53h		15	16	17	18	19			7h		15	16	17	18	19
		54h		20	21	22	23	24			8h		20	21	22	23	24
		55h		25	26	27	28	29			9h		25	26	27	28	29
		56h		30	31	32	33	34			Ah		30	31	32	33	34
		57h		35	36	37	38	39			Bh		35	36	37	38	39
		58h		40	41	42	43	44			Ch		40	41	42	43	44
		59h		45	46	47	48	49			Dh		45	46	47	48	49
		5Ah		50	51	52	53	54			Eh		50	51	52	53	54
		5Bh		55	56	57	58	59			Fh		55	56	57	58	59
		5Ch		60	61	62	63	64			10h		60	61	62	63	64
		5Dh		65	66	67	68	69			11h		65	66	67	68	69
		5Eh		70	71	72	73	74			12h		70	71	72	73	74
		5Fh		75	76	77	78	79			13h		75	76	77	78	79
		60h		80	81	82	83	84			14h		80	81	82	83	84
		61h		85	86	87	88	89			15h		85	86	87	88	89
		62h		90	91	92	93	94			16h		90	91	92	93	94
		63h		95	96	97	98	99			17h		95	96	97	98	99
		64h	5	0	1	2	3	4			18h	14	0	1	2	3	4
		65h		5	6	7	8	9			19h		5	6	7	8	9
		66h		10	11	12	13	14			1Ah		10	11	12	13	14
		67h		15	16	17	18	19			1Bh		15	16	17	18	19
		68h		20	21	22	23	24			1Ch		20	21	22	23	24
		69h		25	26	27	28	29			1Dh		25	26	27	28	29
		6Ah		30	31	32	33	34			1Eh		30	31	32	33	34
		6Bh		35	36	37	38	39			1Fh		35	36	37	38	39
		6Ch		40	41	42	43	44			20h		40	41	42	43	44
		6Dh		45	46	47	48	49			21h		45	46	47	48	49
		6Eh		50	51	52	53	54			22h		50	51	52	53	54
		6Fh		55	56	57	58	59			23h		55	56	57	58	59

Table 31. Display RAM bitmap *…continued*

RAM bank	RAM bank select	RAM address	Row (Back-plane)	Column (segment) Bit					RAM bank	RAM bank select	RAM address	Row (Back-plane)	Column (segment) Bit				
	SMB[2:0]	ADD[6:0]		4	3	2	1	0		SMB[2:0]	ADD[6:0]		4	3	2	1	0
1	001	70h	5	60	61	62	63	64	3	011	24h	14	60	61	62	63	64
		71h		65	66	67	68	69			25h		65	66	67	68	69
		72h		70	71	72	73	74			26h		70	71	72	73	74
		73h		75	76	77	78	79			27h		75	76	77	78	79
		74h		80	81	82	83	84			28h		80	81	82	83	84
		75h		85	86	87	88	89			29h		85	86	87	88	89
		76h		90	91	92	93	94			2Ah		90	91	92	93	94
		77h		95	96	97	98	99			2Bh		95	96	97	98	99
		78h	6	0	1	2	3	4			2Ch	15	0	1	2	3	4
		79h		5	6	7	8	9			2Dh		5	6	7	8	9
		7Ah		10	11	12	13	14			2Eh		10	11	12	13	14
		7Bh		15	16	17	18	19			2Fh		15	16	17	18	19
		7Ch		20	21	22	23	24			30h		20	21	22	23	24
		7Dh		25	26	27	28	29			31h		25	26	27	28	29
		7Eh		30	31	32	33	34			32h		30	31	32	33	34
		7Fh		35	36	37	38	39			33h		35	36	37	38	39
2	010	0h		40	41	42	43	44			34h		40	41	42	43	44
		1h		45	46	47	48	49			35h		45	46	47	48	49
		2h		50	51	52	53	54			36h		50	51	52	53	54
		3h		55	56	57	58	59			37h		55	56	57	58	59
		4h		60	61	62	63	64			38h		60	61	62	63	64
		5h		65	66	67	68	69			39h		65	66	67	68	69
		6h		70	71	72	73	74			3Ah		70	71	72	73	74
		7h		75	76	77	78	79			3Bh		75	76	77	78	79
		8h		80	81	82	83	84			3Ch		80	81	82	83	84
		9h		85	86	87	88	89			3Dh		85	86	87	88	89
		Ah		90	91	92	93	94			3Eh		90	91	92	93	94
		Bh		95	96	97	98	99			3Fh		95	96	97	98	99
		Ch	7	0	1	2	3	4			40h	16	0	1	2	3	4
		Dh		5	6	7	8	9			41h		5	6	7	8	9
		Eh		10	11	12	13	14			42h		10	11	12	13	14
		Fh		15	16	17	18	19			43h		15	16	17	18	19
		10h		20	21	22	23	24			44h		20	21	22	23	24
		11h		25	26	27	28	29			45h		25	26	27	28	29
		12h		30	31	32	33	34			46h		30	31	32	33	34
		13h		35	36	37	38	39			47h		35	36	37	38	39
		14h		40	41	42	43	44			48h		40	41	42	43	44
		15h		45	46	47	48	49			49h		45	46	47	48	49

Table 31. Display RAM bitmap *...continued*

RAM bank	RAM bank select	RAM address	Row (Back-plane)	Column (segment)				
	SMB[2:0]	ADD[6:0]		Bit 4	3	2	1	0
2	010	16h	7	50	51	52	53	54
		17h		55	56	57	58	59
		18h		60	61	62	63	64
		19h		65	66	67	68	69
		1Ah		70	71	72	73	74
		1Bh		75	76	77	78	79
		1Ch		80	81	82	83	84
		1Dh		85	86	87	88	89
		1Eh		90	91	92	93	94
		1Fh		95	96	97	98	99
		20h	8	0	1	2	3	4
		21h		5	6	7	8	9
		22h		10	11	12	13	14
		23h		15	16	17	18	19
		24h		20	21	22	23	24
		25h		25	26	27	28	29
		26h		30	31	32	33	34
		27h		35	36	37	38	39
		28h		40	41	42	43	44
		29h		45	46	47	48	49
		2Ah		50	51	52	53	54
		2Bh		55	56	57	58	59
		2Ch		60	61	62	63	64
		2Dh		65	66	67	68	69
		2Eh		70	71	72	73	74
		2Fh		75	76	77	78	79
		30h		80	81	82	83	84
		31h		85	86	87	88	89
		32h		90	91	92	93	94
		33h		95	96	97	98	99
3	011	4Ah	16	50	51	52	53	54
		4Bh		55	56	57	58	59
		4Ch		60	61	62	63	64
		4Dh		65	66	67	68	69
		4Eh		70	71	72	73	74
		4Fh		75	76	77	78	79
		50h		80	81	82	83	84
		51h		85	86	87	88	89
		52h		90	91	92	93	94
		53h		95	96	97	98	99
		54h	17	0	1	2	3	4
		55h		5	6	7	8	9
		56h		10	11	12	13	14
		57h		15	16	17	18	19
		58h		20	21	22	23	24
		59h		25	26	27	28	29
		5Ah		30	31	32	33	34
		5Bh		35	36	37	38	39
		5Ch		40	41	42	43	44
		5Dh		45	46	47	48	49
		5Eh		50	51	52	53	54
		5Fh		55	56	57	58	59
		60h		60	61	62	63	64
		61h		65	66	67	68	69
		62h		70	71	72	73	74
		63h		75	76	77	78	79
		64h		80	81	82	83	84
		65h		85	86	87	88	89
		66h		90	91	92	93	94
		67h		95	96	97	98	99

In multiplexed LCD applications, the data of each row of the display RAM is time-multiplexed with the corresponding backplane (row 0 with COM0, row 1 with COM1, and so on).

Two multiplex drive modes are available:

- 1:18 multiplex drive mode
  - GMX = 0 (default value, see Table 12)
  - pins COM0 to COM17 are active

- 1:12 multiplex drive mode
  - GMX = 1 (default value, see Table 12)
  - pins COM0 to COM12 are active

8.5.2.1 Display RAM addressing

For addressing the display RAM the following steps have to be taken:

- Select the display RAM bank (SMB[2:0]) with the Sel_mem_bank command (see Section 8.1.1.8)
- Set the requested address counter (ADD[6:0]) with the Set_mem_addr command (see Section 8.1.1.9)
- Write data to the display RAM with the Write_data command (WD[4:0]) (see Section 8.1.1.11)
- Read the data from the display RAM with the Read_data command (RD[4:0]) (see Section 8.1.1.10)

8.5.3 General-purpose RAM

The PCA8539 has to general-purpose RAM. The access to the RAM is controlled by the Sel_mem_bank command (SMB[2:0]) (see Table 13). General-purpose RAM 1 has the size of 640 bit (80 $\times$ 8) and general-purpose RAM 2 of 400 bit (80 $\times$ 5).

8.5.3.1 General-purpose RAM addressing

For addressing the general-purpose RAM the following steps have to be taken:

- Select the general-purpose RAM (SMB[2:0]) with the Sel_mem_bank command (see Section 8.1.1.8)
- Set the requested address counter (ADD[6:0]) with the Set_mem_addr command (see Section 8.1.1.9)
- Write data to the general-purpose RAM with the Write_data command (WD[7:0] or WD[4:0]) (see Section 8.1.1.11)
- Read the data from the general-purpose RAM with the Read_data command (RD[7:0] or RD[4:0]) (see Section 8.1.1.10)

9. Bus interfaces

9.1 Control byte and register selection

After initiating the communication over the bus and sending the slave address (I²C-bus, see Section 9.2) or subaddress (SPI-bus, see Section 9.3), a control byte follows. The purpose of this byte is to indicate both, the content for the following data bytes (RAM or command) and to indicate that more control bytes will follow.

Typical sequences could be:

- Slave address/subaddress - control byte - command byte - command byte - command byte - end
- Slave address/subaddress - control byte - RAM byte - RAM byte - RAM byte - end
- Slave address/subaddress - control byte - command byte - control byte - RAM byte - end

This allows sending a mixture of RAM and command data in one access or alternatively, to send just one type of data in one access. In this way, it is possible to configure the device and then fill the display RAM with little overhead. The display bytes are stored in the display RAM at the address specified by the data pointer.

Table 32. Control byte description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6 to 5	RS[1:0]		**register selection**
		00, 10, 11	command register
		01	RAM data
4 to 0	-	-	unused

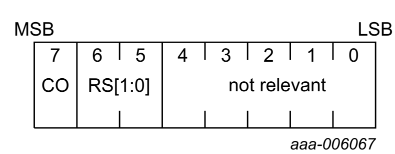


Fig 29. Control byte format

9.2 I²C interface

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

In Chip-On-Glass (COG) applications, where the track resistance between the SDA output pin to the system SDA input line can be significant, the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance may generate a voltage divider. As a consequence it may be possible that the acknowledge cycle, generated by the LCD driver, cannot be interpreted as logic 0 by the master. Therefore it is an advantage for COG applications to have the acknowledge output separated from the data line. For that reason, the SDA line of the PCA8539 is split into SDAIN and SDAOUT.

In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAOUT pin to the system SDAIN line to guarantee a valid LOW level.

By splitting the SDA line into SDAIN and SDAOUT (having the SDAOUT open circuit), the device could be used in a mode that ignores the acknowledge cycle. Separating the acknowledge output from the serial data line can avoid design efforts to generate a valid acknowledge level. However, in that case the I²C-bus master has to be set up in such a way that it ignores the acknowledge cycle.[2]

By connecting pin SDAOUT to pin SDAIN the SDAIN line becomes fully I²C-bus compatible (see Figure 30). The following definition assumes that SDAIN and SDAOUT are connected and refers to the pair as SDA.

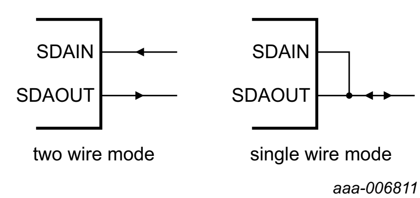


Fig 30. SDAOUT and SDAIN configuration

9.2.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as a control signal (see Figure 31).

2. For further information, consider the NXP application note: Ref. 1 "AN10170".

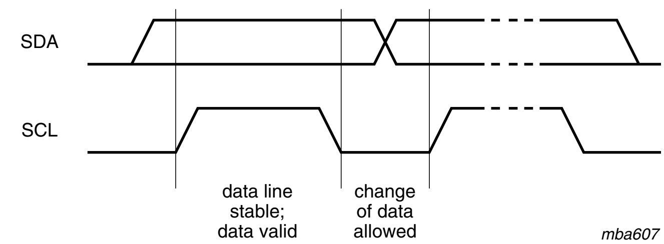


Fig 31. Bit transfer

9.2.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH is defined as the START condition (S).

A LOW-to-HIGH change of the data line while the clock is HIGH is defined as the STOP condition (P).

The START and STOP conditions are shown in Figure 32.

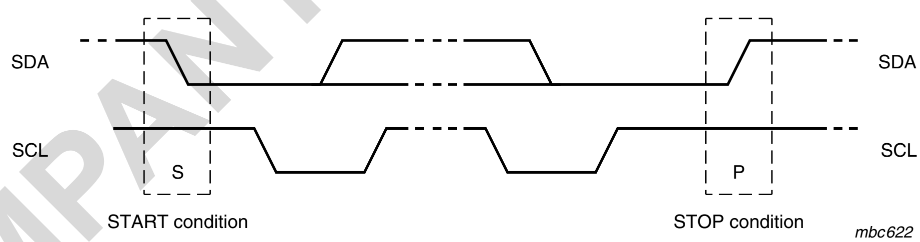


Fig 32. Definition of START and STOP conditions

9.2.3 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 33.

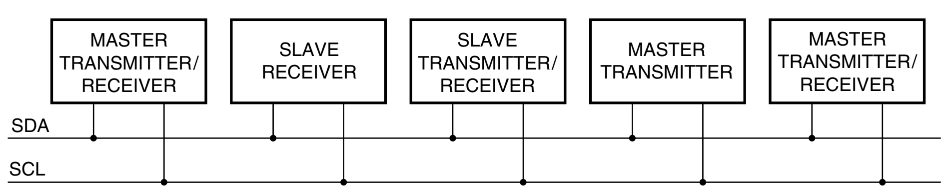


Fig 33. System configuration

9.2.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I²C-bus is shown in Figure 34.

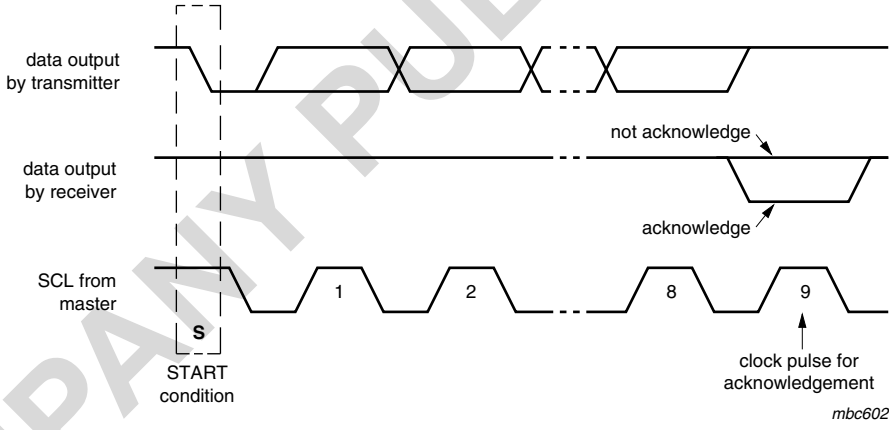


Fig 34. Acknowledgement on the I²C-bus

9.2.5 I²C-bus controller

The PCA8539 acts as an I²C-bus slave. It does not initiate I²C-bus transfers.

9.2.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

9.2.7 I²C-bus slave address

Device selection depends on the I²C-bus slave address.

Two different I²C-bus slave addresses can be used to address the PCA8539 (see Table 33).

Table 33. I²C slave address byte

Bit	Slave address							
	7 MSB	6	5	4	3	2	1	0 LSB
slave address	0	1	1	1	0	1	SA0	R/$\overline{W}$

The least significant bit of the slave address byte is bit R/$\overline{W}$ (see Table 34).

Table 34. $R/\overline{W}$-bit description

$R/\overline{W}$	Description
0	write data
1	read data

Bit 1 of the slave address is defined by connecting the input SA0 to either V_{SS1} (logic 0) or V_{DD1} (logic 1). Therefore, two instances of PCA8539 can be distinguished on the same I^2C-bus.

9.2.8 I^2C-bus protocol

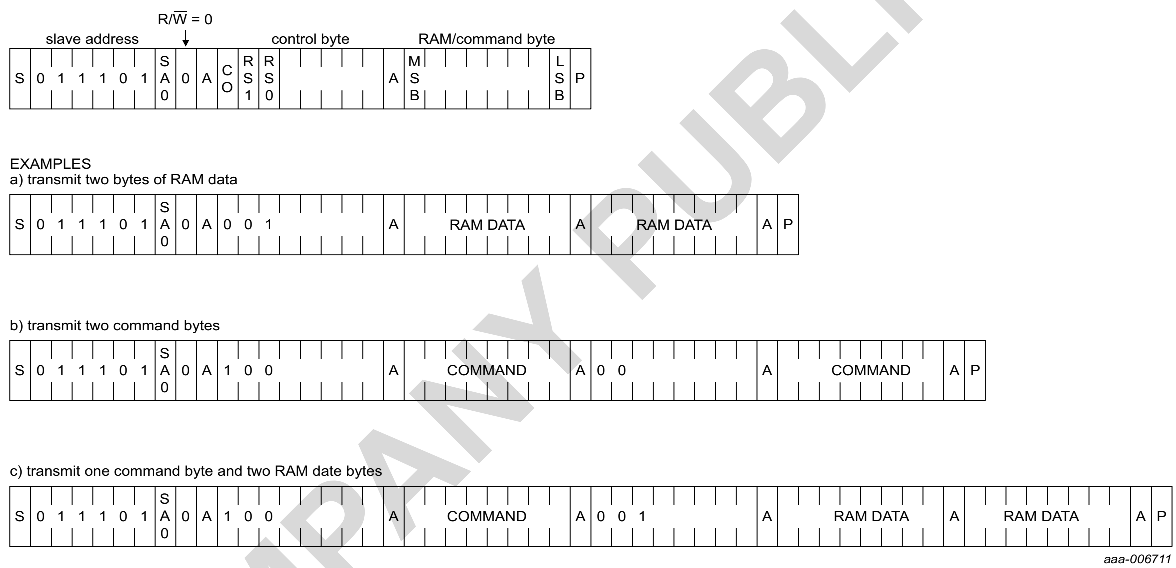


Fig 35. I^2C-bus protocol write mode

The I^2C-bus protocol is shown in Figure 35. The sequence is initiated with a START condition (S) from the I^2C-bus master which is followed by one of the two slave addresses available. All PCA8539 with the corresponding SA0 level acknowledge in parallel to the slave address, but all PCA8539 with the alternative SA0 level ignore the whole I^2C-bus transfer.

After acknowledgement, a control byte (see Section 9.1) follows which defines if the next byte is RAM or command information. The control byte also defines if the next byte is a control byte or further RAM or command data.

In this way, it is possible to configure the device and then fill the display RAM with little overhead.

The display bytes are stored in the display RAM at the address specified by the data pointer.

The acknowledgement after each byte is made only by the addressed PCA8539. After the last display byte, the I^2C-bus master issues a STOP condition (P). Alternatively a START may be issued to RESTART an I^2C-bus access.

If a register readout is made, the $R/\overline{W}$ bit must be logic 1 and then the next data byte following is provided by the PCA8539 as shown in Figure 36.

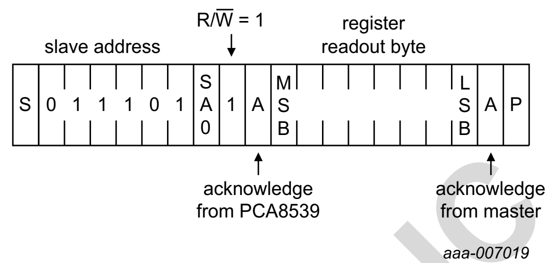


Fig 36. I²C-bus protocol read mode

9.3 SPI interface

Data transfer to the device is made via a four-line SPI-bus (see Table 35). The SPI-bus is initialized whenever the chip enable line pin $\overline{CE}$ is inactive.

Table 35. Serial interface

Symbol	Function	Description
$\overline{CE}$	chip enable input; active LOW[1]	when HIGH, the interface is reset
SCL	serial clock input	input may be higher than V_{DD1}
SDI/SDAIN	serial data input	input may be higher than V_{DD1}; input data is sampled on the rising edge of SCL
SDO	serial data output	

[1] The chip enable must not be wired permanently LOW.

9.3.1 SPI-bus data transfer

The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the MSB sent first.

The transmission is controlled by the active LOW chip enable signal $\overline{CE}$. The first byte transmitted is the subaddress byte.

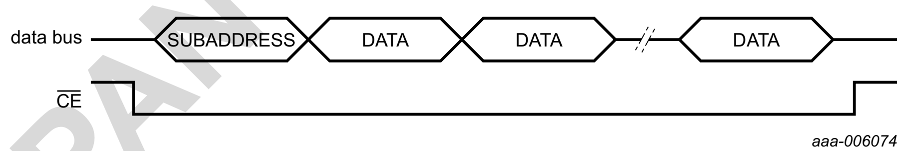


Fig 37. SPI data transfer overview

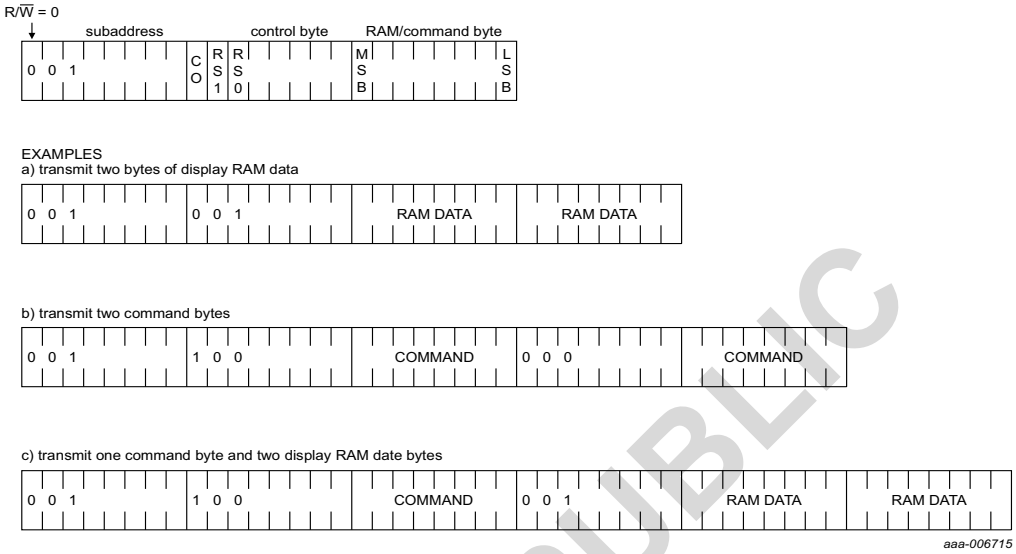
The subaddress byte opens the communication with a read/write bit and a subaddress. The subaddress is used to identify multiple devices on one SPI bus.

Table 36. Subaddress byte definition

Bit	Symbol	Value	Description
7	$R/\overline{W}$		**data read or write selection**
		0	write data
		1	read data
6 to 5	SA	01	**Subaddress**; other codes cause the device to ignore data transfer
4 to 0	-		unused

After the subaddress byte, a control byte follows (see Section 9.1). The purpose of this byte is to indicate the content for the following data bytes (RAM, command or control byte).

In this way, it is possible to send a mixture of RAM and command data in one access or alternatively, to send just one type of data in one access.



Data transfers are terminated by de-asserting $\overline{CE}$ (set $\overline{CE}$ to logic 1).

Fig 38. SPI-bus write example

10. Internal circuitry

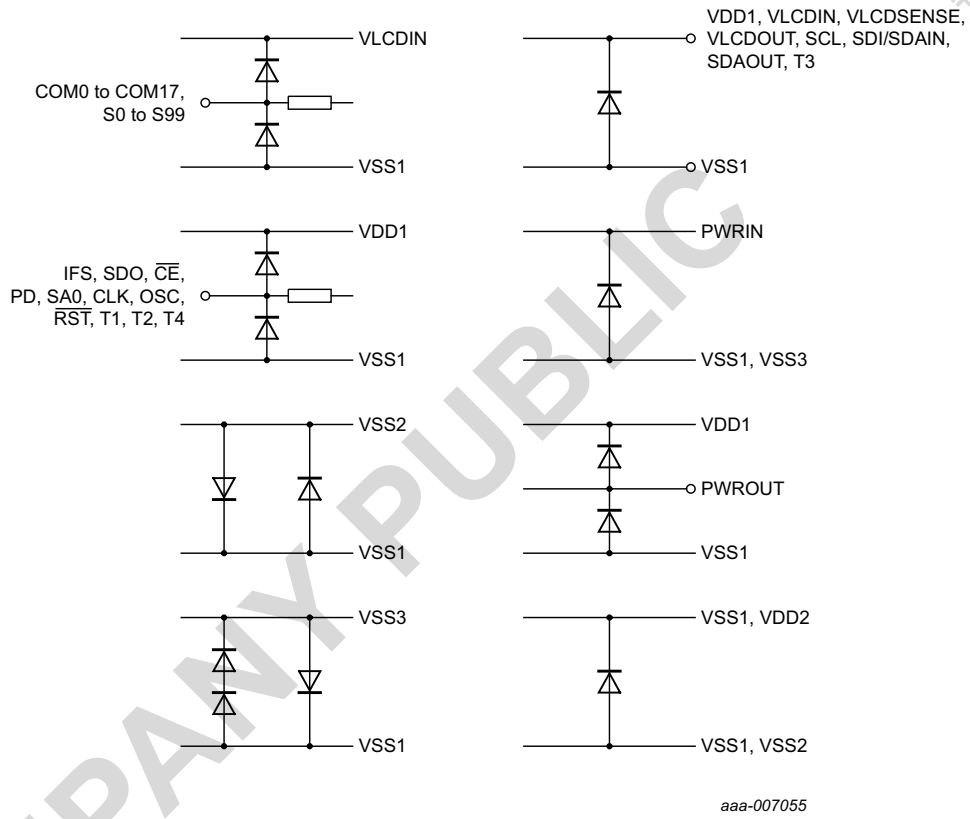


Fig 39. Device protection diagram

11. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

12. Limiting values

Table 37. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD1}	supply voltage 1	analog and digital		–0.5	+6.5	V
V_{DD2}	supply voltage 2	charge pump		–0.5	+6.5	V
I_{DD1}	supply current 1	analog and digital		–50	+50	mA
I_{DD2}	supply current 2	charge pump		–50	+50	mA
V_{LCD}	LCD supply voltage	external supply, input on pin VLCDIN		–0.5	+20	V
$I_{DD(LCD)}$	LCD supply current			–50	+50	mA
V_i	input voltage	on pins CLK, OSC, $\overline{RST}$, PD, IFS, SCL, SDI/SDAIN, SA0, $\overline{CE}$		–0.5	+6.5	V
		on pin VLCDSENSE		–0.5	+20	V
I_I	input current			–10	+10	mA
V_O	output voltage	on pins S0 to S99, COM0 to COM17, VLCDOUT		–0.5	+20	V
		on pins SDO, SDAOUT, CLK		–0.5	+6.5	V
I_O	output current			–10	+10	mA
I_{SS}	ground supply current			–50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P/out	power dissipation per output			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[1]	-	±3000	V
I_{lu}	latch-up current		[2]	-	100	mA
T_{stg}	storage temperature		[3]	–65	+150	°C
T_{amb}	ambient temperature	operating device		–40	+105	°C

[1] Pass level; Human Body Model (HBM), according to Ref. 7 "JESD22-A114".

[2] Pass level; latch-up testing according to Ref. 9 "JESD78" at maximum ambient temperature ($T_{amb(max)}$).

[3] According to the store and transport requirements (see Ref. 12 "UM10569") the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

13. Static characteristics

Table 38. Static characteristics

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD1}	supply voltage 1		2.5	-	5.5	V
V_{DD2}	supply voltage 2		2.5	-	5.5	V
V_{LCD}	LCD supply voltage	$V_{LCD} \geq V_{DD2}$				
		external supply, input on pin VLCDIN	4.0	-	16.0	V
		internal supply, output on pin VLCDOUT	4.0	-	16.0	V
I_{DD1}	supply current 1	on pin V_{DD1}; see Figure 40				
		default condition after power-on and Initialize command	-	40[1]	59[2]	µA
		display enabled; internal clock	-	95[1]	-	µA
I_{DD2}	supply current 2	on pin V_{DD2}				
		default condition after power-on and Initialize command; charge pump off	-	0	-	µA
		V_{DD2} = 5 V; charge pump at $V_{LCD} = 2 \times V_{DD2}$; V_{LCD} = 8 V; C_{VLCD} = 100 nF; display disabled; see Figure 41	-	25	-	µA
$I_{DD(LCD)}$	LCD supply current	on pin VLCDIN; external V_{LCD} = 8 V				
		display disabled	-	7	12	µA
		MUX 1:18; ¼ bias; f_{fr} = 80 Hz; all display elements on; frame inversion mode; display enabled; no display attached; see Figure 42	-	70	-	µA
$I_{DD(pd)}$	power-down mode supply current	on pin VDD1; pin PD is HIGH; V_{DD1} = 5 V; T_{amb} = 25 °C	-	2	-	µA

Table 38. Static characteristics *...continued*

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = –40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Accuracy						
ΔV_{LCD}	LCD voltage variation	on pin VLCDOUT; internal V_{LCD}; V_{LCD} = 8 V; T_{amb} = 25 °C; see Figure 43	7.9	8	8.1	V
Δf_{fr}	frame frequency variation	internal clock; f_{fr} = 80 Hz; T_{amb} = 25 °C; see Figure 44	77	80	83	Hz
ΔT_{meas}	measurement temperature variation	T_{amb} = 25 °C	22	25	28	°C
Output resistance						
R_o	output resistance	on pin COM0 to COM17; external V_{LCD} = 8 V	-	1	-	kΩ
		on pin S0 to S99; external V_{LCD} = 8 V	-	2.5	-	kΩ
Logic						
On pins CLK, OSC, PD, $\overline{RST}$, IFS, SA0						
V_{IL}	LOW-level input voltage		–0.3	-	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	-	V_{DD1} + 0.3	V
I_{LI}	input leakage current	V_I = V_{DD1} or V_{SS1}	-	0	-	µA
On pins CLK						
V_{OH}	HIGH-level output voltage		$0.8V_{DD1}$	-	V_{DD1} + 0.3	V
V_{OL}	LOW-level output voltage		–0.3	-	$0.2V_{DD1}$	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 4.6 V; V_{DD1} = 5 V	1	-	-	mA
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD1} = 5 V	1	-	-	mA
I_{LO}	output leakage current	V_O = V_{DD1} or V_{SS1}	-	0	-	µA
I^2C-bus						
On pins SCL, SDI/SDAIN						
V_{IL}	LOW-level input voltage		–0.3	-	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	-	5.5	V
I_{LI}	input leakage current	V_I = V_{DD1} or V_{SS1}	-	0	-	µA

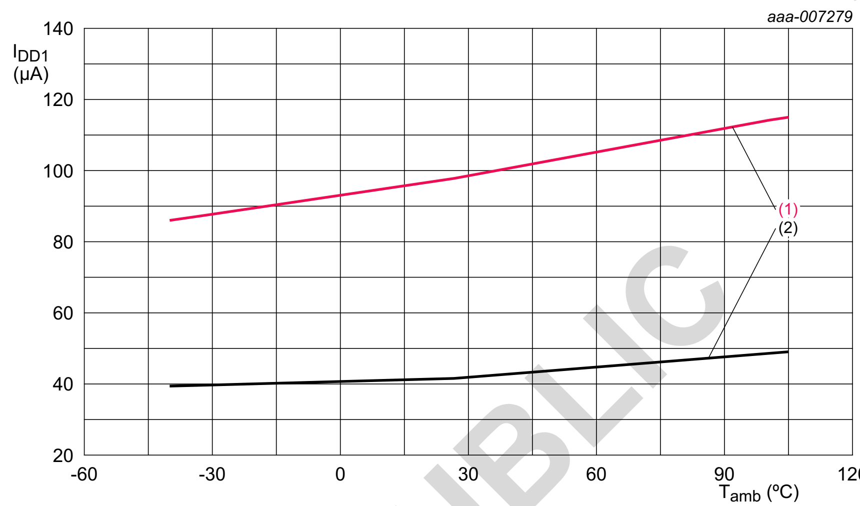
Table 38. Static characteristics *…continued*

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = –40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
On pin SDAOUT						
V_O	output voltage		–0.5	-	+5.5	V
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V	6	-	-	mA
I_{LI}	input leakage current	V_I = V_{DD1} or V_{SS1}	-	0	-	µA
I_{LO}	output leakage current	V_O = V_{SS1}	-	0	-	µA
SPI-bus						
On pins SCL, SDI/SDAIN, $\overline{CE}$						
V_{IL}	LOW-level input voltage		–0.3	-	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	-	V_{DD1} + 0.3	V
I_{LI}	input leakage current	V_I = V_{DD1} or V_{SS1}	-	0	-	µA
On pin SDO						
V_{OH}	HIGH-level output voltage		$0.8V_{DD1}$	-	V_{DD1} + 0.3	V
V_{OL}	LOW-level output voltage		–0.3	-	$0.2V_{DD1}$	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 4.6 V; V_{DD1} = 5 V	1	-	-	mA
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD1} = 5 V	1	-	-	mA
I_{LO}	output leakage current	V_O = V_{DD1} or V_{SS1}	-	0	-	µA

[1] V_{DD1} = 5 V; T_{amb} = 25 °C.

[2] V_{DD1} = 5.5 V; T_{amb} = 105 °C.

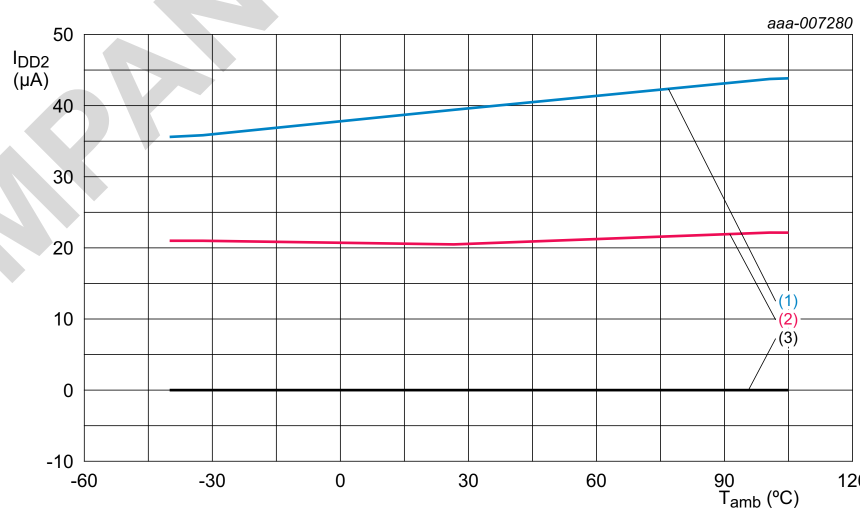


V_{DD1} = 5 V.

(1) Display enabled, oscillator enabled.

(2) Default conditions after power-on and initialization.

Fig 40. Typical I_{DD1} with respect to temperature

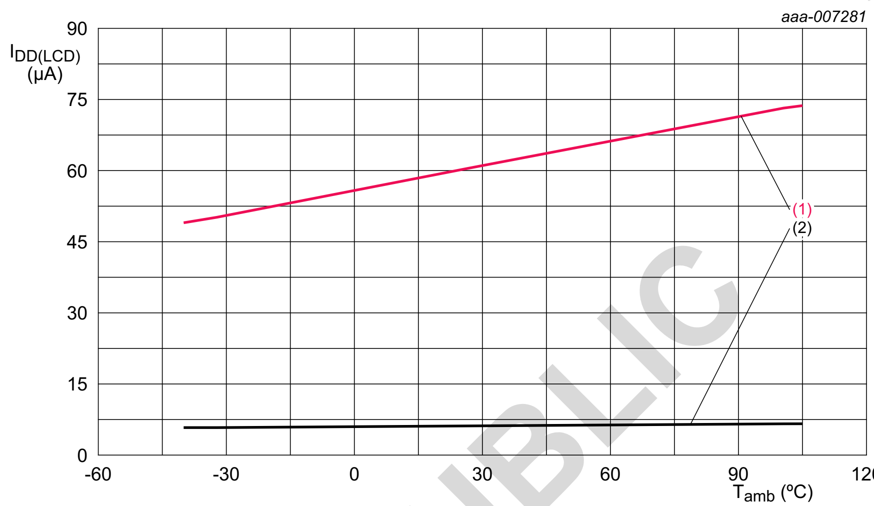


(1) V_{DD2} = 3 V; charge pump at $V_{LCD} = 3 \times V_{DD2}$; V_{LCD} = 8 V; C_{VLCD} = 100 nF; display disabled.

(2) V_{DD2} = 5 V; charge pump at $V_{LCD} = 2 \times V_{DD2}$; V_{LCD} = 8 V; C_{VLCD} = 100 nF; display disabled.

(3) Default conditions after power-on and initialization; charge pump off.

Fig 41. Typical I_{DD2} with respect to temperature

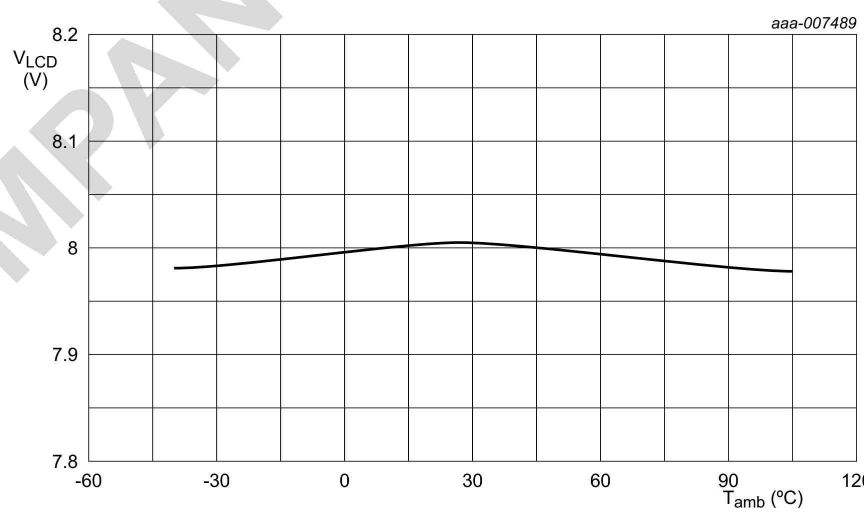


External V_{LCD} = 8 V.

(1) Driving mode 1:18, f_{fr} = 80 Hz; frame inversion; no load; display enabled.

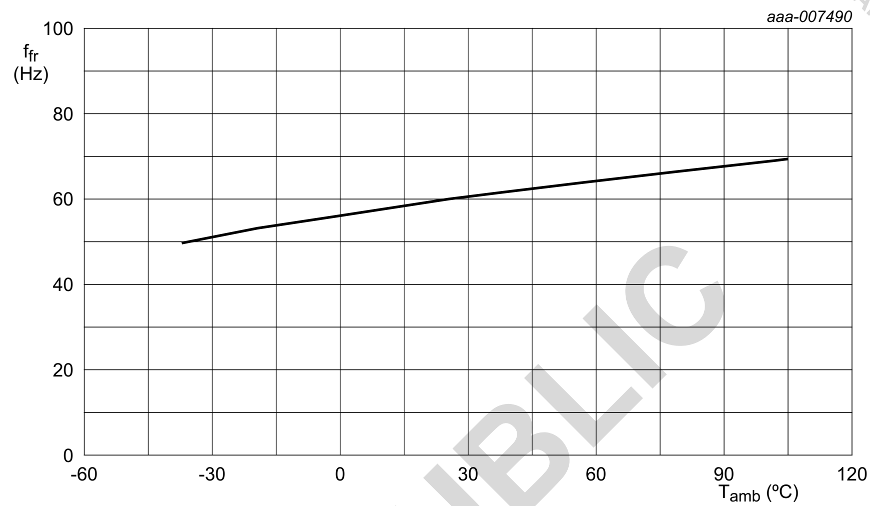
(2) Driving mode 1:18, f_{fr} = 80 Hz; frame inversion; no load; display disabled.

Fig 42. Typical $I_{DD(LCD)}$ with respect to temperature



Conditions: V_{DD2} = 5 V; charge pump at V_{LCD} = 2 × V_{DD2}; V_{LCD} = 8 V; VLCD[8:0] = 134h; temperature compensation disabled.

Fig 43. Typical V_{LCD} variation with respect to temperature



Conditions: frame frequency prescaler = 00111; 80 Hz typical.

Fig 44. Typical frame frequency variation with respect to temperature

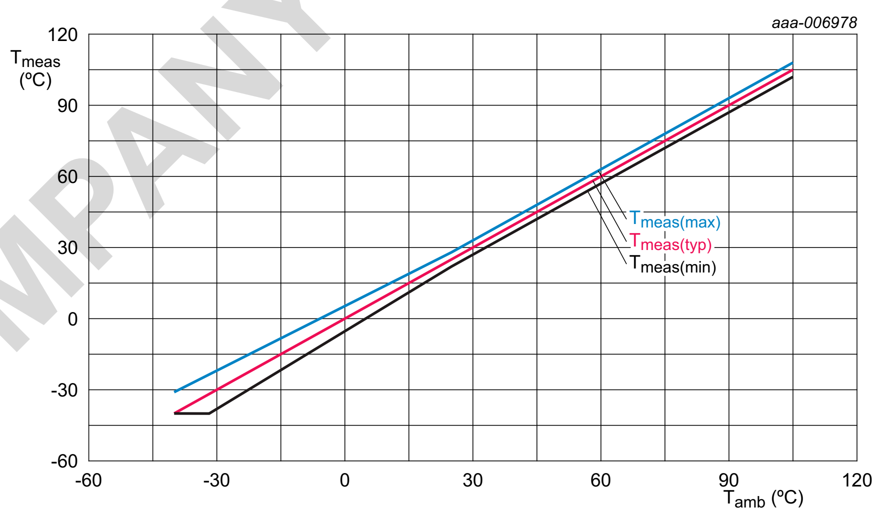


Fig 45. Measurement temperature variation with respect to temperature

14. Dynamic characteristics

14.1 General timing characteristics

Table 39. General dynamic characteristics

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = –40 °C to +105 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{clk(int)}$	internal clock frequency	on pin CLK; T_{amb} = 25 °C; FF[4:0] = 00111	61600	64000	66400	Hz
$f_{clk(ext)}$	external clock frequency	on pin CLK	36000	-	288000	Hz
$t_{clk(H)}$	HIGH-level clock time	external clock source used	5	-	-	µs
$t_{clk(L)}$	LOW-level clock time		5	-	-	µs

14.2 I²C-bus timing characteristics

Table 40. I²C-bus timing characteristics

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = –40 °C to +105 °C; unless otherwise specified.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL frequency		-	-	400	kHz
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	-	-	µs
$t_{VD;DAT}$	data valid time	[2]	-	-	0.9	µs
$t_{VD;ACK}$	data valid acknowledge time	[3]	-	-	0.9	µs
t_{LOW}	LOW period of the SCL clock		1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	-	-	µs
t_f	fall time	of both SDA and SCL signals	-	-	0.3	µs
t_r	rise time	of both SDA and SCL signals	-	-	0.3	µs
C_b	capacitive load for each bus line		-	-	400	pF
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
$t_{w(spike)}$	spike pulse width		-	-	50	ns

[1] All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS1} to V_{DD1}.

[2] $t_{VD;DAT}$ = minimum time for valid SDA output following SCL LOW.

[3] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output LOW.

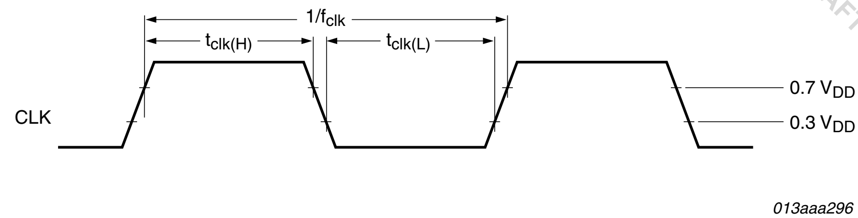


Fig 46. Driver timing waveforms

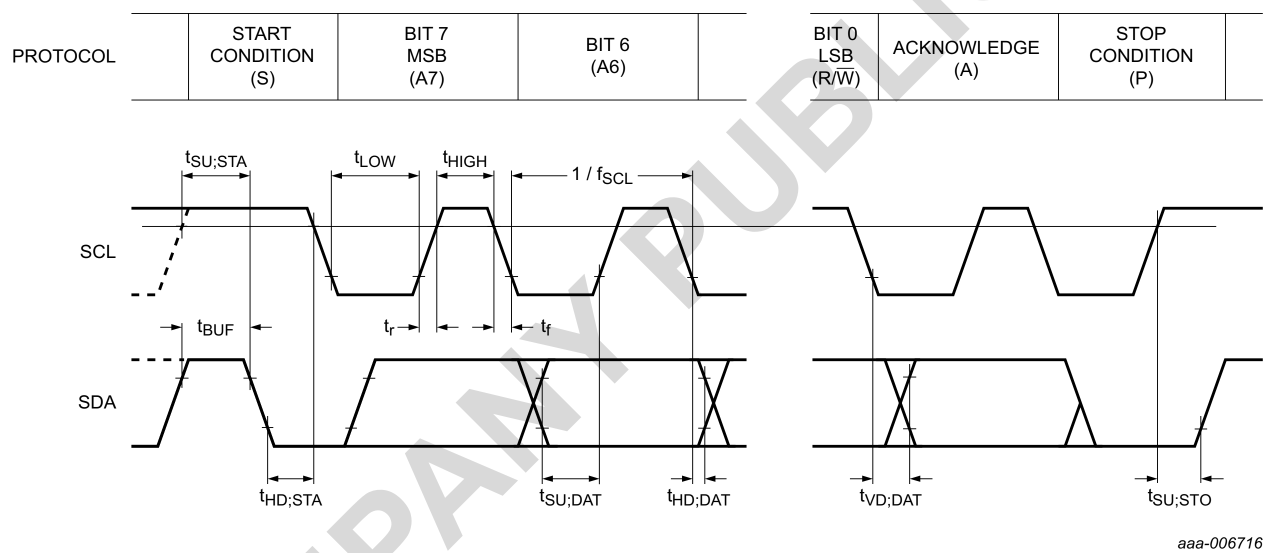


Fig 47. I²C-bus timing diagram

14.3 SPI-bus timing characteristics

Table 41. SPI-bus characteristics

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS1} to V_{DD1} (see Figure 48).

Symbol	Parameter	Conditions	Min	Max	Unit
Pin SCL					
$f_{clk(SCL)}$	SCL clock frequency		-	3.0	MHz
t_{SCL}	SCL time		333	-	ns
$t_{clk(H)}$	clock HIGH time		100	-	ns
$t_{clk(L)}$	clock LOW time		150	-	ns
t_r	rise time	for SCL signal	-	100	ns
t_f	fall time	for SCL signal	-	100	ns
Pin $\overline{CE}$					
$t_{su(CE\_N)}$	CE_N set-up time		30	-	ns
$t_{h(CE\_N)}$	CE_N hold time		30	-	ns
$t_{rec(CE\_N)}$	CE_N recovery time		30	-	ns

Table 41. SPI-bus characteristics *...continued*

V_{DD1}, V_{DD2} = 2.5 V to 5.5 V; V_{SS1} = 0 V; V_{LCD} = 4.0 V to 16.0 V; T_{amb} = −40 °C to +105 °C; unless otherwise specified. All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS1} to V_{DD1} (see Figure 48).

Symbol	Parameter	Conditions	Min	Max	Unit
Pin SDI					
t_{su}	set-up time	set-up time for SDI data	30	-	ns
t_h	hold time	hold time for SDI data	30	-	ns
Pin SDO					
$t_{d(R)SDO}$	SDO read delay time	C_L = 100 pF	-	150	ns
$t_{dis(SDO)}$	SDO disable time	[1]	-	50	ns
$t_{t(SDI-SDO)}$	transition time from SDI to SDO	to avoid bus conflict	0	-	ns

[1] No load value; bus is held up by bus capacitance; use RC time constant with application values.

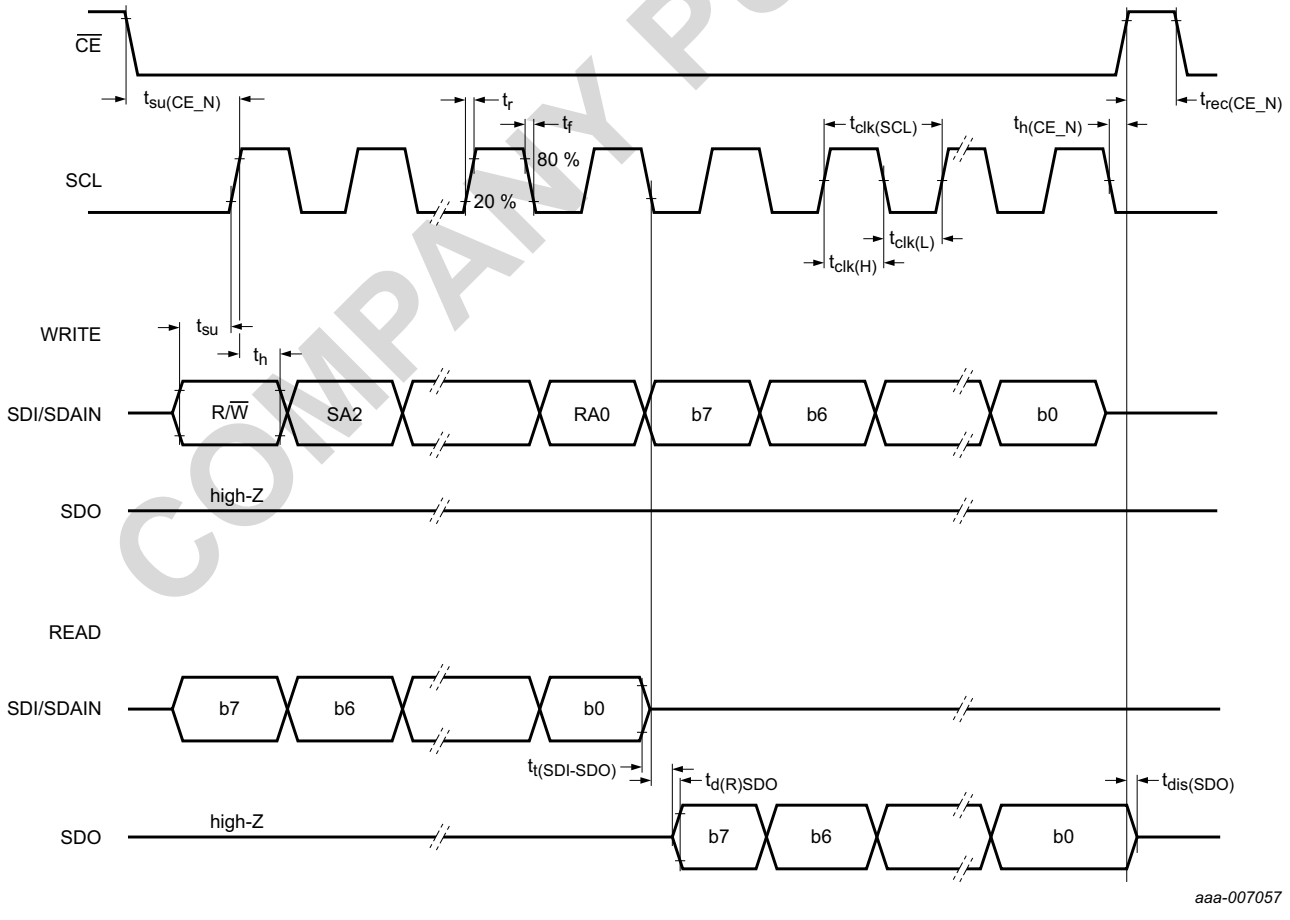


Fig 48. SPI-bus timing

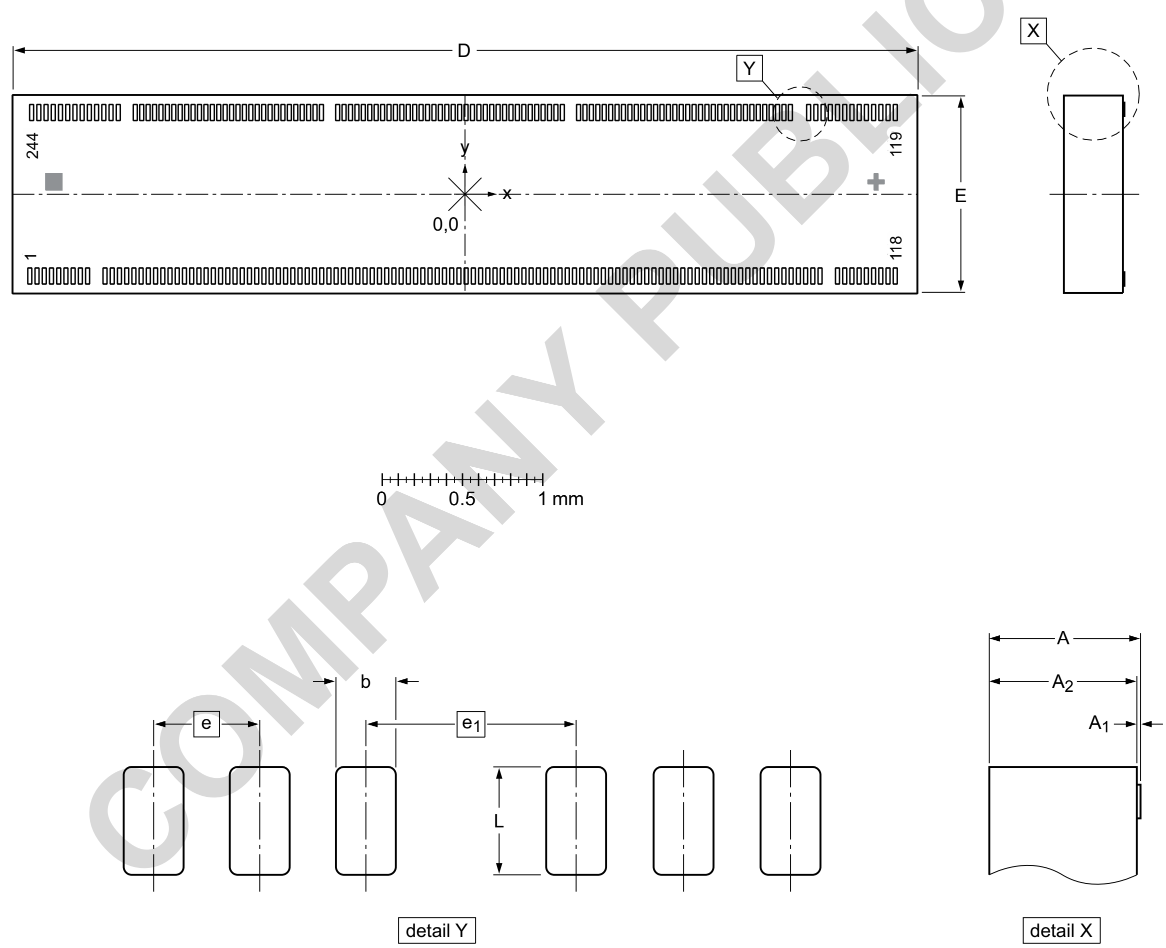
15. Test information

15.1 Quality information

This product has been qualified to the appropriate Automotive Electronics Council (AEC) standard Q100 or Q101 and is suitable for use in automotive applications.

16. Bare die outline

Bare die; 244 bumps | PCA8539DUG



Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCA8539DUG						~~13-03-20~~ 13-06-18

Fig 49. Bare die outline of PCA8539DUG

Table 42. Dimensions of PCA8539DUG

Original dimensions are in mm.

Unit (mm)	A	A_1	A_2	b	D	E	e	e_1	L
max	-	0.018	-	-	-	-	-	-	-
nom	0.395	0.015	0.38	0.025	5.64	1.24	0.040	0.114	0.1
min	-	0.012	-	-	-	-	-	-	-

Table 43. Bump locations of PCA8539DUG

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 49

Symbol	Pin	Coordinates		Pitch	Symbol	Pin	Coordinates		Pitch
		X (µm)	Y (µm)	X (µm)			X (µm)	Y (µm)	X (µm)
COM13	1	-2711.3	-509.0	-	COM4	119	2681.5	509.0	-
	2	-2666.3	-509.0	-45.0		120	2636.5	509.0	45.0
	3	-2621.3	-509.0	-45.0		121	2591.5	509.0	45.0
COM14	4	-2576.3	-509.0	-45.0	COM3	122	2546.5	509.0	45.0
	5	-2531.3	-509.0	-45.0		123	2501.5	509.0	45.0
COM15	6	-2486.3	-509.0	-45.0	COM2	124	2456.5	509.0	45.0
	7	-2441.3	-509.0	-45.0		125	2411.5	509.0	45.0
COM16	8	-2396.3	-509.0	-45.0	COM1	126	2366.5	509.0	45.0
	9	-2351.3	-509.0	-45.0		127	2321.5	509.0	45.0
VLCDIN	10	-2242.7	-509.0	-108.6	COM0	128	2276.5	509.0	45.0
	11	-2197.7	-509.0	-45.0		129	2231.5	509.0	45.0
	12	-2152.7	-509.0	-45.0	COM17	130	2186.5	509.0	45.0
	13	-2107.7	-509.0	-45.0		131	2141.5	509.0	45.0
VLCDSENSE	14	-2062.7	-509.0	-45.0	S99	132	2027.9	509.0	113.6
	15	-2017.7	-509.0	-45.0	S98	133	1987.9	509.0	40.0
	16	-1972.7	-509.0	-45.0	S97	134	1947.9	509.0	40.0
VLCDOUT	17	-1927.7	-509.0	-45.0	S96	135	1907.9	509.0	40.0
	18	-1882.7	-509.0	-45.0	S95	136	1867.9	509.0	40.0
	19	-1837.7	-509.0	-45.0	S94	137	1827.9	509.0	40.0
	20	-1792.7	-509.0	-45.0	S93	138	1787.9	509.0	40.0
VSS2	21	-1747.7	-509.0	-45.0	S92	139	1747.9	509.0	40.0
	22	-1702.7	-509.0	-45.0	S91	140	1707.9	509.0	40.0
	23	-1657.7	-509.0	-45.0	S90	141	1667.9	509.0	40.0
	24	-1612.7	-509.0	-45.0	S89	142	1627.9	509.0	40.0
	25	-1567.7	-509.0	-45.0	S88	143	1587.9	509.0	40.0
	26	-1522.7	-509.0	-45.0	S87	144	1547.9	509.0	40.0
	27	-1477.7	-509.0	-45.0	S86	145	1507.9	509.0	40.0
	28	-1432.7	-509.0	-45.0	S85	146	1467.9	509.0	40.0
	29	-1387.7	-509.0	-45.0	S84	147	1427.9	509.0	40.0
	30	-1342.7	-509.0	-45.0	S83	148	1387.9	509.0	40.0

Table 43. Bump locations of PCA8539DUG *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 49

Symbol	Pin	Coordinates		Pitch	Symbol	Pin	Coordinates		Pitch
		X (µm)	Y (µm)	X (µm)			X (µm)	Y (µm)	X (µm)
VSS3	31	-1297.7	-509.0	-45.0	S82	149	1347.9	509.0	40.0
	32	-1252.7	-509.0	-45.0	S81	150	1307.9	509.0	40.0
	33	-1207.7	-509.0	-45.0	S80	151	1267.9	509.0	40.0
	34	-1162.7	-509.0	-45.0	S79	152	1227.9	509.0	40.0
VSS1	35	-1117.7	-509.0	-45.0	S78	153	1187.9	509.0	40.0
	36	-1072.7	-509.0	-45.0	S77	154	1147.9	509.0	40.0
	37	-1027.7	-509.0	-45.0	S76	155	1107.9	509.0	40.0
	38	-982.7	-509.0	-45.0	S75	156	1067.9	509.0	40.0
	39	-937.7	-509.0	-45.0	S74	157	1027.9	509.0	40.0
	40	-892.7	-509.0	-45.0	S73	158	987.9	509.0	40.0
	41	-847.7	-509.0	-45.0	S72	159	947.9	509.0	40.0
	42	-802.7	-509.0	-45.0	S71	160	907.9	509.0	40.0
	43	-757.7	-509.0	-45.0	S70	161	867.9	509.0	40.0
	44	-712.7	-509.0	-45.0	S69	162	827.9	509.0	40.0
	45	-667.7	-509.0	-45.0	S68	163	787.9	509.0	40.0
	46	-622.7	-509.0	-45.0	S67	164	747.9	509.0	40.0
	47	-577.7	-509.0	-45.0	S66	165	707.9	509.0	40.0
T1	48	-532.7	-509.0	-45.0	S65	166	606.9	509.0	101.0
	49	-487.7	-509.0	-45.0	S64	167	566.9	509.0	40.0
T2	50	-442.7	-509.0	-45.0	S63	168	526.9	509.0	40.0
	51	-397.7	-509.0	-45.0	S62	169	486.9	509.0	40.0
T4	52	-352.7	-509.0	-45.0	S61	170	446.9	509.0	40.0
	53	-307.7	-509.0	-45.0	S60	171	406.9	509.0	40.0
	54	-262.7	-509.0	-45.0	S59	172	366.9	509.0	40.0
OSC	55	-217.7	-509.0	-45.0	S58	173	326.9	509.0	40.0
	56	-172.7	-509.0	-45.0	S57	174	286.9	509.0	40.0
SA0	57	-127.7	-509.0	-45.0	S56	175	246.9	509.0	40.0
	58	-82.7	-509.0	-45.0	S55	176	206.9	509.0	40.0
IFS	59	-37.7	-509.0	-45.0	S54	177	166.9	509.0	40.0
	60	7.3	-509.0	-45.0	S53	178	126.9	509.0	40.0
VDD1	61	52.3	-509.0	-45.0	S52	179	86.9	509.0	40.0
	62	97.3	-509.0	-45.0	S51	180	46.9	509.0	40.0
	63	142.3	-509.0	-45.0	S50	181	6.9	509.0	40.0
	64	187.3	-509.0	-45.0	S49	182	-33.1	509.0	40.0
	65	232.3	-509.0	-45.0	S48	183	-73.1	509.0	40.0

Table 43. Bump locations of PCA8539DUG *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 49

Symbol	Pin	Coordinates		Pitch	Symbol	Pin	Coordinates		Pitch
		X (μm)	Y (μm)	X (μm)			X (μm)	Y (μm)	X (μm)
VDD2	66	277.3	-509.0	-45.0	S47	184	-113.1	509.0	40.0
	67	322.3	-509.0	-45.0	S46	185	-153.1	509.0	40.0
	68	367.3	-509.0	-45.0	S45	186	-193.1	509.0	40.0
	69	412.3	-509.0	-45.0	S44	187	-233.1	509.0	40.0
	70	457.3	-509.0	-45.0	S43	188	-273.1	509.0	40.0
	71	502.3	-509.0	-45.0	S42	189	-313.1	509.0	40.0
	72	547.3	-509.0	-45.0	S41	190	-353.1	509.0	40.0
	73	592.3	-509.0	-45.0	S40	191	-393.1	509.0	40.0
PD	74	637.3	-509.0	-45.0	S39	192	-433.1	509.0	40.0
	75	682.3	-509.0	-45.0	S38	193	-473.1	509.0	40.0
T3	76	727.3	-509.0	-45.0	S37	194	-513.1	509.0	40.0
	77	772.3	-509.0	-45.0	S36	195	-553.1	509.0	40.0
	78	817.3	-509.0	-45.0	S35	196	-593.1	509.0	40.0
	79	862.3	-509.0	-45.0	S34	197	-633.1	509.0	40.0
	80	907.3	-509.0	-45.0	S33	198	-673.1	509.0	40.0
PWROUT	81	952.3	-509.0	-45.0	S32	199	-713.1	509.0	40.0
	82	997.3	-509.0	-45.0	S31	200	-753.1	509.0	40.0
PWRIN	83	1042.3	-509.0	-45.0	S30	201	-793.1	509.0	40.0
	84	1087.3	-509.0	-45.0	S29	202	-894.1	509.0	101.0
	85	1132.3	-509.0	-45.0	S28	203	-934.1	509.0	40.0
	86	1177.3	-509.0	-45.0	S27	204	-974.1	509.0	40.0
	87	1222.3	-509.0	-45.0	S26	205	-1014.1	509.0	40.0
	88	1267.3	-509.0	-45.0	S25	206	-1054.1	509.0	40.0
	89	1312.3	-509.0	-45.0	S24	207	-1094.1	509.0	40.0
$\overline{CE}$	90	1357.3	-509.0	-45.0	S23	208	-1134.1	509.0	40.0
	91	1402.3	-509.0	-45.0	S22	209	-1174.1	509.0	40.0
CLK	92	1447.3	-509.0	-45.0	S21	210	-1214.1	509.0	40.0
	93	1492.3	-509.0	-45.0	S20	211	-1254.1	509.0	40.0
	94	1537.3	-509.0	-45.0	S19	212	-1294.1	509.0	40.0
$\overline{RST}$	95	1582.3	-509.0	-45.0	S18	213	-1334.1	509.0	40.0
	96	1627.3	-509.0	-45.0	S17	214	-1374.1	509.0	40.0
SDI/SDAIN	97	1672.3	-509.0	-45.0	S16	215	-1414.1	509.0	40.0
	98	1717.3	-509.0	-45.0	S15	216	-1454.1	509.0	40.0
	99	1762.3	-509.0	-45.0	S14	217	-1494.1	509.0	40.0
SDO	100	1807.3	-509.0	-45.0	S13	218	-1534.1	509.0	40.0
	101	1852.3	-509.0	-45.0	S12	219	-1574.1	509.0	40.0

Table 43. Bump locations of PCA8539DUG *…continued*

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 49

Symbol	Pin	Coordinates		Pitch	Symbol	Pin	Coordinates		Pitch
		X (µm)	Y (µm)	X (µm)			X (µm)	Y (µm)	X (µm)
SCL	102	1897.3	-509.0	-45.0	S11	220	-1614.1	509.0	40.0
	103	1942.3	-509.0	-45.0	S10	221	-1654.1	509.0	40.0
	104	1987.3	-509.0	-45.0	S9	222	-1694.1	509.0	40.0
SDAOUT	105	2032.3	-509.0	-45.0	S8	223	-1734.1	509.0	40.0
	106	2077.3	-509.0	-45.0	S7	224	-1774.1	509.0	40.0
	107	2122.3	-509.0	-45.0	S6	225	-1814.1	509.0	40.0
	108	2167.3	-509.0	-45.0	S5	226	-1854.1	509.0	40.0
	109	2212.3	-509.0	-45.0	S4	227	-1894.1	509.0	40.0
COM17	110	2320.9	-509.0	-108.6	S3	228	-1934.1	509.0	40.0
	111	2365.9	-509.0	-45.0	S2	229	-1974.1	509.0	40.0
COM7	112	2410.9	-509.0	-45.0	S1	230	-2014.1	509.0	40.0
	113	2455.9	-509.0	-45.0	S0	231	-2054.1	509.0	40.0
COM6	114	2500.9	-509.0	-45.0	COM16	232	-2160.2	509.0	106.1
	115	2545.9	-509.0	-45.0		233	-2205.2	509.0	45.0
COM5	116	2590.9	-509.0	-45.0	COM8	234	-2250.2	509.0	45.0
	117	2635.9	-509.0	-45.0		235	-2295.2	509.0	45.0
	118	2680.9	-509.0	-45.0	COM9	236	-2340.2	509.0	45.0
-	-	-	-	-		237	-2385.2	509.0	45.0
-	-	-	-	-	COM10	238	-2430.2	509.0	45.0
-	-	-	-	-		239	-2475.2	509.0	45.0
-	-	-	-	-	COM11	240	-2520.2	509.0	45.0
-	-	-	-	-		241	-2565.2	509.0	45.0
-	-	-	-	-	COM12	242	-2610.2	509.0	45.0
-	-	-	-	-		243	-2655.2	509.0	45.0
-	-	-	-	-		244	-2700.2	509.0	45.0

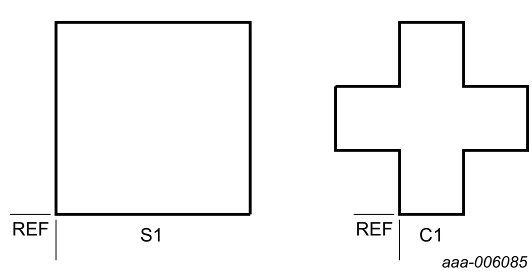


Fig 50. Alignment marks

Table 44. Alignment marking

All x/y coordinates represent the position of the REF point (see Figure 50) with respect to the center (x/y = 0) of the chip; see Figure 49.

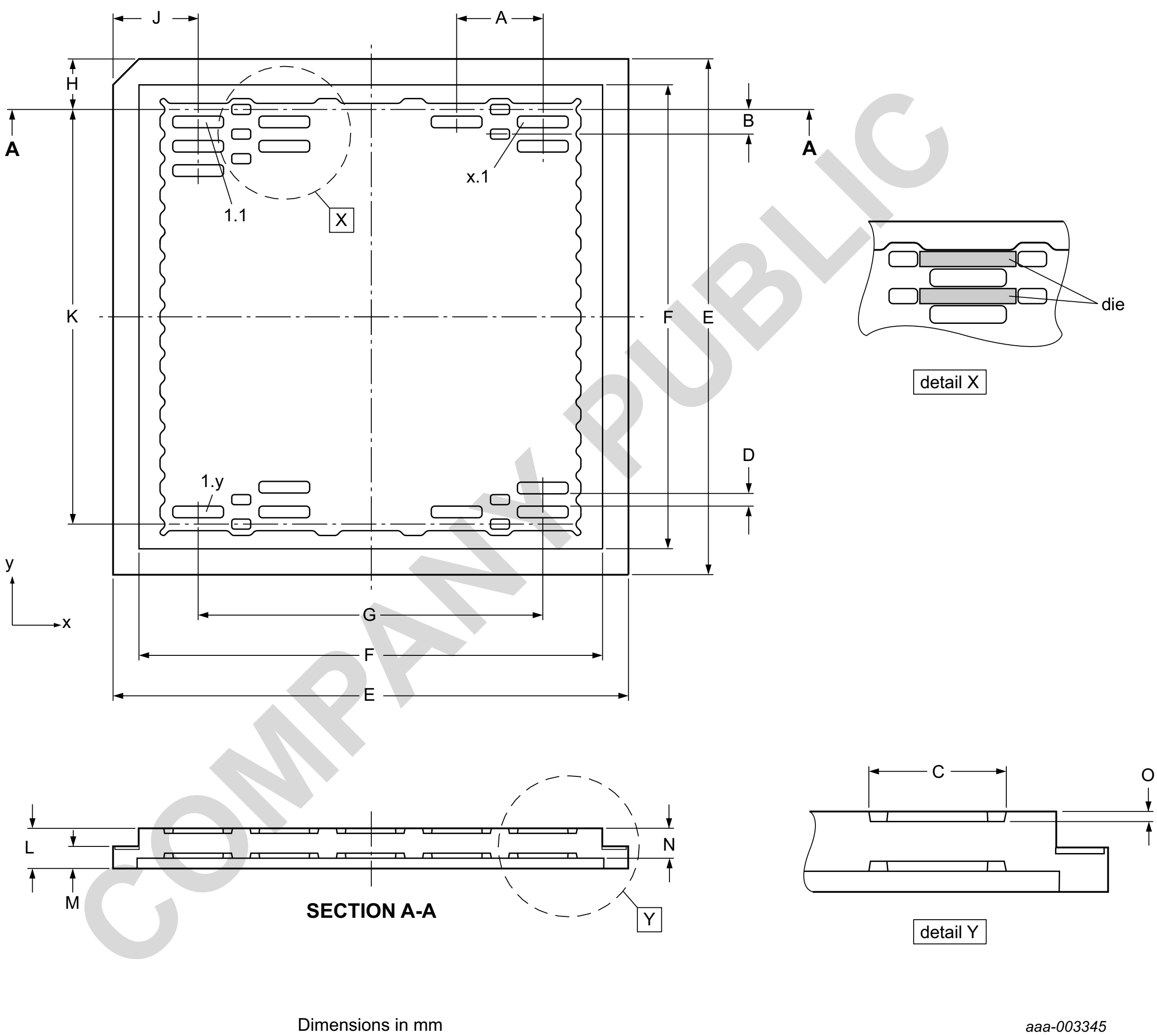
Symbol	Size (μm)	X (μm)	Y (μm)
S1	90 × 90	–2585.0	36.0
C1	90 × 90	2522.0	36

17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

18. Packing information

18.1 Packing information on the tray



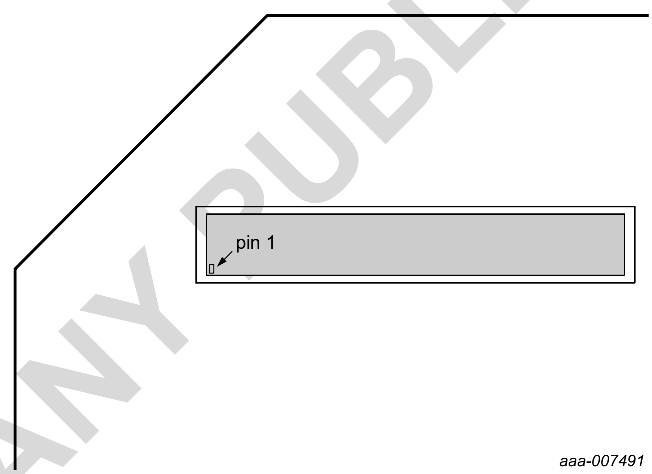
Schematic drawing, not drawn to scale. Top side view. For dimensions, see Table 45. Tray has pockets on both, top side and bottom side. The IC is stored with the active side up. To get the active side down, turn the tray.

Fig 51. Tray details of PCA8539U

Table 45. Specification of 3 inch tray details

Tray details are shown in Figure 51. Nominal values without production tolerances.

Tray details														
Dimensions														
A	B	C	D	E	F	G	H	J	K	L	M	N	O	Unit
7.0	2.5	5.74	1.34	76.0	68.0	56.0	6.75	10.0	62.5	4.2	2.6	3.2	0.48	mm
Number of pockets														
x direction							y direction							
9							26							



The orientation of the IC in a pocket with active side up is indicated by the position of pin 1 with respect to the chamfer on the upper left corner of the tray.

Fig 52. Die alignment in the tray

19. Appendix

19.1 LCD segment driver selection

Table 46. Selection of LCD segment drivers

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	f_{fr} (Hz)	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCF8566TS	24	48	72	96	-	-	-	2.5 to 6	2.5 to 6	N	N	69	–40 to 85	I^{2}C	VSO40	N
PCF85162T	32	64	96	128	-	-	-	1.8 to 5.5	2.5 to 6.5	N	N	82	–40 to 85	I^{2}C	TSSOP48	N
PCA85162T	32	64	96	128	-	-	-	1.8 to 5.5	2.5 to 8	N	N	110	–40 to 95	I^{2}C	TSSOP48	Y
PCF8551ATT[6]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	N	N	32, 64, 96, 128[1]	–40 to 85	I^{2}C	TSSOP48	N
PCF8551BTT[6]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	N	N	32, 64, 96, 128[1]	–40 to 85	SPI	TSSOP48	N
PCF85176T	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	N	N	82	–40 to 85	I^{2}C	TSSOP56	N
PCA85176T	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	N	N	110	–40 to 95	I^{2}C	TSSOP56	Y
PCF85176H	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	N	N	82	–40 to 85	I^{2}C	TQFP64	N
PCA85176H	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	N	N	82	–40 to 95	I^{2}C	TQFP64	Y
PCA8546ATT[5]	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	N	N	60 to 300[1]	–40 to 95	I^{2}C	TSSOP56	Y
PCA8546BTT[5]	-	-	-	176	-	-	-	1.8 to 5.5	2.5 to 9	N	N	60 to 300[1]	–40 to 95	SPI	TSSOP56	Y
PCA8547AHT[3][5]	44	88		176	-	-	-	1.8 to 5.5	2.5 to 9	Y	Y	60 to 300[1]	–40 to 85	I^{2}C	TQFP64	Y
PCA8547BHT[3][5]	44	88		176	-	-	-	1.8 to 5.5	2.5 to 9	Y	Y	60 to 300[1]	–40 to 95	SPI	TQFP64	Y
PCF85134HL	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 6.5	N	N	82	–40 to 85	I^{2}C	LQFP80	N
PCA85134H	60	120	180	240	-	-	-	1.8 to 5.5	2.5 to 8	N	N	82	–40 to 95	I^{2}C	LQFP80	Y
PCF8545ATT[5]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	N	N	60 to 300[1]	–40 to 85	I^{2}C	TSSOP56	N
PCF8545BTT[5]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 5.5	N	N	60 to 300[1]	–40 to 85	SPI	TSSOP56	N
PCF8536AT[4]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	N	N	60 to 300[1]	–40 to 85	I^{2}C	TSSOP56	N
PCF8536BT[4]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	N	N	60 to 300[1]	–40 to 85	SPI	TSSOP56	N
PCA8536AT[4]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	N	N	60 to 300[1]	–40 to 95	I^{2}C	TSSOP56	Y
PCA8536BT[4]	-	-	-	176	252	320	-	1.8 to 5.5	2.5 to 9	N	N	60 to 300[1]	–40 to 95	SPI	TSSOP56	Y
PCF8537AH[3]	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	Y	Y	60 to 300[1]	–40 to 85	I^{2}C	TQFP64	N
PCF8537BH[3]	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	Y	Y	60 to 300[1]	–40 to 85	SPI	TQFP64	N
PCA8537AH[3]	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	Y	Y	60 to 300[1]	–40 to 95	I^{2}C	TQFP64	Y

Table 46. Selection of LCD segment drivers *...continued*

Type name	Number of elements at MUX							V_{DD} (V)	V_{LCD} (V)	V_{LCD} (V) charge pump	V_{LCD} (V) temperature compensat.	f_{fr} (Hz)	T_{amb} (°C)	Interface	Package	AEC-Q100
	1:1	1:2	1:3	1:4	1:6	1:8	1:9									
PCA8537BH[3]	44	88	-	176	276	352	-	1.8 to 5.5	2.5 to 9	Y	Y	60 to 300[1]	–40 to 95	SPI	TQFP64	Y
PCA9620H[3]	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	Y	Y	60 to 300[1]	–40 to 105	I^2C	LQFP80	Y
PCA9620U[3]	60	120	-	240	320	480	-	2.5 to 5.5	2.5 to 9	Y	Y	60 to 300[1]	–40 to 105	I^2C	bare die	Y
PCF8552DUG[6]	36	72	108	144	-	-	-	1.8 to 5.5	1.8 to 5.5	N	N	32, 64, 96, 128[1]	–40 to 85	I^2C	bare die	N
PCF8576DU	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	N	N	77	–40 to 85	I^2C	bare die	N
PCF8576EUG	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 6.5	N	N	77	–40 to 85	I^2C	bare die	N
PCA8576FUG[5]	40	80	120	160	-	-	-	1.8 to 5.5	2.5 to 8	N	N	200	–40 to 105	I^2C	bare die	Y
PCF85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 6.5	N	N	82, 110[2]	–40 to 85	I^2C	bare die	N
PCA85133U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	N	N	82, 110[2]	–40 to 95	I^2C	bare die	Y
PCA85233U	80	160	240	320	-	-	-	1.8 to 5.5	2.5 to 8	N	N	150,220[2]	–40 to 105	I^2C	bare die	Y
PCF85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	N	N	60 to 90[1]	–40 to 85	I^2C	bare die	N
PCA85132U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	N	N	60 to 90[1]	–40 to 95	I^2C	bare die	Y
PCA85232U	160	320	480	640	-	-	-	1.8 to 5.5	1.8 to 8	N	N	117 to 176[1]	–40 to 95	I^2C	bare die	Y
PCF8538UG[5][3]	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	Y	Y	45 to 300[1]	–40 to 85	I^2C, SPI[2]	bare die	N
PCA8538UG[3]	102	204	-	408	612	816	918	2.5 to 5.5	4 to 12	Y	Y	45 to 300[1]	–40 to 105	I^2C, SPI[2]	bare die	Y

[1] Can be selected by command.

[2] Can be selected by pin configuration.

[3] Extra feature: Temperature sensor.

[4] Extra feature: 6 PWM channels.

[5] In development. Expected product release end of 2013.

[6] In development. Expected product release mid of 2014.

20. Abbreviations

Table 47. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
CRC	Cyclical Redundancy Check
COG	Chip-On-Glass
DC	Direct Current
EMC	ElectroMagnetic Compatibility
ESD	ElectroStatic Discharge
HBM	Human Body Model
I^2C	Inter-Integrated Circuit bus
IC	Integrated Circuit
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MSB	Most Significant Bit
MUX	Multiplexer
OTP	One Time Programmable
PCB	Printed-Circuit Board
RC	Resistance-Capacitance
RAM	Random Access Memory
RMS	Root Mean Square
SCL	Serial CLock line
SDA	Serial DAta line
SPI	Serial Peripheral Interface
TC	Temperature Coefficient

21. References

[1] **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2] **AN10439 —** Wafer Level Chip Size Package

[3] **AN10706 —** Handling bare die

[4] **AN10853 —** ESD and EMC sensitivity of IC

[5] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[6] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[7] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[8] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[9] **JESD78 —** IC Latch-Up Test

[10] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[11] **UM10204 —** I^2C-bus specification and user manual

[12] **UM10569 —** Store and transport requirements

22. Revision history

Table 48. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA8539 v.0.04	<tbd>	Objective data sheet	-	PCA8539 v.0.03
Modifications:	• added security note section • adjusted clock frequency values • adjusted LCD supply current value • corrected bare die outline drawing • adjusted rise and fall time values in SPI-bus spec			
PCA8539 v.0.03	20130426	Objective data sheet	-	PCA8539 v.0.02
PCA8539 v.0.02	20130423	Objective data sheet	-	PCA8539 v.0.01
PCA8539 v.0.01	-	Objective data sheet	-	-

23. Legal information

23.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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25. Tables

26. Figures

27. Contents

continued >>

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