Section 1 Electrical Specifications (Preliminary)

1.1 Overview

The specifications in this section are for devices operating under the following conditions. Where a special condition is required for a given specification, the condition will be indicated. Furthermore, the specifications in this section are not guaranteed unless the conditions listed below are met.

1.1.1 Pin Groups

Symbol	Pin Group Supplied by	Related Pins/Ports
PgE	EVCC, EVSS	Related ports: JP0, P0, P8, P9, P10, P11 Related pins: $\overline{\text{RESET}}$, FLMD0
PgA0	A0VREF, A0VSS	Related port: AP0

1.1.2 General Measurement Conditions

1.1.2.1 Common Conditions

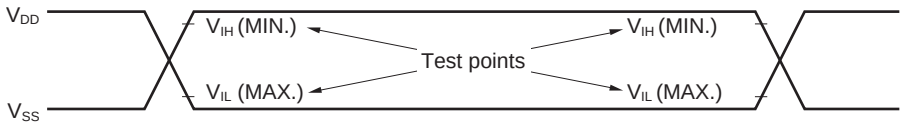
- Power supply
  - REGVCC = EVCC = VPOC to 5.5 V
  - For the characteristics of the following sections, REGVCC = EVCC = 3.0 to 5.5 V
    1.9, **1.11**, **1.12**, **1.13**, **1.14**, **1.15**, **1.16**, **1.17**, **1.18**, **1.19**, **1.20**, **1.21**, **1.22**, **1.23**, **1.27**, **1.29**
  - A0VREF = 3.0 V to 5.5 V
  - AWOVSS = ISOVSS = EVSS = A0VSS = 0 V
- Capacitance of the internal regulator
  - AWOVCL: 0.1 µF +/– 30%
  - ISOVCL: 0.1 µF +/– 30%
- Operating temperature
  - Ta = –40 to +125°C
- Load conditions
  - CL = 30 pF

NOTE

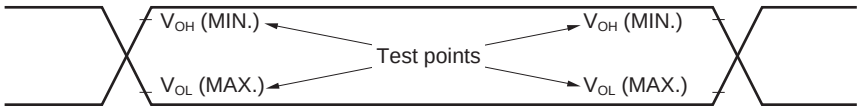
"VPOC" means POC (power on clear) detection voltage. For more detail, refer to **Section 1.24, POC Characteristics**.

1.1.2.2 AC Characteristic Measurement Condition

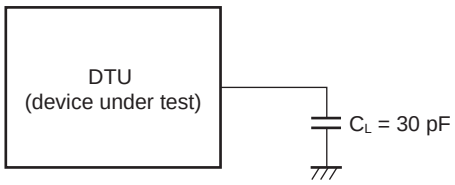
(1) AC test input measurement points



(2) AC test output measurement points



(3) Load conditions



CAUTION

If the load capacitance exceeds 30pF due to the circuit configuration, it is recommended to insert a buffer in order to reduce capacitance till less than 30pF.

1.2 Absolute Maximum Ratings

CAUTIONS

1. **Do not directly connect outputs (or input/outputs) to each other or to VDD, VCC, or GND.**
2. **Even momentarily exceeding the absolute maximum rating for just one item creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings. The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.**
3. **When designing an external circuit ensure that the connections don't conflict with the port state of this device.**

1.2.1 Supply Voltages

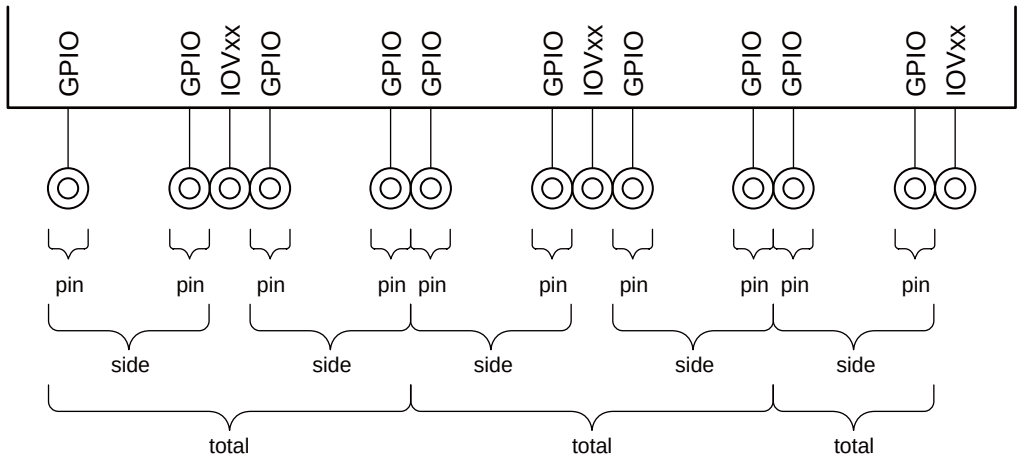
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System supply voltage	REGVCC		–0.5		6.5	V
	AWOVSS		–0.5		0.5	V
	ISOVSS		–0.5		0.5	V
Port supply voltage	EVCC		–0.5		6.5	V
	EVSS		–0.5		0.5	V
A/D-converter supply voltage	A0VREF		–0.5		6.5	V
	A0VSS		–0.5		0.5	V

1.2.2 Port Voltages

Item	Pin Group*1	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	PgE	VI		–0.5		EVCC + 0.5 (Do not exceed 6.5 V)	V
	PgA0			–0.5		A0VREF + 0.5 (Do not exceed 6.5 V)	V

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

1.2.3 Port Current



Definition of the condition:

- **Per pin:** Output current of one GPIO
- **Per side:** Total output current of all GPIO pins on one side of one IOVxx
- **Total:** Total output current of both sides of one IOVxx

Note:

- **GPIO:** General-purpose I/O pin (JP0_0 to 5, P0_0 to 14, P8_0 to 12, P9_0 to 6, P10_0 to 15, P11_0 to 7, AP0_0 to 15)
- **IOVxx:** Power supply pin for I/O pins (EVCC, EVSS, A0VREF, A0VSS)

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per pin			–10	mA
			Per side (Total of P9_0 to P9_6)			–48	mA
			Per side (Total of P10_6 to P10_9)			–40	mA
			Per side (Total of P10_10 to P10_14, P11_1 to P11_7)			–48	mA
			Per side (Total of P10_0 to P10_2)			–30	mA
			Per side (Total of P0_0 to P0_3, P10_3 to P10_5, P10_15, P11_0)			–48	mA
			Per side (Total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P8_2, P8_10 to P8_12)			–48	mA
			Per side (Total of JP0_0 to JP0_2)			–30	mA
			Per side (Total of P0_7 to P0_10, P8_0, P8_1, P8_3 to P8_9			–48	mA
			Total (EVCC)			–60	mA
		PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
Low-level output current	IOL	PgE	Per pin			10	mA
			Per side (Total of P9_0 to P9_6)			48	mA
			Per side (Total of P10_6 to P10_14, P11_1, P11_2)			48	mA
			Per side (Total of P11_3 to P11_7)			48	mA
			Per side (Total of P10_0 to P10_2)			30	mA
			Per side (Total of P0_0 to P0_6, P0_11 to P0_14, P10_3 to P10_5, P10_15, P11_0)			48	mA
			Per side (Total of JP0_0 to JP0_5, P8_2, P8_10 to P8_12)			48	mA
			Per side (Total of P0_7 to P0_10)			40	mA
			Per side (Total of P8_0, P8_1, P8_3 to P8_9)			48	mA
			Total (EVSS)			60	mA
		PgA0	Per pin			10	mA
			Total (A0VSS)			48	mA

1.2.4 Temperature condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Storage temperature	Tstg		–55		170	°C
Operating ambient temperature	Ta	R7F7010212AFP	–40		85	°C
		R7F7010222AFP	–40		85	°C
		R7F7010232AFP	–40		85	°C
		R7F7010242AFP	–40		85	°C
		R7F7010252AFP	–40		85	°C
		R7F7010353AFP	–40		105	°C
		R7F7010213AFP	–40		105	°C
		R7F7010223AFP	–40		105	°C
		R7F7010233AFP	–40		105	°C
		R7F7010243AFP	–40		105	°C
		R7F7010354AFP	–40		125	°C
		R7F7010214AFP	–40		125	°C
		R7F7010224AFP	–40		125	°C
		R7F7010234AFP	–40		125	°C
		R7F7010244AFP	–40		125	°C

1.3 Capacitance

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI*1	f = 1 MHz 0 V for non measurement pins			10	pF
Input/output capacitance	CIO*2				10	pF

Note 1. CI: Capacitance between the input pin and ground

Note 2. CIO: Capacitance between input/output pin and ground

1.4 Operational Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f_{CPUCLK}				80	MHz
Peripheral clock frequency					*1	MHz
Power supply*3	REGVCC EVCC		VPOC *2		5.5	V
	A0VREF*4		3.0		5.5	V

Note 1. For maximum frequency of peripherals, refer to Section 10, Clock Controller, in the RH850/F1L Group User's Manual: Hardware.

Note 2. “VPOC” means POC (power on clear) detection voltage (typ. 2.95V@at power-on, typ. 2.9V@after (except) power-on). For detail, refer to **Section 1.24, POC Characteristics**.

Note 3. This item shows the power supply range only. The operational condition of power supply voltage shows <Common condition> of **Section 1.1.2, General Measurement Conditions**

Note 4. When the terminal of P8 and P9 is used as analog input, it is necessary to A0VREF = EVCC.

1.5 Oscillator Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MainOsc frequency	f_{MOSC}	Crystal/Ceramic	8		24	MHz
MainOsc oscillation stabilization time	t_{MSTB}	EMCLK is operated by High Speed Internal Oscillator	0*1		17.9*1	ms
		EMCLK is operated by Low Speed Internal Oscillator	0*1		593.7 *1	ms

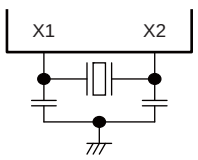
Note 1. Oscillator stabilization time depends on value of MOSCST register. Select appropriate stabilization time in accordance with oscillator specifications.

CAUTION

The oscillation stabilization time differs according the matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by an oscillator matching test.

NOTE

Recommended oscillator circuit is shown below.



1.6 Internal Oscillator Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LS IntOsc frequency	f_{RL}		220.8	240	259.2	kHz
HS IntOsc frequency	f_{RH}		7.36	8	8.64	MHz
		Ta = 25°C	7.6	8	8.4	MHz
HS IntOsc oscillation stabilization time	t_{RHSTB}	ROSCST = 0100_B*1	15.5	16.7	18.2	µs

Note 1. Set 0100_B in ROSCST register.

1.7 PLL Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input frequency	$f_{PLLICLK}$		8		24	MHz
Output frequency (PLL for CPU)	f_{CPLL}		25		80	MHz
Output frequency (PLL for Peripheral)	f_{PPLL}		25		80	MHz
Lock time	t_{LCKP}		104.0	112.3	122.1	µs

Note: PLL jitter*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output period jitter	t_{CPJ}	par = 4*2	–150		150	ps
		par = 8*2	–250		250	ps
		par = 16*2	–300		300	ps
Long term jitter	t_{LTJ}	term = 1 µs	–500		500	ps
		term = 10 µs	–1		1	ns
		term = 20 µs	–2		2	ns

Note 1. This specification is based on simulation and not tested during outgoing inspection.
Note 2. “par” is set by PA[2:0] bit of PLLC register.

1.8 Regulator Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	REGVCC		VPOC*1		5.5	V
Output voltage	AWOVCL		1.1	1.25	1.35	V
	ISOVCL		1.1	1.25	1.35	V
Capacitance	CAWOVCL	AWOVCL pin	0.07	0.10	0.13	µF
	CISOVCL	ISOVCL pin	0.07	0.10	0.13	µF
Voltage gradient	RAVS	REGVCC = 0 V → 3.0 V	0.02		500	V/ms

Note 1. “VPOC” means POC (power on clear) detection voltage (typ. 2.95V@at power-on, typ. 2.9V@after (except) power-on).
For detail, refer to **Section 1.24, POC Characteristics**.

1.9 Pin Characteristics

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH	CMOS		0.65 × IOVCC		IOVCC + 0.3	V
		SHMT1(except FLMD0 pin)		0.7 × IOVCC		IOVCC + 0.3	V
		SHMT1(FLMD0 pin)*2		0.66 × EVCC		EVCC + 0.3	V
		SHMT2		0.75 × IOVCC		IOVCC + 0.3	V
		SHMT4		0.8 × IOVCC		IOVCC + 0.3	V
Low level input voltage	VIL	CMOS		–0.3		0.35 × IOVCC	V
		SHMT1		–0.3		0.3 × IOVCC	V
		SHMT2		–0.3		0.25 × IOVCC	V
		SHMT4		–0.3		0.5 × IOVCC	V
Input hysteresis for Schmitt	VH	SHMT1		0.3			V
		SHMT2		0.2 × IOVCC			V
		SHMT4		0.1			V
Input leakage current	ILIH	VI = IOVCC*1				0.5	µA
	ILIL	VI = 0 V*1				–0.5	µA
Internal pull-up resistance	RU			20 (275 µA)	40	100	kΩ
Internal pull-down resistance	RD			20 (275 µA)	40	100	kΩ
High level output voltage*6	VOH	Fast mode (40 MHz mode)					
			IOH = –5 mA (6 pins)*3	IOVCC – 1.0			V
			IOH = –3 mA (10 pins)*3	IOVCC – 1.0			V
			IOH = –1 mA (16 pins)*3	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins)*3	IOVCC – 0.5			V
		Slow mode (10 MHz mode)					
			IOH = –1 mA (16 pins)*3	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins)*3	IOVCC – 0.5			V
Low level output voltage*6	VOL	Fast mode (40 MHz mode)					
			IOL = 5 mA (6 pins)*3			0.4	V
			IOL = 3 mA (10 pins)*3			0.4	V
			IOL = 1 mA (16 pins)*3			0.4	V
		Slow mode (10 MHz mode)					
			IOL = 1 mA (16 pins)*3			0.4	V
Output frequency	f_O	Slow mode	CL = 30 pF			10	MHz
			CL = 50 pF			6	MHz
			CL = 100 pF			3	MHz
		Fast mode, except below pins	CL = 30 pF			40	MHz
			CL = 50 pF			24	MHz
			CL = 100 pF			12	MHz
		Fast mode, P0_2 and P0_3	CL = 30 pF			80	MHz
Rise/Fall time	t_{KRP}/t_{KFP}	Slow mode	CL = 30 pF*3			37	ns
			CL = 50 pF*3			62	ns
			CL = 100 pF*3			124	ns
		Fast mode (Except below pins)	CL = 30 pF*3			7	ns
			CL = 50 pF*3			12	ns
			CL = 100 pF*3			24	ns
		Fast mode, P0_2 and P0_3	CL = 100 pF*4			6.15	ns

Note: "IOVCC" means the pins are assigned to the power supply (EVCC and A0VREF).

Note 1. Not select the analog input function of ADCn.

Note 2. When the internal pull-up resistor of FLMD0 pin is applied by FLMDCNT register, please connect 95 kΩ or more as external pull-down resistor. In addition, this external pull-down resistor is possible to correspond of special spec.

Note 3. The number of pin indicates simultaneous ON.
Measurement point: 0.1 × VDD 5 V to 0.9 × VDD 5 V

Note 4. Measurement point: 0.2 × VDD 5 V to 0.8 × VDD 5 V

Note 5. Except AP0

Note 6. The total current of IOH/IOL is shown in the following table.

Item	Symbol	Pin Group	Condition	MIN.	TYP.	MAX.	Unit
High-level output current	IOH	PgE	Per side (Total of P9_0 to P9_6)			–7	mA
			Per side (Total of P10_6 to P10_9)			–20	mA
			Per side (Total of P10_10 to P10_14, P11_1 to P11_7)			–30	mA
			Per side (Total of P10_0 to P10_2)			–15	mA
			Per side (Total of P0_0 to P0_3, P10_3 to P10_5, P10_15, P11_0)			–30	mA
			Per side (Total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P8_2, P8_10 to P8_12)			–30	mA
			Per side (Total of JP0_0 to JP0_2)			–3	mA
			Per side (Total of P0_7 to P0_10, P8_0, P8_1, P8_3 to P8_9			–17	mA
			Total (EVCC)			–60	mA
		PgA0	Total (A0VREF)			–16	mA
Low-level output current	IOL	PgE	Per side (Total of P9_0 to P9_6)			7	mA
			Per side (Total of P10_6 to P10_14, P11_1, P11_2)			30	mA
			Per side (Total of P11_3 to P11_7)			25	mA
			Per side (Total of P10_0 to P10_2)			15	mA
			Per side (Total of P0_0 to P0_6, P0_11 to P0_14, P10_3 to P10_5, P10_15, P11_0)			30	mA
			Per side (Total of JP0_0 to JP0_5, P8_2, P8_10 to P8_12)			10	mA
			Per side (Total of P0_7 to P0_10)			8	mA
			Per side (Total of P8_0, P8_1, P8_3 to P8_9)			9	mA
			Total (EVSS)			60	mA
		PgA0	Total (A0VSS)			16	mA

Note: For detail of the definition of “side” and “total”, refer to **Section 1.2.3, Port Current**.

1.10 Power Supply Currents

Item	Symbol	Condition				MIN.	TYP.	MAX.	Unit
		CPU	PLL	Ta	Peripheral				
RUN mode current	IDDR	Run (80 MHz)	Run	–40 to 125°C	All peripherals run		25	60	mA
					All peripherals stop		19		mA
HALT mode current	IDDH	Run (80 MHz)	Run	–40 to 125°C	All peripherals run		20	56	mA
STOP mode current	IDDS	Stop	Stop	–40 to 85°C	All peripherals stop		0.35	3.5	mA
				105°C	All peripherals stop			8	mA
				125°C	All peripherals stop			12	mA
Deep STOP mode current	IDDDS	Power off	Power off	–40 to 85°C	AWO: All peripherals stop ISO: Power off		35	350	µA
				105°C	AWO: All peripherals stop ISO: Power off			700	µA
				125°C	AWO: All peripherals stop ISO: Power off			1000	µA
Cyclic RUN mode current	IDDCR	Run (HS IntOsc)	Stop	–40 to 85°C	(*a)		1.6	11	mA
				105°C	(*a)			17	mA
				125°C	(*a)			24	mA
Cyclic STOP mode current	IDDCS	Stop	Stop	–40 to 85°C	(*b)		0.40	6	mA
				105°C	(*b)			9	mA
				125°C	(*b)			13	mA

NOTES

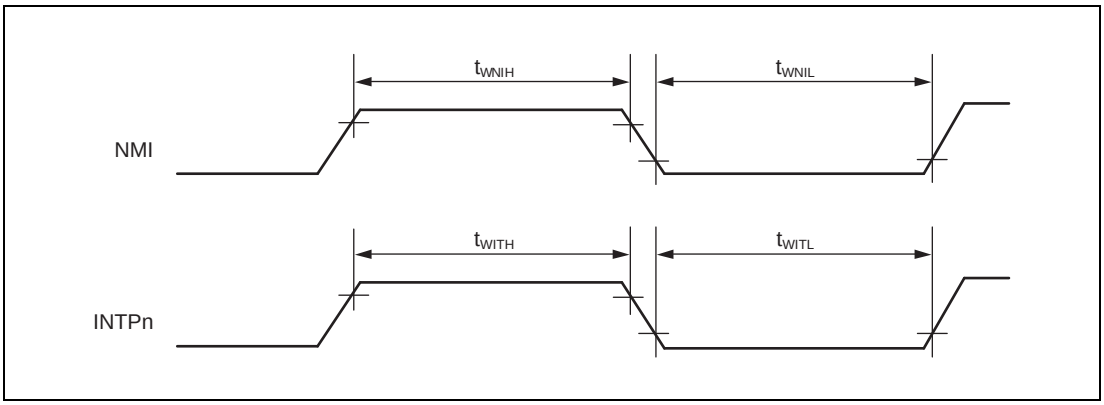
1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only.
   - Ta = 25°C
   - REGVCC = EVCC = A0VREF = 5.0 V
   - AWOVSS = EVSS = A0VSS = 0 V
2. REGVCC, EVCC and A0VREF total current. But the I/O buffer is stopped.

(*a) (*b) Operating condition of each function is shown in following table.

Function		Condition (*a)	Condition (*b)
AWO			
	MainOsc	Stop	Stop
	HS IntOsc	Run	Stop
	TAUJ0	Run (LS IntOsc)	Run (LS IntOsc)
	CLMA0	Run	Stop
	CLMA1	Stop	Stop
	ADCn	Stop	Stop
	LPS	Stop	Stop
	FOUT	Stop	Stop
	RRAM	Run (Fetch)	Stop
ISO			
	CPU	Run (HS IntOsc)	Stop
	except CPU	Stop	Stop

1.11 Interrupt Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high/low level width	t_{WNIH}/ t_{WNIL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by High Speed Internal Oscillator)	756			ns
		Level detection mode (EMCLK is operated by Low Speed Internal Oscillator)	5.13			µs
INTPn input high/low level width	t_{WITH}/ t_{WITL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by High Speed Internal Oscillator)	756			ns
		Level detection mode (EMCLK is operated by Low Speed Internal Oscillator)	5.13			µs



1.12 Power Up/Down Timing

Table 1.1 In case the $\overline{\text{RESET}}$ pin is used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REGVCC ↑ and IOVDD ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}		2			ms
FLMD0, 1 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMDR}		1			ms
FLMD0, 1 hold time (vs $\overline{\text{RESET}}$ ↑)	t_{HMDR}		1			ms
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVDD ↓ delay time	t_{DRPD}		0			ms

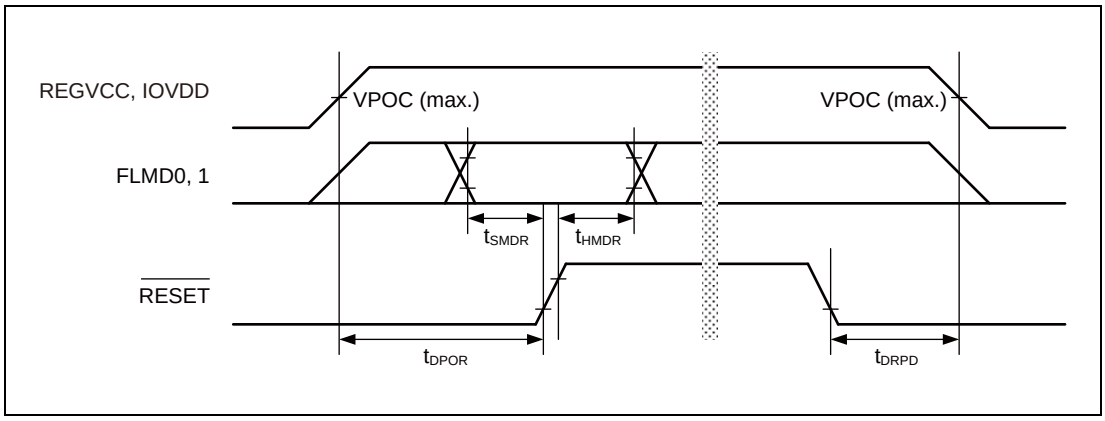
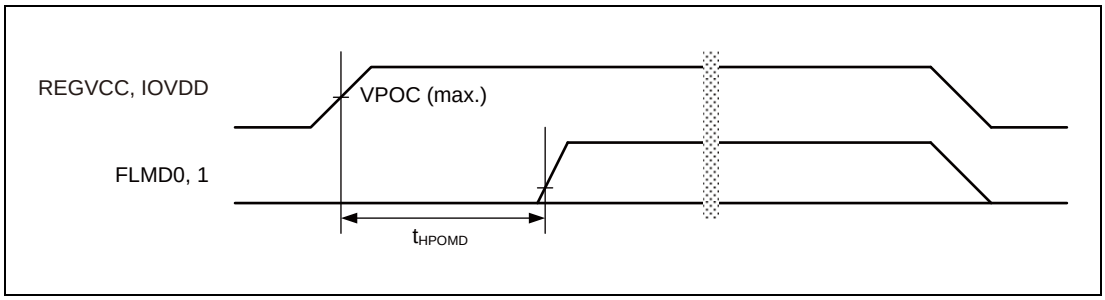


Table 1.2 In case the $\overline{\text{RESET}}$ pin is not used*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REGVCC ↑ and IOVDD ↑ to FLMD0, 1 hold time	t_{HPOMD}		2			ms

Note 1. The $\overline{\text{RESET}}$ pin is always pulled up (high fixed).



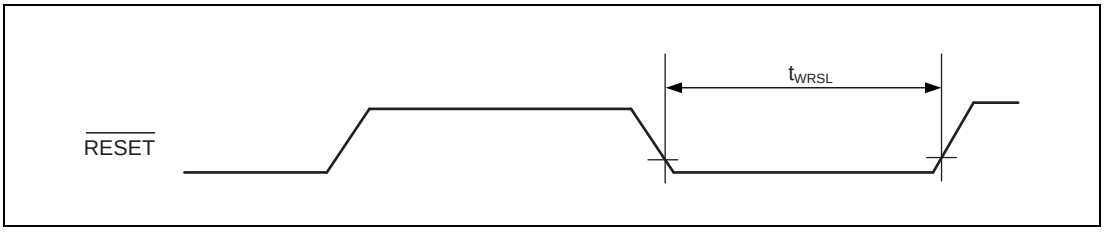
NOTE

REGVCC = IOVDD (IOVDD: EVCC = A0VREF)

This condition is available in Normal operation mode only.

1.13 $\overline{\text{RESET}}$ Timing

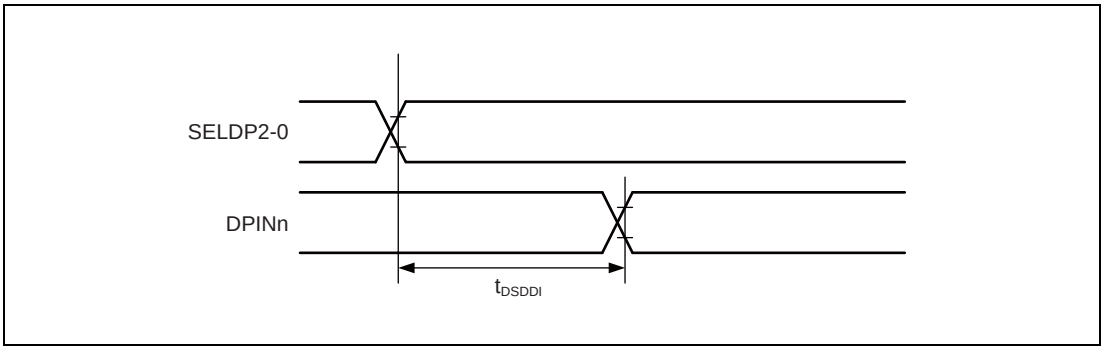
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width	t_{WRSL}	Except power on	600			ns



1.14 Port polling timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DPINn input delay time (vs SELDP2-0)	t_{DSDDI}				150	ns

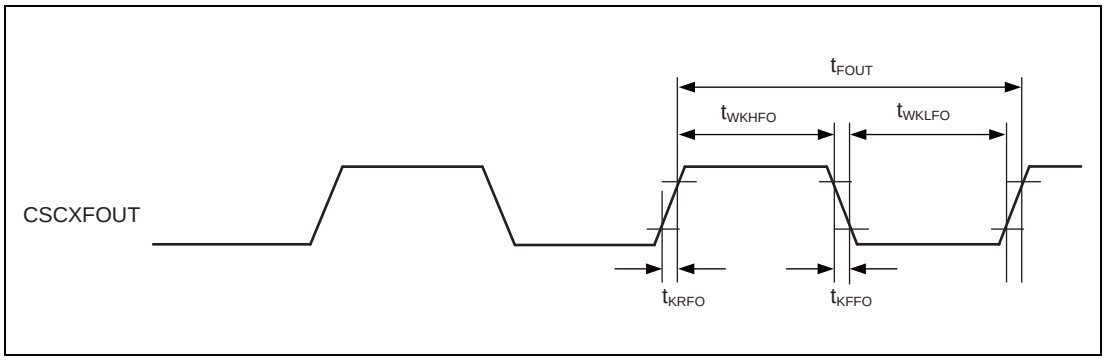
Note: n = 7 to 0



1.15 CSCXFOUT Timing

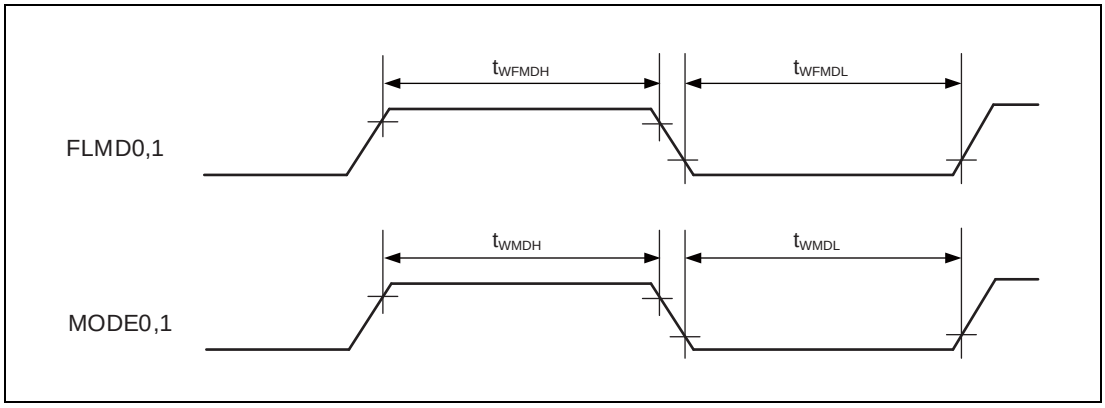
Condition: These specs are the fast mode case.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CSCXFOUT output cycle	t_{FOUT}	JP0_3 pin	100 (max. 10 MHz)			ns
		Except JP0_3 pin (Fast mode)	41.6 (max. 24 MHz)			ns
CSCXFOUT high/ low level width	t_{WKHFO}/ t_{WKLFO}	JP0_3 pin	t_{FOUT}/2 – 37			ns
		Except JP0_3 pin (Fast mode)	t_{FOUT}/2 – 10			ns
CSCXFOUT rise/ fall time	t_{KRFO}/ t_{KFFO}	JP0_3 pin			37	ns
		Except JP0_3 pin (Fast mode)			10	ns



1.16 Mode Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0,1 input high/low level width	t_{WFMDH}/ t_{WFMDL}		600			ns
MODE0, 1 input high/low level width	t_{WMDH}/ t_{WMDL}		600			ns



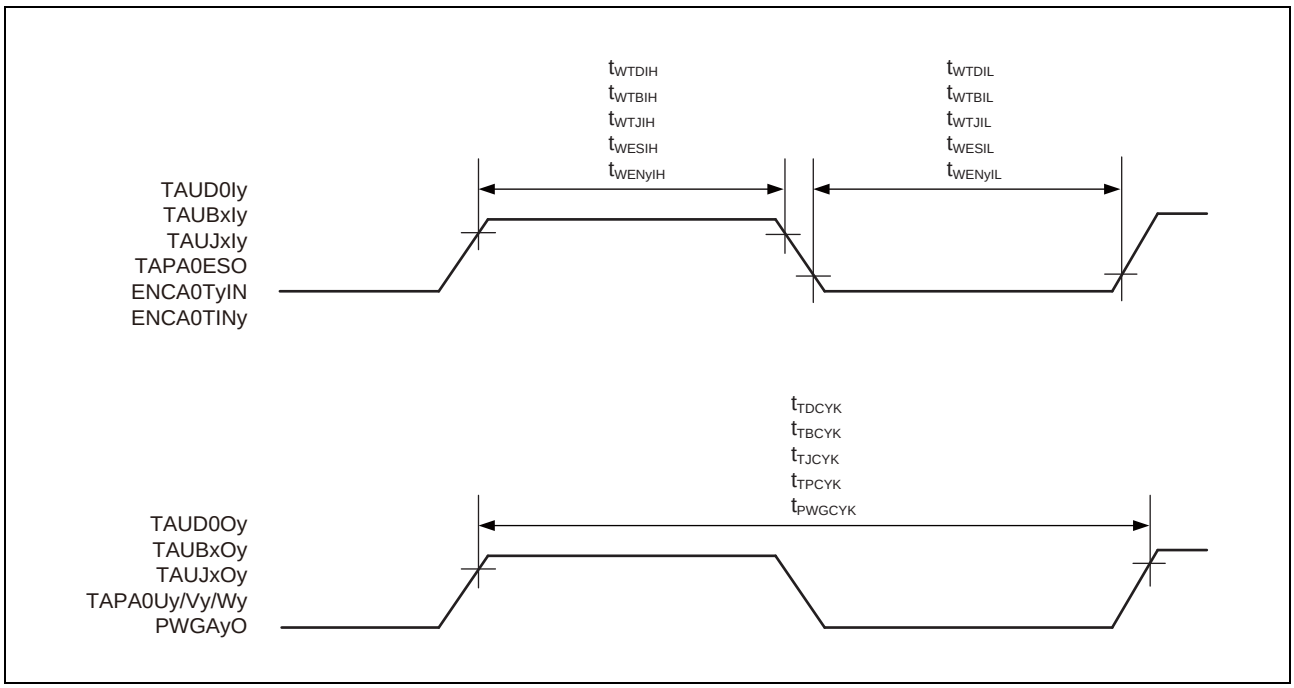
1.17 Timer Timing

Condition: Specs of TAPA0Uy/Vy/Wy (y = P, N) are the fast mode case.

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUD0Iy input high/low level width (y = 0 to 15)	t_{WTDIH}/ t_{WTDIL}		n × Tsamp + 20[*1, *2]			ns
TAUD0Oy output cycle (y = 0 to 15)	t_{TDCYK}	Slow mode			10	MHz
TAUBxIy input high/low level width (x = 0, y = 0 to 15)	t_{WTBIH}/ t_{WTBIL}		n × Tsamp + 20[*1, *2]			ns
TAUBxOy output cycle (x = 0, y = 0 to 15)	t_{TBCYK}	Slow mode			10	MHz
TAUJxIy input high/low level width (x = 0, 1, y = 0 to 3)	t_{WTJIH}/ t_{WTJIL}		600			ns
TAUJxOy output cycle (x = 0, 1, y = 0 to 3)	t_{TJCYK}	Slow mode			10	MHz
TAPA0ESO input high/low level width	t_{WESIH}/ t_{WESIL}		600			ns
TAPA0Uy/Vy/Wy output cycle (y = P, N)	t_{TPCYK}	Slow mode			10	MHz
ENCA0TINy input high/low level width (y = 0, 1)	t_{WENTIH}/ t_{WENTIL}		n × Tsamp + 20[*1]			ns
ENCA0yIN input high/low level width (y = A, B, Z)	t_{WENyIH}/ t_{WENyIL}		n × Tsamp + 20[*1]			ns
PWGAyO output cycle (y = 0 to 47)	t_{PWGCYK}	Slow mode			10	MHz

Note 1. n: Sampling number of the digital noise filter for each input.
Tsamp: Sampling time of the digital noise filter for each input.

Note 2. Input more than 1 count clock width of each timer counter channel.

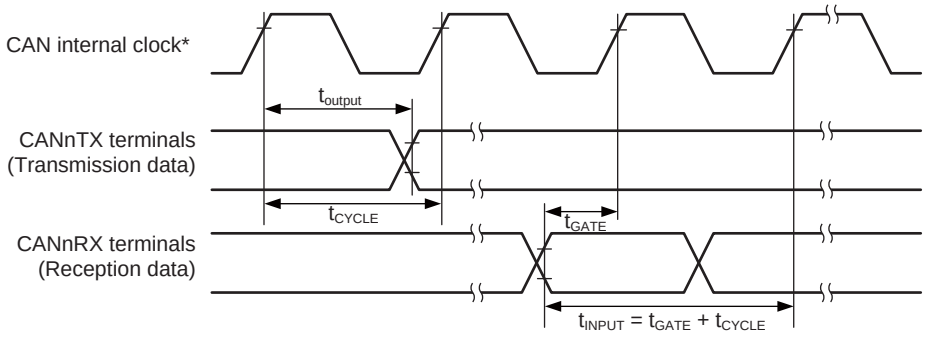


1.18 RLIN2/RLIN3 Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate		LIN function	1		115.2	kbps
		UART function			1.5	Mbps
RLIN2 transfer rate			1		20	kbps

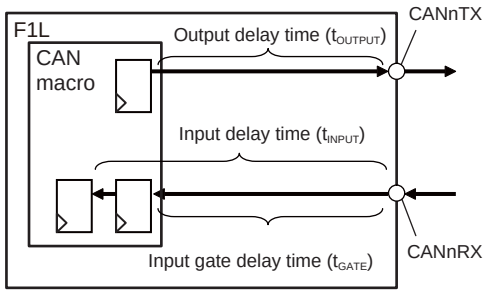
1.19 RS-CAN Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					1	Mbps
CAN node delay time	t_{NODE}	t_{CYCLE} = 62.5 ns			100	ns
Internal delay time (Input/output)		Input + Output (t_{INPUT} + t_{OUTPUT})			50.0	ns



CAN Node delay time (t_{NODE}) = Input delay time (t_{INPUT}) + Output delay time (t_{OUTPUT})

Internal delay time ($t_{INTDEL1}$, $t_{INTDEL2}$) = Internal gate delay Time (t_{GATE}) + Output delay time (t_{OUTPUT})



NOTE

Internal clock of CAN is the clock selected by CKSC register.

1.20 CSI Timing

1.20.1 CSIG Timing

Condition: CSIGnSO and CSIGnSC (output) pin are the fast mode.

Table 1.3 CSIG Timing (Master Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYMGn}		100			ns
CSIGnSC high level width	t_{KWHMGn}		$0.5 \times t_{KCYMGn} - 10$			ns
CSIGnSC low level width	t_{KWLMGn}		$0.5 \times t_{KCYMGn} - 10$			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSIMGn}		30			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSIMGn}		0			ns
CSIGnSO output delay (vs. CSIGnSC)	t_{DSOMGn}				7	ns
CSIGnRYI setup time (vs. CSIGnSC)	t_{SRYIGn}	CSIGnCTL1.CSIGnSIT = x CSIGnCTL1.CSIGnHSE = 1	$2 \times t_{KCYGn} + 25$			ns
CSIGnRYI High level width	t_{WRYIGn}	CSIGnCTL1.CSIGnHSE = 1	$t_{KCYGn} + 5$			ns

Table 1.4 CSIG Timing (Slave Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro operation clock cycle time	t_{KCYGn}		12.5 (max. 80 MHz)			ns
CSIGnSC cycle time	t_{KCYSGn}		200			ns
CSIGnSC high level width	t_{KWHSGn}		$0.5 \times t_{KCYSGn} - 10$			ns
CSIGnSC low level width	t_{KWLSGn}		$0.5 \times t_{KCYSGn} - 10$			ns
CSIGnSI setup time (vs. CSIGnSC)	t_{SSISGn}		20			ns
CSIGnSI hold time (vs. CSIGnSC)	t_{HSISGn}		$t_{KCYGn} + 5$			ns
SO output delay (vs. CSIGnSC)	t_{DSOSGn}				30	ns
CSIGnRYO output delay	t_{SRYOGn}				38	ns
$\overline{\text{CSIGnSSI}}$ setup time (vs.CSIGnSC)	$t_{SSSISGn}$		$0.5 \times t_{KCYSGn} - 5$			ns
$\overline{\text{CSIGnSSI}}$ hold time (vs. CSIGnSC)	$t_{HSSISGn}$		$t_{KCYGn} + 5$			ns

1.20.2 CSIH Timing

Condition:

- REGVCC = EVCC = 3.0 V to 5.5 V
- CSIHnSO and CSIHnSC (output) pin are the fast mode, and CL = 100 pF (n = 0)/50 pF (n = 1 to 3).

Table 1.5 CSIH Timing (Master Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYMHn}		100			ns
CSIHnSC high level width	t_{KWHMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSC low level width	t_{KWLMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSIMHn}	SI Positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	19			ns
		SI Negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	14			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSIMHn}	SI Positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	0			ns
		SI Negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	t_{KCYHn}/2			ns
CSIHnSO output delay (vs. CSIHnSC)	t_{DSOMHn}				7	ns
CSIHnRYI setup time (vs. CSIHnSC)	t_{SRYIHn}	CSIHnCTL1.CSIHnSIT = x CSIHnCTL1.CSIHnHSE = 1	2 × t_{KCYHn} + 25			ns
CSIHnRYI high level width	t_{WRYIHn}	CSIHnCTL1.CSIHnHSE = 1	t_{KCYHn} + 5			ns
CSIHnCSS0-7 inactive width	$t_{WSCSBHn}$		CSIDLE × t_{KCYMHn} – 11			ns
CSIHnCSS0-7 setup time (vs. CSIHnSC)	$t_{SSCSBHn0}$	CSIHnCTL1.CSIHnDAP = 0	CSSETUP × t_{KCYMHn} – 23			ns
	$t_{SSCSBHn1}$	CSIHnCTL1.CSIHnDAP = 1	(CSSETUP + 0.5) × t_{KCYMHn} – 23			ns
CSIHnCSS0-7 hold time (vs. CSIHnSC)	$t_{HSCSBHn0}$	CSIHnCTL1.CSIHnSIT = 0	CSSHOLD × t_{KCYMHn} – 5			ns
	$t_{HSCSBHn1}$	CSIHnCTL1.CSIHnSIT = 1	(CSSHOLD + 0.5) × t_{KCYMHn} – 5			ns

NOTE

CSIDLE: Setting value of CSIHnCFGx.CSIHnIDx[2:0]

CSSETUP: Setting value of CSIHnCFGx.CSIHnSPx[3:0]

CSSHOLD: Setting value of CSIHnCFGx.CSIHnHDx[3:0]

However, when n = 0, x = 0 to 7; when n = 1, x = 0 to 5; and when n = 2, 3, x = 0 to 3.

CAUTION

When the serial clock level is changed during the communication (CSIHnCFGx.CSIHnCKPx) and the IDLE has a setting of 0.5 transmission clock clock period an inactive width time t_{WSCSB} of "0.5 × t_{KCYMHn}" is added.

However, when n = 0, x = 0 to 7; when n = 1, x = 0 to 5; and when n = 2, 3, x = 0 to 3.

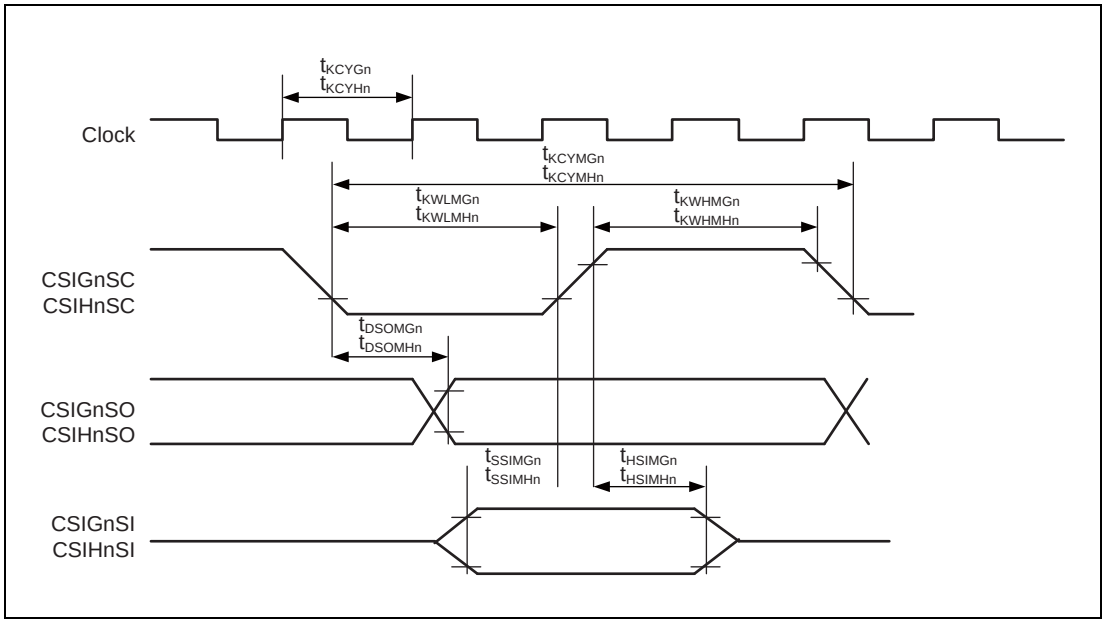
Table 1.6 CSIH Timing (Slave Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYSHn}		200			ns
CSIHnSC high level width	t_{KWHSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSC low level width	t_{KWLSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSI setup time (vs. CSIHnSC)	t_{SSISHn}		20			ns
CSIHnSI hold time (vs. CSIHnSC)	t_{HSISHn}		$t_{KCYHn} + 5$			ns
SO output delay (vs. CSIHnSC)	t_{DSOSHn}				30	ns
CSIHnRYO output delay	t_{SRYOHn}				38	ns
$\overline{\text{CSIHnSSI}}$ setup time (vs. CSIHnSC)	$t_{SSSISHn}$		$0.5 \times t_{KCYSHn} - 5$			ns
$\overline{\text{CSIHnSSI}}$ hold time (vs. CSIHnSC)	$t_{HSSISHn}$		$t_{KCYHn} + 5$			ns

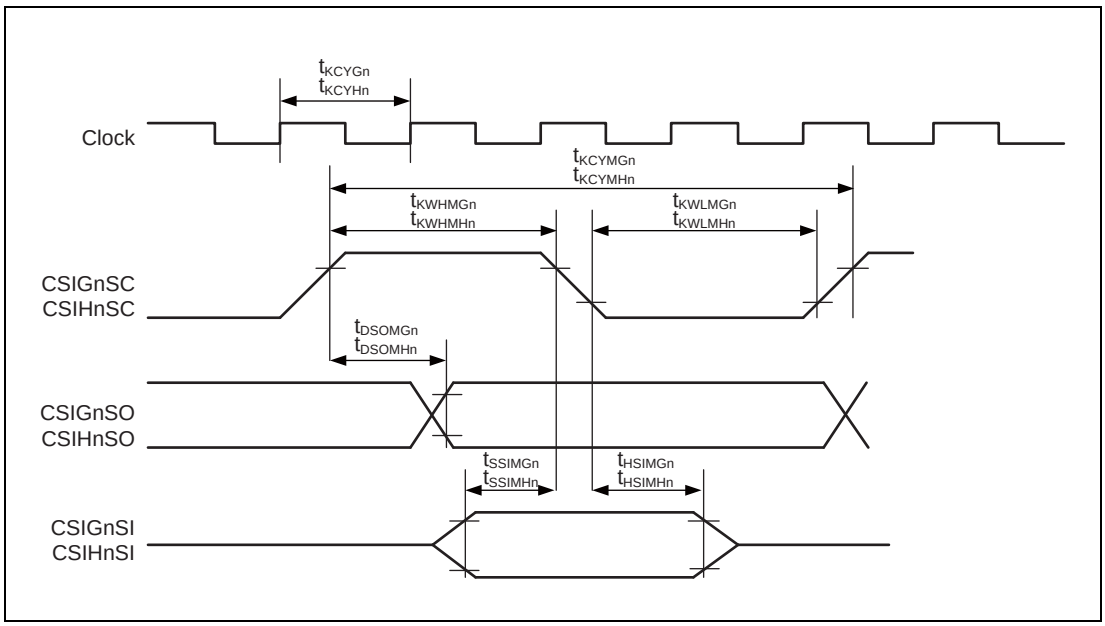
(1) SCKO/SI/SO

Master Mode:

- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)



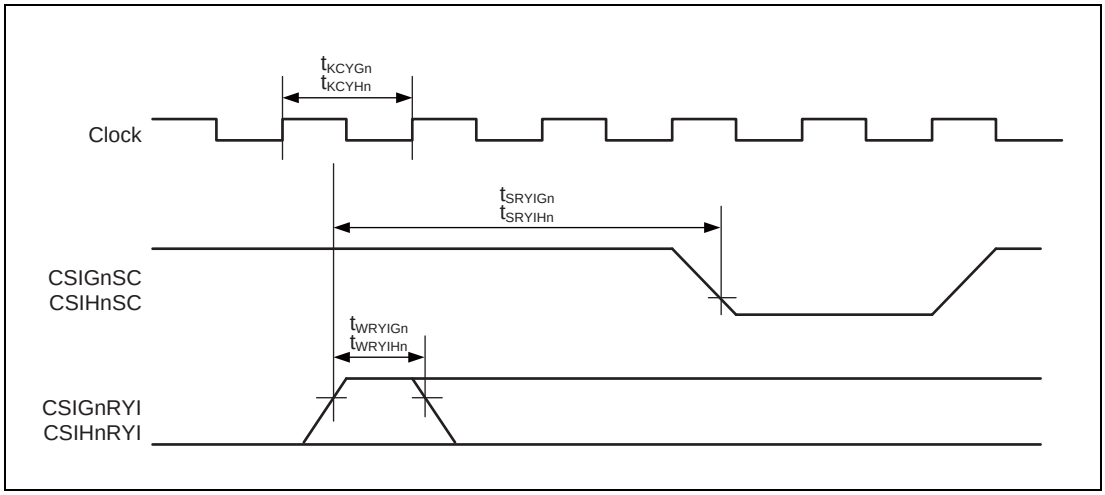
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)



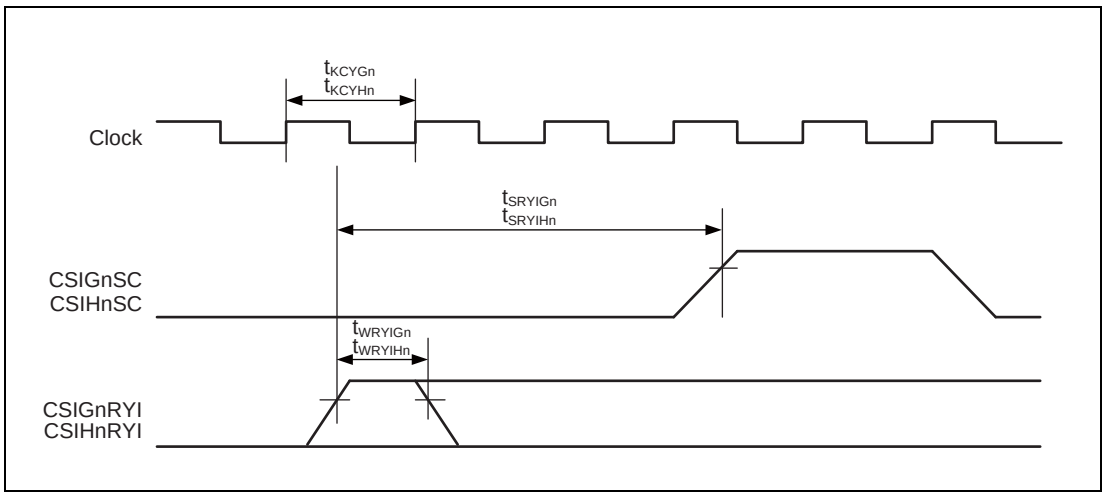
(2) RYI

- CSIG: Only master mode (CSIGnCTL1: CSIGnHSE = 1, CSIGnCTL1: CSIGnSIT = 0)
- CSIH: Only master mode (CSIHnCTL1: CSIHnHSE = 1, CSIHnCTL1: CSIHnSIT = 0)

– CSIG (CSIGnCTL1: CSIGnCKR = 0)
– CSIH (CSIHnCFGm: CSIHnCKPm = 0)



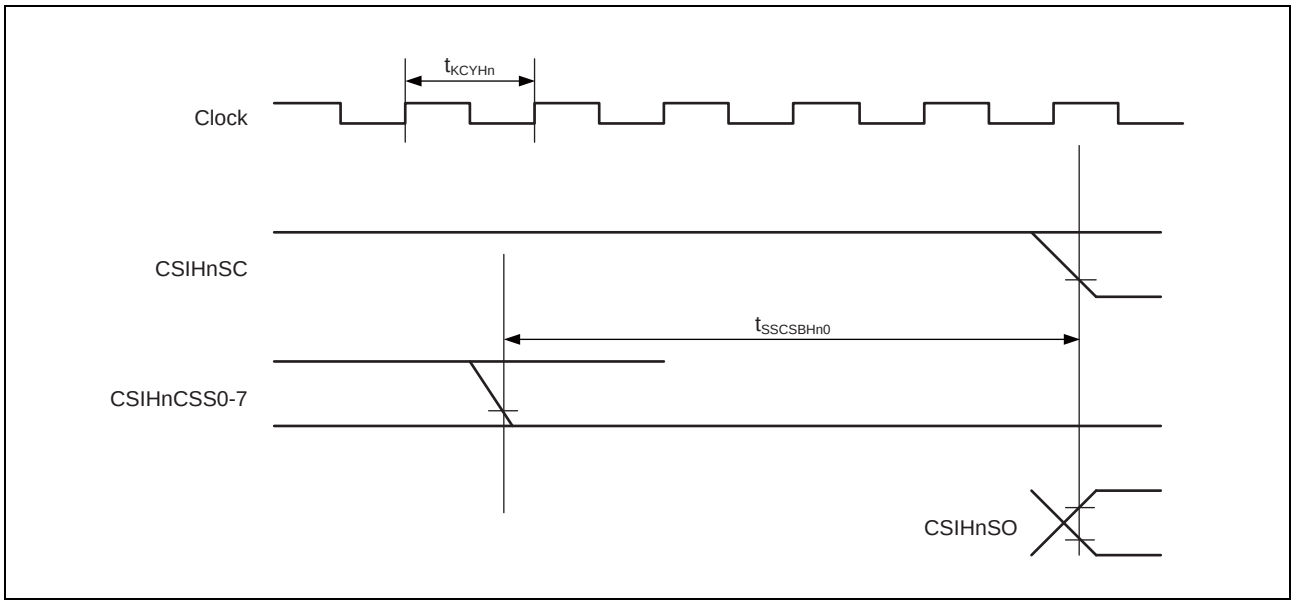
– CSIG (CSIGnCTL1: CSIGnCKR = 1)
– CSIH (CSIHnCFGm: CSIHnCKPm = 1)



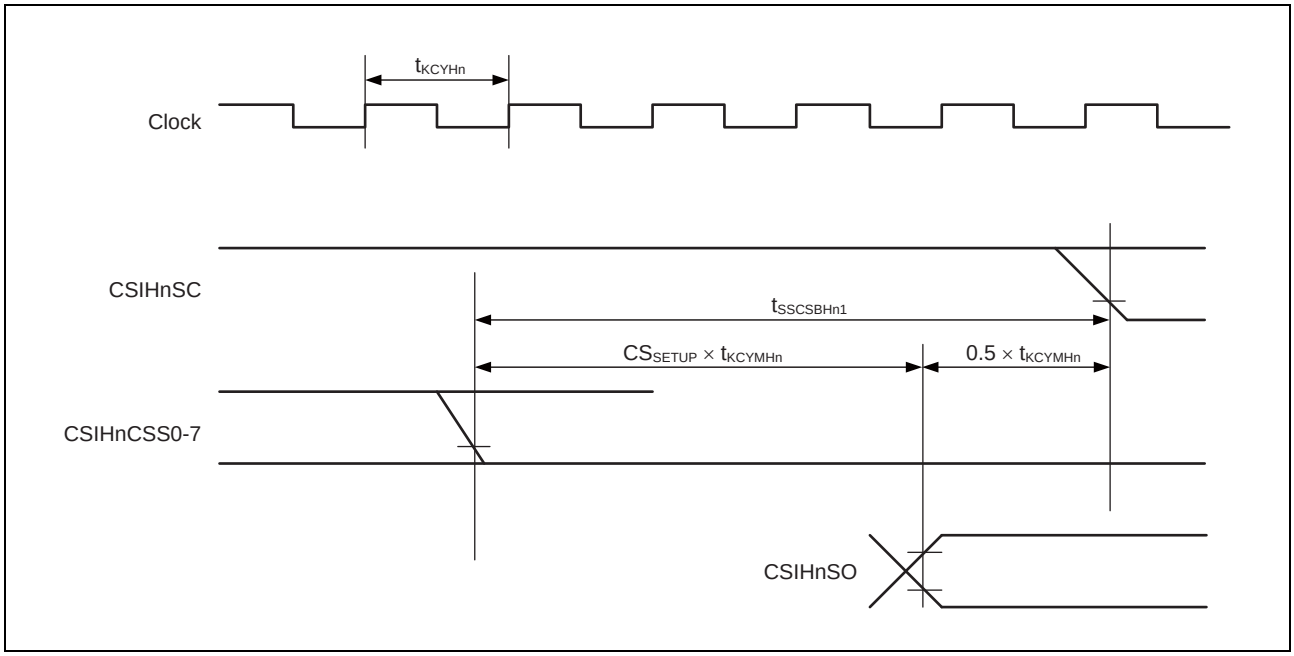
(3) CSSn

Only Master Mode (Setup Time):

- CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0

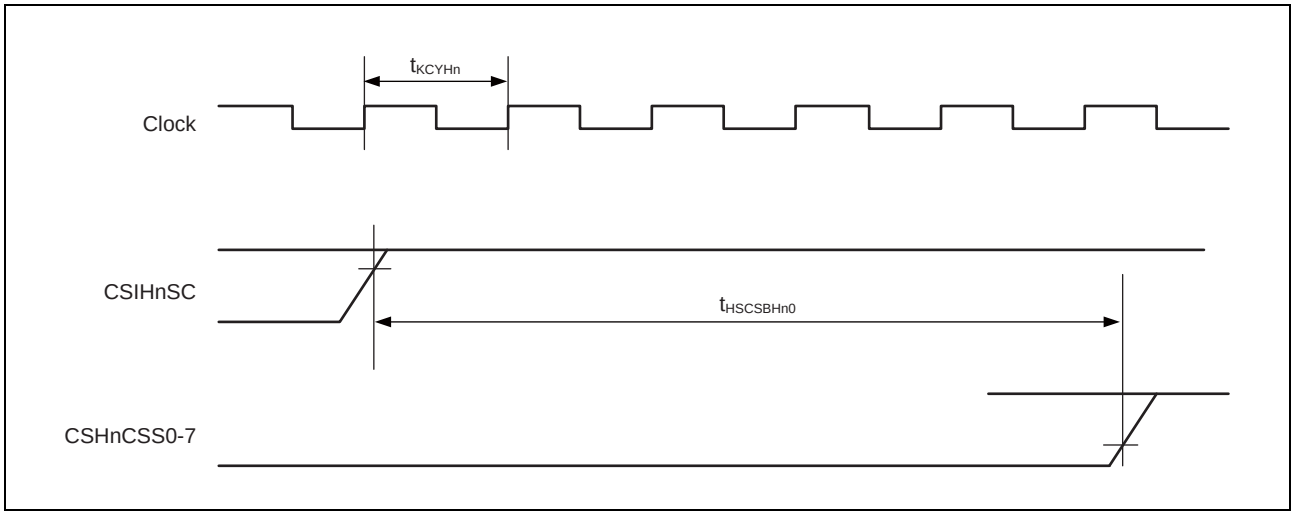


- CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 1

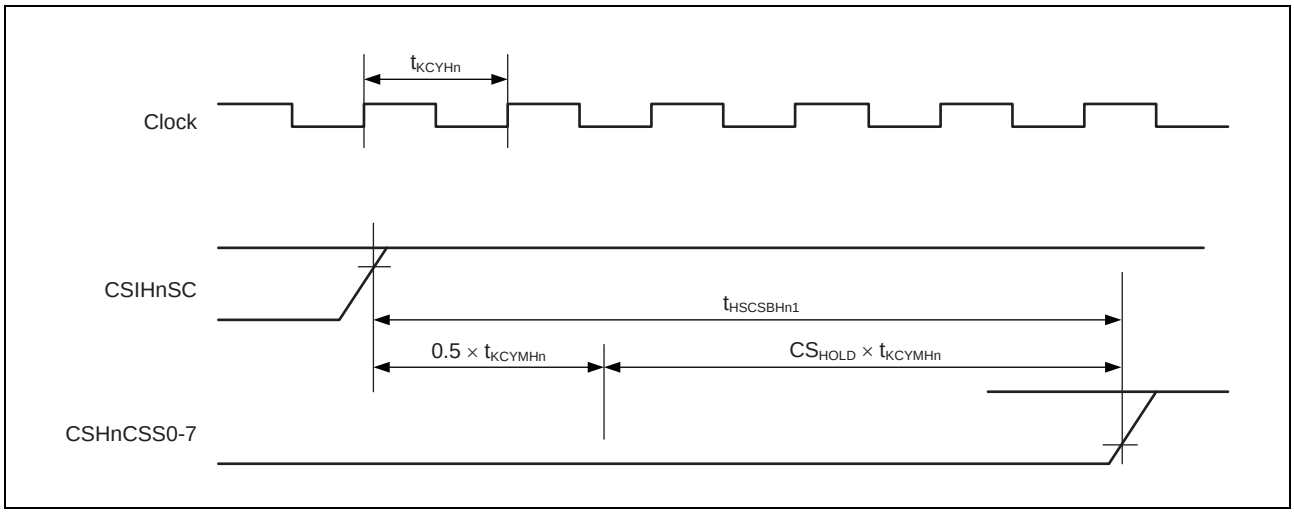


Only Master Mode (Hold Time):

- CSIHnCTL1: CSIHnSIT = 0, CSIHnCFGm: CSIHnCKPm = 0,
  CSIHnCFGm: CSIHnDAPm = 0



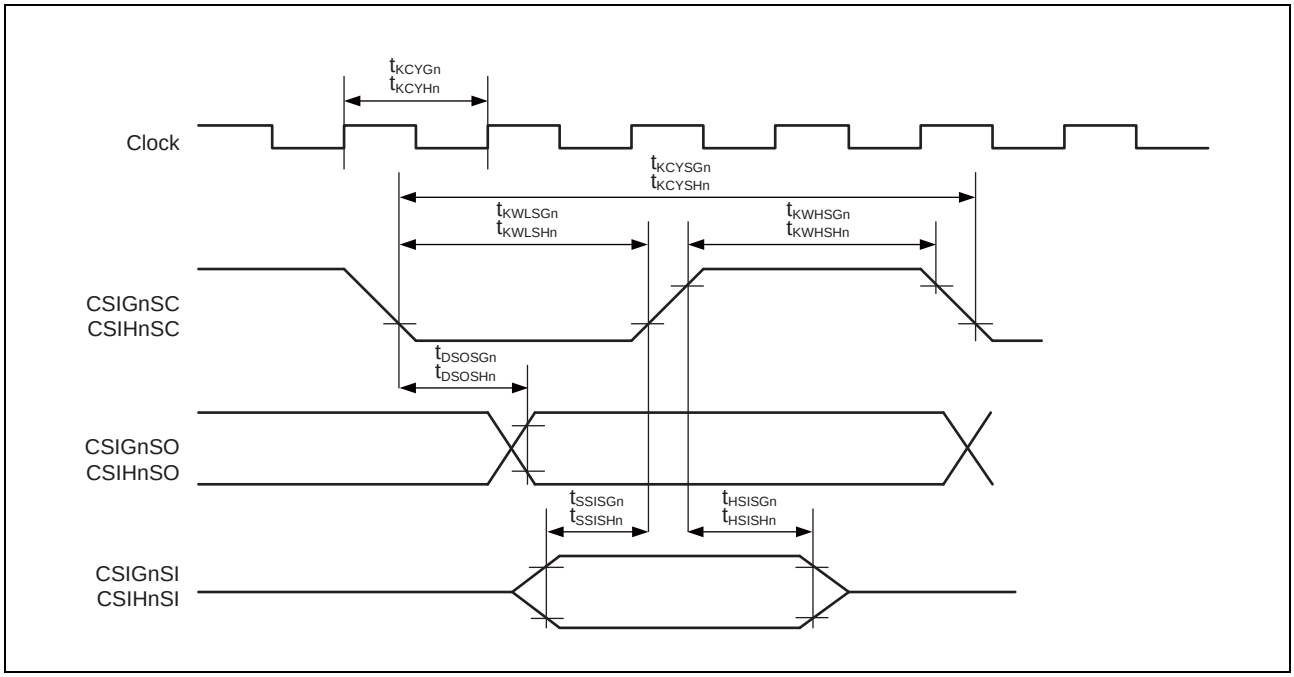
- CSIHnCTL1: CSIHnSIT = 1, CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0



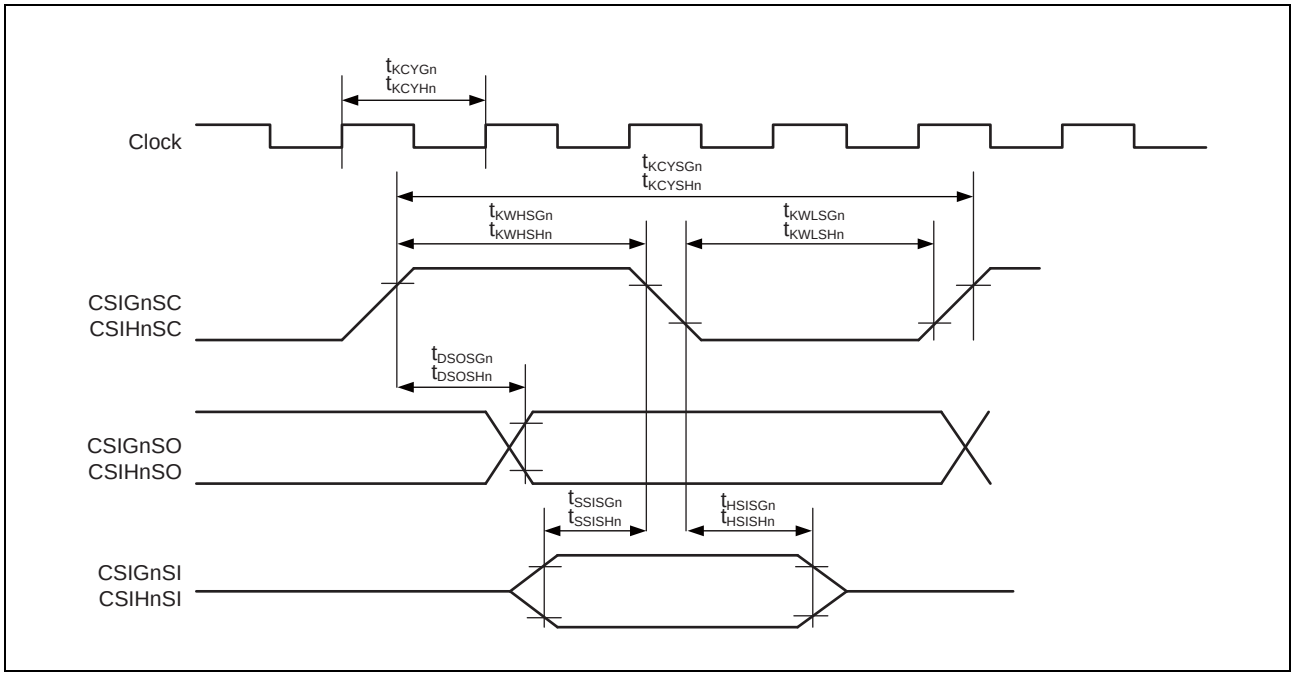
(4) SCKO/SI/SO

Slave Mode:

- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)

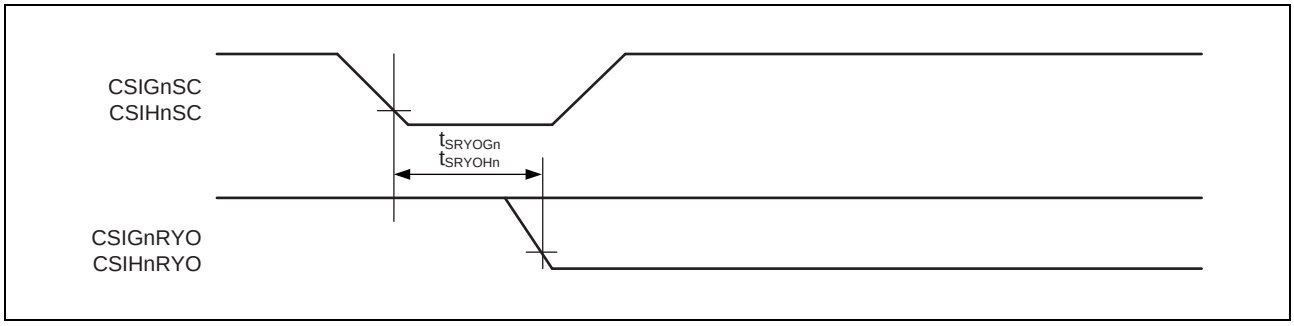


- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)

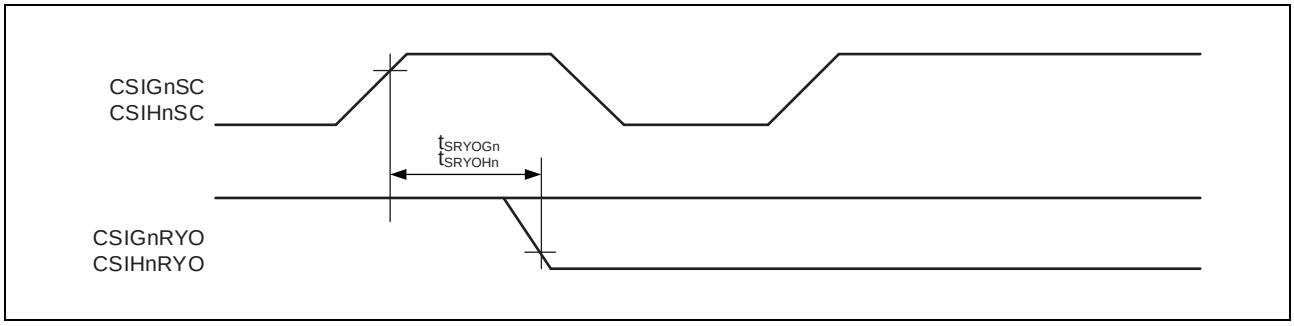


(5) RYO

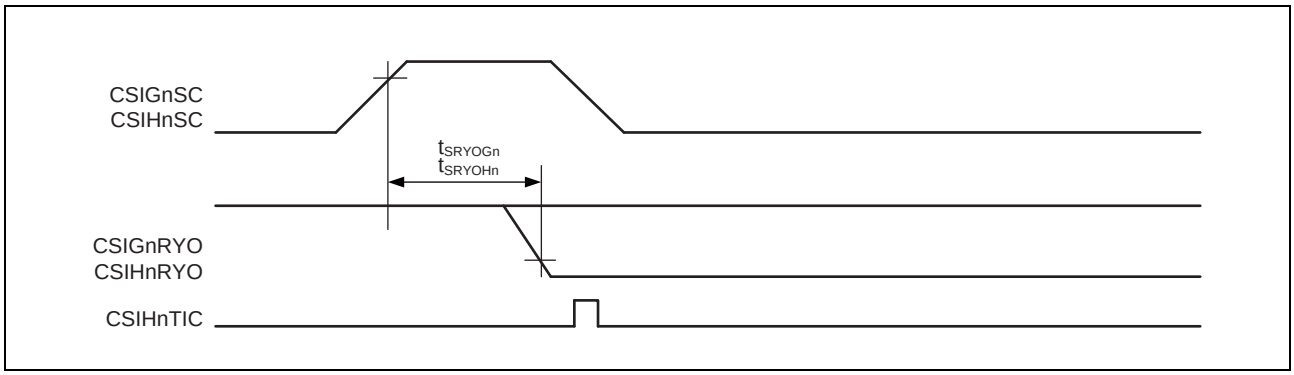
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 0/0)



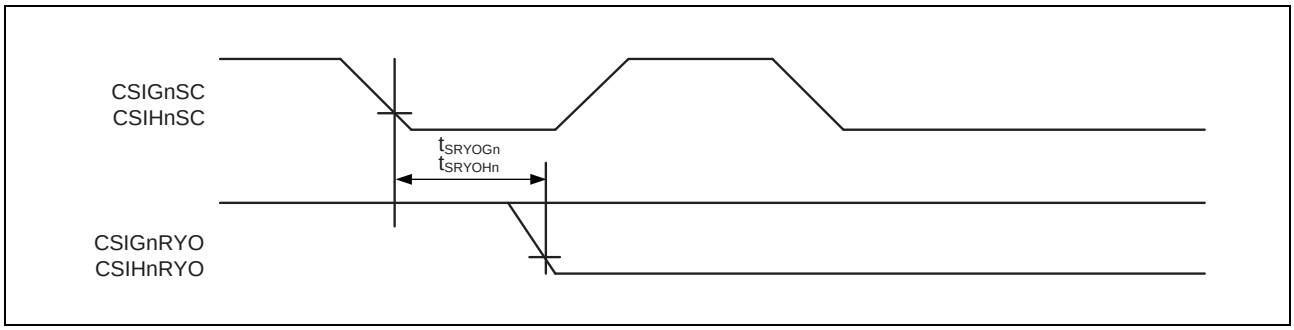
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 0/1)



- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 1/0)



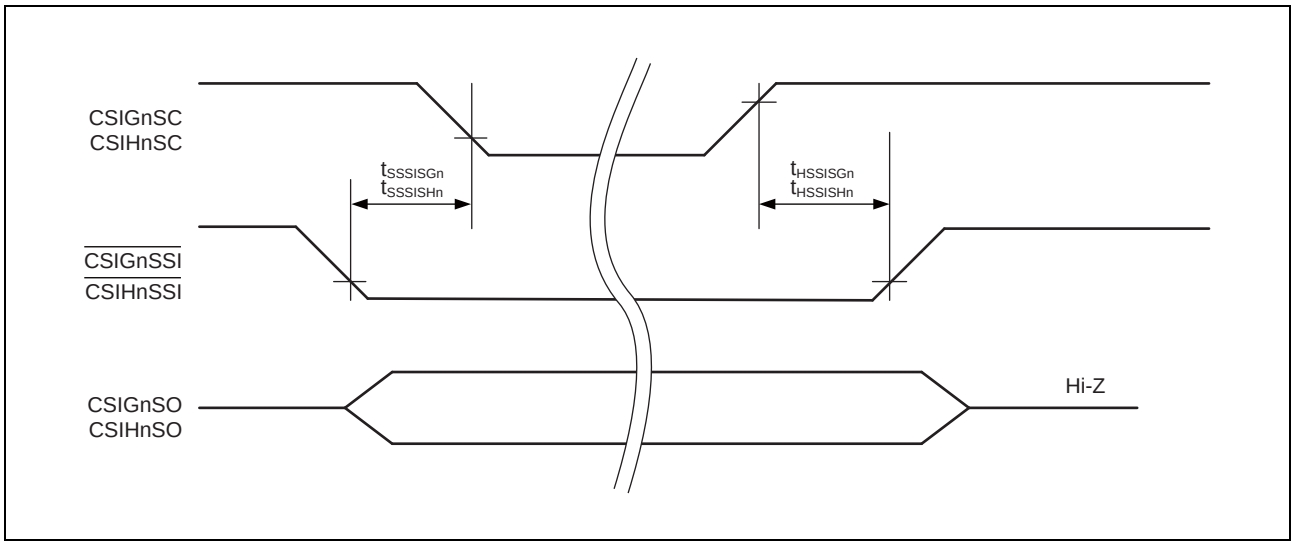
- CSIG (CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 1/1)



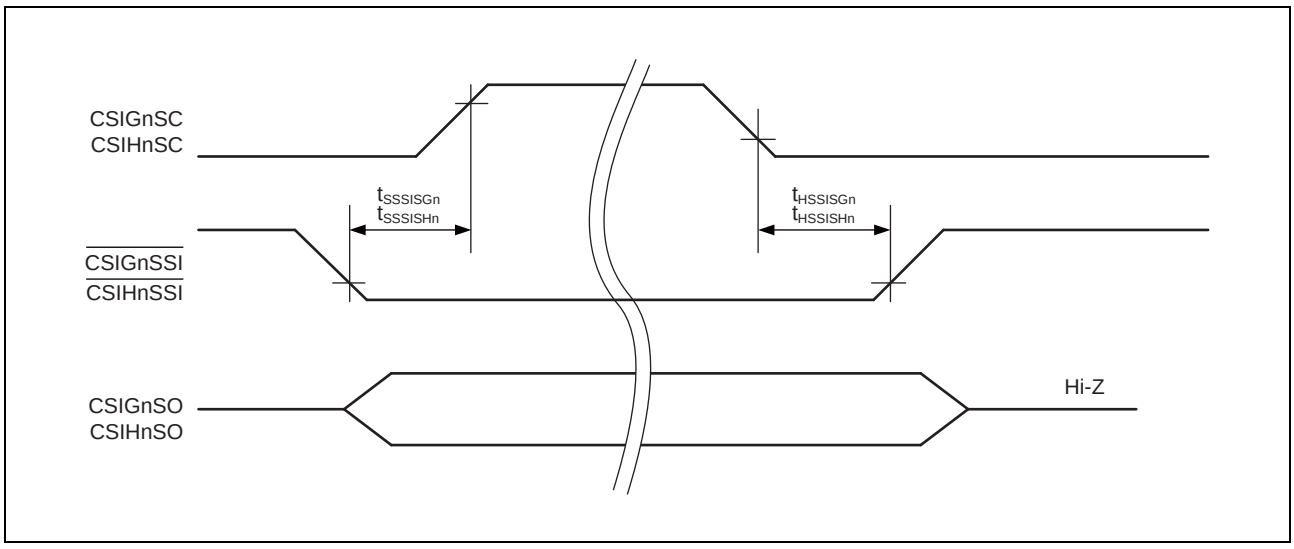
(6) SSI

Slave Mode:

- CSIG (CSIGnCTL1: CSIGnSSE=1, CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 0/0 or 1/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)



- CSIG (CSIGnCTL1: CSIGnSSE=1, CSIGnCTL1: CSIGnCKR/CSIGnCFG0: CSIGnDAP0 = 1/0 or 0/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGm: CSIHnCKPm/CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)



1.21 RIIC Timing

Table 1.7 RIIC Timing (Normal Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SCL clock period	f_{CLK}		0		100	kHz
Bus free time (between stop/start condition)	t_{BUF}		4.7			µs
Hold time*1	t_{HD}: STA		4.0			µs
SCL clock low-level width	t_{LOW}		4.7			µs
SCL clock high-level time	t_{HIGH}		4.0			µs
Setup time for start/restart condition	t_{SU}: STA		4.7			µs
Data hold time	t_{HD}: DAT	CBUS compatible master	5.0			µs
		IIC mode	0*2			µs
Data setup time	t_{SU}: DAT		250			ns
SDA and SCL signal rise time	t_R				1000	ns
SDA and SCL signal fall time	t_F				300	ns
Stop condition setup time	t_{SU}: STO		4.0			µs
Capacitance load of each bus line	Cb				400	pF

Note: SCL: RIIC0SCL pin
SDA: RIIC0SDA pin

Note 1. At the start condition, the first clock pulse Is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIIC0SDA signal (at VIH min. of RIIC0SCL signal). In order to occupy the undefined area at the falling edge of RIIC0SCL.

Note 3. If the system does not extend the RIIC0SCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Note 4. The fast mode IIC bus can be used in normal mode IIC bus system. In this case, set the fast mode IIC bus so that it meets the following conditions.
- If the system does not extend the RIIC0SCL signal's low state hold time: t_{SU}: DAT ≥ 250 ns
- If the system extends the RIIC0SCL signal's low state hold time:
Transmit the following data bit to the RIIC0SDA line prior to releasing the RIIC0SCL line ($t_{Rmax.}$ + t_{SU}: DAT = 1000 + 250 = 1250 ns: Normal mode IIC bus specification).

Note 5. Cb: Total capacitance of one bus line (unit: pF)

Table 1.8 RIIC Timing (Fast Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SCL clock period	f_{CLK}		0		400	kHz
Bus free time (between stop/start condition)	t_{BUF}		1.3			µs
Hold time*1	t_{HD}: STA		0.6			µs
SCL clock low-level width	t_{LOW}		1.3			µs
SCL clock high-level time	t_{HIGH}		0.6			µs
Setup time for start/restart condition	t_{SU}: STA		0.6			µs
Data hold time	t_{HD}: DAT	IIC mode	0*2			µs
Data setup time	t_{SU}: DAT		100*4			ns
SDA and SCL signal rise time	t_R		20 + 0.1 × Cb*5		300	ns
SDA and SCL signal fall time	t_F		20 + 0.1 × Cb*5		300	ns
Stop condition setup time	t_{SU}: STO		0.6			µs
Pulse width with spike suppressed by input filter	t_{SP}		0		50	ns
Capacitance load of each bus line	Cb				400	pF

Note: SCL: RIIC0SCL pin
SDA: RIIC0SDA pin

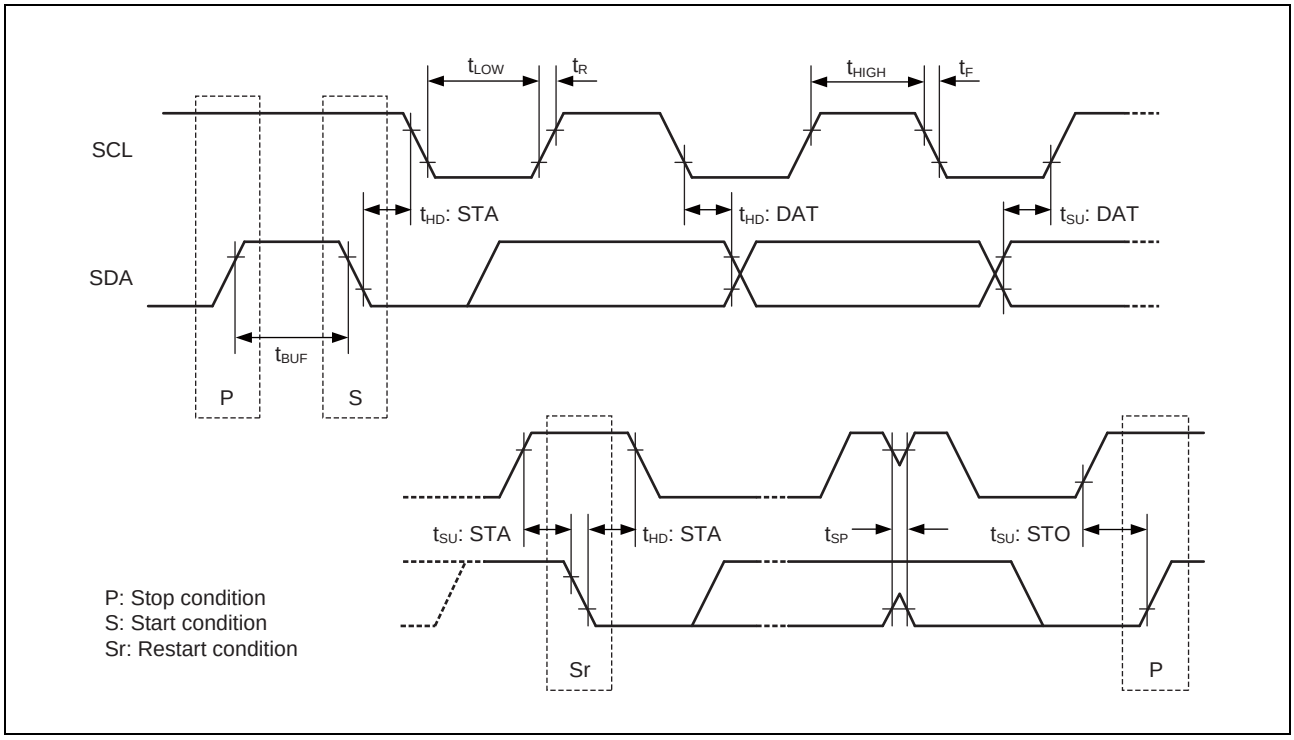
Note 1. At the start condition, the first clock pulse Is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIIC0SDA signal (at VIH min. of RIIC0SCL signal). In order to occupy the undefined area at the falling edge of RIIC0SCL.

Note 3. If the system does not extend the RIIC0SCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Note 4. The fast mode IIC bus can be used in normal mode IIC bus system. In this case, set the fast mode IIC bus so that it meets the following conditions.
- If the system does not extend the RIIC0SCL signal's low state hold time: t_{SU}: DAT ≥ 250 ns
- If the system extends the RIIC0SCL signal's low state hold time:
Transmit the following data bit to the RIIC0SDA line prior to releasing the RIIC0SCL line ($t_{Rmax.}$ + t_{SU}: DAT = 1000 + 250 = 1250 ns: Normal mode IIC bus specification).

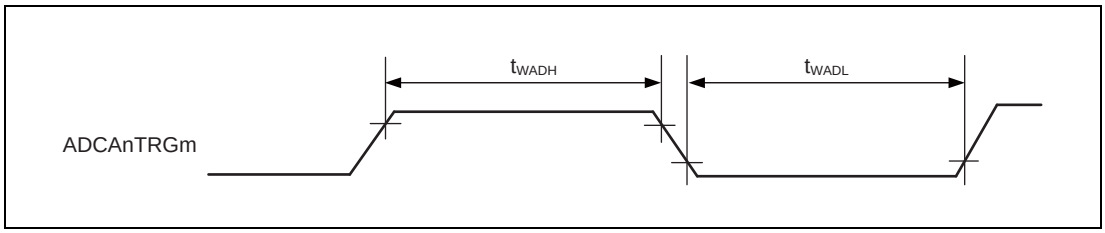
Note 5. Cb: Total capacitance of one bus line (unit: pF)


tLOW
tR
tHIGH
tF
SCL
SDA
tHD: STA
tHD: DAT
tSU: DAT
tBUF
P
S
tSU: STA
tHD: STA
tSP
tSU: STO
Sr
P
P: Stop condition
S: Start condition
Sr: Restart condition

1.22 ADTRG Timing

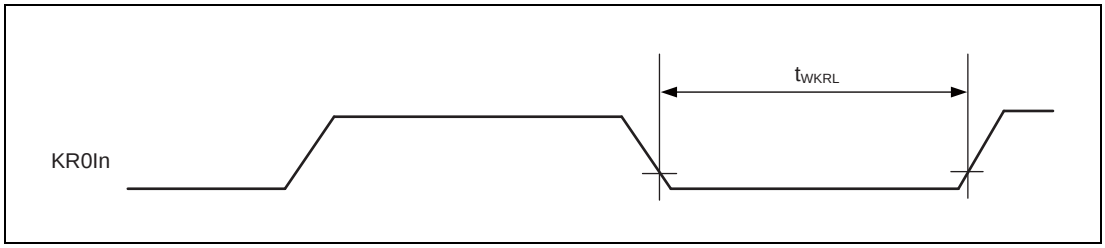
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCAnTRGm input high/ low level width	t_{WADH}/ t_{WADL}		n × Tsamp + 20*[1]			ns

Note 1. n: Sampling number of the digital noise filter for each input.
Tsamp: Sampling time of the digital noise filter for each input.



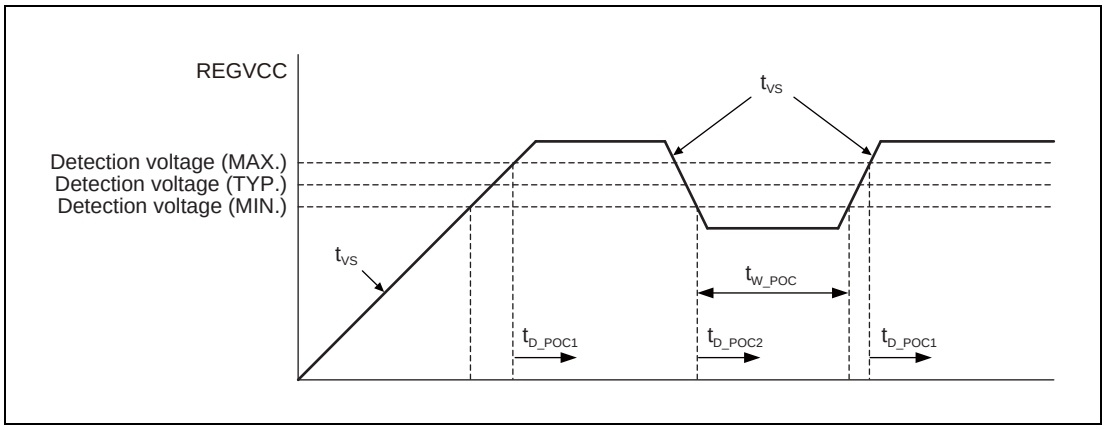
1.23 Key Return Timing

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
KR0In input low level width	t_{WKRL}		600			ns



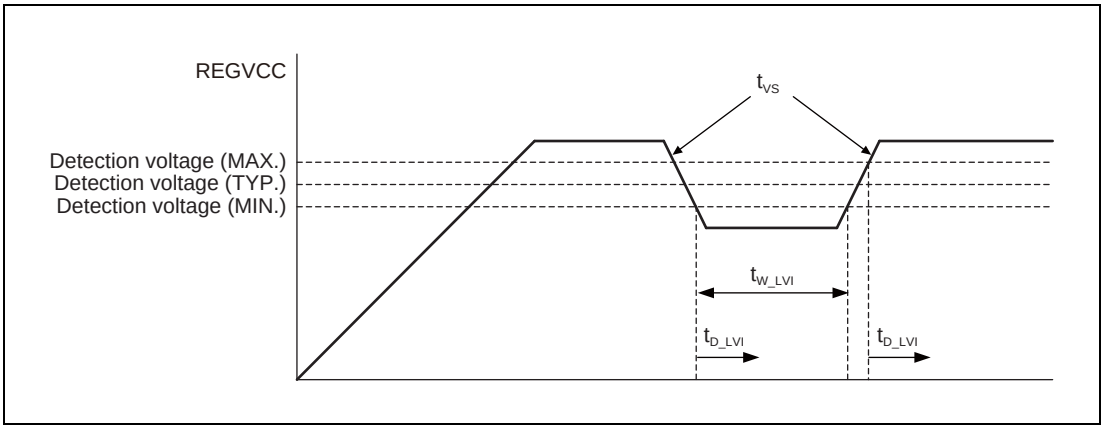
1.24 POC Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage	VPOC	At power-on	2.8	2.95	3.1	V
		After (except) power-on	2.8	2.9	3.0	V
Voltage gradient	t_{VS}		0.02		500	V/ms
Response time 1	t_{D_POC1}	t_{VS} = 0.02 V/ms to 20 V/ms			2	ms
		t_{VS} = 20 V/ms to 500 V/ms			5	ms
Response time 2	t_{D_POC2}				5	µs
REGVCC minimum width	t_{W_POC}		0.2			ms



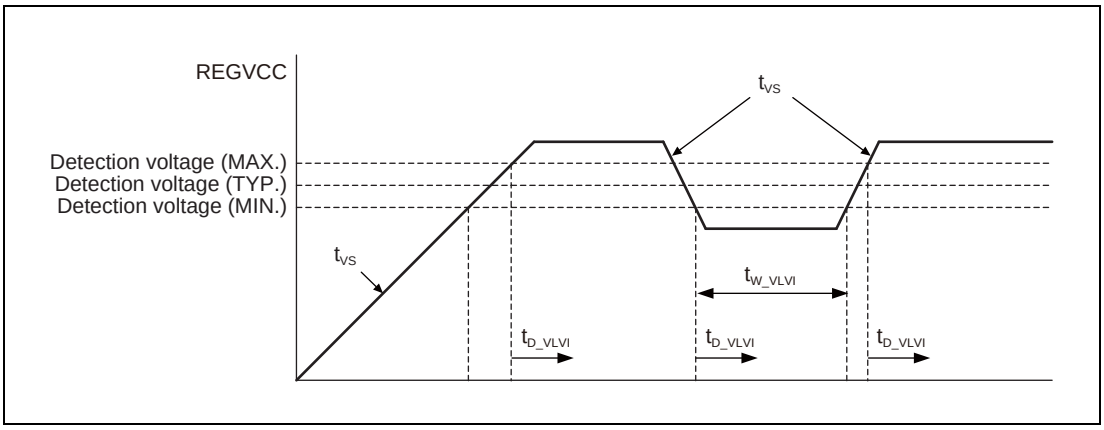
1.25 LVI Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage	VLVI0	At power-on	3.87	4.0	4.13	V
		After (except) power-on	3.9	4.0	4.1	V
	VLVI1	At power-on	3.57	3.7	3.83	V
		After (except) power-on	3.6	3.7	3.8	V
	VLVI2	At power-on	3.37	3.5	3.63	V
		After (except) power-on	3.4	3.5	3.6	V
Voltage gradient	t_{VS}		0.02		500	V/ms
Response time	t_{D_LVI}				2	ms
REGVCC minimum width	t_{W_LVI}		0.2			ms



1.26 VLVI Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Detection voltage	VVLVI		1.8	1.9	2.0	V
Voltage gradient	t_{VS}		0.02		500	V/ms
Response time	t_{D_VLVI}	t_{VS} = 0.02 V/ms to 20 V/ms			2	ms
		t_{VS} = 20 V/ms to 500 V/ms			5	ms
REGVCC minimum width	t_{W_VLVI}		0.2			ms



1.27 Flash Programming Characteristics

1.27.1 Serial Programming Interface

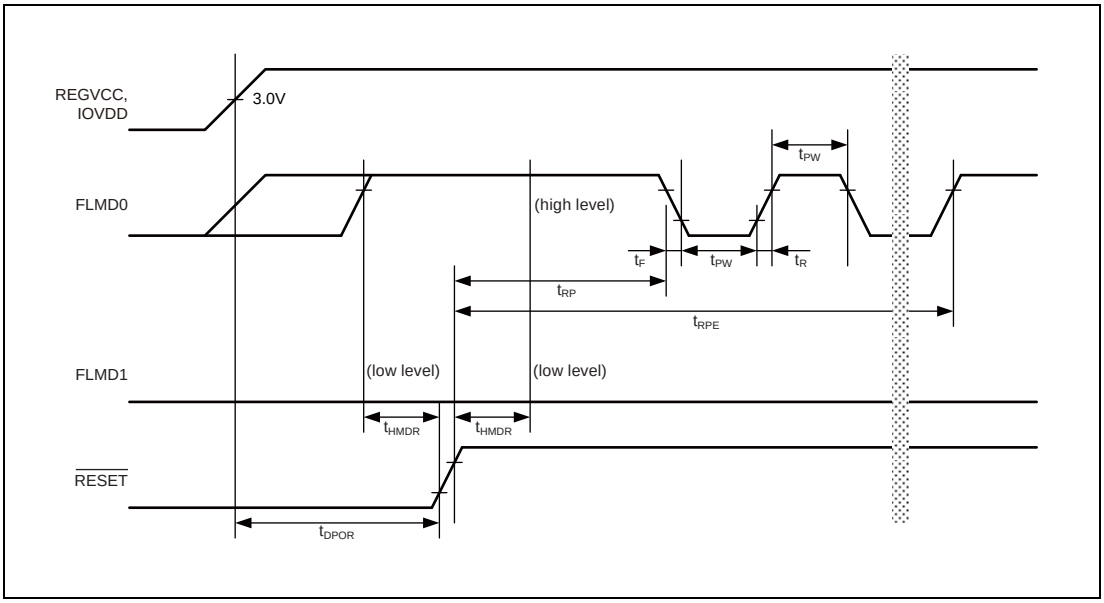
1.27.1.1 Serial programmer setup timing

Condition: Ta = 0 to 40°C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REGVCC ↑ and IOVDD ↑ to RESET ↑ delay time	t_{DPOR}		2			ms
FLMD0, 1 setup time (vs RESET ↑)	t_{SMDR}		1			ms
FLMD0, 1 hold time (vs RESET ↑)	t_{HMDR}		1			ms
FLMD0 pulse input start time	t_{RP}		1.5			ms
FLMD0 pulse input end time	t_{RPE}				11.5	ms
FLMD0 low/high level width	t_{PW}		0.8			µs
FLMD0 rise time	t_R				20	ns
FLMD0 fall time	t_F				20	ns

NOTE

IOVDD: EVCC = A0VREF



1.28 Core Voltage Monitor Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High AWOVCL, ISOVCL detection voltage	VCVMH		1.40	1.50	1.60	V
Low AWOVCL, ISOVCL detection voltage	VCVML		1.00	1.05	1.10	V
Response time	t_{D_CVM}		0.2		10	µs

1.29 A/D Converter Characteristics

(1/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Macro operation clock					8		40	MHz
Resolution	RESn	12-bit mode			12	12	12	bit
		10-bit mode			10	10	10	bit
A0VREF voltage range	A0VREF				3.0		5.5	V
Conversion time	T_{CONn}				1.15			µs
Overall error*1	TOEn	12-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm, w/o channel T&H			±4.0	LSB
				ADCA0I0-5, w/channel T&H			±6.0	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm, w/o channel T&H			±6.0	LSB
				ADCA0I0-5, w/channel T&H			±8.0	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm, w/o channel T&H			±8.0	LSB
				ADCA0I0-5, w/channel T&H			±10.0	LSB
		10-bit mode	AnVREF = 4.5 V to 5.5 V	ADCAnIm			±1.0	LSB
				ADCAnImS			±2.0	LSB
			AnVREF = 3.6 V to 4.5 V	ADCAnIm			±1.5	LSB
				ADCAnImS			±2.5	LSB
			AnVREF = 3.0 V to 3.6 V	ADCAnIm			±2.0	LSB
				ADCAnImS			±3.0	LSB
Analog input voltage	VAIN0SN	Channel T&H not used			AnVSS		AnVREF	V
		Channel T&H used			0.2		A0VREF – 0.2	V
Recovery time from power down		Deep STOP mode			1			µs
Operation current	IA0VREF	Channel T&H not used				1.1	3.0	mA
		Channel T&H used (6 pins)					*2	mA
STOP, DeepSTOP, CyclicSTOP current (@LPS is stopped)	IA0VREFS					1	10	µA
Channel T&H current	ITH					0.5	1.3	mA/ch
Channel T&H hold time	t_{THHOLD}				0.2		10	µs

(2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Accuracy of self-diagnosis function	TESH0SN	12bit mode	Self-diagnosis voltage level = A0VREF	4015-|TOEn|		4095	LSB
			Self-diagnosis voltage level = 2/3A0VREF	2651-|TOEn|	2731	2811+|TOEn|	LSB
			Self-diagnosis voltage level = 1/2A0VREF	1968-|TOEn|	2048	2128+|TOEn|	LSB
			Self-diagnosis voltage level = 1/3A0VREF	1285-|TOEn|	1365	1445+|TOEn|	LSB
			Self-diagnosis voltage level = A0VSS	0		80+|TOEn|	LSB
		10bit mode	Self-diagnosis voltage level = A0VREF	1003-|TOEn|		1023	LSB
			Self-diagnosis voltage level = 2/3A0VREF	663-|TOEn|	683	703+|TOEn|	LSB
			Self-diagnosis voltage level = 1/2A0VREF	492-|TOEn|	512	532+|TOEn|	LSB
			Self-diagnosis voltage level = 1/3A0VREF	321-|TOEn|	341	361+|TOEn|	LSB
			Self-diagnosis voltage level = A0VSS	0		20+|TOEn|	LSB

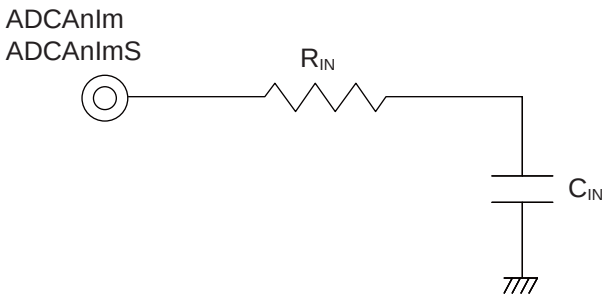
Note 1. This does not include quantization error.

Note 2. 3.0 + 1.3 × (the number of used channel T&H)

CAUTION

Applying a digital pulse to the AP0 pin during A/D conversion may lead to the result of A/D conversion not being as expected due to coupling noise. The same problem may arise in operation of the digital buffer as an output pin. Therefore, we recommend not using the digital buffer in applying pulses to the AP0 pin, in output operation, and in similar operations during A/D conversion.

1.29.1 Equivalent Circuit of the Analog Input Block



Terminals	Condition	RIN (kΩ)	CIN (pF)
ADCA0I0-5	When channel T&H is used	6.2	2.1
	When channel T&H is not used	2.4	3.3
ADCA0I6-15	—	2.4	3.3
ADCA0I0S-3S, 5S-16S		3.6	8.4
ADCA0I4S, 17S-19S	—	5.4	8.4

CAUTION

This specification is not tested during outgoing inspection. Therefore RIN and CIN are reference values only and not guaranteed. In addition these values are specified as maximum values.

1.30 Flash Characteristics

(1) Code Flash

The code flash memory is shipped in the erased state. If the code flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Table 1.9 Basic characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}		4		40	MHz
Operation voltage	V_{DD}		3.0		5.5	V
Number of rewrites*1	CWRT	Data retention 20 years*2	1000			times
Programming temperature (Ta)	TPRG	R7F7010xx2	–40		85	°C
		R7F7010xx3	–40		105	°C
		R7F7010xx4	–40		125	°C

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 1000), the device can be erased “n” times for each block. For example, when a block of 32 KB is erased after 256 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Table 1.10 Programming characteristic

Item	Symbol	Condition	Block size	MIN.	TYP.	MAX.	Unit
Programming time		fPCLK ≥ 20 MHz CWRT < 100 times	256 B		2*1	6*1	ms
			8 KB		50	90	ms
			32 KB		200	360	ms
			2 MB		12.5	21.5	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	256 B		2.4*1	7.2*1	ms
			8 KB		60	108	ms
			32 KB		240	432	ms
			2 MB		15	26	s
Erasure time		f_{PCLK} ≥ 20 MHz CWRT < 100 times	8 KB		50	120	ms
			32 KB		200	480	ms
			2 MB		12.8	28	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	8 KB		60	144	ms
			32 KB		240	576	ms
			2 MB		15.4	33.6	s

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

(2) Data Flash

The data flash memory is shipped in the erased state. If the data flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception

Table 1.11 Basic characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}		4		40	MHz
Operation voltage	V_{DD}		3.0		5.5	V
Number of rewrites*1	CWRT	Data retention 20 years*2	125 k			times
		Data retention 3 years*2	250 k			times
Programming temperature (Ta)	TPRG	R7F7010xx2	–40		85	°C
		R7F7010xx3	–40		105	°C
		R7F7010xx4	–40		125	°C

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 125000), the device can be erased “n” times for each block. For example, when a block of 64 bytes is erased after 4 bytes of writing have been performed for different addresses 168 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the data flash memory.

Table 1.12 Programming characteristics

Item	Symbol	Condition	Block size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz	4 B		0.3*1	1.7*1	ms
		f_{PCLK} ≥ 20 MHz	32 KB		2.5	6.8	ms
Erasure time		f_{PCLK} ≥ 20 MHz	64 B		3*1	10*1	ms
		f_{PCLK} ≥ 20 MHz	32 KB		1.6	5.2	ms
Blank check time		f_{PCLK} ≥ 20 MHz	4 B			30*1	µs
			64 B			100	µs

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

1.31 Injection Currents

Table 1.13 Definition of Pin Group

Symbol	Power Supply for Pin Group	Pin
PgE	EVCC, EVSS	$\overline{\text{RESET}}$, FLMD0, JP0, P0, P10, P11
PgA0	A0VREF, A0VSS	AP0

1.31.1 Absolute Maximum Ratings

Condition: Ta = 25°C

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJPM}	PgE	Per pin			10	mA
			Total			60	mA
		PgA0	Per pin			10	mA
			Total			60	mA
Negative overload current VIN < VSS	I_{INJNP}	PgE	Per pin			–10	mA
			Total			–60	mA
		PgA0	Per pin			–10	mA
			Total			–60	mA

CAUTIONS

1. The DC injection current (total) must satisfy the specifications of the injection current per pin.
2. Do not impress an overvoltage on P8 and P9 pins.

1.31.2 DC Characteristics for Overload Current

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJP}	PgE	Per pin			2	mA
			Total			50	mA
		PgA0	Per pin			3	mA
			Total			20	mA
Negative overload current VIN < VSS	I_{INJIN}	PgE	Per pin			–2	mA
			Total			–50	mA
		PgA0	Per pin			–3	mA
			Total			–20	mA

NOTE

These specifications are not tested on sorting and are specified based on the device characterization.

1.31.3 DC Characteristics for Pins Influenced by Injected Current on an Adjacent Pin

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Leakage current coupling factor for positive overload current	K_{INJP}	PgE			3.0×10^{-6}	—
		PgA0			4.8×10^{-6}	—
Leakage current coupling factor for negative overload current	K_{INJN}	PgE			7.5×10^{-6}	—
		PgA0			2.6×10^{-6}	—

NOTES

1. These specifications are not tested on sorting and are specified based on the device characterization.
2. An overload current through a pin will cause a certain error current in the adjacent pins. This error current must be added to the respective leakage current (ILIH or ILIL) of the adjacent pins.
3. The amount of error leakage current depends on the overload current and is defined by the overload coupling factor K_{INJ}.
   The total current through a pin is:
   $| I_{total} | = |$ ILIH or ILIL $| + (| I_{INJn} | \times K_{INJn})$

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Degradation of overall error*1	I_{INJP}	Par = 3 mA			±1.3	LSB
		Total = 20 mA			±3.8	LSB
	I_{INJN}	Par = –3 mA			±1.4	LSB
		Total = –20 mA			±4.5	LSB

Note 1. This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Note: These specifications are not tested on sorting and are specified based on the device characterization.

CAUTION

When there is an increased leakage current on the analog input pins, based on currents injected into the pins adjacent to the converted channel, the effect on the ADC accuracy depends on the external analog source impedance.

[Example] Conditions: A0VREF = 5.0 V, external analog source impedance = 10 kΩ.

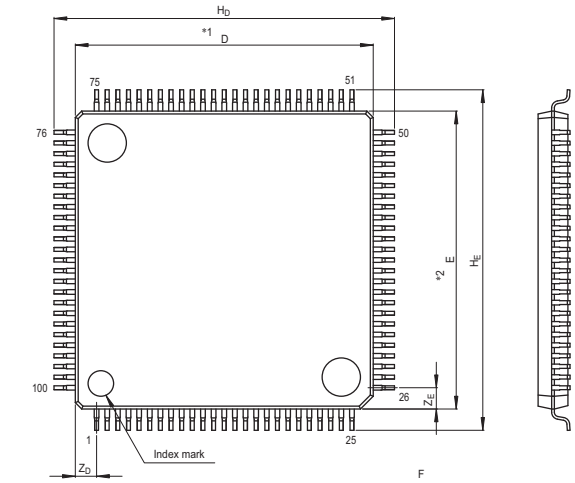
If there is a leakage current of 1μA by injected current, the effect on the ADC accuracy is 1 (μA) × 10 k (Ω) / 5 (V) = 0.2%FSR

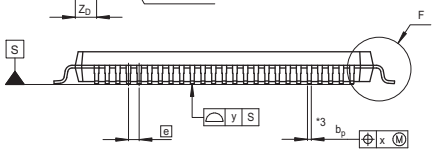
1.31.4 A/D Diagnosis Function Influenced by Injected Current

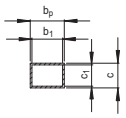
Refer to **Section 1.29, A/D Converter Characteristics**.

Section 2 Package Dimensions

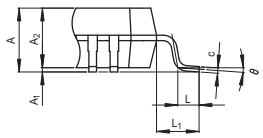
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g







Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	RH850/F1L (100-Pin Version) Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Jun 25, 2013	—	First Edition issued
0.81	Dec 03, 2013	1	1.1.2.1 Common Conditions, Power supply, Capacitance of the internal regulator changed
		4	1.2.3 Port Current changed
		5	1.3 Capacitance, note 1 and note 2 changed
		5	1.4 Operational Condition, note 2 changed
		5	1.5 Oscillator Characteristics, CAUTION changed
		6	1.7 PLL Characteristics changed
		6	1.8 Regulator Characteristics changed; note 1 changed
		7, 8	1.9 Pin Characteristics changed, note 2 and note 6 changed
		9	1.10 Power Supply Currents changed
		11	1.11 Interrupt Timing changed
		12	1.12 Power Up/Down Timing, timing diagram changed
		18	1.20.2 CSIH Timing, CAUTION changed
		31	1.24 POC Characteristics changed
		32	1.25 LVI Characteristics, changed
		33	1.26 VLVI Characteristics changed
		35	1.28 Core Voltage Monitor Characteristics changed
		35, 36	1.29 A/D Converter Characteristics changed
		37	1.30 Flash Characteristics, (1) Code Flash, Table 1.9 Basic Characteristics, note 2 changed
		37	1.30 Flash Characteristics, (1) Code Flash, Table 1.10 Programming Characteristics changed
		38	1.30 Flash Characteristics, (2) Data Flash, Table 1.11 Basic Characteristics, note 2 changed
		38	1.30 Flash Characteristics, (2) Data Flash, Table 1.12 Programming Characteristics, note 2 changed
		39, 40	1.31 Injection Currents, added

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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