intel.

Intel® Power Thermal Analysis Tool (Intel® PTAT) – Server Edition

User Guide

September 2023

Revision 4.4.0

Intel Confidential

Intel Confidential

Contents

Intel Confidential

intel

Figures

Tables

Revision History

Revision Number	Description	Date
4.4	• New memory intensity test added. • Intel® Advanced Matrix Extension (Intel® AMX) exercisable workload added on Linux.	December 2023
4.3	• PMAX changes for Windows.	August 2023
4.2	• Added support for Birch Stream.	August 2023
4.1	• Added Emerald Rapids support. • Updated user guide with more details on changes in nTDP test.	June 2023
4.0	• Intel® PTU renamed as Intel® Power and Thermal Analysis Tool (Intel® PTAT).	January 2023
3.2	• Removed Extended Rd/Wr Memory test option. • Removed turbo test option for "All Cores". • Notes on PMAX test workload.	October 2022
3.1	• Added BIOS settings for PCSTATE Test. • Updated PCSTATE Test Description and examples. • Updated Windows* System Requirements and Settings.	September 2022
3.0	• PCSTATE test update. • Updated Running the Test and Monitor in GUI Mode Intel® PTU usage.	May 2022
2.9	• High Bandwidth Memory (HBM) test case description. • Mem Test update.	April 2022
2.8	• Wording updates.	January 2022
2.7	• Updated the Intel® Optane™ PMem stress guide.	December 2021
2.6	• Updated for SRMT feature integration. • Updated for pcstate and PMem feature integration. • Minor wording changes and Notes added for BIOS settings.	October 2021
1.2	• Added NVDIMM monitor fields information.	January 2020
1.1	• Updated for Unified Intel® PTU 2.0 release.	October 2019
1.0	• Initial release	February 2019

1 Introduction

1.1 Purpose of This Document

This document describes the use and operation of Intel® Power Thermal Analysis Tool (Intel® PTAT) for Windows* and Linux*. The Intel® PTAT tool is intended for thermal and power delivery testing only. It is not intended for performance testing. The intended use is to run the different tests that are implemented to gather data on temperature, power delivery and CPU frequency.

1.2 Reference Documents

Users may find valuable information related to Intel® PTAT in a variety of specifications and Intel documents, listed in the following table.

Table 1-1. Reference Documents

Title	Document Number
Intel® Power Thermal Analysis Tool (Intel® PTAT) for Windows*	637674
Intel® Power Thermal Analysis Tool (Intel® PTAT) for Linux*	637673
3rd Generation Intel® Xeon® Scalable Processors, Codename Ice Lake-SP External Design Specification (EDS), Volume One: Architecture	574451
3rd Gen Intel® Xeon® Scalable Processor, Codename Ice Lake External Design Specification (EDS), Volume Two: Registers	574942
3rd Gen Intel® Xeon® Scalable Processors, Codename Ice Lake BIOS Writer's Guide	594768
Intel® Xeon® Processor Scalable Family and Cascade Lake Thermal/Mechanical Specification and Design Guide (TMSDG)	547814
Skylake-FPGA TMSDG Addendum -	560573
Intel® Xeon® Processor Scalable Family-based Platforms Windows* PTU	560555
Skylake-SP Server Processor Based Platforms Linux* PTU	560556
Intel® Xeon® Processor Scalable Memory Family External Design Specification, Volume Two: Registers, Part A	546832
Intel® Xeon® Scalable Family/2nd Generation Intel® Xeon® Scalable Family of Processors External Design Specification Volume Two: Registers, Part B	546833
Intel® Xeon® Processor Scalable Family (Skylake) and Cascade Lake Server Processor External Design Specification (EDS) Volume Three: Electrical	546834
Purley Platform Skylake PMax Detection Circuit	548692
Intel® Optane™ PMem 200 Series Memory Linux* Testing Guidance	619351
Eagle Stream Server and Fishhawk Falls Workstation Platforms Thermal Mechanical Specification Design Guide (TMSDG)	609847

Intel Confidential

1.3 Definition of Terms

The following table lists and defines the most relevant terms used in this document.

Table 1-2. Terms Definitions

Term	Definition
Intel® Advanced Vector Extensions	Intel® Advanced Vector Extensions (Intel® AVX) promotes legacy 128-bit SIMD instruction sets that operate on XMM register sets to use a Vector Extension (VEX) prefix that operates on 256-bit Vector Registers (YMM).
Intel® Advanced Vector Extensions 512	The base of the 512-bit SIMD instruction extensions is referred to as Intel® Advanced Vector Extensions 512 (Intel® AVX-512) foundation instructions. They include extensions of the Intel® AVX family of SIMD instructions but are encoded using a new encoding scheme, which supports 512-bit vector registers and up to 32 vector registers in 64-bit mode.
DDR4/DDR5	The Fourth and Fifth generation of the DDR SDRAM memory technology.
DTS	Digital Thermal Sensor
nTDP	Near TDP, a feature within the Intel® PTAT to achieve a close-to-TDP power level.
PCH	Platform Controller Hub, the next generation chipset with centralized platform capabilities, including the main I/O interfaces, along with display connectivity, audio features, power management, manageability, and security and storage features.
PECI	Platform Environment Control Interface (PECI), one-wire interface that provides a communication channel between Intel's processor and chipset components to external monitoring devices.
Intel® PTU	Intel® Power Thermal Utility
Intel® PTAT	Intel® Power Thermal Analysis Tool
Intel® SSE	Intel® Streaming SIMD Extensions (Intel® SSE)
TCASE_MAX	The maximum die operating temperature, as measured at the geometric center of the package substrate at the top of the Integrated Heat Spreader (IHS).
TDP	Thermal Design Power (TDP), thermal solutions should be designed to dissipate this target power level. TDP is not the maximum power that the chipset can dissipate.
TMARGIN	The delta between the hottest die temperature and the DTS thermal profile.
TSENSOR	The die temperature as reported by the device DTS.
TSOD	Temperature Sensor on DIMM (TSOD)
PMax (aka PMax.max)	This is a rare loading condition that equates to the maximum instantaneous electrical total power drawn from all rails in a processor package, typically running virus (a synthetic stress application) specifically designed to reach maximum consumed power with an ALL-core Turbo and TjMax scenario. The recipe to reach PMax.max for Sapphire Rapids and later products is under development.

Intel Confidential

Term	Definition
PMax.app	This is less than PMax and an electrical power threshold drawn from ALL rails in a processor package, typically running realistic application(s) at an ALL-core turbo frequency. The worst case PMax.App event can occur with Intel® AVX1, Intel® AVX2, Intel® AVX3 or TMUL licenses. These are real-workload worst case applications that is, non-virus. The Pmax.App condition must be sustained by the PSU, the processor voltage regulators, and if not met would impact processor performance. Due to variance in Silicon characteristics, not all parts will reach or exceed the Pmax.App guidelines and a recipe is provided below using Stress Virus applications to mimic real world worst application loading.
IccIN_Max (aka IccMax.max)	This is a rare loading condition and is the highest VccIN only instantaneous maximum electrical current drawn. This VccIN current may or may not correspond to Pmax loading condition, as this current is only for the VccIN VR, and it depends if the allocated VccIN power's portion is worst case for from the Pmax loadling condition. VccIN OCP must be set above IccIN_Max.
IccIN_Max.app	This is less than IccMax and is the electrical current drawn by the VccIN VR only, while running realistic applications at P0nmax and Tjmax and is the current the VR and PSU must be able to sustain. This is the current of the VccIN VR corresponding to PMax.App. Intel extensively surveys real world applications and optimizes the processor to deliver the best possible performance for these workloads. Systems that cannot support up to IccMax.App may see a performance impact for some real applications.

1.4 Software Package

1.4.1 Linux*: Red Hat*, CentOS*, and Fedora*

The Linux* Intel® PTAT software package consists of:

- Command-Line Interface (CLI) binaries:
  — **ptat** (executable): Includes the formerly known as **ptugen** (workload stress), and **ptumon** (thermal power monitoring and logging).
  — **ptusys**: This driver is needed to read and write the MMCFG address if the default kernel driver `/dev/mem` is not allowed to access above 1 M of system address space.
  — **pcstateMwaitLKM:** This driver is required to execute all the core state tests integrated in Intel® Power Thermal Utility (Intel® PTU) release version 3.5.

1.4.2 Windows*

The Windows* Intel® PTAT is provided in one installer that consists of:

- CLI binaries with option to run workload (ptugen) and monitoring (ptumon) concurrently.
- GUI binaries.

Intel's CCHWAPI driver.

2 Prerequisites and Installation

2.1 Prerequisites

Intel® PTAT is developed to be run as superuser (Linux*: Root, Windows*: Administrator) only; it supports only 64-bit system (BIOS and OS in 64-bit mode).

For Windows*-GUI mode, the minimum screen resolution support is 1024×768.

2.2 System Requirements

Intel® PTAT Server edition supports the following Intel® Xeon® based processors:

- All Intel Xeon GNR-D Processor Families, codenamed Kaseyville D.
- All Intel® Xeon® D-1700 and D2700 Processor Families, codenamed Ice Lake D.
- All 4th Gen Intel® Xeon® Processor Scalable Family, formerly codenamed Sapphire Rapids single or multiple socket-based processors, non- High Bandwidth Memory (HBM) and HBM processors.
- All 1st Gen Intel® Xeon® processor Scalable family (codenamed Skylake) single- or multiple-socket-based processors single or multiple socket-based processors.
- All 2nd Gen Intel® Xeon® processor Scalable family (codenamed Cascade Lake) single- or multiple-socket-based processors, and Multi-Chip Package (MCP) processors.
- All 3rd Gen Intel® Xeon® Scalable family (codenamed Ice Lake) single- or multiple-socket-based processors Server single or multiple socket-based processors.
- All 3rd Gen Intel® Xeon® Scalable family (codenamed Cooper Lake) single or multiple socket-based processors, and MCP processors.

Intel® PTAT requires at least eight-GB memory for each socket to run, but 16 GB for each socket is recommended.

Near-TDP (nTDP) requires the Engineering Sample (ES) part to run.

Pmax and Pmax.App tests require additional measurement hardware to capture the maximum power. See *Purley Platform Skylake PMax Detection Circuit*, document number 569065, for more information.

For maximum power generation, do not run other commands or background processes that require higher CPU utilization.

2.3 Windows* System Requirements and Settings

Windows* supported versions:

- Windows Server* 2019 and 2022

Select the "High Performance" power plan setting under the "Control Panel/System and Security/Power Options" Windows* setting.

Intel® Advanced Vector Extensions 512 (Intel® AVX-512) require a Windows* registry update once and a reboot.

Before installing Intel® PTAT, please disable secure boot and memory integrity from BIOS otherwise Intel® PTAT will not work correctly.

For early Windows* versions such as Windows Server* 2008 without service pack:

Note: To prevent any issues with MSR access, disable the Windows Defender Credential Guard feature.

1. Modify the OS registry file by opening the "regedt32" program
2. Create a new key entry: "Extended State" inside
   `HKLM\\System\CurrentControlSet\Control\Session Manager\Kernel`
3. Create two QWORDS entries inside
   `HKLM\\System\CurrentControlSet\Control\SessionManager\Kernel\Extended State`
4. Set AllowedFeatures = 0xFF
5. Set ThreadPersistentFeatures = 0x10

2.4 Linux* System Requirements and Settings

Linux* OSs supported:

- Red Hat Enterprise Linux* (REHL*) 6.x, 7.x, and 8.x
- CentOS* 6.x, 7.x, and 8.x
- Fedora* 5.6.6-300.fc32.x86_64 for building PCSTATE driver and running core state tests.
- PTAT was tested on kernel versions 4.18, 5.19, 6.2.

2.5 BIOS Settings

Enable RAPL (Running Average Power Limit) and set the DIMM thermal configuration in the BIOS to Closed-Loop Thermal Throttling (CLTT) mode for DIMM temperature support.

For Windows* Intel® PTAT, secure boot must be disabled.

The Intel® Optane™ persistent memory (Intel® Optane™ PMem) module DIMM must be configured in App Direct (AD) mode for maximum power and bandwidth. Two-Level Memory (2LM) mode may not provide the maximum power and thermal conditions due to the DDR4 acting as the Intel® Optane™ PMem cache.

Turn on the Intel® Hyper-Threading Technology (Intel® HT Technology) in the BIOS before using this utility. For core state tests, Intel® HT must be disabled.

P-state tests are supported with HW-P Disable and HW-P Native settings.

When HW-P Disable is set, acpi_cpufreq scaling driver is used and when HW-P Native is set, intel_pstate scaling driver is used.

2.6   Installation

2.6.1   Linux*

Install the Linux* Intel® PTAT by following these steps:

1. Log in under root user to the machine where the tool will be installed.
2. Run the following installation steps:
    ```
    # mkdir –p /root/ptat
    # cd /root/ptat
            Copy and unzip the <PTAT tar file>.tar to /root/ptat
    # tar xvf *ptat*.tar
    ```

Building the **ptusys** driver code:

On newer kernel versions (6.x), boot the kernel with ibt=off.

Kernel sources should be installed for your kernel version to build our kernel modules.

Try

yum install kernel-devel-$(uname -r) or

apt install kernel-devel-$(uname -r)

1. Log in under root user to the machine where the tool will be installed:
    ```
    # cd /root/ptat/driver/ptusys
    ```
2. Make the driver code and run install:
    ```
    # make clean all
    # make install
    ```

Building the **pcstateMwaitLKM** driver code:

3. Log in under root user to the machine where the tool will be installed:
    ```
    # cd /root/ptat/driver/pcstate
    ```

Intel Confidential

4. Make the driver code:

```
# make clean
# make
```

Loading the PCSTATE driver

5. insmod pcstateMwaitLKM.ko

Make sure **intel_vsec** drivers are installed

Note: Both **ptusys** and **pcstate** drivers require the development and kernel package to build. UFS and other die specific data on newer generation products require the respective upstream module/driver(s) to be available and loaded, otherwise zero values will be shown.

Yocto 5.10 customer release (GRR) comes with **intel_vsec** driver. **intel_vsec** driver and the **oobmsm** driver can't be loaded at the same time, neither will load automatically. For PTAT, the process will be

1. Install intel_vsec driver
   ```
   # modprobe intel_vsec,
   ```
2. run PTAT
3. Uninstall Install intel_vsec driver, when not needed.
   ```
   # rmmod intel_vsec.
   ```

Make sure Module C6 is enabled.

To enable command line help, either copy the ptat_usage.txt to the same location as PTAT binary or set the path for usage file using PTAT_HELP_DIR environment setting.

2.6.2   Windows*

Install the Windows* Intel® PTAT by following these steps:

1. Log in as Administrator to the machine where the tool will be installed.

2. Disable Windows Defender - Manage Windows Defender Credential Guard - Windows Security | Microsoft Learn

3. Copy the software installer to "Downloads" (or other temporary) folder.

4. Double-click the executable, the setup window will show:

Intel Confidential
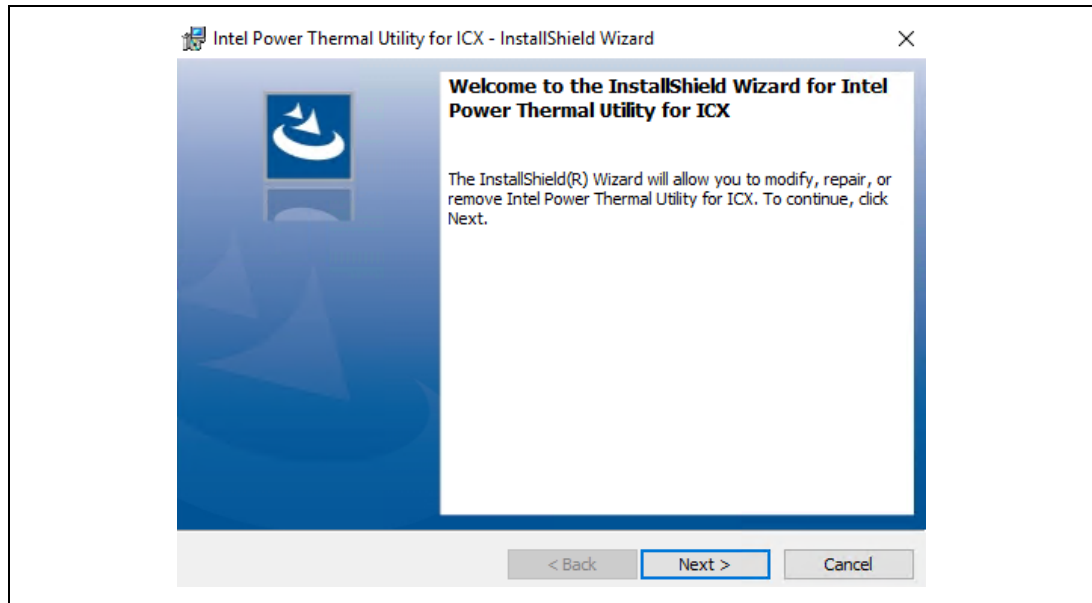
Note: If a previous version is already installed, you will need to remove the existing version of the Intel® PTAT first. Use "Add/Remove Programs" on the "Control Panel", navigate to the "Intel Power Thermal Utility – Server Edition", and then click **Uninstall**.

5. Follow the instructions as presented and accept the license. The default folder is: C:\Program Files\Intel\Power Thermal Utility – Server Edition.
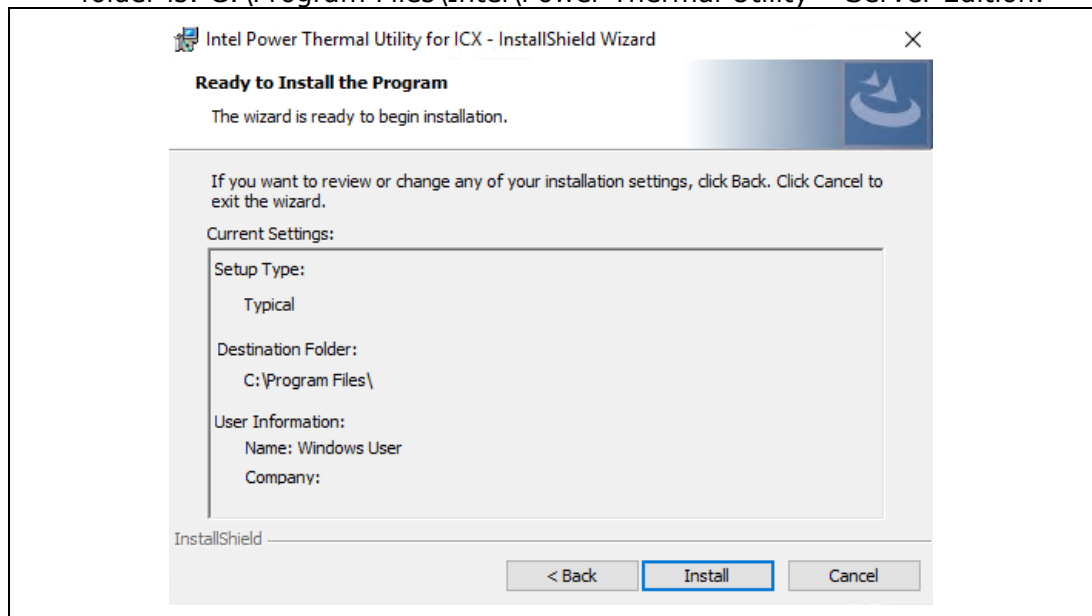
Uninstall the Windows* Intel® PTAT by following these steps:

1. Click the Windows* icon in bottom left corner, and then select the "Uninstall Server PTAT under Intel Power Thermal for…" menu.

Intel Confidential
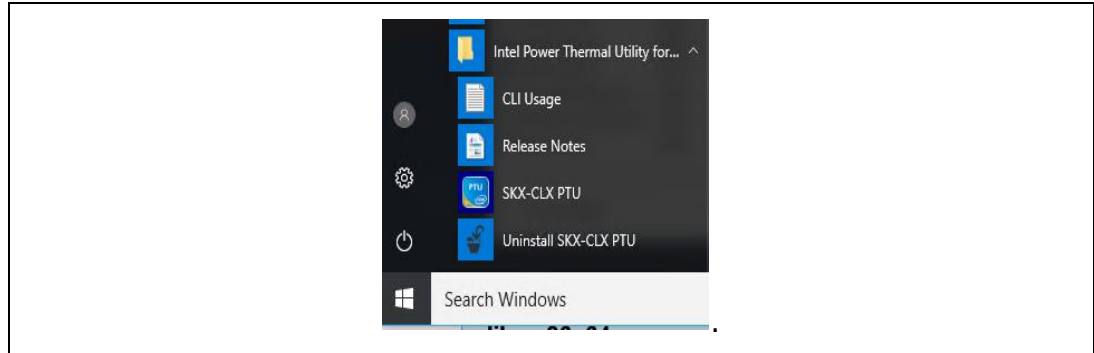
2. Or open "Control Panel" → "Programs and Features" and locate the Intel® PTAT installer then click **Uninstall**.

Intel Confidential

3 Intel® PTAT Tests Description

3.1 Intel® PTAT Test Features and Intended Use

The Intel® PTAT tests are designed for thermal and power delivery evaluations. This chapter describes the tests and their intended usages.

Note: Disable the turbo feature first before running the tests, turbo feature requires stable Silicon/TDP like QS and PRQ samples.

3.1.1 Thermal Design Power (TDP) Test

This test is intended to evaluate the thermal solution capability by executing a synthetic workload that mimics the Thermal Design Power (TDP) at Electrical, Mechanical and Thermal Specification (EMTS) conditions. The Digital Thermal Sensor (DTS) maximum and thermal profiles are based on the operation at P1 state, so the turbo feature should be disabled for TDP testing.

If the specification is met, then the part is expected to be less than or equal to the rated TDP and operate at the advertised base frequency while below the temperature limits. No throttling should be observed during this test.

Condition for Turbo test and power level test (100%):
1. Turbo should be off.
2. Temp should be constant using the thermal head.
3. HW P-State must be disabled.

Note: Not all parts are expected to reach the advertised TDP level with this test due to variation in manufacturing. If this is the case, the temperatures at TDP can be calculated using thermal resistance from case to ambient, or the "near TDP" feature can be used with some conservatism.

3.1.2 TDP Test with nTDP Enabled

This test uses the same workload as the "TDP test" but will increase core and uncore voltage levels until the advertised TDP is reached. nTDP is available on non-production parts only. For most cases, the package power will reach within about 3% of the advertised TDP.

Besides evaluating the thermal solution, this test is useful for system thermal testing by providing the maximum and worst cases preheat to the downstream components.

Because the nTDP increases the core and uncore voltage to reach the TDP, the result is a higher power density than the TDP workload; it is, therefore, a

slightly conservative test. It is expected that the nTDP feature might reduce the thermal margin by up to a few degrees.

From PTAT versions later than 4.0, run time option (-t) will have no effect while running the nTDP test. Manually collect the nTDP test data to check the voltage increment and power numbers. User action is required (ctrl-c) to terminate the process. Legacy automation code must update nTDP test cases to incorporate this change (post 4.0 builds).

3.1.3 Core IA/ Intel® Streaming SIMD Extensions (Intel® SSE) Test

Previously known as "Core Power Level Test". This test uses the same baseline as the TDP test, except that it allows the processor to stress the Intel® PTAT at several power levels. The user can also choose which core to test. This is helpful to evaluate fan speed control algorithms, power testing, or other sensitivity studies.

Note: Like the TDP Test, the Core IA/Intel® SSE test uses the Intel® SSE Intel® Advanced Vector Extensions (Intel® AVX) power codes as the workload. Because the power level is variable, it is possible to exceed the TDP of the part.

3.1.4 Core Intel® Advanced Vector Extensions 2 (Intel® AVX2), Core Intel® AVX-512, AMX/TMUL Tests

These tests use the Intel® AVX2 , Intel® AVX-512 and AMX instructions to stress the cores. Operations range from a light vector to a heavy vector. The user can choose which core to test and what power level to use. This test may generate higher power than the TDP power.

3.1.5 Pmax and Pmax.App Tests

These two tests are meant to test the power delivery mechanisms to the processor. The platform power delivery system that does not meet Intel processors' Pmax guidance may experience a system reset or a blue screen while running this test.

When running Pmax, the user should enable the turbo feature and run the part at a higher Tj temperature (getting a DTS about 5).

Notes:

- When the Pmax detector circuit is asserted, the T-STAT [bit 3] and T-LOG [bit 3] is set. If the bit 3 is the only thing set, you should expect a value of 0x8.
- As processor complexity increases, the uncore power footprint has increased. This affects generation of, "TDP-like," workloads using a core-only approach. We suggest multiple workloads at the same time across multiple processor technologies.

- Additional power measurement hardware may be needed to capture the expected power spike because of the fast-sampling rate needed.
- The PTAT PMAX test may not reach expected power levels as specified in *Eagle Stream Platform External Design Specification (EDS), Volume Three: Electrical*, document number 613206.
- A mutli-part workload is being developed to better test PMAX.APP on Eagle Stream processors. At this time, it may not be possible to reach rated PMAX values on Sapphire Rapids or Emerald Rapids processors.

3.1.6   Turbo Check Test

Turbo check allows the user to verify that turbo frequencies are met in accordance with the published values. The test will sweep through core configurations (P0n) to report power, core and uncore frequencies, utilization, temperature, and voltage (IA Intel® SSE, Intel® AVX2 and Intel® AVX-512 workloads will be used). This evaluation will check that the part can reach the maximum turbo frequencies specified, +/- 1 bin off difference with frequencies is acceptable. For specific frequency validation test use, contact your Field Applications Engineer (FAE) for further assistance of the tool.

Depending on the number cores and bins, turbo test creates multiple turbo records during turbo test. You will find some records where frequency bin more than +- one bin. If you have more than 90% of passing (+-1 bin) records then we consider it a passing turbo test.

To achieve the result in the frequency binning system throttling is possible, which can bring down the core and bus frequency.

Condition for Turbo test:
   a. C1 auto demotion disabled.
   b. SGX disabled in BIOS.
   c. C6 being enabled.
   d. Memory integrity disabled.
   e. HW-P state disabled.
   f. C state enabled.
   g. Energy efficient turbo disabled.

Note: Enable the turbo feature first before running the test. Otherwise, it will run without turbo.

3.1.7   Memory (MEM) Tests

This test stresses the processor's memory power rails. The user can choose which core to execute the memory test. By default, the test uses a 64-MB memory size for each core thread to do a Read/Write (R/W):

- **Read**: Performs a sequential read-only operation on the given cores.

- **Write**: Performs a sequential write-only operation on the given cores.

- **Read/Write**: Performs both read and write operations sequentially. The test will do 50% writes and 50% reads.

Intel Confidential

For memory power data correlation, contact your memory supplier.

3.1.8 PMem Tests

3.1.8.1 Windows*

This test stresses the processor's memory power rails that are supplied to PMem module DIMMs. The user can choose which core to run the AD R/W to and from the PMem. This test uses Intel® AVX-512 instructions to do load and store operations. Make sure that the current OS is supporting Intel® AVX-512 instructions. By default, the test uses a 256 MB memory size and 100% power level for each core thread to do a R/W.

- **AD read:** Performs an AD read-only operation on the given cores.
- **AD write:** Performs an AD write-only operation on the given cores.
- **Use custom:** Performs either an AD read or write operation based on the selection in the "Memory Test" configuration.

Notes:

- A different core count will influence the "Power and Bandwidth" of the memory test.
- MEM and PMem tests can be run together with the CPU test by checking both CPU and MEM and PMem check boxes. However, by doing so, the cores activity might be reduced, and the overall package power might be lower as well. For the best result, select more cores assigned to CPU test and fewer cores assigned to the MEM and PMem tests.

3.1.8.2 Linux*

Currently, a single stress with the R/W operation for Intel® Optane™ PMem is provided. To get the maximum power on the processor's memory power rails and the maximum bandwidth on the memory bus, all the available cores on the systems are used. The Intel® HT Technology option is also enabled.

Before running the Intel® Optane™ PMem test, provision the PMem with the number of regions equals to the number of sockets (cpus). For example, for a two-socket configuration, provision two regions with two namespaces and mount them as two directories for two sockets. The directories can be provided using the option "pmdir" as explained in Intel® PTAT Available Commands and Command Line Options. For provisioning, see *Intel® Optane™ PMem 200 Series Memory Linux* Testing Guidance*, document number 619351.

Note: The referenced document could change with the update for newer versions of Intel® Optane™ PMem.

Intel Confidential

3.1.9   PCSTATE Tests

The C State test sets the specified CPU(s) and its core(s) to a particular C-State, as indicated by the test parameter. The test keeps the target cores in that C-State for a user-specified interval up to a maximum duration (15 million microseconds). The test can be run for extended durations using a repeat option as another parameter. By default, the test sets the target cores to C0 for three million microseconds and repeats for five times.

The P State test sets the specified CPU(s) and its core(s) to a particular P-State, as indicated by the test parameter. The test keeps the target cores in that P-State for a user-specified interval up to a maximum duration (15 million microseconds). The test can be run for extended durations using a repeat option as another parameter. The frequency of the cores is maintained at the P-state specified.

Please disable soft lockup in the kernel, while running the PCstate tests. You can use 'sudo sysctl kernel.soft_watchdog=0' to do this.

3.1.10 HBM Test

HBM (High bandwidth memory) test can be done by booting the system without DDR memory. This configuration is equivalent to the system where HBM is being used as the replacement to DDR memory.

Now running the DDR stress test should generate more package power and temperature in comparison with the CPU which does not have HBM and using DDR. The difference between these two configurations should show how power and temp is added by the HBM component.

So HBM power (run DDR stress) = CPU with HBM – CPU without HBM

Note: Intel® PTAT does not report bandwidth, temperature, and power for HBM package die.

4 *Intel® PTAT Monitor*

This section describes the Intel® monitor features and usage.

4.1 Intel® PTAT Monitor Data

The following table lists the Intel® PTAT monitor data, as it is shown un the command line format (fields/columns):

Table 4-1. 4.1   Intel® PTAT Monitor Data

Field	Column
Timestamp	The time field consists of mm/dd/yy, 24 hours, minutes, seconds, and milliseconds.
TSDLT	The time delta between last sample and current. If delta is more than one second, it will display ">1sec.
Device	The monitored devices: CPU, MEM, PCH, and FPGA.
Cor	Shows the core number of the monitored CPU.
Thr	Shows the thread number of the monitored core.
CFreq	Shows the current average CPU (core) and thread frequency in Megahertz (MHz).
UFreq	Shows the current uncore frequency in Megahertz (MHz).
PState	Shows the frequency state of the core. P0 representing the highest frequency (performance) and Pn representing the lowest frequency (efficient).
Util	Shows the current average CPU/core and thread utilization in percentage (%).
IPC	Shows the average of retired instructions per cycle of the CPU/core.
C0	Shows the core in active state.
C1	Shows the core in halt state.
C6	Shows the core in low power state.
PC2	Shows how the CPU in Package C2 state.
PC3	Shows how the CPU in Package C3 state (for 3rd Gen Intel® Xeon® Scalable processors, codename Ice Lake only).
PC6	Shows how the CPU in Package C6 state.
PC7	Shows how the CPU in Package C7 state (for 3rd Gen Intel® Xeon® Scalable processors, codename Ice Lake only).
MC	The memory controller number of the monitored memory.
Ch	The memory channel number of the monitored memory.
SI	The DIMM slot number of the monitored memory.
Read	Shows the current memory read bandwidth (per channel).
Write	Shows the current memory write bandwidth (per channel).

Field	Column
DDRT-Rd	Shows the current DCPMM read bandwidth (per channel).
DDRT-Wr	Shows the current DCPMM write bandwidth (per channel).
DTS	Shows the current maximum package and core DTS.
Temp	The Temperature column shows the current die temperature in Celsius (°C) degrees.
Volt	Shows the current average CPU and core voltage.
UVolt	Shows the current uncore voltage (for 3rd Gen Intel® Xeon® Scalable processors, codename Ice Lake only).
Power	Shows the current power in Watts (W) of CPU/Memory/FPGA.
TStat	Shows thermal status of the monitored CPU: **bit-0**: Thermal Throttle - this indicates whether the thermal sensor high temperature signal is active. **bit-1**: PROCHOT - this indicates whether PROCHOT# signal is asserted. **bit-2**: Critical Temperature - this indicates whether the temperature is above the max. operating temperature. **bit-3**: Pmax - this indicates whether Pmax detector circuit has asserted.
TLog	Shows the thermal status log of the monitored CPU/Memory (see TStat for bit field descriptions).
#TL	Shows number of TLog events being hits.
TMargin	Shows the thermal margin of the monitored CPU.
N-CTemp	Shows DCPMM controller temperature (NVDIMM only).
N-MTemp	Shows DCPMM media temperature (NVDIMM only).
N-DCPwr	Shows DCPMM total power (NVDIMM only).
N-12VPwr	Shows DCPMM 12V power (NVDIMM only).
N-1.2Pwr	Shows DCPMM 1.2V power (NVDIMM only).

**Intel Confidential**

5 Running Intel® PTAT on Windows*

The Intel® PTAT GUI can be launched from the installed Intel® PTAT icon on the Windows* desktop or using the Windows* menu "Start Menu" → "Intel Power Thermal Utility – Server Edition" → "PTAT".

7
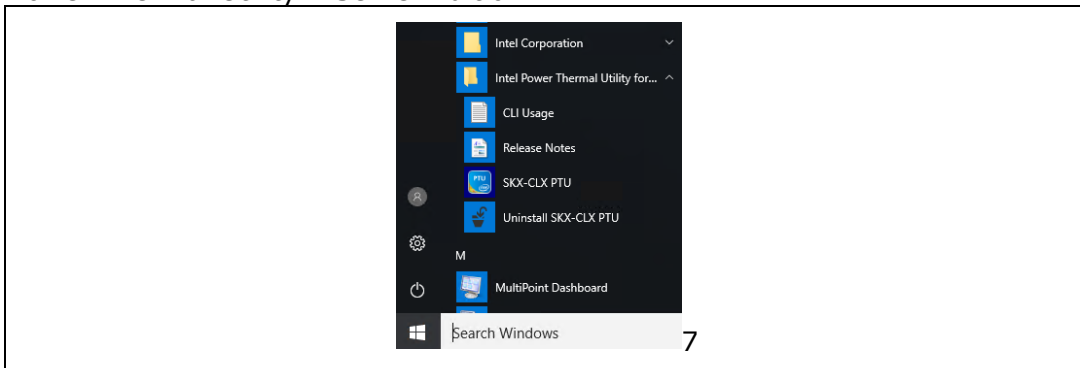
5.1 Running the Test and Monitor in CLI Mode

The Intel® PTAT CLI shares the same executable as the GUI Intel® PTAT (PTAT.exe). The file is located at `C:\Program Files\Intel\Power Thermal Utility – Server Edition`. Open a Windows Command Prompt* application with administrator privileges:
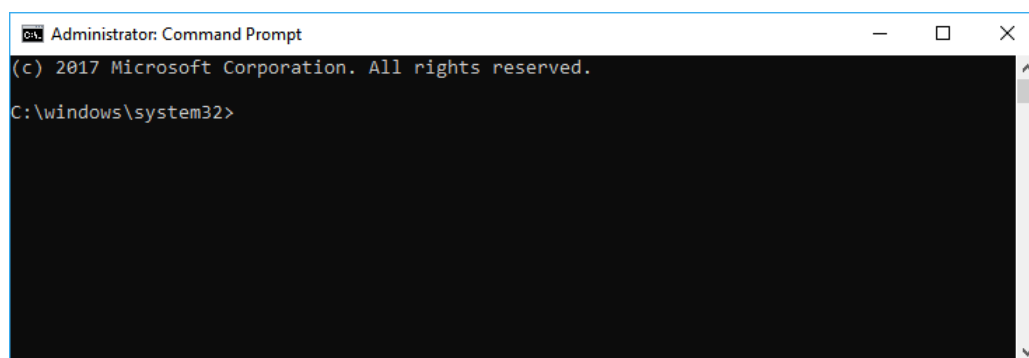
Change the directory to `C:\Program Files\Intel\Power Thermal Utility – Server Edition\`.

Run the Intel® PTAT either specifying PTAT.exe by itself or using the start program to launch the Intel® PTAT command.

For example, to run the CPU TDP test: `> start /wait ptat.exe –ct 1`

When running Intel® PTAT in command-line mode, the user needs to specify at least a test to run. The monitor can be executed by itself without any test running. Use the –mon option to run as monitor mode, or use –log to log data in the background.

5.1.1   Running Test Examples

- Run default TDP test with turbo off:
  ```
  > start /wait ptat.exe ct 1 –b 0
  ```

- Run TDP with near-TDP enabled:
  ```
  > start /wait ptat.exe –ct 2
  ```

- Run the core Intel® AVX-512 with power level 50% and turbo on:
  ```
  > start /wait ptat.exe –ct 5 –cp 50 –b 1
  ```

- Run the core IA/Intel® SSE with power level 70% on core 1, 2, 3 and 7:
  ```
  > start /wait ptat.exe –ct 3 –cp 70 –cpucore 0x8E
  ```

- Run Pmax on socket 0 only:
  ```
  > start /wait ptat.exe –ct 6 –cpu 0x1
  ```

- Run the turbo test using Intel® AVX-512 instructions only:
  ```
  > start /wait ptat.exe –ct 8 –avx 3 –b 1
  ```

5.1.2   Running Intel® PTAT Monitor Examples

- Run the default Intel® PTAT monitor:
  ```
  > start /wait ptat.exe –mon
  ```


- Run the Intel® PTAT monitor in long version (level 2) with core 0, 1 showing only:
  ```
  > start /wait ptat.exe –mon –l 2 –moncore 0x3
  ```

Intel Confidential

```
Administrator: Command Prompt                                                    —  □  ×

Index Device Cor Thr CFreq UFreq  Util  IPC Temp DTS  Power  Volt UVolt TStat TLog #TL TMargin
    1 CPU0    -   -  1832   900  0.38 1.01   34  71   24.6 1.162 0.762   0x0  0x0   0  60.609
    1 CPU0    0   -  2453     -  1.26 1.82   28  77      - 1.140     -   0x0  0x0   0       -
    1 CPU0    0   -  2909     -  2.39 1.02    -   -      -     -     -     -    -    -       -
    1 CPU0    0   -  1997     -  0.14 0.80    -   -      -     -     -     -    -    -       -
    1 CPU0    1   -  2161     -  0.48 0.60   29  76      - 1.140     -   0x0  0x0   0       -
    1 CPU0    1   -  1682     -  0.25 0.34    -   -      -     -     -     -    -    -       -
    1 CPU0    1   -  2641     -  0.71 0.27    -   -      -     -     -     -    -    -       -
    1 CPU0    2   -  1922     -  0.48 1.46   26  79      - 0.902     -   0x0  0x0   0       -
    1 CPU0    2   -  2025     -  0.62 0.19    -   -      -     -     -     -    -    -       -
    1 CPU0    2   -  1819     -  0.33 1.28    -   -      -     -     -     -    -    -       -
    1 CPU0    3   -  1672     -  0.41 0.27   31  74      - 1.175     -   0x0  0x0   0       -
    1 CPU0    3   -  1827     -  0.74 0.10    -   -      -     -     -     -    -    -       -
    1 CPU0    3   -  1518     -  0.08 0.16    -   -      -     -     -     -    -    -       -
    1 CPU0    4   -  1834     -  0.22 0.75   27  78      - 0.897     -   0x0  0x0   0       -
    1 CPU0    4   -  2102     -  0.40 0.45    -   -      -     -     -     -    -    -       -
    1 CPU0    4   -  1566     -  0.05 0.30    -   -      -     -     -     -    -    -       -
    1 CPU0    5   -  1897     -  0.32 0.96   27  78      - 0.902     -   0x0  0x0   0       -
    1 CPU0    5   -  1552     -  0.28 0.57    -   -      -     -     -     -    -    -       -
    1 CPU0    5   -  2241     -  0.35 0.40    -   -      -     -     -     -    -    -       -
    1 CPU0    6   -  1553     -  0.15 0.74   29  76      - 0.895     -   0x0  0x0   0       -
    1 CPU0    6   -  1487     -  0.23 0.43    -   -      -     -     -     -    -    -       -
    1 CPU0    6   -  1619     -  0.06 0.31    -   -      -     -     -     -    -    -       -
    1 CPU0    7   -  1968     -  0.35 1.70   28  77      - 0.902     -   0x0  0x0   0       -
    1 CPU0    7   -  1856     -  0.26 0.42    -   -      -     -     -     -    -    -       -
    1 CPU0    7   -  2080     -  0.45 1.27    -   -      -     -     -     -    -    -       -
    1 CPU0    8   -  1929     -  0.18 0.68   29  76      - 0.907     -   0x0  0x0   0       -
    1 CPU0    8   -  1680     -  0.17 0.19    -   -      -     -     -     -    -    -       -
    1 CPU0    8   -  2179     -  0.20 0.49    -   -      -     -     -     -    -    -       -
    1 CPU0    9   -  1431     -  0.64 0.93   25  80      - 0.915     -   0x0  0x0   0       -
    1 CPU0    9   -  1370     -  1.23 0.58    -   -      -     -     -     -    -    -       -
    1 CPU0    9   -  1492     -  0.06 0.35    -   -      -     -     -     -    -    -       -
    1 CPU0   10   -  1571     -  0.14 0.71   26  79      - 0.905     -   0x0  0x0   0       -
    1 CPU0   10   -  1551     -  0.25 0.31    -   -      -     -     -     -    -    -       -
```

- Run the Intel® PTAT Mon using filter to show memory data only:

```
> start /wait ptat.exe –mon –filter 0x30
```

```
Administrator: Command Prompt                                                    —  □  ×

CVS File Enabled:            No

[09/25/2019 14:29:38] No tests selected.
[09/25/2019 14:29:39] PTU Mon started.

Press <Ctrl-C> to stop PTU...

Index Device MC Ch S1     Read    Write  DDRT-Rd  DDRT-Wr  Temp  Power  TLog
    1 MEM0    -  -  -    105.4     20.6      0.0      0.0    22    0.0  0x0
    1 MEM0    0  0  -    105.4     20.6      0.0      0.0    22      -  0x0
    1 MEM0    0  0  0        -        -        -        -    22      -  0x0
    2 MEM0    -  -  -    140.5     23.9      0.0      0.0    22    0.0  0x0
    2 MEM0    0  0  -    140.5     23.9      0.0      0.0    22      -  0x0
    2 MEM0    0  0  0        -        -        -        -    22      -  0x0
    3 MEM0    -  -  -    127.2     21.7      0.0      0.0    22    0.0  0x0
    3 MEM0    0  0  -    127.2     21.7      0.0      0.0    22      -  0x0
    3 MEM0    0  0  0        -        -        -        -    22      -  0x0
    4 MEM0    -  -  -    130.7     20.9      0.0      0.0    22    0.0  0x0
    4 MEM0    0  0  -    130.7     20.9      0.0      0.0    22      -  0x0
    4 MEM0    0  0  0        -        -        -        -    22      -  0x0
    5 MEM0    -  -  -    159.6     27.7      0.0      0.0    22    0.0  0x0
    5 MEM0    0  0  -    159.6     27.7      0.0      0.0    22      -  0x0
    5 MEM0    0  0  0        -        -        -        -    22      -  0x0
    6 MEM0    -  -  -    149.9     25.7      0.0      0.0    22    0.0  0x0
    6 MEM0    0  0  -    149.9     25.7      0.0      0.0    22      -  0x0
    6 MEM0    0  0  0        -        -        -        -    22      -  0x0



<CC:\ptu>trl-C> pressed. Exiting...


[09/25/2019 14:29:47] PTU stopped.
```

Run the Intel® PTAT logger for one minute and save the files as CSV:

```
> start /wait ptat.exe -log –t 60 –csv
```

- Run the Intel® PTAT to show summary data and quit.

  ```
  > start /wait ptat.exe –s
  ```

Intel Confidential

5.2   Running the Test and Monitor in GUI Mode

5.2.1   Intel® PTAT Main Screen

The Intel® PTAT main dialog window consists of the following menus:

- File
- Tab Control View
- Test Menu Selections
- Start/Stop operation.

Once the Intel® PTAT GUI launches, the monitor tab view is displayed and the Intel® PTAT message window appears. Intel® PTAT must not be running during software or firmware upgrade.

Figure 5-1. Intel® PTAT GUI Main Screen

Figure 5-2. Intel® PTAT GUI Message Window

Document Number: 615177, Revision: 4.4

Intel Confidential

5.2.2 Intel® PTAT GUI Tabs

Navigate to the different sub-windows by clicking the tabs (under the menus). There is a total of five tabs available in Intel® PTAT: **Summary**, **Monitor**, **Graph**, **Data Log**, and **Turbo Check**.

Figure 5-3. Intel® PTAT Tabs
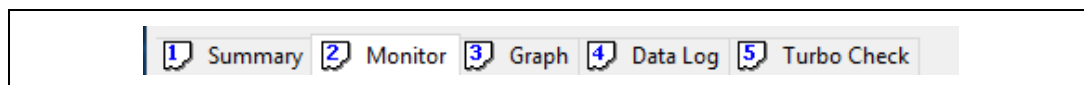
5.2.2.1 Summary Tab

The **Summary** tab shows the following groups: **System Info**, **Processor**, **Memory**, and **PCH**.

Figure 5-4. Intel® PTAT GUI Screen - Summary Tab View
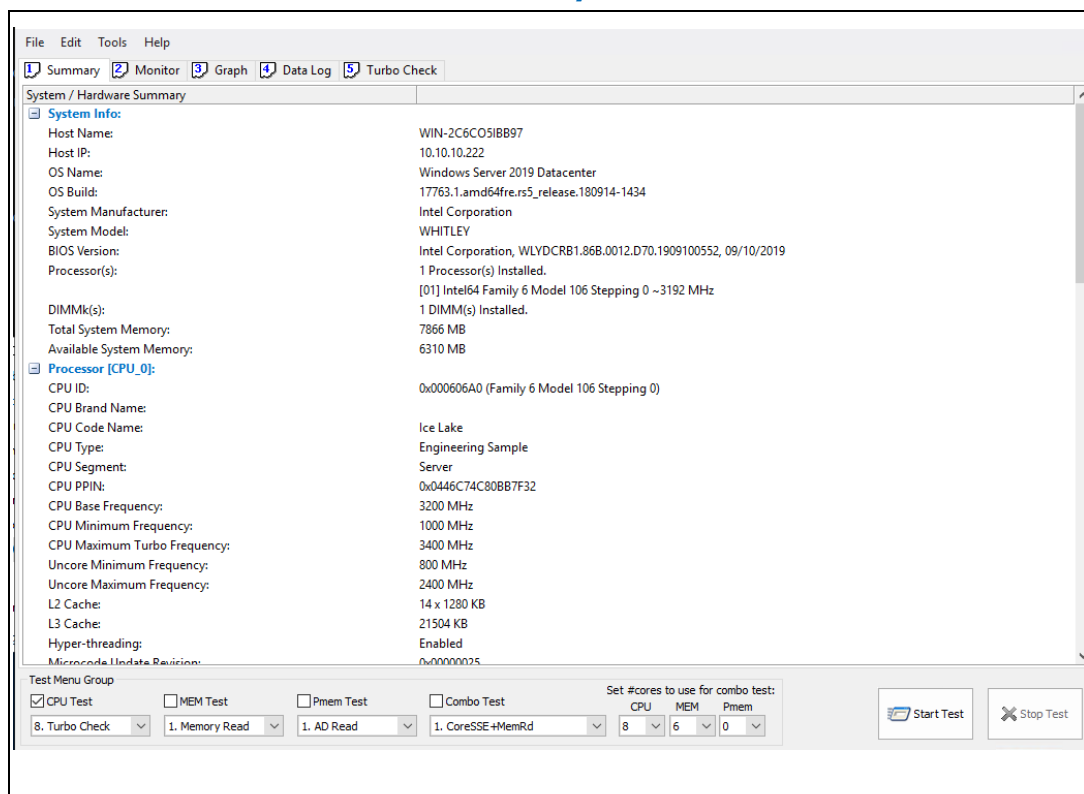
5.2.2.1.1 System Info

System Info shows information such as the Windows* OS version, the BIOS version, and the total installed memory.

Intel Confidential

5.2.2.1.2 Processor

Processor shows a list of the processors installed, and the CPU information such as CPUID, brand name, frequency, microcode version, TDP power, TProchot data, and turbo binning.

5.2.2.1.3 Memory

Memory shows a list of the installed DIMMs and the DIMM information such as DIMM speed, capacity, vendor information, and temperature threshold.

5.2.2.1.4 PCH

PCH shows a list of the installed PCHs and the PCH information such as the device ID, stepping, and CTRIP.

Note: The **Summary** tab information can be exported to a CSV file. Select **File →
Save HW Summary...** and a Dialog window will appear.
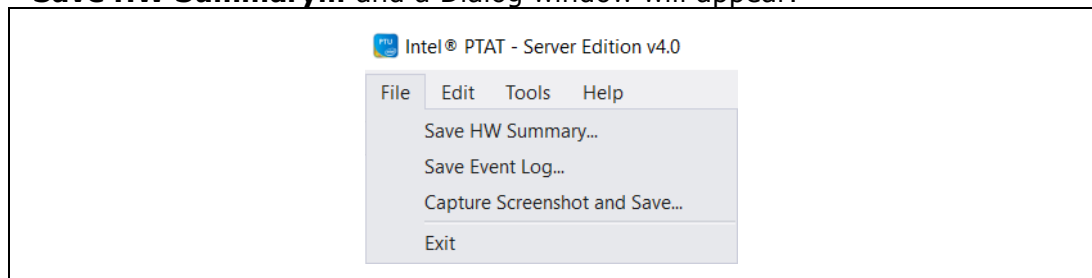
5.2.2.2 Monitor Tab

The **Monitor** tab shows real-time data of the CPU, memory, PCH, and the event log. In the bottom screen, it displays a list of core utilization in a graphical bar and the core usage percentage.

In the middle of the **Monitor** tab screen, there are four Excel*-like tabs, labeled as **Event**, **CPU**, **MEM**, and **PCH**.

Intel Confidential

Figure 5-5. Intel® PTAT GUI Screen - Monitor Tab View
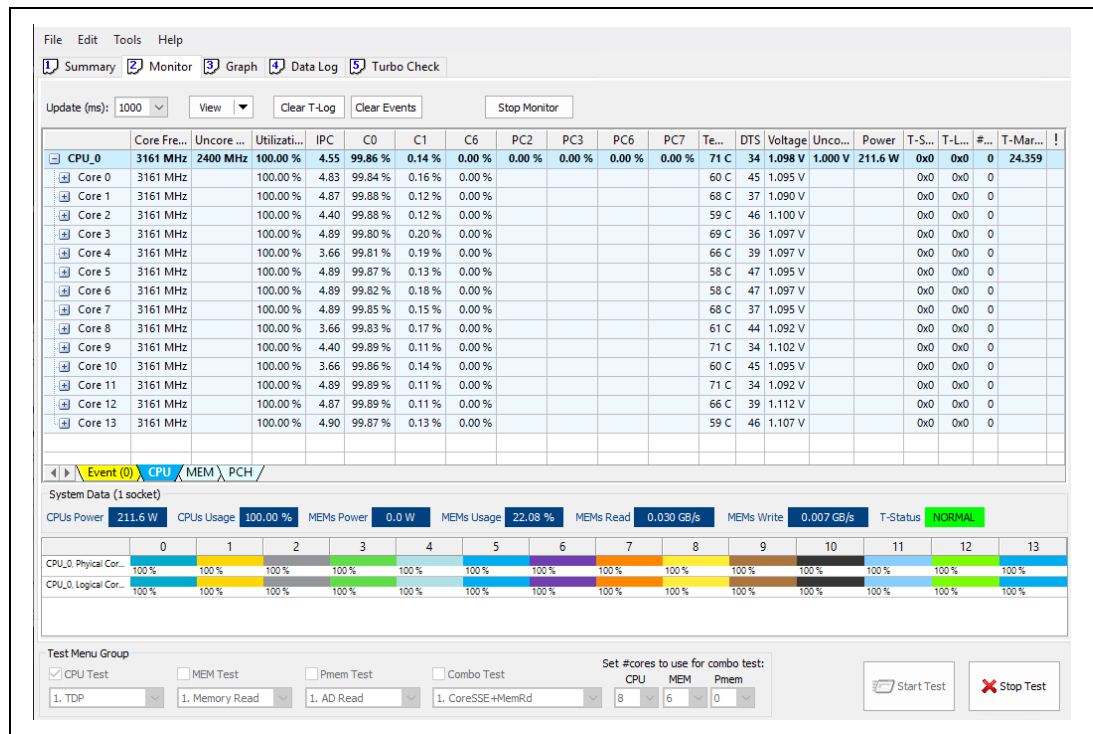
5.2.2.3 Monitor Tab - Event

The **Event** log holds a list of events that were triggered by the thermal status and thermal logs from the CPU and memory.

Figure 5-6. Monitor Tab - Event
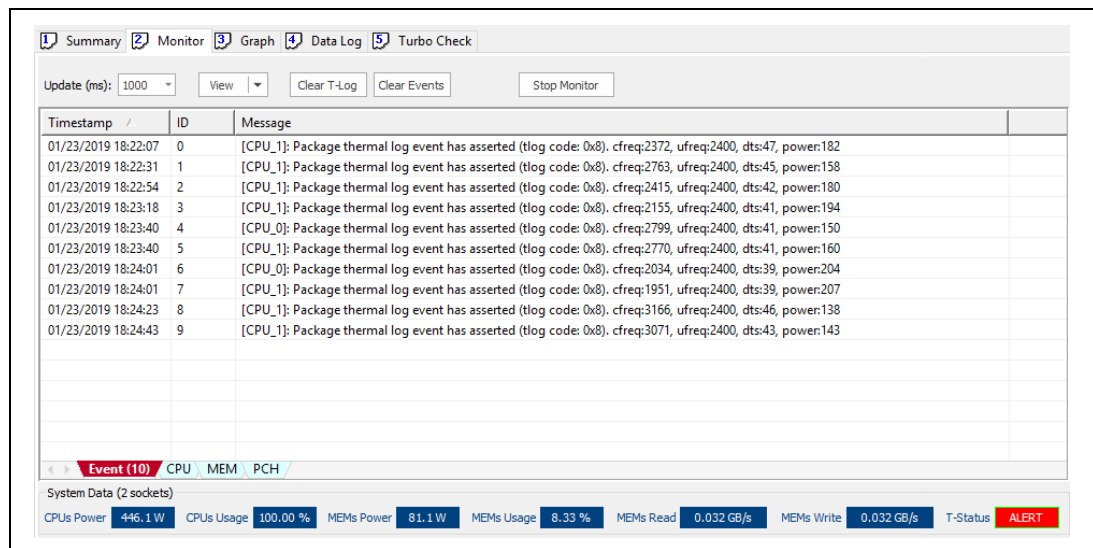
When there is an assertion from a thermal status or thermal log, that assertion is logged to the **Event** log along with the following information: Timestamp,

Intel Confidential

Event ID, and Messages. Some messages contain information such as the core frequency, the uncore frequency, the DTS, and power data.

5.2.2.4 Monitor Tab – CPU Monitoring

The CPU tab shows a list of relevant data of the all the processor sockets. The following subsections describe the information of each column field.

Figure 5-7. Monitor Tab - CPU

	Core Freq...	Uncore Fr...	Utilizati...	IPC	C0	C1	C6	PC2	PC6	Tem...	DTS	Voltage	Power	T-St...	T-Log	#TL	T-Margin	!
⊞ CPU_0	997 MHz	1200 MHz	1.01 %	0.14	1.01 %	2.26 %	95.95 %	0.00 %	0.00 %	28 C	70	0.700 V	28.2 W	0x0	0x0	0	59.656	
⊟ CPU_1	1005 MHz	1200 MHz	1.26 %	0.15	1.25 %	3.19 %	95.94 %	0.00 %	0.00 %	27 C	71	0.697 V	30.8 W	0x0	0x0	0	61.047	
C0, T0	1375 MHz		4.98 %	1.10	4.95 %	9.81 %	92.47 %			27 C	71	0.747 V		0x0	0x0	0		
C0, T1	1000 MHz		1.01 %	1.10										0x0	0x0	0		
C1, T0	997 MHz		1.77 %	0.61	0.98 %	13.78 %	95.37 %			25 C	73	0.695 V		0x0	0x0	0		
C1, T1	997 MHz		1.24 %	0.61										0x0	0x0	0		
C2, T0	997 MHz		1.28 %	0.11	1.77 %	1.98 %	95.96 %			25 C	73	0.683 V		0x0	0x0	0		
C2, T1	997 MHz		1.27 %	0.11										0x0	0x0	0		
C3, T0	997 MHz		1.26 %	0.07	1.22 %	2.53 %	96.15 %			25 C	73	0.695 V		0x0	0x0	0		
C3, T1	997 MHz		1.13 %	0.07										0x0	0x0	0		
C4, T0	997 MHz		1.17 %	0.13	1.25 %	2.44 %	95.92 %			25 C	73	0.695 V		0x0	0x0	0		
C4, T1	997 MHz		1.26 %	0.13										0x0	0x0	0		
C5, T0	997 MHz		1.26 %	0.07	1.24 %	2.44 %	96.20 %			25 C	73	0.688 V		0x0	0x0	0		
C5, T1	997 MHz		1.14 %	0.07										0x0	0x0	0		
C6, T0	997 MHz		1.19 %	0.07	1.24 %	2.46 %	96.19 %			26 C	72	0.694 V		0x0	0x0	0		
C6, T1	997 MHz		1.07 %	0.07														

Update (ms): 1000   View ▼   Clear T-Log   Clear Events   Stop Monitor

Event (0)   CPU   MEM   PCH

5.2.2.4.1 Device Column

The **Device** column shows a list of the processors and each core threads detected in the system. Clicking the plus icon ⊞ will expand the view of list of each core and thread data. On the other hand, the core and thread data will not be visible when collapsing with the minus icon ⊟ .

⊞ CPU_0
⊟ CPU_1
C0, T0
C0, T1
C1, T0
C1, T1
C2, T0
C2, T1
C3, T0
C3, T1
C4, T0
C4, T1
C5, T0
C5, T1
C6, T0
C6, T1

Note: For example, C0 represents the **Core 0** data, and T0 represents the **Thread 0** data.

Document Number: 615177, Revision: 4.4

Intel Confidential

5.2.2.4.2 Core Frequency Column

The **Core Frequency** column shows the current operating frequency of each core thread. The frequency value is in megahertz (MHz). The CPU line shows the average frequency of all core threads.

	Core Freq...	Uncore Fr...	Utilizati...	IPC	C0	C1	C6	PC2	PC6	Tem...	DTS	Voltage	Power	T-St...	T-Log	#TL	T-Margin	!
⊞ CPU_0	997 MHz	1200 MHz	1.09 %	0.10	1.10 %	2.85 %	96.10 %	0.00 %	0.00 %	30 C	68	0.698 V	28.3 W	0x0	0x0	0	57.859	

5.2.2.4.3 Uncore Frequency Column

The **Uncore Frequency** column shows the current Uncore operating frequency. The frequency value is in megahertz (MHz).

5.2.2.4.4 Utilization Column

The **Utilization** column shows the current core and threads' usage. The utilization value is in percentage. The CPU line shows the average utilization of all core threads.

5.2.2.4.5 IPC Column

The **IPC** column shows the average number of retired Instructions per Cycle (IPC). Each core and thread have their own IPC. The CPU line shows the average IPC of all core threads.

5.2.2.4.6 C-States (C0, C1, C6) Column

The **C-States** column shows the residency in each of the C-state as a percent of the total time. C-states are measured per core and the values are in percentage. The CPU line shows the average C-state of all cores.

5.2.2.4.7 Package C-States (PC2, PC3, PC6, PC7) Column

The **Package C-States** column shows the residency in each of the Package C-State as a percent of total time. Package C-States are measured per CPU package and the values are in percentage.

5.2.2.4.8 Temperature Column

The **Temperature** column shows the current die temperature in Celsius (°C) degrees. Each core has its own temperature. The CPU line shows the package temperature, which is the highest temperature of all cores.

5.2.2.4.9 DTS Column

The **DTS** column reports a relative distance to a fixed temperature (Tprochot). This value represents the maximum temperature of the package and cores. A value of "0" indicates that the PROCHOT# activation temperature has been reached. Each core has its own DTS. The CPU line shows the package DTS, which is the highest temperature of all cores.

5.2.2.4.10 Voltage Column

The **Voltage** column shows the current core P-state voltage. Each core has its own voltage. The CPU line shows the average voltage of all cores.

5.2.2.4.11 Uncore Voltage Column

The **Uncore Voltage** column shows the current uncore operating voltage.

5.2.2.4.12 Power Column

The **Power** column shows the current package power consumed of the CPU including the IA Core and the system agent.

5.2.2.4.13 T-Status Column

The **T-Status** column refers to as the Package and core thermal status, it tracks the package and core level temperature changes. The status is encapsulated in four status bits as shown as follows. Each core has its own status bits, except that Pmax status is package-level only. The CPU line shows the package thermal status. The value of this field is displayed in hexadecimal. When a value is greater than 0, the color of the text will display in red.

Note: All the bits are set and cleared by hardware.

Note: When the T-Status is asserted, an event of that status is logged with the timestamp in the **Event** log.

- Bit[0]: This bit indicates whether the thermal sensor high-temperature output signal (PROCHOT#) is currently active. A value of 0 indicates not active, and a value of 1 indicates active. This is better known as "Processor Thermal Throttle".

- Bit[1]: This bit indicates whether the PROCHOT# signal is being asserted. Active = 1; Inactive = 0.

- Bit[2]: When set, this bit indicates that the temperature has exceeded above the maximum operating temperature for 20 ms or more.

- Bit[3]: The status bit for the Pmax detector. An assertion means that the Pmax detector circuit has asserted (up to 1 ms delay). The status bit is deasserted when the core throttle is released to indicate that the Pmax condition has been dealt with.

5.2.2.4.14 T-Log Column

The **T-Log** column performs the same as the **T-Status** column, except that the T-log bits are cleared by the software. When the T-log bits are asserted by the hardware, the Intel® PTAT will store the bits into an internal buffer and clear the T-log (hardware) register.

Note: When the T-log bit is set, it will remain set unless the "Clear T-Log" button is pressed, in that case, all the bits will be zeroed out.

Note: When the T-log is asserted, an event of that status will be logged with the timestamp in the **Event** log.

5.2.2.4.15 #TL Column

The **#TL** column keeps track of how many T-logs were hit for each update.

5.2.2.4.16 T-Margin Column

The **T-Margin** column shows the average thermal margin above the TSpec value. When this value is negative, it indicates that the firmware must increase the fan speed. With a positive value, the firmware may decrease the fan speed. See the Processor Thermal DTS 2.0 specification for more details.

5.2.2.5 Monitor Tab – MEM Monitoring

The MEM tab shows a list of relevant data of the memory subsystem from all sockets. The following subsections describe the information of each column field.

Figure 5-8. Monitor Tab - MEM

5.2.2.5.1 Device Column

The **Device** column shows a list of the DIMMs detected in the system. Clicking the plus icon ⊞ will expand the view of list of DIMMs data. On the other hand, the individual DIMM data will not be visible when collapsing the minus icon ⊟ .

Intel Confidential

MC0 represents **Memory Controller 0**. There is a maximum of four memory controllers for Ice* Lake Server design.

CH0 represents **Memory Channel 0**. There is a maximum of eight channels for the Ice Lake Server design.

The numbering is in logical ordering.

SL0 represents **DIMM Slot 0**. There is a maximum of two DIMM slots for the Ice Lake Server design.

5.2.2.5.2 DIMM Speed Column

The **DIMM Speed Column** shows the DIMM operating frequency for that DIMM slot. The speed is displayed in megahertz (MHz).

5.2.2.5.3 DIMM Size Column

The **DIMM Size** column shows the DIMM capacity for that DIMM slot. The size is displayed in gigabytes (GB).

5.2.2.5.4 Temperature Column

The **Temperature** column shows the current DIMM temperature in Celsius (°C) degrees. Each DIMM has its own temperature. The MEM line shows the highest temperature of all DIMM slots.

5.2.2.5.5 Power Column

The **Power** column shows the current DIMM power consumed of all the DIMMs.

Note: If the PMem module is present, the DIMM power will include the 12V rail supplying to the DIMM controller.

Intel Confidential

5.2.2.5.6 Read Column

The **Read** column shows the current DDR4 memory read bandwidths of each memory channel. Each channel has its own bandwidth data. The MEM line shows the sum of all channels' bandwidth. The value is displayed in megabytes per second (MB/s).

5.2.2.5.7 Write Column

The **Write** column shows the current DDR4 memory write bandwidths of each memory channel. Each channel has its own bandwidth data. The MEM line shows the sum of all channels' bandwidth. The value is displayed in megabytes per second (MB/s).

5.2.2.5.8 DDR-T Read Column

The **DDR-T Read** column shows the current DDR-T read bandwidths of each PMem module. Each channel has its own bandwidth data. The MEM line shows the sum of all PMem modules bandwidth. The value is displayed in megabytes per second (MB/s).

5.2.2.5.9 DDR-T Write Column

The **DDR-T Write** column shows the current DDR-T write bandwidths of each PMem module. Each channel has its own bandwidth data. The MEM line shows the sum of all PMem modules bandwidth. The value is displayed in megabytes per second (MB/s).

5.2.2.5.10 T-Log Column

T-Log monitors the MEMHOT assertion events. The T-Log bit status is shown below:

- Bit[0]: This bit indicates the ev_asrt_templo event.
- Bit[1]: This bit indicates the ev_asrt_tempmid event.
- Bit[2]: This bit indicates the ev_asrt_temphi event.

5.2.2.6 Monitor Tab– PCH Monitoring

The PCH tab show list of relevant data of the platform controller hub from all sockets. The followings describe the data of each column field.

Intel Confidential
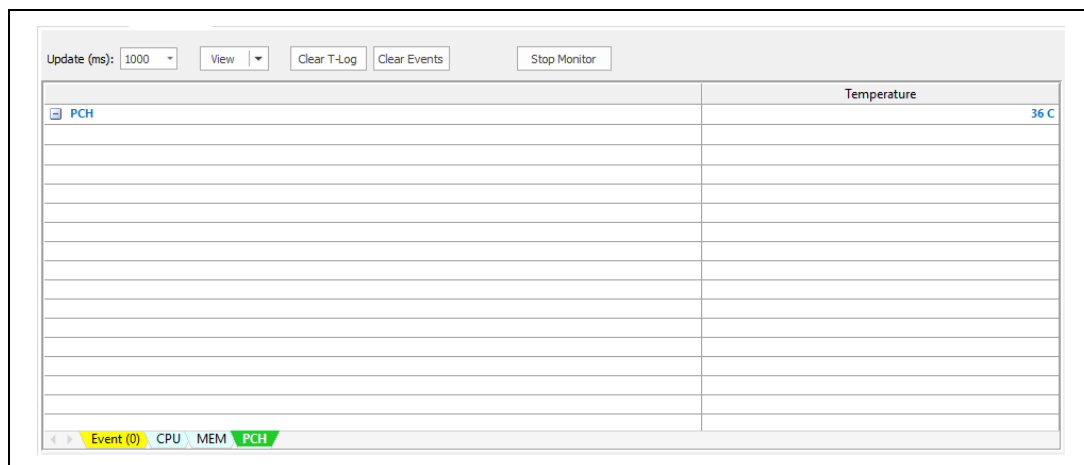
5.2.2.6.1 Device Column

The **Device** column shows one single PCH item. Clicking the plus icon ⊞ or icon ⊟ does not change anything.

5.2.2.6.2 Temperature Column

The **Temperature** column shows the current PCH temperature in Celsius (°C) degrees.

5.2.2.7 Monitor Tab – User Control

The upper screen of the **Monitor** tab provides user control settings such as changing the data update rate, changing the font size, clearing the thermal log, clearing the events, and switching the monitor on and off.

5.2.2.7.1 Update (ms)

By default, the **Monitor** data is updated each one second (1000 ms). The user can change the update rate from 10 ms to 5000 ms.

Intel Confidential

Figure 5-9. View Drop-Down Menu
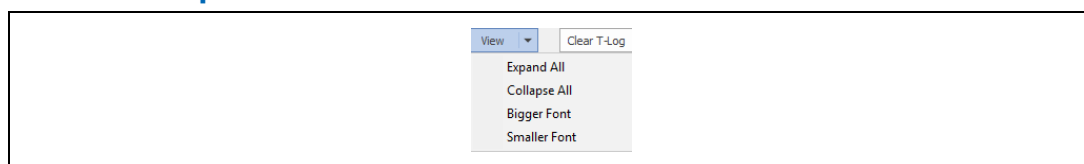
The user can select **Expand All** and **Collapse All** to maximize and minimize the core and thread data or the memory per channel or memory per slot data. In addition, the user can change the font size to bigger or smaller in the monitoring data list screen and the core usage bar screen.

- Clear T-Log Button: Clicking the "Clear T-Log" button will clear all the T-log status and the #TL.

- Clear Events Button: Clicking the "Clear Events" button will clear all the events in the Event log.

- Start/Stop Monitor Button: By default, the monitor is running with 1000 ms update rate when the Intel® PTAT is invoked. By clicking the "Stop Monitor" button, the monitor stops updating the data and the **Event** log does not run.

5.2.2.8 Monitor Tab – System Data

The middle bottom screen of the monitor tab provides system data in real time such as CPUs power, CPUs usage, MEMs power, and MEMs bandwidth from all sockets. In addition, the T-Status indicator helps to quickly see whether the system is running in a normal or abnormal status.

Figure 5-10. Monitor Tab – System Data
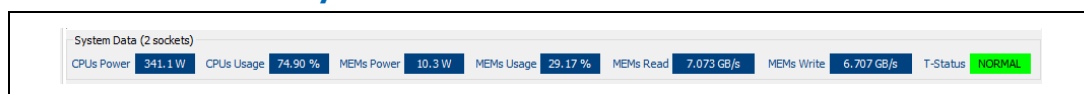
5.2.2.8.1 CPUs Power

The **CPUs Power** box shows the current CPU power from all sockets. The value is the sum of all CPUs power and is displayed in watts (W).

5.2.2.8.2 CPUs Usage

The **CPUs Usage** box shows the current CPU utilization from all sockets. The value is the average utilization of all CPUs and is displayed in percentage.

5.2.2.8.3 MEMs Power

The **MEMs Power** box shows the current DIMM power from all sockets. The value is the sum of all DIMMs power and is displayed in watts (W).

5.2.2.8.4 MEMs Usage

The **MEMs Usage** box shows the total system memory usage. The value is displayed in percentage.

5.2.2.8.5 MEMs Read

The **MEMs Read** box shows the total memory read bandwidths from all sockets. The read bandwidth includes the DDR4 and DDR-T access. The value is displayed in gigabytes per second (GB/s).

5.2.2.8.6 MEMs Write

The **MEMs Write** box shows the total memory write bandwidths from all sockets. The write bandwidth includes the DDR4 and DDR-T access. The value is displayed in gigabytes per second (GB/s).

5.2.2.8.7 T-Status

The **T-Status** box shows "NORMAL" if no thermal events are asserted. Otherwise, it will show "ALERT" when there is a thermal event asserted and it will change the box to RED color.

Figure 5-11. Monitor Tab – System Data Alert
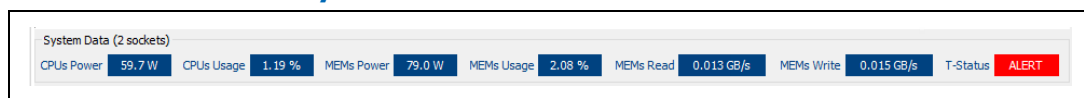
5.2.2.9 Monitor Tab – CPU Usage Bar

The bottom screen of the monitor tab displays the average CPU utilization in percentage, along with the graphical bar indication. The first row contains the physical cores data, and the second row contains the logical cores (for Intel® HT Technology-enabled CPUs).

Figure 5-12. Monitor Tab - CPU
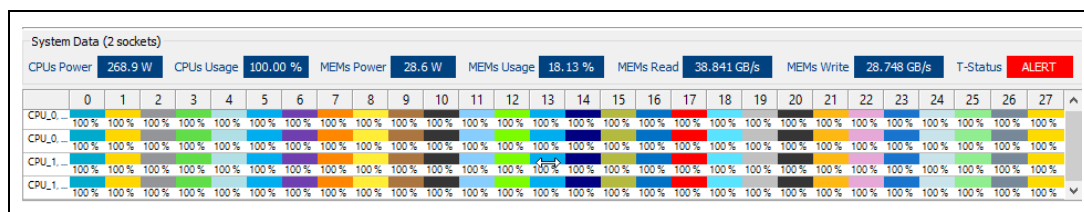
5.2.2.10 Graph Tab

The **Graph** tab shows real-time graphical line data of the CPU and memory. Within the main graph window, there are multiple graphs, and they can be accessed using Excel*-like tabs in the bottom of the window. Each CPU and MEM has its own tab.

Intel Confidential

The user can use the mouse wheel to zoom in and out of the graph.

By default, the graph will hold 20,000,000 samples. When the maximum number of samples has reached, it will erase all the records and restart with sample 0.

Figure 5-13. Intel® PTAT GUI Screen with Graph Tab View
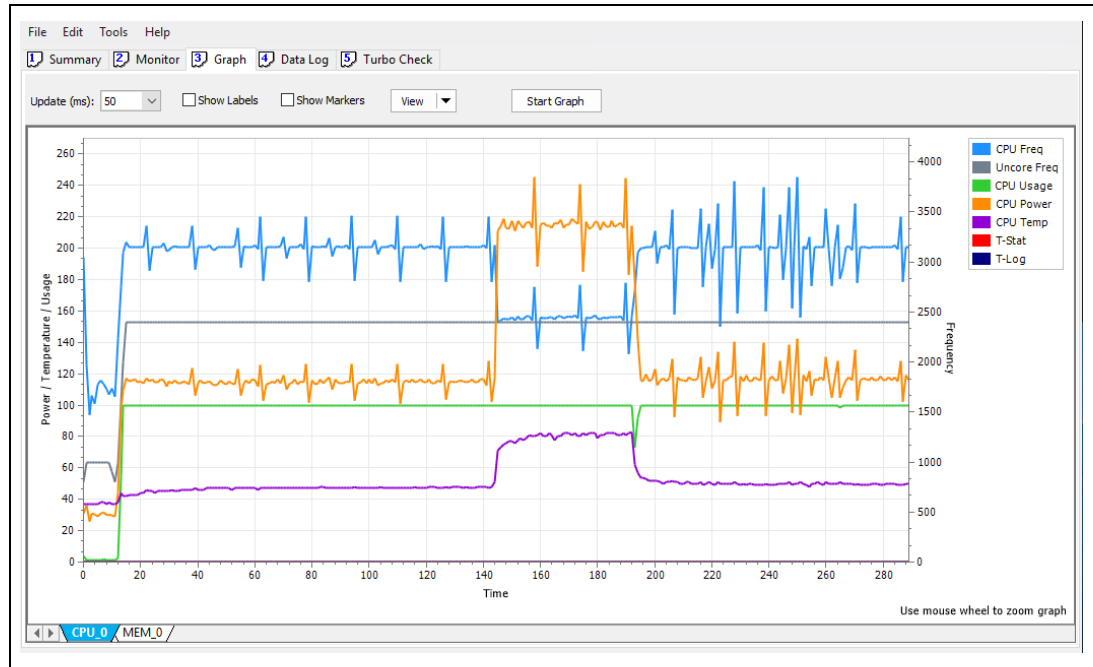
5.2.2.11 Graph Tab – CPU Graph

The CPU graph provides the following graphical line data:
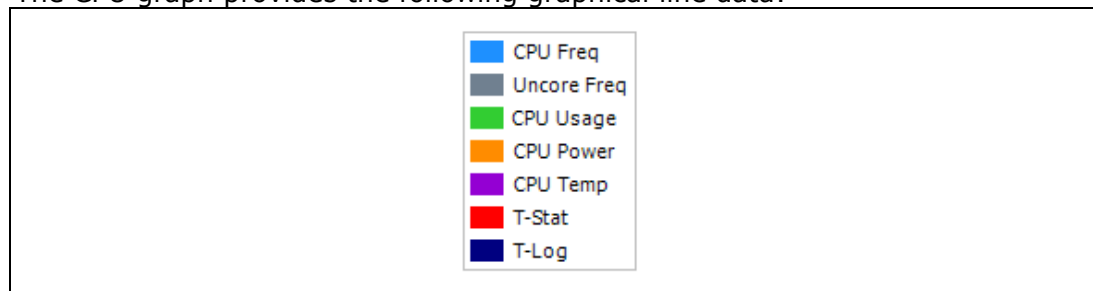
- CPU Freq: Average frequency of all cores
- Uncore Freq: Uncore frequency, also known as CLM frequency
- CPU Usage: Average utilization of all cores
- CPU Power: CPU package power
- CPU Temp: CPU package temperature
- T-Stat: Thermal status
- T-Log: Thermal log

Intel Confidential

Note: The frequency scale is in the secondary Y axis (right hand side).

Note: For readability purposes, the actual T-Stat value is multiplied by 30 and the T-log value is multiplied by 60.

Figure 5-14. Graph Tab – CPU Graph
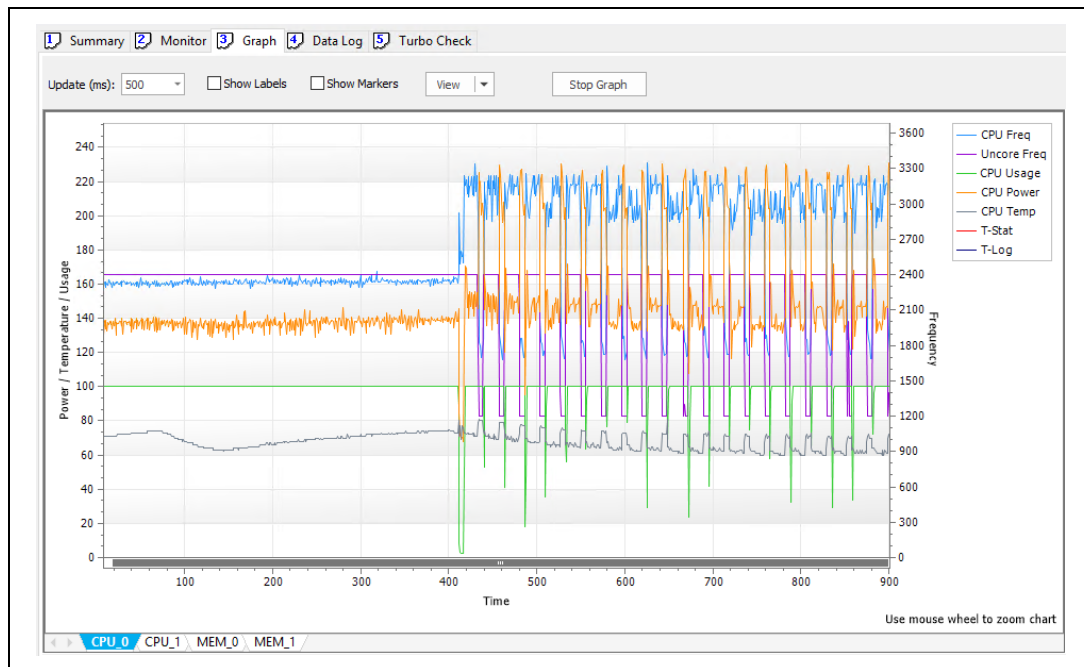
5.2.2.12 Graph Tab – MEM Graph

The MEM graph provides the following graphical line data:
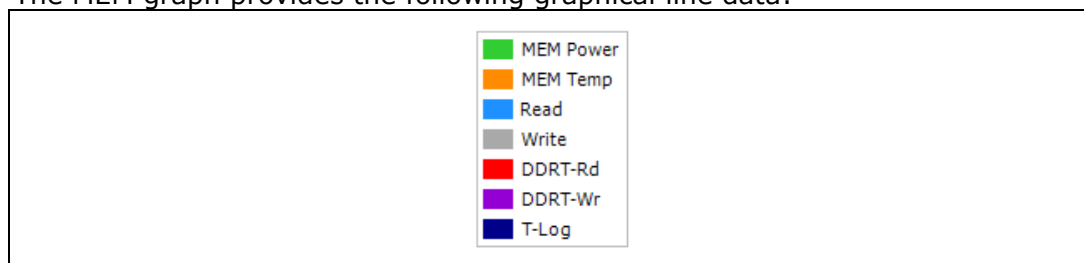
- MEM Power: Total memory power of this socket
- MEM Temp: Highest temperature of all DIMMs
- Read: Total DDR4 memory read bandwidths
- Write: Total DDR4 memory write bandwidths
- DDRT-Rd: Total DDR-T memory read bandwidths
- DDRT-Wr: Total DDR-T memory write bandwidths
- T-Log: Thermal log

Note: For readability purposes, the actual T-Log value is multiplied by 60.

Document Number: 615177, Revision: 4.4

Intel Confidential

Figure 5-15. Graph Tab – MEM Graph
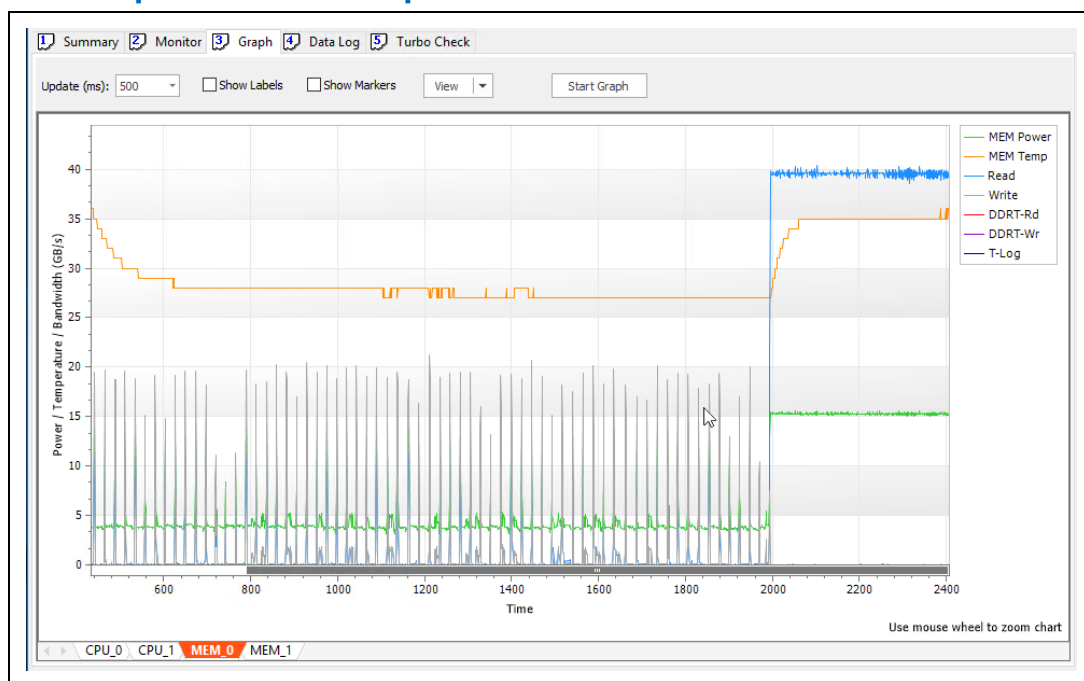
5.2.2.13 Graph Tab – User Control

The upper screen of the **Graph** tab provides user control settings such as changing the data update rate, enabling the labels and markers, resetting the graph data, and switching the graph on and off.

Figure 5-16. Graph Tab – User Control

Intel Confidential
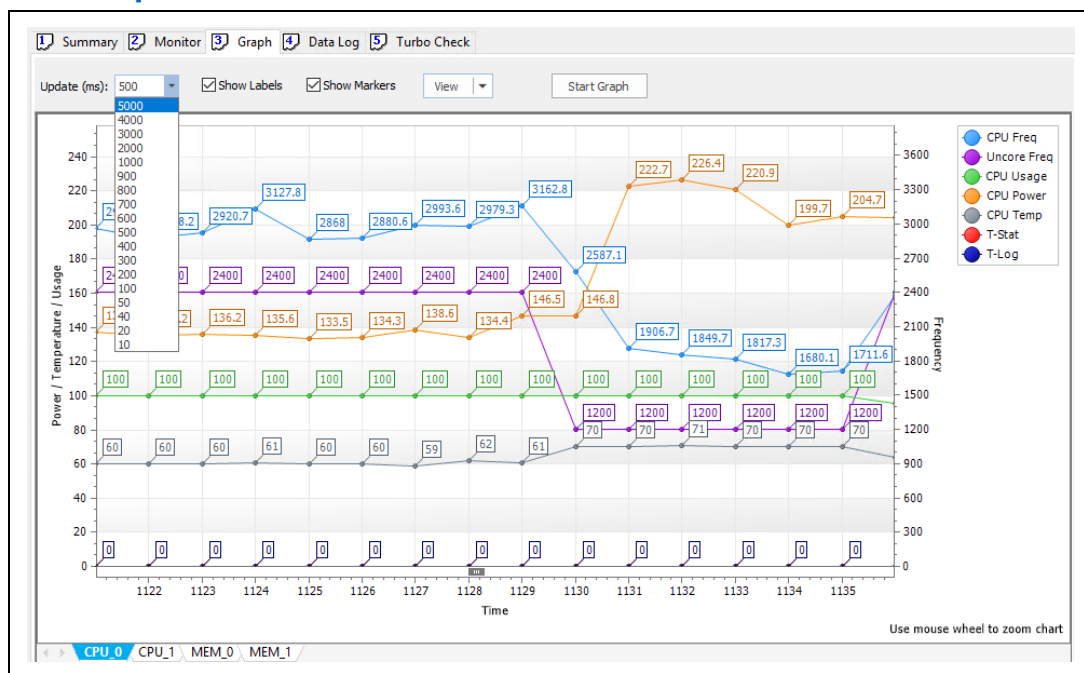
5.2.2.13.1 Update (ms)

By default, the **Graph** data is updated in one second (1000 ms). The user can change the update rate from 10 ms to 5000 ms.

5.2.2.13.2 Show Labels

Checking "Show Labels" will display the numeric value of each data point.

5.2.2.13.3 Show Markers

Checking "Show Markers" will display a solid circle of each data point.

5.2.2.13.4 View Drop-Down Menu
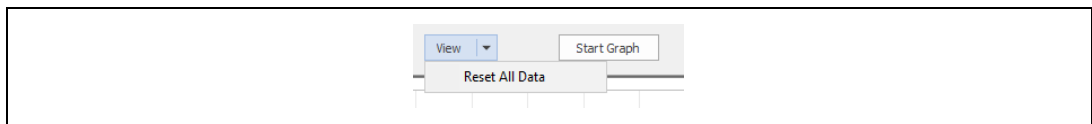
The user can select "Reset All Data" to erase all the data shown in the graph window.

5.2.2.13.5 Start and Stop Graph Button

By default, the graph is not running when the Intel® PTAT is invoked. Clicking the "Start Graph" button, the graph will start updating the data with the selected update rate.

5.2.2.14 Data Log Tab

The **Data Log** tab provides the ability to capture the data in a buffer list and later export it to a file. All the CPUs data is captured into one log and all MEMs data is stored in a separated window (Excel*-like tab).

The user can select two different levels to capture data.

The user can save the log as a CSV formatted file or a plain text (.txt) file.

Note: The oldest entries are shown at the bottom of list.

Intel Confidential

Figure 5-17. Data Log View
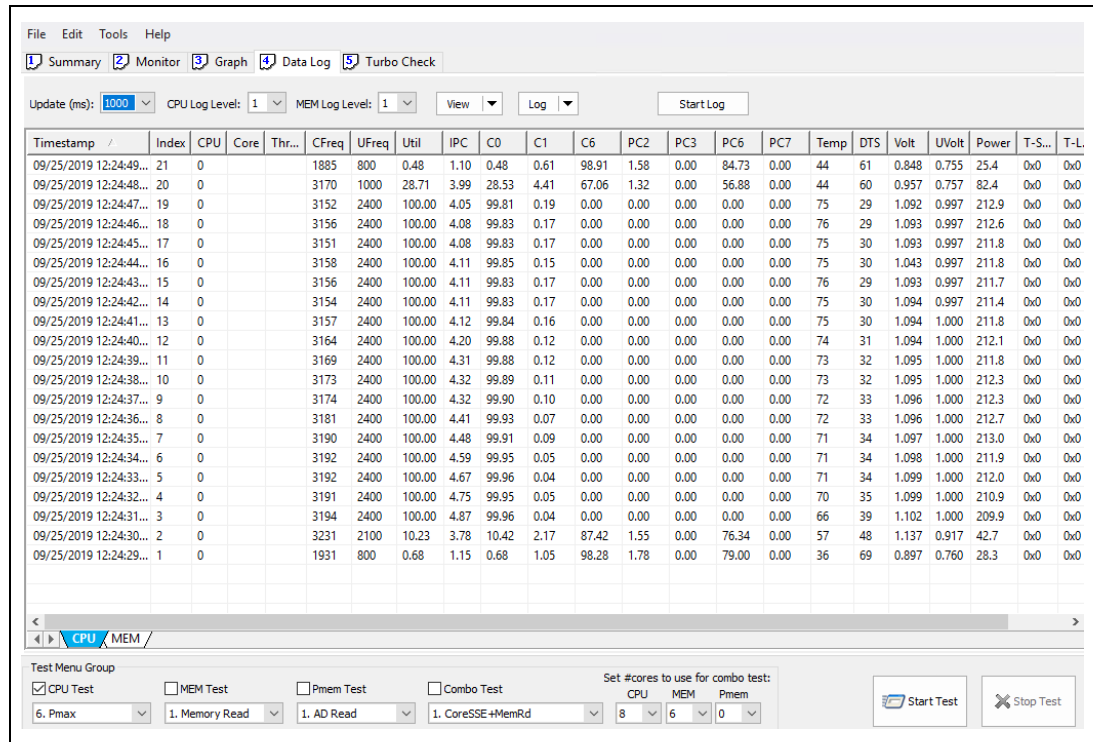
5.2.2.15 Data Log Tab – CPU Log

The CPU **Data Log** tab keeps track of the related data. The data fields are described in Figure 5-18.

Figure 5-18. Data Log – CPU Log

Intel Confidential
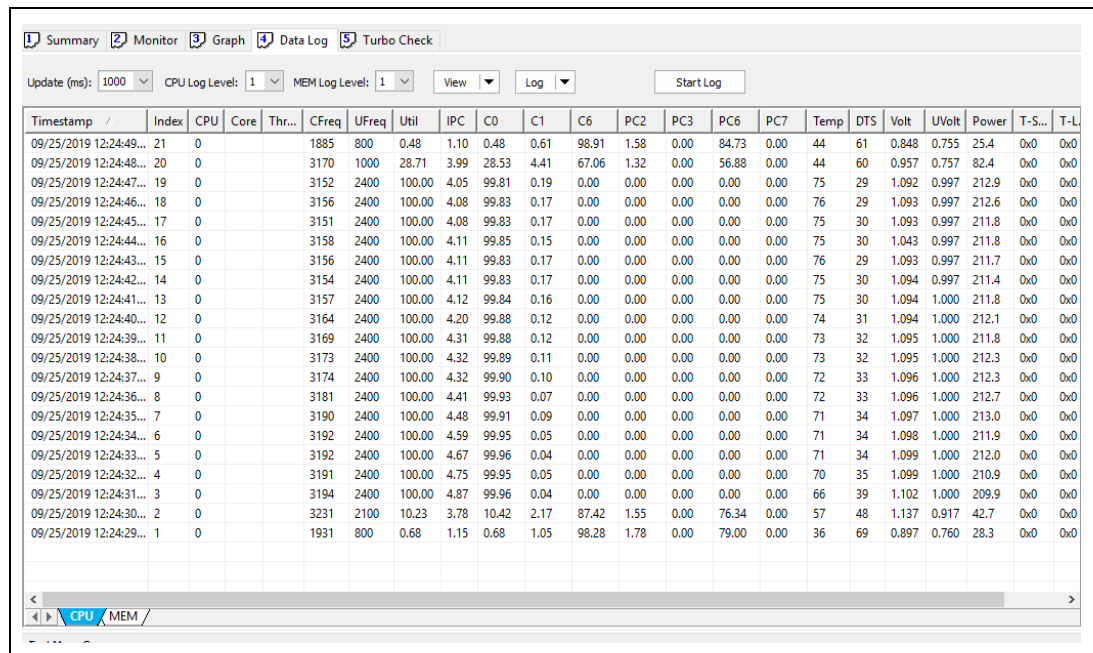
- Timestamp: Date and time values (MM/DD/YYYY hh:mm:ss.ms)

- Index: The index number of this record

- CPU: The CPU number.

- Core: The core number (**Level 2**-log only)
  Data Log → CPU Log Level: Select **2**

- Thread: Thread number (**Level 3**-log only)
  Data Log → CPU Log Level: Select **3**
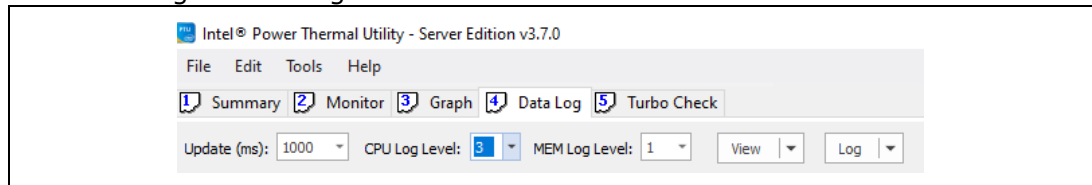
- CFreq: The CPU average frequency of all core threads/Core thread frequency (megahertz)

- UFreq: The uncore frequency (megahertz)

- Util: The CPU average utilization/Core thread utilization (percentage)

- IPC: The CPU average IPC of all cores/Core thread IPC

- C0: The CPU average C-State 0 of all cores/Core C0 (percentage)

- C1: The CPU average C-State 1 of all cores/Core C1 (percentage)

- C6: The CPU average C-State 6 of all cores/Core C6 (percentage)

- PC2: The CPU average Package C-State 2 (percentage)

- PC3: The CPU average Package C-State 3 (percentage)

- PC6: The CPU average Package C-State 6 (percentage)

- PC7: The CPU average Package C-State 7 (percentage)

- Temp: The CPU package temperature/Core temperature

- DTS: CPU package DTS or core DTS

- Volt: The CPU average voltage of all cores /Core voltage

- Power: The CPU package power (wattage)

- T-Stat: The thermal status (package/core level)

- T-Log: The thermal Log (package/core level)

- T-Margin: The thermal Margin (package level)

5.2.2.16 Data Log Tab – MEM Log

The **MEM Data** log keeps track of the memory-related data. The following figure describes the data fields.

Intel Confidential

Figure 5-19. Data Log View

- Timestamp: Date and time values (MM/DD/YYYY hh:mm:ss.ms)

- Index: The index number of this record

- MEM: The MEM number (memory socket)

- MC: Memory Controller number (Level 2-log only)

- Chnl: The memory channel number (Level 2-log only)

- Slot: The DIMM slot number (Level 2-log only)

- Temp: The DIMM highest temperature of all DIMMs/Single DIMM temperature

- Power: The total DIMMs power (wattage)

- Read: The total DDR4 memory read bandwidths

- Write: the total DDR4 memory write bandwidths

- DDRT-Rd: The total DDR-T memory read bandwidths

- DDRT-Wr: The total DDR-T memory write bandwidths

- T-Log: The thermal log (tempLo, tempMid, tempHi)

5.2.2.17 Data Log Tab – User Control

The upper screen of the **Data Log** tab provides user control settings such as changing the data update rate, changing the CPU and MEM log levels, resetting columns, configuring log options, and switching the data log on and off.

Intel Confidential

Figure 5-20. Data Log View – User Control
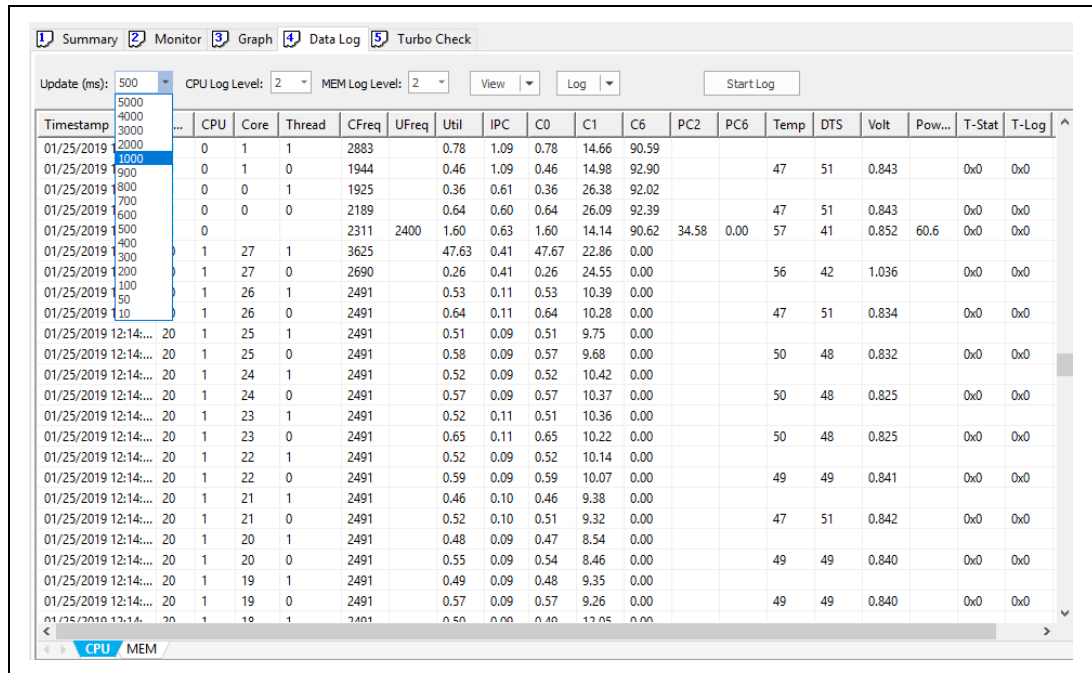
5.2.2.17.1 Update (ms)

By default, **Data Log** data is updated in one second (1000 ms). The user can change the update rate from 10 ms to 5000 ms.

5.2.2.17.2 CPU Log Level

By default, **Data Log** uses the CPU log Level 1. For Level 1 logging, only the CPU package level data is logged. For Level 2 logging, further breakdown of core and thread data will be logged.

5.2.2.17.3 MEM Log Level

By default, **Data Log** uses the MEM log level 1. For Level 1 logging, only the MEM socket level data are logged. For Level 2 logging, further breakdown of memory channel and DIMM slot data will be logged.

5.2.2.17.4 View Drop-Down Menu
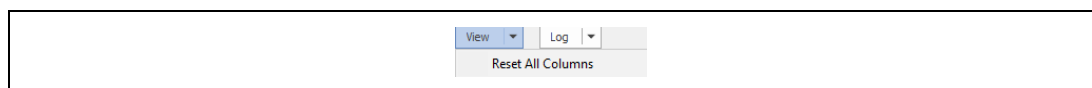
The user can resize the columns width across evenly by selecting "Reset All Columns".

Intel Confidential

5.2.2.17.5 Log Drop-Down Menu
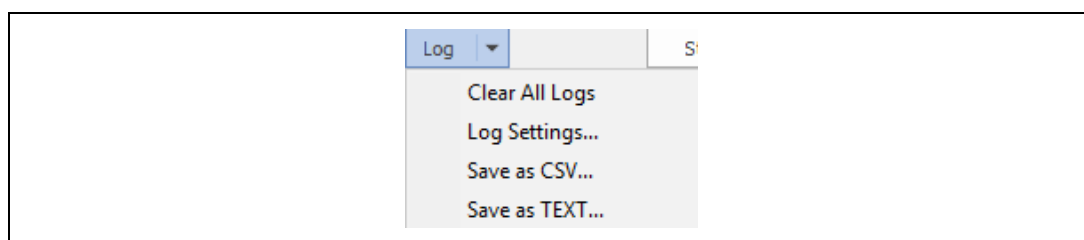
Clicking the **Log** down arrow will bring up a list of menus.

5.2.2.17.6 Clear All Logs Menu

Selecting this option will clear all the data in both CPU and MEM lists.

5.2.2.17.7 Start/Stop Log Button

By default, the **Data Log** is not running when the Intel® PTAT is invoked. By clicking the "Start Log" button, the log will start updating the data with the selected update rate.

5.2.2.17.8 Log Settings… Menu

Selecting this option will bring up the "PTAT Log Settings" dialog box:
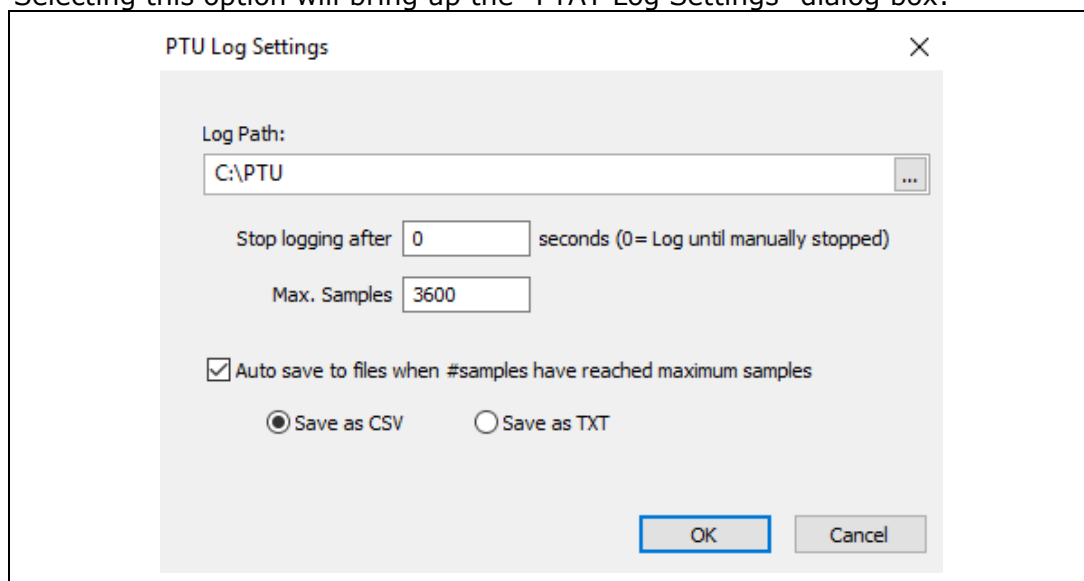
By default, the Log Path is set to "C:\PTAT". The user can change to another log path by either typing into the edit box field or click the "…" button to open the browse directory dialog box to choose the path.

The user can specify how long the logging should run, by changing the "Stop logging after" field. The default is 0, which means that the log will run forever until the "Stop Log" button is pressed.

The maximum number of samples or records to save the log in the buffer list is 3600. After the 3600-sample limit has been reached, both CPU and MEM lists will be cleared and restart with new data.

The **Auto Save** feature allows the log in the buffer list to save into files automatically when the maximum number of samples has been reached. By default, this item is enabled.

The user can choose whether the log will be saved in a CSV-formatted file or a plain text file (.txt).

5.2.2.17.9 Save as CSV... Menu

Selecting this option will save both CPU and MEM logs into a CSV-formatted file, and the files will be stored in the "Log Path" specified in the log settings.

5.2.2.17.10 Save as Text File... Menu

Selecting this option will save both CPU and MEM logs into a CSV-formatted file, and the files will be stored in the "Log Path" specified in the log settings.

Note: By default, log files are stored in the "C:\PTAT" folder. The saved files are:

- **<timestamp>_ptatlog**.csv (or .txt): This file contains information about the Intel® PTAT program and how the command was invoked.

Intel Confidential

Figure 5-21 Sample of the Intel® PTAT Main Log File
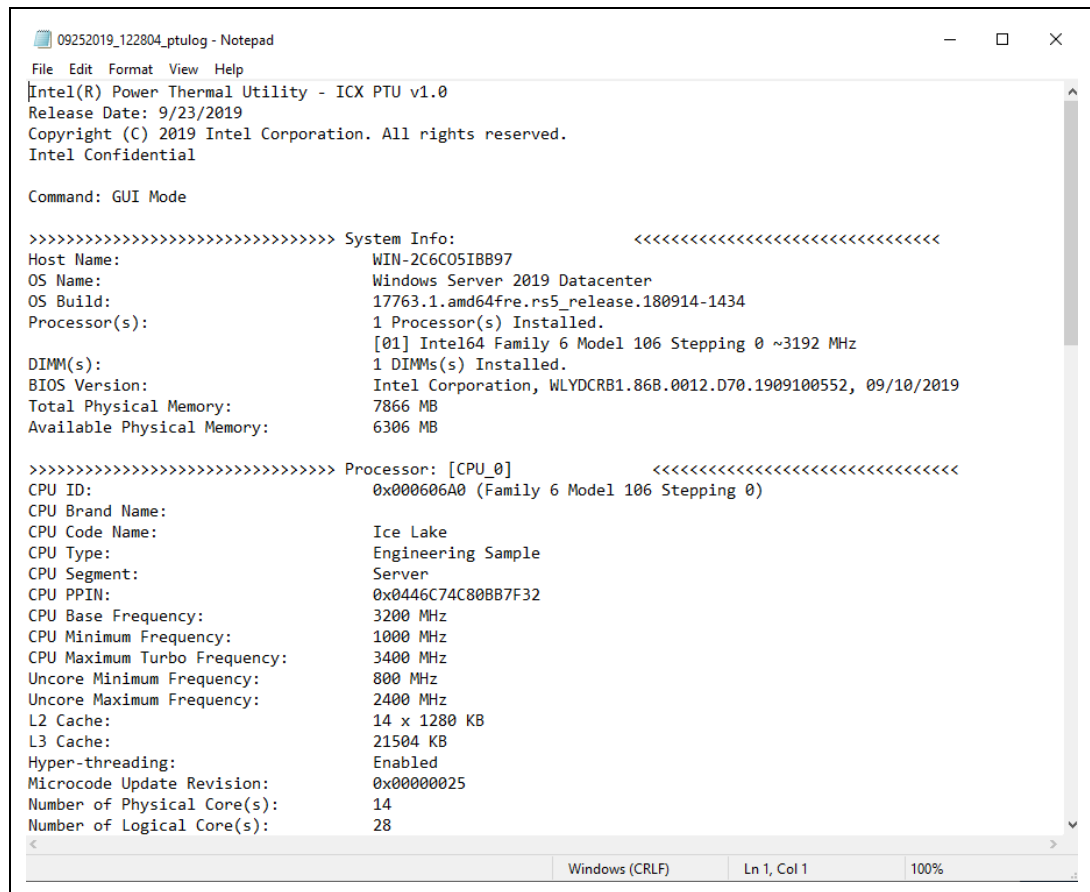
- **<timestamp>_ptatlog_cpu**.csv (or .txt): This file contains information about the CPU data from all sockets.

Figure 5-22 Sample of the CPU Log File.

- **<timestamp>_ptatlog_mem**.csv (or .txt): This file contains information about the MEM data from all sockets.

Figure 5-23 Sample of the MEM Log File

	A	B	C	D	E	F	G	H	I	J	K	L	M
1	Timestam	Index	MEM	MC	Chnl	Slot	Temp	Power	Read	Write	DDRT-Rd	DDRT-Wr	T-Log
2	24:29.2	1	0				23	0	222.5	33.2	0	0	0x0
3	24:30.2	2	0				23	0	429	211.9	0	0	0x0
4	24:31.2	3	0				23	0	65.2	21.5	0	0	0x0
5	24:32.2	4	0				23	0	40.9	9.6	0	0	0x0
6	24:33.2	5	0				24	0	36.1	8.3	0	0	0x0
7	24:34.2	6	0				24	0	35.2	7.8	0	0	0x0
8	24:35.2	7	0				24	0	45	10.6	0	0	0x0
9	24:36.3	8	0				24	0	35.3	8.6	0	0	0x0
10	24:37.3	9	0				24	0	34.9	7.4	0	0	0x0
11	24:38.3	10	0				24	0	34.6	7.3	0	0	0x0
12	24:39.3	11	0				24	0	29.8	6.8	0	0	0x0
13	24:40.3	12	0				24	0	29	6.5	0	0	0x0
14	24:41.3	13	0				24	0	29.6	6.6	0	0	0x0
15	24:42.3	14	0				24	0	33.1	7.8	0	0	0x0
16	24:43.3	15	0				24	0	34.3	8	0	0	0x0
17	24:44.3	16	0				24	0	30.3	7.1	0	0	0x0
18	24:45.3	17	0				24	0	28.3	6.5	0	0	0x0
19	24:46.4	18	0				24	0	30	7.2	0	0	0x0
20	24:47.4	19	0				24	0	33.2	7.7	0	0	0x0
21	24:48.8	20	0				24	0	124.6	171	0	0	0x0
22	24:49.4	21	0				24	0	159.9	29.1	0	0	0x0
23													
24													
25													
26													

5.2.2.18 Turbo Check Tab

The **Turbo Check** tab contains the results after the turbo check test ran. There are three Excel*-like tabs in the main window: IA/Intel® SSE, Intel® AVX2, and Intel® AVX-512.

When the turbo check is run, it will cycle through all the three tabs and fill in the data for each test run.

Document Number: 615177, Revision: 4.4

Intel Confidential

Figure 5-24. Turbo Check Tab

The list stores the following result columns:

- Instr: This column shows the type of CPU instructions being run.

- CPU: This column shows the CPU number. If there is more than one socket in the system, the run will start with CPU number 0, followed by CPU number 1, and so on.

- #Cores: This column shows the number of active cores being run.

- CFreq (Act): This column shows the actual (average) frequency read of #cores are active.

- CFreq (Exp): This column shows the expected frequency (from the Resolved/Fused data) of the active number of cores.

- UFreq: This column shows the current uncore frequency when the test is run.

- Util (Act): This column shows the actual CPU utilization of the active number of cores.

- Util (Exp): This column shows the expected CPU utilization of the active number of cores.

Note: If %Util (Act) is much higher than the %Util (Exp), this indicates that some other background processes or applications were running at the same time when the turbo test is run. For best results, stop all other processes when the turbo check is being executed.

- Power: This column shows the CPU power consumed of the entire package.

Intel Confidential

- TDP: This column shows the TDP power of this CPU.
- Temp: This column shows the CPU package temperature of the active number of cores.
- Volt: This column shows the CPU average voltage of the active number of cores.

5.2.2.19 Turbo Check Tab – IA/Intel® SSE Turbo

This screen shows the results of the IA/Intel® SSE turbo check. IA/Intel® SSE is similar to the Intel® AVX 128 light workload.

Figure 5-25. Turbo Check Tab – IA/Intel® SSE

5.2.2.20 Turbo Check Tab – Intel® AVX2 Turbo

This screen shows the results of the Intel® AVX2 turbo check. Intel® AVX2 uses Intel® AVX 256 instruction sets to generate the Intel® AVX2 light workloads.

Document Number: 615177, Revision: 4.4

Intel Confidential

Figure 5-26. Turbo Check Tab – Intel® AVX2

5.2.2.21 Turbo Check Tab – Intel® AVX-512 Turbo

This screen shows the results of the Intel® AVX-512 turbo check. Intel® AVX-512 uses Intel® AVX-512 instruction sets to generate the Intel® AVX-512 light workloads.

Figure 5-27. Turbo Check Tab – Intel® AVX-512

Intel Confidential

5.2.2.22 Turbo Check Tab – User Control

The upper screen of the **Turbo Check** tab provides user control settings such as changing the type of runs, selecting the active cores, and saving the data to a file.

Figure 5-28. Turbo Check Tab – User Control

5.2.2.22.1 Select Run

There are four options in the list to choose. By default, "Check All" is selected.

- Run All: IA/Intel® SSE, Intel® AVX2, and Intel® AVX-512 instructions are performed.
- IA/Intel® SSE: Only IA/Intel® SSE instructions will be performed.
- AVX2: Only Intel® AVX2 instructions are performed.
- AVX-512: Only Intel® AVX-512 instructions are performed.

5.2.2.22.2 Export to File… Button

Clicking the "Export" button brings up a "Save File" dialog window and allows the user to choose a folder to save the turbo check list data from all tabs to a file using a CSV format.

Figure 5-29. Turbo Check Export to File...
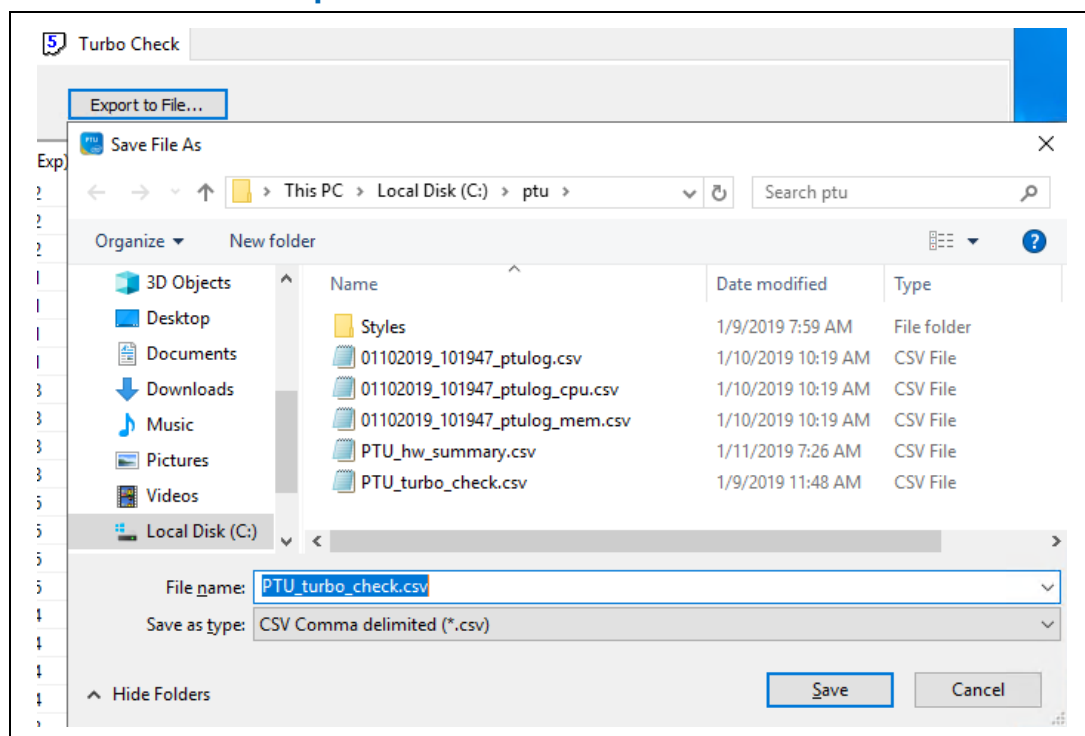
5.2.3 Intel® PTAT Groups

5.2.3.1 Test Menu Group

The **Test Menu** group is shown in the bottom of the Intel® PTAT GUI main screen. The test menu is grouped as □CPU Test , □MEM Test , □Pmem Test and □Combo Test .
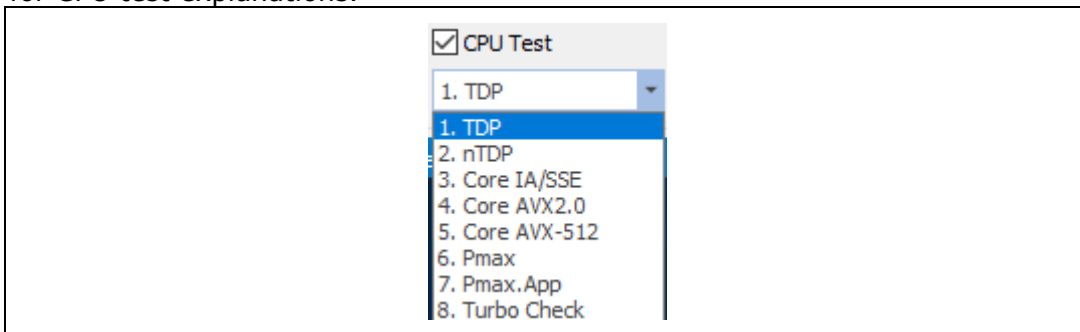
Figure 5-30. Test Menu Group
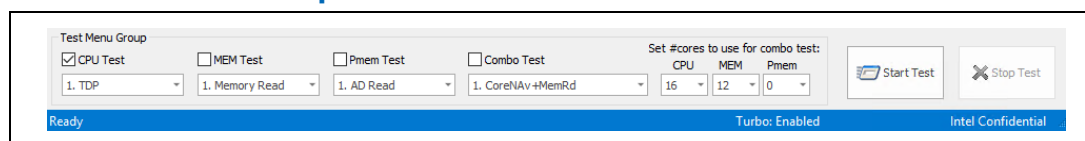
Checking the check box in the test group enables the test run of that group. The CPU test, the MEM test, and the PMem test can be selected to run individually or together. When "Combo Test" is selected, all other test groups are unchecked. On the other hand, if the CPU/MEM/PMem test group is checked, the combo check is unchecked.

Intel Confidential

5.2.3.2 CPU Test Group
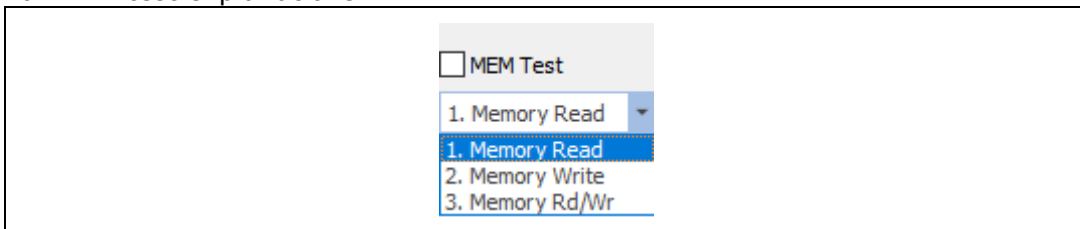
The **CPU Test** group consists of eight tests. See Intel® PTAT Tests Description for CPU test explanations.

Note - SRF (Sierra Forrest) – Intel ATOM based CPU does not support all core features listed above. It supports only subset of the feature.
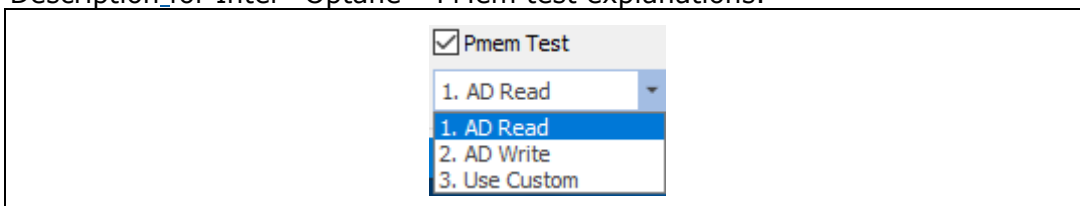
5.2.3.3 MEM Test Group

The **MEM Test** group consists of four tests. See Intel® PTAT Tests Description for MEM test explanations.

5.2.3.4 PMem Test Group

The **PMem Test** group consists of three tests. See Intel® PTAT Tests Description for Intel® Optane™ PMem test explanations.

5.2.3.5 Combo Test Group

The **Combo Test** group consists of eight tests.

Intel Confidential
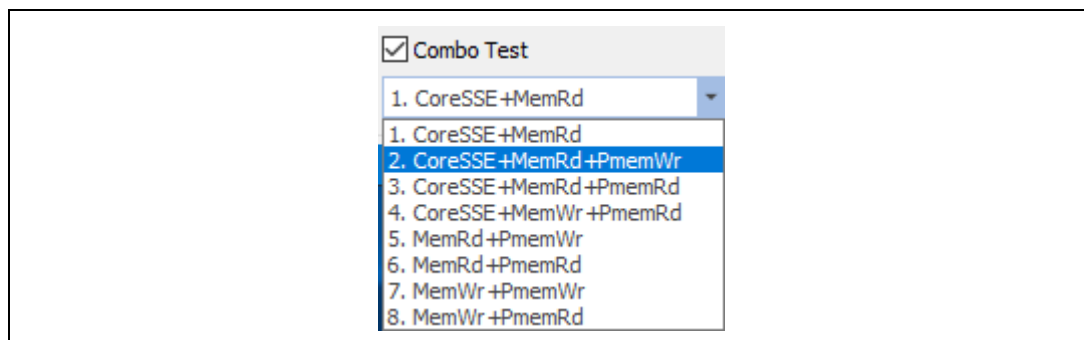
- CoreSSE+MemRd: Runs the core IA/Intel® SSE memory read.

- CoreSSE+MemRd+PmemWr: Runs the core IA/Intel® SSE, memory read, and PMem Write.

- CoreSSE+MemRd+PmemRd: Runs the core IA/Intel® SSE, memory read, and PMem read.

- CoreSSE+MemWr+PmemRd: Runs the core IA/Intel® SSE, memory write, PMem read.

- MemRd+PmemWr: Runs the memory read and the PMem write.

- MemRd+PmemRd: Runs the memory read and the PMem read.

- MemWr+PmemWr: Runs the memory write and the PMem write.

- MemWr+PmemRd: Runs the memory write and the PMem read.

The **Combo Test** will automatically select the number of cores to be used for each combo test. The user can change the core selection if desired.
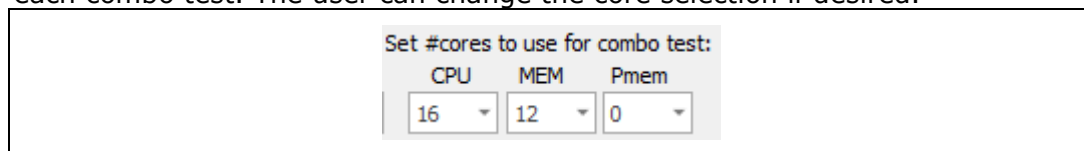
5.2.4 Intel® PTAT Menus

The Intel® PTAT program menu is shown in the following figure. The program title bar. The built-in menu allows the user to access some useful features such as capturing the screenshot, saving the HW summary to file, changing the test configuration, and so forth.

Figure 5-31. Intel® PTAT Program Menu
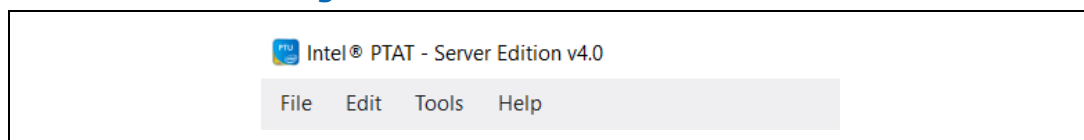
5.2.4.1 File Menu

The **File** menu allows the user to save the HW summary, save the event log, and capture a screenshot.
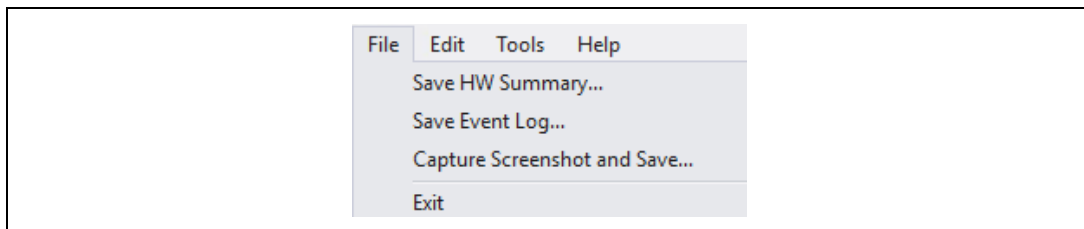
- **Save HW Summary** copies the list of information in a summary tab and saves it into a CSV-formatted file. A dialog box will pop up for file location selection.

- **Save Event Log** copies the list of events in Event tab and save it into a CSV formatted file.

- **Capture Screenshot** takes a snapshot of the current screen and saves it into a file as .BMP format. A dialog box appears for file location selection.

- **Exit** terminates any running tests and exits the program.

5.2.4.2 Edit Menu

Edit menu allows user to change the CPU test configuration, memory test configuration, the Pmax test configuration, and the runtime options.
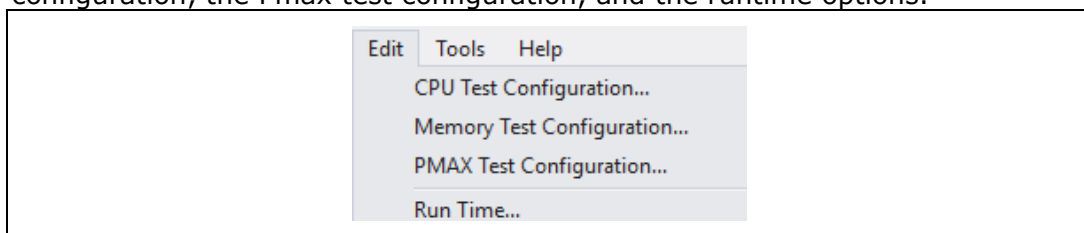
5.2.4.2.1 Edit CPU Test Configuration

Selecting "Edit" → "CPU Test Configuration…" brings up the "Edit CPU Test Configuration" dialog box.

Intel Confidential

Figure 5-32. Edit CPU Test Configuration Window
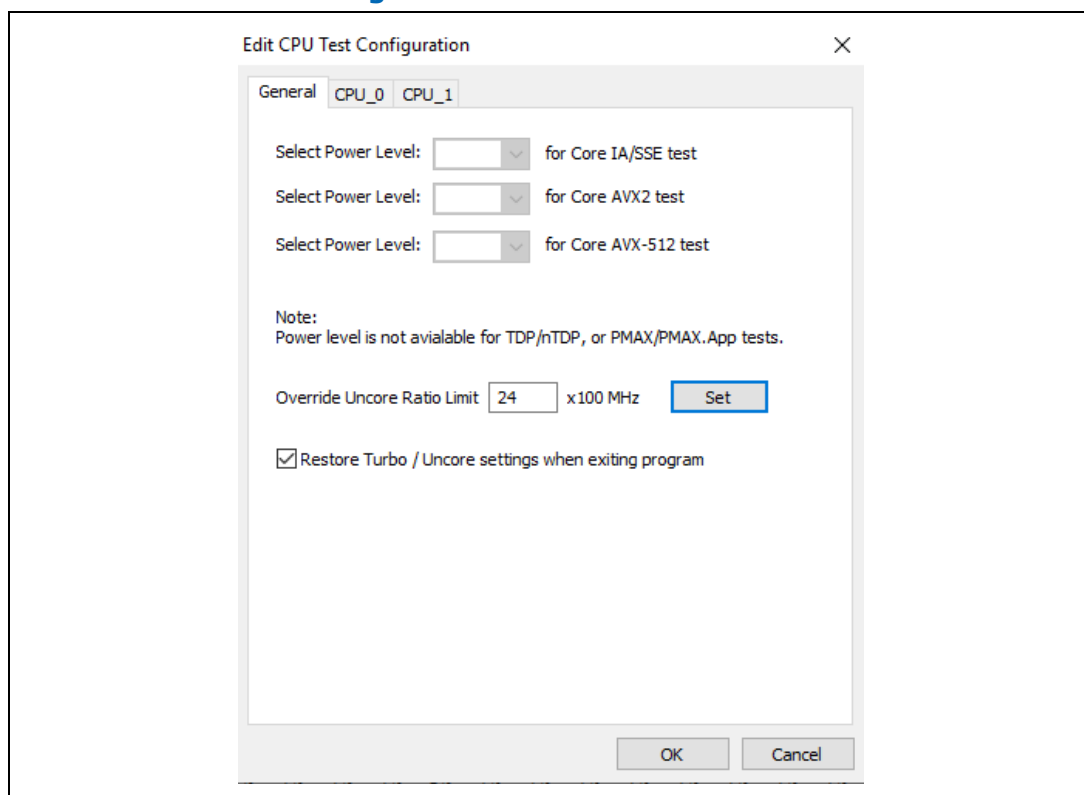
5.2.4.2.2 Edit CPU Test Configuration - General

In this page, the user can change the power level settings for the core IA/Intel® SSE, Intel® AVX2, and the Intel® AVX-512 tests. Valid power levels are 50, 60, 70, 80, 90, and 100.

Note: When TDP/nTDP, or Pmax/Pmax.App tests are selected from the **CPU Test** menu, the power level settings will be disabled. The power level is only applicable for "Core IA/Intel® SSE", "Core AVX2", or "Core AVX-512" tests.

The uncore frequency can be set by changing the number in the uncore Ratio limit and applied by clicking the "Set" button.

By default, Intel® PTAT will restore the original turbo and uncore ratio settings when exiting the program.

5.2.4.2.3 Edit CPU Test Configuration – CPU_0, CPU_1, …

Each CPU socket has its own configuration page. In the CPU_# page, the user can select which cores to run in this CPU socket, and the threads to run the test.

Figure 5-33. Edit CPU Test Configuration
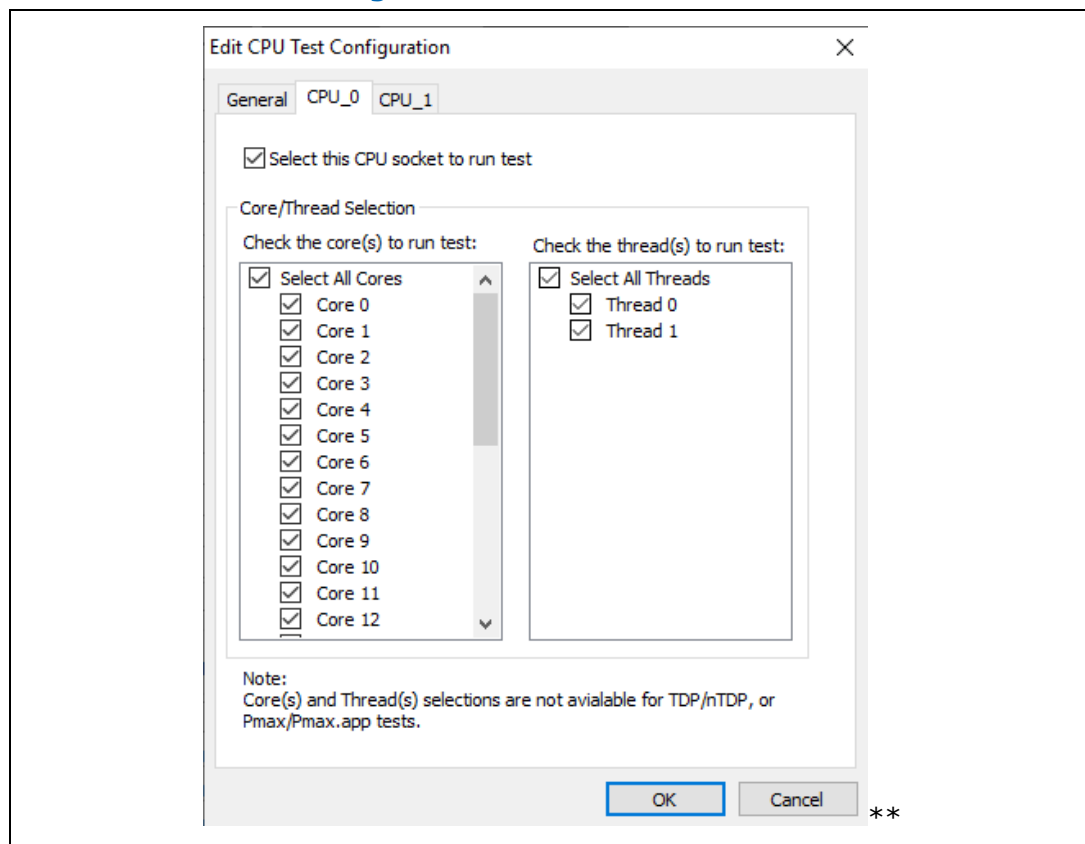
Clicking individual core will toggle on and off the core and thread selection.

Clicking **Select All** toggles checking and unchecking all cores and threads selection.

Note: When TDP/nTDP, or Pmax/Pmax.App tests are selected from the **CPU Test** menu, the power level settings will be disabled. The power level is only applicable for "Core IA/Intel® SSE", "Core AVX2", or "Core AVX-512" tests.

5.2.4.2.4 Edit Memory Test Configuration

Selecting "Edit" → "Memory Test Configuration…" brings up the **Edit Memory Test Configuration** dialog box.

Intel Confidential

Figure 5-34. Edit Memory Test Configuration
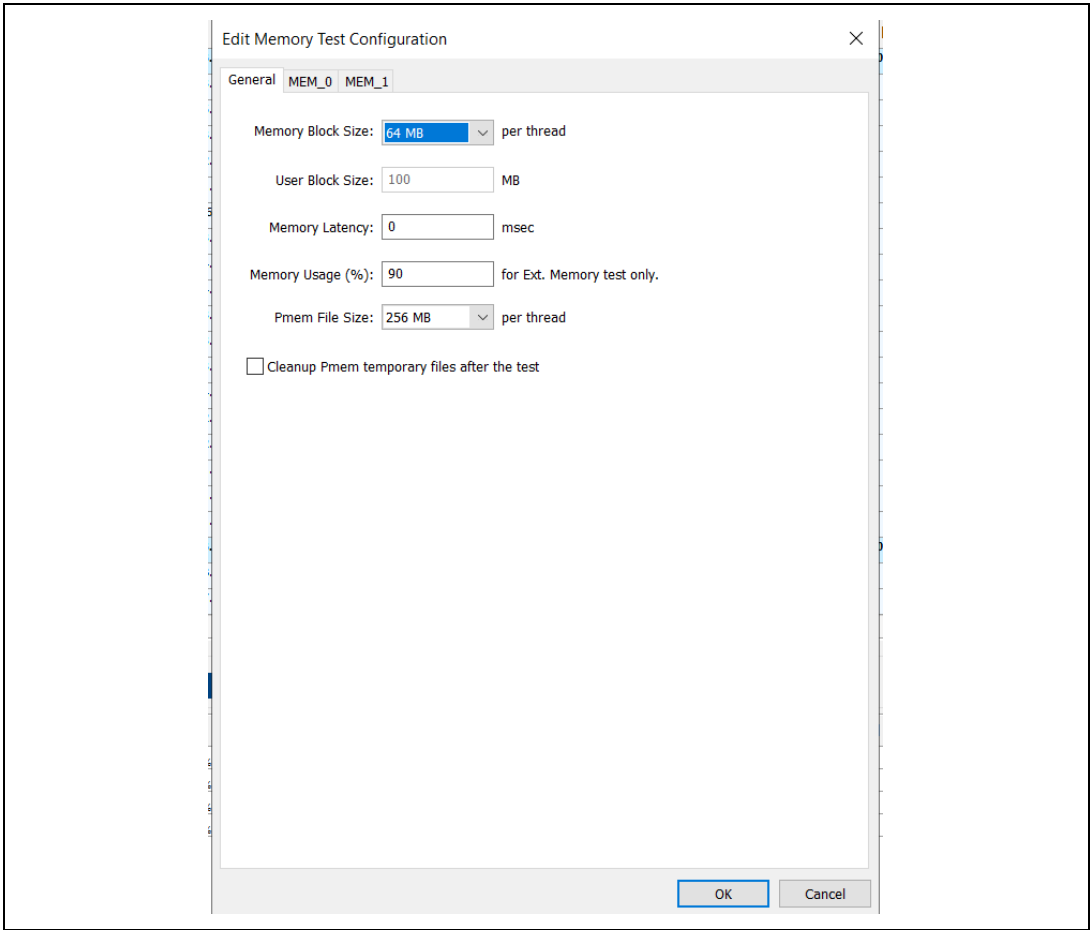
5.2.4.2.5 Edit Memory Test Configuration - General

In this page, the user can change the power level settings for MEM tests. Valid power levels for memory test are only 100.

Note: The PMem tests can only run with 100% power level.

The "Memory Block Size" is available to choose when clicking the drop-down list box.
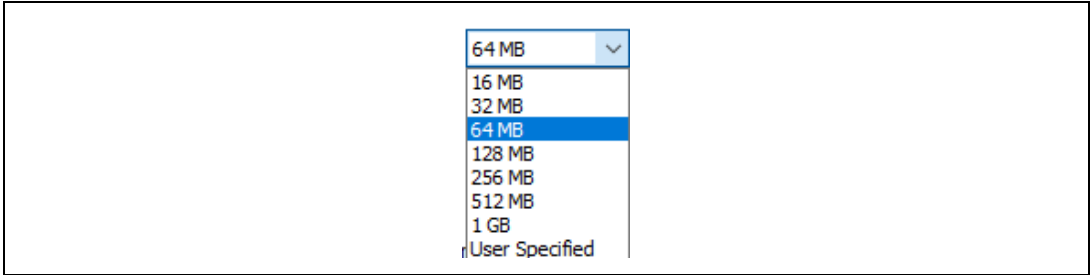
The valid sizes are 16 MB, 32 MB, 64 MB, 128 MB, 512 MB, 1 GB, and "User Specified".

When "User Specified" is selected, the "User Block Size" will be enabled.

User Block Size: 100 MB

"Cleanup Pmem temporary files after the test" is used for PMem testing. When this is enabled, the AD R/W test will delete all the temporary files from the namespace drive.

5.2.4.2.6 Edit Memory Test Configuration – MEM_0, MEM_1, …

Each MEM socket will have its own configuration page. In the MEM_# page, the user can select which cores to run in this MEM/Pmem socket test.

Figure 5-35. Edit Memory Test Configuration

Change the core range **From** and **To** in the MEM selection for memory R/W test.

There is a total of six PMem paths that the user can choose. By default, only PMem 0 is enabled. To enable other **Pmem #** paths, simply click the ☐ Pmem 1 Selection checkbox.

When the "Use Custom" test is selected in the PMem test group, the "Custom Test" type will be used for that **Pmem #** path.
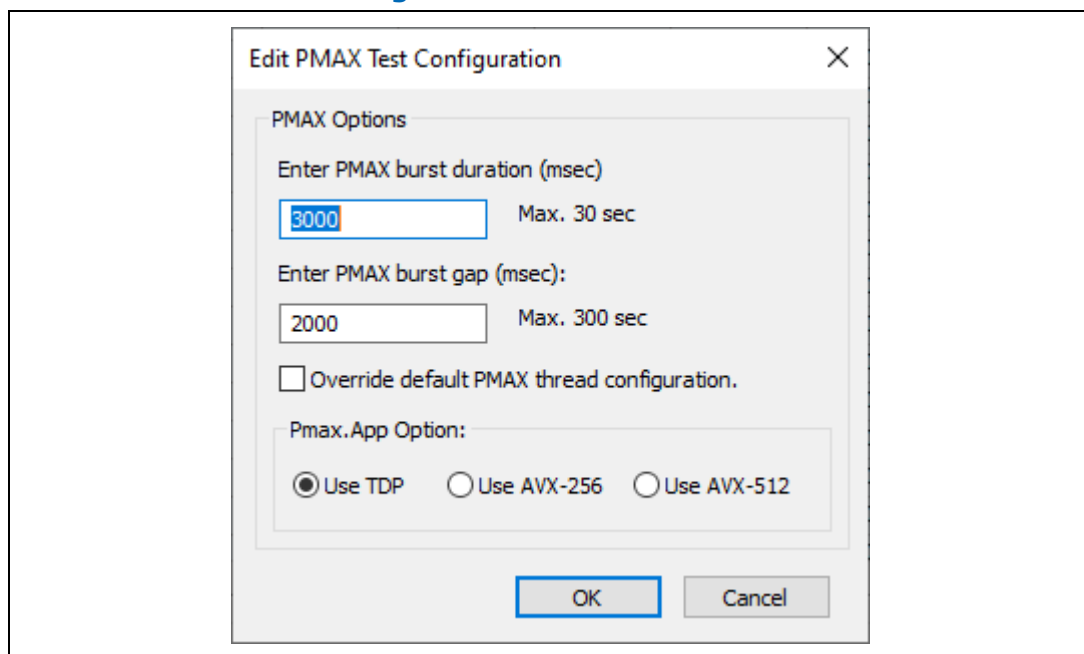
5.2.4.2.7 Edit Pmax Test Configuration

Selecting "Edit" → "Pmax Test Configuration…" brings up the **Edit Pmax Test Configuration** dialog box.

Figure 5-36. Edit Pmax Test Configuration

In this configuration page, the user can change the Pmax burst duration, burst gap, and instruction set to be used for the test.

The Pmax burst duration is used to tell how long the Pmax high current workloads should run after the Pmax workloads have initialized. The default is three seconds.

Burst gap is to tell how long the Pmax should stay in Idle after the duration of the burst. The default is two seconds.

The "Override default thread configuration" checkbox exists to allow the user to force Pmax to use the thread configuration specified in the CPU Test Configuration dialog. When this is deselected, PTAT will ignore the user-specified thread configuration in favor of a configuration likely to generate the highest electrical current.

The Pmax.App option allows the Pmax.App to run with different type of instructions. The available instructions are TDP, Intel® Advanced Vector Extensions 256 (Intel® AVX-256) and Intel® AVX-512.

Intel Confidential

5.2.4.2.8 Edit Run Time

Selecting "Edit" → "Run Time…" will bring up **Edit Run Time** dialog box.
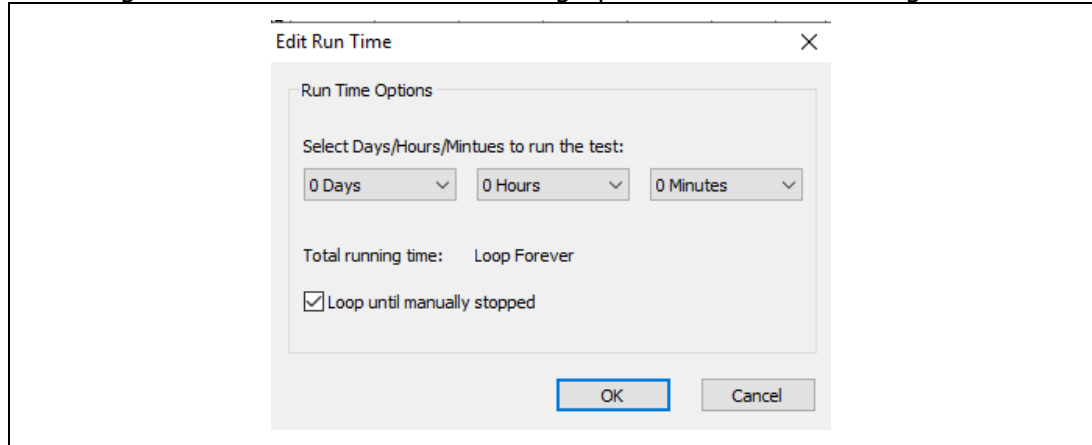
In this option page, the user can select how long the test should run. Select Days/Hours/Minutes from the drop-down list.

By default, "Loop until manually stopped" is enabled. This means that the test will run forever.

5.2.4.3 Tools Menu

The **Tools** menu allows user to open and close the Intel® PTAT message window, enable and disable the turbo, and run a cleanup.
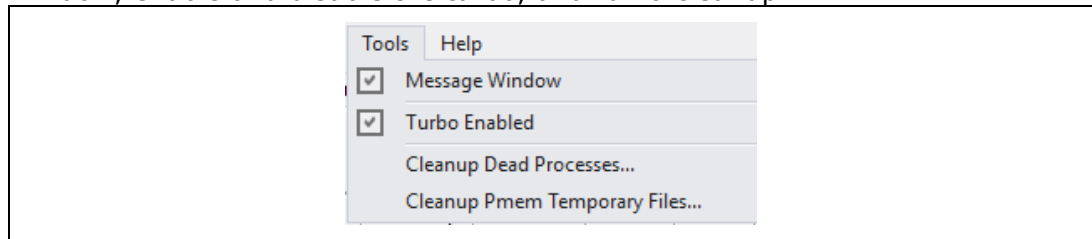
- Checking the **Message Window** box will enable the Intel® PTAT Message Window. A separate window will appear.

- When the **Turbo Enabled** box is checked, all CPUs will enable turbo. Uncheck it will disable Turbo for all CPUs.

- The **Cleanup Dead Processes** will terminate and remove any previous running test processes.

- The **Cleanup Pmem Temporary Files** deletes all temporary files from the PMem path.

Intel Confidential

5.2.4.4 Help Menu
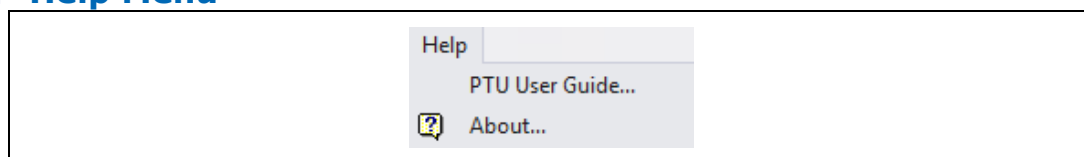
- "Help" → "PTAT User Guide…" opens this *Intel® PTAT User Guide*.
- "Help" → "About" shows the Intel® PTAT version and release date.

Figure 5-37. About Window
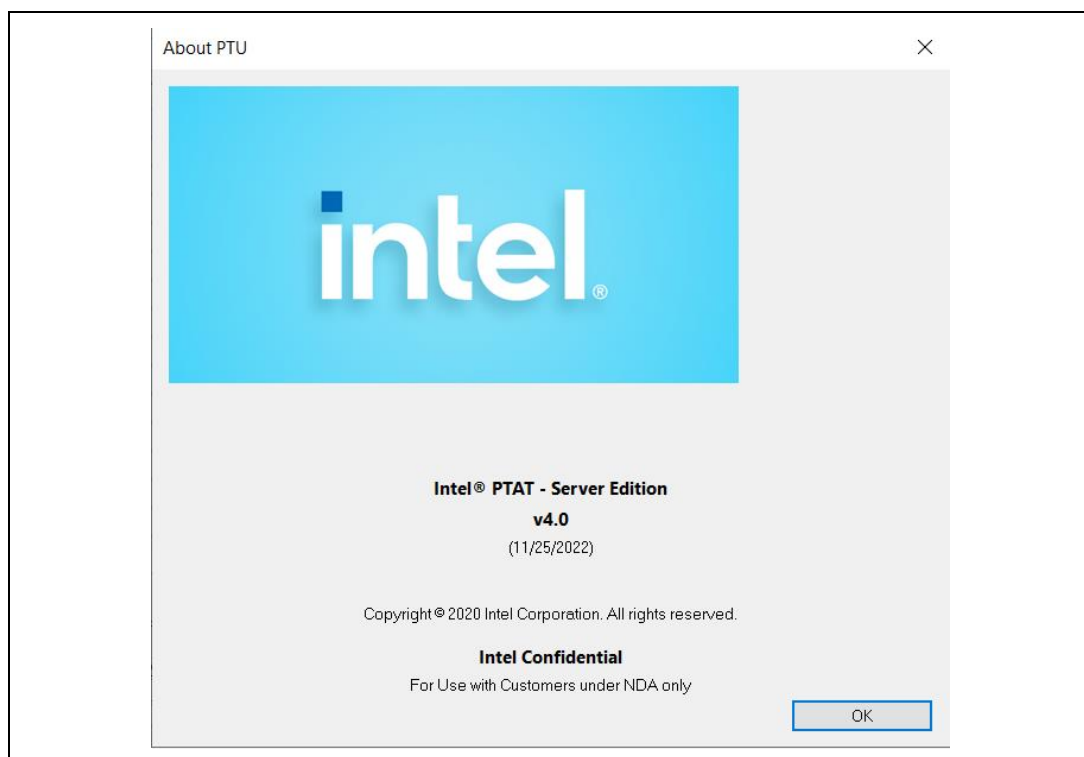
5.2.5 Starting and Stopping the Test
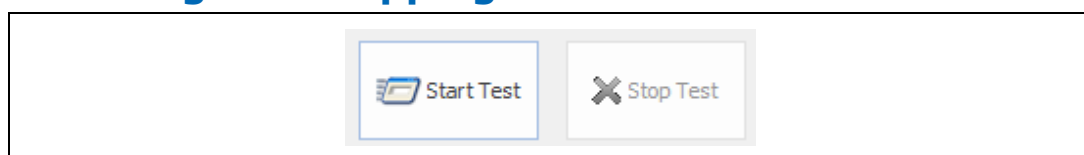
The test can be started by clicking the "Start Test" button. When the test is running, the "Stop Test" button will be visible and enabled, and the "Start Test" button will be grayed out. Clicking the "Stop Test" button will terminate all the tests.
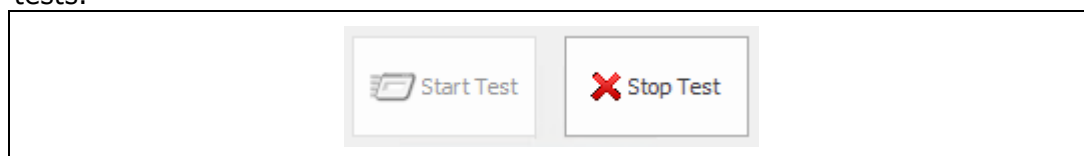
5.2.5.1 Test Running Status

The status bar will display the test running timer when the test is running. If the run time is set to run forever, the timer will count up in number of days, and HH:MM:SS.

Running [0 days, 0:03:06] Last Run: 01/29/2019 10:21:43
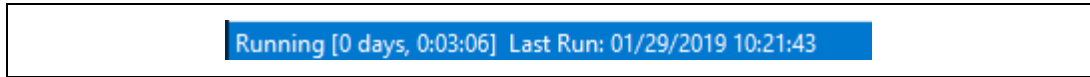
When the run time is specified in the test, the timer will counter down instead. For example, when the time is set to run 1 hour, it will count down from 60 minutes.

Running [0 days, 0:59:55] Last Run: 01/29/2019 10:28:19

When the test is stopped, the status bar will stop the timer and update the last run status.

Stopped [0 days, 0:04:25] Last Run: 01/29/2019 10:21:43
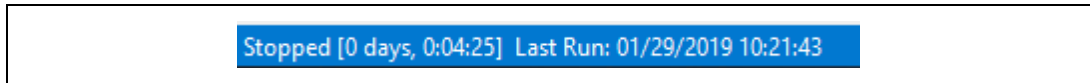
6 Running Intel® PTAT on Linux*

The Linux* Intel® PTAT tool can be run on CLI-mode only. This section describes the process to launch the tool and the available commands for testing. Intel® PTAT should not be running during software or firmware updates.

6.1 Launching the Intel® PTAT

The Intel® PTAT requires superuser (root) to run:

```
#su

#cd <ptat installed directory>

#./ptat
```

6.2 Intel® PTAT Available Commands

The -h option shows the Intel® PTAT available commands as follows:

```
#./ptat -h

Usage: ptat -h |

[-cpu bitmask] [-cpucore bitmask] [-cputhr bitmask]

[-mem bitmask] [-memcore bitmask] [-memthr bitmask]

[-pmem bitmask] [-pmemcore bitmask] [-pmemthr bitmask]

[-fpga bitmask]

[-moncpu bitmask] [-monmem bitmask] [-moncore bitmask]

[-monfpga bitmask]

[-cst | -pst] [-staterepeat num] [-statetime interval] [-statenum num] [-test teststring]

[-filter bitmask]

[-ct cputest] [-mt memtest] [-pt pmemtest] [-pmdir path] [-ft fpgatest]

[-cp power] [-mi intensity]

[-s0 time] [s1 time] [-s2 time]

[-avx level] [-b turbo] [-u ratio]
```

```
[-noclear] [-norestore]

[-i interval] [-t time] [-ts] [-l monlevel] [-scr] [-wf]

[-nd] [-naw]

[-log] [-logdir path] [-csv] [-s] [-q] [-y] [-v]
```

6.3   Command Line Options

The following table lists the available command line options that can be used to run Intel® PTAT:

Table 6-1. Command Line Options

Command	Description
-cpu <bitmask>	Specifies the CPU mask value for CPU tests. Default value is 0xFFFF. For example, **-cpu 0x0** will skip running tests on any CPU; **-cpu 0x1** will run tests on CPU 0 only. **Note:** Use **0x** to specify the value in hexadecimal.
-cpucore <bitmask>	Specifies the core mask value for CPU tests. The default value is 0xFFFFFFFFFFFFFFFF. For example, **-cpucore 0x9** will run the CPU test on core 0 and core 3 only.
-cputhr <bitmask>	Specifies the thread mask value for CPU tests. The default value is 0xFF. For example, **-cputhr 0x2** will run the CPU test on thread 1 only of all cores.
-mem <bitmask>	Specifies the MEM mask value for memory tests. The default value is 0xFFFF. For example, **-mem 0x0** will skip running tests on any MEM; **-mem 0x1** will run tests on MEM 0 only.
-memcore <bitmask>	Specifies the core mask value for memory tests. The default value is 0xFFFFFFFFFFFFFFFF.
-memthr <bitmask>	Specifies the thread mask value for memory tests. The default value is 0xFF.
-pmem <bitmask>	Specifies the PMEM mask value for memory tests. The default value is 0xFFFF. For example, **-pmem 0x0** will skip running tests on any PMEM; **-pmem 0x1** will run tests on PMEM 0 only.
-pmemcore <bitmask>	Specifies the core mask value for PMEM memory tests. The default value is 0xFFFFFFFFFFFFFFFF.
-pmemthr <bitmask>	Specifies the thread mask value for PMEM memory tests. The default value is 0xFF.
-fpga <bitmask>	Specifies which FPGA to run the test. This is a mask value. The default value is 0xFFFFFFFFFFFFFFFF. For example, **-fpga 0x2** will run the test on the socket 1 FPGA only.
-moncpu <bitmask>	Specifies the CPU mask value for the Intel® PTAT monitor and log. The default value is 0xFFFF.
-moncore <bitmask>	Specifies the core mask value for the Intel® PTAT monitor and log. The default value is 0xFFFFFFFFFFFFFFFF.
-monmem <bitmask>	Specifies the MEM mask value for the Intel® PTAT monitor and log. The default value is 0xFFFF.

Intel Confidential

Command	Description
-cst/-pst	There are two main command line formats to choose from for c/p state tests. • -cst -moncpu <cpumask> -moncore <coremask> • -cst -test <preformatted pcstate test string> • -pst -moncpu <cpumask> -moncore <coremask>
-filter <bitmask>	Specify the filter mask value for the Intel® PTAT monitor and log. The default value is 0x17. Bit[0]: Shows the CPU and uncore frequency, utilization, and IPC. Bit[1]: Shows the CPU power and voltage. Bit[2]: Shows the CPU temperature, DTS, and thermal status, log, and margin. Bit[3]: Shows the CPU C and Pkg C-states. Bit[4]: Shows the memory power, temperature, and thermal log. Bit[5]: PMem power and thermal data. Bit[6]: Memory and Pmem read/write bandwidth. Bit[7]: Shows the PCH temperature
-ct	There is a total of eight tests to choose from for CPU stress. The test numbers and names are described as follows. The default is 0. Usage: -ct <test number>, where test number = one of the following values: **Note:** See Intel® PTAT Tests Description for a list of the CPU test descriptions. When 0 is specified, the test will not be performed for any CPU. 0: None. 1: TDP test 2: nTDP test 3: Core IA/Intel® AVX1 test 4: Core Intel® AVX2 test 5: Core Intel® AVX-512 test 6: Pmax test 7: Pmax.App test 8: Turbo test 9: AMX Test (GNR only) 10: Core SSE Test (GNR only)
-mt <test number>	There are three tests to choose from for memory subsystem stress. The test numbers and names are described as follows. The default is 0. **Note:** See Intel® PTAT Tests Description for a list of the memory test descriptions. When 0 is specified, the test will not be performed for any Memory. 0: None 1: Read test 2: Write test 3: R/W test
-pt	Only on Linux*: Single stress test for PMEM.

Intel Confidential

Command	Description
-pmdir <path>	Only on Linux*: The PMEM needs to be provisioned and mounted as different directories for different sockets. For example, for a two-socket configuration, provision two directories. The actual paths on the systems will be <path>0 and <path>1. Example: `-pmdir /mnt/pmem` → should have the paths mounted on the systems as `/mnt/pmem0` and `/mnt/pmem1`)
-ft <test number>	There is only one test to choose for FPGA stress. The test number and test name are described as follows. The default is 0. **Note:** See Intel® PTAT Tests Description for a list of FPGA test descriptions. When 0 is specified, the test will not be performed for any FPGA. 0: None 1: FPGA TDP test
-cp <power level>	Specifies the core power level for CPU test. The valid power levels are 50, 60, 70, 80, 90, and 100. The default is 100. **Note:** Power level settings are not available for TDP/nTDP, or Pmax/Pmax.App tests. The exact power output varies from part to part. Some parts might consume higher power even with the lower power level selected.
-mi <intensity level>	This option must be used with Memory test. There are 0 (lowest) to 5 (highest) intensity levels for memory test you choose. The default is 5.
-s0 <time in ms>	Specify this option to set the Pmax pre-synchronization time. The default is 2000.
-s1 <time in ms>	Specify this option to set the Pmax pre-synchronization time. The default is 5000.
-s2 <time in ms>	Specify this option to set the Pmax post-synchronization time. The default is 3000.
-avx <0..3>	Specify this option to run the Pmax.App and turbo test. The default is 1. 0: Run all versions (for turbo test only) 1: Run the IA/Intel® SSE version 2: Run the Intel® AVX2 version 3: Run the Intel® AVX-512 version
-b <0|1>	Specify this option to enable or disable turbo. 0 is to disable, 1 is to enable. Original turbo settings will be restored when the Intel® PTAT exits the command line program.
-u <ratio>	Specify this option to set the uncore ratio limit.
-noclear	Specify this option not to clear the TLog when program launches. By default, TLog will be cleared when the Intel® PTAT is invoked.
-norestore	Specify this option not to restore the turbo and uncore original settings when the Intel® PTAT exits.
-i <interval>	Specifies the update interval in microseconds. The default is 1000000 (1 second).
-id	Ignore Driver – This option will allow PTAT runs without drivers. Some tool functionality that depends on drivers may not work.

Intel Confidential

Command	Description
-t <run-time>	Specifies the run time in seconds to run the monitor or tests. The default is 0. When specifying 0, the PTAT will run forever. Users will need to use <Ctrl-C> to terminate the Intel® PTAT.
-ts	Specifying this option will include the timestamp in the Intel® PTAT monitor and log.
-l <0,1,2>	Specify this option to change the Intel® PTAT monitor and log output into a short or long version. The default is level 0. 0: Show the package, level data only (short). 1: Show the package, per core, and per memory channel data. 2: Show the package, per core and thread, and per memory channel and DIMM slot data.
-scr	Specifying this option to run the Intel® PTAT monitor in screen mode. The screen will not scroll up.
-wf	Specifying this option to print the Intel® PTAT monitor data in wide format. All sockets' data will be printed in one line.
-nd	Specifying this option to print empty data in spaces, instead of dashes (-).
-naw	Specifying this option to print the line without auto-wrap.
-log	Specifying this option to enable logging to file.
-logdir <path>	Specifying this option to set the log directory where the log files will be saved. The default is `/root/potu/log`.
-csv	Specifying this option save the log file in CSV format.
-q	Specifying this option will suppress any message output, quiet mode.
-s	Specifying this option will print the system summary and exit.
-y	Specifying this option will accept license agreement in advance.
-v	Specifying this option will print the Intel® PTAT version and exit.
-h	Specifying this option will show the Intel® PTAT usage.

6.4 Running the Test and Monitor

When running the Intel® PTAT in command-line mode, the user needs to specify at least one test to run. The monitor can be executed by itself without any test running. Use `-mon` option to run as monitor mode, or use `-log` to log data in the background.

Note: To run the monitor and tests, login as administrator or use the command `-su`.

6.4.1 Running the Intel® PTAT Stress Test Examples

- Run the default TDP test with turbo off:
   ```
   #./ptat –ct 1 –b 0
   ```

- Run the TDP with nTDP enabled:
   ```
   #./ptat –ct 2
   ```

![intel logo]

- Run the core power level with power level 50% and turbo on:

  ```
  #./ptat –ct 3 –cp 50 –b 1
  ```

- Run the core Intel® AVX-512 on core 1, 2, 3, and 7:

  ```
  #./ptat –ct 5 –cpucore 0x8E
  ```

- Run the Pmax on socket 0 only:

  ```
  #./ptat –ct 6 –cpu 0x1
  ```

- Run the turbo test:

  ```
  #./ptat –ct 8 –b 1
  ```

- Run the Intel® Optane™ PMem stress test:

  ```
  #./ptat –pt –pmdir /mnt/pmem
  ```

6.4.2   Running the Intel® PTAT Monitor Examples

- Run the Intel® PTAT monitor in default settings.

  ```
  #./ptat -mon
  ```


- Run the Intel® PTAT monitor in long version mode, level 1:

  ```
  #./ptat -mon –l 1
  ```

- Run the Intel® PTAT monitor using `–filter` to show the CPU thermal and power data only:

  `#./ptat -mon –filter 0x1`

- Run the Intel® PTAT monitor using filter CPU thermal/power and C states data:

  `#./ptat -mon –filter 0x11`

- Run the Intel® PTAT monitor to show memory data only:

  `#./ptat -mon –filter 0x2`

Intel Confidential

```
Time           Dev   Cor Thr MC Ch Sl CFreq UFreq T %Util IPC DTS Temp  Volt  Power TDP TStat TLog #TL TMargin
202239.756_1   MEM0   -   -   -  -  -   -     -   -  -     -   -   35    -    12.45  -    -     -   -    -
202239.756_1   MEM1   -   -   -  -  -   -     -   -  -     -   -   36    -    12.01  -    -     -   -    -
202240.757_2   MEM0   -   -   -  -  -   -     -   -  -     -   -   35    -    12.51  -    -     -   -    -
202240.757_2   MEM1   -   -   -  -  -   -     -   -  -     -   -   36    -    11.95  -    -     -   -    -
```

- Run the Intel® PTAT monitor with screen mode option:

```
#./ptat -mon -core 0x3 -l -scr
```


- Run the Intel® PTAT monitor using -filter for Intel® Optane™ PMem power and DDR-T bandwidth data:

```
# ./ptat -mon -filter 0x70 -pt -pmdir /mnt/pmem -scr
```

Intel Confidential

- Run the Intel® PTAT monitor using -filter for Intel® Optane™ PMem power and DDR-T bandwidth data with -log option:

```
./ptat -mon -filter 0x70 -pt -pmdir /mnt/pmem -log -csv
```

Intel Confidential

6.4.3 Running the Intel® PTAT PCSTATE Test Examples

- Run CSTATE test with default options on socket #0 on cores 0-15

  ```
  #./ptat –cst  –moncpu 0x1 –moncore 0xffff
  ```

- Set cores 0-15 on socket 0 in CState 0 for 3 seconds for 5 times

- Run CSTATE test with user supplied parameters

  ```
  #./ptat –cst  –moncpu 0x1 –moncore 0xffff –statenum 6 –
  statetime 9000000 –staterepeat 7
  ```

- Set cores 0-15 on socket 0 in CState 6 for 9 seconds for 7 times

- Run CSTATE test with preformatted test string

  ```
  #./ptat –cst –test "cs6:p0:c0-15:9000000:7"
  ```

- Set cores 0-15 on socket 0 in CState 6 for 9 seconds for 7 times

- Run CSTATE test with default options on socket #0 on cores 0-15 with the Intel® PTAT monitor in screen mode

  ```
  #./ptat –cst –moncpu 0x1 –moncore 0xffff –scr
  ```

```
Intel(R) Power Thermal Utility - Server Edition 3.5
Host: localhost.localdomain (172.25.77.47) OS: Fedora 32 (Server Edition) Kernel: Linux 5.6.6-300.fc32.x86_64
CPU0: Genuine Intel CPU 0000%@ (0x806F3) SPR ES Freq: 1.5GHz Turbo: 3.9GHz #Cores: 56/112 TDP: 300W Max: 100C #DIMMs: 8
BIOS: EGSDCRB1.86B.0065.D15.2109172316, 09/17/2021 Memory(MB): 515574 total, 514138 free, 1436 used (0%)
 Index Device Cor Thr      C0     C1     C6    PC2    PC6
    17   CPU0   -   -   29.90   0.05  70.04   0.00   0.00
    17   CPU0   0   - 100.00   0.00   0.00      -      -
    17   CPU0   1   - 100.00   0.00   0.00      -      -
    17   CPU0   2   - 100.00   0.00   0.00      -      -
    17   CPU0   3   - 100.00   0.00   0.00      -      -
    17   CPU0   4   - 100.00   0.00   0.00      -      -
    17   CPU0   5   - 100.00   0.00   0.00      -      -
    17   CPU0   6   - 100.00   0.00   0.00      -      -
    17   CPU0   7   - 100.00   0.00   0.00      -      -
    17   CPU0   8   - 100.00   0.00   0.00      -      -
    17   CPU0   9   - 100.00   0.00   0.00      -      -
    17   CPU0  10   - 100.00   0.00   0.00      -      -
    17   CPU0  11   - 100.00   0.00   0.00      -      -
    17   CPU0  12   - 100.00   0.00   0.00      -      -
    17   CPU0  13   - 100.00   0.00   0.00      -      -
    17   CPU0  14   - 100.00   0.00   0.00      -      -
    17   CPU0  15   - 100.00   0.00   0.00      -      -
Stop Cstate Test]not Ctrl-C
```

- Run CSTATE test with default options on socket #0 on cores 0-15 for 1 time

  ```
  #./ptat –cst –moncpu 0x1 –moncore 0xffff –staterepeat 1
  ```

Intel Confidential

```
Enter CState for 3000000 micro seconds
 Index Device Cor Thr     C0      C1      C6    PC2     PC6
     0    CPU0   -   -   25.54   0.03   74.43   0.00    0.00
     0    CPU0   0   -   89.12   0.07   10.81     -       -
     0    CPU0   1   -   88.51   0.03   11.46     -       -
     0    CPU0   2   -   88.16   0.00   11.84     -       -
     0    CPU0   3   -   88.11   0.00   11.89     -       -
     0    CPU0   4   -   88.12   0.00   11.88     -       -
     0    CPU0   5   -   88.15   0.21   11.64     -       -
     0    CPU0   6   -   88.11   0.00   11.89     -       -
     0    CPU0   7   -   88.06   0.00   11.94     -       -
     0    CPU0   8   -   88.06   0.00   11.94     -       -
     0    CPU0   9   -   88.04   0.00   11.96     -       -
     0    CPU0  10   -   88.05   0.00   11.95     -       -
     0    CPU0  11   -   88.11   0.00   11.89     -       -
     0    CPU0  12   -   88.01   0.00   11.99     -       -
     0    CPU0  13   -   88.00   0.00   12.00     -       -
     0    CPU0  14   -   88.00   0.00   12.00     -       -
     0    CPU0  15   -   88.07   0.08   11.86     -       -
     1    CPU0   -   -   29.52   0.05   70.42   0.00    0.00
     1    CPU0   0   -  100.00   0.00    0.00     -       -
     1    CPU0   1   -  100.00   0.00    0.00     -       -
     1    CPU0   2   -  100.00   0.00    0.00     -       -
     1    CPU0   3   -  100.00   0.00    0.00     -       -
     1    CPU0   4   -  100.00   0.00    0.00     -       -
     1    CPU0   5   -  100.00   0.00    0.00     -       -
     1    CPU0   6   -  100.00   0.00    0.00     -       -
     1    CPU0   7   -   99.97   0.00    0.03     -       -
     1    CPU0   8   -   99.89   0.00    0.11     -       -
     1    CPU0   9   -   99.86   0.00    0.14     -       -
     1    CPU0  10   -   99.82   0.00    0.18     -       -
     1    CPU0  11   -   99.76   0.00    0.24     -       -
     1    CPU0  12   -   99.69   0.00    0.31     -       -
     1    CPU0  13   -   99.66   0.00    0.34     -       -
     1    CPU0  14   -   99.63   0.00    0.37     -       -
     1    CPU0  15   -   99.57   0.01    0.42     -       -
```

- Run PSTATE test with user supplied parameters

  ```
  #./ptat -pst -moncpu 0x1 -moncore 0xffff -statenum 6 -
  statetime 9000000 -staterepeat 5
  ```

- Set cores 0-15 on socket 0 in PState 6 for 9 seconds for 5 times. The cores are maintained at the pstate-6 frequency for the duration of the tests.

  ```
  #./ptat -pst -test "ps9:p0:c0-10:5000000:3"
  ```

- Set cores 0-10 on socket 1 in PState 9 for 5 seconds for 3 times. The cores are maintained at the pstate-9 frequency for the duration of the tests.

```
root# ./ptat -pst -test "ps9:p0:c0-10:5000000:3"
```

Index	Device	Cor	Thr	CFreq	UFreq	PState	Util	IPC
0	CPU1	-	-	854	800	9	5.62	1.53
0	CPU1	0	-	999	-	9	11.76	1.32
0	CPU1	1	-	1072	-	9	8.25	1.50
0	CPU1	2	-	1066	-	9	9.27	1.08
0	CPU1	3	-	1071	-	9	5.85	0.37
0	CPU1	4	-	1070	-	9	7.60	0.77
0	CPU1	5	-	1055	-	9	7.34	1.15
0	CPU1	6	-	1067	-	9	11.09	1.09
0	CPU1	7	-	1087	-	9	6.66	0.45
0	CPU1	8	-	1087	-	9	16.91	0.90
0	CPU1	9	-	1081	-	9	7.21	0.81
0	CPU1	10	-	1094	-	9	6.55	0.54
0	CPU1	-	-	850	800	9	4.88	0.61
0	CPU1	0	-	1075	-	9	10.06	1.03
0	CPU1	1	-	1072	-	9	10.24	1.18
0	CPU1	2	-	1068	-	9	14.39	1.12
0	CPU1	3	-	1100	-	9	8.01	0.21
0	CPU1	4	-	1101	-	9	8.01	0.21
0	CPU1	5	-	1070	-	9	10.07	1.20
0	CPU1	6	-	1069	-	9	14.35	1.24
0	CPU1	7	-	1078	-	9	11.91	0.61
0	CPU1	8	-	1088	-	9	20.06	0.54
0	CPU1	9	-	1085	-	9	9.99	0.63
0	CPU1	10	-	1082	-	9	12.23	0.69
0	CPU1	-	-	850	800	9	3.21	0.74
0	CPU1	0	-	1076	-	9	10.07	1.03
0	CPU1	1	-	1077	-	9	10.05	1.01
0	CPU1	2	-	1070	-	9	11.02	1.17

7 Notes

This section contains notes related to Intel® PTAT tool.

7.1 Intel® PTAT PMAX test workload

Intel® PTAT PMAX test workload may not reach specification values for PMAX or PMAX.APP.

- The Intel® AVX-512 workload Intel® PTAT uses for the PMAX is no longer able to reach PMAX or PMAX.APP rated values as published in the *Eagle Stream Platform External Design Specification (EDS), Volume Three: Electrical,* document number 613206.

- At this time, Intel suggests using additional workloads in conjunction with PTAT PMAX to better reach PMAX or PMAX.APP rated values as published in the *Eagle Stream Platform External Design Specification (EDS), Volume Three: Electrical,* document number 613206. Intel® PTAT Intel® AVX-512 workload only provides a subset of testing aimed at CPU cores only. Total package power is a cumulative number based on additional CPU components such as I/O, Accelerators and Memory controllers.

- An additional workload will be provided by Intel via the System Health Check tool kit that may provide a more strenuous workload able to closer reach PMAX or PMAX.APP. This workload also may not fully reach PMAX or PMAX.APP values as published in the *Eagle Stream Platform External Design Specification (EDS), Volume Three: Electrical,* document number 613206.

7.2 Turbo Test Option – "allcores"

The "Run All cores only" checkbox feature under Turbo test in Windows* GUI, and -allcore flag in Windows* CLI and Linux* version, will be removed on the new release v3.8.8 of the Intel® PTAT tool.

Moving forward, this will be covered under the regular Turbo test feature. User can refer to the frequency from the highest number core for the testing.