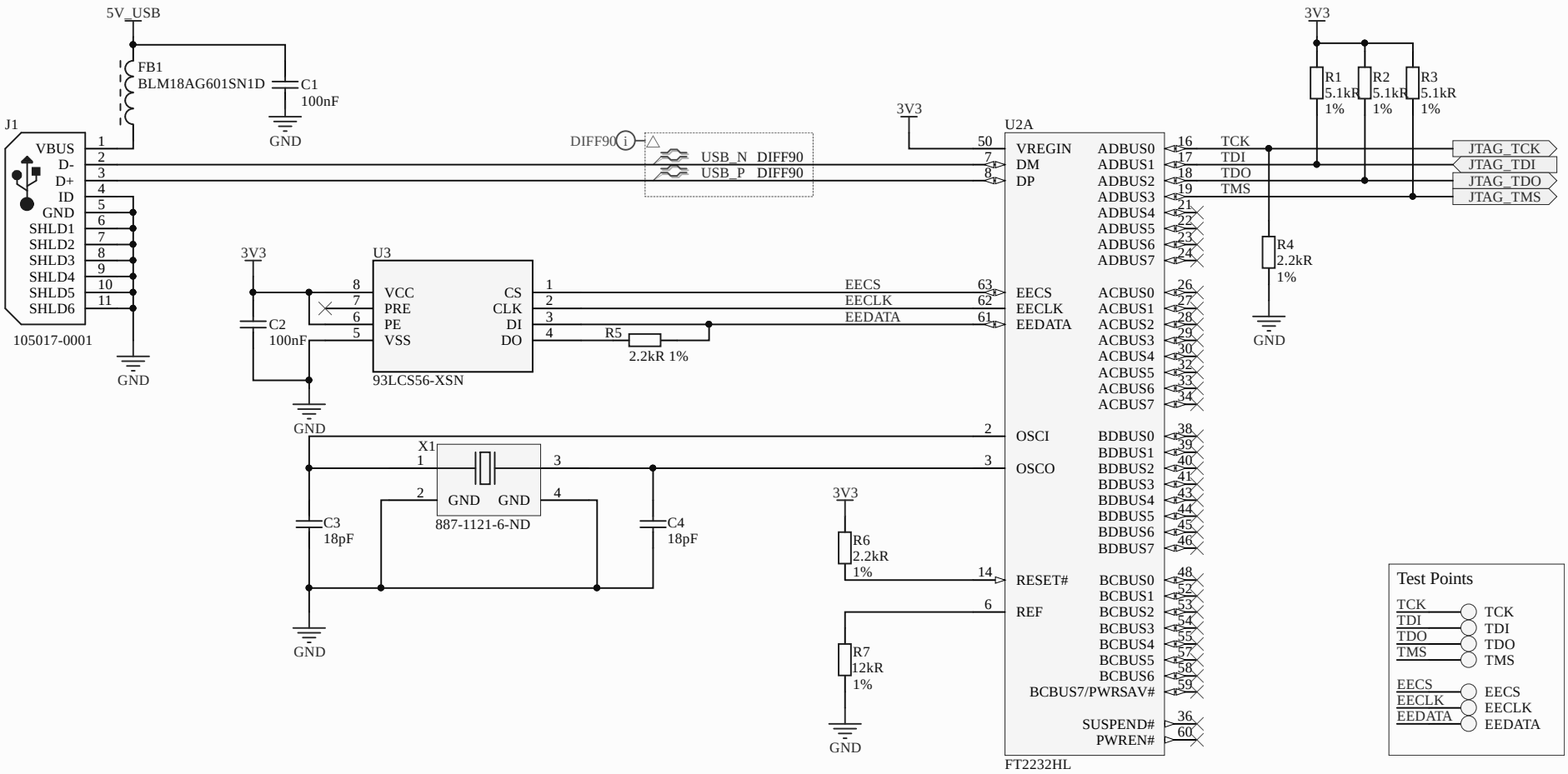
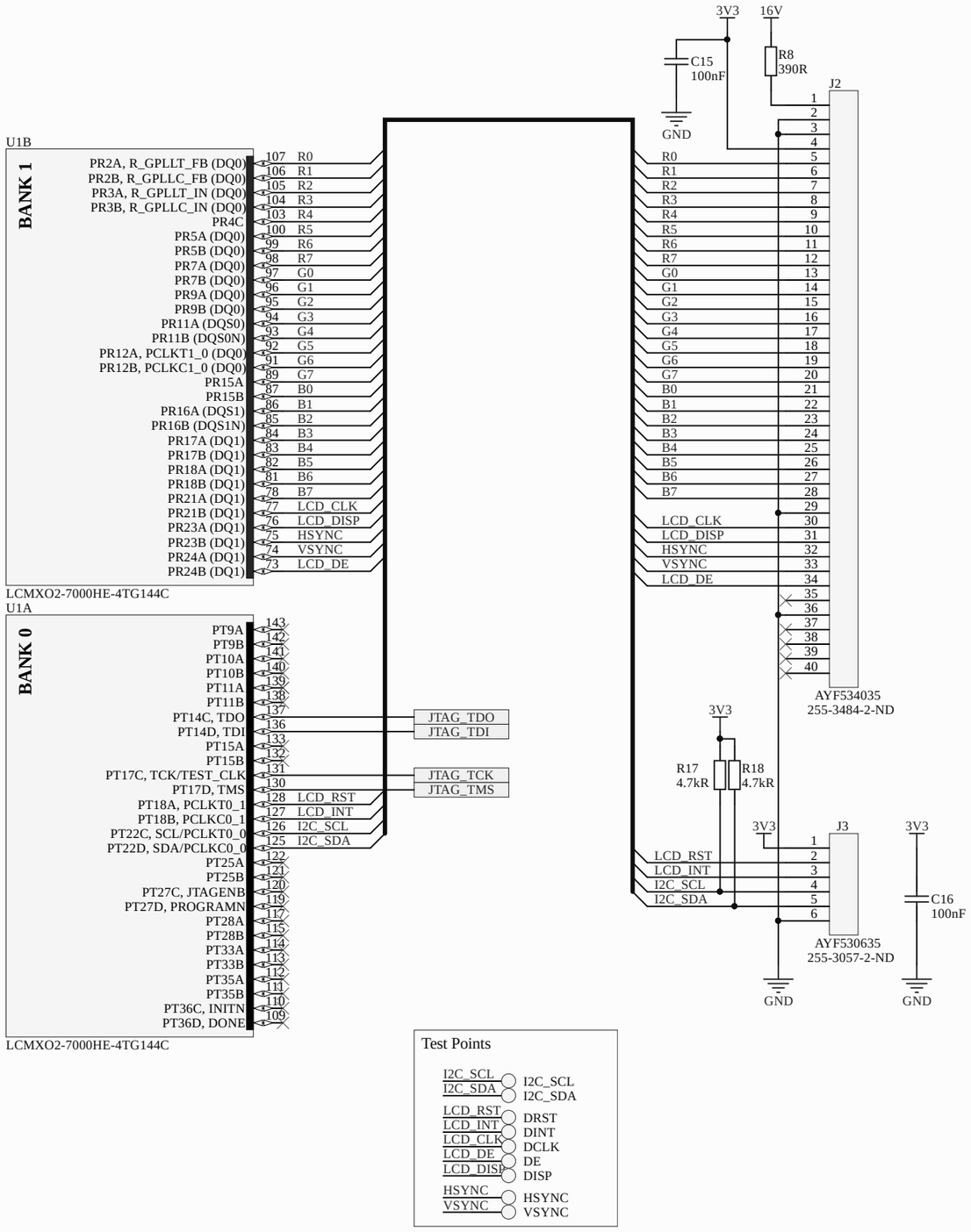
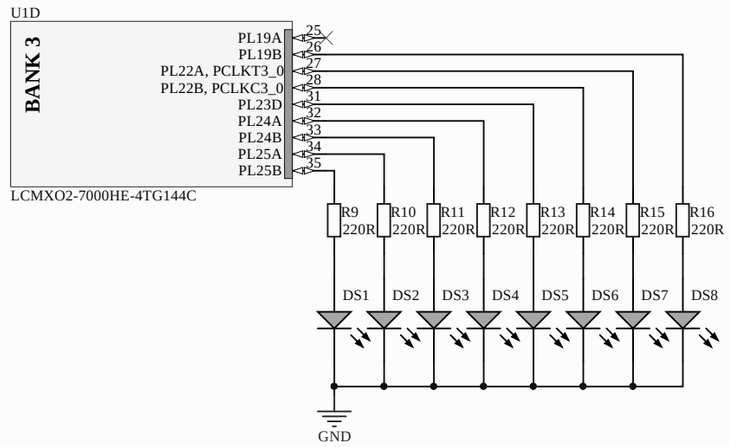


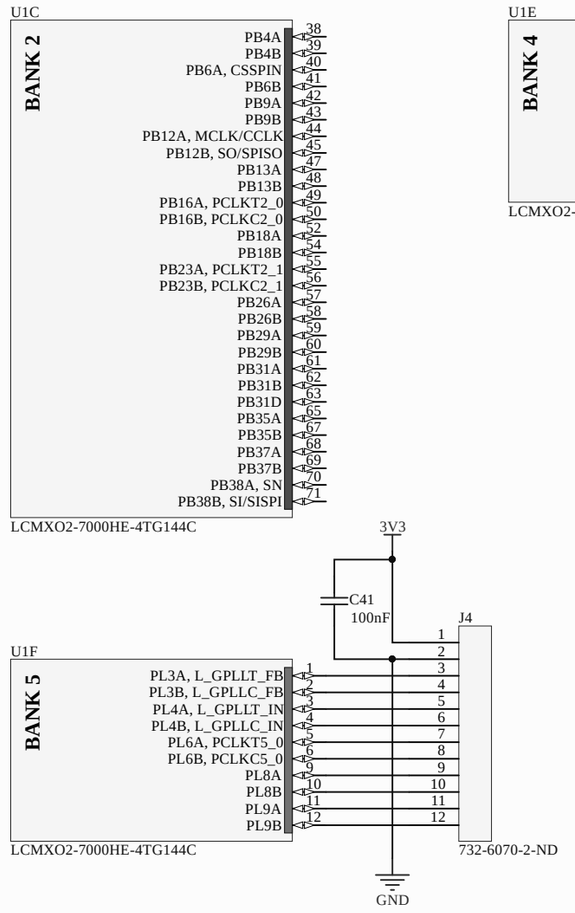
Title	USB to JTAG	
Size: A4	Number:	Revision:
Date: 2018-08-06	Sheet of	
File: C:\Users\..\USB-to-JTAG.SchDoc	Drawn By: Fred Vatnsdal	

LCD Interface and JTAG Programming



Status LEDs



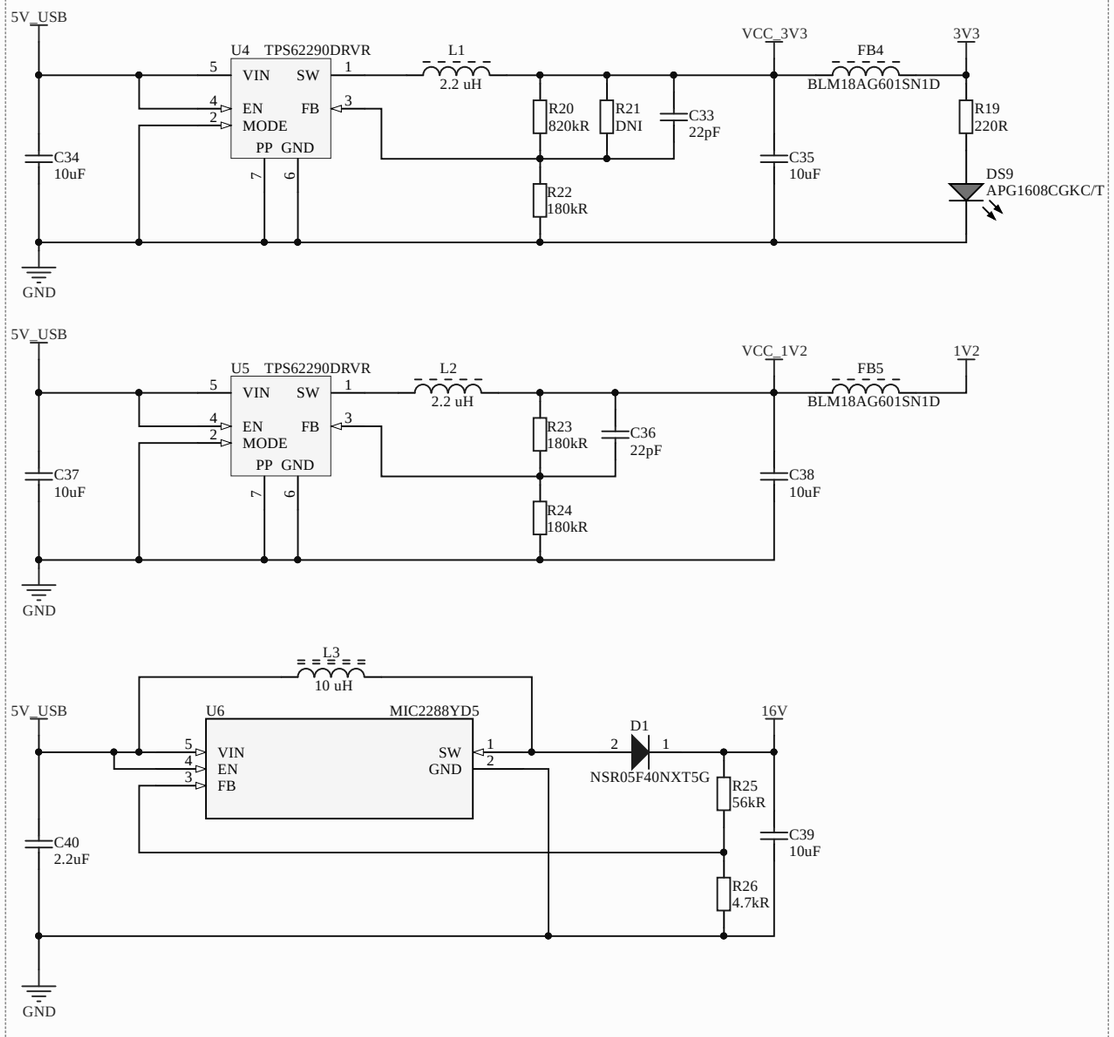


Title: FPGA		
Size: A3	Number:	Revision:
Date: 2018-08-06		Sheet of
File: C:\Users\..\FPGA.SchDoc		Drawn By:

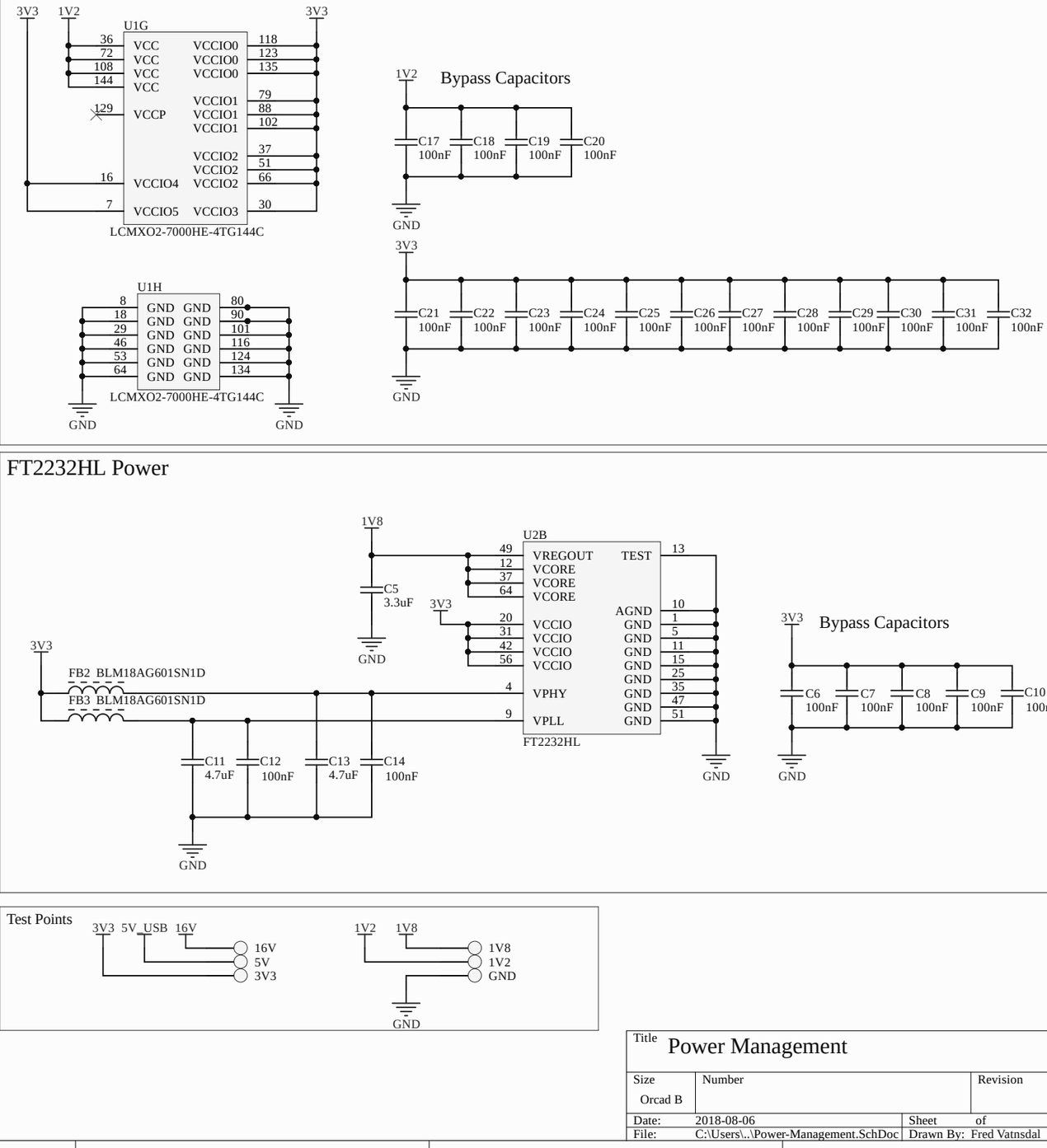
Power Supply

Power Nets

Width Constraint [Pref Width = 1mm Min Width = 0.25mm Max Width = 1.5mm]



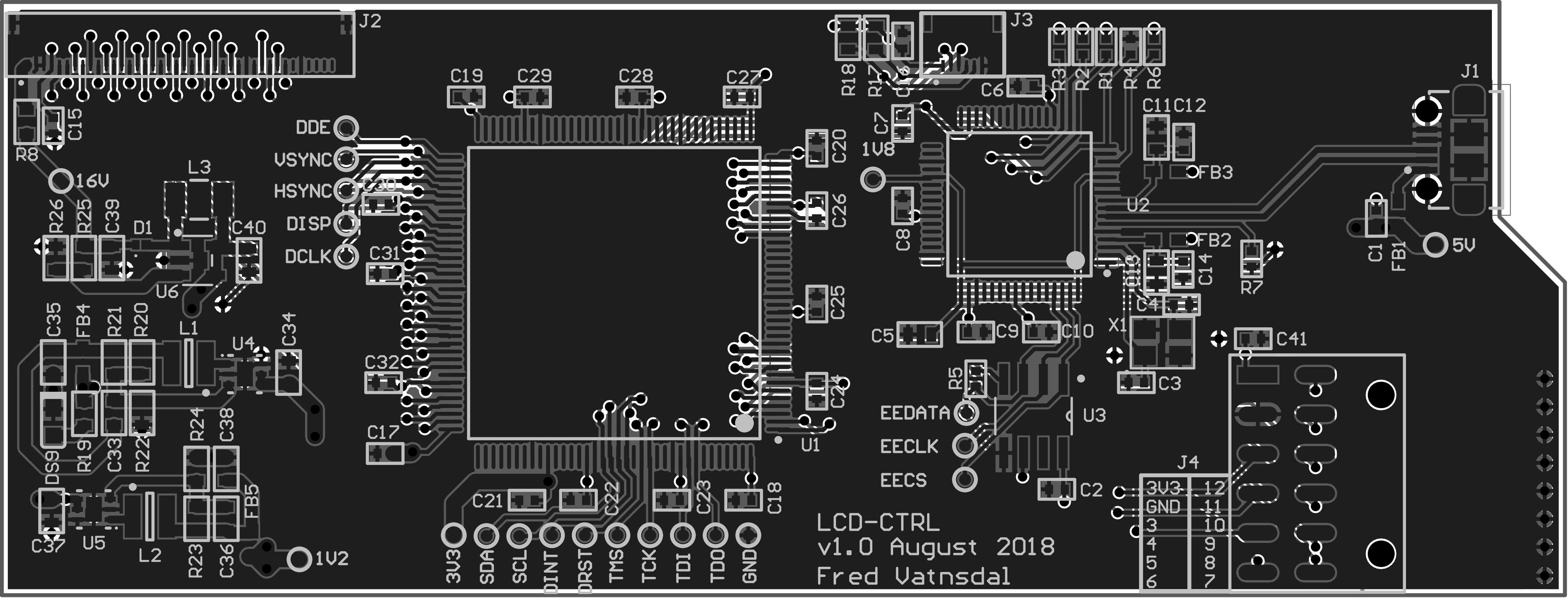
FPGA Power

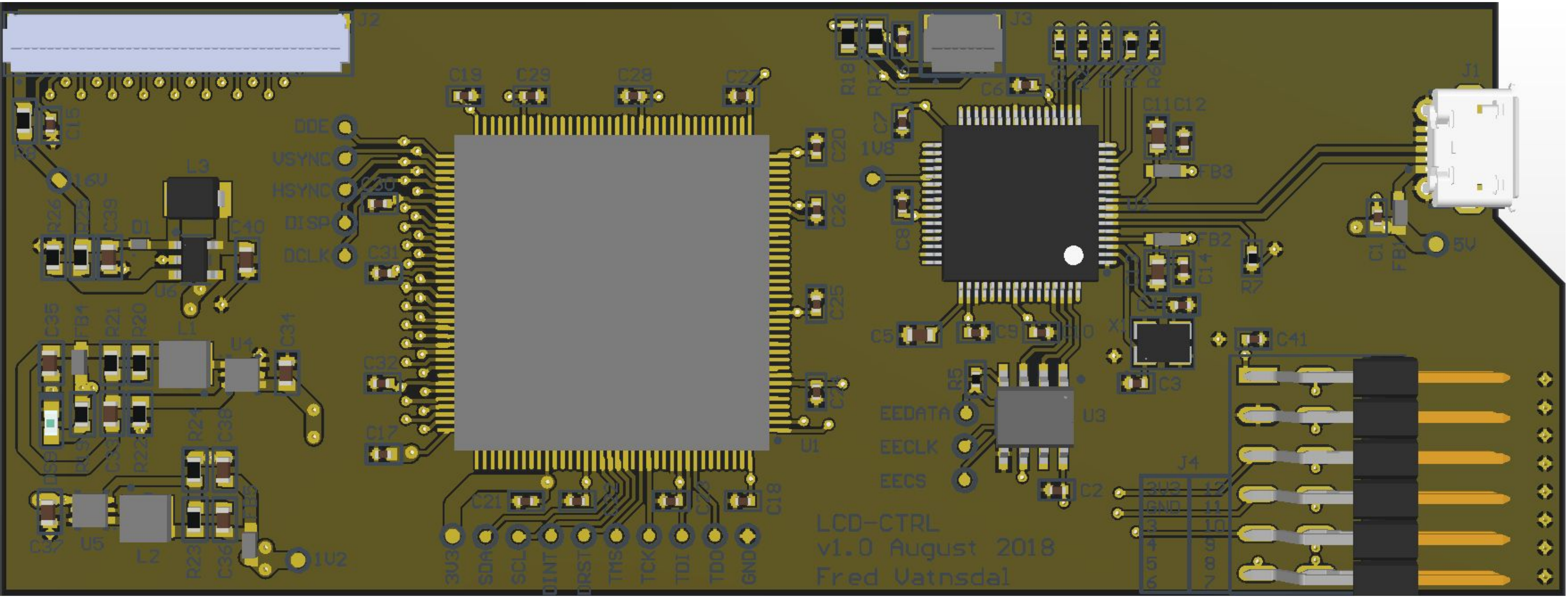


FT2232HL Power

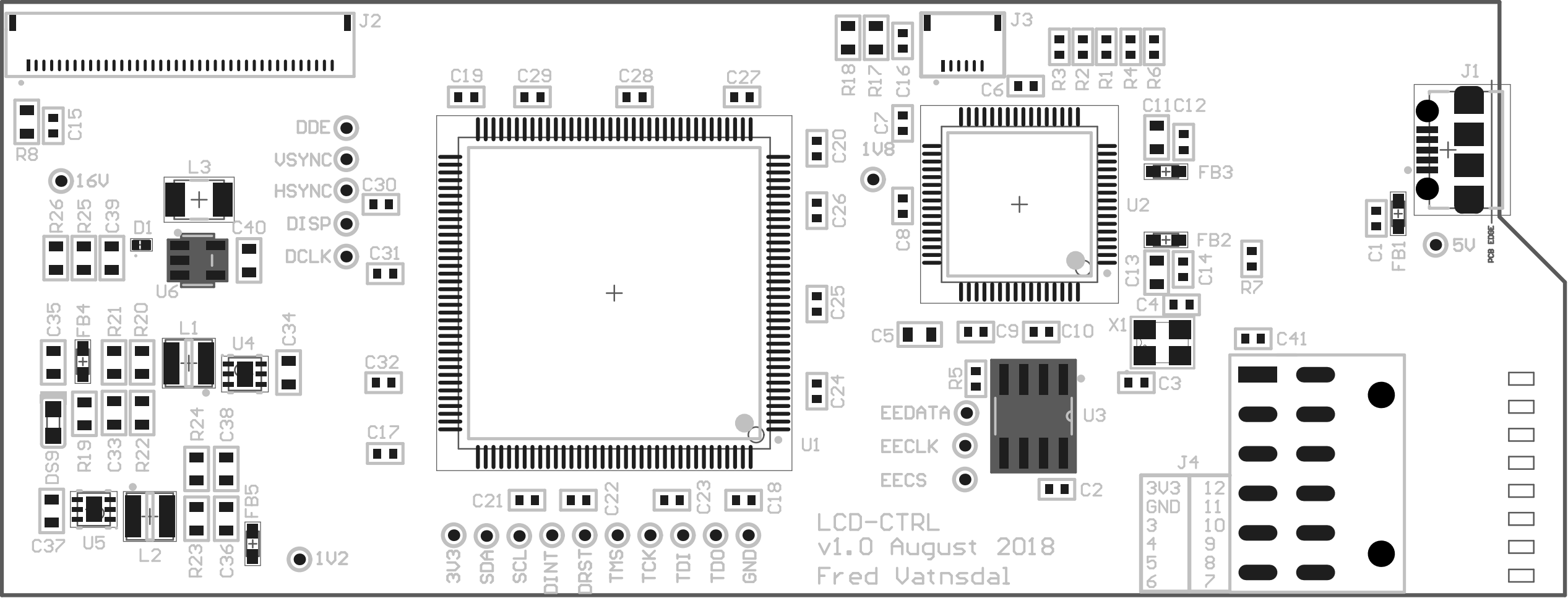
Test Points

Title: Power Management		
Size: Orcad B	Number:	Revision:
Date: 2018-08-06		Sheet of
File: C:\Users\..\Power-Management.SchDoc		Drawn By: Fred Vatnsdal


J2
J3
J1
C19
C29
C28
C27
R18
R17
C16
C6
R3
R2
R1
R4
R6
C11C12
FB3
U2
FB2
C1
FB1
5V
C15
R8
DDE
VSYNC
HSYNC
DISP
DCLK
16V
L3
R26
R25
C39
D1
C40
U6
C30
C31
C20
C26
C25
C24
1V8
C7
C8
C13
C14
R7
C4
X1
C41
C5
C9
C10
C3
R5
EEDATA
EECLK
EECS
U3
C2
J4
3V3
GND
3
4
5
6
12
11
10
9
8
7
C35
FB4
R21
R20
L1
U4
C34
C32
C17
DS9
R19
C33
R22
R24
C38
C37
U5
L2
R23
C36
FB5
1V2
C21
C22
C23
C18
U1
3V3
SDA
SCL
DINT
DRST
TMS
TCK
TDI
TDO
GND
LCD-CTRL
v1.0 August 2018
Fred Vatnsdal



LCD-CTRL
v1.0 August 2018
Fred Vatnsdal
DDE
VSYNC
HSYNC
DISP
DCLK
EEDATA
EECLK
EECS
1V8
16V
1V2
5V
3U3
SDA
SCL
TMS
TCK
TDI
TDO
GND
J1
J2
J3
J4
U1
U3
U4
U5
U6
L1
L2
L3
X1


J2
C15
R8
16V
L3
R26
R25
C39
D1
C40
U6
DDE
VSYNC
HSYNC
C30
DISP
DCLK
C31
C35
FB4
R21
R20
L1
U4
C34
C32
C17
DS9
R19
C33
R22
R24
C38
C37
U5
L2
R23
C36
FB5
1V2
C19
C29
C28
C27
U1
C21
C22
C23
C18
3V3
SDA
SCL
DINT
DRST
TMS
TCK
TDI
TDO
GND
R18
R17
C16
J3
C6
R3
R2
R1
R4
R6
C7
1V8
C20
C26
C8
U2
C11
C12
FB3
FB2
C13
C14
R7
C4
C5
C9
C10
X1
C3
C25
C24
R5
EEDATA
EECLK
EEECS
U3
C2
C41
J4
3V3
GND
3
4
5
6
12
11
10
9
8
7
J1
C1
FB1
5V
LCD-CTRL
v1.0 August 2018
Fred Vatnsdal

R9
R10
R11
R12
R13
R14
R15
R16
PCB EDGE

Comment	Description	Designator	Footprint	LibRef	Quantity
TP		1V2, 1V8, 3V3, 5V, 16V, DCLK, DE, DINT, DISP, DRST, EECLK, EECS, EEDATA, GND, HSYNC, I2C_SCL, I2C_SDA, TCK, TDI, TDO, TMS, VSYNC	TP_0.75DIA	TP	22
C0402C104K4RACTU	CAP CER 0.1UF 16V X7R 0402	C1, C2, C7, C8, C9, C10, C12, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32	CAP_0402_imperial	C0402C104K4RAC-TU	26
C0402C180K3GACTU	CAP CER 18PF 25V NP0 0402	C3, C4	CAP_0402_imperial	C0402C180K3GACTU	2
CAP 3.3uF 10V 0603(1608)	CAP CER 3.3UF 6.3V X5R 0603	C5	CAP_0603_imperial	C0603C335M9PACTU	1
C0402C104K4RAC-TU	CAP CER 0.1UF 16V X7R 0402	C6, C41	CAP_0402_imperial	C0402C104K4RAC-TU	2
CAP 4.7uF 10V 0805(2012)	4.7µF ±10% 25V X5R Ceramic Capacitor -55°C ~ 85°C Surface Mount, MLCC 0603 (1608 Metric) 0.063" L x 0.031" W (1.60mm x 0.80mm)	C11, C13	CAP_0603_imperial	GRM188R61E475KE11D	2
06035A220JAT2A	CAP CER 22PF 50V C0G 0603	C33, C36	CAP_0603_imperial	C1608C0G1H220J080AA	2
GRM31CR61E106KA12L	CAP CER 10UF 10V X5R 0603	C34, C35, C37, C38, C39	CAP_0603_imperial	LMK107BJ106MALTD	5
GRM188R61A225KE34x	CAP CER 2.2UF 10V X7R 0603	C40	CAP_0603_imperial	GRM188R71A225KE15D	1
NSR05F40NXT5G	Schottky Barrier Diode, 2-Pin DSN, Pb-Free, Tape and Reel	D1	ONSC-DSN-2-152AC-01_V	CMP-1055-00232-1	1
APG1608SEKC/T	LED, SMT, 0603(1608), 0.25mm Tthickness, Super Bright Orange	DS1, DS2, DS3, DS4, DS5, DS6, DS7, DS8	KING-LED0603-25-ORANGE_V	CMP-0239-00002-1	8
APG1608CGKC/T	LED, SMT, 0603(1608), 0.25mm Thickness, Green	DS9	KING-LED0603-25-GREEN_V	CMP-0239-00001-1	1
BLM18AG601SN1D	Chip Ferrite Bead for General Use, 600 Ohm, 500 mA, -55 to 125 degC, 1.6 x 0.8 x 0.95 mm SMD, Tape and Reel	FB1, FB2, FB3, FB4, FB5	MURA-BLM18-F-H1-CHIP-2_V	CMP-0686-00436-2	5
105017-0001	Micro-USB B Receptacle, Right Angle, Bottom Mount, Surface Mount, with Solder Tabs, -30 to 85 degC, 5-Pin USB, RoHS, Tape and Reel	J1	USB-MICRO-B_V	CMP-2000-05827-1	1
AYF534035	CONN FFC FPC 40POS 0.50MM R/A	J2	AYF534035	AYF534035	1
AYF530635	CONN FFC FPC 6POS 0.50MM R/A	J3	AYF530635	AYF530635	1
610112249121	Pin header 12P, 610112249121, Würth Elektronik	J4	610112249121	610112249121	1
SRN3015-2R2M	Semi-shielded Power Inductor, 2.2 uH, +/-20%, 1.8 A, -40 to 125 degC, 3 x 3 x 1.5 mm SMD, RoHS and Halogen Free, Tape and Reel	L1, L2	BOUR-SRN3015-2_V	CMP-0007-00003-1	2
CM322522-100KL	Chip Inductor , 10 uH, +/- 10%, -40 to 125 degC, 1210 (3225 Metric), RoHS, Tape and Reel	L3	BOUR-CM322522_V	CMP-1747-00008-1	1
5K1 1% 0402(1005)	RES SMD 5.1K OHM 1% 1/16W 0402	R1, R2, R3	RES_0402_imperial	RC0402FR-075K1L	3
2K2 1% 0402(1005)	YAGEO (PHYCOMP) RC0402FR-072K2L SMD Chip Resistor, Thick Film, 2.2 kohm, 50 V, 0402 [1005 Metric], 63 mW, 1%	R4, R5, R6	RES_0402_imperial	RC0402FR-072K2L	3
RC0402FR-0712KL	RES SMD 12K OHM 1% 1/16W 0402	R7	RES_0402_imperial	RC0402FR-0712KL	1
390R 1% 2512(6432)	PANASONIC ELECTRONIC COMPONENTS ERA3AEB391V SMD Chip Resistor, Thin Film, 390 ohm, 75 V, 0603 [1608 Metric], 100 mW, 0.1%, ERA Series	R8	RES_0603_imperial	ERA3AEB391V	1
220R 1% 0603(1608)	Res Thin Film 0603 220 Ohm 0.1% 1/10W ±25ppm/C Molded SMD Punched Carrier T/R	R9, R10, R11, R12, R13, R14, R15, R16, R19	RES_0603_imperial	ERA-3AEB221V	9
4K7 1% 0603(1608)	Res Thin Film 0603 4.7K Ohm 0.1% 0.1W(1/10W) ±25ppm/C Molded SMD Automotive Punched T/R	R17, R18, R26	RES_0603_imperial	ERA-3AEB472V	3
820K 1% 0603(1608)	RESISTOR, 0603, 0.1W, 1%, 820K	R20, R21	RES_0603_imperial	ERJ-3EKF8203V	2
180K 1% 0603(1608)	RESISTOR, 0603, 180K, 0.1%, 0.1W	R22, R23, R24	RES_0603_imperial	ERA-3AEB184V	3
56K 1% 0603(1608)	PANASONIC ELECTRONIC COMPONENTS ERJ3EKF5602V. SMD Chip Resistor, Thick Film, 56 kohm, 75 V, 0603 [1608 Metric], 100 mW, 1%, ERJ3E Series	R25	RES_0603_imperial	ERJ-3EKF5602V	1
LCMXO2-7000HE-4TG144C	MachXO2 High Performance CPLD with 6864 LUTs, 1.2V, 144-pin TQFP, Speed Grade-4, Commercial Grade, Halogen Free (RoHS)	U1	TQFP144_L	CMP-0111-00327-1	1
FT2232HL	Dual High Speed USB to Multipurpose UART / FIFO IC 3 to 3.6 V, -40 to 85 degC, 64- Pin LQFP, RoHS	U2	FTDI-LQFP-64_L	CMP-2000-06287-1	1
93LCS56-XSN	Imported	U3	SOIC8-N_MC	93LCS56-XSN	1
TPS62290DRVR	Buck Step Down Regulator with 2.3 to 6 V Input and 0.6 to 6 V Output, -40 to 85 degC, 6-Pin SON (DRV), Green (RoHS & no Sb/Br)	U4, U5	DRV6-1600X1000TP	CMP-0323-00361-1	2
MIC2288YD5	Imported	U6	TSOT-23-5_D5	MIC2288YD5	1
7M-12.000MAAJ-T	12MHz ±30ppm Crystal 18pF 100 Ohm -20°C ~ 70°C Surface Mount 4-SMD, No Lead (DFN, LCC)	X1	7M-12.000MAAJ-T	7M-12.000MAAJ-T	1

Design Rules Verification Report

Filename : C:\Users\fredv\Documents\Hardware\Projects\LCD-Controller\LCD-Controller.PcbDoc

Warnings 0
Rule Violations 0
Waived Violations 11

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.13mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.15mm) (Max=1mm) (Preferred=0.254mm) (All)	0
Width Constraint (Min=0.25mm) (Max=1.5mm) (Preferred=1mm) (InNetClass('Power'))	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All),(All)	0
Silk To Solder Mask (Clearance=0mm) (IsPad),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0.1mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	0

Waived Violations	
Board Clearance Constraint (Gap=0mm) (All)	11
Total	11

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0mm < 0.15mm) Between Board Edge And Text "DINT" (53.7mm,0.15mm) on Top Overlay Waived by
Board Outline Clearance(Outline Edge): (0mm < 0.15mm) Between Board Edge And Text "DRST" (55.9mm,0.15mm) on Top Overlay Waived by
Board Outline Clearance(Outline Edge): (0.09mm < 0.15mm) Between Board Edge And Track (108.1mm,0.19mm)(108.1mm,15.43mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.15mm) Between Board Edge And Track (113.588mm,24.855mm)(114.4mm,24.855mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.15mm) Between Board Edge And Track (113.588mm,32.345mm)(114.4mm,32.345mm) on Top
Board Outline Clearance(Outline Edge): (Collision < 0.15mm) Between Board Edge And Track (114.4mm,24.855mm)(114.4mm,32.345mm) on Top
Board Outline Clearance(Outline Edge): (0.103mm < 0.15mm) Between Board Edge And Track (91.2mm,0.23mm)(91.2mm,7.7mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.103mm < 0.15mm) Between Board Edge And Track (91.2mm,0.23mm)(96.9mm,0.23mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.103mm < 0.15mm) Between Board Edge And Track (94.3mm,0.23mm)(94.3mm,7.7mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.09mm < 0.15mm) Between Board Edge And Track (96.9mm,0.19mm)(108.1mm,0.19mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.09mm < 0.15mm) Between Board Edge And Track (96.9mm,0.19mm)(96.9mm,15.43mm) on Top Overlay