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ADPLL Design and Implementation on FPGA

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Abstract:- **This paper presents the ADPLL design using Verilog and its implementation on FPGA. ADPLL is designed using Verilog HDL. Xilinx ISE 10.1 Simulator is used for simulating Verilog Code.This paper gives details of the basic blocks of an ADPLL. In this paper, implementation of ADPLL is described in detail. Its simulation results using Xilinx are also discussed. It also presents the FPGA implementation of ADPLL design on Xilinx vertex5 xc5vlx110t chip and its results. The ADPLL is designed of 200 kHz central frequency. The operational frequency range of ADPLL is 189 Hz to 215 kHz, which is lock range of the design.**

Keywords- ***DCO; ADPLL; FPGA; Loop Filter; Phase Detector***

I. INTRODUCTION

The PLL is a self-correcting control system in which one signal chases another signal.PLL has four types i). Linear PLL ii).Digital Phase Locked Loop iii).All Digital Phase Locked Loop iv). Software PLL (SPLL).ADPLL takes input as only digital signals. Due to digital signal as input signal ADPLL offers various advantages over the different types of PLLs.
Beginning of all digital phase-locked loops (ADPLL) started in 1980[1]. A new Digitally Controlled Oscillator (DCO) has been developed by researchers to obtain good phase and frequency error that was not implemented with 74HC297 IC[3], [2], [4].In 2006 double edge triggered D flip-flop as phase detector was proposed [5] .This design reduced 33% of power dissipation. In 2008 digital FM demodulator was proposed [6]. It was designed by VHDL. In 2009 frequency modulated modem was implemented on field programmable array (FPGA) [7]. In 2010 a field programmable array based linear ADPLL was proposed. This ADPLL used FPGA for implementation [8] .Recently an all-digital phase-locked loop (ADPLL) having a fault detection of the input reference signal was modeled using Verilog hardware descriptive language (HDL) [9].Clock recovery is most important use of ADPLL [10]. Data may affect with noise that noise is called ripple. For reducing ripple in the ADPLL circuit, ripple reduction techniques are also reported in different research papers [3], [11], [10], [12]. An example of the ADPLL is implemented [3]. All the components of ADPLL are fully digital. The ADPLL is designed using Verilog HDL. HDL is very flexible for modifying the design parameters.

ADPLL has many applications in digital communication. An example of it is FSK decoder. It transfers digital signals.FSK decoder transmits serial binary data by using two different frequency. Logic 0 presents one of frequency and logic 1 presents other frequency. FSK decoder is implemented using the 74HC/HCT297 ADPLL IC which has the operating frequency range of 2.1 kHz to 2.7 kHz and this decoder is used as FSK transmitter [3]. A frequency modulated receiving system based on ADPLL was proposed in 2005[13]. In 1987 FSK decoder is implemented for higher frequency range by using IC NE564 [14] .By using an IC SM8223AP FSK decoder is developed [15] .This IC is applicable in telephones, fax machines and modems.FSK decoder can be used as modulator which is useful in digital keying [16]. FSK modem can be used for packet communication [17] .FSK is useful in symbol recovery circuit [18].

The paper is divided in the several sections as follows: Section II provides the ADPLL design and describes all the building blocks of the ADPLL. Section III gives the ADPLL design using Verilog and its simulation results. Section IV shows the FPGA implementation of the ADPLL and its results and, finally the last section V provides the conclusion.

II. ADPLL DESIGN

ADPLL is a negative feedback control system and it consists of a phase detector, loop filter and digitally controlled oscillator. It contains all the digital blocks. In the feedback path a divide-by-N counter is also added in the feedback path to provide a frequency synthesis function. The signal could be single or combination of parallel digital signals. Fig. 1 shows abasic structure of an ADPLL [3, 19].

The aim of the ADPLL is to interlace the phase input v1 and output v2' and also the frequency. To reduce

the difference among two signals phase detector is used. For removing noise loop filter is used. Finally, the digitally-controlled oscillator (DCO) gets the signals from LF and makes closer to the input signal. To realize an ADPLL, existing elements must be digital circuits. There are some advantages: No off-chip components and Insensitive to technology.

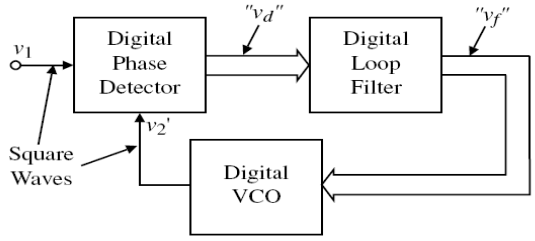

Fig.1: General Block Diagram of ADPLL

A. Building Blocks in an ADPLL

From the basic operation of an ADPLL, three important building blocks are needed to provide phase locking, namely a phase detector, loop filter and digitally-controlled oscillator. Most widely used implementation methods for the building blocks are investigated in this section.

1. Phase Detector

It is also called phase comparator. It compares between input and DCO output signal. Output depends upon the phase error. Output signal contains low frequency and higher frequency component.

EXOR Gate Phase Detector

For ADPLL design EXOR phase detector is used. It compares the reference and DCO signal.

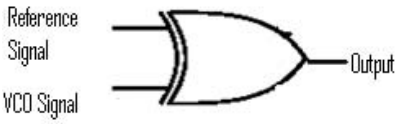

Fig.2:EXOR Gate Phase Detector

Disadvantages of this are it has phase limitation [-90,+90] degrees and it does not senses edges signal edges. Fig.3 shows the "locked" state [8], [11], [13].

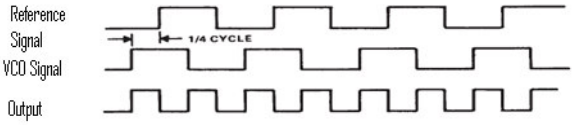

Fig.3: Waveforms of XOR Gate Phase Detector

2. Loop Filter

It is nothing but an integrator. For our ADPLL implementation K counter loop filter is used.

K Counter Loop Filter

K counter loop filter is very important loop filter.It always works with JK or EXOR phase detector. It has two counters.Both are independent .One is called Up and other is Down counter. But both counts in upward direction. Counter has modulus K.

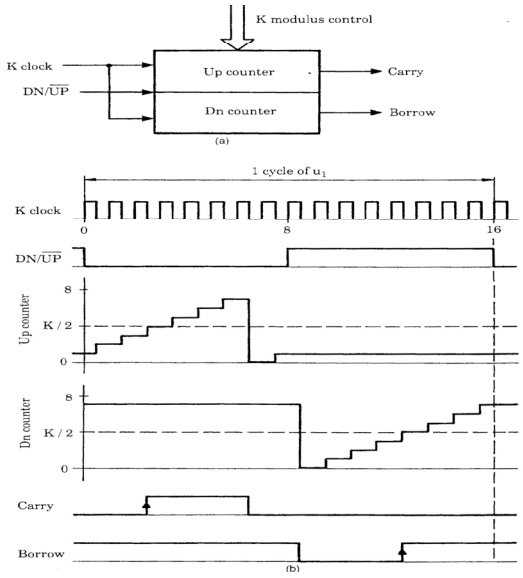

Fig. 4: K Counter Loop Filter (a) Block Diagram (b) Corresponding waveforms.

So counter contents has range from 0 to K-1.Couter clock frequency is M times multiple of center frequency. M has typical values of 8, 16, 32….Down counter is enabled when DN/UP has logic high and up counter is enabled when this logic has low value. When contents exceed K-1 both counters reset. "Carry" is MSB of the Up counter .The "borrow" signal is MSB of the Down counter. When Up-counter stored data ≥ K/2 "carry" is high .When down counter stored data≥ K/2 "borrow" is high. Frequency of DCO is controlled by positive edges of the signal [8], [11], [13].

3. Digital Controlled Oscillator

Digitally Controlled oscillators are nothing but a modified oscillator .Depending upon output of the loop filter they change their frequency. Increment Decrement counter is used for our ADPLL design.

Increment-Decrement Counter

Increment-Decrement Counter consists of two blocks. Carry is assigned to DECR input and Borrow is assigned to INCR input. ID counter with ÷ N

counter for again dividing the OUT. Clock of increment-decrement counter is 2N times multiple of center frequency. Fig. 5 gives overall structure [8], [11], [13].

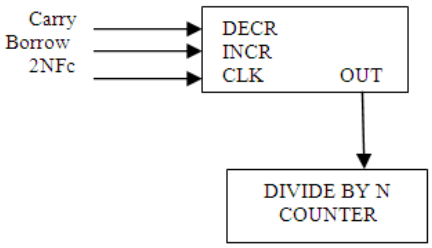

Fig. 5: Increment-Decrement counters

If no Carries and Borrows are present then ID counter divides OUT by 2 on the positive edges of ID clock. The logical function for ID counter is given by

ID out = (NOT (ID clock) AND (NOT (togg1e-FF))

If carry is present then half cycle is added and if borrow is present then half cycle is removed from OUT. Here out is output of increment-decrement counter. The adjusted waveform is shown below.

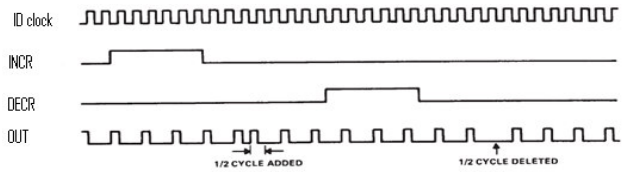

Fig. 6: Waveforms of Increment-decrement counter

III. ADPLL DESIGN USING VERILOG

ADPLL components are Phase Detectors (PDs), Loop Filters (LFs) and Digital Controlled Oscillators (DCOs). Based on all these components we can make various types of ADPLLs. For designing ADPLL, Verilog hardware description language is used. It is simulated in ISE Xilinx 10.1 and then this circuit is implemented into FPGA vertex5 kit.

A. ADPLL Design

All basic building blocks of ADPLL i.e. Phase Detector (PD), Loop Filter (LF) and Digital Controlled Oscillator (DCO) are designed using Verilog (HDL). EXOR gate is used as PD. Output of EXOR PD is fed into K counter. This signal is represented by Dn/up. K counter clock is Kclk signal. Kclk is M time multiple of center frequency. K counter contains two independent counter named as up counter and down counter. The operation of K counter depends upon Dn/up signal. If this signal is low then up counter is active and down counter becomes inactive. In other case when this signal is high then down counter is active and up counter becomes inactive. Outputs of K counter are carry and borrow pulses. Carry and borrow are MSB of the up and down counter respectively. Carry pulse is fed into INC input of ID counter .Whereas borrow pulse is fed into DEC input of ID counter .Output of ID counter is ID_{out} .In general one carry pulse adds half cycle to ID_{out} and one borrow pulse delete half cycle to ID_{out} signal.ID clock is 2N time multiples of center frequency. Output of ID counter (ID_{out}) is fed into divide by N counter, which is the last stage of DCO. $ID_{out}$is used as clock pulses for divide by N counter. For verifying the design test bench has been created and simulation is done. For designing and simulating Xilinx ISE 10.1 tool is used. A diagram of designed and implemented ADPLL [8] is shown in the Fig.7. Also M=2N, so both clock frequency are taken from the same source. The important parameters used for designing ADPLL are listed in the table 1.Table 2 gives synthesis details of the designed ADPLL.

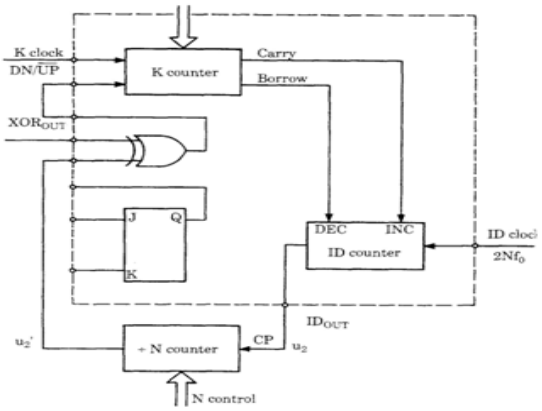

Fig.7: ADPLL circuit diagram

TABLE I: PARAMETERS DETAIL OF DESIGNED ADPLL

Parameters	ADPLL Design
K	8
M	16
N	8
Center Frequency(f_o)	200 kHz

TABLE II: SYNTHESIS DETAILS OF THE DESIGNED ADPLL

Parameters	ADPLL Design
Power Dissipation(watt)	0.561
Combinational Delay (nsec)	12.997
IO Utilization *(bonded IOB)*	4/480
Slice Logic Utilization*(Slice LUTs)*	26/28800
Slice Logic Distribution *(unused Flip Flops)*	7

B. ADPLL Simulation Results

The simulation is done for finding out the hold range. The simulation output of ADPLL in the locked condition at frequency of 189 kHz is shown in Fig.8. tc represents DCO's output at the last stage, in this Fig..tc1 represents input signal. dn/up signal is represented by updwn. K counter clock frequency is given by kclk signal.ID counter output stage is given by idout signal.

Fig. 8 shows that frequency of DCO and input are same and very less phase error among them which is satisfying the condition for locking. Fig. 3 shows simulated waveform of the design for the unlocked case. In this fig tc and tc1 represents DCO and input signal. dn/up signal is represented by updwn. The input frequency of the ADPLL is taken as 215 kHz. Fig. 9 represents the conditions for unlocking. Simulation is performed for different frequencies also. The hold range of the designed ADPLL is 189 kHz-214 kHz.

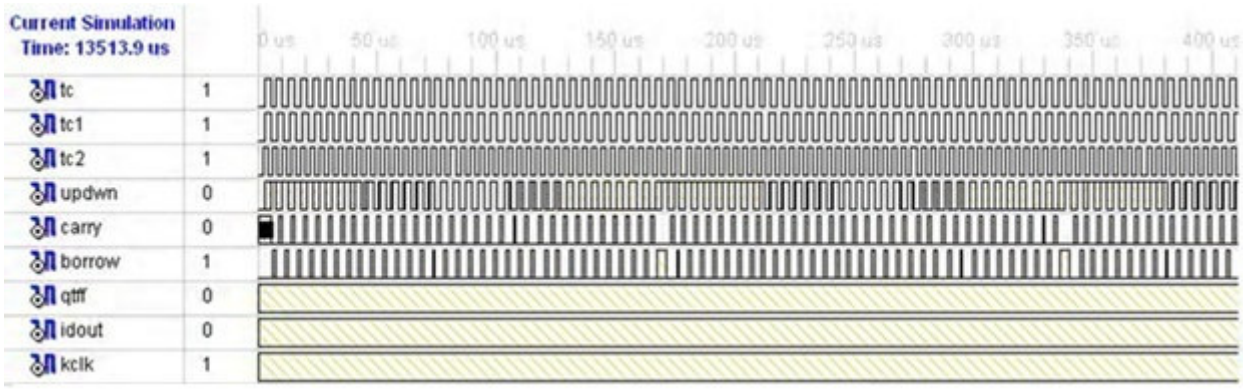

Fig.8: Simulation output of the ADPLL in locked condition at f = 189 kHz

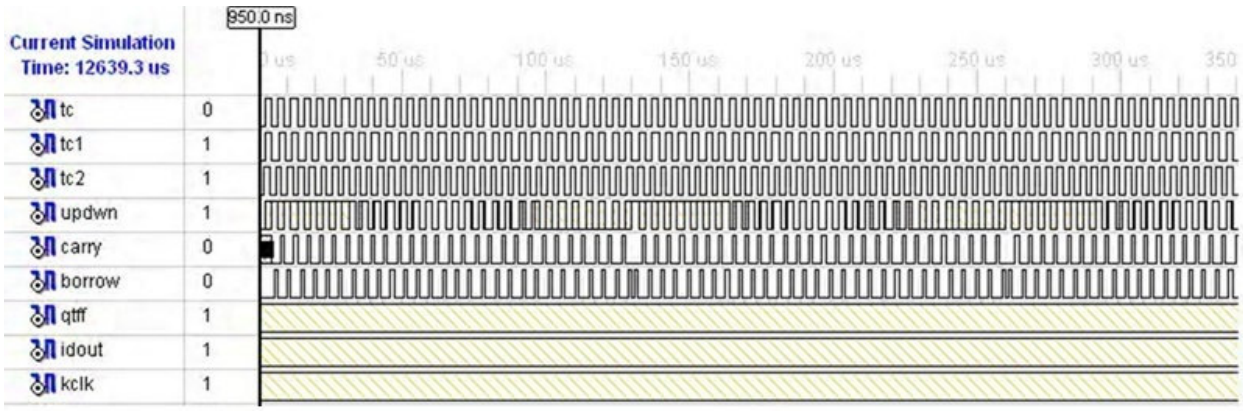

Fig.9: Simulation output of the ADPLL in unlocked condition at f = 215 kHz

IV. FPGA IMPLEMENTATION OF ADPLL

The ADPLL has been implemented into Xilinx vertex5 xc5vlx110t chip. Chip is having 69,120 LUT's. A maximum of 640 IO's are available65 nm CMOS technology based FPGA is taken. FPGA system clock is 100MHz.Pin F34 is used for input signal. Pin G33 is for divide by N counter output. System clock is given by pin AH17. Reset and enable signal are given by AC25, AC24 pin. The FPGA pin description for implementation of ADPLL is given in Table 2.

Table2: FPGA Pin Description

Notation	Description	Pin-assignment	I/O
U1	Original signal	F34	Input
U2	Phase-locked signal	G33	Output
clk	Module clk	AH15	Input
reset	Reset signal	AC25	Input
enable	Enable signal	AC24	Input

A. *FPGA Implementation Results*

The ADPLL designedhere, is used for high frequency applications. It offers better locking among reference signal and DCO signal. The hold range of design is from 189kHz- 215 kHz after simulating ADPLL in Xilinx software.After implementing it on FPGA kit,the hold range comes out to be 194 kHz – 215 kHz.Fig.10 shows the FPGA output for locked case. Fig.11 shows the FPGA output for unlocked case. For showing relation between signals digital phosphor oscilloscope is used. Digital Phosphor Oscilloscope (DPO) having 500 MHz frequency capturing capability. For capturing the output Tektronix TDS 305 4B DPO is used.

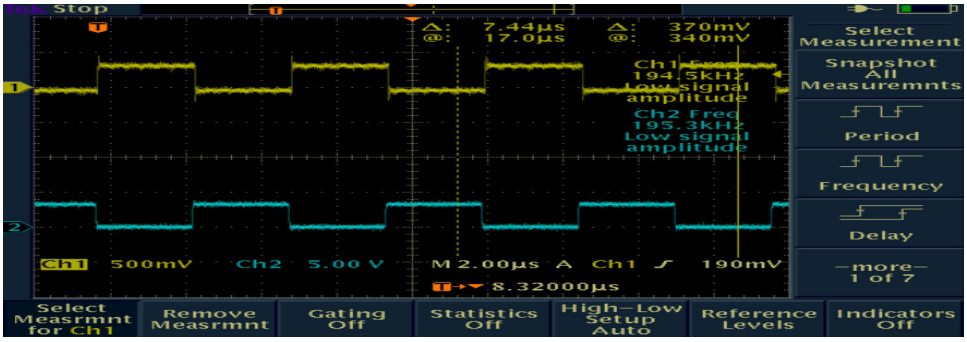

Fig.10: FPGA output of the ADPLL in locked condition at f = 194 kHz

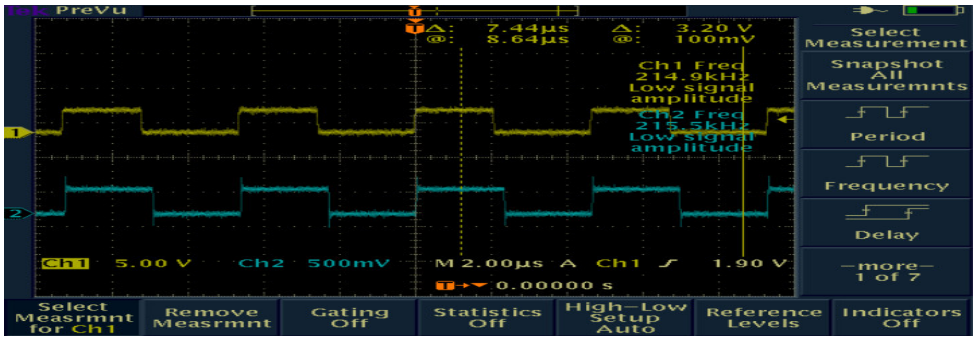

Fig.11: FPGA output of the ADPLL in unlocked condition at f = 215 kHz

V. CONCLUSION

This paper discusses the ADPLL design using Verilog HDL and its simulation in ISE tool CAD Xilinx 10.1. It also presents the FPGA implementation in detail. The ADPLL blocks used for the design are also given here. This PLL is designed for the centre frequency of 200 kHz and its operating frequency range of ADPLL is 189 kHz to 215 kHz, which is the lock range of the design. It is successfully implemented on Xilinx vertex5 xc5vlx110t FPGA kit then its measurements results are also discussed.

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