A Virtual Integration Platform for 2D and 3D IC Design Space Exploration

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***Abstract*—In order to compare the costs and benefits of 2D and 3DIC technologies, an integrated virtual platform for 3DIC system evaluation and design space exploration is developed. The virtual platform is implemented in MATLAB, and is composed of several simulation modules, including a compact 3DIC wire length distribution, a wire pitch and repeater insertion module, a 2D and 3DIC power supply noise estimation module, and a finite difference thermal simulator. The virtual platform is validated against published data for several commercial 2D processors at the 65nm, 45nm, and 32nm nodes. In order to quantify the benefits both 2D and 3D integration approaches, a 32nm CPU core is modeled and the impact of several technology parameters, including interlayer dielectric (ILD) material, on-chip wire material, die thickness, and cooling solution are explored. 3D integration is shown to provide a significant power reduction for the 32nm test case, but more aggressive cooling solutions must be employed to maintain the same clock frequency, due to the increased areal power density of the 3D CPU.**

***Index Terms*—Three-dimensional integrated circuits, integrated circuit modeling, integrated circuit interconnections, power dissipation.**

I. Introduction

ECONOMIC and physical challenges to conventional 2D scaling are driving interest in 3D integration, but uncertainty regarding the fabrication costs and system-level tradeoffs of 3D integration complicate 3DIC design. Projections of 3DIC cost and performance are further complicated by the strongly-coupled nature of communication, power delivery, and thermal management in 3DICs. Additionally, the 3DIC design space is complex, as 3DIC design encompasses a broad spectrum of possible design choices and integration methodologies, ranging from 2.5D interposer-based integration all the way to finely-grained monolithic 3DICs, as shown in Fig. 1, each with unique costs and strengths.

Additionally, different technologies must be evaluated for use in both 2D and 3DICs. Low-k dielectrics can be used to reduce the parasitic capacitances in the wiring stack, simultaneously improving RC delay and reducing the power consumption of the wiring network. Alternate wiring materials are also being considered to improve the RC delay of on-chip interconnects, as well as to reduce the risk of electromigration failures. Fluidic cooling can be used to mitigate the thermal challenges in high performance 2D and 3D ICs. In order to understand the 3D design space, and to decide when a 3D system might have advantages over a 2D system, all of these factors must be modeled simultaneously.

In order to better understand the tradeoffs inherent in 3DIC design, we present an integrated virtual platform for 3DIC evaluation to enable rapid exploration of the 3DIC design space. The virtual platform consists of several simulation modules specially tailored for 3DICs, described in Section II, which have been interconnected to simultaneously explore the signal, power, and thermal behavior of a 3D or 2D system. In order to understand the impact of 3D design on signaling, a novel compact stochastic wire length model has been developed, which accounts for the TSV-induced displacement of logic gates in a 3DIC [1]. Simple models for wire pitch determination and repeater insertion are used to develop a complete picture of the on-chip signaling network [2], [3]. The 3DIC power delivery network is also modeled to determine the maximum simultaneous switching noise in the system, and to understand how many TSVs must be used for power delivery. A multiscale finite difference thermal module is also included, which rapidly and accurately determines the thermal profile of each layer in a 3D stack. All of the models can be applied equally well to 2D ICs, allowing for direct comparison of the costs and benefits of 3D integration and other more conventional technological improvements.

To ensure the reliability of the virtual platform, its predictions are validated against published data for commercial processors in Section III. The virtual platform is used to investigate the impacts of advanced technologies and integration methodologies on a 32nm Sandy Bridge i7 processing core in Sections IV and V. Specifically, the impacts of interlayer dielectric material, wire material, and 2D vs 3D integration on the power consumption, power supply noise, and number of metal layers required for routing are considered.

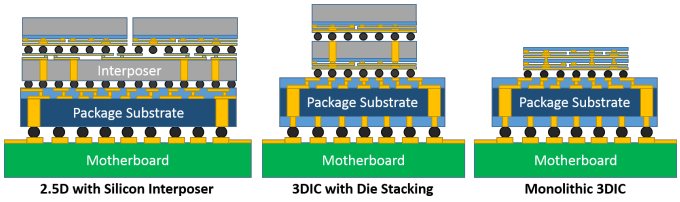

Fig. 1. There are many potential configurations for 3DICs, each with their own costs and advantages. Designers must manage the complexity of the 3DIC design space in order to achieve higher performance and lower cost systems.

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II. Virtual Design Platform

The virtual platform consists of the following:

1) 3D wire length distribution which properly accounts for TSV area
2) Metal layer pitch determination algorithms capable of handling alternate wiring materials
3) An optimal repeater insertion scheme
4) Power supply noise models which account for power delivery in 3DICs
5) A finite difference thermal module for analyzing the thermal impacts of 3D integration

The overall execution flow is shown in Fig. 2. The 3DIC simulation platform can be used to compare the properties of 2D and 3D chips. Currently, the interconnections between logic blocks are not modeled when simulating heterogeneous (SoC-like) 3D stacks, which must be taken into account when simulating such systems. In order to better predict the performance of 3D SoCs, the method of [4] can be used to homogenize a heterogeneous system.

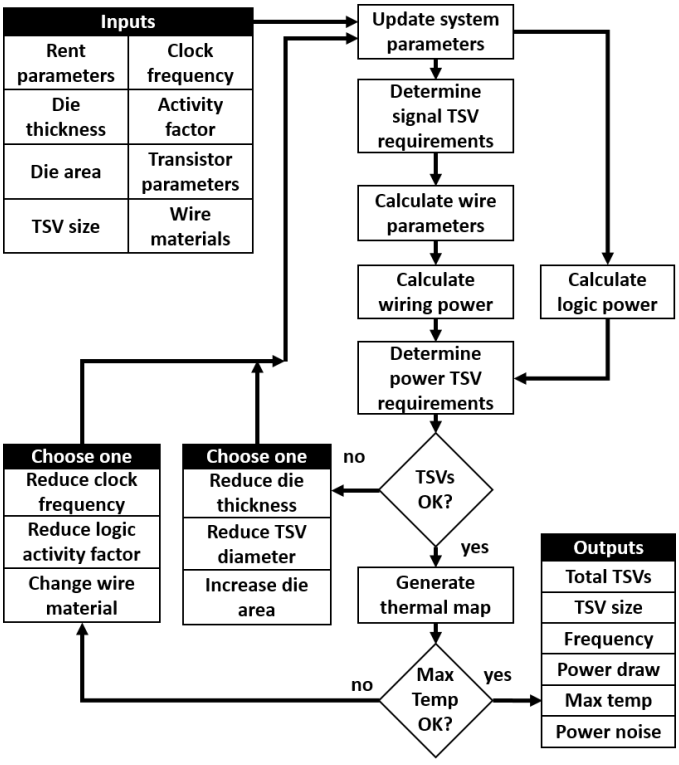

Fig. 2. Block diagram of the virtual platform execution flow.

A. Interconnect modeling

Stochastic wire length distributions have been shown to be effective tools for the rapid prediction of interconnect properties in 2D and 3D ICs [2], [5]–[8]. Efforts have been made to extend 2D wire length distributions to 3DICs [9]–[11], but until recently the impact of TSV diameter on the wire length distribution was difficult to capture. We recently developed a compact model for the wire length distribution in 3DICs which properly accounts for the displacement of logic gates by TSVs [1], which has been integrated into the virtual platform.

Stochastic wire length distributions determine the number of wires of a particular length as

$$I_{idf}(l) = M(l)P_c(l) \tag{1}$$

where $M(l)$ is the number of gate pairs separated by length l, and $P_c(l)$ is the probability that two gates separated by length l will be connected. The general method of determining M and P in 2D ICs is laid out in [5]. The method was extended to consider 3DICs in [9], [10], but the impact of TSV-induced gate blockage was not considered until [11] introduced a modified form of M which accounted for logic displacement, but required brute-force calculation of the correction terms. This work uses expressions for M and P from [10] with a compact correction to M to account for TSV-induced gate displacement [1].

For a symmetric square chip, with a periodic square array of TSVs, the corrected gate pair function is [1]:

$$M_t^*(l) \cong M_t^o(l, N_s) - 2g * g + N_{tsv} M_t^0(l, N = w_{tsv}^2) \tag{2}$$

where M_t^o is the 2D gate pair separation function described in [10], g is the 1D inverse cumulative distribution of *potentially* forbidden gate locations [1], N_{tsv} is the number of TSVs in the logic tier of interest, N_s is the number of logic gates on the tier of interest, w_{tsv} is the TSV width, and l is the grid distance between two gates.

By substituting Eq. (2) for the 2D gate placement function in [10], the impact of TSV-induced logic displacement can be modeled. The wire pitch and number of metal layers are determined using a bottom-up wire scaling technique [2], and an optimal repeater insertion scheme is used to determine the size and number of repeaters required to meet timing constraints [3].

B. Material considerations

As interconnect dimensions continue to scale, the properties of wiring materials have begun to diverge from their bulk values. Surface scattering and grain boundary scattering greatly enhance the resistivity of nanoscale copper wires [12]. In order to capture the impact of these effects on wire resistivity, we use a combined Mayadas-Shatzke and Fuchs-Sondheimer (MS+FS) model [12]–[15], with specularity of 0.55 and backscattering probability of 0.43 [12]. In all cases, the grain size is approximated as the smallest dimension of the wire under consideration.

C. Power supply noise modeling

Power supply noise must be suppressed to ensure reliable system operation, but power delivery in 3DICs is complicated by the limited area available for routing power interconnects between tiers. We use the 3DIC power supply network models developed in [16], [17] to determine the maximum power supply noise in the 3D stack and the number of TSVs required for power delivery.

D. Thermal modeling

Thermal issues are one of the greatest challenges in 3DIC design. In order to design a thermally robust 3D system, the relationships between device technology, system performance area constraints, and packaging materials and technology must be explored. To that end, we utilize a fast and accurate finite difference thermal model.

The heat transfer equation is

$$\nabla \left(K(x,y,z) \cdot \nabla \left(T(x,y,z) \right) \right) = P(x,y,z) \tag{3}$$

where K and T denote thermal conductivity and temperature, respectively, and P is the power excitation. Following the scheme of [18], we discretize the heat transfer equation as

$$\begin{aligned} &\frac{T_{i,j,k} - T_{i-1,j,k}}{\frac{x_1}{k_z l_y l_x}} + \frac{T_{i,j,k} - T_{i+1,j,k}}{\frac{x_2}{k_x l_y l_z}} \\ &+ \frac{T_{i,j,k} - T_{i,j-1,k}}{\frac{y_1}{k_y l_x l_z}} + \frac{T_{i,j,k} - T_{i,j+1,k}}{\frac{y_2}{k_y l_x l_z}} \\ &+ \frac{T_{i,j,k} - T_{i,j,k-1}}{\frac{z_1}{k_z l_x l_z}} + \frac{T_{i,j,k} - T_{i,j,k+1}}{\frac{z_2}{k_z l_x l_z}} = P_{tot} \end{aligned} \tag{4}$$

where $l_x = (x_1 + x_2)/2$, $l_y = (y_1 + y_2)/2$, $l_z = (z_1 + z_2)/2$, and where x_i, y_i, and z_i ($i \in 1, 2$) are the mesh size along the corresponding axis. P is the total power consumption in the volume of interest, shown as the shaded rectangular region in Fig. 3. A similar scheme can be derived for grid points along the boundary of the mesh. In the case that one mesh has multiple materials, we assign the volume-weighted thermal conductivity of the surrounding volume to that grid point.

The accuracy of this finite difference module was assessed in [19], in which the performance of the finite difference scheme was compared against finite element ANSYS models of the same structure. The finite difference model was found to match the ANSYS results with a maximum error of 2.7%.

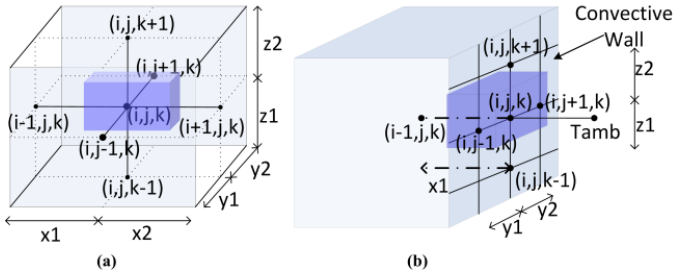

Fig. 3. Finite difference scheme. (a) Points inside the stack. (b) Boundary points at the face of the stack [18].

III. Validation

The virtual platform was validated by comparing its predictions against published data for Intel processors ranging from the 65nm node to the 32nm node [20]–[27]. For each test case, the chip area, number of logic transistors, number of memory transistors, and size and shape of the cores and memory blocks were gathered from published data. Logic cores were simulated with a Rent exponent of 0.6, while memory cores used a value of 0.4 [28].

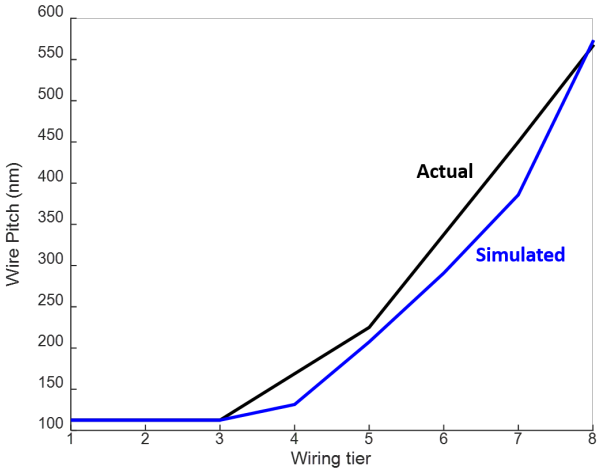

Fig. 4. Actual and expected wire pitch in a Core i7 2700k processor.

The expected wire pitch, number of metal layers, power consumption, and maximum junction temperature generated by the virtual platform have been compared in Table I. The virtual platform shows good agreement with the high level design parameters for processors ranging from 65nm down to 32nm. The wiring algorithms also accurately predict the wire pitch in each level, as shown in Fig. 4.

IV. 2D: Seeking Improvements via Materials Innovation

One path towards increasing system performance is to achieve improvements in the wiring materials. The permittivity of the interlayer dielectric (ILD) material has a strong effect on the parasitic capacitance of the on-chip wires, which in turn determines the RC delay and power consumption of the wiring network. In addition to directly reducing the power required to send signals along the on-chip wires, decreasing the RC delay also reduces the need for power-hungry repeaters.

In order to quantify this effect and to determine the potential of ultra low-k ILD materials, a 32nm Sandy Bridge Core i7 was simulated with a range of different ILD permittivities, ranging from 3.9 (Silicon Dioxide), all the way down to 1 (vacuum). Figure 5 shows that the number of metal layers required to fully route the Sandy Bridge processing core can be reduced from 8 to 6 if the relative dielectric constant of the ILD material can be brought below 1.3. The CPU power

TABLE I
Comparison to Actual Data

Processor	Node	Wiring Tiers Actual	Wiring Tiers Predicted	TDP (W)	Predicted Power (W)
Core 2 Duo E6850	65nm	8	8	65	60.27
Core 2 Duo E8600	45nm	9[2]	8	65	63.62
Core i7 880	45nm	9[2]	7	95	105.56
Core i7 680[1]	32nm	9[2]	6	73	52.74
Core i7 2700k	32nm	9[2]	8	95	91.80

[1] Combined MCM package including 32nm CPU die and 45nm gpu/support die
[2] Includes one global metal layer for power distribution, not modeled here

consumption scales roughly linearly with ILD permittivity, as shown in Fig. 6, and significant power reductions are possible with ultra low-k (ULK) materials. The power reduction comes from both a reduction in wire power, as well as a reduction in the number and size of the repeaters needed to meet timing constraints. While ULK dielectrics may provide one avenue towards reduced power consumption, their manufacture and integration into the wiring stack is challenging, and poses significant reliability concerns. Alternate approaches to reducing wire power consumption will be examined in Section V.

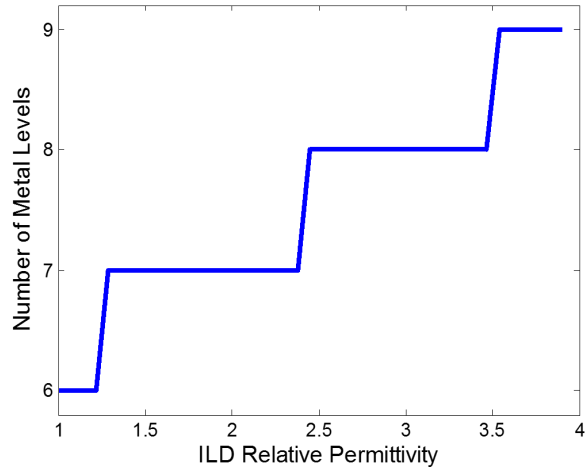

Fig. 5. Impact of interlayer dielectric (ILD) permittivity on the number of metal layers required to route the wires in a Sandy Bridge Core i7 2700k.

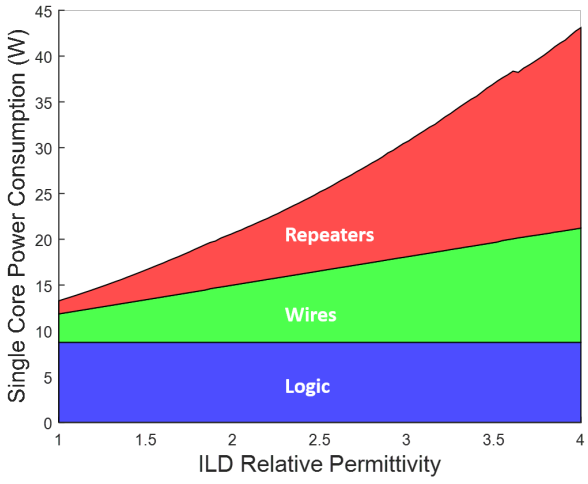

Fig. 6. Impact of interlayer dielectric (ILD) permittivity on the power consumed by wires and repeaters in a Sandy Bridge Core i7 2700k processor core.

The materials used for the wires must be resistant to electromigration. As the critical dimensions of the smallest on-chip wires have decreased, electromigration has become significant concern for system reliability at advanced process nodes [29]–[31]. In order to alleviate electromigration concerns at advanced process nodes, alternate materials may be required, which may have higher resistivities than pure copper, potentially impacting signal performance, power consumption, and the number of metal layers required to fully route a design [32], [33]. It is likely that only the lowest metal levels would utilize alternate wiring materials [34], [35].

To investigate the potential impact of electromigration-resistant metals on wire routing, a hypothetical 7nm Sandy Bridge CPU test case was constructed by scaling the gate pitch, minimum wire pitch, transistor size, and all other lengths in the 32nm Sandy Bridge by a factor of 4.57X (32/7). Two 7nm test cases were considered: *7nm A*, in which all wires are composed of an alternate material, and *7nm B*, in which only wires thinner than 25nm are replaced by the alternate material. The bulk resistivity of the alternate wiring material in both the 32nm and 7nm test cases was swept from 10 Ωnm (slightly lower than bulk Ag), to 60 Ωnm (slightly higher than bulk W). For simplicity, the specularity and reflection parameters of the alternate wiring material are not modified. The results are shown in Fig. 7. Since the lowest metal layers are the most critical for wire routing, small changes at these dimensions can have a large impact on the overall wiring stack. As can be seen in Fig. 7, the use of higher resistivity metals can significantly increase the number of metal levels required for interconnect routing, but this effect can be mitigated by restricting the use of alternate metals to the lowest wiring tiers.

V. 3D: Power Reduction Without Exotic Materials

A. Reducing power consumption

Implementing a design in 3D can greatly reduce the average length of the on-chip interconnects, leading to reductions in the average delay and power consumption of the signaling network [7]. In order to examine the impact of 3D integration on power consumption, a single 18.5mm^2 Sandy Bridge processing core was simulated in different 3D configurations. Unless otherwise noted, we assume a TSV aspect ratio of 20:1, and require that the TSVs use less than 10% of the total die area. Typically, 3DIC designs limit the TSV area to 1% or less to minimize the cannibalization of active area, but we have relaxed that limit here for illustrative purposes. In order to examine the impacts of 3D integration, a single CPU core from a 32nm Sandy Bridge Core i7 2700k is used as a test case throughout this section.

We consider a 3D integration scenario in which logic gates and blocks can be placed on any tier, and in which TSVs are used as point to point interconnects. The core is assumed to be partitioned into N equal pieces, which are then stacked vertically. This configuration is considered in order to illustrate the ultimate limits of 3D integration.

Significant power savings can be obtained by moving to a 3D design, as shown in Fig. 8, though the power reduction comes at the cost of increased areal power density, ultimately placing more stress on the cooling solution. The design implications of the increased power density of 3DICs will be discussed further in Section V-C. It is important to note that 3DICs reduce the power required by on-chip communication, fundamentally improving the overall energy efficiency of the system, as can be seen in Fig. 9.

In order to fully route a 3DIC, space must be allocated on each tier for TSVs. Since TSVs consume space that could

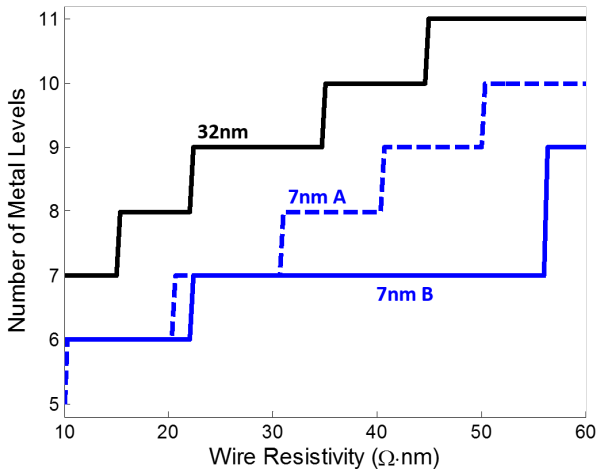

Fig. 7. Impact of wire resistivity on the number of metal layers required to route the wires in a Sandy Bridge CPU. Three cases are considered: a) a 32nm Sandy Bridge core; b) 7nm A, a hypothetical 7nm Sandy Bridge core; and c) 7nm B, in which only wires with width below 25nm are modified.

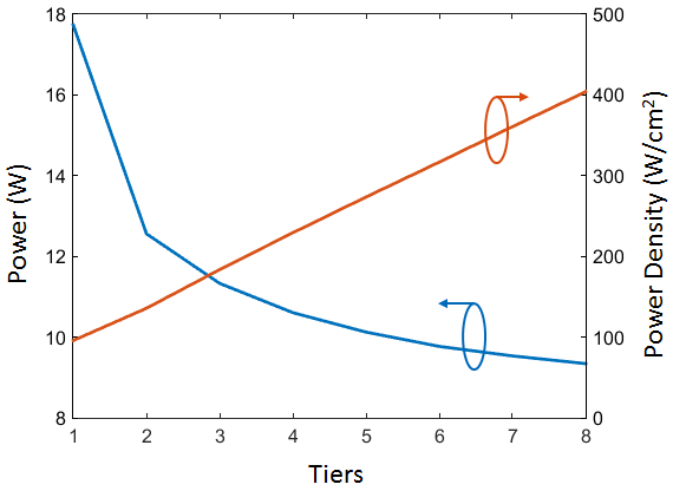

Fig. 8. Impact of block folding on power consumption and power density of a single 32nm Sandy Bridge core.

otherwise be used for logic, it is desirable to minimize the fraction of chip area consumed by TSVs, to avoid unnecessarily increasing the size of each die. In order to minimize the space occupied by TSVs, the TSV aspect ratio can either be increased, directly enabling the use of thinner TSVs, or the die itself can be thinned, to enable the use of low aspect ratio TSVs. Thicker logic tiers are attractive due to their higher mechanical stability, simplifying handling and assembly, but they limit the improvement in average wire length achieved by moving to 3D, since the distance between tiers is greater. TSVs are typically limited to diameters of 5-10μm and aspect ratios between 5-15:1 [36]–[38], with some demonstrations of 20:1 or higher [19], [39], [40].

The impact of die thickness on 3DIC power consumption is examined in Fig. 10. In order to realize the greatest possible power reduction from 3D integration, the active layers should be as thin as possible, to minimize the distance that signals must travel when they are routed between tiers.

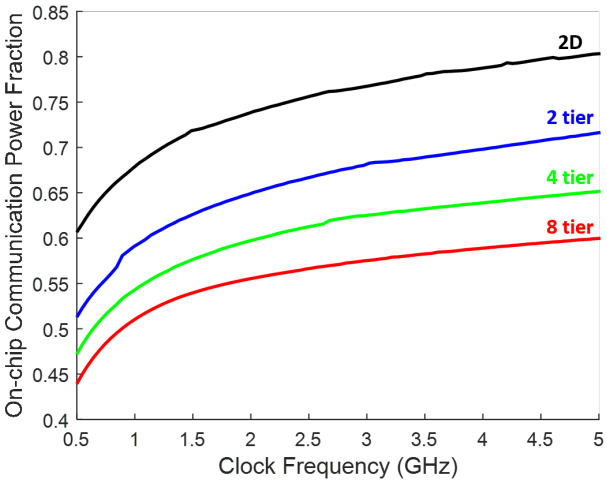

Fig. 9. Fraction of power consumed for on-chip communication as a function of 3D configuration and operating frequency.

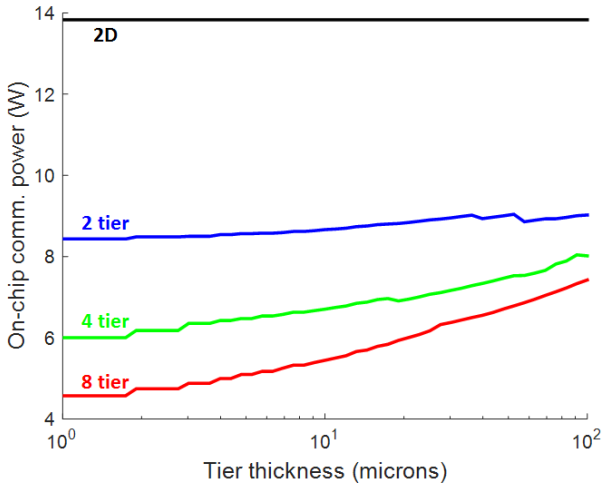

Fig. 10. Impact of die thickness on power consumed by wires and repeaters in a single 32nm Sandy Bridge core implemented in 3D.

B. Power Delivery

In order for an IC to function reliably, the power delivery network must be robust enough to prevent undue fluctuation of the supply voltage [17]. Power delivery becomes more challenging as the power density that must be delivered increases. Power delivery in 3DICs becomes especially challenging, as a high performance 3DIC may have a significantly higher areal power density than an equivalent 2D chip, while simultaneously having less space available for routing power delivery resources. Additionally, in 3DICs power must be delivered to each tier in the stack through TSVs, introducing additional parasitic resistance and inductance into the wiring network.

The most straightforward way to ease the burden on the power network is to reduce the total power consumption of the system. The total power consumption of an IC can be

reduced by moving to a 3D configuration, though the areal power density increases as more tiers are stacked atop one another. As the power density increases, delivering power to all of the tiers of the 3D stack becomes more challenging, and many TSVs may be required to minimize droop in the supply voltage of advanced 3DICs. Silicon area is already a limited resource, and the tradeoff between allocating TSVs for signaling or power delivery must be managed carefully.

The number of power connections to each tier required for stable operation is primarily determined by the maximum power draw of the system, which in turn is strongly dependent upon the interlayer dielectric and the substrate thickness (in 3D configurations). Both 2D and 3D systems benefit from the development of ultralow-k interlayer dielectric materials, and the use of thin substrates in 3D configurations can further reduce the demands on the power supply network.

In order to explore these effects, the Sandy Bridge test case was simulated with several substrate thicknesses and interlayer dielectric permittivities, in order to determine the number of power delivery pads or TSVs needed to reduce the simultaneous switching noise to below 15% of the nominal supply voltage. The results are presented in Fig. 11. For two-tier stacks only a slight increase in power TSVs is observed over the 2D case, but the eight-tier implementation requires roughly an order of magnitude more power connections than the 2D design. The dielectric constant of the ILD material has a strong impact on the power delivery requirements, as it has an outsized impact on the power consumption of the on-chip communication network. The thickness of the 3DIC logic tiers is not a limiting factor for 2-tier designs, but 4- and 8-tier designs can realize nearly as much benefit from extreme die thinning as from the use of ultralow-k dielectrics.

Another method to reduce the power supply noise is to integrate decoupling capacitors onto the die, interposer, or package in order to compensate for the inductance of the power delivery network. While this practice can improve power quality, it also sets up a tradeoff between utilizing die area for logic, decoupling capacitors, and power delivery.

In order to explore this tradeoff, the 32nm Sandy Bridge test case was simulated in several 2D and 3D configurations with varying amounts of silicon area allocated for chip- or interposer-level decoupling capacitors. The power TSV diameter is assumed to be 10 μm and the thickness of each die in the 3D stack is assumed to be 10 μm. As can be seen in Fig. 12, increasing the decoupling capacitance can significantly reduce the number of pads or TSVs required for power delivery. Small area allocations can likely be achieved with on-chip decoupling capacitors, but integrating more than several square millimeters of decoupling capacitors into a 2D or 3D system will likely require the use of either a dedicated capacitor tier, or interposer-based decoupling capacitors. Even with the use of decoupling capacitors, a lower bound on power TSV number is set by the need to keep the current density carried by each TSV low enough to avoid electromigration effects.

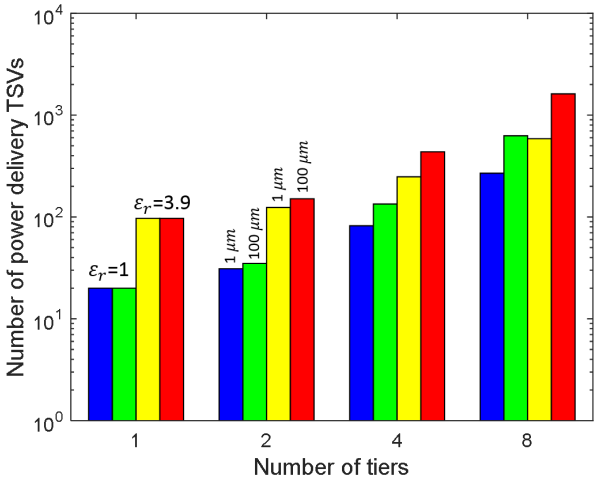

Fig. 11. Impact of interlayer dielectric material, substrate thickness, and degree of 3D integration on power delivery TSV requirements in a hypothetical 3D Sandy Bridge CPU core. In the single-tier (2D) case the required number of power pads is displayed.

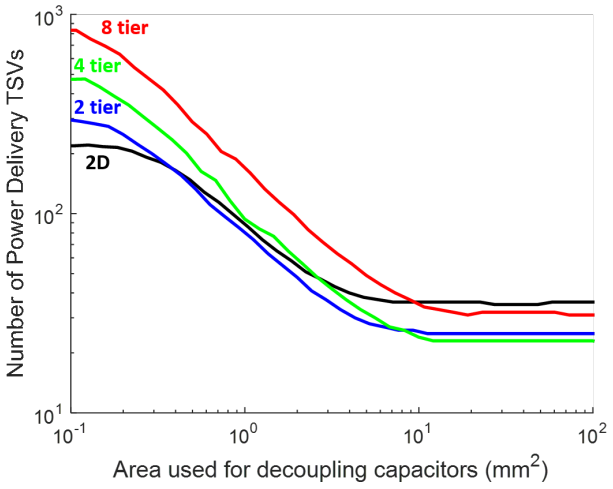

Fig. 12. Power TSV requirements for a single Sandy Bridge core as a function of 3D configuration and area allocated for decoupling capacitors.

C. Thermal management

Thermal management is a key challenge for 3DICs. In the previous sections it has been shown that transforming a 2D design into a 3DIC can yield significant reductions in the average wire length and power consumption of the system, and the use of ultrathin active layers has been shown to further reduce the power consumption of 3DICs. Additionally, low-k dielectrics can be used to decrease the power consumption of the on-chip communication network in both 2D and 3D systems.

While the total power dissipation of an IC is expected to decrease as the device is partitioned into increasing numbers of layers (as shown in Fig. 8), that power reduction is not sufficient to keep the areal power density from increasing as tiers are stacked atop one another, leading to increased stress on the cooling system, and eventually to unreasonable

operating temperatures. Since most conventional 2D ICs are already operating at their thermal limits, a system transformed from 2D to 3D must necessarily either run at a lower operating frequency, or utilize a more aggressive cooling solution.

In order to quantify these tradeoffs, the performance of a single 32nm Sandy Bridge CPU core is examined in several configurations:

1) 2D and 3D configurations are investigated to demonstrate the impact of 3D integration on system performance.
2) The relative permittivity of the ILD material is swept from 1.0 (vacuum) to 3.9 (silicon dioxide) in order to illustrate the impact of ULK materials on system performance
3) Air cooling and microfluidic water cooling are compared in order to demonstrate the benefits of aggressive heat removal techniques. Heat sink parameters are taken from [41]

The CPU core was simulated in each configuration to find the maximum operating frequency which could be maintained while keeping the maximum temperature below 90°C. As can be seen in Fig. 13, the maximum frequency decreases rapidly as the CPU is folded across more and more tiers, as the increased power density of the system increases the strain on the cooling system. The power consumption each core remains essentially constant for the entire range of dielectric constants, as the maximum temperature in the stack is primarily a function of the areal power dissipation of the system and the thermal parameters of the heat sink used. The thermally-limited power draw for each configuration is shown in Fig. 14.

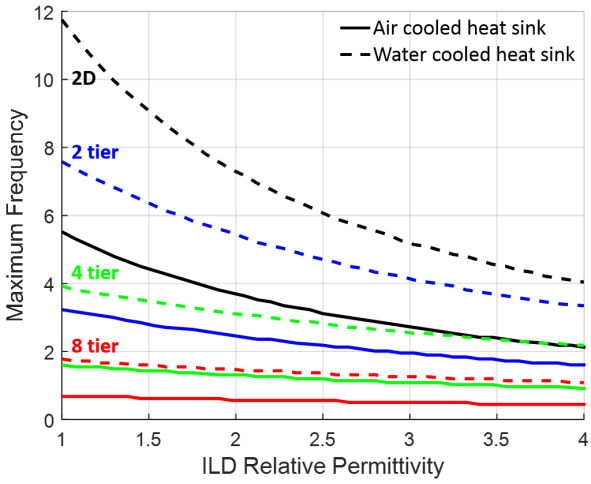

Fig. 13. Maximum operating frequency the Sandy Bridge processing core can achieve while keeping the maximum junction temperature below 90°C. Solid lines correspond to air cooling, and dashed lines correspond to water cooling.

While the water-cooled designs can be run faster than air-cooled designs, they typically sacrifice energy efficiency for performance, as shown in Fig. 15. Water-cooled CPU cores folded over four or more tiers, however, are projected to exhibit equal or better EPC as their air-cooled counterparts, due to the combination of the significant communication power savings benefit from 3D integration and the performance enhancement

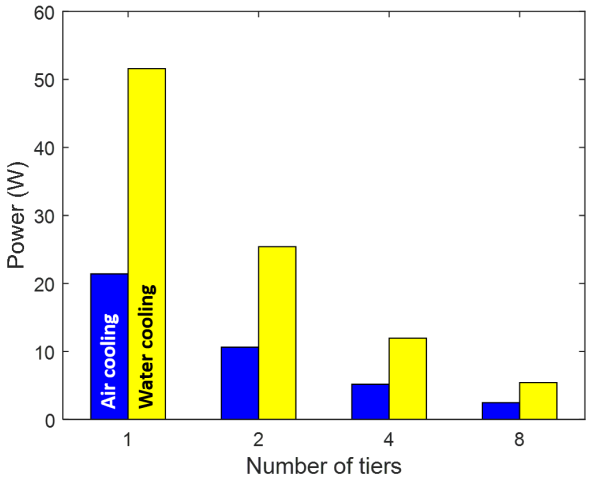

Fig. 14. Maximum power consumption of 2D and 3D Sandy Bridge CPU cores limited to 90°C with air cooling (blue) and water cooling (yellow).

afforded by effective heat removal from the 3D stack. In all cases, reducing the dielectric constant of the ILD material can significantly decrease the power consumption of the CPU core, yielding a significant performance benefit for thermally-limited systems.

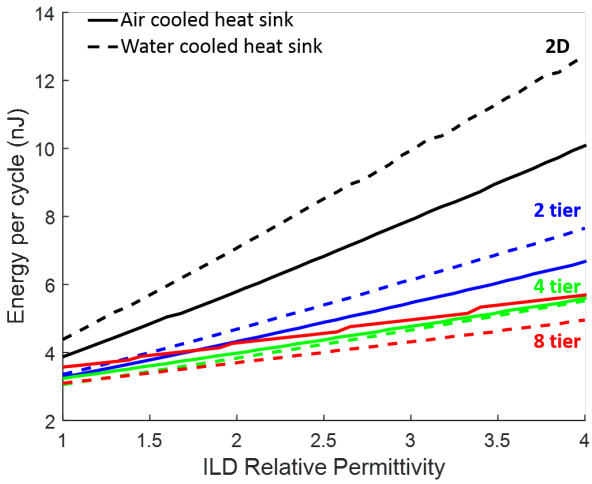

Fig. 15. Energy consumption per clock cycle for 2D and 3D Sandy Bridge CPU cores limited to 90°C with air-cooled (solid lines) and water-cooled (dashed lines) heat sinks.

VI. Conclusion

A virtual integration platform for 2D and 3D IC pathfinding was developed and used to examine the impacts of advanced technologies on system performance. The virtual platform incorporates models for signal delivery, power supply noise, and thermal performance in 2D and 3D ICs, and was validated against wire pitch and power consumption data for recent commercial microprocessors. The impacts of low-k dielectrics, and 3D integration on the performance, power consumption, and power delivery requirements of a 32nm processing core were examined, and a hypothetical 7nm version of the same

processor was simulated to determine the impact of alternate wire materials on the number of metal levels required for signal routing at advanced process nodes.

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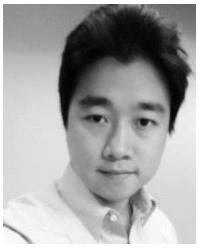

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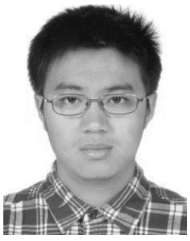

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