Optimal

Signal, Power, Clock and Thermal Interconnect Networks

for High-Performance 2D and 3D Integrated Circuits

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Optimal Signal, Power, Clock and Thermal Interconnect Networks for High-Performance 2D and 3D Integrated Circuits

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SUMMARY

A high-performance 2D or 3D integrated circuit typically has (i) ratio of delay of a 1mm wire to delay of a nMOS transistor > 500, (ii) target impedence of power delivery network < 1mΩ, (iii) clock frequency > 2GHz, and (iv) thermal resistance requirement of heat removal path < 0.6^{o}C/W. This data illustrates the difficulty of obtaining high-quality signal, power, clock and thermal interconnect networks for gigascale 2D and 3D integrated circuits. Specific material, process, circuit, packaging, and architecture solutions to enhance these four types of interconnect networks are proposed and quantitatively evaluated. A microchannel-cooled 3D integrated circuit technology is developed to deal with thermal interconnect problems inherent to stacked dice. The benefits of carbon nanotube technology, improved repeater insertion techniques and parallel processing architectures for signal interconnect networks are evaluated. A circuit technique to periodically reverse current direction in power interconnect networks is proposed. It provides several orders of magnitude improvement in electromigration lifetimes. Methods to control power supply noise and reduce its impact on clock interconnect networks are investigated. Finally, a CAD tool to co-design signal, power, clock and thermal interconnect networks in high-performance 2D and 3D integrated circuits is developed.

CHAPTER 1

INTRODUCTION

The gigascale integration (GSI) era began in 2006 with Intel Corporation releasing an Itanium processor with 1.72 billion transistors [1.1]. The Itanium, like the IBM Power, Sun SPARC, AMD Opteron and Intel Xeon, is a high-performance microprocessor family with yearly system sales greater than $3 billion and profit margins greater than 60% [1.2]. Servers and workstations utilizing these high-performance microprocessors form the backbone of the internet and play an important role in business and scientific computing applications. This research focuses on interconnect issues in such high-performance microprocessors.

1.1. Origin and History of the Problem

Since the invention of the transistor in 1947, interconnects have posed the following three major challenges to solid-state electronics:

1.1.1. The First Interconnect Problem

In the 1950s, semiconductor firms manufactured hundreds of discrete transistors on a wafer. Technicians attired in identical lab coats sat side-by-side, hunched over microscopes that magnified the wafer, so that they could slice apart individual transistors and attach leads and wires to them using tweezers. These transistors were then tested, packaged and shipped to customers. The customers would connect transistors to each other to configure a circuit. This approach was difficult due to several reasons:

- As the number of transistors on a circuit grew, the number of interconnects increased

exponentially. Soldering thousands of connections was difficult, costly and unreliable.

- Connecting discrete transistors together to form a circuit increased size of the built circuit.

Jack Kilby of Texas Instruments and Robert Noyce of Fairchild Semiconductor independently proposed a solution to this interconnect problem: the integrated circuit (IC). Different components of a circuit were now fabricated on the same silicon or germanium substrate. While Kilby had components on the same chip connected together using soldered gold wires [1.3], Noyce connected components together with deposited metal [1.3]. Metal was deposited over oxide layers obtained in accordance with Jean Hoerni's planar process [1.4]. Fig. 1.1 shows the integrated circuits built by Kilby and Noyce.

To summarize, as more and more transistors began to be used in circuits, the number of interconnects grew exponentially. Soldering thousands of interconnects by hand was costly, difficult and unreliable. This can be considered to be the *first interconnect problem*. The integrated circuit was invented to solve this issue.

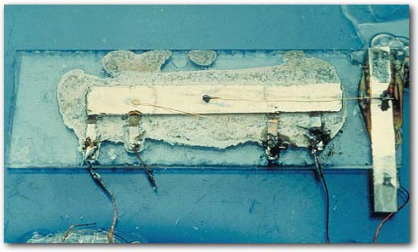
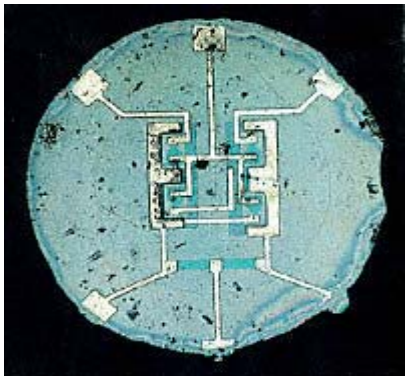
(a)  (b) 

Figure 1.1: (a) Kilby's first IC: an oscillator. (b) Noyce's first IC: a flip-flop.

1.1.2. The Second Interconnect Problem

After the invention of the integrated circuit, more and more transistors were integrated on the same chip. Robert Dennard from IBM gave guidelines for scaling down transistor and interconnect sizes in ICs to gain performance [1.5]. Fig. 1.2 shows tables reproduced from Dennard's paper. As can be observed from Fig. 1.2, transistor performance improved with scaling, while interconnect delay remained the same even when wire lengths were scaled. Furthermore, wires that stretched from one end of an IC to another did not scale in length due to architectural reasons and had delays that increased with scaling. Table 1.1 shows a comparison of the delay of a minimum size nMOS transistor with that of a 1mm long interconnect.

(a)

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	*1/k*
Capacitance C	*1/k*
Voltage V	*1/k*
Current I	*1/k*
Delay time/circuit CV/I	*1/k*

(b)

Parameter	Scaling Factor
Wire length	*k*
Wire resistance	*k*
Wire capacitance	*1/k*
Wire RC delay	*1*

Figure 1.2: Guidelines for scaling (a) transistors, and (b) interconnects.

Several solutions were pursued to tackle this interconnect problem. These include:

- Addition of more layers of metal – While a 0.5μm technology had four metal layers, a 0.18μm technology had six metal layers. Typically, two metal layers were added to a

microprocessor every three years.

- Repeaters – In the mid 1980s, Halil Bakoglu and James Meindl suggested the use of repeaters for interconnects in ICs [1.6]. Wires with repeaters were found to have an order of magnitude improvement in delay.
- Copper interconnects – IBM pioneered the use of copper interconnects in ICs in the 1990s. Copper was found to be about 50% less resistive than aluminum, and also gave important electromigration advantages [1.7].
- Optimal interconnect network design – In the 1990s, Jeffrey Davis and James Meindl derived compact expressions to predict the distribution of wire lengths in an IC [1.8]. They also developed a methodology to estimate optimal wire pitches for different metal layers in a multilevel interconnect network using the stochastic wiring distribution. The resulting optimal wiring networks were found to provide significant performance, die size and power benefits for IC designers.

Table 1.1: Comparison of transistor delay with that of a benchmark 1mm interconnect.

Technology	nMOS CV/I delay	RC delay of 1mm wire
0.6um	17ps	8ps
0.35um	9ps	25ps
0.25um	7ps	50ps
0.18um	5ps	90ps

To summarize, transistor delay improved on scaling integrated circuits, but signal

interconnect delay did not. This issue consumed considerable process and design effort in the 1990s and can be considered the *second interconnect problem*.

1.1.3. The Third Interconnect Problem

Beyond the 0.18um technology generation (circa 2000), new interconnect issues emerged for high-performance microprocessors. Table 1.2 shows that power consumption increased with time and reached 82W at the 0.13um technology node. Heat removal became a serious issue due to power density approaching limits of air-cooling. Thus, thermal interconnects, i.e. interconnects that removed heat from an integrated circuit, became important.

Table 1.2: Microprocessor scaling trends [1.9].

Technology	Frequency	Power	Voltage	Current	Power density
0.6um	100MHz	10W	3.3V	3A	10W/cm^2
0.35um	200MHz	16W	3.3V	5A	15W/cm^2
0.25um	400MHz	17W	2V	9A	20W/cm^2
0.18um	1000MHz	26W	1.7V	15A	25W/cm^2
0.13um	3000MHz	82W	1.5V	55A	55W/cm^2

Table 1.2 indicates that higher power dissipation combined with lower supply voltages caused current requirements of microprocessors to approach 50-100A. It became a challenge to efficiently deliver such high currents from an off-chip DC-DC converter to transistors on the integrated circuit through parasitics of the packaging and on-chip

interconnects. Therefore, power interconnects, i.e. interconnects responsible for delivering power to transistors on the integrated circuit, gained significance.

It can also be observed from Table 1.2 that clock frequency increased exponentially and reached several GHz in a 0.13um technology. For a synchronous IC, a clock signal is typically generated at a central phase-locked loop and has to travel through long interconnect paths to get to hundreds of thousands of flip-flops at the same instant. Distributing such a high frequency synchronous clock became difficult due to across-chip supply voltage fluctuations and manufacturing variations in ever-smaller devices and interconnects. Thus, clock interconnects, i.e. interconnects that delivered a synchronous clock signal to all the flip-flops on the integrated circuit, became important too.

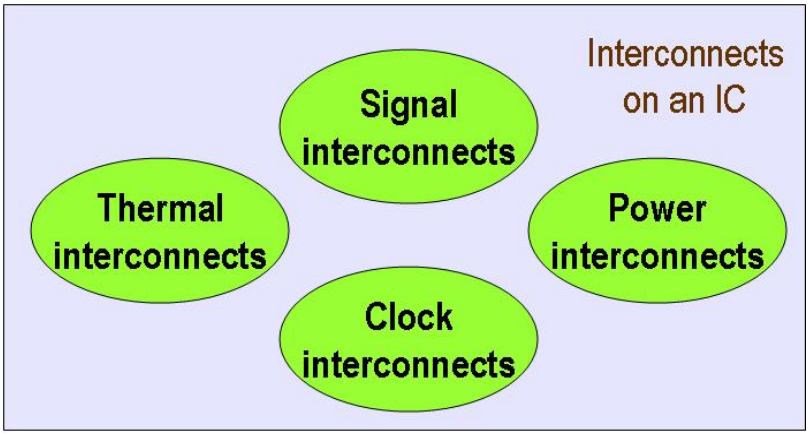


Figure 1.3: A Venn diagram showing four types of interconnect networks in today's ICs.

The above issues with power, clock and thermal interconnects were accompanied by further degradation of signal interconnect networks as described in Table 1.1. Beyond the 0.18um technology generation, one could thus think of high-performance microprocessors having four important types of interconnect networks as shown in Fig. 1.3. This is the

world we live in today. When a new technology was developed in the 1990s, the focus was on it being optimized for signal interconnect networks. Today, however, any new technology needs to be co-optimized for signal, power, clock and thermal interconnect networks. This can be considered the third interconnect problem.

While 2D integrated circuits have been the topic of discussion thus far, 3D stacked integrated circuits are being used today to gain higher packing density and to improve signal interconnect performance. Fig. 1.4 shows a set of DRAM chips stacked on top of each other in a 3D fashion. Interestingly, the idea of 3D stacking is almost 50 years old. The theoretical foundations for this concept were laid by James Early in 1960 [1.10].

Although 3D stacking has been used for low-power applications, high-performance 3D stacked microprocessors have been infeasible largely due to roadblocks associated with thermal and power interconnects. To illustrate this with an example, if two 1V 100W/cm^2 chips are stacked on top of each other, the effective power density to be cooled is 200W/cm^2 compared to 100W/cm^2 when these chips are placed side-by-side. One would also need to deliver 200A/cm^2 to the 3D-IC compared to 100A/ cm^2 when these chips are placed side-by-side. These are serious challenges.

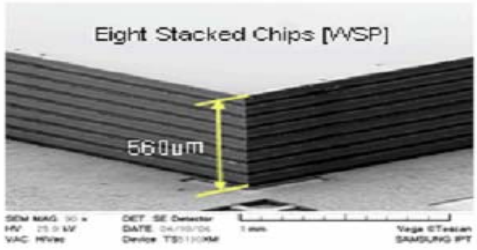


Figure 1.4: Commercially available 3D-DRAMs (Courtesy: Samsung).

To summarize, present-day high-performance 2D and 3D integrated circuits have serious issues with signal, power, clock and thermal interconnects. Each of these interconnect networks needs to be carefully designed to obtain high quality microchips. This can be thought of as the *third interconnect problem*. The objective of this dissertation is to discover techniques to ameliorate the third interconnect problem.

1.2. Dissertation Outline

This manuscript begins by investigating techniques to enhance thermal, signal, power and clock interconnect networks in Chapters 2, 3 and 4. Following this, a CAD tool called IntSim that simulates a GSI chip by co-designing these four types of interconnect networks is presented in Chapter 5. The dissertation concludes with a summary of the major contributions of this research in Chapter 6. Appendices A and B are used to streamline the material in this dissertation and improve its readability.

CHAPTER 2

THERMAL INTERCONNECT NETWORKS

CMOS scaling over the past twenty years has been accompanied with a tremendous increase in power densities. This is depicted in Fig. 2.1. In fact, power densities of today's 2D microprocessors are so high that they require designers to limit performance to use standard air cooling technology [2.2]. Three dimensional stacking of high-performance microprocessors has also been difficult due to power density limitations [2.3]. Thus, thermal interconnect networks are crucial to high-performance 2D and 3D integrated circuits.

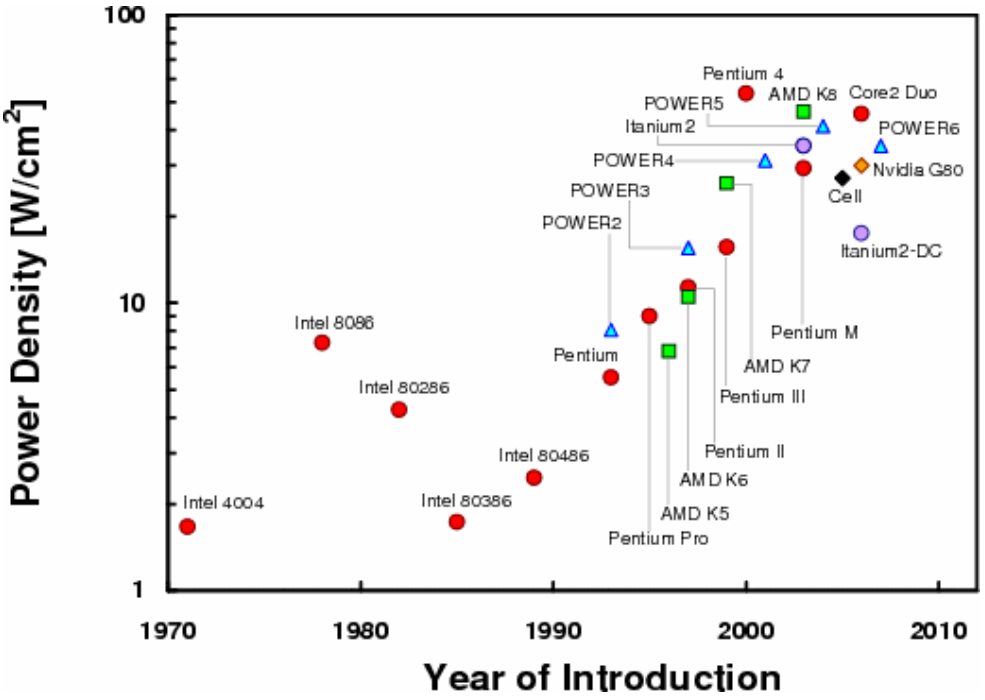


Figure 2.1: Power density of commercial microprocessors [2.1].

This chapter begins with the derivation of a model that relates thermal and electrical performance of an integrated circuit. Following this, the theory and fabrication process for a 3D microprocessor with integrated microchannel cooling are developed. The work in this chapter has been described by the author in [2.4].

2.1. A Model to Relate Thermal and Electrical Performance of an IC

This section explores the relationship between electrical performance of an integrated circuit and thermal resistance of its heat removal solution. Some background is first provided in Section 2.1.1, following which a summary of the model is provided in Section 2.1.2. An example showing how this model can be applied is described in Section 2.1.3.

2.1.1. The Nose-Sakurai Model

In 2000, Nose and Sakurai considered an inverter driving a fan-out of 4 (FO4) and derived expressions for optimal supply and threshold voltages [2.5]. The researchers essentially minimized power consumption of the FO4 inverter for a certain target clock frequency, logic depth, temperature and device technology. Henceforth, these optimal supply and threshold voltage values are denoted as $V_{dd}(T)$ and $V_t(T)$ respectively, where T is the absolute temperature. This work from Nose and Sakurai yielded the following interesting relationships between leakage power (P_{leak}), dynamic power (P_{dyn}) and total power (P) of any CMOS circuit.

$$\frac{P_{leak}}{P_{dyn}} = \frac{2N_s\alpha}{\alpha - 1} \qquad \ldots(2.1)$$

$$\frac{P_{leak}}{P} = \frac{2N_s\alpha}{2N_s\alpha + \alpha - 1} \quad \ldots(2.2)$$

Here, α is an exponent in the power-law MOSFET model [2.6] and N_s is the sub-threshold slope in mV. Substituting α= 1.3 and N_s = 0.04mV (which corresponds to around 100mV/decade), we find that the ratio of leakage power to total power of a microprocessor is about 25%. Commercial microprocessors such as [2.7] have such leakage power to total power ratios.

2.1.2. Summary of Proposed Model

The proposed model is summarized below using three simple relationships denoted as Eq. (2.3), Eq. (2.4) and Eq. (2.5). Meanings of the symbols below are provided in Table 2.1.

$$R_{th} = \frac{T - T_{amb}}{P} \quad \ldots(2.3)$$

$$P = P_{dyn} + P_{leak} = P_{leak}\left(\frac{\alpha - 1}{2N_s\alpha}\right) + P_{leak}$$
$$= P_{leak}\left(\frac{\alpha - 1}{2N_s\alpha} + 1\right) \quad \ldots(2.4)$$

$$P_{leak} = \left.\frac{W}{L}\right)_{av} N_{gates} V_{dd}(T) I_{leak0} e^{-\frac{V_t(T)}{N_s}} \quad \ldots(2.5)$$

Eq. (2.3) represents the definition of thermal resistance while Eq. (2.4) follows from Eq. (2.1). Short-circuit power of a microprocessor is typically less than 10% of the total power and is neglected [2.6]. Eq. (2.5) computes total leakage power of logic cores of a microprocessor. It takes leakage power of a single minimum size gate and multiplies this quantity by the number of gates and typical gate size.

Table 2.1: Description of symbols in model.

Symbol	Description
R_{th}	Thermal resistance of logic cores in ^{o}C/W
T_{amb}	Ambient temperature in K
P	Total power of logic cores in W
N_{gates}	Number of logic gates
$\left.\frac{W}{L}\right)_{av}$	Width to length ratio of transistors in a typical logic gate
I_{leak0}	Leakage current co-efficient of a typical minimum size logic gate in A

Eq. (2.3) when rearranged is

$$P = \frac{T - T_{amb}}{R_{th}} \qquad \ldots(2.6)$$

Combining Eq. (2.4) and Eq. (2.5), we get

$$P = \left.\frac{W}{L}\right)_{av} N_{gates} V_{dd}(T) I_{leak0} e^{-\frac{V_t(T)}{N_s}} \left(\frac{\alpha - 1}{2N_s\alpha} + 1\right) \qquad \ldots(2.7)$$

Eq. (2.6) and Eq. (2.7) represent two equations with two unknowns, total logic power *P* and temperature *T*. These can be solved self-consistently to obtain closed-form solutions for *T* and *P*. An interested reader can refer to Appendix A for details of this solution. An example for application of this model is provided in the following section.

2.1.3. Application of Model to a Pentium Microprocessor

The proposed model is used to evaluate logic power consumption, temperature,

optimal supply voltage and optimal threshold voltage for the 130nm Intel Pentium 4 microprocessor. This processor had 12.5 million logic gates, ran at a clock frequency of 3GHz (16 FO4 delays) and had a die size of 76mm^2 for its logic core [2.8]. Based on data in [2.9], each minimum size nFET in this processor had a capacitive load of around 4.2fF and a leakage current of 100nA/μm at a threshold voltage of 0.19V (at room temperature). Thermal resistance is taken to be 0.6^{o}C-cm^2/W, 3 sigma threshold voltage variation is assumed to be 0.1V [2.10] and range of operation temperatures for this chip is specified as 300K to 400K [2.5].

Table 2.2: Comparison of model predictions with actual data from the 130nm Pentium 4 microprocessor.

	Model	Actual value
Total logic power	94W	~80W
Temperature	100^{o}C	80^{o}C-100^{o}C
Supply voltage	1.2V	1.4V
Threshold voltage at 300K	0.21V	0.19V

These values yield a total logic power of 94W, temperature of 100^{o}C, optimal supply voltage of 1.2V and optimal threshold voltage of 0.21V, as shown in Table 2.2. The error in values of these quantities with respect to actual data from the Pentium 4 processor [2.8][2.9][2.10][2.11] could be due to multiple reasons: (i) Drain induced barrier lowering is neglected in the model. (ii) An increased supply voltage value could have been chosen by the Pentium 4 designers to analog circuits functioned reliably, or to avoid disruptive

changes in design of power delivery systems. (iii) Power reduction techniques such as multiple threshold voltages and downsizing of gates in non-critical paths were utilized in the processor. Despite these potential sources of error, the model seems to be a reasonably accurate relationship between electrical and thermal performance of an integrated circuit. It can be used to find the impact of different types of heat removal solutions on an integrated circuit. It can also provide approximate estimates for supply voltage, threshold voltage and logic power of an integrated circuit prior to design.

2.2. Heat Removal for 3D Integrated Circuits

As mentioned earlier in this chapter, heat removal is one of the most critical challenges with high-performance 3D integrated circuits. Today's air cooled heat sinks have thermal resistance limits around 0.6^{o}C-cm^{2}/W. This makes their use as heat removal solutions for a 3D-IC consisting of two 100W/cm^{2} chips difficult [2.3]. Microchannel cooling technology is a potential solution to this problem.

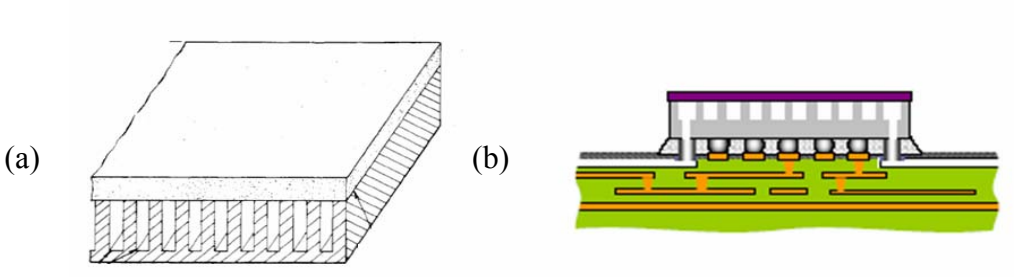


Figure 2.2: (a) Original concept of a microchannel heat sink from Tuckerman and Pease [2.13]. (b) An assembly technology for microchannel heat sinks proposed by Dang, Bakir, Joseph, Kohl and Meindl [2.14].

Microchannel cooling technology was invented in the early 1980s at Stanford University by David Tuckerman and Fabian Pease [2.13]. These inventors proposed etching channels on the back side of a silicon chip and passing a coolant such as water

through these channels. This improved heat removal rates from integrated circuits tremendously. Fig. 2.2(a) is a picture from Tuckerman and Pease's original paper. Over the past 25 years, several enhancements to this original concept have been proposed and evaluated [2.13][2.14]. One such concept from Dang, Bakir, Joseph, Kohl and Meindl (Fig. 2.2(b)) involves delivering fluid to a microchannel heat sink using fluidic I/Os and microchannels on a printed wiring board [2.14]. The authors contend that this would allow cheap, wafer-level fabrication and assembly of microchannel heat sinks to multiple chips on a single printed wiring board. It would also preclude manual attachment of tubes to the backside of each chip in a multi-chip server (Fig. 2.3).

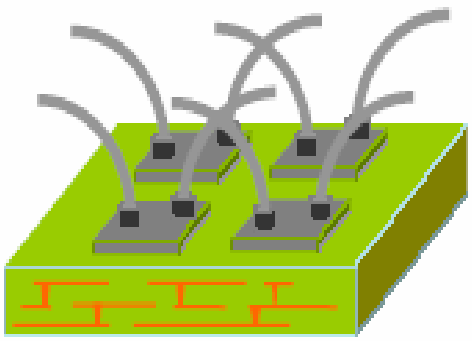


Figure 2.3: Manual attachment of tubes to the backside of each chip on a printed wiring board.

A point to note is that all the published experimental work on microchannel cooling thus far has dealt with 2D integrated circuits. A microchannel-cooled high-performance 3D integrated circuit technology is described in the rest of this chapter.

2.2.1. Concept

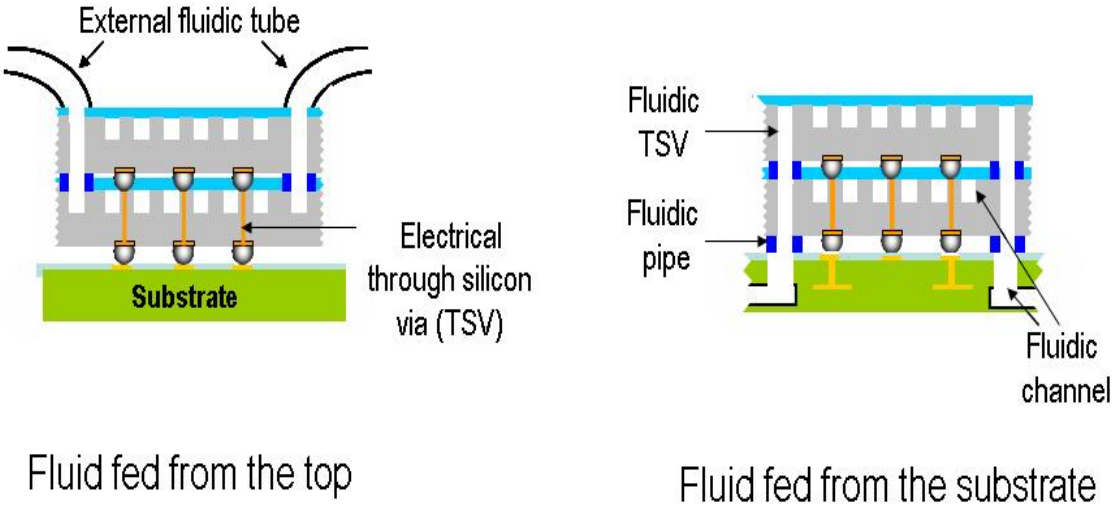


Figure 2.4: A microchannel-cooled 3D integrated circuit.

Potential methods to implement a microchannel-cooled 3D integrated circuit technology are illustrated in Fig. 2.4. Cooling fluid can be delivered to the 3D stack either using tubes on the back side of the 3D stack or using fluidic channels on the substrate. This fluid is delivered to microchannel heat sinks on the back side of each chip in the 3D stack using fluidic through-silicon vias (TSVs) and fluidic pipes. Electrical through-silicon vias are present to deliver power to different chips in the 3D stack and to communicate between different chips. A polymer such as Avatrel is used to cover the microchannels [2.14].

2.2.2. Fabrication Process

The fabrication process for such microchannel-cooled 3D-ICs involves two major parts:

(i) Chip-Level Fabrication Technology

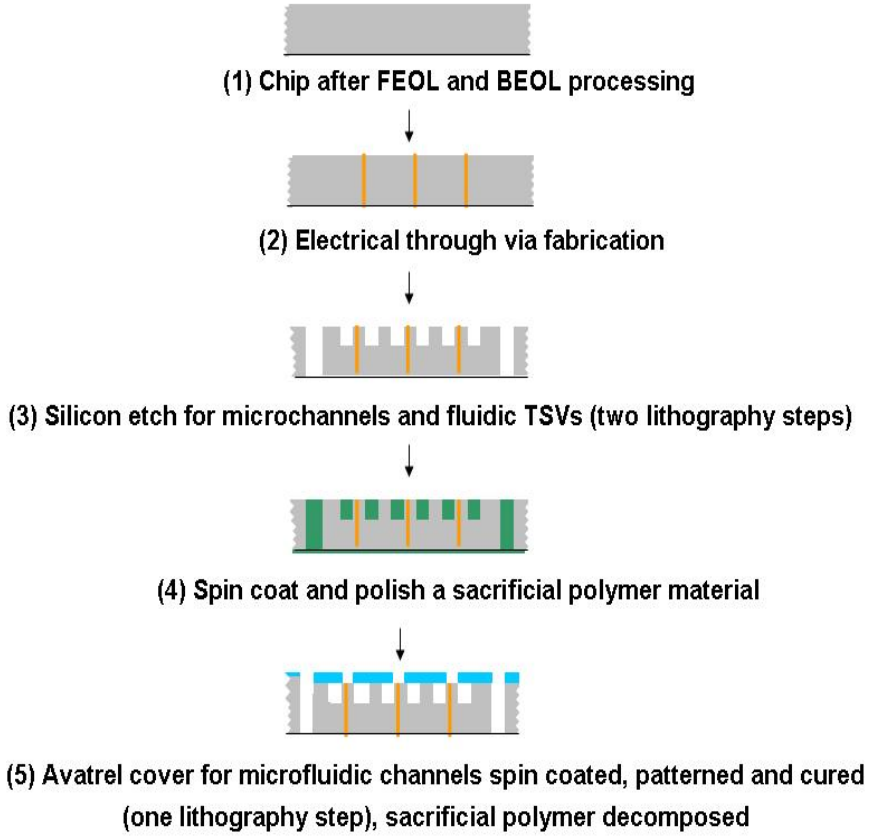


Figure 2.5: Chip-level fabrication process for microchannel-cooled 3D integrated circuits. The extra lithography steps for fluidic network fabrication are indicated.

The chip-level fabrication process is depicted in Fig.2.5. It begins with fabricating electrical TSVs on an integrated circuit that has undergone front end of line (FEOL) and back end of line (BEOL) processing. Several processes are available for fabricating electrical TSVs such as [2.15] and [2.16]. In this work, [2.15] is used due to its simplicity and compatibility with equipment available with Georgia Tech's cleanroom. Following this, the Bosch process is utilized for etching fluidic through-silicon vias and microchannels as shown in step (3) of Fig. 2.5. A sacrificial polymer material such as Unity

is then spin-coated on the microchannels and polished in step (4). An interested reader can refer to [2.14] for more details of steps (3) and (4). A polymer (Avatrel) is spun-on, patterned and cured to form a cover for the microchannels and fluidic TSVs in step (5). Unity is then decomposed by heating to 260^{o}C. Fig. 2.6 shows a cross-sectional microscope microscope image of a sample after this chip-level fabrication process is complete. The entire process outlined above proceeds at less than 260^{o}C, allowing it to be CMOS compatible. Furthermore, the fluidic network processing in Fig. 2.5 occurs at the wafer-level and requires just three micron scale lithography steps. This makes the process economically feasible.

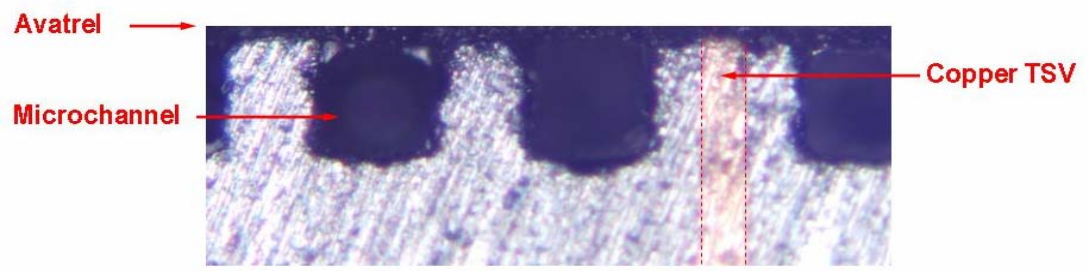


Figure 2.6: Cross-sectional microscope image of a sample after chip-level fabrication. Microchannels are about 200um tall and 150um wide while copper vias are about 50um in diameter. Silicon thickness is 400um. Electrical through-silicon via density is 2500/cm^2.

(ii) Assembly Technology

This part of the project (Section 2.2.2(ii)) was completed by Calvin King. The assembly technology for microchannel-cooled 3D integrated circuits is outlined in Fig. 2.7. After solder bumping, fluidic pipes are fabricated with a polymer such as Avatrel [2.14] for the top chip in a two chip 3D stack. The bottom chip in the two chip 3D stack is first

assembled onto the substrate with a flip-chip bonder. Following this, the top chip in the 3D stack is assembled onto the bottom chip as shown in step (3) of Fig. 2.7. Underfill is dispensed to seal fluidic pipes and control co-efficient of thermal expansion mismatches between the chip and the substrate. Fig. 2.8(a) shows SEM images of a chip with solder bumps and polymer pipes. Fig. 2.8(b), on the other hand, is a cross-sectional SEM image of two silicon chips with solder bumps, fluidic pipes, fluidic through-silicon vias, Avatrel covers and electrical pads. These chips are assembled on top of each other and to a silicon substrate. Fig. 2.6 and Fig. 2.8 thus demonstrate the chip-level fabrication technology and assembly technology required for a microchannel-cooled 3D integrated circuit.

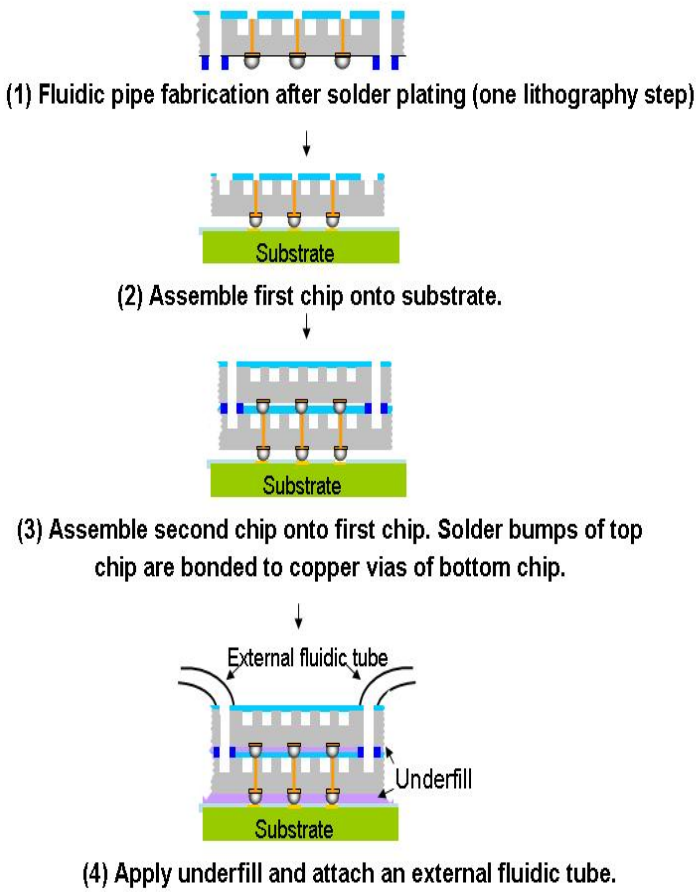


Figure 2.7: Assembly process for microchannel-cooled 3D integrated circuits.

(a) (b)

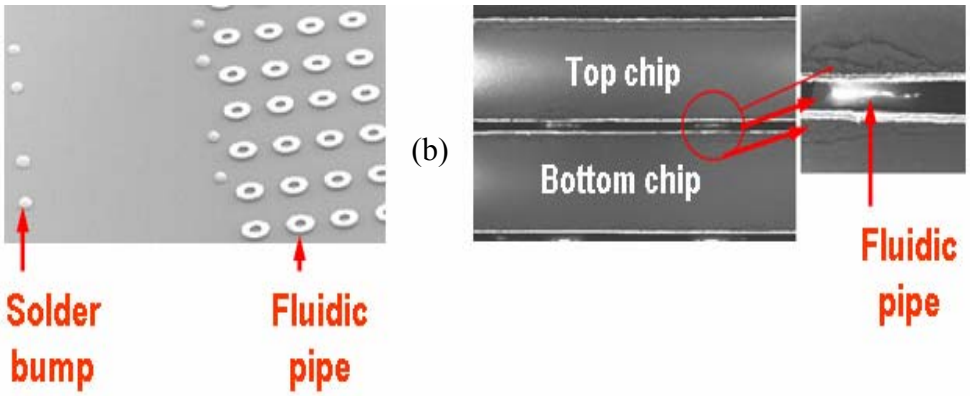
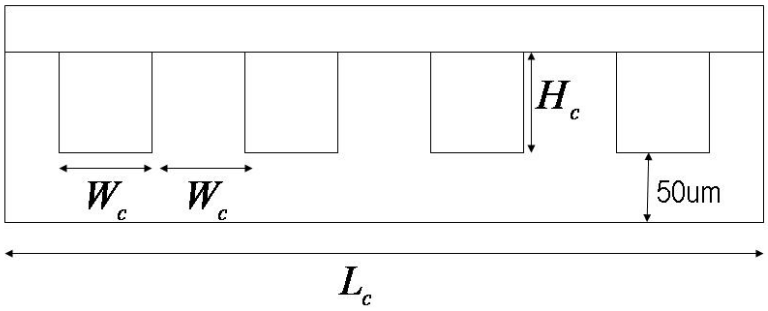


Figure 2.8: (a) SEM image of a chip with solder bumps and polymer pipes. (b) Cross-sectional SEM image of an assembled two chip 3D stack with fluidic networks.

2.2.3. Theoretical Analysis

The thermal resistance of a microchannel heat sink can be written as a sum of three components: R_{cond}, which is due to conduction of heat from the circuits to the microchannel heat sink, R_{conv}, which is due to convective heat transfer between the heat sink and the coolant fluid and R_{heat}, which is due to heating of the fluid as it passes through the heat exchanger. R_{cond} is typically less than 0.01^{o}C/W due to the excellent thermal conductivity of silicon and the short distance between heat generating circuits and microchannels [2.14]. Some commonly used equations for R_{conv} and R_{heat} are given in Fig. 2.9 [2.14]. Equations for pressure drop of the cooling fluid in microchannels ($\Delta P_{channels}$) and fluidic through-silicon vias or pipes ($\Delta P_{via/pipe}$) are also provided in Fig. 2.9. These equations have been verified with experimental data multiple times since the original work from Tuckerman and Pease [2.13][2.14].



Model	Description of symbols
$R_{conv} = \frac{2W_c H_c}{k_f Nu_\infty n_c L_c (2H_c + W_c)(H_c + W_c)}$ where $Nu_\infty = 8.2(1 - 1.9\alpha + 3.8\alpha^2 - 5.8\alpha^3 + 5.4\alpha^4 - 2\alpha^5)$ $R_{heat} = \frac{f\,Re\,L_c \mu \left(1 + \frac{W_c}{H_c}\right)^2}{2\rho C_p n_c H_c W_c \Delta P}$ where $f\,Re = 24(1 - 1.4\alpha + 1.9\alpha^2 - 1.7\alpha^3 + \alpha^4 - 0.3\alpha^5)$	k_f = Thermal conductivity of water in W/m-K n_c = Number of channels Nu_∞ = Nusselt number $\alpha = W_c/H_c$ f = Friction factor Re = Reynolds number μ = Viscosity of water in Pa.s ρ = Density of water in kg/m^3 C_p = Specific heat of water in J/K ΔP = Pressure drop in microchannels in Pa $H_{via/pipe}$ = Height of via/pipe in m $D_{via/pipe}$ = Diameter of via/pipe in m $n_{via/pipe}$ = Number of vias/pipes $\dot{V}$ = Overall flow rate of coolant in m^3/s
$\Delta P_{channels} = \frac{f\,Re\,L_c \mu \dot{V} \left(1 + \frac{W_c}{H_c}\right)^2}{2n_c H_c W_c^3}$ $\Delta P_{via/pipe} = \frac{512 H_{via/pipe} \mu \dot{V}}{n_{via/pipe} \pi D_{via/pipe}^4}$	

Figure 2.9: Equations to describe operation of a microchannel-cooled 3D-IC with square dice. Quantities whose units are not indicated in the above table are dimensionless.

For a microchannel-cooled 3D integrated circuit with an external fluidic tube, the ratio of pressure drop in fluidic vias and pipes ($\Delta P_{via\text{-}pipe\text{-}total}$) to the pressure drop in microchannels ($\Delta P_{channels}$) can be written as follows:

$$\frac{\Delta P_{channels}}{\Delta P_{via-pipe-total}} = \frac{f\, Re\, L_c \left(1+\frac{W_c}{H_c}\right)^2 n_{via/pipe} \pi D_{via/pipe}^4}{1024 n_c H_{via-pipe-total} H_c W_c^3} \quad \ldots(2.8)$$

Here, $H_{via\text{-}pipe\text{-}total}$ represents the total length of vias/pipes in the path of the cooling fluid. Note that separate fluidic pathways exist to the top and bottom chip of the two-chip 3D stack. For typical values for these parameters, i.e. L_c=10mm, W_c=100um, H_c=200um, $D_{via/pipe}$=250um, $H_{via\text{-}pipe\text{-}total}$=0.9mm (for 400um silicon chips), n_c=2$n_{via/pipe}$ = 50, we get

$$\frac{\Delta P_{channels}}{\Delta P_{via-pipe-total}} \sim 12 \qquad \textit{and} \qquad \frac{\text{Silicon area for fluidic through vias}}{\text{Chip area}} = 2.5\% \quad \ldots(2.9)$$

The above numbers reveal that fluidic vias and fluidic pipes consume minimal surface area for a two-chip microchannel-cooled 3D integrated circuit, and at the same time have negligible pressure drop through them. This is largely because the total length of fluidic vias and pipes is only 0.9mm while the length of microchannels is as high as 10mm. Further reduction in pressure drop of fluidic vias and pipes is possible by increasing silicon area allocated to these structures. The result in Eq. (2.9) is interesting, since this indicates the fluidic network that provides liquid coolant to the microchannel heat sink does not impose any significant overhead for a two-chip stack. *Essentially, integrated circuits in a multi-chip server would have the same thermal resistance irrespective of whether they are placed side-by-side or form part of two-chip 3D stacks!* Note that experiments by Dang, et

al. in [2.14] revealed that pressure drop through fluidic pipes and through-silicon fluidic vias were negligible for a microchannel-cooled 2D integrated circuit as well.

Another interesting trade-off exists and can be studied with the models in Fig. 2.9. It is well-known that high aspect ratio microchannels are required for heat removal [2.13]. This, in turn, requires a high silicon thickness. However, a high silicon thickness increases the diameter of electrical through-silicon vias. Table 2.3 helps explain this phenomenon. Aspect ratios of through-silicon vias possible today are in the range of 6:1 to 11:1 [2.15][2.16]. Even for a 16:1 aspect ratio electrical through-silicon via technology, Table 2.3 reveals that the diameter of through-silicon vias cannot be reduced below 6um for a thermal resistance limit of 0.6°C/W.

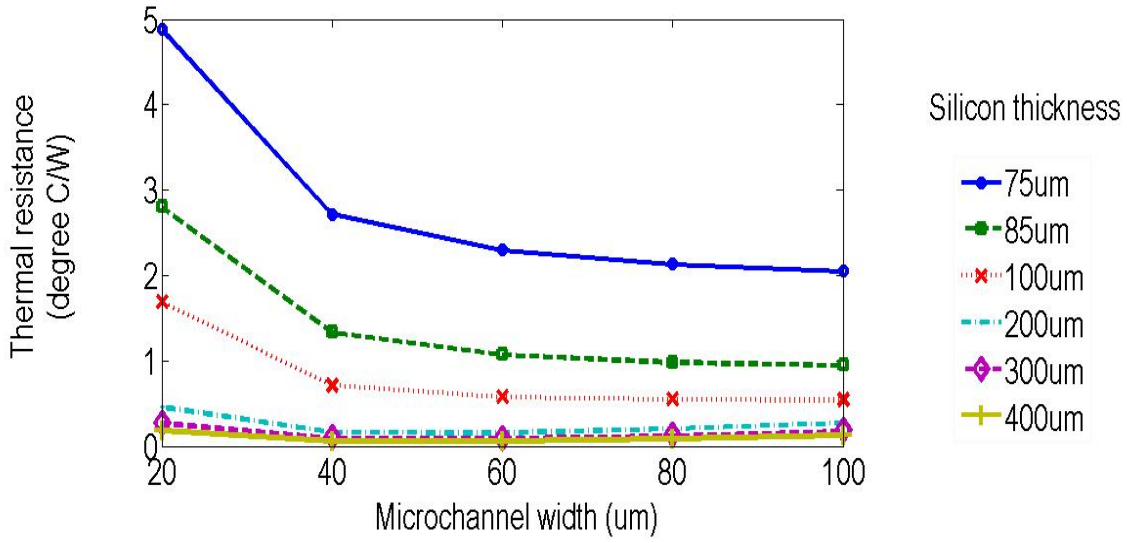


Figure 2.10: Thermal resistance vs. silicon thickness.

On-chip global interconnect widths of today's microprocessors are around 0.5um [2.17]. *To move a significant number of global interconnects into the third dimension, it seems reasonable to expect that through-silicon via diameter needs to be around the same range as global interconnect width. However, due to the silicon thickness requirement imposed by microchannels, the electrical through-silicon via diameter in Table 2.3 is an order of magnitude higher than the global interconnect width*. This could limit the benefits of microchannel-cooled 3D integrated circuits as far as global interconnects are concerned. Note that this analysis considers aggressive pump technology (Table 2.4), and therefore, for standard pump technology, it might be difficult to even reach the numbers given in Table 2.3. Table 2.4 gives a summary of various varieties of micropumps that have been demonstrated in the literature [2.18]. It reveals the aggressiveness of the pump technology assumed for Table 2.3 based on pressure drop and flow rate values.

Table 2.3: Silicon thickness optimization for 100 um wide microchannels (from Fig. 2.10).

Silicon thickness	Thermal resistance (^{o}C/W)	Pressure drop (psi)	Flow rate for each chip in 3D stack (ml/min)	Via diameter (um)		
				Aspect ratio 6:1	Aspect ratio 11:1	Aspect ratio 16:1
75um	2.05	30	7.6	13	7	4.7
85um	0.95	30	19	14	8	5.3
100um	0.55	30	49	17	9	6.3
200um	0.15	30	506	33	18	12
300um	0.09	30	1075	50	27	19
400um	0.07	30	1650	67	36	25

Table 2.4: Micropump technology demonstrated in the literature (from [2.18]).

Micropump description	Volume of pump	Pressure drop (psi)	Flow rate (ml/min)
Rotary micropump with a magnetic micromotor	$6mm^3$ (without motor)	2	0.350 (water)
Vibrating diaphragm micropump with piezoelectric actuation	$42mm^3$	2.4	1.5 (water)
Valveless nozzle-diffuser micropump with piezoelectric actuation	$122mm^3$	0.14	1.5 (ethanol)
Electroosmotic micropump	$1413mm^3$	23	7
Injection EHD micropump	$7mm^3$	0.35	14 (ethanol)
Mini centrifugal magnetic drive pump (from Cole Parmer Product Manual)	$900cm^3$	30	1650

2.2.4. Characterization

The thermal resistance for each chip in a two chip 3D integrated circuit can be obtained by measuring properties of the single microchannel heat sink shown in Fig. 2.11. This is because fluidic TSVs and fluidic pipes delivering fluid to microchannels have a negligible pressure drop overhead. Platinum thin film resistors were fabricated on a chip with a microchannel heat sink to facilitate this measurement. Current was passed through these platinum resistors to produce heat, while temperature changes were measured by monitoring changes in platinum resistance. The chip was packaged and copper pads on the silicon substrate were used to deliver current to the platinum resistors and to monitor their resistances. Deionized water was circulated through the microchannels at a flow rate of 65ml/min using a pump [2.14]. Fig. 2.11 shows details of these measurements. Pump power was measured as 0.3W while pressure drop was measured as 3.4psi [2.14]. The

junction-to-ambient thermal resistance was measured as 0.24°C/W based on the data in Fig. 2.11. Each chip in the two-chip 3D integrated circuit would thus have a junction-to-ambient thermal resistance of 0.24°C/W.

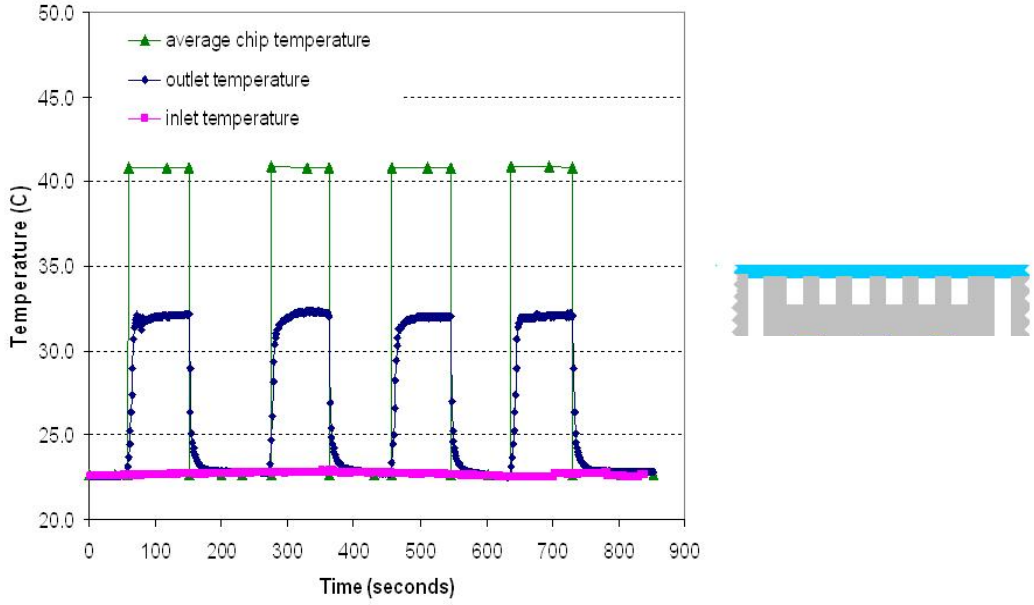


Figure 2.11: Measurement of thermal resistance. Fluid inlet and outlet temperatures also indicated (Courtesy: Bing Dang [2.14]).

2.2.5. Benefits

Microchannel-cooled 3D integrated circuits provide tremendous benefits to high-performance servers. Fig. 2.12 shows the organization of chips in a server when it is composed exclusively of 2D integrated circuits. It also depicts the organization of chips when 3D die stacking is enabled due to microchannel cooling techniques. The distances between three representative chips, denoted as chip 1, chip 2 and chip 3 are indicated. It can be observed that microchannel-cooled 3D integrated circuits enable upto an order of magnitude reduction in chip-to-chip interconnect lengths. This leads to significant

improvements in chip-to-chip interconnect latency, bandwidth and power dissipation.

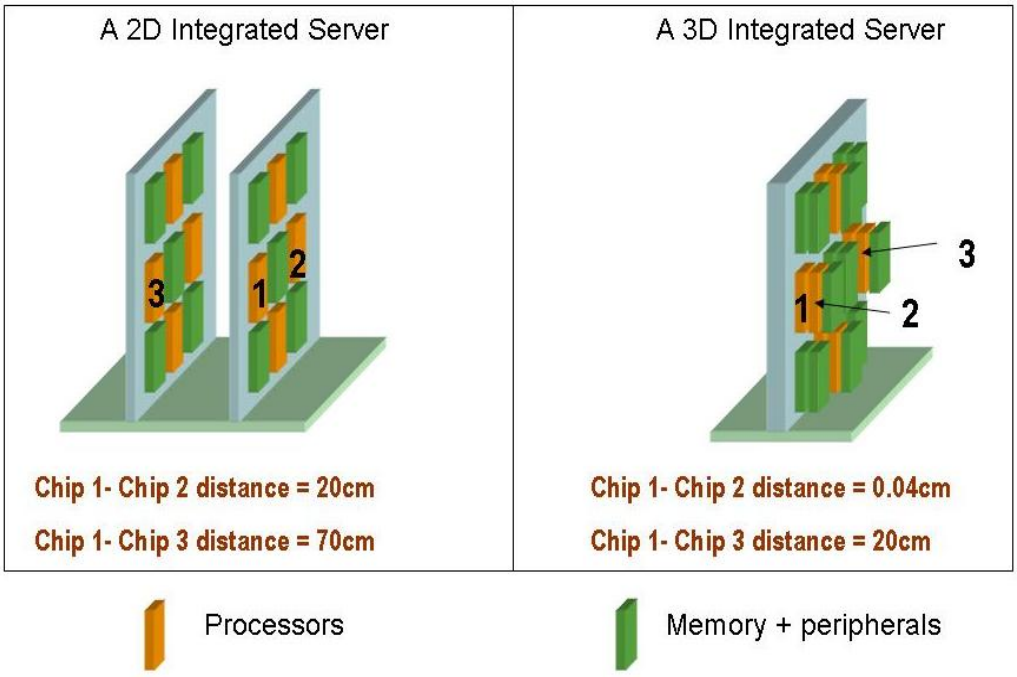


Figure 2.12: Organization of a sample 2D server [2.19] in a 3D configuration. Besides higher logic density, 3D stacking also enables higher memory density.

Another benefit of microchannel-cooled 3D integrated circuits is the reduced thermal resistance when compared to today's air cooled integrated circuits. This can be studied using the electrothermal model summarized in Section 2.1. When a 3GHz logic core in a 2D air cooled server has 0.6^{o}C/W thermal resistance, the model reveals that its chip temperature is 88^{o}C and power is 102W. This data is obtained for the 65nm technology described in [2.17]. Table 2.5 shows results obtained from the equations in Section 2.1 when this logic core forms part of a 0.24^{o}C/W microchannel-cooled 3D-IC. Three cases are considered where the microchannel-cooled logic core has (i) the same frequency, (ii) the same power, and (iii) the same temperature as the air cooled 3GHz logic core. For the

same frequency case, an 18% reduction in power results along with a 41°C reduction in temperature. For the same power case, a 10% increase in frequency is obtained along with a 36°C reduction in temperature. This reduction in chip temperatures is beneficial for server reliability. If chip temperature is fixed at 88°C, a 3GHz air cooled logic core can be clocked at 4.5GHz with a microchannel heat sink. This 50% increase in frequency over the 3GHz logic core is substantial. However, the equations in Section 2.1 reveal that the 4.5GHz logic core would have a current of 203A compared to 105A for the 3GHz logic core, indicating improved power delivery schemes would be needed. These improved power delivery schemes are described in Chapter 4.

Table 2.5: Benefits of microchannel-cooled 3D integrated circuits for a processor with 40 million logic gates constructed in a 65nm technology.

	Frequency	Power	Temperature	Optimal supply voltage	Optimal threshold voltage
Air cooled processor with thermal resistance 0.6°C/W	3GHz	102W	88°C	0.97V	0.29V
Microchannel-cooled processor with thermal resistance 0.24°C/W	3GHz	83W	47°C	0.87V	0.29V
	3.3GHz	102W	52°C	0.92V	0.29V
	4.5GHz	254W	88°C	1.25V	0.27V

2.3. Summary

A microchannel-cooled 3D integrated circuit technology is developed in this chapter to address heat removal challenges inherent to stacked high-performance microprocessors.

The presented microfluidic cooling networks are CMOS compatible, involve four minimally demanding lithography steps and are fabricated at the wafer-level. Electrical through-silicon via density for fabricated samples is 2500/cm^2. Measurements reveal each chip in a two-chip microchannel-cooled 3D stack would have a junction-to-ambient thermal resistance of 0.24^{o}C/W. A tremendous reduction in chip-to-chip interconnect lengths is obtained due to this technology. However, on-chip global interconnect length reduction with microchannel-cooled high-performance 3D integrated circuits appears difficult, due to silicon thickness limitations imposed by the heat removal solution. A newly derived electrothermal model that co-designs electrical and thermal functionality of an IC reveals that a 3GHz logic core of an air-cooled microprocessor could run at 4.5GHz when it forms part of a microchannel-cooled 3D integrated circuit due to improved thermal resistance values. Challenges associated with microchannel-cooled 3D integrated circuits are development of pumps that work reliably over the lifetime of a server and fluid leakage.

CHAPTER 3

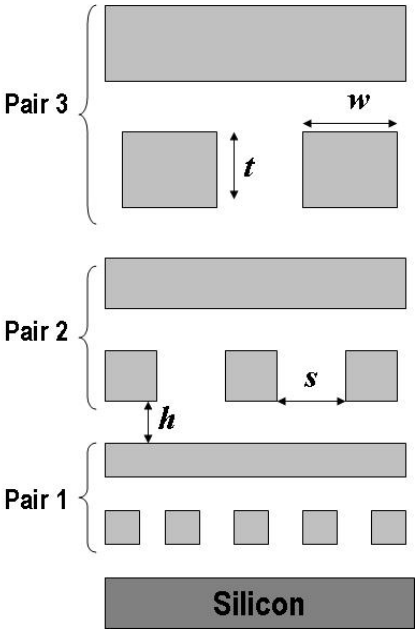
SIGNAL INTERCONNECT NETWORKS

Signal interconnect networks consume the bulk of the wiring area of today's microprocessors. Table 3.1 shows wire pitches of high-performance and low-power 65nm technologies [3.1] from Intel Corporation. Pitches of interconnect levels are normally selected by semiconductor manufacturers using a stochastic wire length distribution. This looks at previous generations of a certain microprocessor and predicts wire lengths of a microprocessor that needs to be designed with the current logic technology [3.2][3.3]. Once the wire length distribution is known, algorithms are used to find pitches of different interconnect levels based on certain performance criteria and cost limitations [3.2][3.3].

Table 3.1: Interconnect pitches of 65nm logic technologies.

	High-performance 65nm technology	Low-power 65nm technology
M1	210nm	210nm
M2	210nm	210nm
M3	220nm	220nm
M4	280nm	280nm
M5	330nm	275nm
M6	480nm	280nm
M7	720nm	420nm
M8	1080nm	1080nm

The methodology summarized in the previous paragraph forms the basis of a CAD tool called MINDS that was developed by Venkatesan, Davis and Meindl in 2003 to study signal interconnect networks [3.2]. MINDS is used in this chapter to evaluate different opportunities and ideas for enhancing signal interconnect networks.



$$2e_w A_m = \chi P \sqrt{\frac{A_m}{N_{gates}}} \int_{l_{min}}^{l_{max}} li(l)dl$$

$$\tau_{rc} = \frac{2.2\rho c l^2}{P^2} = \frac{\beta}{f} \qquad \ldots(3.1)$$

$$\tau_{rc} = \frac{2.75 l \sqrt{2\rho c R_o C_o}}{P} = \frac{\beta}{f} \qquad \ldots(3.2)$$

Figure 3.1: Equations in MINDS.

The algorithm in MINDS can be understood better with the equations in Fig. 3.1. In Eq. (3.1) and Eq. (3.2), A_m is the core area, χ is a factor to convert point-to-point wire length to net length, e_w is a wire efficiency factor, P is the wire pitch, l_{min} and l_{max} are the minimum and maximum wire lengths on the pair of metal levels respectively, N_{gates} is the number of logic gates, c is the wire capacitance per unit length, β is a factor which is 0.25 for local wires and 0.9 for other wires, R_o and C_o are the resistance and capacitance of a minimum

size repeater respectively and ρ is the wire resistivity. Also, $i(l)dl$ is the number of point-to-point interconnects whose length lies between l and $l+dl$. Estimates for this quantity are obtained from a stochastic wire length distribution model derived by Davis and Meindl in [3.4]. The right hand side of Eq. (3.1) thus indicates the area needed for routing wires of length l_{min} to l_{max} in a pair of wiring levels, while the left hand side of Eq. (3.1) gives the area available for routing wires in that pair of wiring levels. It is assumed that $w=s= P/2$ and $t=h=P$ where w, t, s, h and P are as indicated in Fig. 3.1. The RC delays of interconnects, with and without repeater insertion are given in Eq. (3.1) and Eq. (3.2). Repeater insertion is carried out using a sub-optimal Bakoglu methodology [3.2].

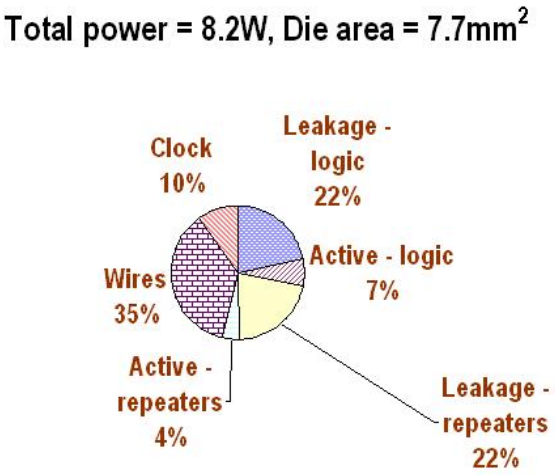
Starting from the first pair of wiring levels, Eq. (3.1) and Eq. (3.2) are solved simultaneously. This helps determine the minimum wire pitch that allows the delay of the longest wire in a pair of wiring levels to be a certain fraction of the clock frequency. If the pitch obtained is smaller than the minimum pitch projected by the International Technology Roadmap for Semiconductors (ITRS) [3.5] for a certain logic technology, the ITRS minimum pitch is used. Using Eq. (3.1), the length of the longest wire is then calculated. The maximum length for wire pair 1 becomes the minimum length for wire pair 2. These steps are repeated for all wire pairs until the longest interconnect in the wiring distribution is routed. Rent's constants [3.4] are assumed to be k=4 and p=0.6 for all the analysis in this chapter. Logic gates are modeled as two-input NAND gates and are sized based on average wire length estimates. Simulations using MINDS have been shown to match data from commercial microprocessors in [3.2]. Leakage power models from [3.6] are used. The impact of size effects such as surface scattering and grain boundary scattering on copper resistivity are modeled as shown in [3.7]. The values for both

specularity parameter and reflectivity parameter for these types of scattering are chosen to be 0.5 [3.7].

This chapter begins with using MINDS to study signal interconnect challenges in scaled CMOS technologies. Solutions are then suggested to these challenges and their impact is quantified. The work in this chapter has been described by the author in [3.8], [3.9] and [3.10].

3.1. Signal Interconnect Challenges in Scaled CMOS Technologies

This section quantifies the impact of signal interconnect networks on a 4GHz 0.5V 30M gate logic core constructed in a 22nm technology [3.5]. MINDS is used to predict pitches of interconnect levels, power and minimum die size that allow the wiring to be packed in ten metal levels.



Metal levels	Pitch (nm)
M1, M2	44
M3, M4	52
M5, M6	65
M7, M8	97
M9, M10	186

Figure 3.2: Projections from MINDS for a 22nm logic core.

Results from MINDS are summarized in Fig. 3.2. It can be observed that interconnects

and repeaters consume 61% of the total power of this logic core. Moreover, repeaters consume 26% of the total power and repeater leakage power is about 50% of the total leakage power. This data underscores how interconnect technology heavily influences power dissipation of microprocessors in aggressively scaled CMOS technologies. Interestingly, after the author published the above results on repeater power dissipation [3.8], IBM presented data from their chips confirming these results [3.11].

It is well known that designers of today's high-performance microprocessors are given a certain target power dissipation number and are asked to maximize performance within that power budget. This is due to many reasons: (i) Electricity bills of today's servers over their lifetimes cost more than the price of the servers themselves [3.12]. To get a low cost of ownership, it is important to keep power dissipation under control. (ii) Thermal management and power delivery for chips with high power dissipation is difficult. Essentially, if the dominant interconnect and repeater power in Fig. 3.2 is somehow reduced, one could get substantially higher performance for the considered logic core. Thus, it is clear that interconnects impact performance of a logic core significantly.

The cost of ownership of a high-performance microprocessor today depends on its die size, number of interconnect levels and power costs. The 10 interconnect levels needed for this 22nm high-performance microprocessor require 20 lithography steps, compared to 39 lithography steps for the entire microprocessor [3.5]. Ref. [3.2] gives an analysis that shows how the die size of a microprocessor is determined both by the area needed for routing its wires and the silicon area needed for its transistors.

Signal interconnect networks therefore play an important role in determining performance, power and cost of a GSI chip.

3.2. A Technological Solution: Carbon Nanotube Interconnects

Carbon nanotubes are cylinders of graphene, a two dimensional form of graphite. They can be classified as single-walled and multi-walled based on the number of graphene shells forming the nanotube, as depicted in Fig. 3.3. Carbon nanotube interconnects are considered to be a promising alternative to copper interconnects in the long-term [3.13] due to their lower resistivity.

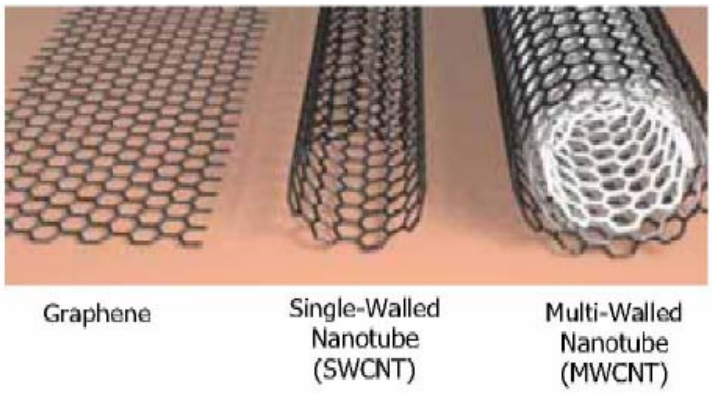


Figure 3.3: Types of carbon nanotube interconnects.

Although several publications have compared the performance of carbon nanotube (CNT) interconnects with copper wires [3.13][3.14], the impact of carbon nanotube interconnects on an entire GSI chip is not known. For example, it is not known what the power or performance benefits to a GSI chip could be if carbon nanotube interconnects are used. If the power or performance benefits are substantial, it could motivate further research on CNTs, while if the power or performance benefits are not significant, it could help focus research expenditure towards more promising approaches. The objective of this work is, therefore, to evaluate the power and performance benefits of using carbon

nanotube interconnects in GSI chips.

3.2.1. Circuit Models

Carbon nanotube interconnects are examples of quantum wires, where transport properties are affected by quantum effects. Due to the confinement of conduction electrons in the transverse direction of the wire, their transverse energy is quantized to a series of discrete values. This causes carbon nanotube interconnects to have some rather unique properties. Multi-walled CNTs form the focus of this study, since previous work has shown that multi-walled CNTs offer higher performance benefits [3.15] than single-walled CNTs for long interconnects.

(i) Resistance Models

An important characteristic of carbon nanotube interconnects is quantum resistance [3.13]. A single shell of graphene, irrespective of length, has two electronic sub-bands that cross the Fermi level and a quantum resistance of $h/4e^2$ = 6.5kΩ, where h is Planck's constant and e is the charge on an electron [3.13]. Due to multiple graphene shells contributing to conduction in multi-walled CNTs, the effective quantum resistance is lower than the 6.5kΩ value mentioned above.

The effective resistivity, ρ, of multi-walled CNTs is modeled using Eq. 3.3 [3.15].

$$\rho = \frac{2\delta R_o}{L} \cdot \frac{1}{\left(1-\frac{D_{min}^2}{D_{max}^2}\right)\frac{aT}{2} + \left(b-\frac{aTL}{l_o}\right)\left(\left(\frac{1}{D_{max}}-\frac{D_{min}}{D_{max}^2}\right)-\frac{L}{D_{max}^2 l_o}log\frac{D_{max}+\frac{L}{l_o}}{D_{min}+\frac{L}{l_o}}\right)} \quad \ldots(3.3)$$

Here, δ is the spacing between adjacent shells in a multi-walled CNT interconnect. This quantity is the van der Waals distance between adjacent graphene layers in graphite,

and is taken to be 0.34nm. L is the length of the interconnect, R_o=12.9kΩ is the quantum resistance of a single conduction channel of a graphene shell, T is the absolute temperature, D_{max} and D_{min} are the outer and inner diameters of the multi-walled CNT interconnect respectively, a is $2.04 \times 10^{-4} nm^{-1} K^{-1}$, b is 0.425 and $l_o = 1000/(T/100-2)$. This model makes three key assumptions: (a) Good contacts to all shells in the multi-walled CNT wire (b) Interaction between different shells of a multi-walled CNT does not impact performance (c) One-third of all shells in the multi-walled CNT are metallic.

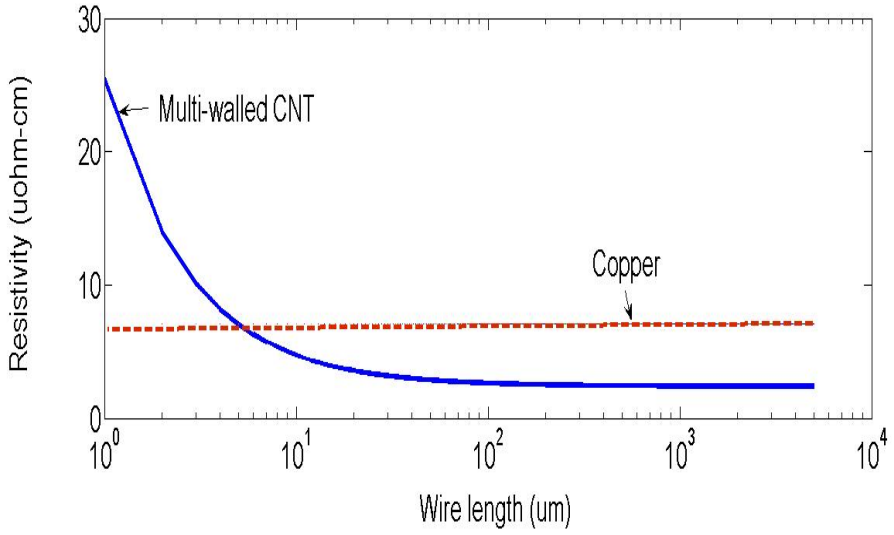


Figure 3.4: Comparison of wire resistivity of a multi-walled CNT interconnect and a copper interconnect at the 22nm technology node.

Fig. 3.4 shows a resistivity comparison of 22nm wide multi-walled CNT interconnects with 22nm wide and 44nm tall copper wires. This is done for all wire lengths in the logic core analyzed in Section 3.1. It can be seen that carbon nanotube interconnects reduce wire

resistivity for a majority of wire lengths in the logic core. For example, carbon nanotube interconnects reduce resistivity of a 1mm wire by as much as 66%. To put this in perspective, the transition from aluminum to copper interconnects reduced resistivity by 45-50% [3.16]. Another observation from Fig. 3.4 is that for short wire lengths, carbon nanotube interconnects do not provide an advantage over copper interconnects. This is due to the quantum resistance [3.13] of carbon nanotube interconnects.

(ii) Capacitance Models

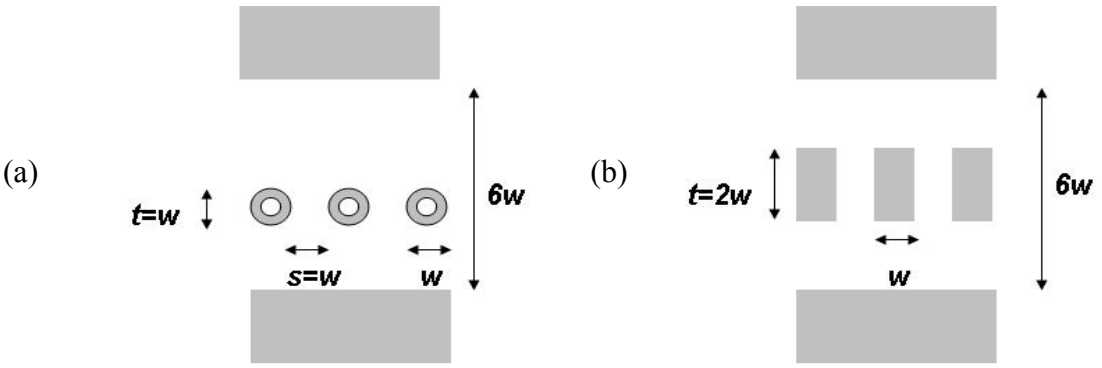


Figure 3.5: Comparison of interconnect architecture of (a) carbon nanotube interconnects, and (b) copper. *t* is the wire thickness, *w* is the wire width and *s* is the wire spacing.

Besides the lower resistivity, another advantage of using 22nm wide multi-walled CNT interconnects over 22nm wide and 44nm tall copper wires is the lower capacitance. This is due to the lower effective aspect ratio and cylindrical shape of multi-walled carbon nanotube interconnects. Using tables and compact models in [3.2][3.17], the structure in Fig. 3.5(a) is found to have 45% reduced electrostatic capacitance compared to the structure in Fig. 3.5(b). Since wire capacitance depends on the ratio of different wire

cross-sectional dimensions and not the cross-sectional dimensions themselves [3.2][3.17], this 45% capacitance advantage is available to all metal levels on a GSI chip that use multi-walled CNT interconnects.

To add electric charge to a quantum wire, one must add electrons to available states above the Fermi level (Pauli Exclusion Principle). A quantum capacitance can thus be defined in series with the electrostatic capacitance for each conduction channel. This capacitance has a value in the order of 200aF/μm, and in virtually all cases is much larger than the electrostatic capacitance. In most practical cases, it can therefore be ignored [3.18].

3.2.2. Manufacturing Challenges

Although carbon nanotube interconnects offer a significant reduction in wire resistivity, several important challenges need to be overcome before they are viable. These challenges include large scale directed growth of horizontally oriented carbon nanotubes, obtaining good contacts to all shells of a horizontal multi-walled CNT and manufacturing at CMOS compatible process temperatures (<400^{o}C) [3.13]. Several research projects in industry and academia are currently directed towards surmounting these barriers [3.13]. The analysis in this manuscript evaluates the benefits provided by carbon nanotube interconnects to a GSI chip *if* the above challenges can be overcome.

Wires in local metal levels of GSI chips typically have lengths less than 100μm. The logic core considered in Section 3.1, for example, is predicted by MINDS to have wires of length ranging from 0.5μm to 28μm in M1 and M2. The quantum resistance of multi-walled CNTs reduces their applicability to such short wires (Fig. 3.4). Many of these short wires in M1 and M2 also have large fan-outs. Distributing large fan-outs is difficult

due to the quantum resistance. Thus, wires in M1 and M2 are assumed to be constructed exclusively with copper for this analysis.

While horizontally oriented carbon nanotubes help transport signals horizontally across a chip, vertical interconnects (vias) are required in each wire level to access higher levels of metal. Since the current conductivity of CNTs in non-axial directions is negligible, horizontally oriented CNTs cannot serve as vias. Copper is therefore required in each metal level for forming vias to higher levels of metal. Power interconnects form a significant portion of the total wiring area of a microprocessor today too. These interconnects are distributed using grid structures with segment lengths less than 1μm, and would be affected by the quantum resistance. Copper would therefore be required in all metal levels for power wiring purposes as well. This constraint of having both copper and carbon nanotubes in each metal level is an important barrier to carbon nanotube interconnect technology. Cost forms one of the major requirements for any interconnect technology, and having both copper and CNTs on the same metal level would cause a significant increase in lithography and process cost.

3.2.3. Power Benefits

A 4GHz 0.5V 30M gate logic core constructed in a 22nm technology is considered for this analysis. Two cases are considered: (a) copper is the only metal used for interconnect levels, and (b) both multi-walled CNTs and copper are used for interconnect levels. The power benefits of case (a) are first studied when the number of metal levels for case (a) and case (b) are the same.

The minimum logic core area that allows all the wiring to be packed into 10 metal levels is obtained with MINDS. Fig. 3.6 shows that while case (a) has a die area

requirement of 7.7mm^2, the die area requirement for case (b) is only 4.7mm^2. If logic cores form 40% of the total die area of the chip, this 39% reduction in die area for the logic core translates to a 15% reduction in total die area. The die area reduction results in more dice being processed per wafer and ameliorates the process cost overhead of having both CNTs and copper in various metal levels.

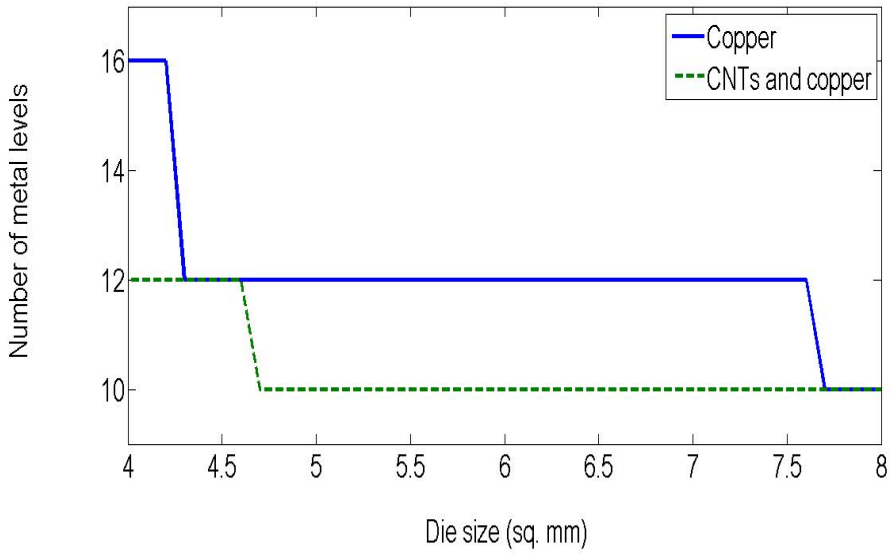


Figure 3.6: Logic core area optimization using MINDS.

The reason for this die area reduction with CNT interconnects is apparent from Table 3.2 which shows wire pitches predicted with MINDS for case (a) and case (b). Essentially, due to the lower resistivity and capacitance of CNT interconnects, a chip using CNTs can have its wires sized smaller for the same clock frequency. Since the area required for routing these smaller size wires is reduced, die area is lower for the chip with CNT interconnects.

Table 3.2: Wire pitch prediction using MINDS.

Metal levels	Pitch (nm)
M1, M2	44
M3, M4	52
M5, M6	65
M7, M8	97
M9, M10	186

Case (a): Chip with copper only.

Metal levels	Pitch (nm)
M1, M2	44
M3, M4	44
M5, M6	45
M7, M8	76
M9, M10	79

Case (b): Chip with CNTs and copper.

The power predicted by MINDS for both cases is summarized in Table 3.3. Interconnect power is reduced by 47% for the logic core with CNT interconnects because of a decrease in total wire capacitance. This is due to two reasons: (a) The 39% reduction in logic core area results in shorter wires. (b) The capacitance per unit length of CNT interconnects is lower than copper. There is also a 48% reduction in logic gate power when CNT interconnects are used. This is primarily due to lower values of wire capacitance, which result in smaller sizes for logic gates required to drive these wires. For the same reason, latch sizes are also reduced. Furthermore, the die area savings cause shorter local clock wires. This reduction in clock wire and latch capacitances allows smaller local clock buffers to be used. The decrease in capacitance associated with latches, local clock wires and clock buffers leads to clock power savings. The clock power for the chip with CNT interconnects is 0.4W compared to 0.8W for the chip constructed exclusively with copper interconnects. This represents a 50% reduction in clock power. Repeater power is also significantly reduced from 2.1W to 0.4W largely due to improved performance offered by

multi-walled CNT interconnects. For the entire logic core, a 56% reduction in power is obtained with multi-walled carbon nanotube interconnects.

Table 3.3: Power reduction with CNT interconnects for a 22nm technology.

	Logic core with copper only	Logic core with CNTs and copper	Percentage reduction in power
Logic gates	2.3W	1.2W	48%
Repeaters	2.1W	0.4W	81%
Interconnects	3W	1.6W	47%
Clock	0.8W	0.4W	50%
Total	8.2W	3.6W	56%

Thus, a 4GHz 22nm logic core with 30M gates and 10 metal levels could have a 56% reduction in power and a 39% reduction in area if multi-walled carbon nanotubes are used along with copper for its interconnect technology. Of course, there is a process cost overhead to utilizing both carbon nanotubes and copper in various metal levels.

The power benefits of carbon nanotube interconnects are now studied. This is done by assuming the 4GHz 0.5V 30M gate 22nm logic core with carbon nanotube interconnects has the same die area as the logic core constructed exclusively with copper interconnects. The wire pitches and number of metal levels obtained with MINDS are shown in Table 3.4. While the logic core with CNT interconnects requires 8.8 metal levels, the logic core constructed exclusively with copper interconnects requires 10 metal levels. Carbon nanotube interconnects thus allow a 12% reduction in the total number of metal levels. The

cause for this reduction in number of metal levels is apparent from Table 3.4. The lower resistivity and capacitance of carbon nanotube interconnects allows smaller wire pitches, and this, in turn, leads to reduced wire area and fewer metal levels.

Table 3.4: Wire pitch prediction using MINDS.

Metal levels	Pitch (nm)
M1, M2	44
M3, M4	52
M5, M6	65
M7, M8	97
M9, M10	186
Metal levels	10
Die area	7.7mm^2

Case (a): Chip with copper only.

Metal levels	Pitch (nm)
M1, M2	44
M3, M4	44
M5, M6	74
M7, M8	91
M9, M10	121
Metal levels	8.8
Die area	7.7mm^2

Case (b): Chip with CNTs and copper.

Table 3.5 shows a comparison of power consumption for the chip with carbon nanotube interconnects when it has the same die area as the chip constructed exclusively with copper interconnects. As described previously, wire capacitance reduces with carbon nanotube interconnects due to their lower effective aspect ratio and cylindrical shape. This decrease in wire capacitance causes a reduction in gate, latch and clock buffer sizes. Repeater power is also lowered due to the improved resistance and capacitance characteristics of carbon nanotube interconnects.

Thus, a 4GHz 22nm logic core with 30M gates and a die area of 7.7mm^2 could have a

43% reduction in power and 12% reduction in number of metal levels if multi-walled carbon nanotubes are used along with copper for its interconnect technology.

Table 3.5: Power reduction with CNT interconnects for a 22nm technology.

	Logic core with copper only	Logic core with CNTs and copper	Percentage reduction in power
Logic gates	2.3W	1.6W	30%
Repeaters	2.1W	0.6W	71%
Interconnects	3W	2W	33%
Clock	0.8W	0.6W	25%
Total	8.2W	4.7W	43%

3.2.4. Performance Benefits

This section of the manuscript describes the performance benefits of using multi-walled carbon nanotube interconnects in the logic core studied in Section 3.2.3. Two cases are considered: (a) The logic core has copper interconnects only and runs at 4GHz with a power budget of 8.2W (b) The logic core has both multi-walled CNT interconnects and copper and has a power budget of 8.2W (same as case (a)). The maximum clock frequency for the logic core in case (b) is evaluated.

Multiple simulations are run with MINDS for this purpose. For each clock frequency, the minimum die size for which the interconnects can be packed into 10 metal levels is computed. Power consumption is evaluated for this value of the die size. Fig. 3.7 indicates that a logic core with carbon nanotube interconnects can be clocked at frequencies as high

as 6.1GHz and still have a power dissipation of less than 8.2W. A logic core constructed exclusively with copper interconnects can be clocked only at 4GHz for 8.2W power dissipation, as shown in Table 3.5. There is a 6.5% die area reduction for the case involving multi-walled CNT interconnects.

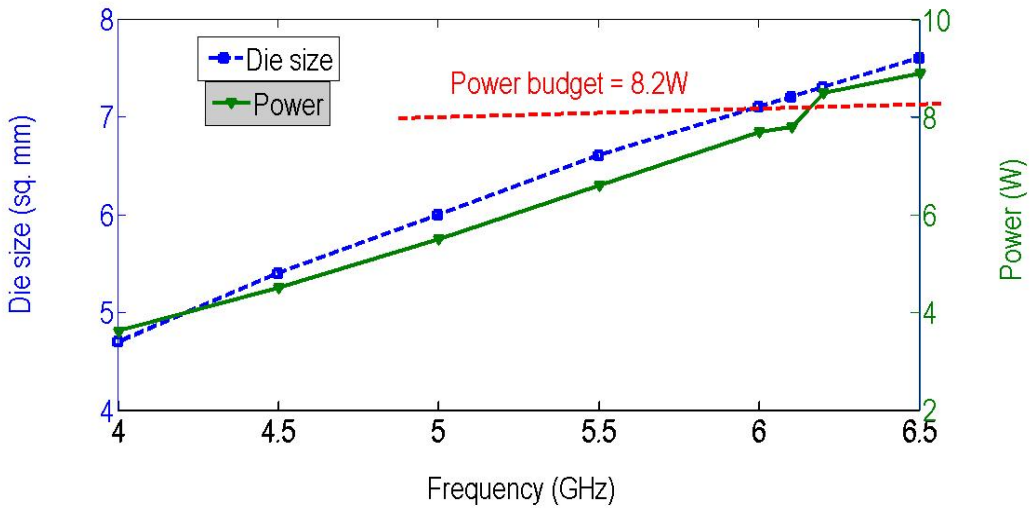


Figure 3.7: Performance optimization with multi-walled CNT interconnects.

Table 3.6 reveals the wire pitches predicted by MINDS for the chip with just copper and for the chip with both multi-walled CNT interconnects and copper. Although the chip with multi-walled CNT interconnects and the chip with copper interconnects have approximately the same power consumption, the distribution of power is different (Fig. 3.8). The clock power, interconnect power and logic gate power for the chip with multi-walled CNT interconnects are higher due to its higher clock frequency. Repeater power is lower due to the reduced capacitance and resistance associated with carbon nanotube interconnects.

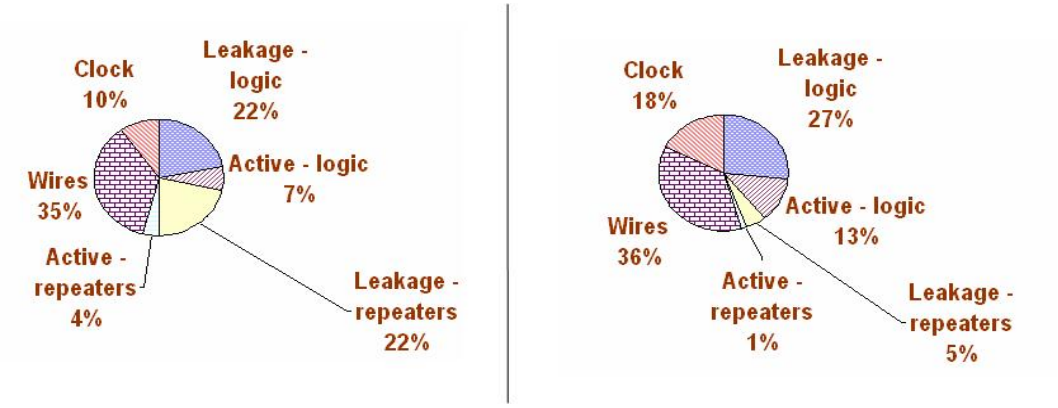
Table 3.6: Wire pitch prediction using MINDS.

Metal levels	Pitch (nm)
M1, M2	44
M3, M4	52
M5, M6	65
M7, M8	97
M9, M10	186

Case (a): Chip with copper only.

Metal levels	Pitch (nm)
M1, M2	44
M3, M4	44
M5, M6	75
M7, M8	119
M9, M10	119

Case (b): Chip with CNTs and copper.



Case (a): Copper interconnects only.

Case (b): CNT and copper interconnects.

Figure 3.8: Power consumption of logic cores.

Thus, carbon nanotube interconnects allow a 43% increase in clock frequency for a 22nm logic core with a die area reduction of 6.5%. There is a process cost penalty of having both copper and CNT interconnects on eight metal levels.

3.2.5. Conclusion

For a 4GHz 8.2W 22nm logic core with 30M gates and 10 metal levels, carbon nanotube interconnects are found to provide (a) 56% reduced power and 39% reduced die size, or (b) 43% reduced power and 12% fewer metal levels, or (c) 43% higher frequency and 6.5% reduced die size. While these are substantial benefits, carbon nanotube interconnects also come with challenges. There is a process cost overhead since eight metal levels require both carbon nanotube interconnects and copper. Fabrication of carbon nanotube interconnects is immature today and needs significant progress before being considered a contender to replace copper. To the best of the author's knowledge, this work represents the first system level comparison between carbon nanotube and copper interconnects.

3.3. A Circuit Solution: Improved Repeater Insertion Techniques

Improved repeater insertion techniques could help mitigate the repeater power issues discussed in Section 3.1. The equations in Fig. 3.9 summarize a repeater insertion model derived by the author to minimize energy-delay product (EDP). In this model, k is the number of repeaters, h is the size of repeaters i.e. the ratio of width of a repeater transistor to the width of a minimum size transistor, R_{int} is the wire resistance, C_{int} is the wire capacitance, V_{dd} is the supply voltage, b is the percentage of time the circuit is sleep gates, f is the frequency, a is the activity factor and R_o, C_o and I_{leak} are the resistance, capacitance and leakage of a minimum size repeater respectively. The derivation of this model is described in Appendix B. The repeater number and repeater size that minimize energy-delay product of wires in a 100nm technology are obtained from this model and results are compared with SPICE simulations for the same in Table 3.7. It can be observed from Table 3.7 that the error of this model is <10% for all the cases that are considered.

$$Delay = k\left[0.7\frac{R_o}{h}\left(\frac{C_{int}}{k}+hC_o\right)+\frac{R_{int}}{k}\left(0.4\frac{C_{int}}{k}+0.7hC_o\right)\right]$$

$$Power = \left(a\frac{1}{2}C_oV_{dd}^2f+bV_{dd}I_{leak}\right)hk+a\frac{1}{2}C_{int}V_{dd}^2f$$

$$Energy-delay\ product\ (EDP) = Delay^2.Power$$

Set $\frac{d(EDP)}{dh}=0, \frac{d(EDP)}{dk}=0$, simplify and approximate to get

$$k=\gamma\sqrt{\frac{R_{int}C_{int}}{R_oC_o}}, \quad h=\delta\sqrt{\frac{R_oC_{int}}{R_{int}C_o}}$$

where $\gamma=\left(0.73+0.07\log\Phi_{gate}\right)^2$, $\delta=\left(0.88+0.07\log\Phi_{gate}\right)^2$ and $\Phi_{gate}=\frac{a\frac{1}{2}C_oV_{dd}^2f}{a\frac{1}{2}C_oV_{dd}^2f+bV_{dd}I_{leak}}$

$$\text{Optimal delay} = \sqrt{R_{int}C_{int}R_oC_o}\left(\frac{0.7}{\delta}+0.7\gamma+\frac{0.4}{\gamma}+0.7\delta\right)$$

Optimal energy-delay product

$$=R_{int}C_{int}^2\left[R_o\left(a\frac{1}{2}C_oV_{dd}^2f+bV_{dd}I_{leak}\right)\left(\frac{0.7}{\delta}+0.7\gamma+\frac{0.4}{\gamma}+0.7\delta\right)^2\left(\gamma\delta+\Phi_{gate}\right)\right]$$

Figure 3.9: An energy-delay product minimization model for repeater insertion.

Fig. 3.10 illustrates that transistor area of future microchips would consist *mainly* of logic transistors, memory transistors (SRAM cells) and communication transistors (repeaters). Logic and memory transistors perform inherently different functions; they used to have the same device parameters, but this is not the case anymore. Similarly, the author proposes that logic and communication transistors also need to have their own uniquely optimized device parameters in the future. For example, communication transistors could have different values of threshold voltage (V_t) from logic transistors. The rationale behind this proposal can be obtained from the newly derived repeater insertion

model as described in the following pages of this manuscript. A 22nm microprocessor with parameters outlined in Table 3.8 is considered for analysis.

Table 3.7: Comparison of model with SPICE simulations for a 100nm technology. Transistor models [3.19] have R_o=14.1kohm, C_o=0.7fF, I_{leak}=52.5nA. Interconnect dielectric constant is 3. Repeater size is defined at the beginning of Section 3.3.

Wire width	Number of repeaters - from model	Repeater size – from model	Number of repeaters – from SPICE	Repeater size – from SPICE
100nm	2.1/mm	40	2.2/mm	40
200nm	1.05/mm	80.4	1.15/mm	80
400nm	0.52/mm	161	0.55/mm	150
600nm	0.35/mm	241	0.35/mm	240
800nm	0.26/mm	322	0.28/mm	300

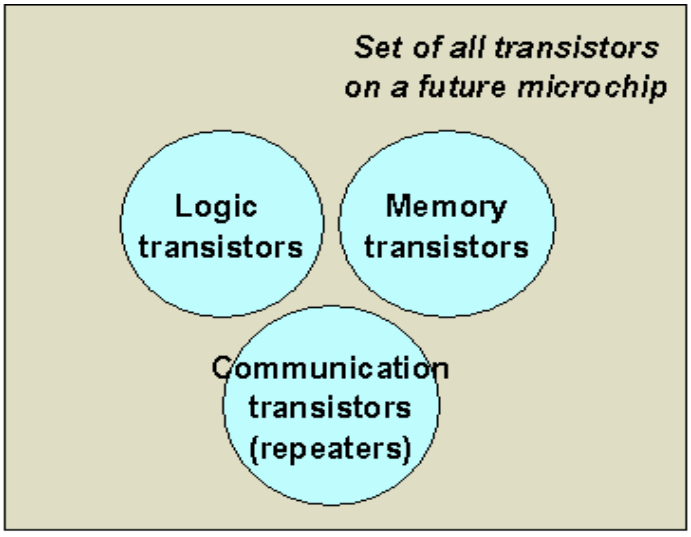


Figure 3.10: Three types of transistors in GSI chips.

Table 3.8: Parameters of a 22nm technology [3.5].

Quantity	Value
Technology node	22nm
Frequency	4GHz
Number of gates	40M
Die area	$12mm^2$
Supply voltage	0.5V
Threshold voltage	0.18V
Metal levels	10

$$\text{Optimal } EDP = R_{\text{int}} C_{\text{int}}{}^2 [R_o (a \frac{1}{2} C_o V_{dd}{}^2 f + b V_{dd} I_{leak})(\frac{0.7}{\delta} + 0.7\gamma + \frac{0.4}{\gamma} + 0.7\delta)^2 (\gamma\delta + \phi_{gate})]$$

$$\text{where } \gamma = (0.73 + 0.07 \ln \phi_{gate})^2 \text{ and } \delta = (0.88 + 0.07 \ln \phi_{gate})^2$$

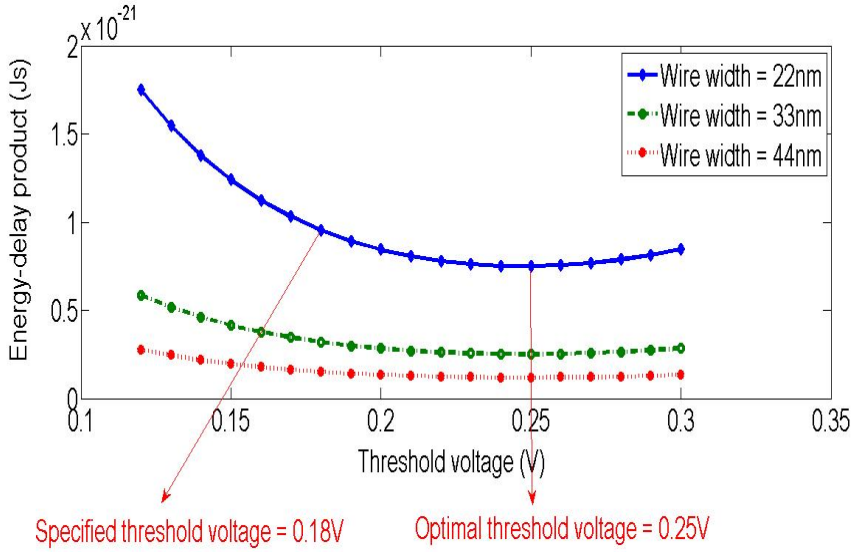


Figure 3.11: Energy-delay product for a repeated wire as a function of threshold voltage.

The repeated wire EDP vs. V_t plot of Fig. 3.11 indicates that an optimal V_t =0.25V exists for all repeated wires on a chip that minimizes their EDP. This is because the wire-independent term inside square brackets in the optimal EDP expression must be minimized to minimize EDP. Since *all* repeaters on a chip have the same optimal V_t value, a single lithography and implant step is sufficient to fix the threshold voltage for *all* repeater transistors.

Fig. 3.12 shows that delay of a repeated wire with the new model is fairly insensitive to increase in V_t near the optimal point. The delay at V_t = 0.25V is only 5% higher than the delay at V_t =0.18V. The reason for this is again evident from the model. The expression for delay of the repeated wire using the model is

$$\text{Optimal delay} = \sqrt{R_o C_o R_{\text{int}} C_{\text{int}}}\left(\frac{0.7}{\delta} + 0.7\gamma + \frac{0.4}{\gamma} + 0.7\delta\right) \quad \ldots(3.4)$$

$$\text{where } \gamma = (0.73 + 0.07\ln\phi_{gate})^2 \text{ and } \delta = (0.88 + 0.07\ln\phi_{gate})^2$$

$$R_o \text{ proportional to } \frac{V_{dd}}{(V_{dd} - V_t)^{1.3}} \text{ (by the power law MOSFET model [3.21])}$$

When V_t is increased, two terms are affected in Eq. (3.4). The term inside the square root sign increases due to the increase of repeater output resistance R_o. This has the effect of increasing the delay. However, ϕ_{gate}, the ratio of dynamic power to total power of a repeater, increases because leakage power goes down when V_t is increased. The effect of the larger ϕ_{gate} is to have larger values of γ and δ, i.e. when V_t is increased, the model inserts more repeaters and bigger repeaters. This decreases the ($0.7/\delta + 0.7\gamma + 0.4/\gamma + 0.7\delta$) term in the above equation and has the effect of decreasing the delay. An example is provided in Fig. 3.12 to illustrate this. When the V_t value is increased from 0.18V to 0.25V,

the square root term in Eq. (3.4) increases by a factor of 1.17 while the $(0.7/\delta+0.7\gamma+0.4/\gamma+0.7\delta)$ term decreases by a factor of 0.89, with the net result that the delay increases by only 5%. This delay overhead can be counteracted in a power-efficient manner by increasing wire pitch by just 3.6%.

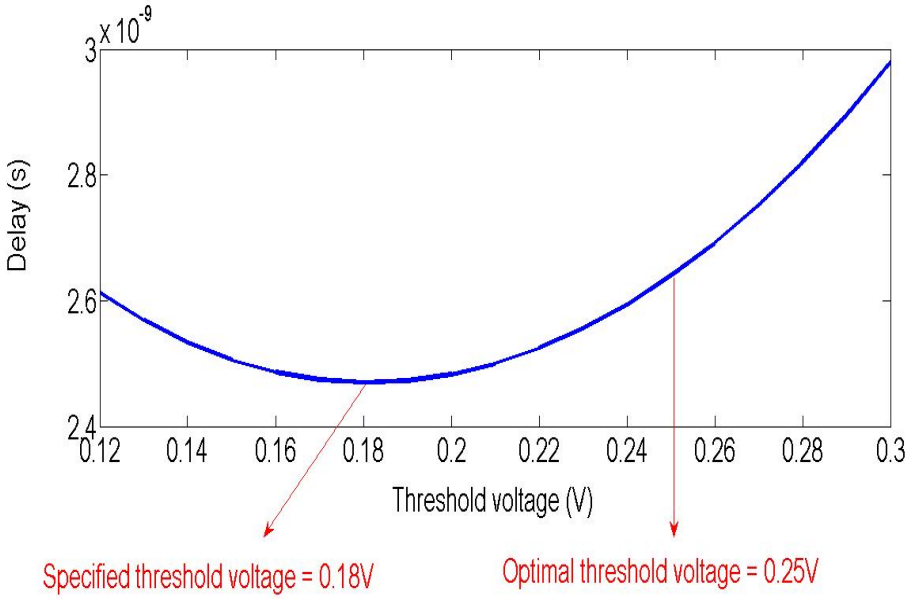


Figure 3.12: Delay of a 22nm wide 10mm long repeated wire when repeater insertion is carried out to minimize the energy-delay product.

The delay of an inverter driving a fan-out of 4 (FO4 delay) is considered to be representative of the delay of a typical logic circuit such as an ALU or a multiplexer which generally has short wires [3.22]. Fig. 3.13 shows that the delay of a fan-out of 4 inverter having average length wires is sensitive to its threshold voltage. It can be seen that if the threshold voltage is increased from 0.18V to 0.25V, the delay of the fan-out of 4 inverter increases by 38%, compared to just a 5% increase in delay of a repeated wire for the same

increase in threshold voltage. The reason for this can be understood better with the equation for delay of a fan-out of 4 inverter.

$$\text{FO4 delay} = 0.7\frac{R_o}{W}(C_{\text{int}} + C_o W)$$

Here, W is the width of an average size inverter and C_{int} is the capacitance of an average length wire. When V_t is increased, the output resistance R_o of the inverter increases and impacts the FO4 delay. As can be observed in Eq. (3.4), a repeated wire has its delay depending on the *square root* of R_o. A fan-out of 4 inverter, on the other hand, has its delay depending on R_o, and is more sensitive to increases in R_o. Fig. 3.14 reveals that a 91% increase in gate sizes is required to have the same delay at V_t = 0.25V as the delay at V_t = 0.18V. This large gate size overhead prevents increase in V_t values of logic transistors.

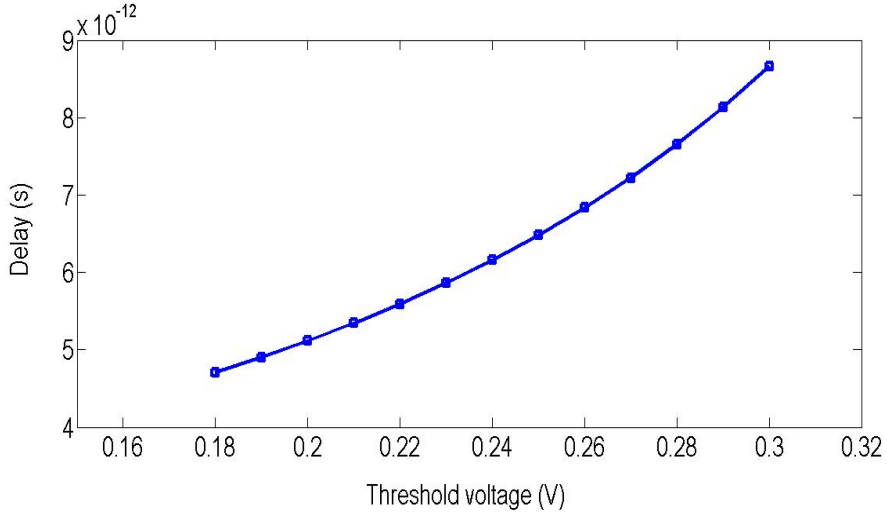


Figure 3.13: Fan-out of 4 inverter delay for a 22nm technology.

To summarize the results obtained in the last few pages, optimally repeated wires can have higher threshold voltages than specified. This is because their delay is not sensitive to threshold voltage. Any small delay increases can be counteracted power-efficiently by using slightly larger wires. On the other hand, the delay of logic circuits increases substantially with increase in threshold voltage. This is because there does not exist any technique to compensate the delay penalty when threshold voltage values are increased. Thus, an optimized GSI chip would have higher threshold voltages for its repeater transistors compared to its logic transistors. Using the same arguments, an optimized GSI chip could also have longer channel lengths and/or thicker gate oxides for its repeater transistors compared to its logic transistors. To the best of the author's knowledge, this is the first time this idea has been proposed.

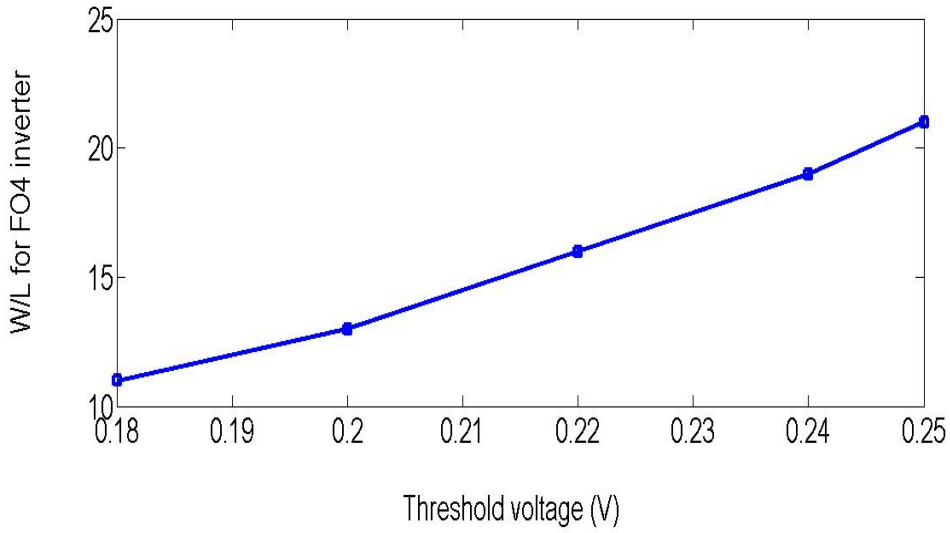


Figure 3.14: Percentage increase in gate sizes required to have the same FO4 delay at the specified threshold voltage as the delay at threshold voltage = 0.18V.

Table 3.9 shows power benefits of the EDP repeater insertion methodology when it is compared to the commonly used sub-optimal repeater insertion model for a 22nm technology with supply voltage=0.5V and threshold voltage=0.18V. The EDP model with unique threshold voltage values for logic and repeater transistors would reduce power of a repeated wire by 53% for 13% higher wire size. The total repeater area for this case is less than the total repeater area for the sub-optimal repeater insertion model.

Table 3.9: Power consumption for different repeater insertion models for a 22nm 10mm wire.

Repeater insertion model	Repeater number	Repeater size	Wire pitch (nm)	Delay (ns)	Power (μW)
Bakoglu [3.23]	766	27	44	2.07	384
Sub-optimal model [3.2]	346	30	47	2.07	223
EDP model	293	19	51	2.07	147
EDP model with unique V_t values for logic and repeaters	307	28	53	2.07	105

The benefits of these repeater insertion techniques are analyzed with MINDS at the system level for the 22nm 40M gate logic block considered in Section 3.1. *Table 3.10 indicates power savings obtained when the EDP model is used along with unique threshold voltage values for logic and repeater transistors. A 26% reduction in total logic block power is obtained for a 9% increase in the number of wire levels.* Repeater power, in particular, is lowered by 78%, while repeater area is reduced by 33%.

Table 3.10: Benefits of energy-delay product based repeater insertion for a 22nm logic block.

	Sub-optimal model	New EDP model with unique threshold voltage values for logic and repeaters
Die area	$12mm^2$	$12mm^2$
Wire pitches of pairs of metal levels (nm)	44, 45, 60, 93, 250	44, 57, 60,109, 109, 285
Power	Total = 17.4W Logic gates = 5.7W Repeaters = 5.8W Wires = 4.5W Clock = 1.5W	Total = 12.9W Logic gates = 5.7W Repeaters = 1.25W Wires = 4.5W Clock = 1.5W
Number of metal levels	9.3	10.1
Repeater area	$3.6mm^2$	$2.4mm^2$
Number of repeaters	9.6 million	5.8 million

3.4. An Architectural Solution: Parallel Processing Architectures

In the early 1990s, Chandrakasan, Sheng and Brodersen proposed the use of parallel processing architectures as a potential technique to reduce power [3.20]. The impact of that early work has been substantial, with several multi-core processors available today. This section studies the implications of such parallel processing architectures on signal interconnect networks. Single core, dual core and quad core chips depicted in Fig. 3.15 are compared for this purpose.

Fig. 3.15 shows that while the single core chip is clocked at 10GHz, the dual core chip is assumed to have two 5GHz cores, and the quad core chip is assumed to have four 2.5GHz cores. If software is completely parallel, which is the case for many

high-performance applications, these three architectures would have the same throughput. Note that Chandrakasan, Sheng and Brodersen compared similar systems for their work [3.20]. The single core chip is taken to have 60% of its area, i.e. 45mm^2, consumed by cache memory [3.2]. Hence, the dual core and quad core chips are taken to have 45mm^2 of cache memory as well.

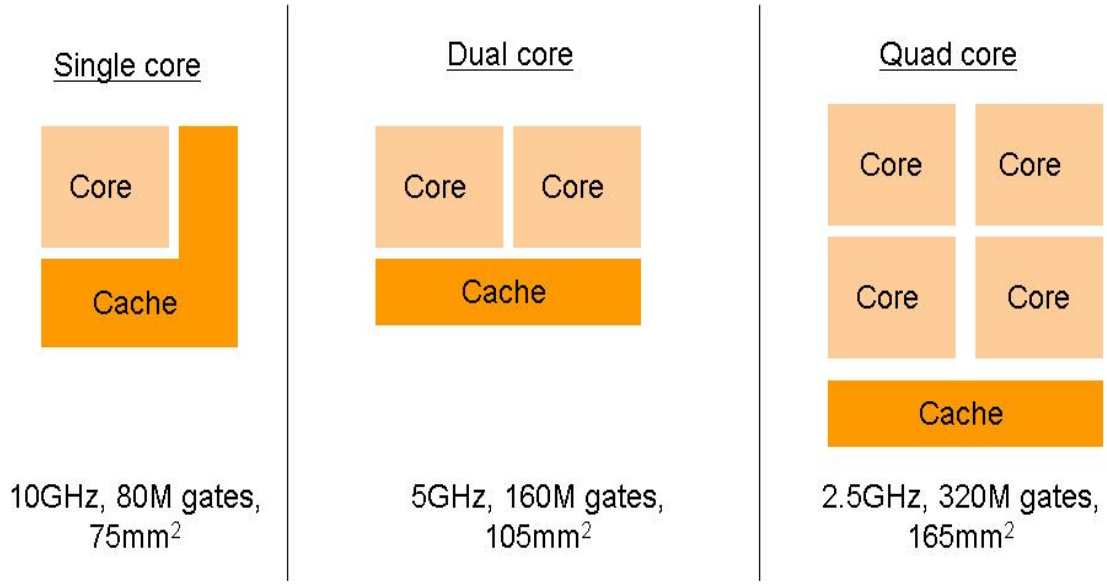


Figure 3.15: Single core, dual core and quad core chips used for case study. A 22nm device technology is considered.

3.4.1. Intra-Core Interconnect Networks

The interconnect networks within a core are first analyzed. Multiple simulations are run in MINDS with different supply and threshold voltage values such that the total power of logic cores is minimized. The chosen supply and threshold voltages and power consumption of 10GHz, 5GHz and 2.5GHz logic cores are summarized in Table 3.11. As

can be observed, supply voltages can be lowered and threshold voltages can be raised with multiple lower frequency cores. This is due to the reduced performance requirements associated with lower frequencies [3.20]. This results in a reduction in both dynamic and leakage power. Different components of the power of each core are listed in Table 3.12.

Table 3.11: Optimized supply and threshold voltage.

	Single core 10GHz chip	Dual core 5GHz chip	Quad core 2.5GHz chip
Supply voltage	0.75V	0.58V	0.48V
Threshold voltage	0.18V	0.22V	0.24V
Total power of logic cores	167W	78W	49.2W

Table 3.12: Components of power for each logic core.

	10GHz 30mm^2 80M gate core	5GHz 30mm^2 80M gate core	2.5GHz 30mm^2 80M gate core
Dynamic power of logic gates	27W	4W	0.8W
Leakage power of logic gates	24W	3.6W	1.1W
Dynamic power of repeaters	7W	4.5W	0.8W
Leakage power of repeaters	11W	2.8W	2W
Interconnect power	61W	18W	6.2W
Clock power	36W	5.6W	1.2W

The interconnect requirements for these three logic cores are obtained with MINDS and are shown in Table 3.13 and Fig. 3.16. Table 3.13 indicates that the dual core chip has smaller wire pitches than the single core chip and the quad core chip has smaller wire pitches than the dual core chip. This is because MINDS equates RC delay of the longest wire in each pair of metal levels to a certain fraction of the clock frequency for evaluating wire pitch. Eq. (3.1) and Eq. (3.2) (reproduced on the following page) describe this condition. It should be noted that Eq. (3.2) is modified to reflect the fact that an energy-delay product based repeater insertion methodology is used for this analysis.

$$\tau_{rc} = \frac{2.2\rho c l^2}{P^2} = \frac{\beta}{f} \qquad \text{for unrepeated wires, and}$$

$$\tau_{rc} = \frac{l\sqrt{2\rho c R_o C_o}}{P}\left(\frac{0.7}{\delta} + 0.7\gamma + \frac{0.4}{\gamma} + 0.7\delta\right) = \frac{\beta}{f} \text{ for repeated wires}$$

These equations indicate clearly that when clock frequencies are lowered for a logic core, the wire pitch reduces for both repeated and unrepeated wires. This helps explain the trend shown in Table 3.13.

When wire pitches are reduced, the area needed for routing wires also reduces. For a fixed die area, the number of interconnect levels is decided by the area needed for routing wires. Thus, multiple core lower frequency chips with smaller wire pitches would require a fewer number of metal levels. Fig. 3.16 reveals that the dual core chip needs 25% fewer metal levels for intra-core communication than the single core chip. The quad core chip needs 38% fewer metal levels for intra-core communication than the single core chip.

Table 3.13: Pitches of metal levels for the considered logic cores.

	10GHz 30mm^2 80M gate core	5GHz 30mm^2 80M gate core	2.5GHz 30mm^2 80M gate core
M1, M2 pitch	44nm	44nm	44nm
M3, M4 pitch	81nm	54nm	47nm
M5, M6 pitch	83nm	73nm	64nm
M7, M8 pitch	134nm	103nm	97nm
M9, M10 pitch	141nm	171nm	262nm
M11, M12 pitch	199nm	415nm	
M13, M14 pitch	292nm		
M15, M16 pitch	650nm		

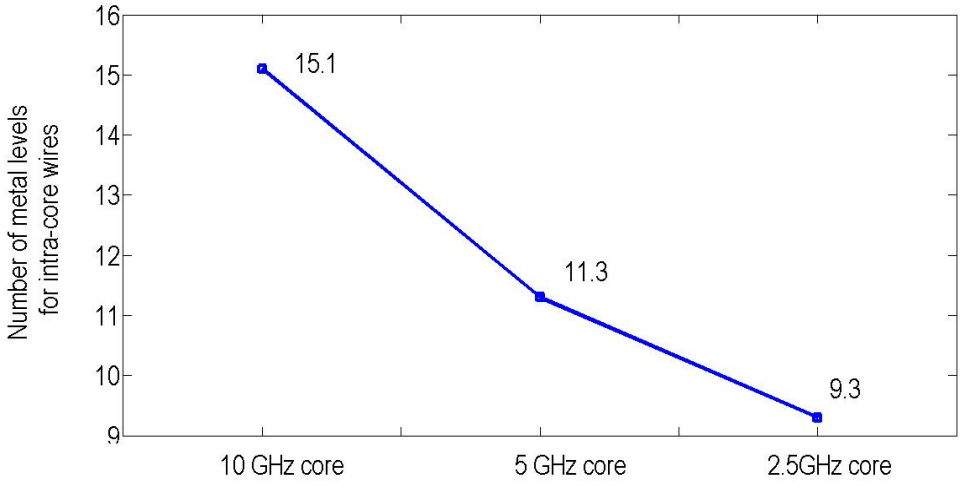


Figure 3.16: Number of interconnect levels required for intra-core wiring.

MINDS provides another interesting result. Table 3.14 reveals that while a benchmark 1mm wire for the 10GHz single core chip is routed in a 134nm pitch metal level, the same

wire is routed in a 103nm pitch metal level for the 5GHz dual core chip and in a 47nm pitch metal level for the 2.5GHz quad core chip. It is well known that copper resistivity increases exponentially with smaller wire dimensions [3.7]. A resistivity calculation using compact models in [3.7] show a 91% increase in resistivity of a 1mm wire as one moves from the 10GHz single core chip to the 2.5GHz quad core chip. It reveals that the impact of copper resistivity increases due to size effects would be more pronounced in lower frequency parallel processing architectures.

Table 3.14: Impact of size effects in parallel processing architectures.

	10GHz 30mm^2 80M gate core	5GHz 30mm^2 80M gate core	2.5GHz 30mm^2 80M gate core
Pitch of metal level used for routing 1mm wire	134nm	103nm	47nm
Resistivity of metal level used for routing 1mm wire	3.3uohm-cm	3.8uohm-cm	6.3uohm-cm

3.4.2. Inter-Core Interconnect Networks

Currently available dual core and eight core chips use a crossbar switch for inter-core communication [3.24][3.25]. For this reason, a crossbar is considered in this work as well. Publications on the above mentioned dual core chip [3.24] suggest that 144 byte lines are needed for its inter-core wiring. The eight core chip [3.25] uses a 134 GB/s crossbar for inter-core wiring. In this thesis, it is assumed that each core has a dedicated connection from its center to its crossbar. This connection has an aggressive bandwidth of 512GB/s in

each direction, and is shown in Fig. 3.17. The topmost metal layer pitch for intra-core wiring of each chip in the case study is used for routing inter-core busses as well.

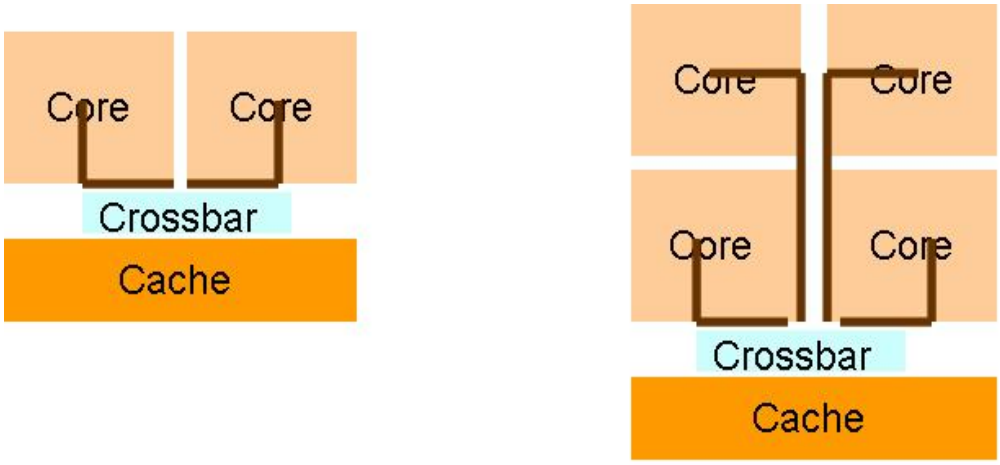


Figure 3.17: Inter-core communication network of dual core and quad core chips.

The number of wiring levels needed for inter-core wiring of the 5GHz dual core chip is obtained as follows: If *a* is the length of each side of the logic core, the longest wire in the stochastic wiring distribution of each core has length = 2*a*. Its bandwidth is 5Gbps, since its delay is equal to the clock period and clock frequency is 5GHz. The bandwidth of each wire of the bus from the center of a core to the crossbar (shown in Fig. 3.17) is thus 10Gbps, since the bus length is *a*. To get 512 GBps in each direction, we need 512Gbps*8bits/10Gbps*2directions=819 wires. Since each wire has a pitch of 415nm and length of '*a*' for the dual core case, the area needed for each bus to the crossbar assuming 40% wiring efficiency = 819 wires* 415nm**a*/0.4 = 4.7mm^2. As the wiring area available for each metal level is 30mm^2, the bus to the crossbar takes up 16% of each metal level.

Similar calculations for the four core chip suggest the bus from each of its cores to the crossbar takes up 39% of a metal level. *Thus, as the number of cores increases, the wiring overhead of inter-core wiring increases. This overhead, however, is small compared to the intra-core wiring, in spite of the aggressive bandwidth chosen for the inter-core wiring busses.*

Table 3.15: Inter-core communication overheads.

	Dual core 5GHz chip	Quad core 2.5GHz chip
Metal levels for inter-core communication	16% of one metal level	39% of one metal level
Power overhead of inter-core communication	6W	8W

Evaluation of the power overhead of the inter-core communication network is difficult. It depends on the design of the crossbar switch, the extent of parallelism in the software (which decides the activity factor of the buses) and cache coherence protocols. The power overhead of inter-core communication for the dual core chip is roughly assumed to be 8% of the total power of the cores based on previous work [3.20]. Similar estimates obtained for the power overhead of the quad core chip's inter-core communication network are shown in Table 3.15. Although these power estimates are approximate and are not rigorously obtained, the error in total power is minimal due to the small values of these numbers (when compared to the total power of logic cores obtained in Table 3.11).

3.4.3. Intra-Core and Inter-Core Communication Networks

Combining the results from Section 3.4.1 and Section 3.4.2, one can obtain the results shown in Table 3.16.

Table 3.16: Summary of results.

	Single core 10GHz chip	Dual core 5GHz chip	Quad core 2.5GHz
Number of metal levels considering both intra-core and inter-core communication	15.1	11.5	9.7
Total power considering logic cores and inter-core network	167W	82W	57W
Power density	550W/cm^2	137W/cm^2	48W/cm^2
Die area	75mm^2	105mm^2	165mm^2

It can be observed that the dual core chip requires 24% fewer metal levels than the single core chip and the quad core chip requires 35% fewer metal levels than the single core chip. Table 3.16 also reveals that the power and power density drop dramatically due to reduced frequency parallel processing architectures, as predicted by Chandrakasan, Sheng and Brodersen [3.20]. In particular, the single core 10GHz chip has an unacceptable power density of 550W/cm^2. To put this in perspective, the maximum power density that can be cooled with today's air cooled heat sinks is about 100W/cm^2 [3.26]. The dual core chip reduces the power density by a factor of almost four while the quad core chip provides an order of magnitude reduction in power density. In today's data centers where power and cooling costs are comparable to server hardware costs, this tremendous reduction in power

and power density provides a significant reduction of cost of ownership of a server. *The contribution of this work is the finding that the number of metal levels reduces significantly with parallel processing architectures*. This, in the author's opinion, is another attractive benefit of parallel processing, which along with the power and power density decrease, would make parallel processing architectures more attractive. The main drawback is the die area increase depicted in Table 3.16. However, the significant reductions in power, power density and number of metal levels seem promising enough to overlook this die area penalty (at least for the transition from single core to dual core). This is primarily because power and cooling costs are comparable to hardware costs in today's data centers. *Another interesting result from this study is the increased impact of copper size effects in parallel processing architectures.*

3.5. Summary

Signal interconnect networks are projected to play an important role in future GSI chips. For a high-performance logic core constructed in a 22nm technology, signal interconnects are predicted to consume 35% of the total power while repeaters are predicted to consume 26% of the total power. Interconnects also contribute to more than half the total number of lithography steps to a CMOS process, thus impacting cost of a GSI chip significantly. Several techniques are studied to tackle these issues.

For a 4GHz 8.2W 22nm logic core with 30M gates and 10 metal levels, carbon nanotube interconnects are found to provide (a) 56% reduced power and 39% reduced die size, or (b) 43% reduced power and 12% fewer metal levels, or (c) 43% higher frequency and 6.5% lower die size. The drawback of using these interconnects is the increased

process cost of utilizing both carbon nanotube and copper interconnects in various metal levels. Of course, this analysis assumes carbon nanotube technology will be mature enough to be manufacturable.

A compact model to minimize energy-delay product of a repeated wire is derived. This model has less than 10% error when compared to SPICE simulations. It is also found that utilizing uniquely optimized device technologies for logic and repeater transistors is beneficial to future GSI chips. To the best of the author's knowledge, this represents the first time this idea has been proposed. The above energy-delay product based repeater insertion technique, when used along with uniquely optimized threshold voltage values for logic and repeater transistors, is found to provide a 26% reduction in power for a 9% increase in number of metal levels for a 22nm 4GHz logic core.

Architectures where multiple logic cores run at lower frequencies are found to give a 24%-35% reduction in number of metal levels compared to architectures which have a single high-frequency core. It is also found that these lower frequency parallel processing architectures are impacted more by size-dependent resistivity increases in copper.

CHAPTER 4

POWER INTERCONNECT NETWORKS

There are three main concerns for on-chip power interconnect network design in GSI chips [4.1]: (a) IR drop – This is the resistive drop in the power distribution network. (b) Simultaneous switching noise – This represents the potential drop across the inductance of the packaging and solder bumps. Decoupling capacitors are typically added to the on-chip power distribution network to compensate this drop. (c) Electromigration (EM) – This is a reliability issue caused by long-term current flow through copper wires and solder bumps. Three-dimensional integrated circuits have higher current densities than two-dimensional ones, and therefore face even more significant challenges with the three issues mentioned above.

Power supply noise in integrated circuits is typically restricted to 10% of the supply voltage [4.1] due to noise margin considerations. With the reduced supply voltages and increased chip currents that accompany CMOS scaling, this goal has become tougher to reach due to IR drop and simultaneous switching noise concerns. Electromigration is also exacerbated with scaling due to the increased chip currents and feature size reduction for on-chip interconnects, vias and solder bumps. This, in turn, leads to higher current densities through these components. This chapter is organized as follows. Section 4.1 provides the summary of a technique proposed by the author to reduce EM in solder bumps and on-chip global power distribution networks. Section 4.2 describes a technique to reduce IR drop and Ldi/dt noise issues in future GSI chips. Section 4.3 discusses power distribution in 3D GSI chips. The chapter concludes with a summary in Section 4.4. The

work in this chapter has been described by the author in [4.2] and [4.3].

4.1. Electromigration Resistant Power Delivery Systems

Current is normally fed from an off-chip DC-DC converter to transistors on the processor through a printed wiring board, a package, solder bumps and chip-level global interconnects (Fig. 4.1). Electromigration concerns could make the transfer of such high currents through many of these interconnections difficult. In fact, the ITRS predicts that current density per solder bump would reach $4x10^4$ A/cm^2 at the 32nm node, and that EM would necessitate material changes. In the long term, the ITRS says a new solder technology may need to be invented that can tolerate higher current densities. Temperature increases in the package and higher levels of on-chip interconnect stacks exacerbate the above EM concerns [4.4][4.5]. For example, [4.4] shows experimental data which indicate that chip-level solder bump temperature can be 30^{o}C higher than that of the transistors. Fig. 4.2 is an IR thermal image showing temperature increases in the packaging of an Intel microprocessor [4.4].

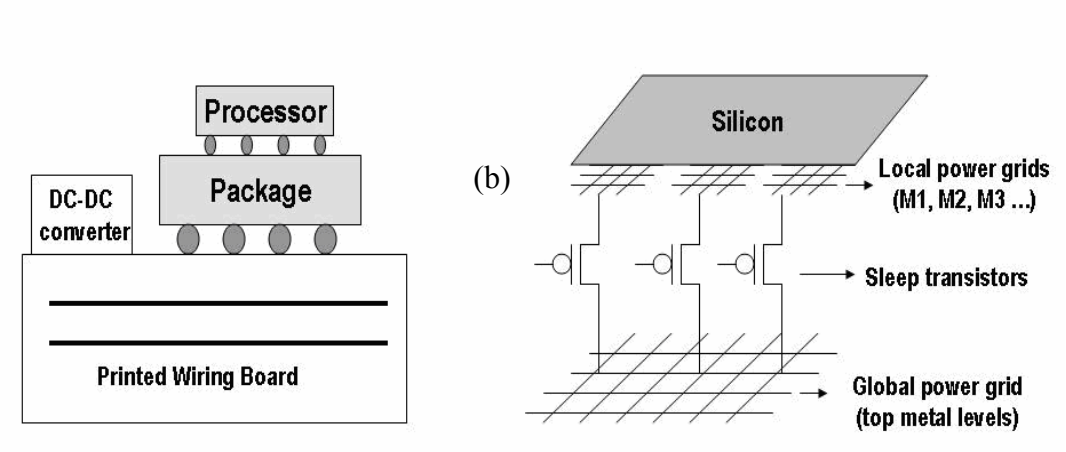


Figure 4.1: (a) Current delivery path for a microprocessor. (b) On-chip power distribution network. Sleep transistor symbols are drawn as shown for convenience.

It has been known for the last 10-15 years that EM lifetimes for AC (TTF_{AC}) are several orders of magnitude higher than DC lifetimes (TTF_{DC}) [4.6][4.7]. Dependence of EM on AC frequency f is normally understood with the following model [4.6][4.7].

$$\begin{aligned} TTF_{AC} &= TTF_{DC} \qquad \text{when } f \le 1/2TTF_{DC} \\ &= 2f(TTF_{DC})^2 \quad \text{when } f > 1/2TTF_{DC} \\ &\approx 1000TTF_{DC} \quad \text{for high AC frequencies} \end{aligned} \qquad \ldots(4.1)$$

Eq. (4.1) has been confirmed with experimental data for several interconnect and via materials such as Cu, Al, Al/Cu and W [4.4][4.5]. Power wires and bumps carrying DC are thus the bottleneck for EM lifetimes of a system because signal wires and bumps normally carry AC [4.6][4.7]. This work proposes a way to deliver high currents through the bumps and chip-level global wiring of a power delivery system with reduced EM.

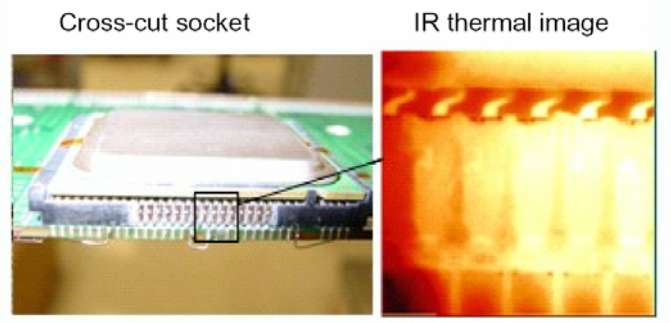


Figure 4.2: Temperature increases in the packaging of an Intel microprocessor [4.4].

4.1.1. Proposed Technique

The power delivery system for a microprocessor can be represented as shown in Fig. 4.3. On-chip sleep transistors [4.8] T1 and T2 are used to cut off the power supply from inactive circuit blocks and reduce leakage power. These sleep transistors are normally

placed between on-chip global power distribution networks and on-chip local power distribution networks as shown in Fig. 4.1(b) [4.8]. It can be seen from Fig. 4.3 that current flow through the power delivery system is unidirectional, causing EM concerns.

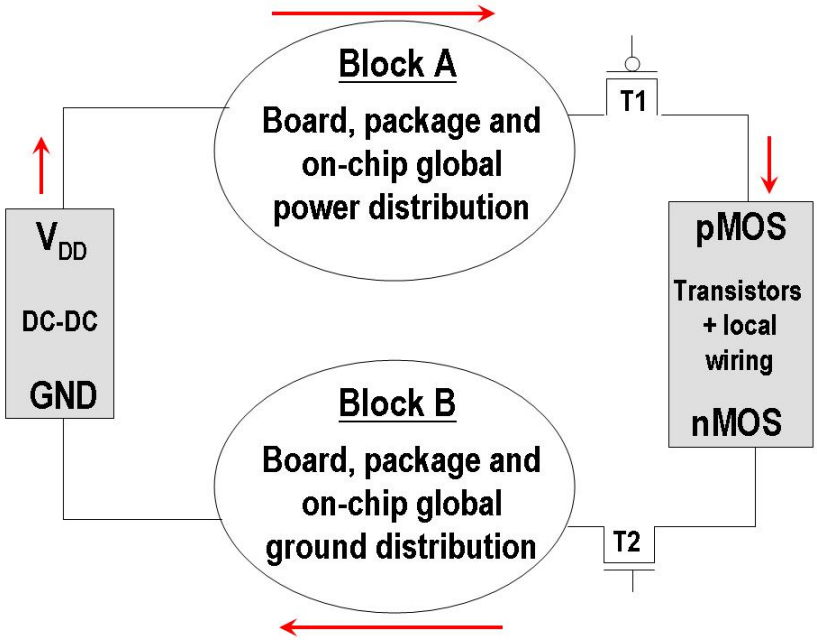
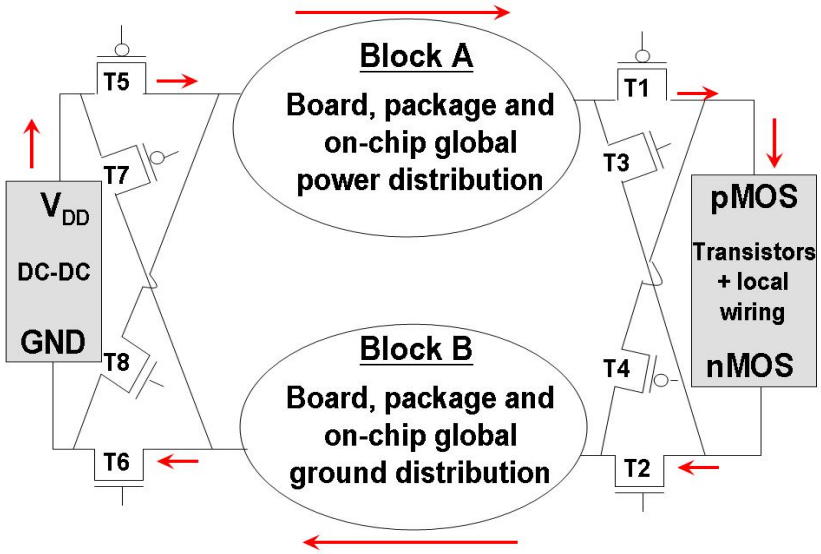


Figure 4.3: Unidirectional current flow in a standard power delivery system.

The author suggests the alternate power delivery system which is depicted in Fig. 4.4. Two on-chip sleep transistors, T3 and T4 are added. Four FETs (T5, T6, T7 and T8) are also added at the output of the DC-DC converter. This modified power delivery system works as follows: During the first power-up of the processor, T1, T2, T5 and T6 are ON while T3, T4, T7 and T8 are OFF. Fig. 4.4(a) indicates the direction of current flow in this case.

(a)



(b)

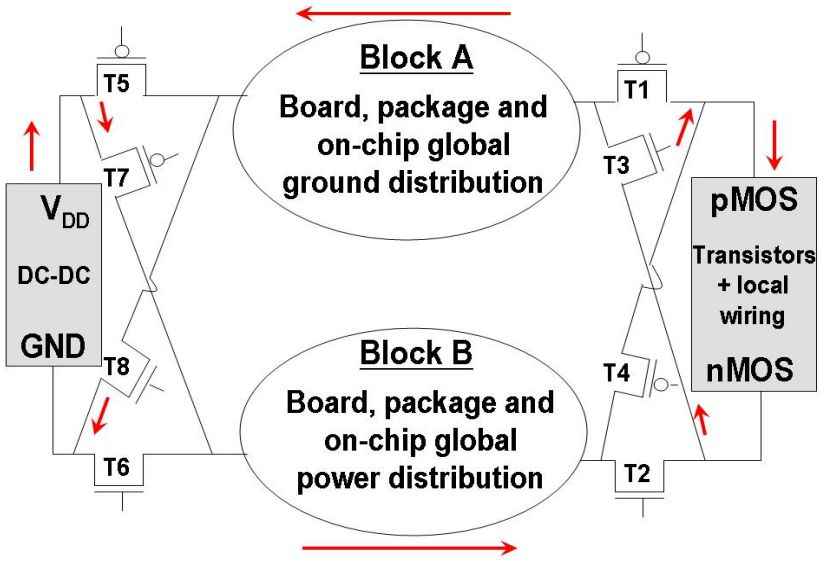


Figure 4.4: Schematic of the newly proposed power delivery system when the microprocessor is (a) powered up the first time, and (b) powered up the second time. Current direction is indicated with arrows.

When the user shuts down his computer and boots it up again, T1, T2, T5 and T6 are turned OFF while T3, T4, T7 and T8 are turned ON as shown in Fig. 4.4(b). This results in current through the board, package, solder bumps and on-chip global wires reversing, as shown in Fig. 4.4(b). Fig. 4.4 shows that current received by the on-die transistors is always in the same direction. Switching between Fig. 4.4(a) and 4.4(b) continues every time the processor is shut down and restarted. Thus, bidirectional current flows through the power delivery system and causes EM time-to-failure to improve for solder bumps, board/package wiring and on-chip global wires. It should be kept in mind that MOSFETs T5, T6, T7 and T8 need high W/L ratios to reduce I^2R losses. Sleep transistors T3 and T4 have the same size as T1 and T2, and therefore take 1%-6% of the die area of the chip [4.9][4.10].

4.1.2. Measurements

Assuming (i) the microprocessor is turned on/off once a day, and (ii) DC EM lifetime =10 years, Eq. (4.1) predicts that EM lifetimes for the new power delivery system shown in Fig. 4.4 could be as much as 1000 times higher than that of the standard power delivery system shown in Fig. 4.3. However, practical constraints such as varying processor on/off times, current variations with workload and non-uniform current density across the die would reduce benefits of this scheme. It is difficult to estimate how much these factors would affect efficiency of the proposed system. However, it should be noted that with a DC EM lifetime of 10 years and a processor switched on/off once a day, the total on/off cycles is 3650. The law of large numbers [4.11] suggests that a certain amount of averaging of the above variations would occur. Since EM with a non-symmetric AC stress depends on average DC value [4.7], this could reduce impact of the above non-idealities.

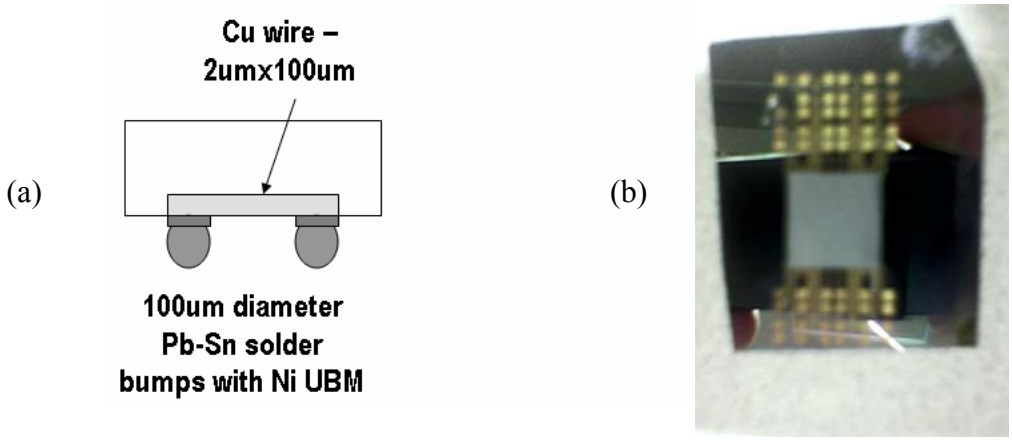


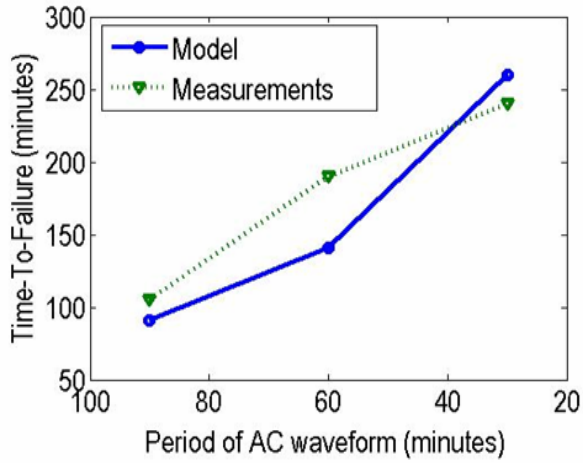
Figure 4.5: (a) Schematic of test structure. (b) Chip fabricated for testing.

A simple experiment was conducted with bumps made of eutectic solder to show operation of the proposed EM resistant systems. A structure shown in Fig. 4.5(a) was fabricated and 4A of current was passed at 115^{o}C. A 30% resistance increase was chosen as the failure criterion. Fig. 4.5(b) is a picture of the chip having the structure shown in Fig. 4.5(a).

Testing revealed that the DC lifetime was 65 minutes. The polarity of DC was changed periodically as shown in Fig. 4.4. EM lifetimes were obtained and are plotted in Fig. 4.6(a). The results indicate that the EM lifetimes with bi-directional current follow Eq. (4.1) quite well. SEMs of normal and failed solder bumps are shown in Fig. 4.6(b). It can thus be concluded that the proposed power delivery system shown in Fig. 4.4 significantly improves EM lifetimes of solder bumps and on-chip global interconnects. The improvement in I/O interconnect EM obtained with this technique could enable use of

novel packaging technologies such as conductive adhesives that suffer from EM issues [4.12].

(a)



(b)

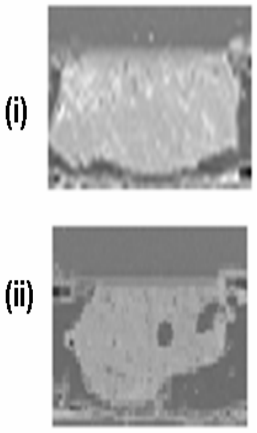


Figure 4.6: (a) Comparison of measurements with Eq. (4.1). (b) SEM image of solder bump (i) before failure (ii) after failure.

The two added sleep transistors, T3 and T4, are connected between power and ground wirings and consume leakage power. The power consumed by these transistors at the 32nm node can be computed based on sleep transistor sizing models given in [4.13] and ITRS device technology parameters. Assuming chip power is 100W and sleep transistors are high threshold voltage (V_t) devices with 0.15V higher V_t [4.13] than ITRS low V_t transistors, the total leakage power consumed by T3 and T4 would be 0.3W. One concern with switching power and ground networks as shown in this chapter is that a printed wiring board normally has other chips sharing a common power and/or ground connection with the processor. These additional chips would need to have their power and ground networks switched with sleep transistors to implement this scheme. The large EM benefits possible

with this technique could encourage its implementation in spite of the above weakness, especially for applications that are EM critical, such as automotive electronics [4.14], 3D stacked high-performance microprocessors and military electronics.

4.1.3. Conclusions

This work, for the first time, proposes interchanging power and ground networks of a microprocessor chip every time it is rebooted. This helps improve solder bump EM, a serious challenge for future technology generations, by as much as three orders of magnitude. This can be achieved without the need for material changes. Joule Heating induced EM concerns with solder bumps, on-chip global wires and on-chip global vias can also be reduced. This technique could be particularly useful in the fast-growing automotive electronics market. Reliability, and not performance, is the driver for integrated circuits built for these applications [4.14][4.15]. Chips for automotive applications typically operate around 150^{o}C [4.15][4.16], and solder bump EM is an important concern since these temperatures are close to the melting point for solder [4.15][4.16]. High-performance 3D integrated circuits consume significantly high currents as well, and would benefit from this technique.

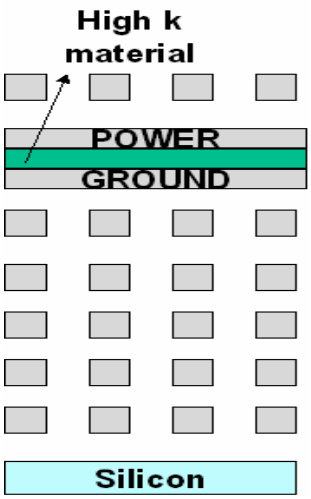
4.2. MIM Power-Ground Plane Decoupling Capacitors

Currently available high-performance microprocessors typically use grid structures for power distribution and MOS capacitors for decoupling power supply noise. Unfavorable scaling trends with chip currents, supply voltages, MOS capacitor leakage and wire resistance, however, are causing severe challenges to this power distribution architecture. The trend towards Silicon-on-Insulator wafers that significantly worsen power supply noise is another issue [4.17].

4.2.1. Proposed Technique

An improved power distribution architecture that uses on-chip power and ground planes separated by a high k dielectric is depicted in Fig. 4.7. The experimental data below gives a proof-of-concept demonstration that large area power and ground planes separated by a high k dielectric can be manufactured with good yield. A low temperature process was used to fabricate and test 3000 1mm x 1mm MIM (metal-insulator-metal) capacitors with a Ta_2O_5 dielectric (dielectric constant=25) and 1um thick copper layers. Measurements showed that for a 400nm Ta_2O_5 dielectric, the capacitance was 47nF/cm^2 and the breakdown voltage was higher than 100V. Not even a single defect was detected among the 3000 capacitors tested, indicating excellent quality of the manufacturing process. For a 200 nm thick dielectric, the measured capacitance was 77nF/cm^2 and breakdown occured at 5MV/cm. Only one defect was detected among the 3000 capacitors fabricated. I-V curves of the measurements are shown in Fig. 4.8(a). 1cm x 1cm and 4cm x 4cm capacitors were also fabricated with good yield.

(a)



(b)

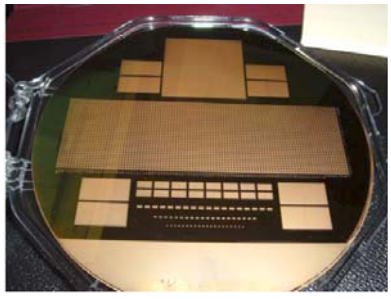
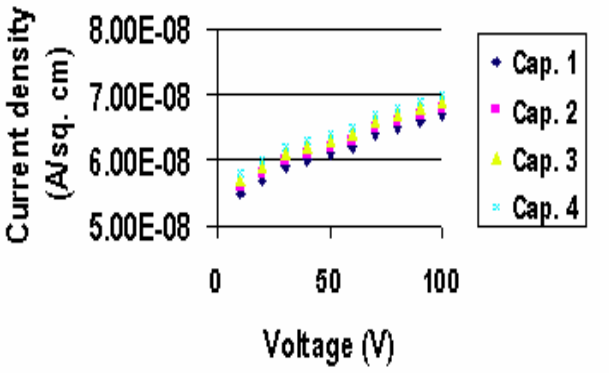


Figure 4.7: (a) Proposed MIM power-ground plane capacitor structure (henceforth referred to as MIM plane decaps). (b) Test structure.

To test if the dielectric was scalable to thinner dimensions, 2.5nm and 6nm dielectrics were deposited in an oxide-metal-silicon structure and probed with a Hg probe. Fig. 4.8(b) shows a TEM of the structure. At 1-2V, measured leakage currents were small (of the order of 10nA/cm^2), indicating scalability of the PVD process to thin dielectric layers. This behavior was reproduced at all points on the PVD film indicating its uniformity. This experiment indicates that several orders of magnitude improvement in capacitance density are possible beyond the 77nF/cm^2 value measured in the previous page. The requirement for this is that sufficiently planar capacitor electrodes are available. The experimental data in this section represent the results of the author's collaboration with Symmorphix Inc, a startup company based in Silicon Valley.

(a)



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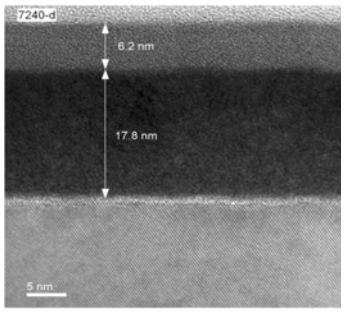


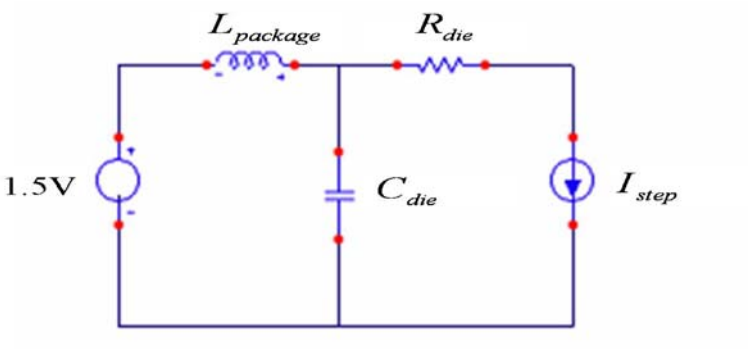
Figure 4.8: (a) I-V curve for capacitor with 400nm dielectric. (b) TEM of a 6nm Ta_2O_5 layer above a 17nm Ta electrode.

4.2.2. Benefits for Power Delivery

A power plane is essentially a very fine power grid where the grid segments are right next to each other. Using the IR drop equation in [4.1] and comparing the on-chip IR drop

of a power plane to that of an equal thickness commercial microprocessor global power grid [4.16], it is found that the IR drop for the power plane case is about 25% that of the grid.

(a)



	Symbol	Baseline	MIM plane decap
Power grid resistance	R_{die}	0.34Ω	0.08Ω
On-die decoupling cap.	C_{die}	300nF	Cap.Density *4cm^2
Package inductance	$L_{package}$	3.3pH	3.3pH
Current step	I_{step}	40A	40A

(b)

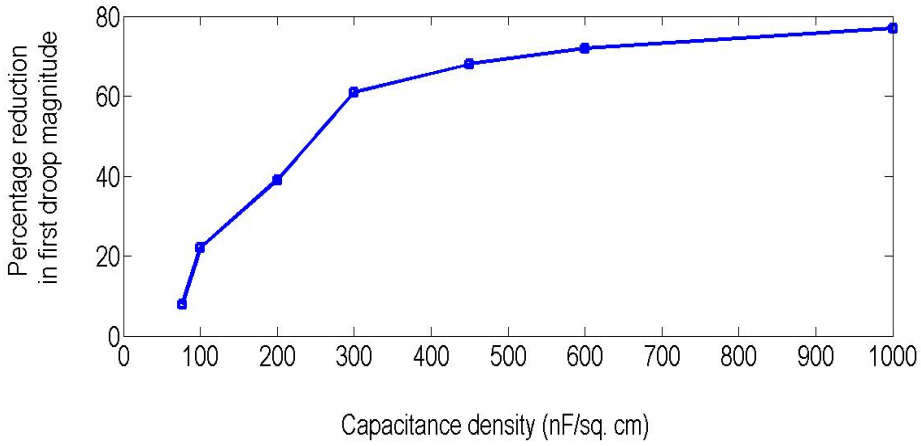


Figure 4.9: (a) Power delivery network used for analysis. (b) Reduction in first droop magnitude.

A lumped element power delivery system model (Fig. 4.9) is simulated in SPICE to get an approximate estimate of the simultaneous switching noise caused by package inductance (called the first droop). Fig. 4.9 shows that a 8% reduction in first droop magnitude can be obtained by using a MIM plane decap arrangement with 77nF/cm^2 instead of a grid-based power delivery system with 300nF transistor decoupling capacitance [4.18]. A 61% reduction in first droop magnitude can be obtained by using a MIM plane decap arrangement with 450nF/cm^2.

4.2.3. Benefits for Clock Distribution

Fig. 4.10(a) shows a clock wire of a commercial chip [4.18] that has shields to provide nearby return paths. When ground planes are present as shown in Fig. 4.10(b), they (i) provide nearby return paths for the clock transmission line, allowing coplanar shields to be placed further away from the clock wire to reduce capacitance, and (ii) reduce return path resistance. Both of these improve latency.

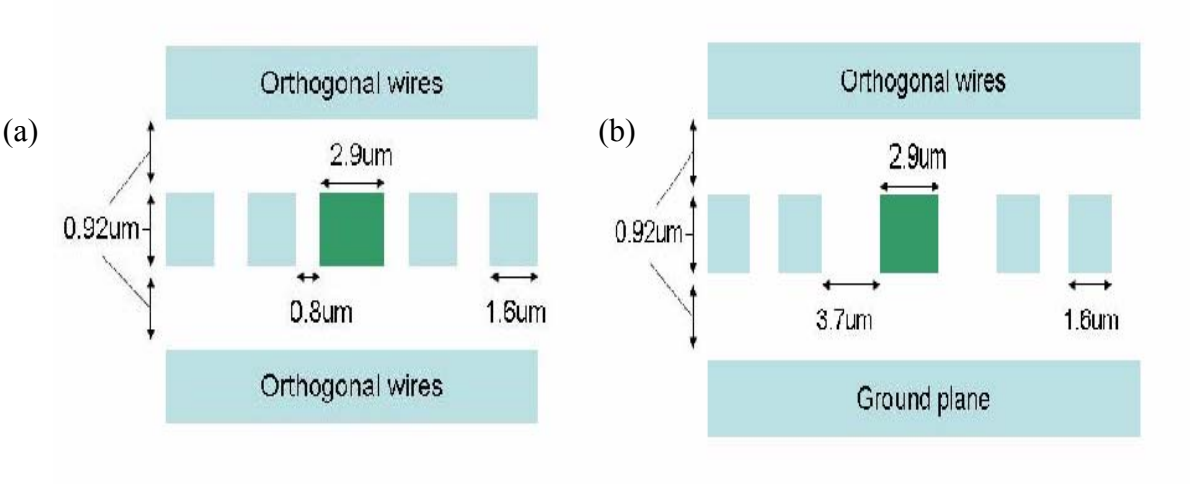


Figure 4.10: (a) Clock wire with grid based power distribution. Shields flank clock wire. (b) Clock wire with MIM plane decaps.

A section of a 2GHz clock tree with 2.5mm of the above wires is considered which has an inverter driving a fan-out of two. Drivers are modeled in SPICE using 180nm device models. RAPHAEL, a CAD tool for parasitic extraction [4.19], is used for finding the interconnect RLC parameters. Table 4.1 gives a summary of the resistance, capacitance and inductance per unit length of the configurations in Fig. 4.10(a) and Fig. 4.10(b). SPICE simulations show that the latency of that particular section of the clock tree is about 5% better for the clock wire with MIM plane decaps.

Table 4.1: Electrical characteristics of clock wire.

	Resistance per mm	Capacitance per mm	Inductance per mm
Fig. 4.10(a)	12.1Ω	0.37pF	0.35nH
Fig. 4.11(b)	11Ω	0.33pF	0.58nH

4.2.4. Benefits for Signal Interconnects

Two global bus configurations (Fig. 4.11) are compared in SPICE with Partial Electrical Equivalent Circuit (PEEC) models [4.1] for the RLC wires. Fig. 4.11(b) uses power planes, so coplanar shields are not needed, unlike the power grid case in Fig. 4.11(a). This enables a designer to have increased spacing between signal wires for the same cross-sectional area of the bus. Thus, wire capacitance for Fig. 4.11(b) is reduced compared to Fig. 4.11(a). Bus length is 2.8mm and each wire is assumed to have a 80fF load capacitance. Signal wires in Fig. 4.11(a) have 100Ω resistive drivers. SPICE simulations predict worst case crosstalk noise for Fig. 4.11(a) to be $0.38*V_{dd}$. To have the

same peak crosstalk noise, the driver resistance for the wires in Fig. 4.11(b) is found to be 170Ω. SPICE simulations show that the delay of the global busses in Fig. 4.11(a) and Fig. 4.11(b) are 112ps and 87ps respectively. These simulations also indicate energy per bit for a 180 nm technology is 22% lower for a wire in Fig. 4.11(b).

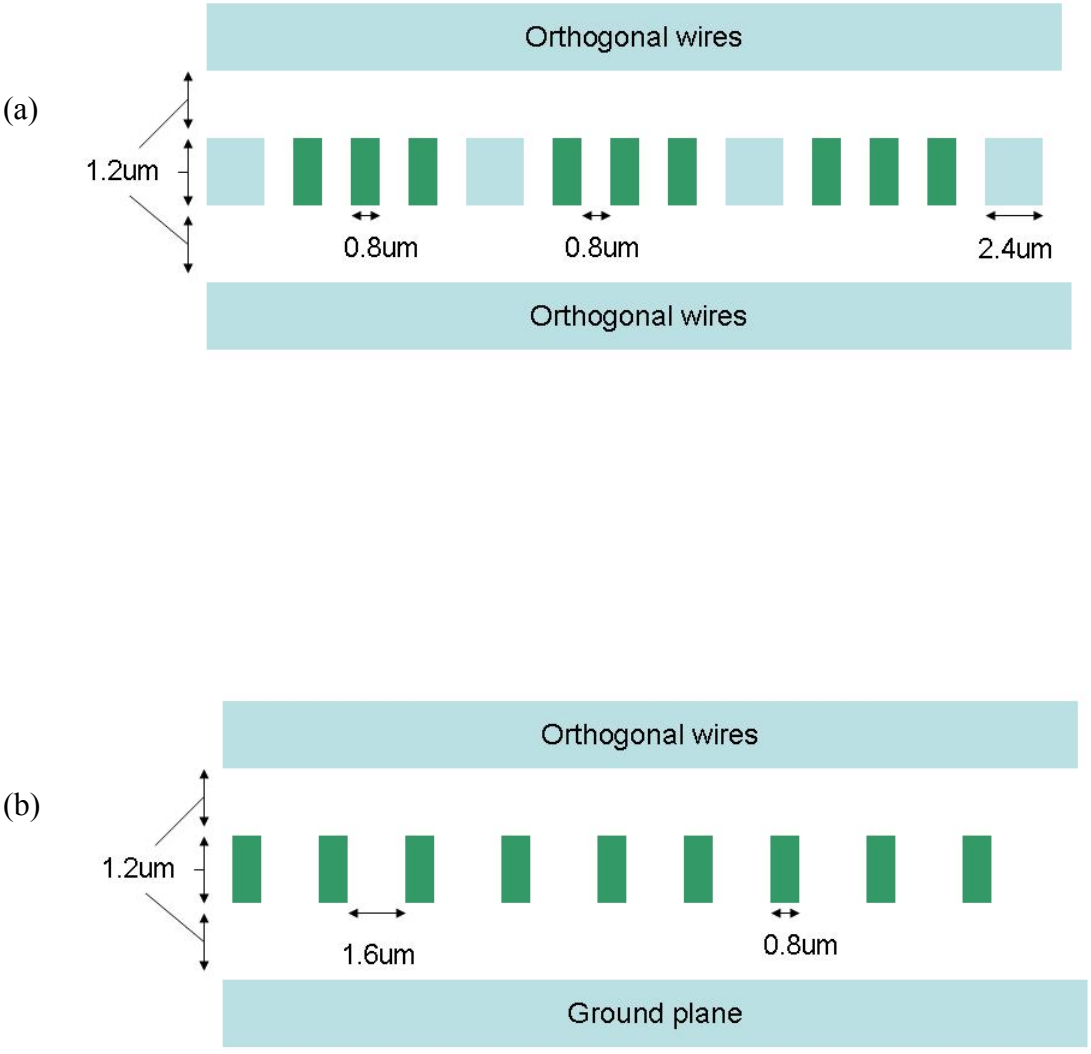


Figure 4.11: (a) Conventional grid based configuration with coplanar shields in blue. (b) Signal wires with MIM plane decaps.

4.2.5. Conclusions

This work suggests using power and ground planes separated by high k dielectrics in interconnect levels of high-performance microprocessors. Such structures could reduce IR drop by a factor of 4 and decrease simultaneous switching noise caused by package inductance by 8%-60% in power interconnect networks of high-performance microprocessors. This MIM plane decap structure also provides important benefits for signal and clock interconnects. Prototypes of this structure have been fabricated. Testing reveals it is possible to fabricate such MIM plane decaps with good yield. Symmorphix Inc., a startup company based in Sunnyvale, was responsible for the experimental work on this project while the author was responsible for the theoretical analysis. Interestingly, when this work was in progress, Freescale Semiconductor conducted research on using high-k capacitors in interconnect levels with power grids [4.20]. Such structures are now part of Freescale Semiconductor's high-performance microprocessor products.

4.3. Power Delivery for 3D Integrated Circuits

As mentioned previously, power delivery is a serious concern for 3D integrated circuits. If a 3D integrated circuit consists of four 100A 1V chips (for example), it would consume a total current of 400A at 1V. Delivering power to such a stack conventionally would cause many challenges with simultaneous switching noise, electromigration and IR drop. One solution to this problem involves having a MIM plane decap structure for each chip in the 3D stack as discussed in Section 4.2. The 3D integrated circuit could also have its power and ground networks interchanged periodically to control electromigration as described in Section 4.1.

A number of approaches to ameliorate power delivery issues of 2D integrated circuits

have been recently proposed in the literature. These include clock-data compensation [4.21], use of active filtering circuits [4.22], placement of the DC-DC converter closer to the IC [4.23][4.24] and embedded decoupling capacitance in the package/board [4.25]. These techniques are applicable to 3D integrated circuits as well.

4.4. Summary

This chapter describes two techniques to ameliorate power interconnect concerns in future high-performance 2D and 3D integrated circuits. The first technique involves periodic reversal of current direction in power delivery systems to enhance electromigration lifetimes of solder bumps and on-chip global power interconnect networks by upto three orders of magnitude. The second technique involves fabrication of power and ground planes separated by a high k dielectric in global interconnect levels. Resistive drop in the global power interconnect network is reduced by a factor of 4 due to the low resistance of power planes. Simultaneous switching noise due to package inductance is reduced by 8% to 60% depending on the decoupling capacitance integrated in this structure.

CHAPTER 5

CO-DESIGN OF SIGNAL, POWER, CLOCK AND THERMAL INTERCONNECT NETWORKS

The interconnect stack and die size of present-day integrated circuits are typically optimized using a CAD tool such as MINDS as described in Chapter 3. While this approach is reasonably accurate for older technologies, sub-90nm chips are significantly interconnect limited and bring up several issues. These include:

- Power distribution networks took up more than 25% of all wiring tracks in a 180nm microprocessor [5.1], and are expected to consume a bigger percentage of total wiring tracks with scaling [5.2]. Power distribution networks thus need to be modeled rigorously and have to be co-optimized along with signal/clock wiring and via blockage.
- Currently available stochastic wire length distributions show significant error when compared to actual data. For example, the commonly used Davis distribution [5.3] shows as much as 38% error with respect to measurement data for circuit blocks analyzed later in this chapter. More accurate wire length estimates are needed.
- Via blockage can take up as much as 10-30% of the total wiring area for some metal levels [5.4]. Assignment of wires in multiple interconnect levels should be done with via blockage considerations in mind.
- Global interconnect pitch needs to be selected based on signal, power and clock wiring considerations.

- Repeater leakage power is substantial as discussed in Chapter 3, and needs to be considered when repeater insertion is performed.
- Wire resistivity increases due to size effects [5.5] need to be modeled.

This chapter presents IntSim, a GUI based CAD tool that helps answer the above concerns and thereby enables better optimization of sub-90nm interconnect networks. After presenting a new stochastic wire length distribution model, this chapter describes logic gate sizing in IntSim. Following this, global, local and intermediate/semi-global interconnect optimization in IntSim are described. The algorithm used to combine together all these models is then presented. Results from IntSim are compared with data from a commercial microprocessor and several case studies are presented to show how IntSim can be used. The work done in this chapter was published by the author in [5.6].

5.1. Models

This section describes various models utilized in the CAD tool developed by the author.

5.1.1. New Stochastic Signal Wire Length Distribution Model

Several publications have discussed stochastic wiring distributions [5.7]. The Davis distribution [5.3], which is considered one of the most accurate [5.8], assumes gates are uniformly distributed all over the chip and then finds a distribution of wire lengths using Rent's rule. This assumption leads to a sea of uniformly distributed gates with uniform white space between them. In general, however, this assumption of uniformly distributed gates is not valid. A look at the layout of an integrated circuit shows, in most cases, that gates are placed close to each other with little blank space between them. The derivation of

a new wire length distribution that considers random arrangement of gates in a circuit block is discussed in this section. Comparison with actual data later in this document shows that error is reduced substantially compared to the Davis distribution.

For the purpose of this derivation, the author defines a new quantity called a gate socket. Any chip is considered to have many gate sockets, some of which are occupied by gates, as shown in Fig. 5.1. The number of gate sockets $N_{sockets}$ is related to the number of gates N_{gates} by the relation:

$$N_{gates} = N_{sockets} \cdot p_{gates} \qquad \ldots(5.1)$$

where p_{gates} is the percentage of die area that is occupied by logic gates. For example, a chip with 10 million gates and 50% of the die area occupied by logic gates [5.9] would have 20 million gate sockets, with gates randomly distributed in 10 million of them. If $N_{sockets}$ calculated with Eq. (5.1) is not an integer, it is rounded off to the nearest integer as an approximation.

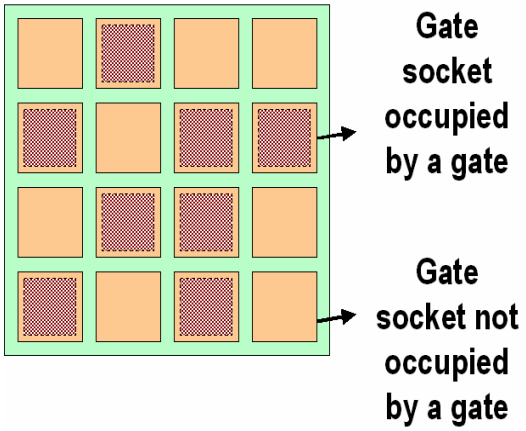


Figure 5.1: An illustration of the gate socket concept.

The expected number of interconnects of a certain length l is given as the product of $M(l)$, the number of gate socket pairs separated by a distance l, and $I_{exp}(l)$, the average number of interconnects between a gate socket pair separated by l [5.3].

$$i(l) = M(l).I_{\exp}(l) \qquad \ldots(5.2)$$

The number of gate socket pairs separated by a distance l is similar to Davis' derivation [5.3] of the number of gate pairs separated by a distance l. Therefore,

$$M(l) = \begin{cases} \frac{l^3}{3} - 2l^2\sqrt{N_{sockets}} + 2lN_{sockets} & 1 \le l < \sqrt{N_{sockets}} \\ \frac{1}{3}\left(2\sqrt{N_{sockets}} - l\right)^3 & \sqrt{N_{sockets}} \le l < 2\sqrt{N_{sockets}} \end{cases} \qquad \ldots(5.3)$$

It should be noted that the value of l is in gate socket lengths. A gate socket length is defined as the distance between two adjacent gate sockets and is equal to (Die area/$N_{sockets}$)$^{0.5}$. Davis [5.3] defines gate pitch as (Die area/N_{gates})$^{0.5}$. A gate socket length is thus equal to (N_{gates} /$N_{sockets}$)$^{0.5}$ = $p_{gates}{}^{0.5}$ gate pitches.

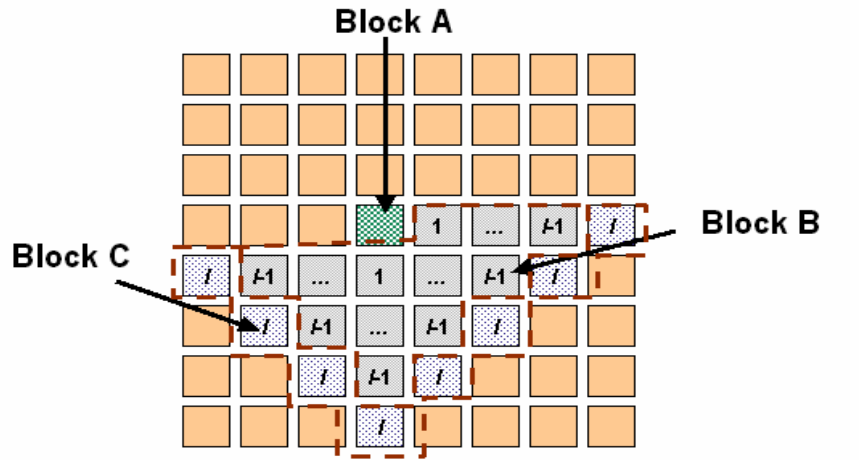


Figure 5.2: Block definitions to find average number of wires between a gate socket pair.

The average number of interconnects between a gate socket pair separated by l is given

by:

$$I_{\exp}(l) = P(Gate\ in\ block\ A).\frac{I_{A-to-C}}{N_C} \quad \ldots(5.4)$$

where *P(Gate in block A)* is the probability that block A of Fig. 5.2 is occupied by a gate, $I_{A\text{-}to\text{-}C}$ is the average number of interconnects connecting block A to block C and N_C is the number of gates in block C.

$$P(Gate\ in\ block\ A) = \frac{N_{gates}}{N_{sockets}} = p_{gates} \quad \ldots(5.5)$$

From the Davis derivation [5.3],

$$I_{A-to-C} = \alpha k\left[(N_A+N_B)^p - N_B^p + (N_B+N_C)^p - (N_A+N_B+N_C)^p\right] \quad \ldots(5.6)$$

f.o. is the average fan-out of the system, $\alpha = f.o./(f.o.+1)$, k and p are Rent's constants and N_A, N_B are the number of gates in blocks A and B respectively. If gates are randomly distributed in gate sockets, the following approximations hold from Fig. 5.2.

$$\begin{aligned} N_A &= 1 \\ N_B &= p_{gates}.l.(l-1) \\ N_C &= 2p_{gates}.l \end{aligned} \quad \ldots(5.7)$$

Combining Equations (5.2), (5.3), (5.4), (5.5), (5.6), (5.7) and normalizing, we get the average number of interconnects of length l gate socket lengths to be:

$$i(l) = \begin{cases} \dfrac{\alpha k}{2}\Gamma\left(\dfrac{l^3}{3} - 2l^2\sqrt{N_{sockets}} + 2lN_{sockets}\right) l^{2p-4} & 1 \le l < \sqrt{N_{socket} \\ \dfrac{\alpha k}{6}\Gamma\left(2\sqrt{N_{sockets}} - l\right)^3\ l^{2p-4} & \sqrt{N_{sockets}} \le l < 2\sqrt{N_{soc} \end{cases} \quad \ldots(5.8)$$

where

$$\Gamma = \frac{2N_{gates}(1-N_{gates}^{p-1})}{\left(-N_{sockets}^{p}\frac{1+2p-2^{2p-1}}{p(p-1)(2p-1)(2p-3)}-\frac{1}{6p}+\frac{2\sqrt{N_{sockets}}}{2p-1}-\frac{N_{sockets}}{p-1}\right)}$$

The average wire length for this interconnect distribution is

$$L_{avg}(\text{in gate socket lengths}) = \frac{\int_{1}^{2\sqrt{N_{sockets}}} li(l)dl}{\int_{1}^{2\sqrt{N_{sockets}}} i(l)dl}$$

$$= \frac{\left[\frac{p-0.5}{p}-\sqrt{N_{sockets}}-\frac{p-0.5}{6\sqrt{N_{sockets}}(p+0.5)}+N_{sockets}^{p}\left(\frac{-p-1+4^{p-0.5}}{2(p+0.5)p(p-1)}\right)\right]}{\left(-N_{sockets}^{p}\frac{1+2p-2^{2p-1}}{p(p-1)(2p-1)(2p-3)}-\frac{1}{6p}+\frac{2\sqrt{N_{sockets}}}{2p-1}-\frac{N_{sockets}}{p-1}\right)}$$

For a large number of gates and p>0.5, this expression can be simplified to

$$L_{avg}(\text{in gate pitches}) = p_{gates}^{1-p}N_{gates}^{p-0.5}\left(\frac{p+1-4^{p-0.5}}{2(p-0.5)(p+0.5)p}\right) \quad \ldots(5.9)$$

When gates are uniformly distributed over the die area, Davis derived the expression for average wire length to be:

$$L_{avg}(\text{in gate pitches}) = N_{gates}^{p-0.5}\left(\frac{p+1-4^{p-0.5}}{2(p-0.5)(p+0.5)p}\right) \quad \ldots(5.10)$$

Average wire length with the new wiring distribution is therefore the Davis average wire length multiplied by a factor that depends on the Rent's constant p and the fraction of total die area occupied by logic gates. Most typical circuit blocks have 50-75% of the total die area occupied by logic gates [5.9]. Fig. 5.3 shows a comparison of measured average lengths and average lengths predicted by the Donath distribution [5.3], the Davis distribution and the new distribution for 22 ISCAS'89 circuit blocks. Rent's constants and

number of gates for these benchmark circuits are obtained from [5.10]. While the Donath distribution and the Davis distribution have an average error of 75% and 38% with respect to actual data respectively, the new model has an error between 8% and 24% corresponding to values of p_{gates} ranging from 0.5 to 0.75.

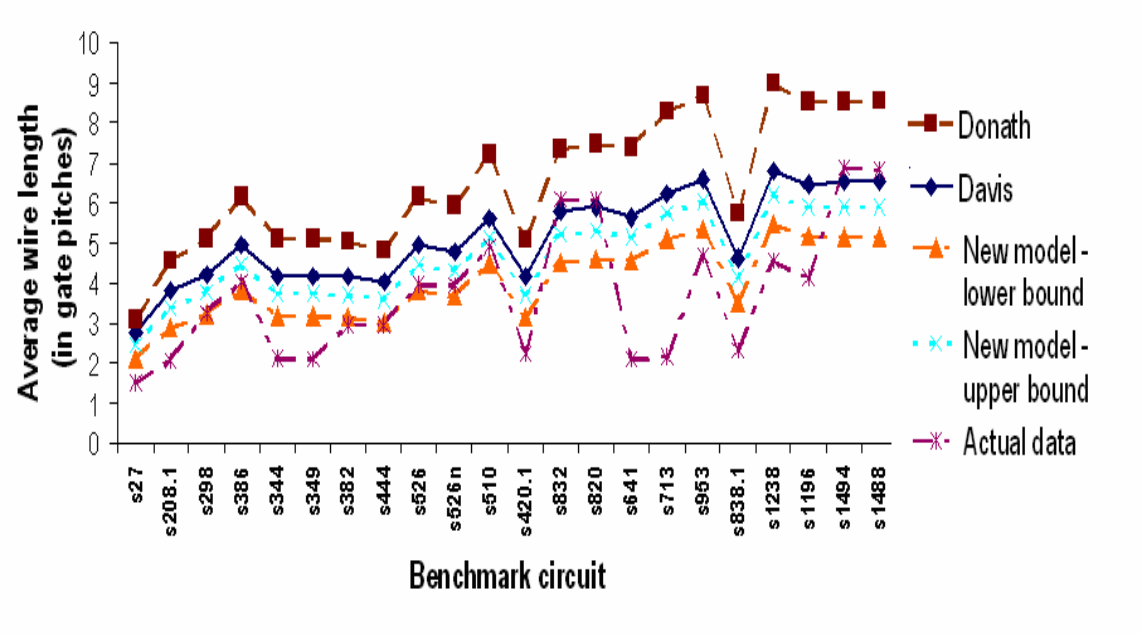


Figure 5.3: Validation of average wire lengths with new model with actual data from 22 ISCAS'89 circuit blocks. Average error of: Donath distribution = 75%, Davis distribution = 38%, New distribution = 8%-24%.

Table 5.1 shows a comparison of average wire length obtained from measurements with values predicted by the Davis distribution and the new distribution, for benchmark circuits provided by Davis in [5.11]. It can be seen that while the Davis distribution has an average error of 26% for these circuits, the new distribution has average errors of only 2%-12 %.

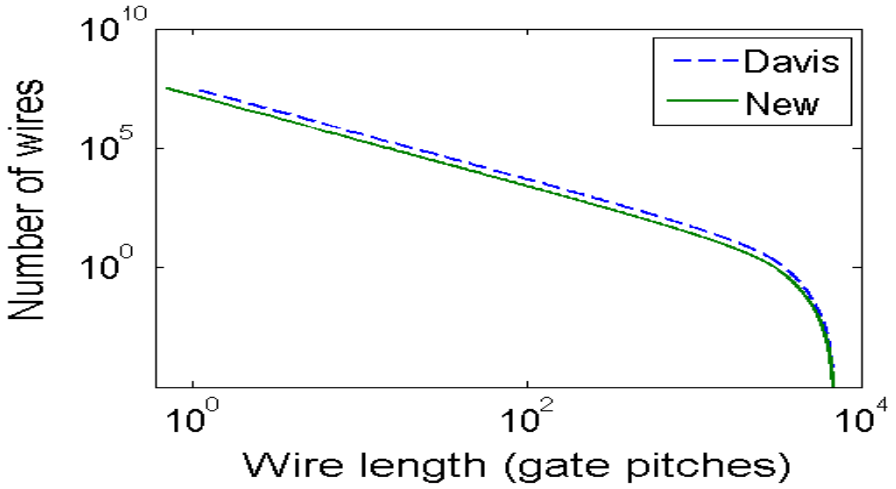
Table 5.1: Validation of model with actual data for average wire length.

Number of gates	Rent's constant p	Actual data	Davis average length	New model with p_{gates}=0.5	New model with p_{gates}=0.75
2146	0.75	3.53	5.26	4.37	4.87
576	0.75	2.98	3.9	3.22	3.6
528	0.59	2.20	3.12	2.44	2.79
671	0.57	2.63	3.12	2.45	2.82
1239	0.47	2.14	2.96	2.26	2.64
73	0.667	2.00	2.35	1.89	2.14
78	0.667	2.27	2.38	1.91	2.17
72	0.667	1.88	2.34	1.88	2.13
252	0.667	2.73	2.96	2.39	2.71
236	0.667	2.198	2.93	2.36	2.67
237	0.667	2.887	2.93	2.36	2.67
55	0.667	1.579	2.23	1.79	2.03
59	0.667	1.38	2.25	1.81	2.06
62	0.667	2.08	2.28	1.83	2.08
Average error			26%	2%	12%

Fig. 5.4 shows how the new wiring distribution differs from the Davis distribution for a 36 sq. mm circuit block with 12 million gates, p_{gates} = 0.5, average fan-out = 3, and Rent's constants k=4 and p=0.55. Equations (5.9) and (5.10) suggest average length for the new distribution would be 27% less than the average length for the Davis distribution. While the log scale plot in Fig. 5.4(a) indicates only a small difference for short lengths, the linear

scale plot in Fig. 5.4(b) shows a noticeable difference and captures the trend of the wiring distribution moving towards shorter lengths.

(a)



(b)

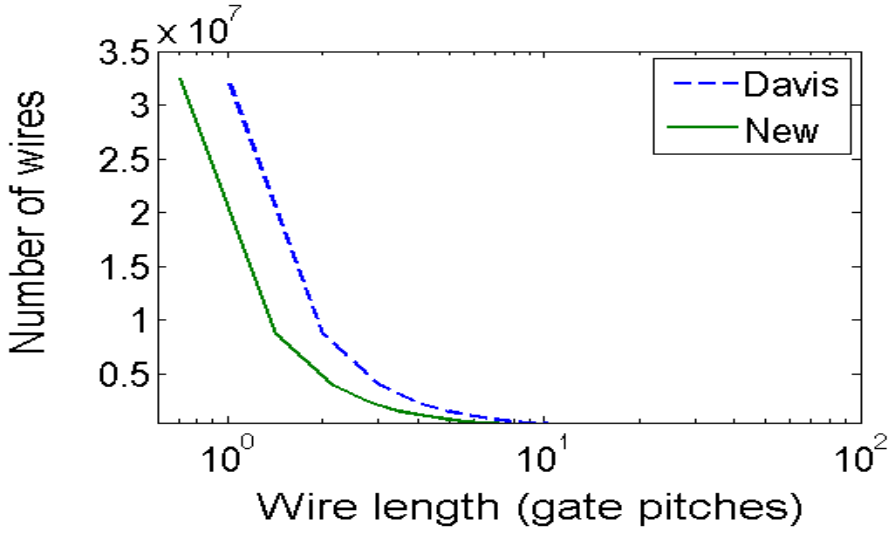


Figure 5.4: (a) Comparison of new distribution with Davis distribution in the log scale. (b) Comparison of new distribution with Davis distribution in the linear scale for short lengths.

5.1.2. Logic Gate Model

Logic gates are modeled as two input NAND gates and are sized based on average wire length estimates provided by the new wiring distribution. If W is the device width, the delay of a logic path having two input NAND gates driving a fan-out *f.o.* is given by [5.9]:

$$t_d = L_d 0.7 \frac{R_{NAND}}{W}\left(f.o.C_{NAND}W + f.o.\chi C_{\text{int}} \right) \qquad \ldots(5.11)$$

where L_d is the logic depth, $\chi = 4/(f.o.+3)$ is a factor that converts point-to-point net length to wiring net length, R_{NAND} is the average drive resistance of a minimum size 2 input NAND gate, C_{NAND} is the input capacitance of the NAND gate and C_{int} is the capacitance of an average wire. C_{NAND} is computed assuming nMOS and pMOS devices are sized equally in a 2 input NAND gate, while R_{NAND} is obtained from equations given in [5.9]. If c is the capacitance per unit length of a wire, A is the die area and F is the feature size, the area of a NAND gate of width W is given by $20.4(7.3+W)F^2$ [5.3]. Eq. (5.9) indicates

$$\begin{aligned} C_{\text{int}} = cL_{avg} &= cp_{gates}^{1-p} N_{gates}^{p-0.5} \left(\frac{p+1-4^{p-0.5}}{2(p-0.5)(p+0.5)p} \right) \sqrt{\frac{A}{N_{gates}}} \\ &= c\left(\frac{20.4(7.3+W)F^2}{A} \right)^{1-p} \left(\frac{p+1-4^{p-0.5}}{2(p-0.5)(p+0.5)p} \right) \sqrt{A} \end{aligned} \qquad \ldots(5.12)$$

It is interesting to note that unlike with previous wiring distributions, the length of an average length wire with the new distribution is a function of logic gate size. Essentially, it means if the die area is fixed and we use smaller size gates, they can be placed closer to each other, and so average wire lengths would reduce. If we define a constant

$$k_1 = c\left(\frac{20.4F^2}{A} \right)^{1-p} \left(\frac{p+1-4^{p-0.5}}{2(p-0.5)(p+0.5)p} \right) \sqrt{A}$$

Eq. (5.11) becomes:

$$t_d = L_d 0.7 \frac{R_{NAND}}{W}\left(f.o.C_{NAND}W + f.o.\chi k_1 (7.3+W)^{1-p} \right) \quad \ldots(5.13)$$

The delay expression in Eq. (5.13) is equated to (1-margin)/*f* for finding gate size where *f* is the frequency and margin is the fraction of a clock cycle that constitutes skew and variability.

5.1.3. Global Interconnect Model

The choice of global interconnect pitch significantly impacts performance of signal, power and clock interconnect networks [5.1]. In this section, a compact physical model for global wire pitch is derived by considering all these three types of interconnect networks. The existing literature for global wire pitch models consists of [5.12], which considered only signal interconnects while deciding global interconnect pitch, and [5.13], which gave a design plane for choice of global interconnect pitch without providing a single optimal value that could be used in a technology.

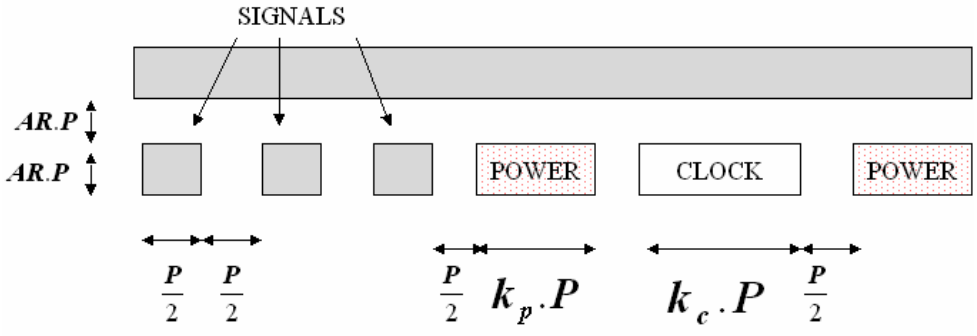


Figure 5.5: Cross-section of global wiring layers for an integrated circuit.

Fig. 5.5 shows two thick global metal layers of a certain integrated circuit. An

expression for IR drop of a uniform power grid with flip chip packaging is given by [5.2]

$$V_{IR} = \frac{\rho I_T}{2\pi} \frac{d_{pad\_to\_pad}}{N.AR.k_p.P^2} \ln\left(\frac{0.65\, d_{pad\_to\_pad}}{l_{pad}}\right) \quad \ldots(5.14)$$

where ρ is the wire resistivity, $d_{pad\_to\_pad}$ is the distance between two adjacent power pads, l_{pad} is the length of a pad, I_T is the current distributed per pad and N is the number of power grid segments between two pads. The total area occupied by the power distribution in two orthogonal global wire levels can be estimated using Fig. 5.6.

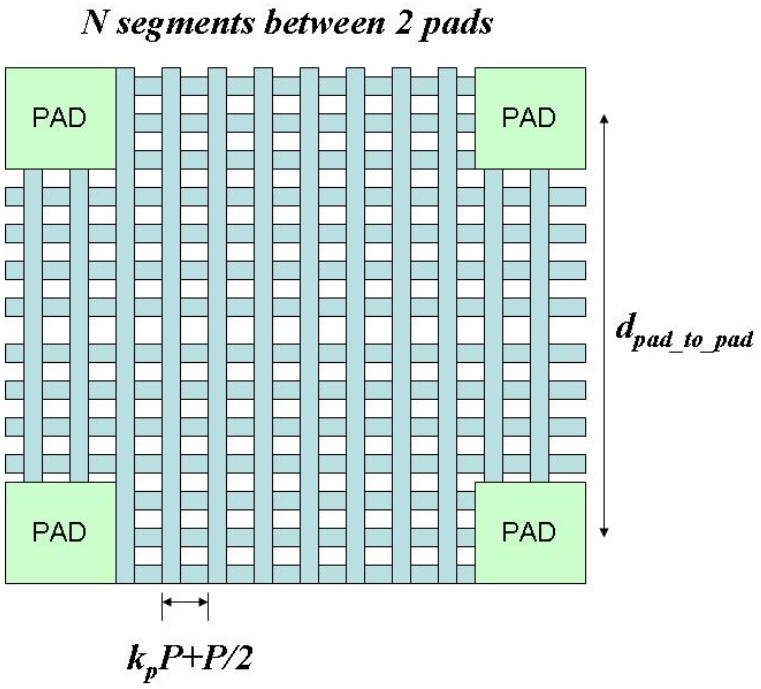


Figure 5.6: Top view of a global power grid between four pads.

Essentially, the area occupied by a single power wire is $(k_pP+P/2).d_{pad\_to\_pad}$ and there are N segments between two pads. Therefore, the area occupied by power wires on two orthogonal metal levels is $2.N.(k_pP+P/2).d_{pad\_to\_pad}$. Since the number of power pads is

N_{power_pads}, the total area occupied by power wiring is

$$A_{power} = N_{power\_pads}.2N.(k_p.P + \frac{P}{2}).d_{pad\_to\_pad} \quad \ldots(5.15)$$

where N_{power_pads} is the number of power pads. Since the global wire area of clock wires is negligible [5.14], the area occupied by global signal, power and clock wires is:

$$A_{total} = 2A_{power} + l_{signal}.P \quad \ldots(5.16)$$

Note that l_{signal} is the total length of global signal interconnects and $2A_{power}$ is considered since power and ground networks have equal areas. Using Equations (5.14), (5.15) and (5.16),

$$A_{total} = \left[2.\left(k_p + 0.5\right).N_{power\_pads}.\rho.\frac{I_T.d_{pad\_to\_pad}^{\ 2}}{\pi AR.k_p.V_{IR}}.\ln\left(\frac{0.65.d_{pad\_to\_pad}}{l_{pad}}\right)\right]\frac{1}{P} + l_{signal}.P \quad \ldots(5.17)$$

Also, $A_{total}=e_w.A_{die}$ where e_w is a wiring efficiency factor and A_{die} is the die area. Using the above two equations,

$$l_{signal} = \frac{e_w.A_{die}}{P} - \left[2.\left(k_p + 0.5\right).N_{power\_pads}.\rho.\frac{I_T.d_{pad\_to\_pad}^{\ 2}}{\pi.AR.k_p.V_{IR}}.\ln\left(\frac{0.65.d_{pad\_to\_pad}}{l_{pad}}\right)\right]\frac{1}{P^2}$$

Since a designer typically wants to route as many signal wires in the global wire levels as possible, $dl_{signal}/dP=0$. This gives

$$P = 4.\left(k_p + 0.5\right).N_{power\_pads}.\rho.\frac{I_T.d_{pad\_to\_pad}^{\ 2}}{\pi.e_w.A_{die}.AR.k_p.V_{IR}}.\ln\left(\frac{0.65.d_{pad\_to\_pad}}{l_{pad}}\right) \quad \ldots(5.18)$$

The global wire pitch is also a function of clock wiring. Based on [5.15], the maximum distance a buffer can drive four similar buffers (with acceptable slew) through a tapered H Tree is a good metric for how well a clock tree operates. Fig. 5.7, Fig. 5.8 and Fig. 5.9 reveal that the H tree in Fig. 5.7 is equivalent to the wire in Fig. 5.9.

The slew for the wire [5.16] in Fig. 5.9 is

$$\begin{aligned} Slew &= \frac{t_{90\%} - t_{10\%}}{0.8} \\ &= 1.1\left(\frac{r}{2}\right)(2c)D^2 + 2.75\left(4R_oC_o + \frac{R_o}{W}.2c.D + 4C_oW\frac{r}{2}D\right) \end{aligned} \quad \ldots(5.19)$$

To get the buffer size that gives the best-case slew, we set *d(Slew)/dW=0* and substitute the obtained *W* in Eq. (5.19) to get

$$Slew_{best} = 1.1rcD^2 + 1.1(R_oC_o + D\sqrt{R_oC_orc}) \quad \ldots(5.20)$$

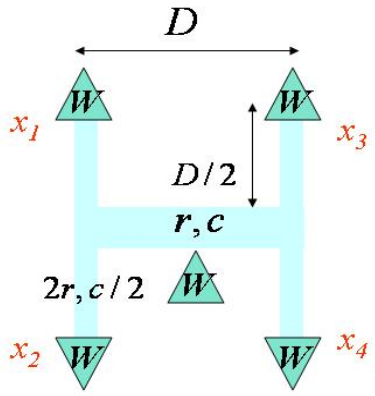


Figure 5.7: A tapered H tree that is typically used for clock distribution purposes. The wire resistance per unit length is denoted as *r* and the wire capacitance per unit length is denoted as *c*. Due to symmetry, x_1, x_2, x_3 and x_4 are equipotential points.

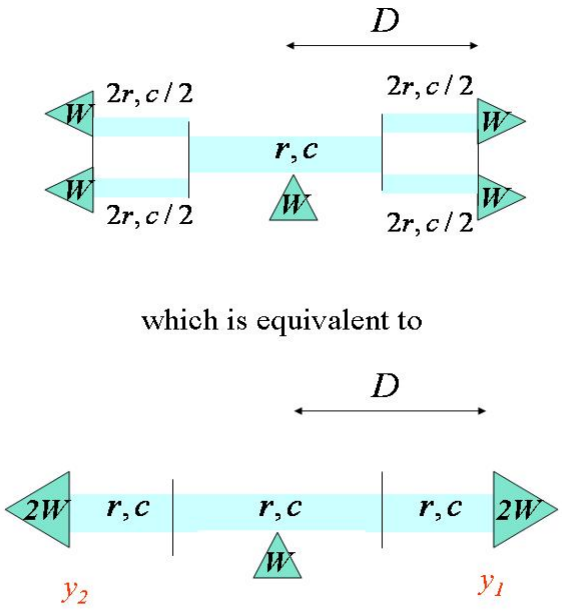


Figure 5.8: The equipotential points from Fig. 5.7 are merged in this figure. Distributed RC wire models show the equivalence between the top and bottom configurations in this figure. Due to symmetry, y_1 and y_2 are equipotential points.

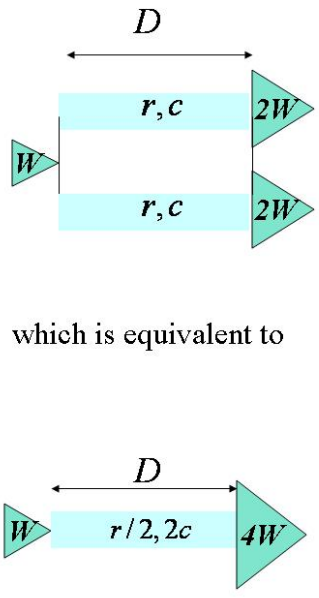


Figure 5.9: Equipotential points from Fig. 5.8 are merged in this figure.

The maximum drive distance is obtained when the best-case slew in Eq. (5.20) just meets a particular slew requirement fixed by a designer i.e. $Slew_{best}=\beta/f$ where f is the clock frequency and β is normally 0.15-0.25. Using this equation, the fact that $r=\rho/k_cP^2$ and Eq. (5.20), we get

$$P=\frac{D}{2}\sqrt{\frac{c\rho}{k_cR_oC_o}}.\frac{1}{\frac{\beta}{fR_oC_o}-11}\left[\sqrt{72.6+\frac{44\beta}{fR_oC_o}}+11\right] \quad \ldots(5.21)$$

In Eq. (5.21), c is a function of ratios of wire dimensions [5.17] and therefore does not change with wire pitch as long as all wire dimensions are scaled. From Eq. (5.18) and Eq. (5.21),

$$P=Max.\left[\begin{array}{l} 4.\left(k_p+0.5\right).N_{power\_pads}.\rho.\frac{I_T.d_{pad\_to\_pad}{}^2}{\pi.e_w.A_{die}.AR.k_p.V_{IR}}.\ln\left(\frac{0.65.d_{pad\_to\_pad}}{l_{pad}}\right), \\ \frac{D}{2}\sqrt{\frac{c\rho}{k_cR_oC_o}}.\frac{1}{\frac{\beta}{fR_oC_o}-11}\left(\sqrt{72.6+\frac{44\beta}{fR_oC_o}}+11\right) \end{array}\right] \quad \ldots(5.22)$$

To verify this equation, the parameters in Eq. (5.22) are chosen based on published data from a commercial microprocessor [5.1] and values from the ITRS as:

k_p=2, N_{power_pads}=2100, ρ=2.2x10^{-8}ohm-m, I_T=0.13, e_w=0.4, $d_{pad\_to\_pad}$ =400um, A_{die}=400 sq. mm, AR=0.6, V_{IR}=30mV, l_{pad}=100um, D=2mm, c=4x10^{-10}F/m, k_c=1.9, R_oC_o=1.85ps, β=0.25, and f=1.3GHz

This gives P=max(0.5um,1.35um)=1.35um. This result matches well with data from that particular microprocessor, which had a pitch of 1.26um [5.1].

5.1.4. Local Interconnect Model

IntSim has two wire levels for routing local signal, power and clock wiring. Local

interconnect pitch, P_{local}, is selected as $2F$, where F is the feature size [5.17]. The length of the longest wire routed in local interconnect levels, l_{max}, is obtained from [5.17] as

$$2e_w A = \chi P_{local} \sqrt{\frac{A}{N_{sockets}}} \int_1^{l_{max}} li(l)dl \qquad \ldots(5.23)$$

Essentially, the left hand side of Eq. (5.23) represents the area *available* for routing wires in the two local interconnect levels, and the right hand side of Eq. (5.23) denotes the area *required* for routing all wires having lengths between 1 and l_{max} gate socket lengths. e_w is a wiring efficiency factor given by:

$$e_w = 1 - e_{router} - e_{power/gnd} - e_{signal\_vias} \qquad \ldots(5.24)$$

where e_{router} is the efficiency of the wire routing tool (typically around 0.5), $e_{power/gnd}$ is the fraction of area used by power and ground wires and e_{signal_vias} is the fraction of area used by signal vias. $e_{power/gnd}$ is obtained from the model for local power distribution networks derived in [5.18]. Via blockage in local interconnect levels comes from vias to wires routed in higher metal levels and vias for repeaters. Based on the model for via blockage given in [5.4],

$$e_{signal\_vias} = \sqrt{\frac{(2N_{wires\_higher} + 2N_{repeaters}).(P_{local} + s\lambda)^2}{A}} \qquad \ldots(5.25)$$

where N_{wires_higher} is the number of wires routed in higher metal levels, $N_{repeaters}$ is the number of repeaters for higher metal levels, λ is the design rule unit and s is a via covering factor which is typically 3 [5.4]. N_{wires_higher} is found from the stochastic wiring distribution by finding the number of wires whose length is greater than l_{max}. IntSim also runs electromigration checks on local power wiring based on maximum current density limits

set by the user. The local interconnect model used in IntSim is more accurate than local interconnect models used in prior multilevel interconnect simulators such as MINDS. This is because IntSim rigorously models wiring efficiency by calculating the area consumed by signal via blockage and power wires, while MINDS assumes wiring efficiency is 0.4 for all designs. Also, IntSim utilizes the improved stochastic wire length distribution described in Section 5.1 while MINDS makes use of the Davis distribution.

5.1.5. Intermediate and Semi-Global Interconnect Model

Intermediate and semi-global wires in IntSim are modeled based on Eq. (5.26) and Eq. (5.27). The right hand side of Eq. (5.26) denotes the area required for routing wires of length lying between l_{min} and l_{max} in a pair of wire levels, and the left hand side denotes the area available for routing. Here, P is the pitch of the pair of wiring levels. Eq. (5.27) represents the condition that the delay of the longest wire in a pair of metal levels should be a certain fraction of the clock period, as discussed in [5.17]. Eq. (5.27a) represents this criterion when no repeaters are inserted while Eq. (5.27b) represents the case when repeaters are inserted with the Energy-Delay Product minimization strategy discussed in Chapter 3. Width of wires is equal to spacing between wires.

$$2e_w A = \chi P \sqrt{\frac{A}{N_{sockets}}} \int_{l_{\min}}^{l_{\max}} li(l)dl \qquad \ldots(5.26)$$

$$\tau_{rc} = 4.4 \frac{\rho(P,ar)}{ar.P^2} c l_{\max}^{\ 2} \sqrt{\frac{A}{N_{sockets}}} = \frac{\beta}{f} \qquad \ldots(5.27a)$$

$$\tau_{rc} = \sqrt{\frac{A}{N_{sockets}}} \frac{2l_{\max}\sqrt{\rho(P,ar)cR_oC_o}}{ar.P} \left(\frac{0.7}{\delta} + 0.7\gamma + \frac{0.4}{\gamma} + 0.7\delta \right) = \frac{\beta}{f} \qquad \ldots(5.27b)$$

$$\gamma = (0.73 + 0.07 \ln \phi_{gate})^2, \delta = (0.88 + 0.07 \ln \phi_{gate})^2$$

$$\phi_{gate} = \frac{\frac{1}{2} a C_o V_{dd}{}^2 f}{\frac{1}{2} a C_o V_{dd}{}^2 f + b V_{dd} I_{leak}}$$

$$e_w = 1 - e_{router} - e_{power/gnd} - e_{signal\_vias}$$

In these equations, ρ is the wire resistivity, c is the wire capacitance per unit length, b is the percentage of time the circuit is not sleep gated, f is the clock frequency, V_{dd} is the supply voltage, a is the activity and ar is the wire aspect ratio. R_o, C_o and I_{leak} are the resistance, capacitance and leakage of a minimum size repeater respectively. The value of β is 0.25 for short wires and 0.9 for long wires. The wiring efficiency factor for intermediate and semi-global levels (e_w) has two sources. The first source is via blockage due to vias to higher levels of metal and due to repeaters (e_{signal_vias}). These are modeled based on [5.4]. The second source is power via blockage (e_{power_gnd}) that is modeled based on [5.18]. Wire resistivity increases due to size effects are modeled as shown in [5.5].

The intermediate and semi-global wire model for IntSim is superior to models for the same in prior multilevel interconnect simulators such as MINDS due to the following reasons: (i) IntSim utilizes an energy-delay product based repeater insertion model while MINDS makes use of the sub-optimal repeater insertion model [5.17]. As explained in Chapter 3, the energy-delay product based repeater insertion model is more relevant to sub-90nm technologies. (ii) IntSim rigorously models wiring efficiency by considering the area consumed by signal via blockage and power via blockage, while MINDS assumes wiring efficiency is 0.4 for all designs. (iii) IntSim utilizes the improved stochastic wire length distribution described in Section 5.1 while MINDS makes use of the Davis distribution.

5.2. Implementation of CAD Tool

This section describes the algorithm and graphical user interface design for IntSim.

5.2.1. Algorithm

In IntSim, the process of selecting wire pitches for different interconnect levels proceeds in several steps:

1. Input all parameters: The user inputs various details of the system that is being modeled.

2. Logic gate sizing: Logic gates are sized based on Eq. (5.13) such that clock frequency targets are reached.

3. Generation of stochastic wiring distribution: Based on the logic gate size chosen in Step 2, the fraction of die area occupied by logic gates, p_{gates}, is found. This is used to generate the stochastic wiring distribution given in Eq. (5.8).

4. Set baseline parameters for iterations: The design of power interconnects and their area allocation depends on the chip power. However, chip power is not known until repeaters are designed in the multilevel wiring network, especially in sub-90nm chips where repeaters consume a significant fraction of total power. Also, design of the interconnect stack needs some knowledge of via blockage caused by repeaters. Thus, an iterative process is followed for assigning wires in a multilevel wiring network. An initial chip power estimate is set (as 100W, say) and the number of repeaters is set as 0.

5. Local interconnect modeling: Local wire pitch is set as $2F$. Using Equations (5.23), (5.24) and (5.25), the longest wire routed in M1 and M2 is determined.

6. Arrangement of wires without repeaters: Once the longest wire routed in M1/M2 is determined, it is set as l_{min} in Eq. (5.26). Equations (5.26) and (5.27a) are then used to find

the pitch of M3/M4 and and maximum wire length routed in them. This in turn is set as l_{min} for the next pair of metal levels and this process continues till the longest interconnect of the wiring distribution is assigned a pitch.

7. Global interconnect modeling: A top-down process of global interconnect pitch selection and repeater insertion then begins. Global wire pitch is constrained to be the value found from Eq. (5.22). The area needed for routing power wires is then found from Eq. (5.15), and it helps calculate the area available for signal wires in global wire levels. Clock wire area is neglected in IntSim because previous work has shown it is small [5.14]. Repeaters are inserted into these global signal wires, and the shortest signal wire routed in global wire levels is found based on a formula similar to Eq. (5.26).

8. Assignment of wires with repeaters: Based on the length of shortest global signal wire, wires with repeaters are assigned to the pair of metal levels below the global wire levels, based on Equations (5.26) and (5.27b). The pitch and shortest wire l_{min} are found for this pair of wiring levels and l_{min} is set as l_{max} for the pair of wiring layers below it. Repeater insertion is performed for the pair of wiring layers below it. This keeps continuing till one runs out of die area for placing more repeaters or till the addition of repeaters does not improve wire delay.

9. Power computation and iteration: Once repeaters are assigned, the total chip power is calculated. Logic gate power is found using device widths calculated in Step 2 and formulae given in [5.9]. Local clock power is computed by extending models in [5.19]. Wire power is calculated based on the stochastic wiring distribution [5.3], and repeater power is calculated based on Step 8 and repeater power models given in [5.20]. Leakage power variability is modeled as discussed in [5.21]. If the total power calculated is different

from the power estimate used for designing power distribution wiring, IntSim sets

$$Estimated\ power = \frac{Old\ estimated\ power + Calculated\ power}{2}$$

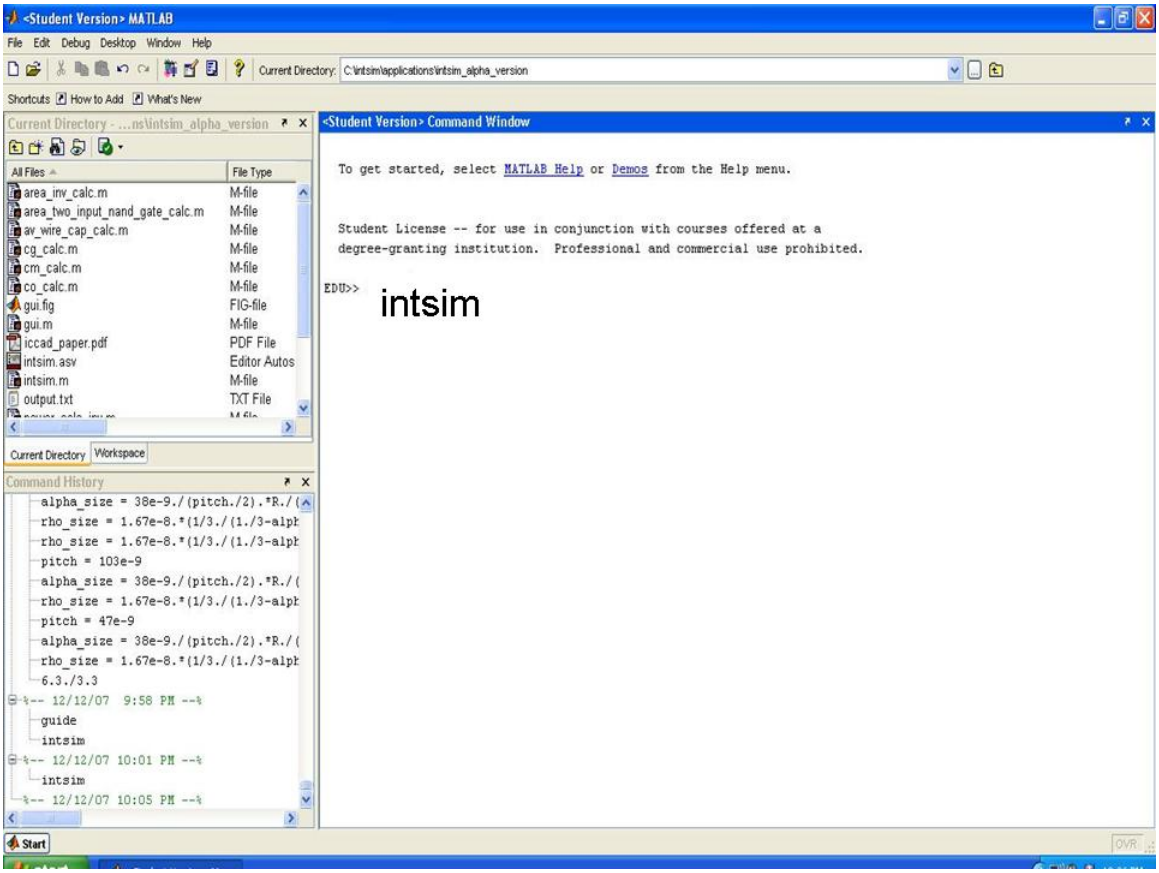
and goes back to Step 5. For the next iteration, the number of repeaters is set as the value calculated in Step 8.

10. Data output: When the simulation converges, the total number of wire levels, pitches of each wire level and a power estimate are output.

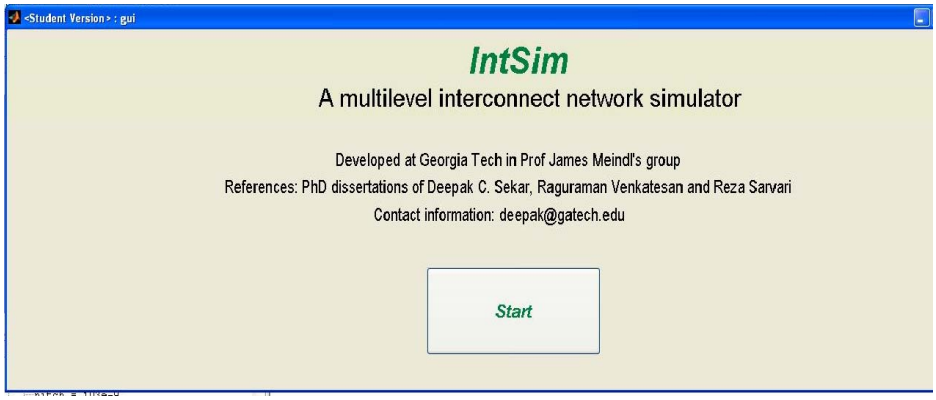
5.2.2. Graphical User Interface

IntSim is designed to run in MATLAB with an easy-to-use graphical user interface (GUI). A description of how a typical simulation in IntSim is performed is given below.

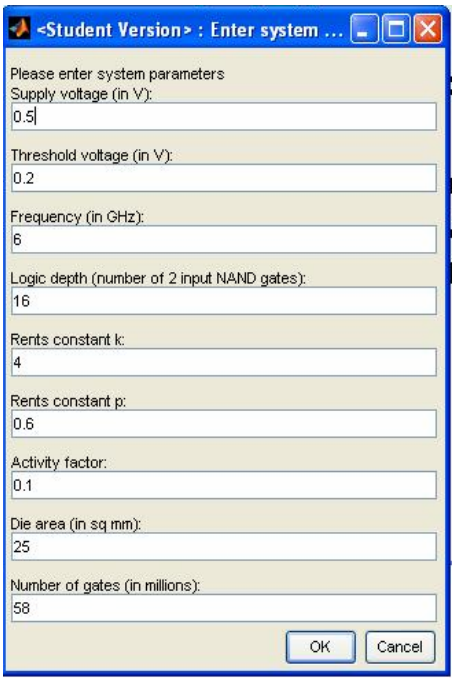
1. Type “intsim” in the command prompt for MATLAB.



2. Click “Start” in the pop-up menu that opens up.

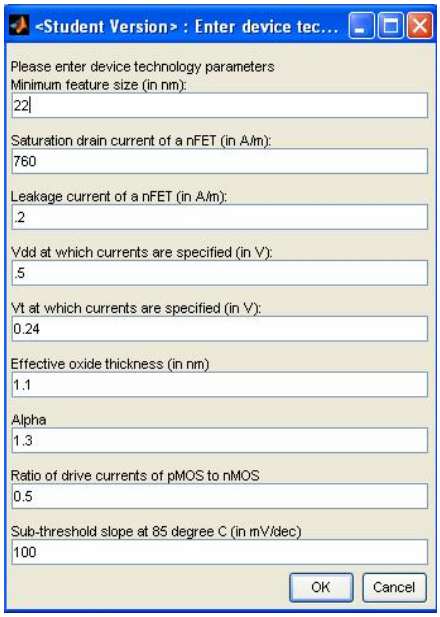


3. Enter system parameters such as supply voltage, threshold voltage, clock frequency, logic depth, Rent’s constants, activity factor, die area and number of gates.

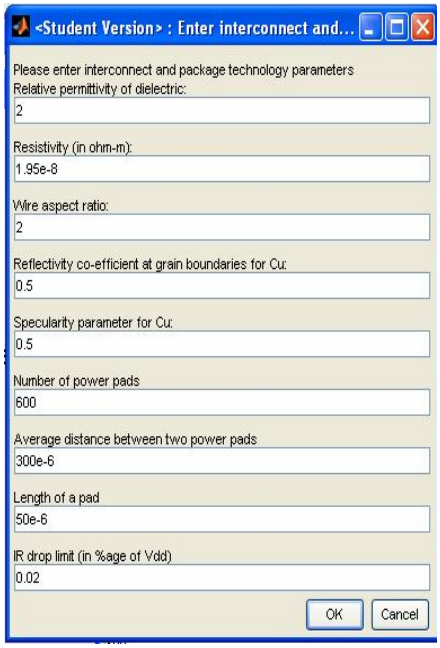


4. Enter device technology parameters such as minimum feature size, saturation drain current of a nFET, leakage current of a nFET, effective oxide thickness, ratio of drive

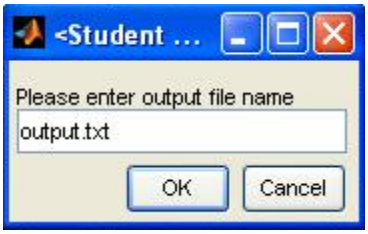
currents of pMOS to nMOS and subthreshold slope.



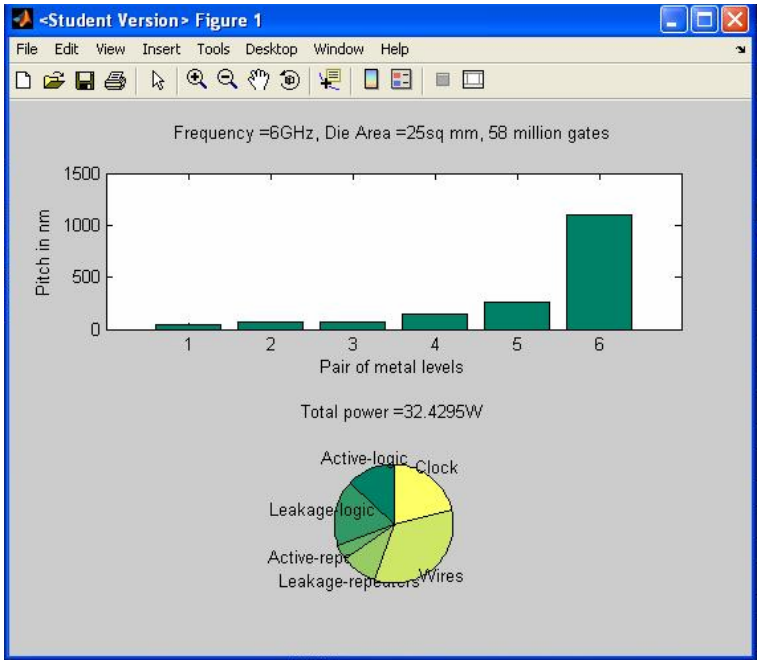
5. Enter interconnect/package technology parameters such as dielectric constant, wire aspect ratio, number/size of power pads and average distance between power pads.



6. Specify filename where text output of simulation needs to be stored.



7. A pop-up window opens with some of the results of the simulation. A user can also look at his/her specified text file for more results.



5.3. Verification and Case Studies

This section shows the verification of IntSim and details its use with two case studies.

5.3.1. Verification of CAD Tool

In this section, IntSim is used to predict wiring requirements of a commercially available 65nm 3GHz high-performance dual core microprocessor [5.22]. The predictions

for number of interconnect levels, wire pitches and logic core power are compared with actual values of these quantities. Details of this chip's transistor parameters and number of gates in each core are obtained from published data in [5.22][5.23]. The dielectric constant for interconnects is 2.9, contacted gate pitch is 220nm and supply voltage is 1.325V [5.22][5.23]. Rent's constants k and p are chosen as 4 and 0.55 respectively based on guidelines in [5.9] that custom chips would have Rent's parameters around these values. Area of a logic core is obtained from die photos and published information about total die area [5.22]. Package technology parameters are obtained from data on older high-performance chips with the assumption that package technology does not scale. The values of wire pitch obtained are not very sensitive to package technology parameters, so these rough calculations are not expected to cause significant error.

Table 5.2: Comparison of results from IntSim with actual data.

	Actual data	Prediction from IntSim
M1	210nm	220nm
M2	210nm	220nm
M3	220nm	283nm
M4	280nm	283nm
M5	330nm	283nm
M6	480nm	283nm
M7	720nm	880nm
M8	1080nm	880nm

Table 5.2 shows a comparison between wire pitches predicted by IntSim and actual

wire pitches used for that technology [5.23]. *IntSim predicts the number of metal levels to be 8, which is exactly what is used for that interconnect technology.* The wire pitches predicted by IntSim are similar to the ones actually used. One notable difference is that IntSim chooses wire pitches of two adjacent orthogonal metal levels to be the same, while the actual data has different wire pitches for adjacent orthogonal wiring levels.

IntSim also predicts the total power of logic cores of this chip to be 62.3W, while total chip power based on measured data is 80W [5.22]. Published data is not available regarding the percentage of chip power consumed by caches and I/Os for this microprocessor. However, another 65nm processor had 19% of its total power consumed by these components and 81% of total power taken up by logic cores [5.24]. Assuming the processor analyzed with IntSim has similar numbers, *the logic core power for this processor is 65.6W, which is quite close to IntSim's prediction of 62.3W*.

5.3.2. Case Study of a 22nm Air-Cooled 2D Integrated Circuit

This section shows the results of a case study conducted with IntSim on a future 22nm air-cooled logic core with 58M gates. The purpose of this study is to show how IntSim can be used to project interconnect requirements and generate die size, frequency and power estimates in future generations of technology. Device technology parameters are chosen to be ITRS low operating power technology parameters. Rent's parameters k and p are 4 and 0.6 respectively. Two "fat" global wire levels are used for this design. The logic core is assumed to be cooled with an air cooled heat sink having a thermal resistance of $0.6^{o}C\text{-}cm^2/W$. For a maximum operation temperature of $85^{o}C$ (for reliability) and ambient temperature of $25^{o}C$, the maximum power density of the logic core can be $(85\text{-}25)/0.6=100W/cm^2$.

Table 5.3 shows power, power density and interconnect requirements predicted by IntSim for different frequency and die size values for this logic core. Tables such as these can help a microprocessor architect generate rough estimates for frequency, die size, pitches of interconnect levels and power of a chip prior to design. For example, a clock frequency of 6.5GHz and die size of 25mm^2 would be a good choice for the logic core analyzed in Table 5.3. This is because 6.5GHz is the highest frequency that gives a power density less than 100W/cm^2.

Table 5.3: Design space exploration with IntSim.

Frequency	Die size	Power predicted by IntSim	Power density predicted by IntSim	Number of metal levels predicted by IntSim
5GHz	15mm^2	18W	120W/cm^2	14
	20mm^2	19.9W	100W/cm^2	12
	25mm^2	20.9W	84W/cm^2	10
5.5GHz	15mm^2	24.6W	164W/cm^2	14
	20mm^2	26.6W	133W/cm^2	12
	25mm^2	25.4W	102W/cm^2	12
6GHz	15mm^2	28W	187W/cm^2	14
	20mm^2	31W	155W/cm^2	12
	25mm^2	33.8W	135W/cm^2	12

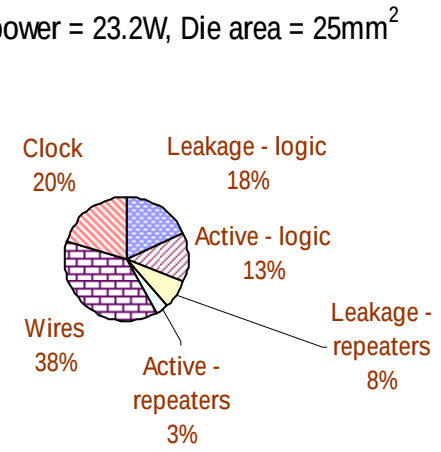


Figure 5.10: Power predictions from IntSim.

Power predictions from IntSim for this 25mm^2 5.5GHz logic core are summarized in Fig. 5.11. The wiring requirement is summarized in Table 5.4. These wire pitch values can be used to develop a multilevel interconnect technology suitable for this logic core.

Table 5.4: Wiring predictions from IntSim.

Metal levels	Wire pitches	Repeater count	Percentage of total wire area available for signal wires	Percentage of total wire area available for power wires and vias	Percentage of total wire area used for signal via blockage
M1, M2	44nm		29%	15%	6%
M3, M4	100nm		42%	4%	4%
M5, M6	111nm		38%	4%	8%
M7, M8	176nm	2.5M	45%	5%	~0%
M9, M10	224nm	0.5M	43%	7%	~0%
M11, M12	782nm	0.02M	25%	25%	~0%

5.3.3. Case Study of a 22nm Microchannel-cooled 3D Integrated Circuit

This section shows the results of a case study conducted with IntSim on a future 22nm microchannel-cooled logic core with 58M gates. The microchannel-cooled logic core forms part of the 3D integrated circuit configuration described in Chapter 2. This structure is shown below in Fig. 5.11.

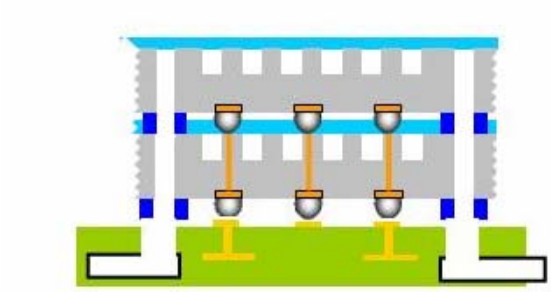


Figure 5.11: Schematic of Microchannel-cooled 3D Integrated Circuit under consideration.

The junction-to-ambient thermal resistance for each chip in this 3D integrated circuit is 0.24^{o}C-cm^{2}/W, as discussed in Chapter 2. For a maximum operation temperature of 85^{o}C (for reliability) and ambient temperature of 25^{o}C, the maximum power density of the logic core can be (85-25)/0.24=250W/cm^{2}. Supply voltage is 0.8V while other device and system parameters are taken from the ITRS. Through-silicon electrical and fluidic vias are assumed to consume 5% of the total area of this logic core.

Simulations are run with IntSim for different clock frequency and die size values as shown in Table 5.5. The maximum clock frequency that results in a power density of less than 250W/cm^{2} is 8.5GHz while the minimum die size that allows this clock frequency and power density is 35mm^{2}. Thus, a designer could choose 8.5GHz as the clock frequency and

$35mm^2$ as the die size.

Table 5.5: Design space exploration with IntSim.

Frequency	Die size	Power predicted by IntSim	Power density predicted by IntSim	Number of metal levels predicted by IntSim
8GHz	$30mm^2$	83W	$276W/cm^2$	10
	$35mm^2$	79W	$226W/cm^2$	12
	$40mm^2$	81W	$202W/cm^2$	10
8.5GHz	$30mm^2$	92W	$307W/cm^2$	12
	$35mm^2$	86W	$246W/cm^2$	12
	$40mm^2$	92W	$229W/cm^2$	12
9GHz	$30mm^2$	102W	$340W/cm^2$	14
	$35mm^2$	105W	$300W/cm^2$	12
	$40mm^2$	112W	$280W/cm^2$	10

The wiring requirement is summarized in Table 5.6. These wire pitch values can be used to develop a multilevel interconnect technology suitable for this logic core. An interesting point to note is that for certain metal levels such as M1, M2, M9 and M10, the area occupied by signal interconnects is less than the area occupied by ancillary functionality such as power interconnects, via connections to higher levels of metal, electrical through-silicon vias and fluidic through-silicon vias. Table 5.6 reveals that, on the average, *interconnects responsible for ancillary functionality consume 40% of all routable wiring tracks for the logic core!*

Table 5.6: Wiring predictions from IntSim.

Metal levels	Wire pitches	Percentage of total area for signal wires	Percentage of total area for power wires and vias	Percentage of total wire area for signal via blockage	Percentage of total area for electrical and fluidic through-silicon vias
M1, M2	44nm	22%	15%	3%	5%
M3, M4	74nm	39%	4%	2%	5%
M5, M6	164nm	37%	7%	1%	5%
M7, M8	296nm	33%	12%	~0%	5%
M9, M10	944nm	23%	22%	~0%	5%
Averaged from M1 to M10		30%	20%		

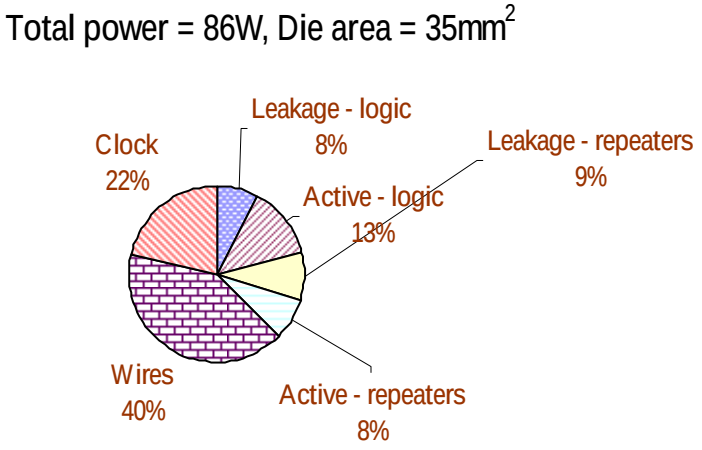


Figure 5.12: Power predictions from IntSim.

Power predictions from IntSim for this 35mm^2 8.5GHz logic core are summarized in Fig. 5.12.

5.3.4. Applications

IntSim could be used in industry for prediction of interconnect pitches, number of metal levels, die size, power and/or clock frequency of an integrated circuit prior to design. It could also be used to study scaling trends and estimate benefits of different technology and design innovations. Students in universities could use this CAD tool and interactively learn how a GSI chip works as well.

5.4. Summary

This chapter describes a CAD tool called IntSim that co-designs signal, power, clock and thermal interconnects along with via blockage. IntSim utilizes a new stochastic signal wire length distribution model, a newly derived global interconnect model, an energy-delay product based repeater insertion model, and an algorithm that co-designs various types of interconnects and vias on an integrated circuit. IntSim is verified with actual data from a commercial microprocessor and is used in this chapter to predict characteristics of logic cores in future 2D and 3D stacked integrated circuits. It is available for download from www.ece.gatech.edu/research/labs/gsigroup.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

This chapter begins with a summary of the contributions of this dissertation in Section 6.1. Following this, avenues for future research are described in Section 6.2.

6.1. Contributions of this Research

The main findings of this research are as follows:

- A microchannel-cooled high-performance 3D Integrated Circuit technology with each die having a thermal resistance of 0.24^{o}C/W to its heat sink is developed. Fluidic network fabrication proceeds at the wafer-level, is compatible with CMOS processing and flip-chip assembly and requires four lithography steps. Demonstrated through-silicon electrical via density is 2500/cm^2. To the best of the author's knowledge, this represents the first experimental effort towards microchannel cooling of 3D integrated circuits.
- Carbon nanotube interconnects can potentially provide a 56% reduction in power and 39% reduction in die size for a 22nm 4GHz logic core, *if* manufacturing challenges with carbon nanotube interconnects are solved.
- Compact repeater insertion models that involve minimization of energy-delay product of a repeated wire are developed. It is also found, for the first time, that use of unique device technologies for logic and repeater transistors could be beneficial to future GSI chips.
- Parallel processing architectures could significantly reduce interconnect

requirements in future chips. A 2.5GHz quad core chip, for example, requires five fewer metal levels than a 10GHz single core chip for a 22nm technology.

- A circuit technique that improves solder bump electromigration lifetimes by several orders of magnitude is invented. This can be particularly useful in applications where solder electromigration is a serious challenge, such as 3D-ICs and automotive electronics.
- An improved on-chip power distribution architecture for 2D and 3D integrated circuits consisting of power and ground planes separated by a high k dielectric is proposed. The feasibility of fabricating such structures with high yield is demonstrated.
- A CAD tool called IntSim is developed to simulate multilevel interconnect networks in GSI chips. IntSim includes an improved stochastic signal wire length distribution, a newly derived global interconnect model and a methodology to co-design signal, power, clock and thermal interconnects. Results from IntSim have been validated with data from a 65nm microprocessor. This CAD tool is available for download from www.ece.gatech.edu/research/labs/gsigroup and is also provided in a CD on the back-cover of hard copies of this document.

6.2. Avenues for Future Research

Several opportunities for future research on this topic exist. Some of these are listed in this section.

6.2.1. Wafer-to-Wafer Bonding Approach for Microchannel Cooled 3D-ICs

The work on thermal interconnects can be extended by exploring wafer-to-wafer

bonding approaches [6.1] for enclosing microchannels instead of using the sacrificial polymer and Avatrel approach that is described in Chapter 2. Essentially, silicon dioxide obtained during back-end-of-line (BEOL) processing of one of the chips in a 3D stack would cover the microchannels of a chip below it in the 3D stack, as shown in Fig. 6.1.

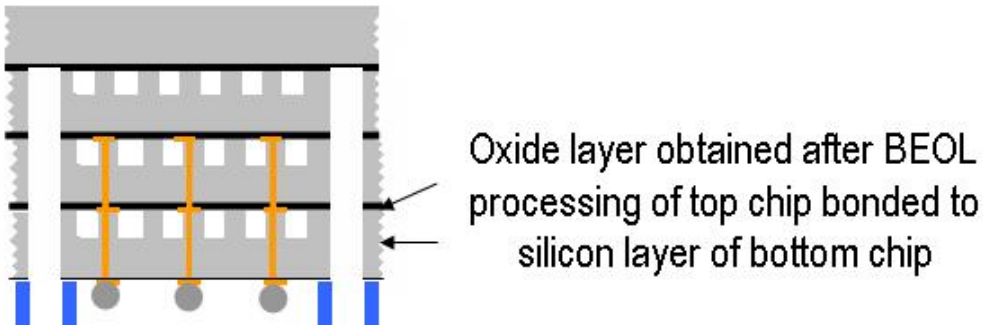


Figure 6.1: Wafer-to-wafer bonding approach for fabrication of microchannel-cooled 3D Integrated Circuits.

6.2.2. 3D Stacked SRAM Cache Memory

A high-performance microprocessor today typically has 40% of its area occupied by logic circuits while 60% of its area is consumed by SRAM arrays. While logic circuits require 10 to 12 levels of metal for sub-45nm technologies, SRAM caches rarely require more than 5 to 6 levels of metal. SRAM cells also frequently have longer channel lengths, higher threshold voltages and thicker gate oxides compared to logic circuits. This opens up opportunities for fabricating SRAM arrays on a separate chip and 3D stacking them with logic circuits to form a microprocessor, as shown in Fig. 6.2. The process for fabricating SRAM arrays could have fewer levels of metal, higher threshold voltages, longer channel

lengths and/or higher oxide thickness thereby saving process and mask cost. The challenges involved with implementing this scheme are the increased cost of 3D stacking and the elevated power densities that arise from such stacking.

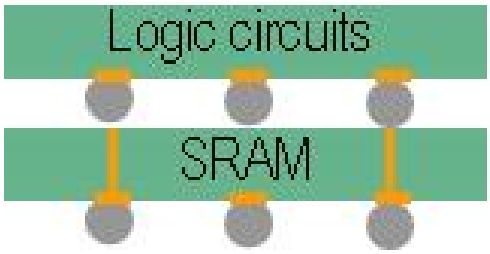


Figure 6.2: 3D stacking of SRAM with logic circuits to form a microprocessor.

6.2.3. Stacking of 3D Phase Change Memory Arrays with Microprocessors

Three-dimensional one time programmable (OTP) arrays were introduced by Matrix Semiconductor in 2003 at the Intl. Solid State Circuits Conference [6.2]. These arrays consisted of multiple layers of polysilicon diodes as steering elements and antifuses as memory elements. One could envision the antifuse being replaced by a resistive memory element such as a phase change material. Phase change materials such as $Ge_2Sb_2Te_5$ (GST) and GeSb are being investigated by several DRAM and flash memory manufacturers as next-generation memory materials, since phase change memory arrays could have the speed of DRAM and the non-volatility of flash memory. Stacking such 3D phase change memory arrays with microprocessor chips could provide high memory bandwidths along with low latency, while reducing the area occupied by storage class memory in a high-performance server considerably. Fig. 6.3 shows a pictorial representation of this

concept.

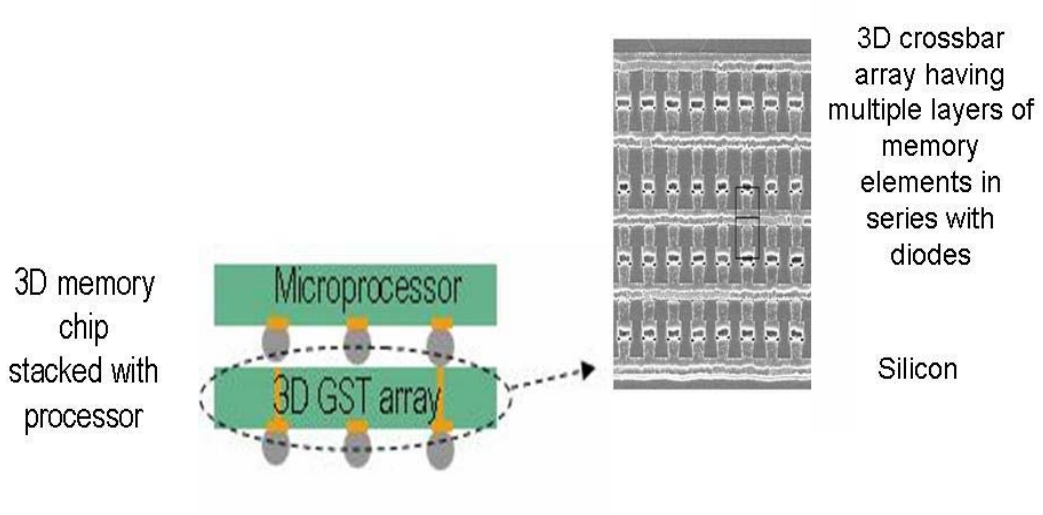


Figure 6.3: Stacking of 3D phase change memory arrays with microprocessors.

6.2.4. Physical Limits of Copper Interconnects

Copper wire resistivity increases exponentially when feature sizes scale down as discussed in Chapter 3. Scaling a circuit block from one technology generation to the next typically brings in about 50% die area savings. However, increases in wire resistivity could cause a die area penalty to be incurred while scaling down. This is because wires would need to be sized larger to compensate for increases in wire resistivity, which in turn, would require more die area. It would be interesting to study how this die area penalty changes with scaling. With speed and power advantages of scaling reducing in the post-classical scaling era [6.3], most integrated circuit manufacturers scale just to get higher component density. If even component density is sacrificed due to copper wire resistivity increases, that might prevent many manufacturers from scaling device technologies in the future.

APPENDIX A

SOLUTION OF EQUATIONS TO CO-DESIGN THERMAL AND ELECTRICAL FUNCTIONALITY

The two equations representing the model derived in Section 2.1 are given below for convenience. These essentially represent two equations in two unknowns, temperature (T) and power (P).

$$P = \frac{T - T_{amb}}{R_{th}} \qquad \ldots(A.1)$$

$$P = \left.\frac{W}{L}\right)_{av} N_{gates} V_{dd}(T) I_{leak0} e^{-\frac{V_t(T)}{N_s}} \left(\frac{\alpha - 1}{2N_s\alpha} + 1\right) \qquad \ldots(A.2)$$

Table A.1: Description of symbols used in model.

Symbol	Description
R_{th}	Thermal resistance of logic cores in ^{o}C/W
T_{amb}	Ambient temperature in K
N_{gates}	Number of logic gates
N_s	Sub-threshold slope factor in mV
$\left.\frac{W}{L}\right)_{av}$	Width to length ratio of transistors in a typical logic gate
I_{leak0}	Leakage current co-efficient of a typical minimum size logic gate in A
$V_{dd}(T)$	Optimal supply voltage obtained from the Nose-Sakurai model in V
$V_t(T)$	Optimal threshold voltage obtained from the Nose-Sakurai model in V

A description of symbols used in Eq. (A.1) and Eq. (A.2) is given in Table A.1. Substituting equations for optimal supply and threshold voltage values from Nose and Sakurai's paper in Eq. (A.1) and Eq. (A.2) and solving them self-consistently, we get the following cubic equation for temperature.

$$T^3 + T^2\left(-\frac{2}{B} - T_{amb} - R_{th}\frac{2nk}{q}\frac{A}{B^2}\right) + T\left(\frac{2T_{amb}}{B} + \frac{1}{B^2} - R_{th}\frac{A}{B^2}\left(\frac{\alpha-1}{\alpha}\right) - R_{th}\frac{2nkC}{qB^2}\right) - \frac{T_{amb}}{B^2} - R_{th}\frac{C}{B^2}\left(\frac{\alpha-1}{\alpha}\right) = 0 \quad \ldots(A.3)$$

where

$$A = k_1 afC_l \frac{nk}{q}\left(-log\left(\frac{2afC_l}{I_o}.\frac{340nk}{q}.\frac{1}{1-340\left(\frac{fC_lKL_d}{I_o}\right)^{1/\alpha}\frac{nk}{eq}}\right) + \frac{(\alpha-1)}{e}\left(\frac{fC_lKL_d}{I_o}\right)^{1/\alpha}\right)$$

$$B = \left(\frac{fC_lKL_d}{I_o}\right)^{1/\alpha}\frac{nk}{eq}$$

$$C = \Delta V_t . k_1 afC_L$$

$$k_1 = \left(\frac{W}{L}\right)_{av} N_{gates}\frac{I_{leak0}}{I_o}$$

In the above equations, a is the activity factor, f is the clock frequency in Hz, C_l is the load capacitance of a minimum size nMOS transistor in F, n is a sub-threshold slope factor, k is Boltzmann's constant, q is charge on an electron in C, I_o is leakage current of a minimum size nMOS transistor in A, L_d is the logic depth, α is the exponent of the Alpha power law MOSFET model, ΔV_t is the change in threshold voltage due to all sources of variation in Vand K is a delay co-efficient. A reader could refer to [A.1] for more details on these symbols. Quantities whose units are not indicated are dimensionless.

There exist closed form solutions to cubic equations such as Eq. (A.3). For example, the Cardano solution [A.2] could be utilized to solve Eq. (A.3) to obtain temperature. Once temperature is obtained, Eq. (A.1) can be used to obtain power.

APPENDIX B

A MODEL TO MINIMIZE ENERGY-DELAY PRODUCT OF A REPEATED WIRE

For the purpose of this derivation, repeaters are considered to be inserted into an interconnect with resistance R_{int} and capacitance C_{int}. The output resistance and input capacitance of a minimum size repeater are R_o and C_o respectively. If the size of each repeater is h times the size of a minimum size repeater and if k repeaters are inserted into the wire, the repeated wire can be represented as shown in Fig. B.1. Here, R_o/h is the output resistance of a single repeater and hC_o is the input capacitance of a single repeater while R_{int}/k and C_{int}/k are the resistance and capacitance of a single segment of the repeated wire respectively.

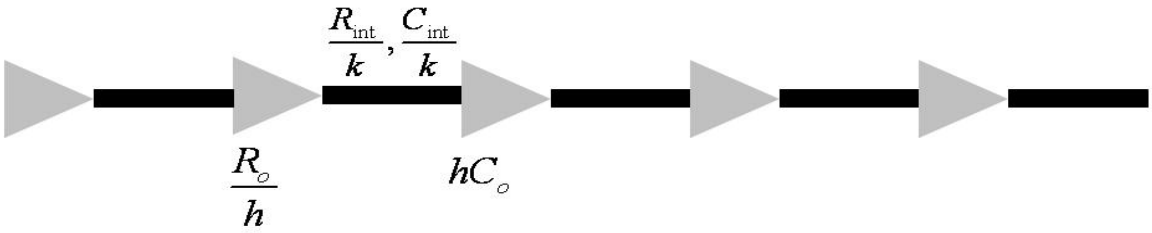


Figure B.1: Diagrammatic representation of a repeated wire.

The delay of this repeated wire [B.1] can be written as shown in Eq. (B.1). If a is the activity factor, V_{dd} is the supply voltage, f is the clock frequency, b is the fraction of leakage power that is not saved with clock gating and I_{leak} is the leakage current of a minimum size

repeater, the power of the repeated wire can be approximated by Eq. (B.2).

$$Delay = k\left[0.7\frac{R_o}{h}\left(\frac{C_{int}}{k}+hC_o\right)+\frac{R_{int}}{k}\left(0.4\frac{C_{int}}{k}+0.7hC_o\right)\right] \quad \ldots(B.1)$$

$$Power = \left(a\frac{1}{2}C_oV_{dd}^2f+bV_{dd}I_{leak}\right)hk+a\frac{1}{2}C_{int}V_{dd}^2f \quad \ldots(B.2)$$

A reader might observe that while dynamic power and leakage power are considered in Eq. (B.2), short circuit power is neglected. This is because short circuit power forms less than 10-15% of the total power of a sub-100nm repeated wire and previous work has shown that it can be neglected in a repeater optimization analysis [B.2-97]. Results from the model are compared with SPICE simulations in Chapter 3 to confirm this assumption.

$$Energy\text{-}Delay\ Product\ (EDP) = Delay^2.Power$$
$$=\left[0.7\frac{kR_o}{h}\left(\frac{C_{\text{int}}}{k}+hC_o\right)+R_{\text{int}}\left(0.4\frac{C_{\text{int}}}{k}+0.7hC_o\right)\right]^2\left[\left(a\frac{1}{2}C_oV_{dd}^2f+bV_{dd}I_{leak}\right)hk+a\frac{1}{2}C_{\text{int}}V_{dd}^2f\right]$$

To obtain optimal values of h and k that minimize the energy-delay product, $d(EDP)/dh$ and $d(EDP)/dk$ are set as zero. The equation $d(EDP)/dh$=0 gives

$$\left[0.7\frac{kR_o}{h}\left(\frac{C_{int}}{k}+hC_o\right)+R_{int}\left(0.4\frac{C_{int}}{k}+0.7hC_o\right)\right]^2\left(a\frac{1}{2}C_oV_{dd}^2f+bV_{dd}I_{leak}\right)k \quad \ldots(B.3)$$
$$+2\left[0.7\frac{kR_o}{h}\left(\frac{C_{int}}{k}+hC_o\right)+R_{int}\left(0.4\frac{C_{int}}{k}+0.7hC_o\right)\right]\left(-\frac{0.7R_oC_{int}}{h^2}+0.7R_{int}C_o\right)$$
$$\left[\left(a\frac{1}{2}C_oV_{dd}^2f+bV_{dd}I_{leak}\right)hk+a\frac{1}{2}C_{int}V_{dd}^2f\right]=0$$

The equation $d(EDP)/dk$=0 gives

$$\left[0.7\frac{kR_o}{h}\left(\frac{C_{int}}{k}+hC_o\right)+R_{int}\left(0.4\frac{C_{int}}{k}+0.7hC_o\right)\right]^2\left(a\frac{1}{2}C_oV_{dd}^2f+bV_{dd}I_{leak}\right)h$$
$$+2\left[0.7\frac{kR_o}{h}\left(\frac{C_{int}}{k}+hC_o\right)+R_{int}\left(0.4\frac{C_{int}}{k}+0.7hC_o\right)\right]\left(-\frac{0.4R_{int}C_{int}}{k^2}+0.7R_oC_o\right)$$
$$\left[\left(a\frac{1}{2}C_oV_{dd}^2f+bV_{dd}I_{leak}\right)hk+a\frac{1}{2}C_{int}V_{dd}^2f\right]=0 \quad \ldots(B.4)$$

Eq. (B.3) and Eq. (B.4) therefore represent two equations in two unknowns, h and k. If $k=\gamma\sqrt{\frac{R_{int}C_{int}}{R_oC_o}}$ and $h=\delta\sqrt{\frac{R_oC_{int}}{R_{int}C_o}}$, where γ and δ are arbitrary variables, Eq. (B.3) is equivalent to

$$\left(\frac{0.7}{\delta}+0.7\gamma+\frac{0.4}{\gamma}+0.7\delta\right)\delta+2\left(0.7-\frac{0.4}{\gamma^2}\right)\left(\gamma\delta+\frac{a\frac{1}{2}C_oV_{dd}^2f}{a\frac{1}{2}C_oV_{dd}^2f+bV_{dd}I_{leak}}\right)=0$$

Denoting the ratio of dynamic power to the total power of a repeater as Φ_{gate}, the above expression is

$$\left(\frac{0.7}{\delta}+0.7\gamma+\frac{0.4}{\gamma}+0.7\delta\right)+\frac{2}{\delta}\left(0.7-\frac{0.4}{\gamma^2}\right)\left(\gamma\delta+\Phi_{gate}\right)=0 \quad \ldots(B.5)$$

where $\Phi_{gate}=Transistor\ dynamic\ power\ fraction=\frac{a\frac{1}{2}C_oV_{dd}^2f}{a\frac{1}{2}C_oV_{dd}^2f+bV_{dd}I_{leak}}$ …(B.6)

Just like Eq. (B.3) has been simplified to Eq. (B.5), Eq. (B.4) can be simplified to

$$\left(\frac{0.7}{\delta}+0.7\gamma+\frac{0.4}{\gamma}+0.7\delta\right)+\frac{1.4}{\gamma}\left(1-\frac{1}{\delta^2}\right)\left(\gamma\delta+\Phi_{gate}\right)=0 \quad \ldots(B.7)$$

Eq. (B.5) and Eq. (B.7) represent two equations in two unknown variables, γ and δ, and one known variable, Φ_{gate}. *Thus, it is clear that γ and δ are functions of Φ_{gate} and are*

independent of other transistor and wire parameters.

From Eq. (B.5) and Eq. (B.7),

$$\frac{1.4}{\gamma}\left(1-\frac{1}{\delta^2}\right)=\frac{2}{\delta}\left(0.7-\frac{0.4}{\gamma^2}\right)$$

This equation when rearranged is

$$0.7\delta^2+\delta\left(\frac{0.4}{\gamma}-0.7\gamma\right)-0.7=0 \qquad \ldots(B.8)$$

Eq. (B.5) when rearranged is

$$0.7\delta^2+\delta\left(2.1\gamma-\frac{0.4}{\gamma}\right)+\left(0.7+1.4\Phi_{gate}-0.8\frac{\Phi_{gate}}{\gamma^2}\right)=0 \qquad \ldots(B.9)$$

Finding the difference between Eq. (B.8) and Eq. (B.9) and simplifying,

$$\delta=\frac{1.4+1.4\Phi_{gate}-0.8\dfrac{\Phi_{gate}}{\gamma^2}}{\dfrac{0.8}{\gamma}-2.8\gamma} \qquad \ldots(B.10)$$

Substituting Eq. (B.10) in Eq. (B.8) and simplifying yields

$$\begin{aligned}\left(\gamma^2\right)^3\left(\Phi_{gate}-1\right)+\left(\gamma^2\right)^2\left(0.5\Phi_{gate}^2-0.43\Phi_{gate}+0.79\right)\\ +\left(\gamma^2\right)\left(0.08\Phi_{gate}-0.57\Phi_{gate}^2\right)+\left(0.16\Phi_{gate}^2-0.09\Phi_{gate}\right)=0\end{aligned} \qquad \ldots(B.11)$$

This is a cubic equation in γ^2. Several closed form solutions are available for cubic equations, with the most prominently used solution being the one proposed by Cardano [B.3]. Using Cardano's solution, the six roots of Eq. (B.11) are given by

$$\gamma = \sqrt{\frac{p}{3u} - u - \frac{1}{3}\left(\frac{0.5\Phi_{gate}^2 - 0.43\Phi_{gate} + 0.79}{\Phi_{gate} - 1}\right)} \qquad \ldots(B.12)$$

where

$$p = \frac{-0.083\Phi_{gate}^4 - 0.43\Phi_{gate}^3 + 0.33\Phi_{gate}^2 + 0.15\Phi_{gate} - 0.21}{\left(\Phi_{gate} - 1\right)^2},$$

$$q = \frac{0.0093\Phi_{gate}^6 + 0.071\Phi_{gate}^5 + 0.034\Phi_{gate}^4 - 0.24\Phi_{gate}^3 + 0.25\Phi_{gate}^2 - 0.13\Phi_{gate} + 0.04}{\left(\Phi_{gate} - 1\right)^3}$$

and $u = \sqrt[3]{\frac{q}{2} \pm \sqrt{\frac{q}{4}^2 + \frac{p}{27}^3}}$

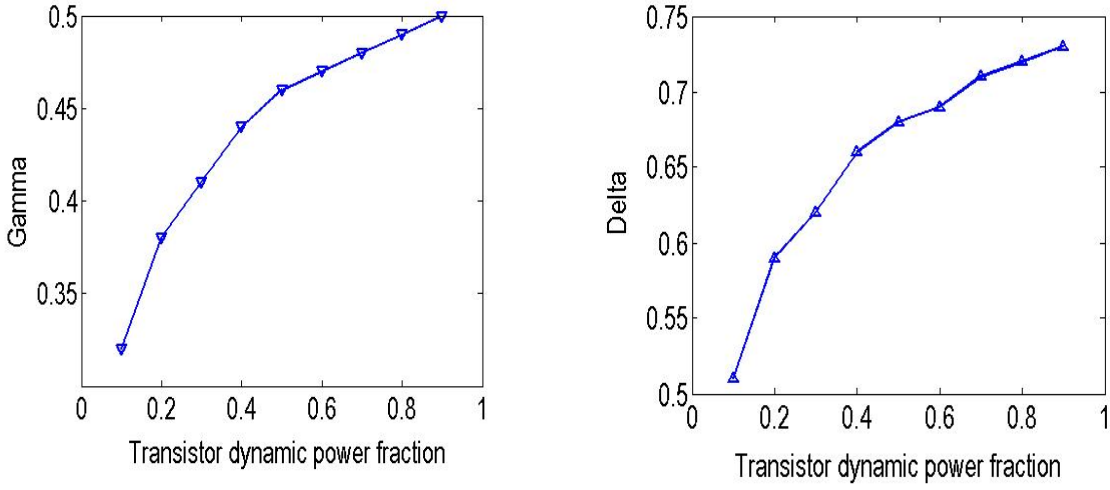


Figure B.2: Analytical solutions for γ (gamma) and δ (delta) for different values of Φ_{gate} (transistor dynamic power fraction).

Closed form solutions for δ can be obtained from Eq. (B.12), Eq. (B.8) and Eq. (B.9). Plotting the obtained values of γ and δ from these analytical solutions in Fig. B.2, it can be seen that γ and δ have a logarithmic dependence on Φ_{gate}.

While the derived analytical solutions for γ and δ are closed-form and exact, their solution is slightly cumbersome since it requires manipulation of complex numbers. Eq. (B.13) and Eq. (B.14) give empirical solutions for γ and δ that are compact and simple to evaluate. These solutions have <5% error, as shown in Fig. B.3.

$$\gamma = \left(0.73 + 0.07 \log \Phi_{gate}\right)^2 \quad \ldots(B.13)$$

$$\delta = \left(0.88 + 0.07 \log \Phi_{gate}\right)^2 \quad \ldots(B.14)$$

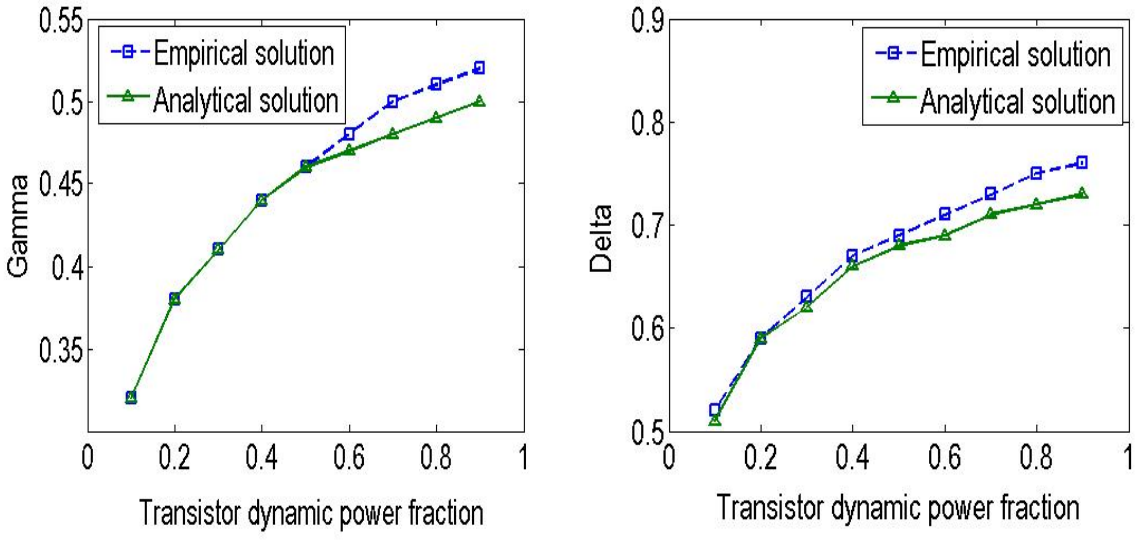


Figure B.3: Comparison of empirical solutions with analytical solutions.

Thus, the model can be summarized as follows

$$k = \gamma \sqrt{\frac{R_{int} C_{int}}{R_o C_o}} \text{ where } \gamma = \left(0.73 + 0.07 \log \Phi_{gate}\right)^2$$

$$h = \delta \sqrt{\frac{R_o C_{int}}{R_{int} C_o}} \text{ where } \delta = \left(0.88 + 0.07 \log \Phi_{gate}\right)^2$$

Substituting these expressions in Eq. (B.1) and Eq. (B.2),

Optimal delay = $\sqrt{R_{int} C_{int} R_o C_o} \left(\frac{0.7}{\delta} + 0.7\gamma + \frac{0.4}{\gamma} + 0.7\delta \right)$

Optimal energy-delay product =

$$R_{int} C_{int}^2 \left[R_o \left(a \frac{1}{2} C_o V_{dd}^2 f + b V_{dd} I_{leak} \right) \left(\frac{0.7}{\delta} + 0.7\gamma + \frac{0.4}{\gamma} + 0.7\delta \right)^2 \left(\gamma\delta + \Phi_{gate} \right) \right]$$

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