Bullshit Prediction of Quantum Computing Timeline

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Wance's prediction

0.1 Semiconductor Transistor Density

Today is 01/15/2022, till now, 3 nm semiconductor manufacturing process haven't been in official production by TSMC [1] or Samsung [2]. According to current 5 nm process, TSMC achieved a $D_{\text{trans}} = 173\,\text{MTr/mm}^2$ (mega-transistor per squared millimeter) MOSFET [3] transistor density in 2019 [4, 5]. This is equivalent to $76\,\text{nm} \times 76\,\text{nm}$ if each transistor is modeled as a square shape. A typical static RAM (SRAM) cell is made up of six MOSFETs [6], which serves as a volatile memory for a classical bit, $D_{\text{bit}} = D_{\text{trans}}/6$.

If we use published commercial processors as our benchmark, take Apple M1 [7] as an example. It uses 5 nm process, having 16000 million transistor on a $119\,\text{mm}^2$ area [8], thus its density is $D_{\text{trans}}^{(\text{M1})} = 134\,\text{MTr/mm}^2$.

0.2 Moore's Law

According to Moore's revised law of doubling transistor count every 18 months ($p = 1.5\,\text{y}$) [9], we predict that when "transistor size" is reduced to a size of a single atom or ion, the era of application of general quantum computing would truly come (for example, the deployment of fault-tolerant quantum computing surpasses all kinds of NISQ computing [16, 17] around the world). Assume it takes N_q year to reduce to single atom radius r_a. Take trapped ion $^{171}\text{Yb}^+$ as an example, hyperfine microwave clock states in ground level are chosen as a qubit, cationic radius $r_a \sim 0.23\,\text{nm}$ [10] and regard it as the size of a memory (yet an ion spacing of $\sim 2\,\mu\text{m}$ in ion chain is ignored), we get the following equation

$$2^{N_q/p} = \frac{(1\,\text{mm})^2 / (2r_a)^2}{D_{\text{bit}}}$$

$$N_p = p \lg \left[\frac{(1\,\text{mm})^2 / (2r_a)^2}{D_{\text{bit}}} \right] = 26.0\,\text{y}$$

$$N_p^{(\text{M1})} = p \lg \left[\frac{D_{\text{bit}}}{D_{\text{bit}}^{(\text{M1})}} \right] + N_p = 26.0\,\text{y} + 0.55\,\text{y}$$

If we choose neutral 133Cs atom, although Rydberg atoms are used (take principal quantum number $n = 66$ [11] and Rydberg atom radius scales with $n^2 a_0 = 230.4\,\text{nm}$ [12], $a_0 = 0.0529\,\text{nm}$ Bohr radius.), one will get unreasonable $N_q = -3.9\,\text{y}$, while we know, there was no general Rydberg quantum computer put in application as any classical computer based on semiconductor chip at that time. In addition, the qubit in 133Cs atom also uses ground-level hyperfine clock states. Thus we take $r_a \sim 0.25\,\text{nm}$ [10], and $N_p = 25.6\,\text{y}$.

Superconducting qubit like transmon usually has size of μm which also yields unreasonable N_q. But a transmon is a type of Cooper-pair box which uses Josephson effect and takes magnetic flux Φ_0 as a quantum. Typical Josephson junction in transmon are fabricated by Al and Al_2O_3 [13]. There are two independent characteristic lengths in superconductor: coherence length ξ and London penetration depth λ_L. As a type-I superconductor, bulk aluminum has $\xi \sim 1600\,\text{nm}$ and $\lambda_L \sim 16\,\text{nm}$ [14]. Using ξ yields an unreasonable N_q. Although effective penetration depth in thin-film electrode is larger than λ_L, to get a positive N_q, let's just use λ_L as the characteristic size of a qubit memory,

$$N_p = p \lg \left[\frac{(1\,\text{mm})^2 / \lambda_L^2}{D_{\text{bit}}} \right] = 10.6\,\text{y}$$

0.2.1 Error Correction Code

If we consider using a logical qubit with quantum error correction (QEC) codes as a qubit memory unit, the predictions vary with the number of physical qubits in a code. Although there are more advanced QEC codes, here I simply use the basic $[[5, 1, 3]]$ code which can encode one logical qubit. For $^{171}Yb^{+}$ ion,

$$N_p = p \lg \left[\frac{(1\,\mathrm{mm})^2 / (2r_a)^2 / 5}{D_{\mathrm{bit}}} \right] = 22.5\,\mathrm{y}$$

For 133Cs neutral atom, $N_p = 22.1\,\mathrm{y}$. For transmon superconducting qubit, $N_p = 7.1\,\mathrm{y}$

0.3 Scaling of Error Rate

Another prediction can be derived from the increasing trend of semiconductor transistors together with decreasing trend of quantum gate error rate. “According to the reported experiment results [1], the soft-error rate (SER) per logic state bit increases 8% for each technology generation.” [20]. To be continued @P.

References

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