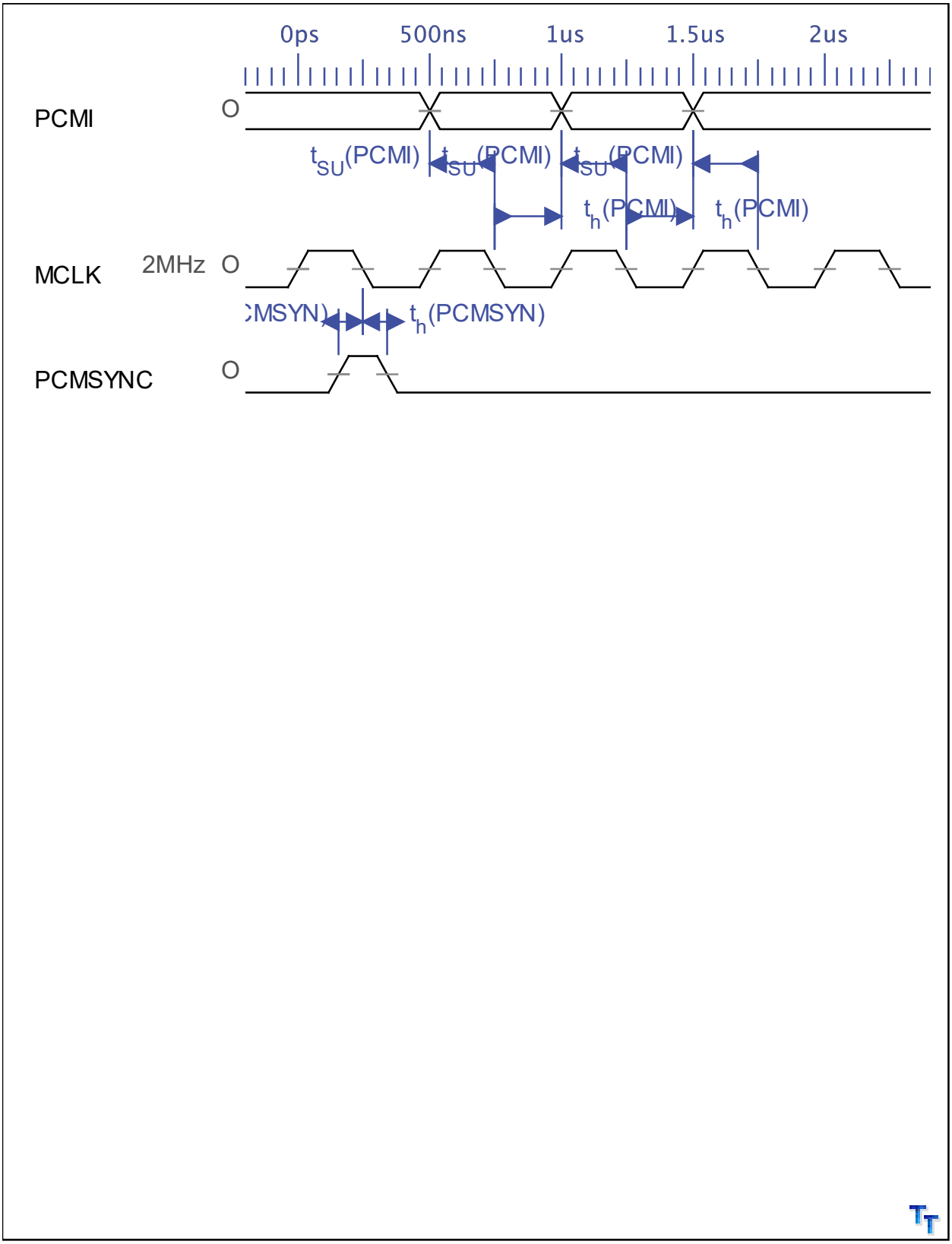
0ps
500ns
1us
1.5us
2us
PCMI
O
t_{SU}(PCMI)
t_{SU}(PCMI)
t_{SU}(PCMI)
t_h(PCMI)
t_h(PCMI)
MCLK
2MHz
O
t_h(PCMSYN)
PCMSYNC
O

General Data

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
t_{SU}(PCMSYN)	Setup time, PCMSYN high before MCLK low	to be defined	20ns	480ns	
t_h(PCMSYN)	Hold time, PCMSYN high after MCLK low	to be defined	20ns	480ns	
t_{SU}(PCMI)	Setup time, PCMI high or low before MCLK low	to be defined	20ns		
t_h(PCMI)	Hold time, PCMI high or low after MCLK low	to be defined	20ns		

Notes:

MCLK = 2 MHz (can't get 2.048 MHz)
Divider ratio on AT91RM9200 = 11
Frame sync period = 128us
Frame sync length = 256 bits