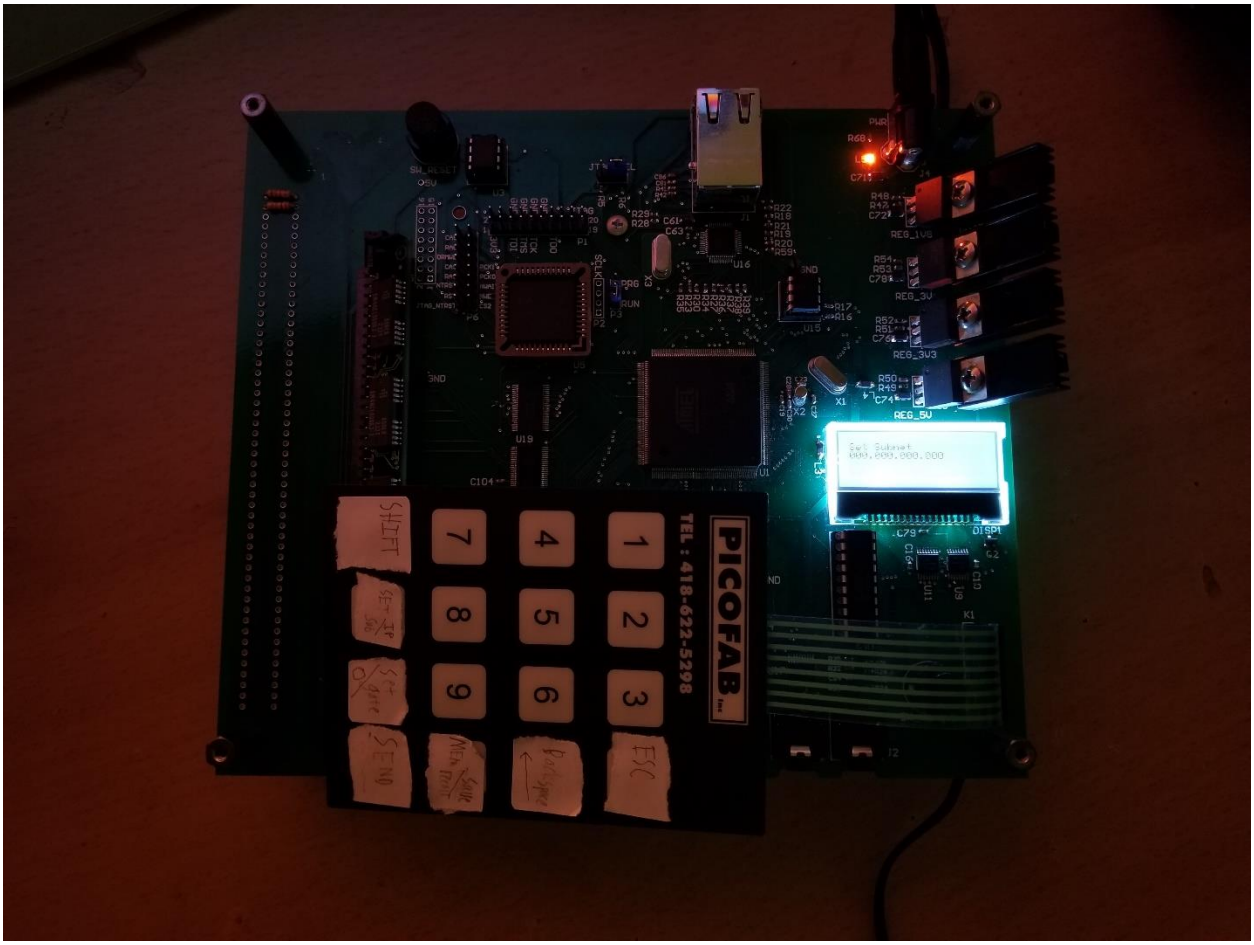
VoIP phone Technical Documentation

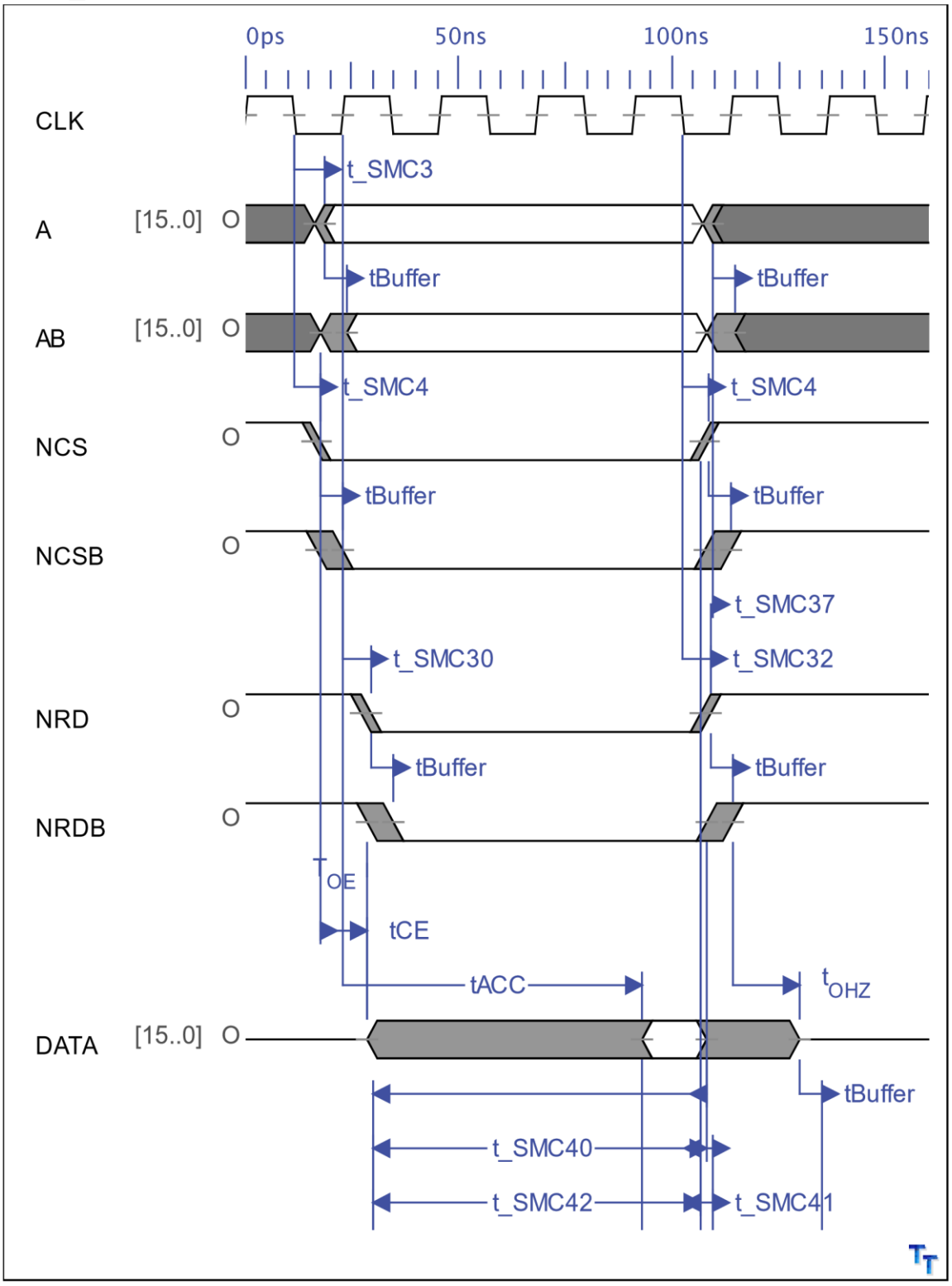


The EE52 VoIP phone is a phone that can communicate with other EE52 VoIP phones. The user controls the phone by using a 128x32 display and a 4x4 keypad. There is a headphone and microphone jack that a headset can be plugged into, and there is a button for putting the phone “on-the-hook” to hangup the call.

Will Werst

Contents

ROM_READ

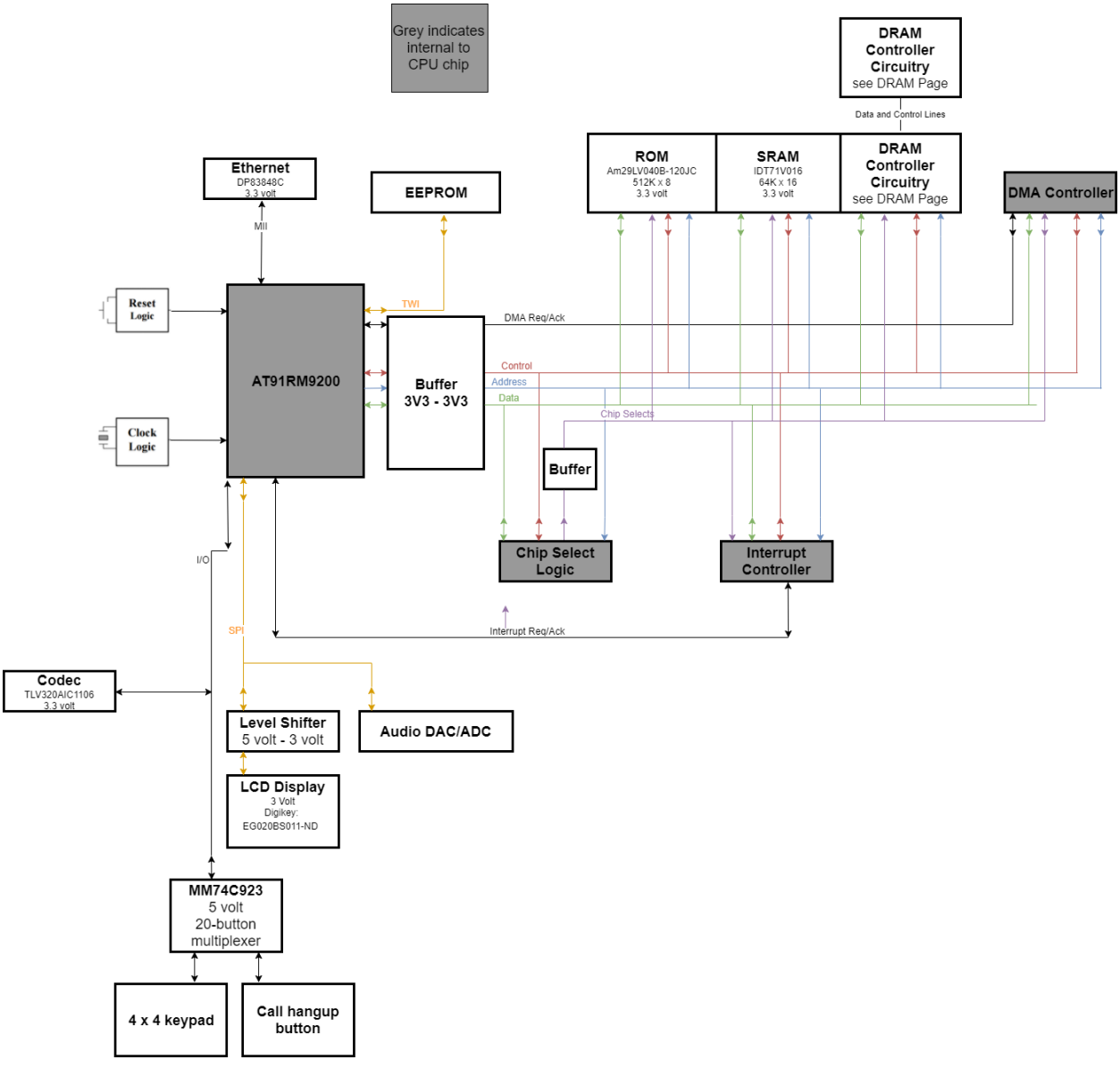


C:\Users\will\GitReps\EE52\ROM_READ.tdml

Overview

Processor	Atmel AT91RM9200
Input power	8V-12V DC 5.5mm barrel jack
Display	128x32
Headphone Jack	3.5mm mono audio jack
Microphone Jack	3.5mm
Keypad	4x4 button keypad

Block Diagram



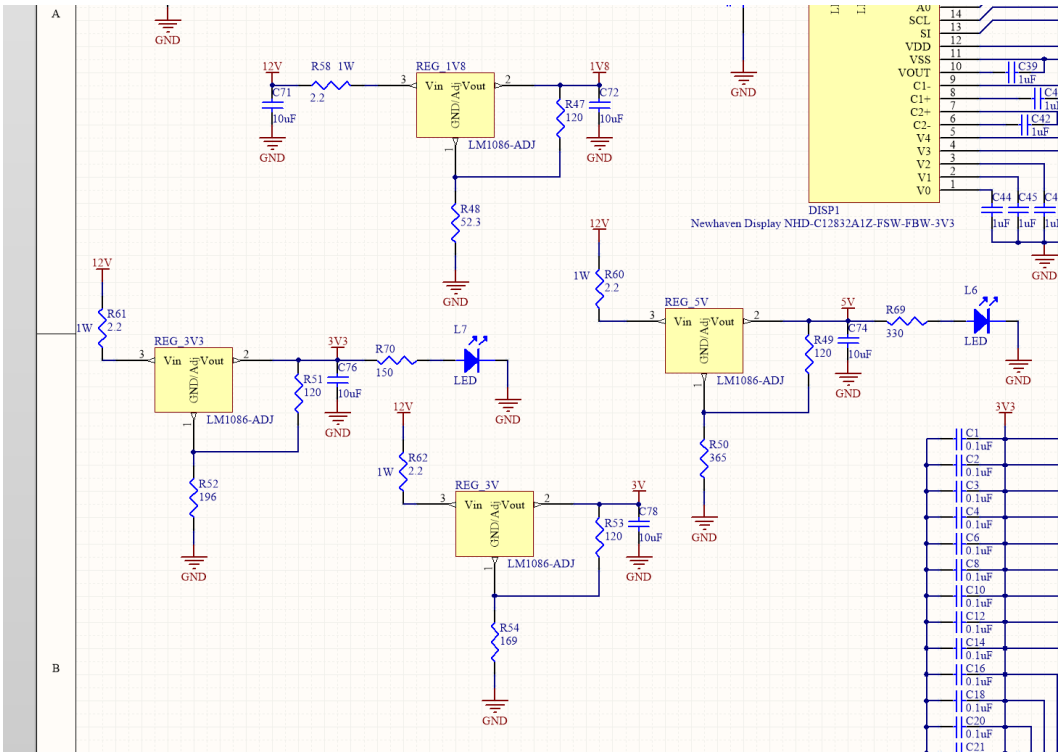
Power Circuitry

The system takes ~8V-12V DC input. The upper bound is due to thermal dissipation constraints of the linear regulator heatsinks. There are four power rails on this board.

Rail	Uses
5V	Reset circuit, DRAM, CPLD
3V3	Audio, SRAM, ROM, CPU
3V	Display
1V8	CPU Core logic

Linear Regulators

The system uses LM1086 linear regulators with heatsinks attached.

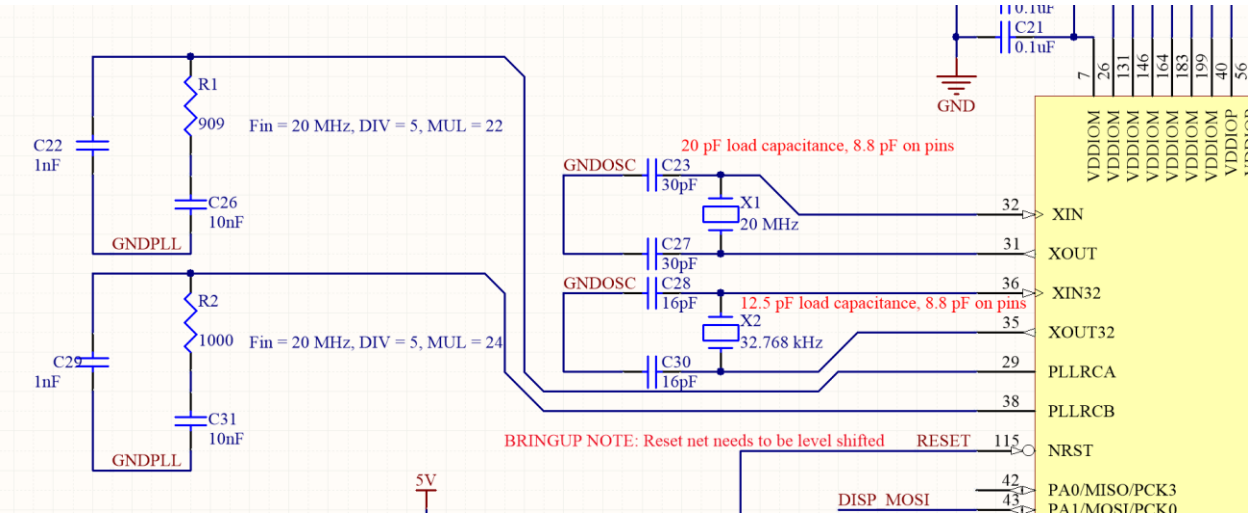


Linear regulators

CPU Support Circuitry

Clocks

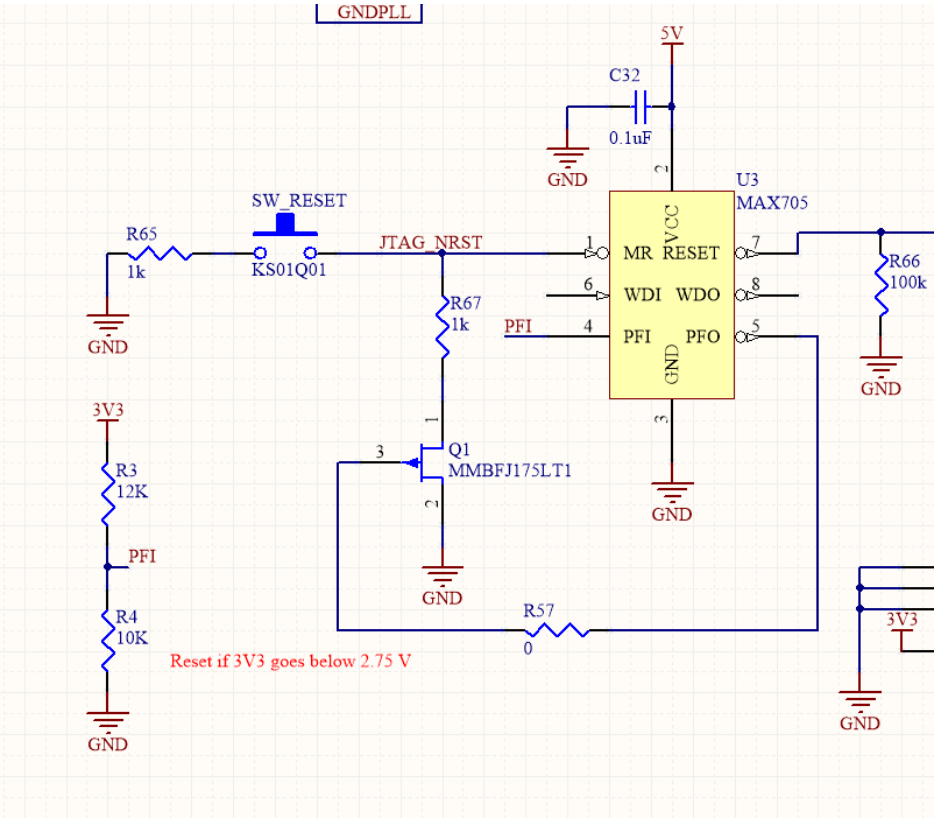
The CPU uses a 32.768 kHz slow clock and a 20 MHz main clock crystal. The main clock is scaled using a PLL to 44 MHz.



Clocks and PLL circuits

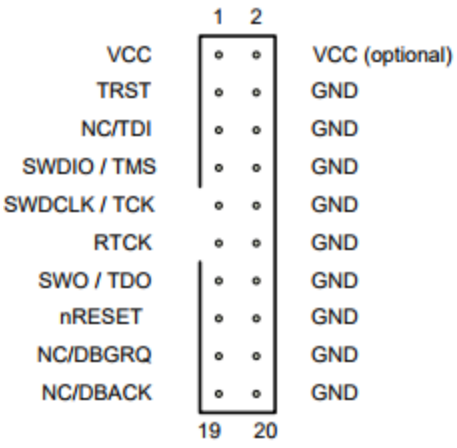
Reset

The reset circuitry uses a MAX705 chip in the standard configuration. The 5-volt reset line output is scaled using a resistor divider for devices that need 3.3V input.



JTAG

This board has a JTAG interface routed and populated for the purposes of debugging. It is a 20-pin legacy ARM IDC 0.1” pitch JTAG connector with the following pinout (see http://infocenter.arm.com/help/topic/com.arm.doc.faqs/attached/13634/cortex_debug_connectors.pdf):

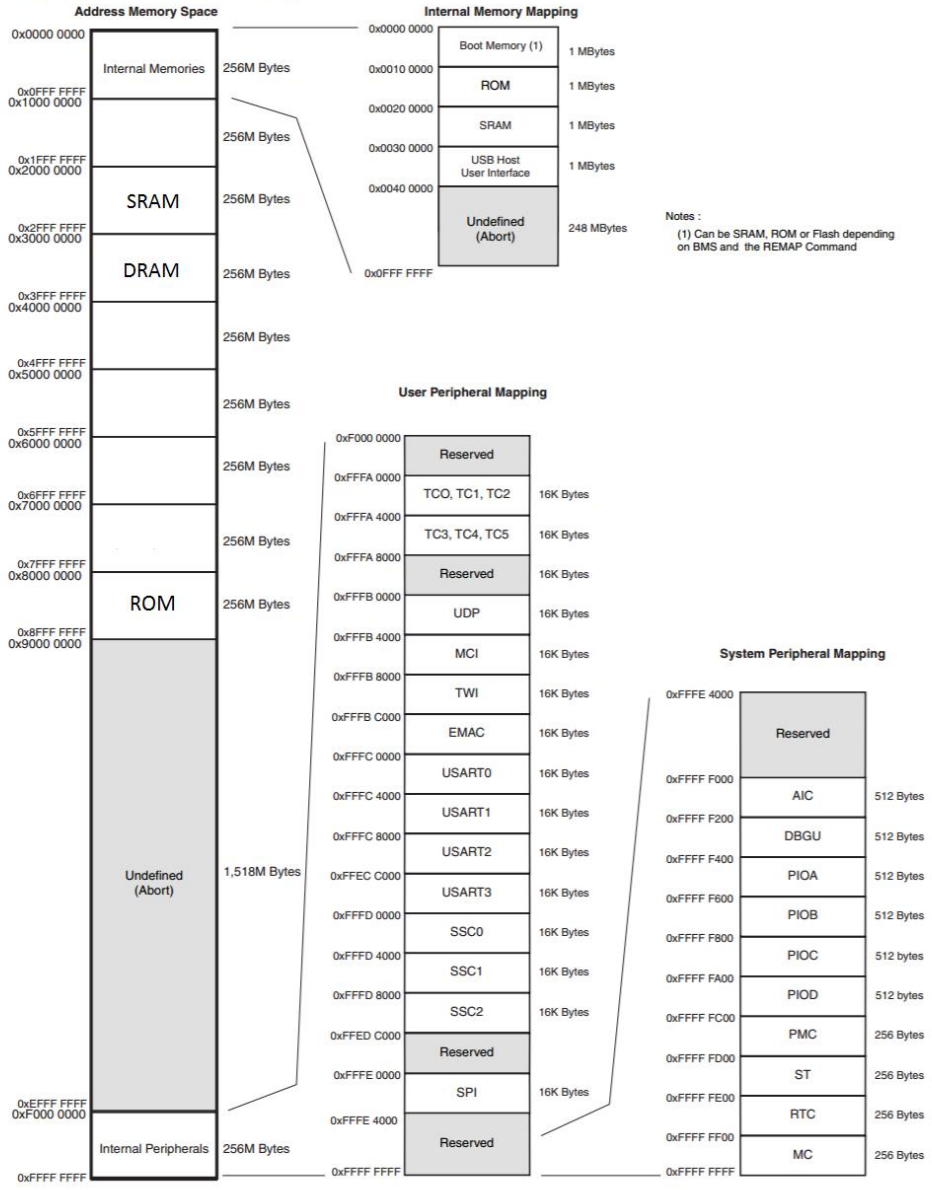


Memory

All memory access is done through 74LVT16245 buffers.

8. Memories

Figure 8-1. AT91RM9200 Memory Mapping



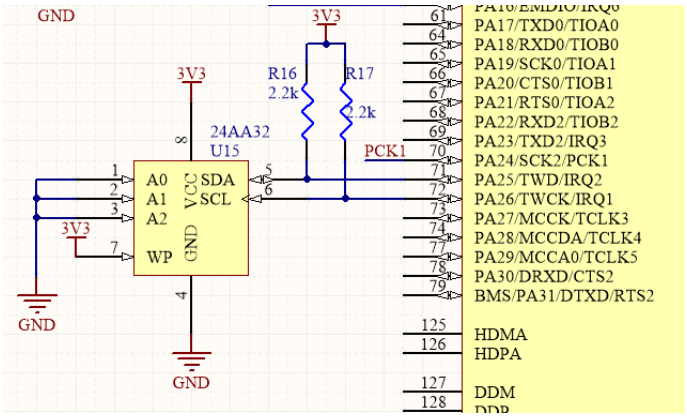
Memory map

Memory Testing

When the system boots, all of the memory in the SRAM and DRAM is checked for errors before the code is copied from ROM to SRAM for program operation. This is done in the memtest.s file. The test works by writing a few sequences of numbers that do not repeat with any 2^n periodicity, and reading back the data and comparing it against the expected sequence. This test seems to do a good job at detecting rare memory integrity issues, but it does not test for DRAM refresh being fast enough to prevent DRAM bit rot.

EEPROM Bootloader

The system uses a 24AA32 over TWI for the bootloader. This bootloader initializes the ARM CPU modes, checks for SRAM and DRAM integrity, and then copies ROM to SRAM. Future possible improvements could be to check a hash of the ROM values against a hash stored in ROM to verify ROM integrity.



ROM

This board uses a 29LV040 chip for ROM. This chip has an address bus width of 19 bits, and a data bus width of 8 bits. It is on chip select 7. See schematic in Appendix.

SRAM

This board uses a IDT71V016 chip for SRAM. This chip has an address bus width of 16 bits, and a data bus width of 16 bits. It is on chip select 1. See schematic in Appendix.

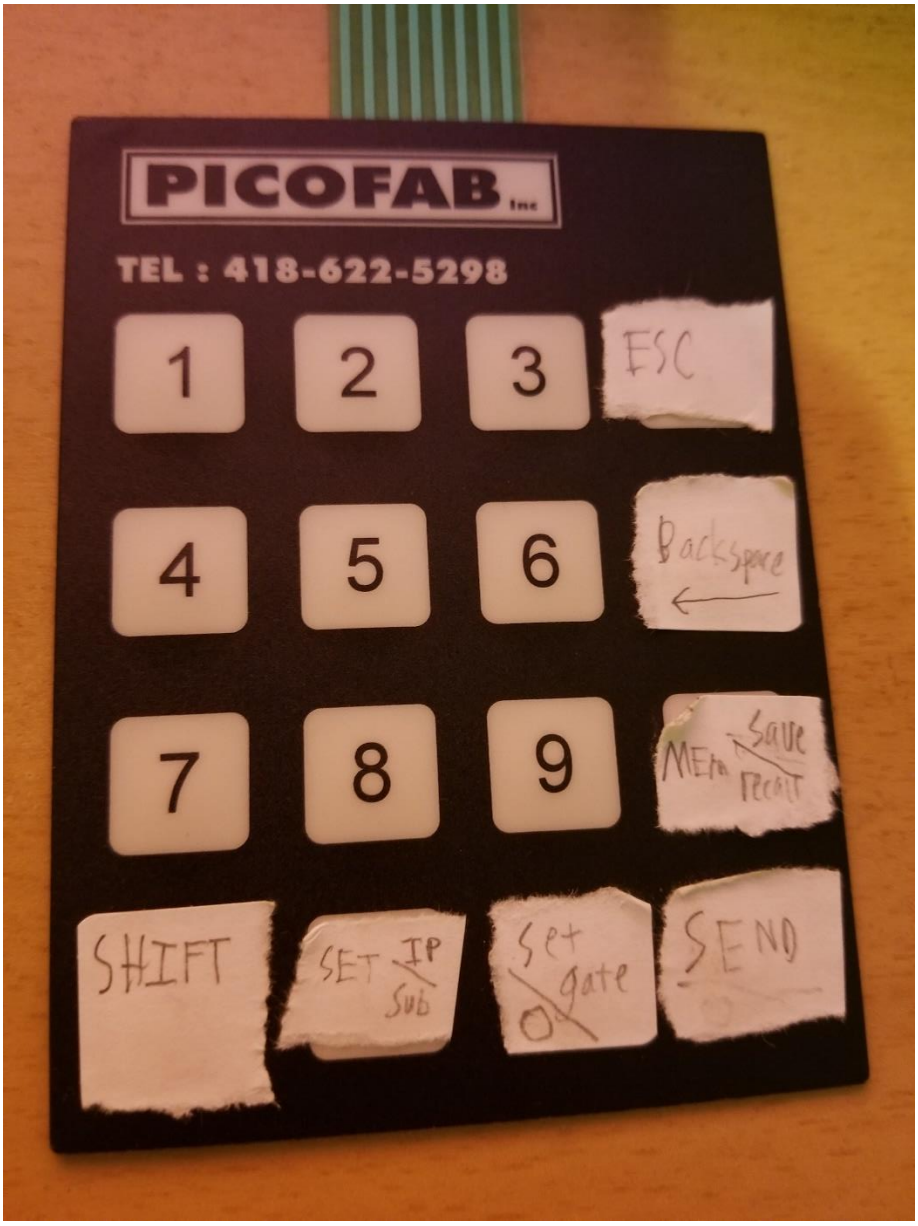
DRAM

This board uses a socket mount DRAM module. The DRAM controller is implemented in a CPLD. The address lines are multiplexed to the DRAM via U19 and U21, which are two buffers that can be toggle high-Z and enabled by the CPLD DRAM controller. The data lines are connected to the CPU data bus via a bidirectional buffer that is enabled when the DRAM chip select goes low. The directionality of the buffer is set by the NRD signal.

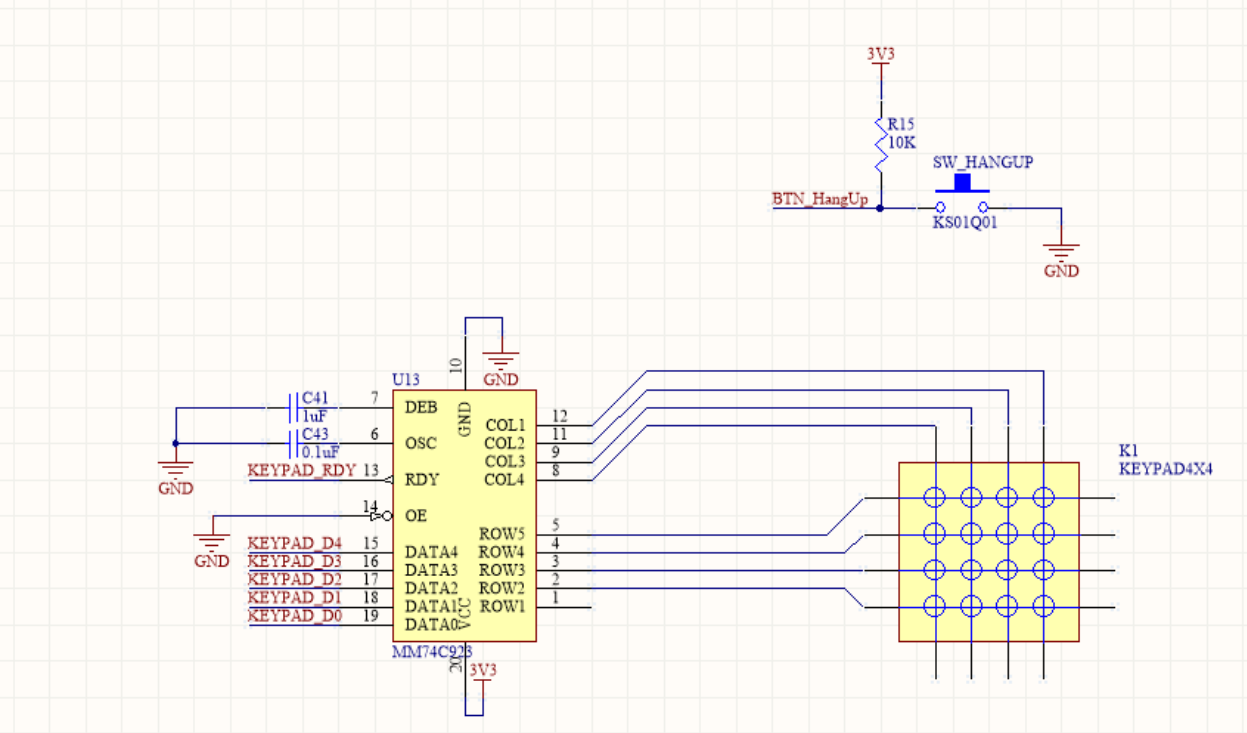
The DRAM has an effective address bus width of 20 bits, and a data bus width of 8 bits. The DRAM is on chip select 2. See Schematic in Appendix.

User Interface Components

Keypad

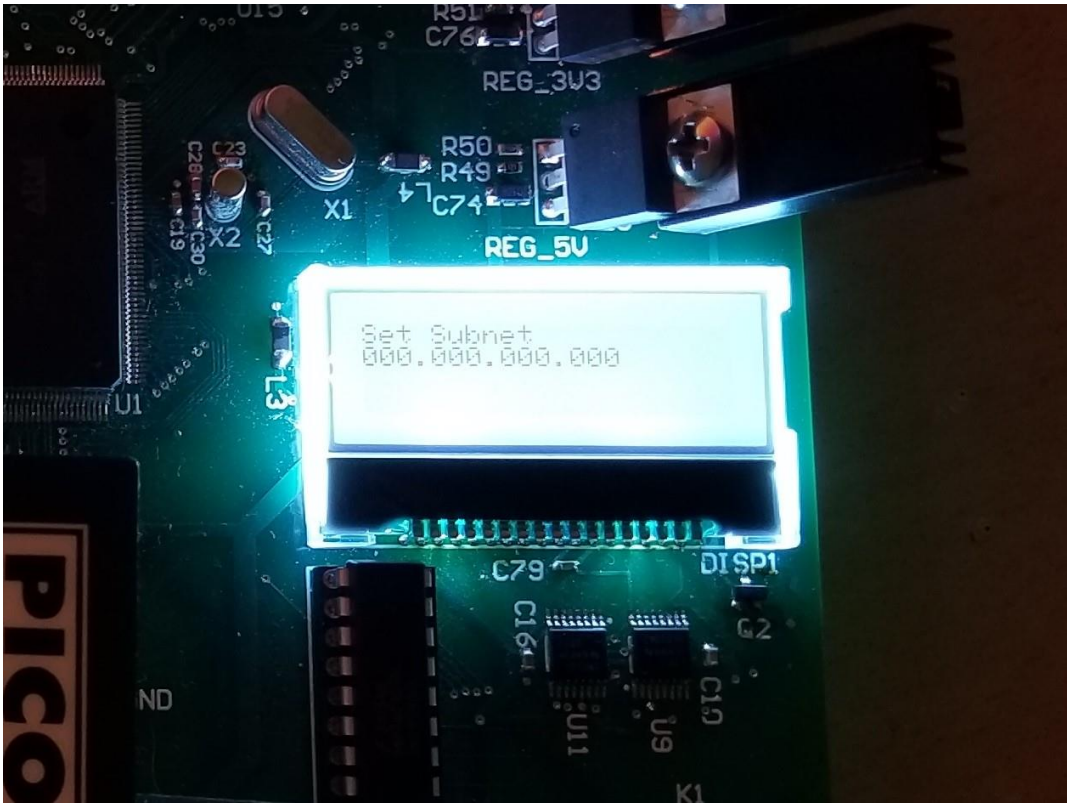


The keypad is used for user input into the device. It is a 4x4 keypad, and since more inputs are needed than are available, a shift key is used to toggle the function of a few keys. The keypad uses a MM74C923 chip for debouncing key presses. Also, on the test board, the hangup button was connected into the ROW1 channel of the chip, to simplify code. The design implemented in schematic works as well, but if the hangup button remains a button that is pressed when it is needed, rather than being a button that is always pressed when the phone is on the hook, then the hangup button can be connected to the debouncer chip. The debouncer chip can only debounce one key at a time, so if the hangup button is pressed while the user wants to press other buttons, the system would not respond to the new button presses, hence why the hangup button was kept separate in the schematic right now.



The above schematic shows the design as routed on the PCB. This design is fully functional, but on the test board, the hangup button was wired into row 1 of debouncer chip for code simplicity.

Display



The display is a NHDC12832 128x32 display. In software, the display is divided into 4 rows. Only the top two rows are used.

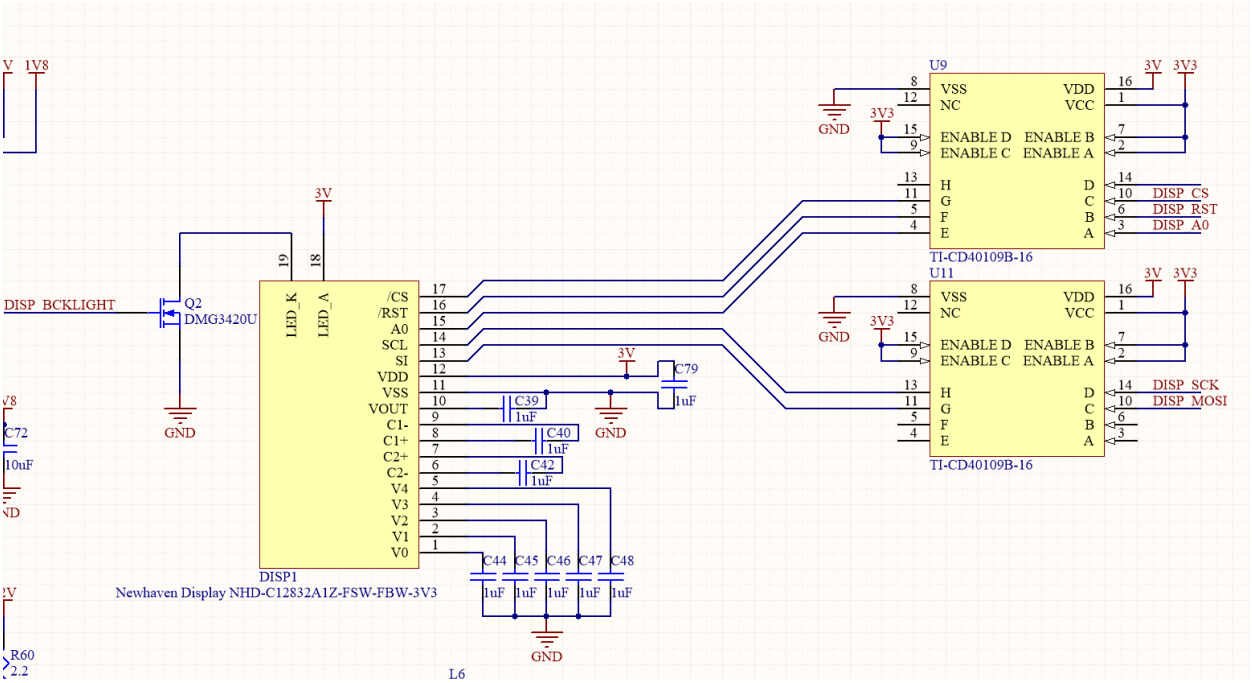
The top row displays the current menu the system is in, or the status of the system if a call is in progress.

The 2nd row displays auxiliary information for a menu, such as the IP address being set, the subnet mask, or the memory location for recall.

Data is streamed to the display using SPI, with the data transfer to the SPI peripheral done using DMA.

The display uses 3 volt power, while the CPU uses 3.3 volt, so level shifters are used.

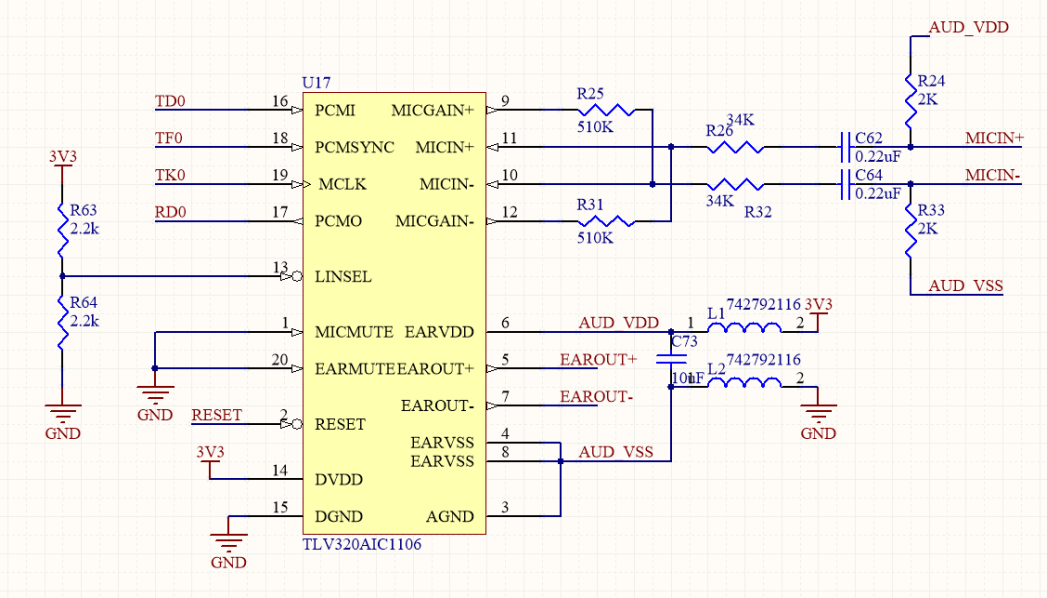
A backlight is available on the display, and is toggled via pin PA5 on the CPU.



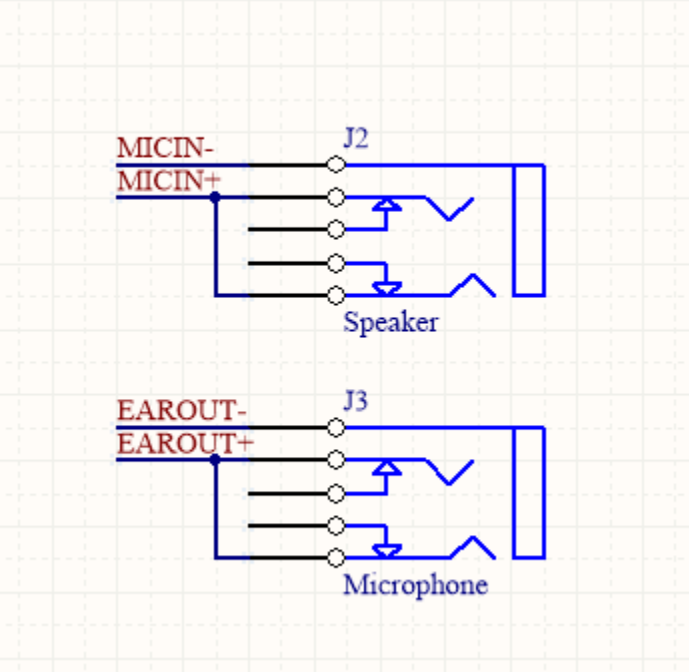
Display and level shifters for display

Audio

The audio circuitry uses the TLV320AIC1106 chip. Depending on whether companding or linear serial stream is desired, R63 or R64 can be stuffed. Currently, the code base only supports linear mode, which corresponds to R64 being stuffed. Data is sent and received from the audio chip via a synchronous serial controller on the ARM chip and a DMA engine on the ARM chip.



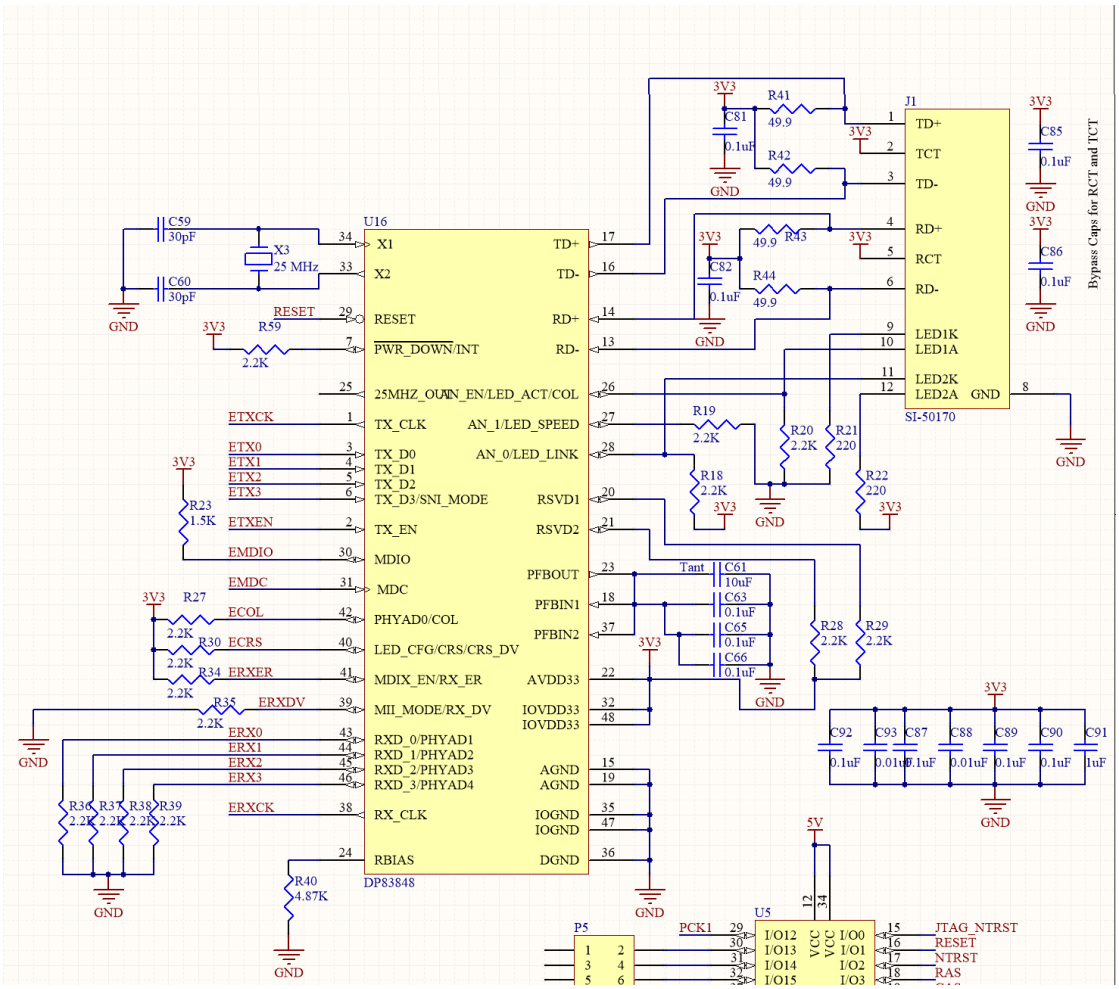
Audio Circuitry



Audio output

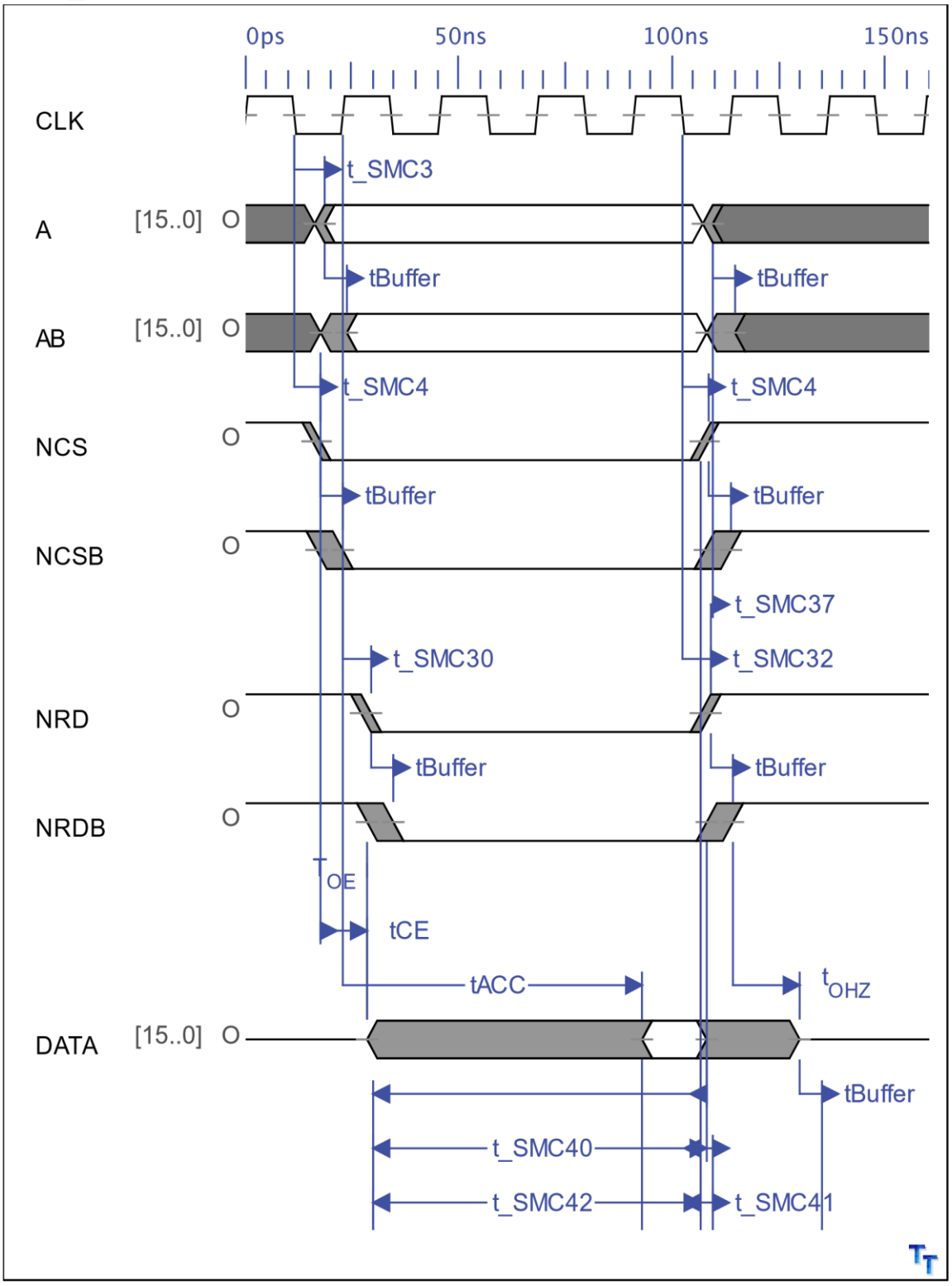
Ethernet

The ethernet circuitry in the schematic is untested, and may not work. It is designed to operate in either 10Base-T or 100Base-T, half or full duplex.


U16
DP83848
J1
SI-50170
U5
P5
Bypass Caps for RCT and TCT
X1
X2
RESET
PWR_DOWN/INT
25MHZ_OUT
TX_CLK
TX_D0
TX_D1
TX_D2
TX_D3/SNI_MODE
TX_EN
MDIO
MDC
PHYAD0/COL
LED_CFG/CRS/CRS_DV
MDIX_EN/RX_ER
MII_MODE/RX_DV
RXD_0/PHYAD1
RXD_1/PHYAD2
RXD_2/PHYAD3
RXD_3/PHYAD4
RX_CLK
RBIAS
LED_EN/LED_ACT/COL
AN_1/LED_SPEED
AN_0/LED_LINK
RSVD1
RSVD2
PFBOUT
PFBIN1
PFBIN2
AVDD33
IOVDD33
IOVDD33
AGND
AGND
IOGND
IOGND
DGND
TD+
TD-
RD+
RD-
TCT
RCT
LED1K
LED1A
LED2K
LED2A
GND
3V3
5V
C59 30pF
C60 30pF
X3 25 MHz
R59 2.2K
R23 1.5K
R27 2.2K
R30 2.2K
R34 2.2K
R35 2.2K
R36 2.2K
R37 2.2K
R38 2.2K
R39 2.2K
R40 4.87K
R41 49.9
R42 49.9
R43 49.9
R44 49.9
R18 2.2K
R19 2.2K
R20 2.2K
R21 220
R22 220
R28 2.2K
R29 2.2K
C81 0.1uF
C82 0.1uF
C85 0.1uF
C86 0.1uF
Tant C61 10uF
C63 0.1uF
C65 0.1uF
C66 0.1uF
C92 0.1uF
C93 0.01uF
C87 0.1uF
C88 0.01uF
C89 0.1uF
C90 0.1uF
C91 1uF
ETXCK
ETX0
ETX1
ETX2
ETX3
ETXEN
EMDIO
EMDC
ECOL
ECRS
ERXER
ERXDV
ERX0
ERX1
ERX2
ERX3
ERXCK
RESET
PCK1
JTAG_NTRST
RESET
NTRST
RAS

Appendix A (ROM Timing)

ROM_READ Page 1



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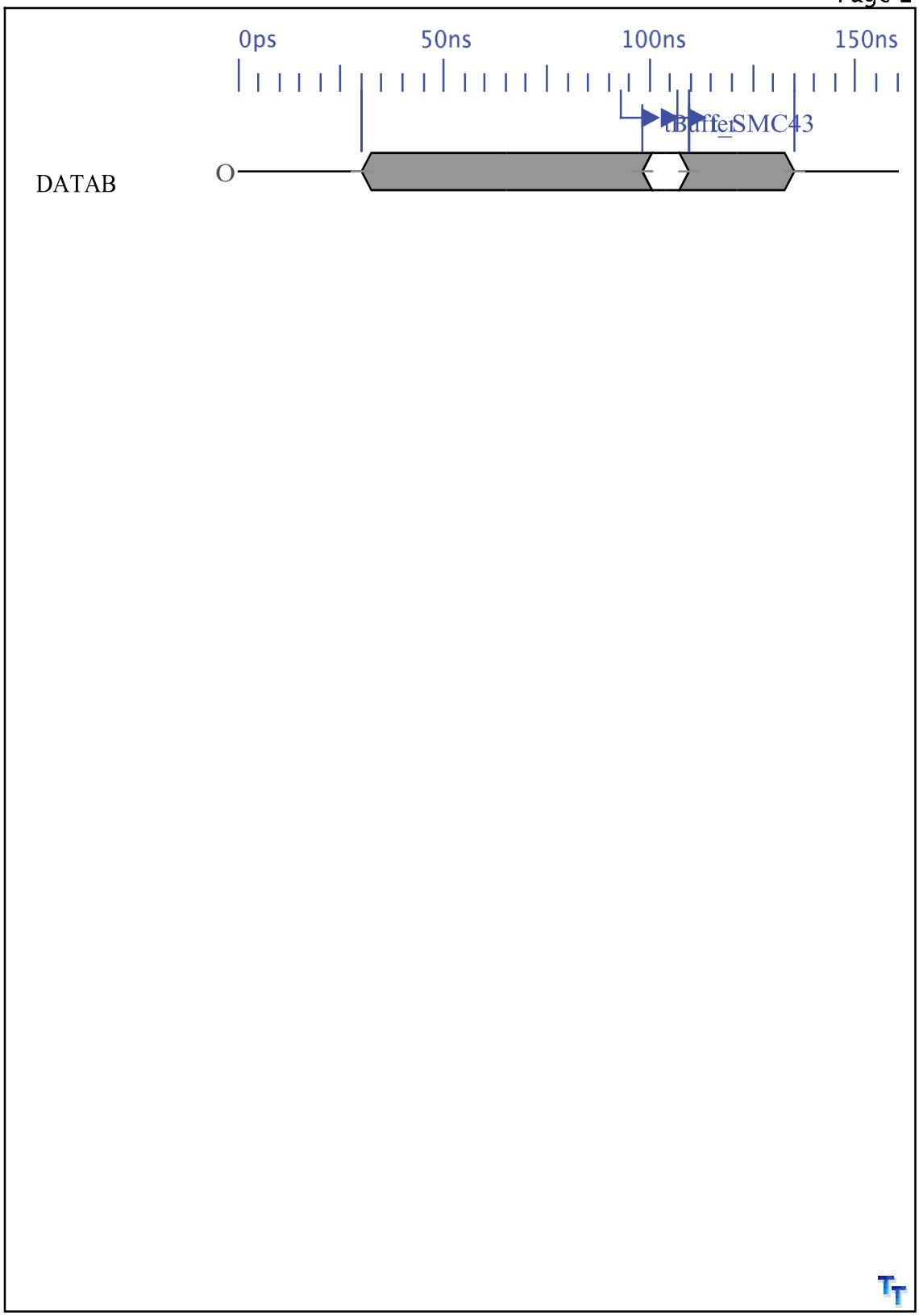

0ps
50ns
100ns
150ns
tBuffer_SMC43
DATAB
O

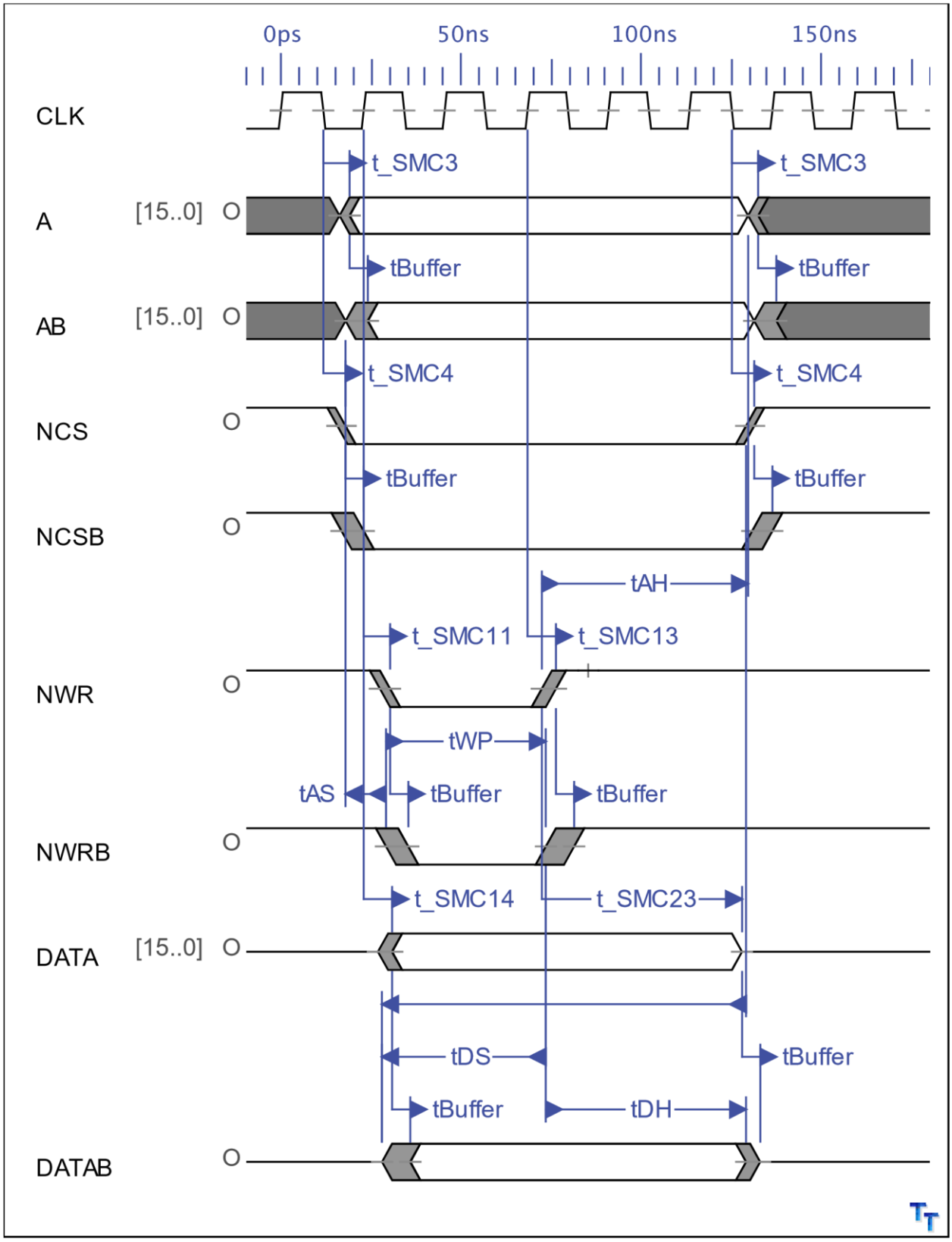
General Data

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
t_SMC3	MCK Falling to A1-A25 valid	to be defined	4.9ns	7.5ns	
t_SMC4	MCK Falling to Chip Select	to be defined	4.3ns	6.5ns	
tBuffer		to be defined	1.3ns	5.1ns	
t_SMC1		to be defined			
t_SMC30	MCK Rising to NRD Active	to be defined	4.7ns	7.0ns	
tACC	Address Access time	defined by memory	0ps	70ns	
tCE	Chip Select Access time	defined by memory	0ns	70ns	
T_{OE}	Output enable access time	defined by memory	0ns	30ns	
t_SMC32		to be defined	4.5ns	6.8ns	
t_SMC40	Data Setup time before NRD	to be defined	7.5ns		
t_SMC4	MCK falling to CHip Select Change	to be defined	4.3ns	6.5ns	
t_SMC41	Data Hold time after NRD rising	to be defined	-3.4ns		
t_SMC37	NRD High to A1-A25 change	to be defined	0.3ns	0.6ns	
t_{OHZ}	Output Enable High to Output in High-Z	defined by memory	0ns	16ns	
t_SMC42	Data Setup before NCS High	to be defined	7.3ns		
t_SMC43	Data Hold after NCS High	to be defined	-3.2ns		

Notes:

Device: AM29LV040

Results:
1 wait states



C:\Users\will\GitReps\EE52\ROM_WRITE.tdml

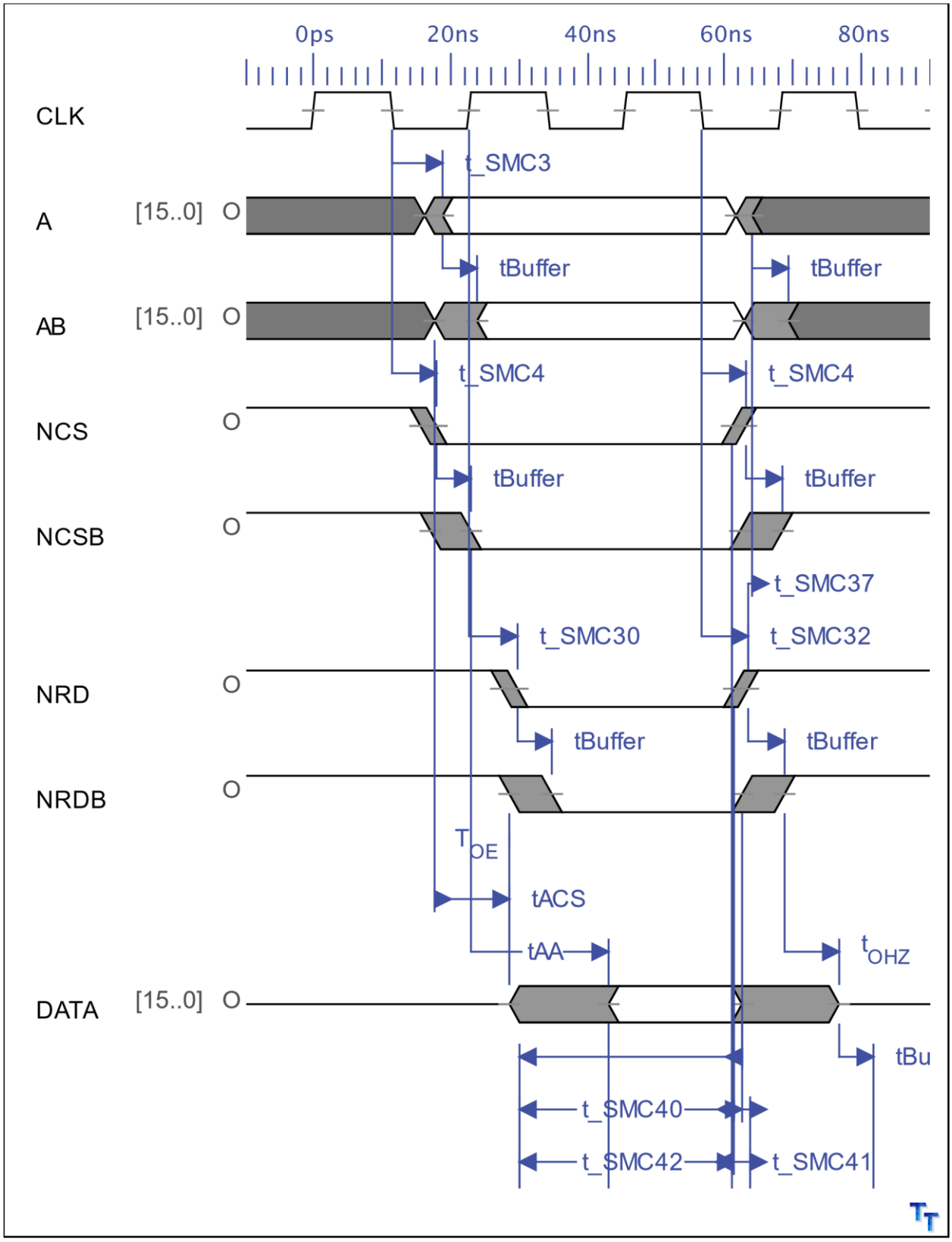
General Data

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
t_SMC3	MCK Falling to A1-A25 valid	to be defined	4.9ns	7.5ns	
tBuffer		to be defined	1.3ns	5.1ns	
t_SMC14	MCK Rising to D0-D15 Valid	to be defined	4.1ns	7.9ns	
t_SMC4	MCK falling to CHip Select Change	to be defined	4.3ns	6.5ns	
tAS	Address Setup to End of Write	to be defined	0ns		
tDS	Data Setup Time	to be defined	35ns		
tDH	Data Hold Time	to be defined	0ns		
tAH	Address Hold from End of Write	to be defined	45ns		
tWP	Write Pulse	to be defined	35ns		
t_SMC11	MCK Rising to NWR Active (with wait states)	to be defined	4.8ns	7.2ns	
t_SMC13	MCK Rising to NWR Inactive	to be defined	4.1ns	7.9ns	
t_SMC23	MCK Rising to Data Out Invalid (1 hold state)	to be defined	55.7ns		
t_SMC17	NWR High to A1-A25 Change	to be defined	3.3ns		

Notes:

Results:
0 setup
2 wait state (pulse length)
2.5 hold parameter

Appendix B (SRAM Timing)



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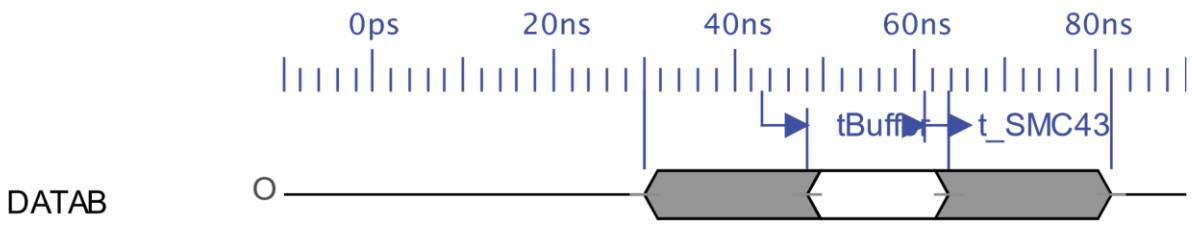
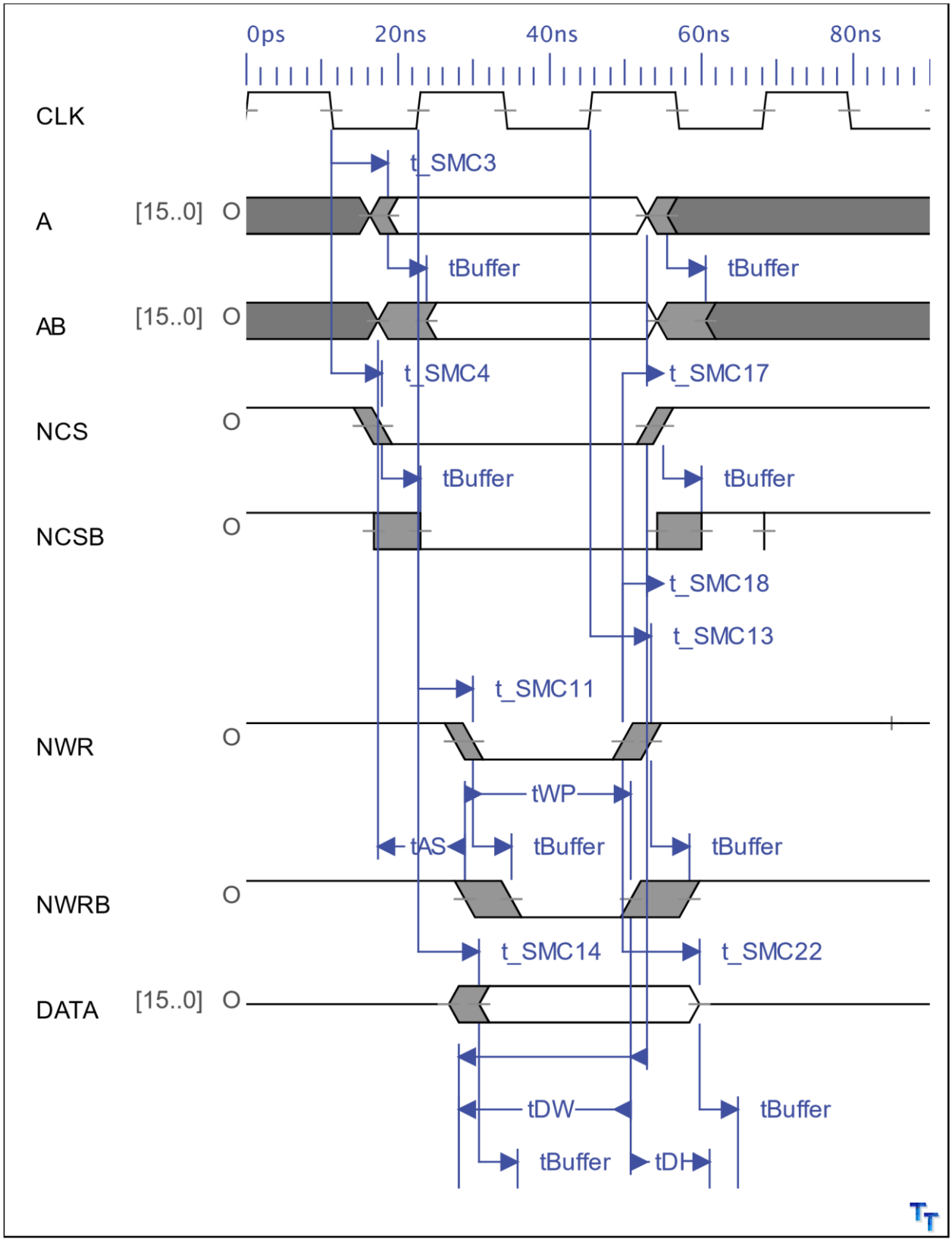

0ps
20ns
40ns
60ns
80ns
t_SMC43
DATAB
O

General Data

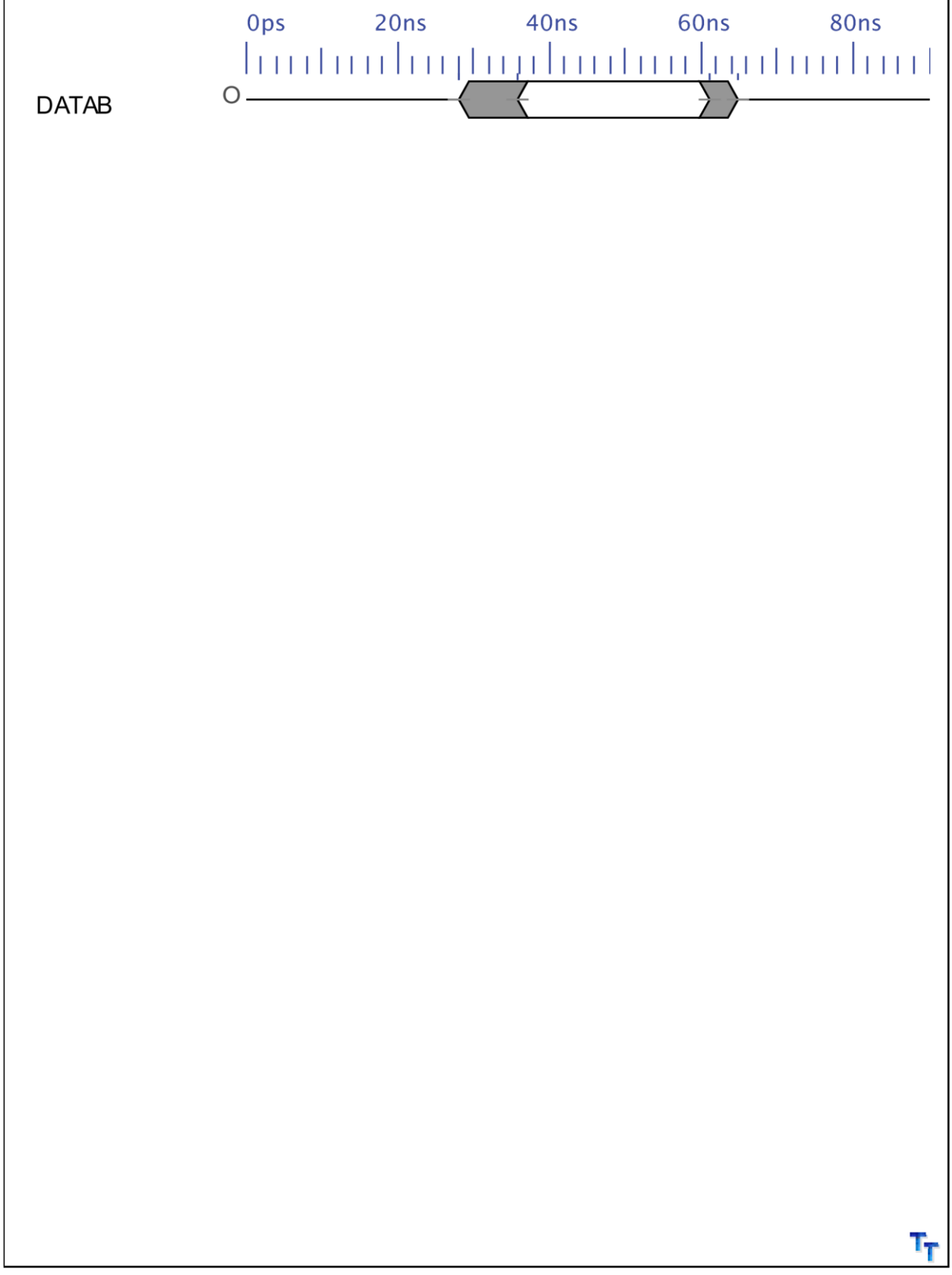
SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
t_SMC3	MCK Falling to A1-A25 valid	to be defined	4.9ns	7.5ns	
t_SMC4	MCK Falling to Chip Select	to be defined	4.3ns	6.5ns	
tBuffer		to be defined	1.3ns	5.1ns	
t_SMC1		to be defined			
t_SMC30	MCK Rising to NRD Active	to be defined	4.7ns	7.0ns	
tAA	Address Access time	defined by memory	0ps	20ns	
tACS	Chip Select Access time	defined by memory	0ns	20ns	
T_{OE}	Output enable access time	defined by memory	0ns	8ns	
t_SMC32	MCK falling to NRD inactive	to be defined	4.5ns	6.8ns	
t_SMC40	Data Setup time before NRD	to be defined	7.5ns		
t_SMC4	MCK falling to CHip Select Change	to be defined	4.3ns	6.5ns	
t_SMC41	Data Hold time after NRD rising	to be defined	-3.4ns		
t_SMC37	NRD High to A1-A25 change	to be defined	0.3ns	0.6ns	
t_{OHZ}	Output Enable High to Output in High-Z	to be defined	0ns	8ns	
t_SMC42	Data Setup before NCS High	to be defined	7.3ns		
t_SMC43	Data Hold after NCS High	to be defined	-3.2ns		

Notes:

Results:
1 wait states



C:\Users\will\GitReps\EE52\SRAM_WRITE.tdml


0ps
20ns
40ns
60ns
80ns
DATAB
0

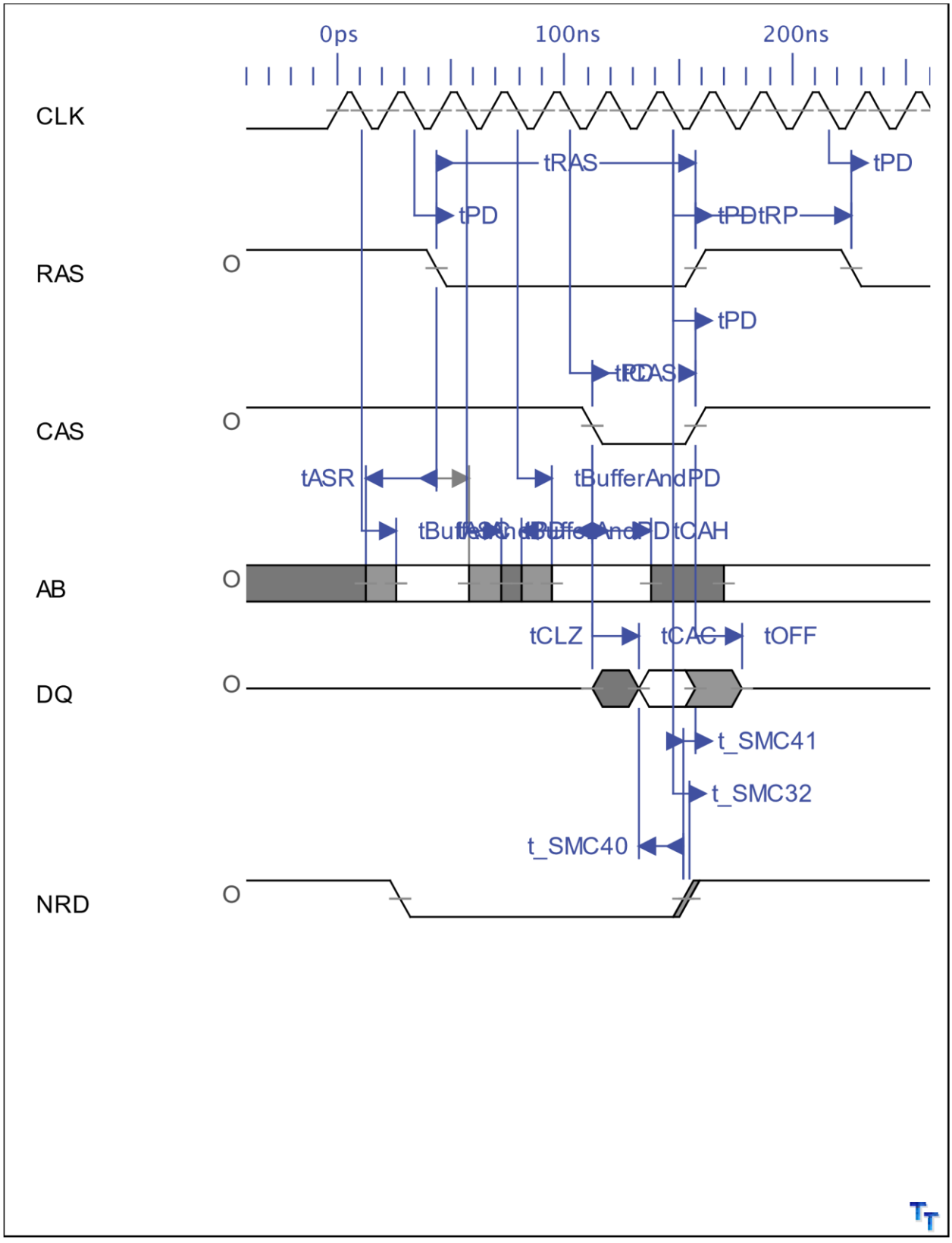
General Data

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
t_SMC3	MCK Falling to A1-A25 valid	to be defined	4.9ns	7.5ns	
tBuffer		to be defined	1.3ns	5.1ns	
t_SMC14	MCK Rising to D0-D15 Valid	to be defined	4.1ns	7.9ns	
t_SMC4	MCK falling to CHip Select Change	to be defined	4.3ns	6.5ns	
tAS	Address Setup to End of Write	to be defined	0ns		
tDW	Data Setup Time	to be defined	9ns		
tDH	Data Hold Time	to be defined	0ns		
tWR	Address Hold from End of Write	to be defined	0ns		
tWP	Write Pulse	to be defined	12ns		
t_SMC11	MCK Rising to NWR Active (with wait states)	to be defined	4.8ns	7.2ns	
t_SMC13	MCK Rising to NWR Inactive	to be defined	4.1ns	7.9ns	
t_SMC22	MCK Rising to Data Out Invalid	to be defined	10.2ns		
t_SMC17	NWR High to A1-A25 Change	to be defined	3.3ns		
t_SMC18	NWR High to Chip Select Inactive	to be defined	3.3ns		

Notes:

Results:
0 setup
1 wait state (pulse length)
0 hold parameter

Appendix C (DRAM Timing)



C:\Users\will\GitReps\EE52\DRAMREAD.tdml

General Data

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
tASR	Row-address setup time before RAS low	to be defined	0ns		
tASC	Column-address setup time before CAS low	to be defined	0ns		
tDS	Data setup time	to be defined	0ns		
tRCS	Read setup time before CAS low	to be defined			
tCWL	W low setup time before CAS	to be defined	20ns		
tRWL	W low setup time before RAS	to be defined			
tWCS	W low setup time before CAS	to be defined	0ns		
tWSR	W high setup time (CAS-before-RAS refresh only)	to be defined	10ns		
tCAH	Column-address hold time after CAS low	to be defined	15ns		
tDHR	Data hold time after RAS low	to be defined	60ns		
tDH	Data hold time	to be defined	15ns		
tAR	Column-address hold time after RAS low	to be defined	60ns		
tRAH	Row-address hold time after RAS low	to be defined	10ns		
tRCH	Read hold time after CAS high	to be defined	0ns		
tRRH	Read hold time after RAS high	to be defined	0ns		
tWCH	Write hold time after CAS low	to be defined	15ns		

tWCR	Write hold time after RAS low	to be defined	60ns		
tWHR	W high hold time (CAS-before-RAS refresh only)	to be defined	10ns		
tCHR	Delay time, RAS low to CAS high	to be defined	20ns		

General Data continued...

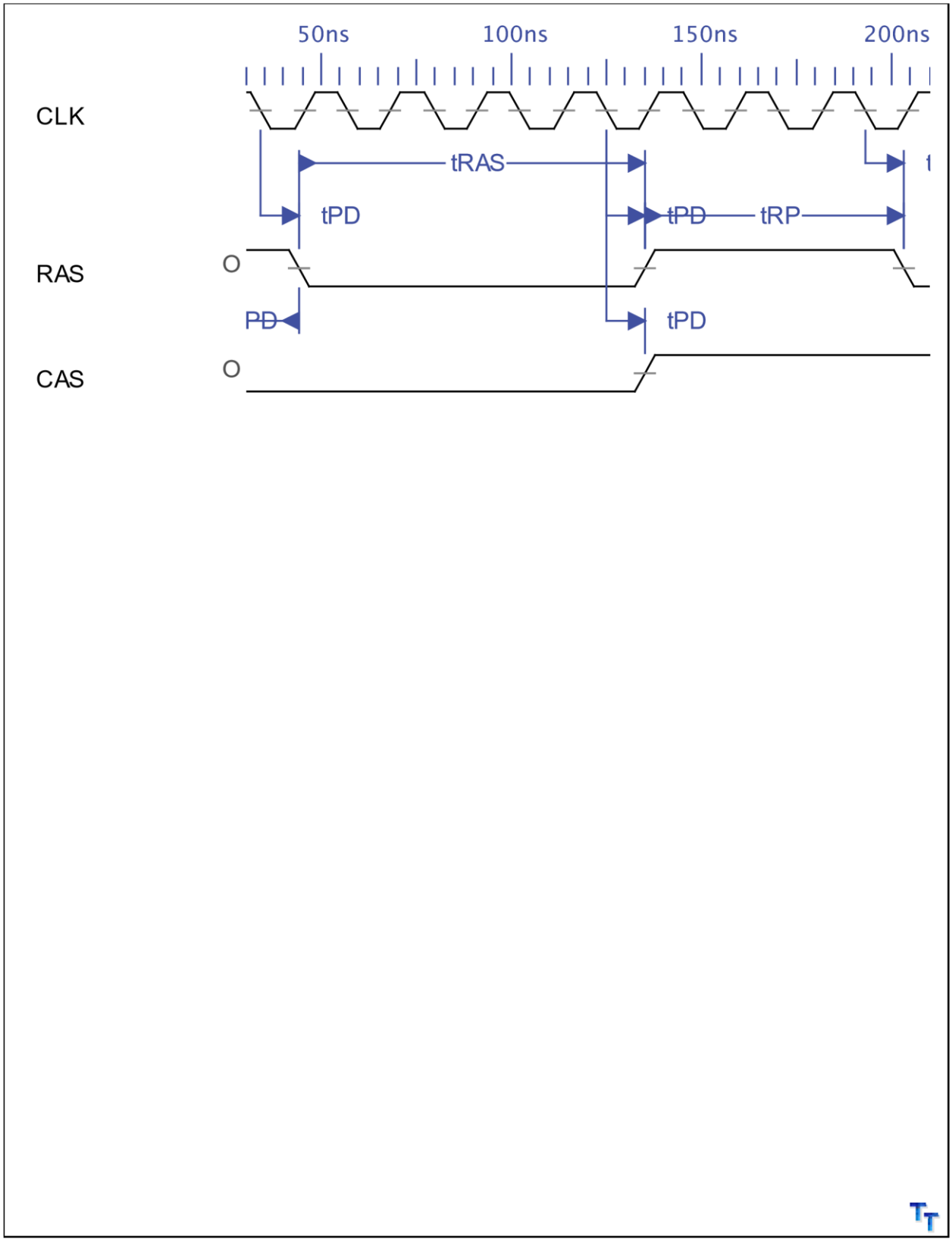
SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
tCRP	Delay time, CAS high to RAS low	to be defined	0ns		
tCSH	Delay time, RAS low to CAS high	to be defined	80ns		
tCSR	Delay time, CAS low to RAS low	to be defined	10ns		
tRAD	Delay time, RAS low to column-address	to be defined	15ns	40ns	
tRAL	Delay time, column-address to RAS high	to be defined	40ns		
tCAL	Delay time, column-address to CAS high	to be defined	40ns		
tRCD	Delay time, RAS low to CAS low	to be defined	20ns	60ns	
tRPC	Delay time, RAS high to CAS low	to be defined	0ns		
tRSH	Delay time, CAS low to RAS high	to be defined	20ns		
tT	Transition time	to be defined	2ns	50ns	
tRAS	Non-page-mode pulse duration, RAS low	to be defined	80ns	10000ns	
tCAS	Pulse duration, CAS low	to be defined	20ns	10000ns	
tCLZ	CAS to output in low Z	to be defined	0ns		

tOFF	output disable time after CAS high	to be defined	0ns	20ns	
tBufferAndPD	Buffer propagation delays	to be defined	1.3ns	15.1ns	
tPD	CPLD worst case path	to be defined		10ns	
tCAC	Access time from CAS low	to be defined		20ns	
tRAC	Access time from RAS low	to be defined		80ns	
tRP	Pulse duration, RAS high	to be defined	60ns		

General Data continued...

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
t_SMC40	Data Setup time before NRD	to be defined	7.5ns		
t_SMC41	Data Hold time after NRD rising	to be defined	-3.4ns		

t_SMC32	MCK falling to NRD inactive	to be defined	4.5ns	6.8ns



C:\Users\will\GitReps\EE52\DRAMREFRESH.tdml

General Data

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
tASR	Row-address setup time before RAS low	to be defined	0ns		
tASC	Column-address setup time before CAS low	to be defined	0ns		
tDS	Data setup time	to be defined	0ns		
tRCS	Read setup time before CAS low	to be defined			
tCWL	W low setup time before CAS	to be defined	20ns		
tRWL	W low setup time before RAS	to be defined			
tWCS	W low setup time before CAS	to be defined	0ns		
tWSR	W high setup time (CAS-before-RAS refresh only)	to be defined	10ns		
tCAH	Column-address hold time after CAS low	to be defined	15ns		
tDHR	Data hold time after RAS low	to be defined	60ns		
tDH	Data hold time	to be defined	15ns		
tAR	Column-address hold time after RAS low	to be defined	60ns		
tRAH	Row-address hold time after RAS low	to be defined	10ns		
tRCH	Read hold time after CAS high	to be defined	0ns		
tRRH	Read hold time after RAS high	to be defined	0ns		
tWCH	Write hold time after CAS low	to be defined	15ns		

tWCR	Write hold time after RAS low	to be defined	60ns		
tWHR	W high hold time (CAS-before-RAS refresh only)	to be defined	10ns		
tCHR	Delay time, RAS low to CAS high	to be defined	20ns		

General Data continued...

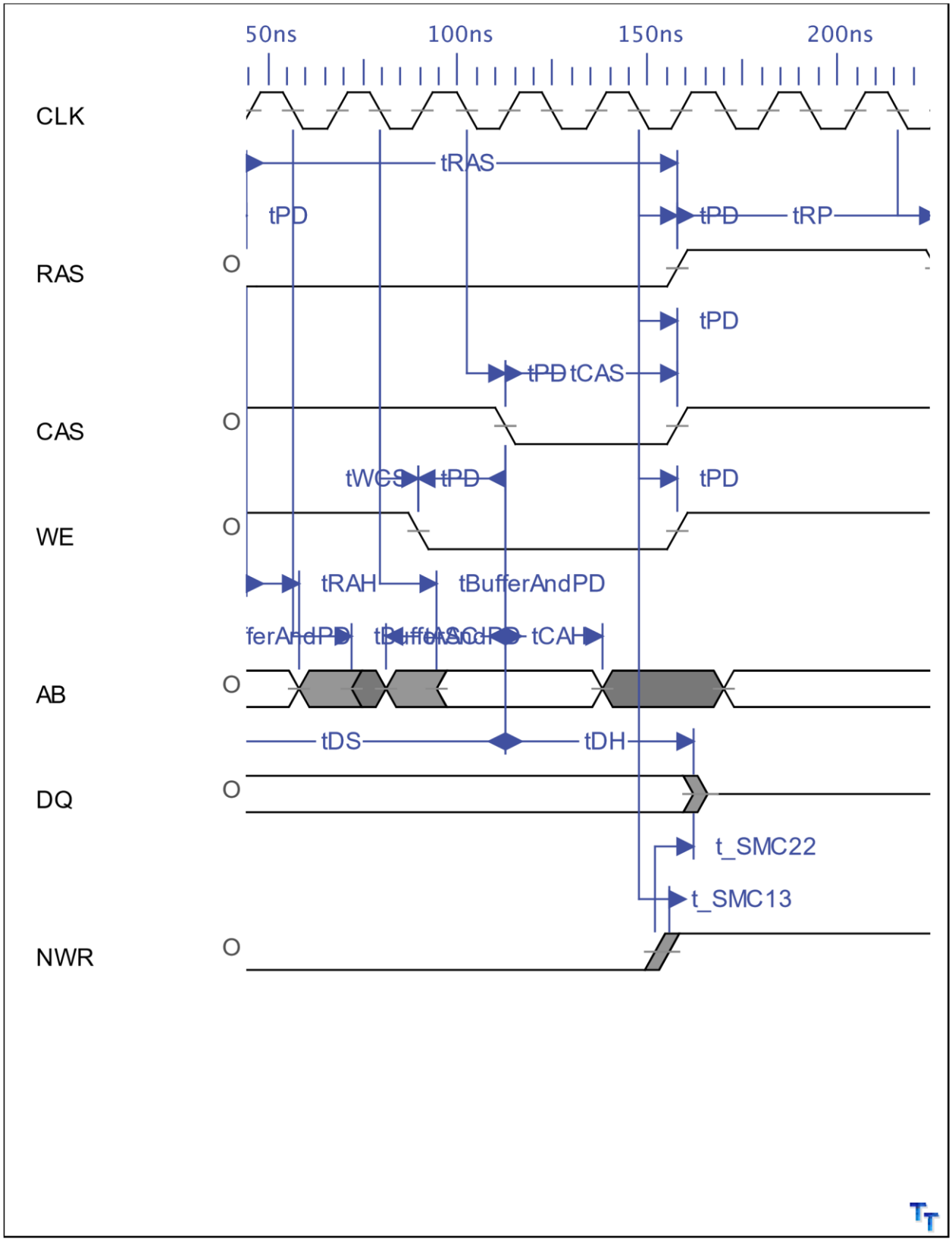
SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
tCRP	Delay time, CAS high to RAS low	to be defined	0ns		
tCSH	Delay time, RAS low to CAS high	to be defined	80ns		
tCSR	Delay time, CAS low to RAS low	to be defined	10ns		
tRAD	Delay time, RAS low to column-address	to be defined	15ns	40ns	
tRAL	Delay time, column-address to RAS high	to be defined	40ns		
tCAL	Delay time, column-address to CAS high	to be defined	40ns		
tRCD	Delay time, RAS low to CAS low	to be defined	20ns	60ns	
tRPC	Delay time, RAS high to CAS low	to be defined	0ns		
tRSH	Delay time, CAS low to RAS high	to be defined	20ns		
tT	Transition time	to be defined	2ns	50ns	
tRAS	Non-page-mode pulse duration, RAS low	to be defined	80ns	10000ns	
tCAS	Pulse duration, CAS low	to be defined	20ns	10000ns	
tCLZ	CAS to output in low Z	to be defined	0ns		

tOFF	output disable time after CAS high	to be defined	0ns	20ns	
tBufferAndPD	Buffer propagation delays	to be defined	1.3ns	15.1ns	
tPD	CPLD worst case path	to be defined		10ns	
tCAC	Access time from CAS low	to be defined		20ns	
tRAC	Access time from RAS low	to be defined		80ns	
tRP	Pulse duration, RAS high	to be defined	60ns		

General Data continued...

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES

tCP	Pulse duration, CAS high	to be defined	10ns



C:\Users\will\GitReps\EE52\DRAMWRITE.tdml

General Data

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
tASR	Row-address setup time before RAS low	to be defined	0ns		
tASC	Column-address setup time before CAS low	to be defined	0ns		
tDS	Data setup time	to be defined	0ns		
tRCS	Read setup time before CAS low	to be defined			
tCWL	W low setup time before CAS	to be defined	20ns		
tRWL	W low setup time before RAS	to be defined			
tWCS	W low setup time before CAS	to be defined	0ns		
tWSR	W high setup time (CAS-before-RAS refresh only)	to be defined	10ns		
tCAH	Column-address hold time after CAS low	to be defined	15ns		
tDHR	Data hold time after RAS low	to be defined	60ns		
tDH	Data hold time	to be defined	15ns		
tAR	Column-address hold time after RAS low	to be defined	60ns		
tRAH	Row-address hold time after RAS low	to be defined	10ns		
tRCH	Read hold time after CAS high	to be defined	0ns		
tRRH	Read hold time after RAS high	to be defined	0ns		
tWCH	Write hold time after CAS low	to be defined	15ns		

tWCR	Write hold time after RAS low	to be defined	60ns		
tWHR	W high hold time (CAS-before-RAS refresh only)	to be defined	10ns		
tCHR	Delay time, RAS low to CAS high	to be defined	20ns		

General Data continued...

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
tCRP	Delay time, CAS high to RAS low	to be defined	0ns		
tCSH	Delay time, RAS low to CAS high	to be defined	80ns		
tCSR	Delay time, CAS low to RAS low	to be defined	10ns		
tRAD	Delay time, RAS low to column-address	to be defined	15ns	40ns	
tRAL	Delay time, column-address to RAS high	to be defined	40ns		
tCAL	Delay time, column-address to CAS high	to be defined	40ns		
tRCD	Delay time, RAS low to CAS low	to be defined	20ns	60ns	
tRPC	Delay time, RAS high to CAS low	to be defined	0ns		
tRSH	Delay time, CAS low to RAS high	to be defined	20ns		
tT	Transition time	to be defined	2ns	50ns	
tRAS	Non-page-mode pulse duration, RAS low	to be defined	80ns	10000ns	
tCAS	Pulse duration, CAS low	to be defined	20ns	10000ns	
tCLZ	CAS to output in low Z	to be defined	0ns		

tOFF	output disable time after CAS high	to be defined	0ns	20ns	
tBufferAndPD	Buffer propagation delays	to be defined	1.3ns	15.1ns	
tPD	CPLD worst case path	to be defined		10ns	
tCAC	Access time from CAS low	to be defined		20ns	
tRAC	Access time from RAS low	to be defined		80ns	
tRP	Pulse duration, RAS high	to be defined	60ns		

General Data continued...

SYMBOL	DEFINITION	DESCRIPTION	MIN	MAX	NOTES
tBuffer		to be defined	1.3ns	5.1ns	
t_SMC13	MCK Falling to NWR inactive	to be defined	4.1ns	7.9ns	

t_SMC22	MCK Rising to Data out invalid	to be defined	10.2ns

Appendix D (DRAM Abel Code)

Appendix E (Software)

Appendix F (Printed Circuit Board)

Appendix G (Schematics)