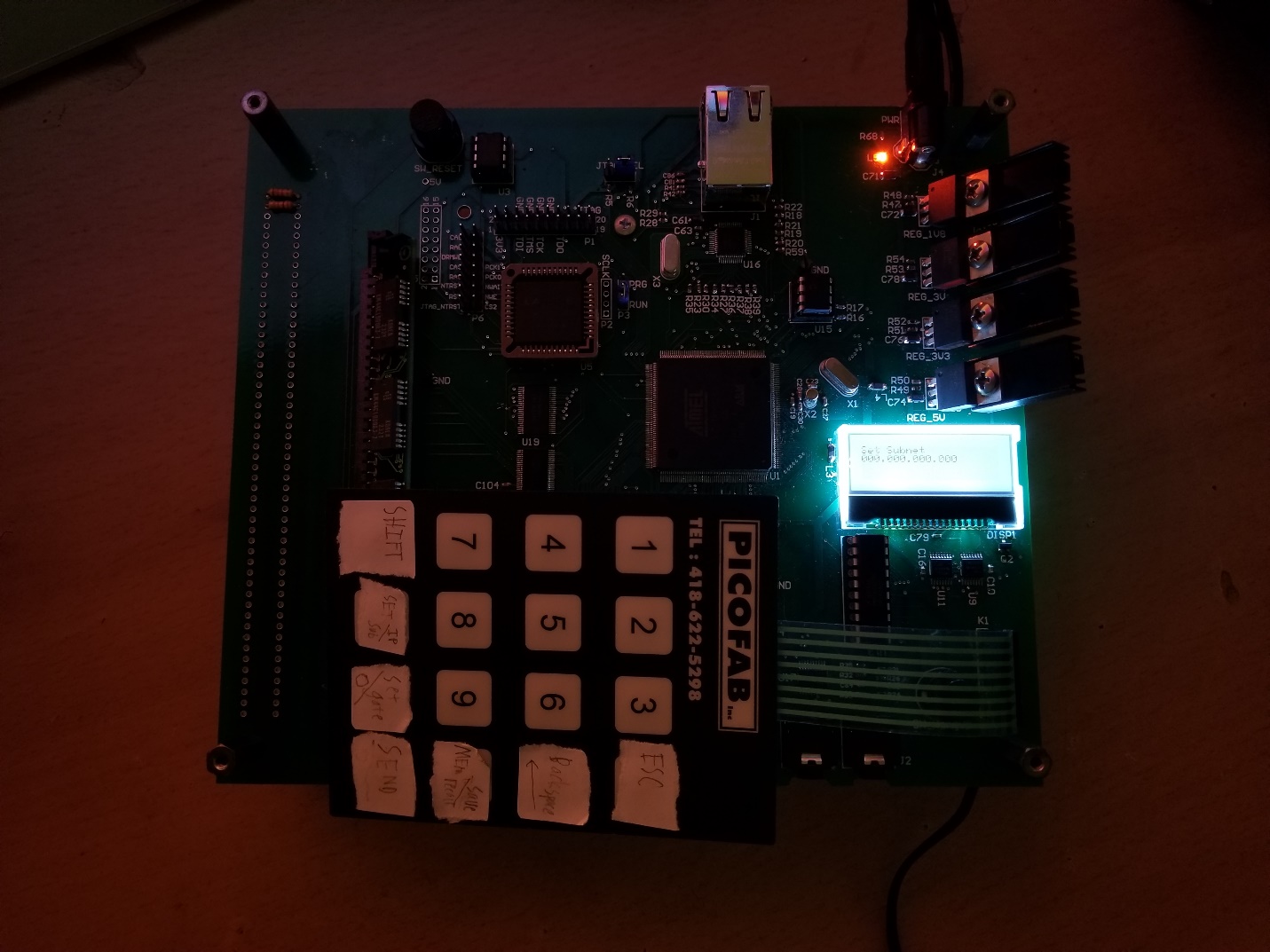
VoIP phone Technical Documentation



The EE52 VoIP phone is a phone that can communicate with other EE52 VoIP phones. The user controls the phone by using a 128x32 display and a 4x4 keypad. There is a headphone and microphone jack that a headset can be plugged into, and there is a button for putting the phone “on-the-hook” to hangup the call.

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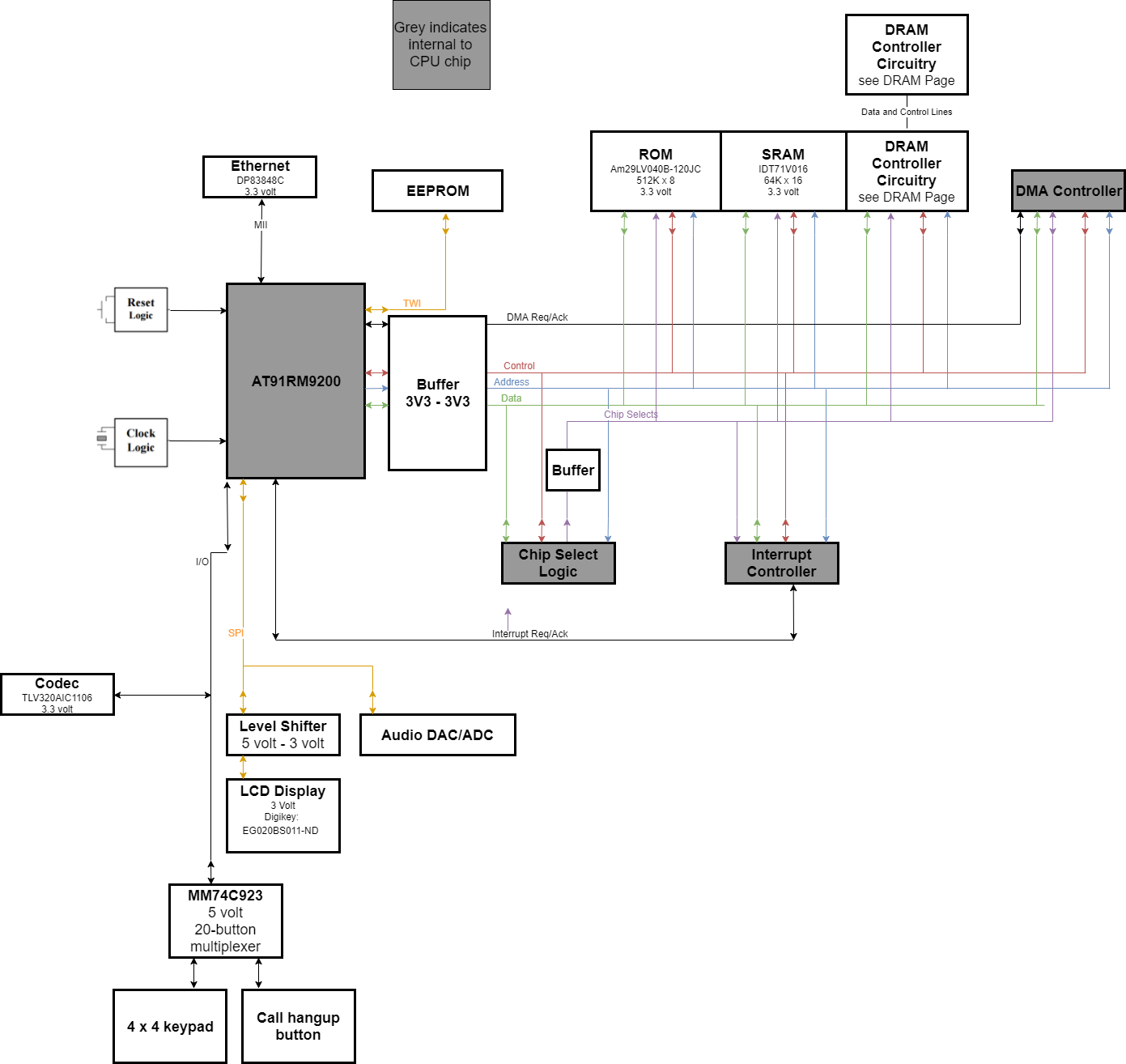
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# Overview

|  |  |
| --- | --- |
| Processor | Atmel AT91RM9200 |
| Input power | 8V-12V DC 5.5mm barrel jack |
| Display | 128x32 |
| Headphone Jack | 3.5mm mono audio jack |
| Microphone Jack | 3.5mm |
| Keypad | 4x4 button keypad |

## Block Diagram



# Power Circuitry

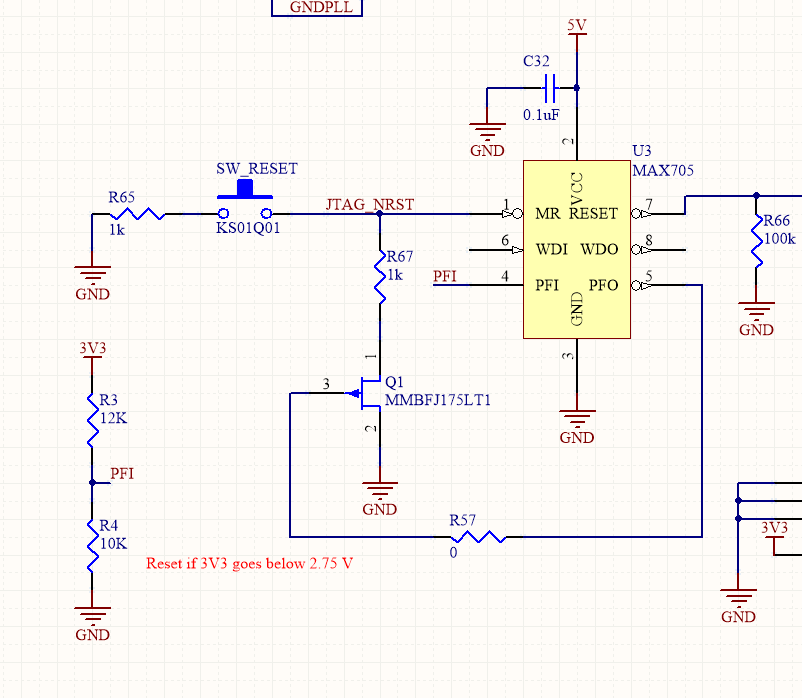
The system takes ~8V-12V DC input. The upper bound is due to thermal dissipation constraints of the linear regulator heatsinks. There are four power rails on this board.

|  |  |
| --- | --- |
| Rail | Uses |
| 5V | Reset circuit, DRAM, CPLD |
| 3V3 | Audio, SRAM, ROM, CPU |
| 3V | Display |
| 1V8 | CPU Core logic |

# CPU Support Circuitry

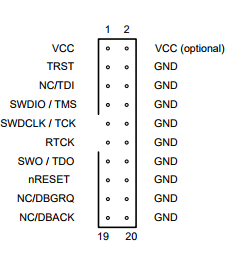
## Reset

The reset circuitry uses a MAX705 chip in the standard configuration.



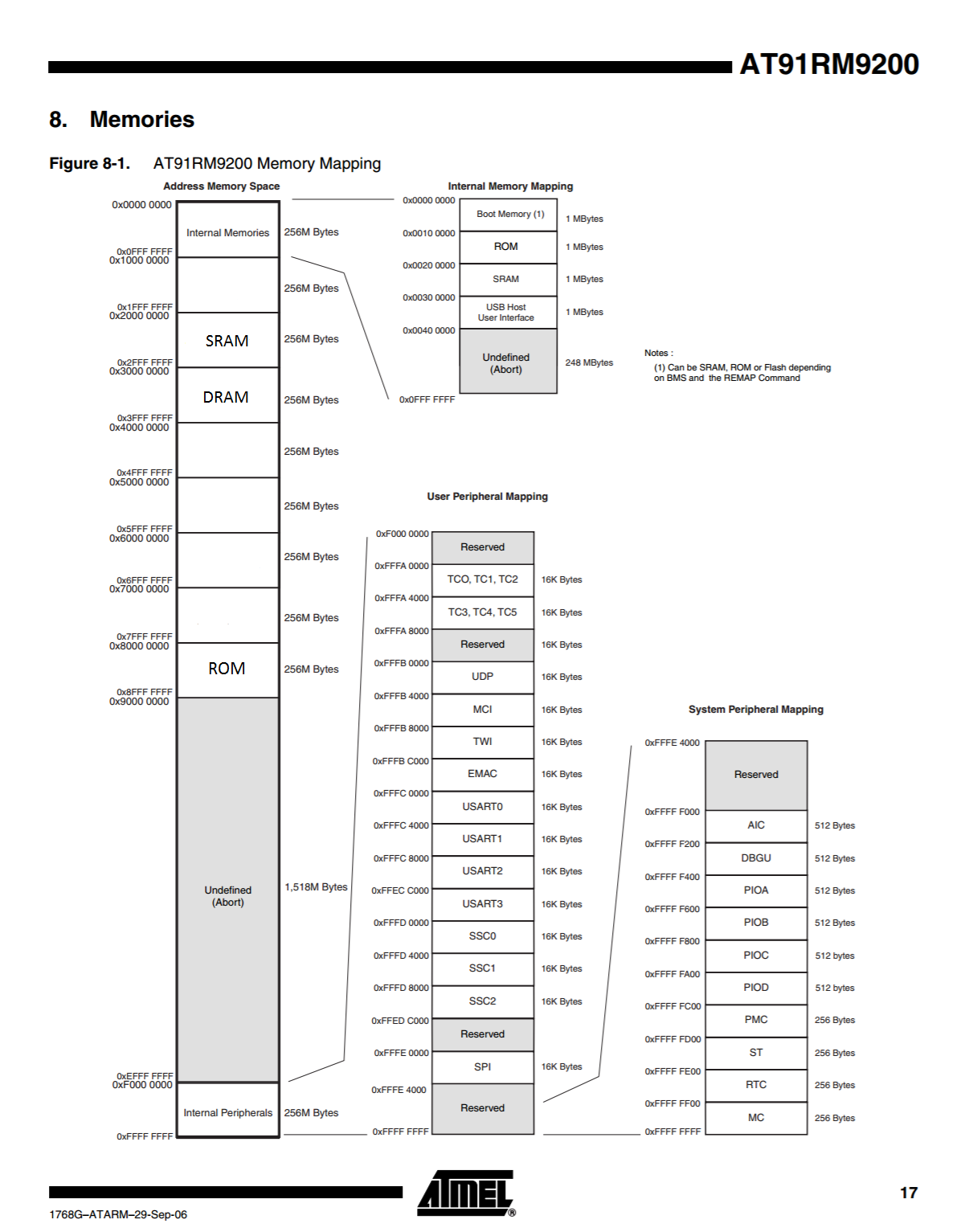
## JTAG

This board has a JTAG interface routed and populated for the purposes of debugging. It is a 20-pin legacy ARM IDC 0.1” pitch JTAG connector with the following pinout (see <http://infocenter.arm.com/help/topic/com.arm.doc.faqs/attached/13634/cortex_debug_connectors.pdf>):



# Memory

All memory access is done through 74LVT16245 buffers.



*Memory map*

## ROM

This board uses a 29LV040 chip for ROM. This chip has an address bus width of 19 bits, and a data bus width of 8 bits. It is on chip select 7. See schematic in Appendix.

## SRAM

This board uses a IDT71V016 chip for SRAM. This chip has an address bus width of 16 bits, and a data bus width of 16 bits. It is on chip select 1. See schematic in Appendix.

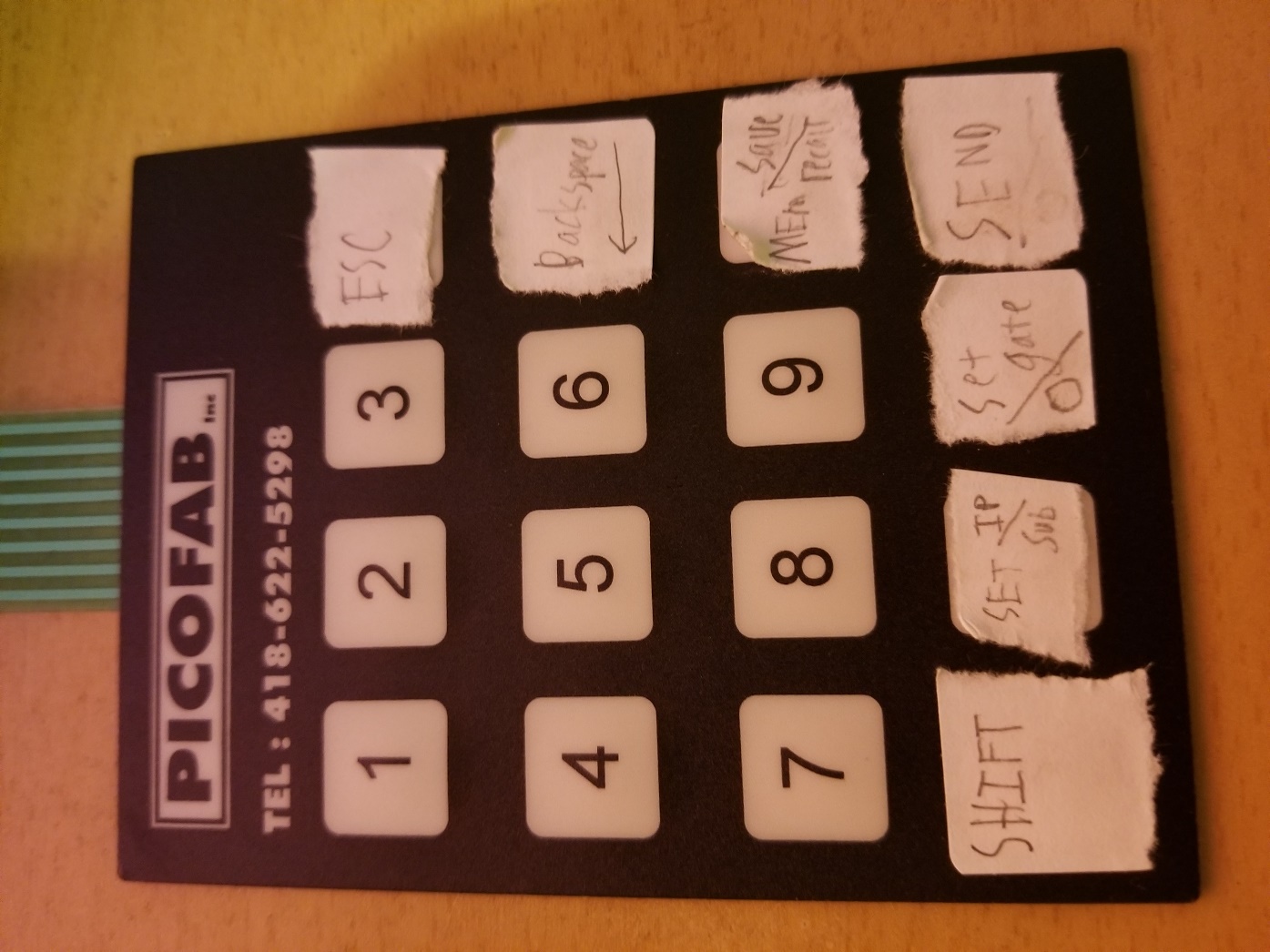
## DRAM

This board uses a socket mount DRAM module. The DRAM controller is implemented in a CPLD. The address lines are multiplexed to the DRAM via U19 and U21, which are two buffers that can be toggle high-Z and enabled by the CPLD DRAM controller. The data lines are connected to the CPU data bus via a bidirectional buffer that is enabled when the DRAM chip select goes low. The directionality of the buffer is set by the NRD signal.

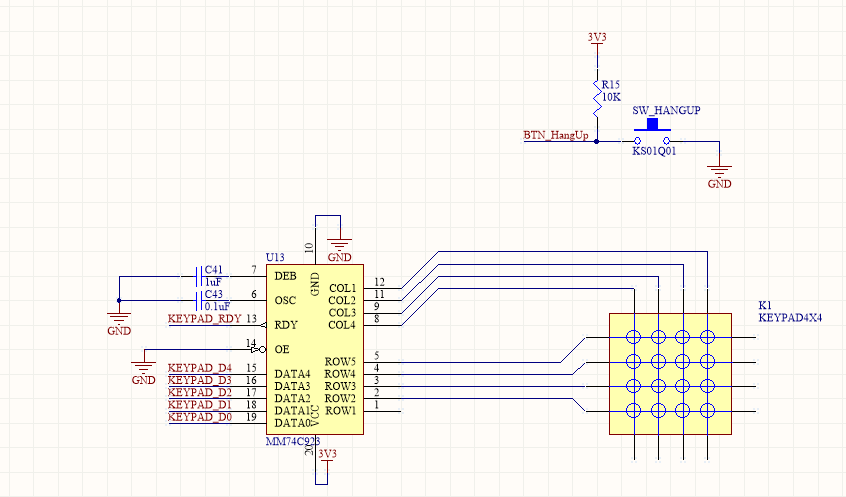
The DRAM has an effective address bus width of 20 bits, and a data bus width of 8 bits. The DRAM is on chip select 2. See Schematic in Appendix.

# User Interface Components

## Keypad



The keypad is used for user input into the device. It is a 4x4 keypad, and since more inputs are needed than are available, a shift key is used to toggle the function of a key.



The above schematic shows the design as routed on the PCB. This design is fully functional

## Display



The display is a 128x32 display, divided into 4 rows. Only the top two rows are used.

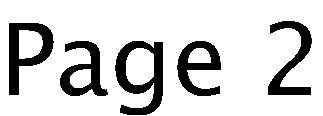
The top row displays the current menu the system is in, or the status of the system if a call is in progress.

The 2nd row displays auxiliary information for a menu, such as the IP address being set, the subnet mask, or the memory location for recall.

## Audio

## Ethernet

# Appendix A (ROM Timing)



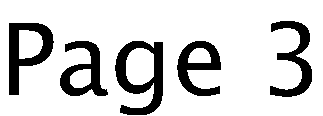
DATAB

O

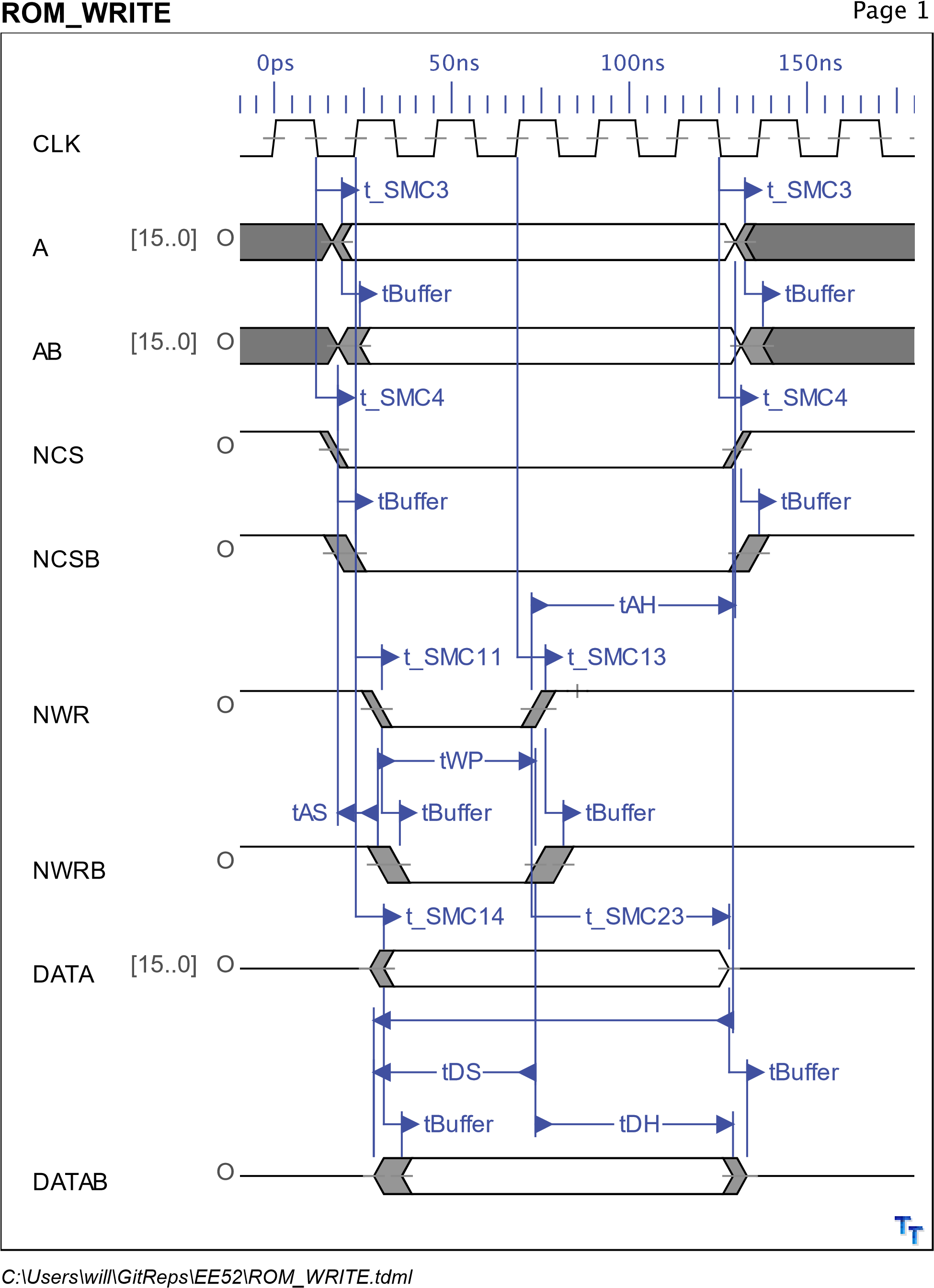
tBuffer

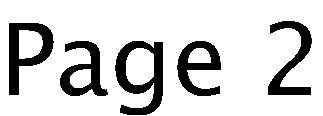
t\_SMC43





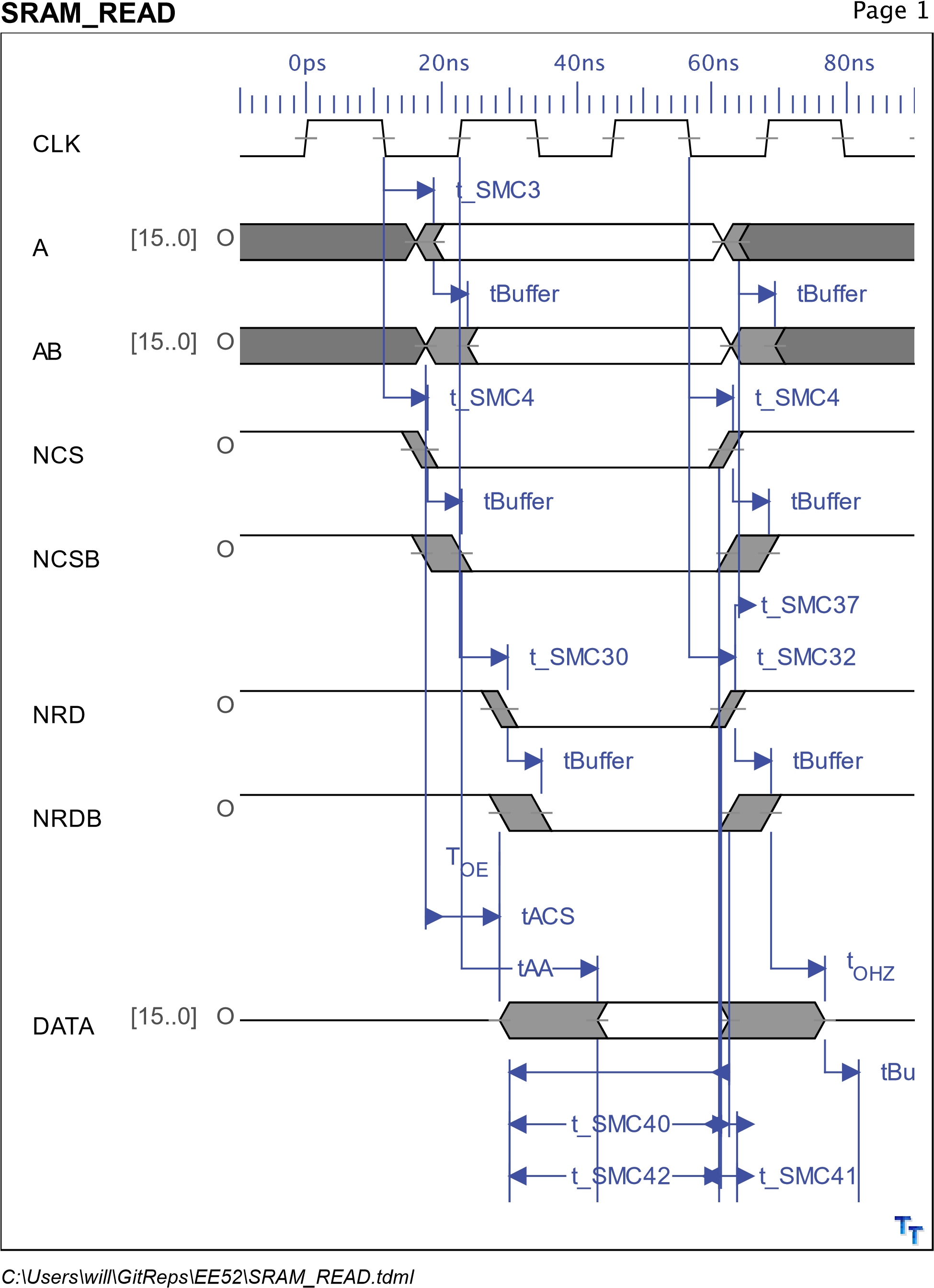
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| General Data |  |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| t\_SMC3 | MCK Falling to  A1-A25 valid | to be defined | 4.9ns | 7.5ns |  |
| t\_SMC4 | MCK Falling to | to be defined | 4.3ns | 6.5ns |  |
|  | Chip Select |  |  |  |  |
| tBuffer |  | to be defined | 1.3ns | 5.1ns |  |
| t\_SMC1 |  | to be defined |  |  |  |
| t\_SMC30 | MCK Rising to  NRD Active | to be defined | 4.7ns | 7.0ns |  |
| tACC | Address Access | defined by | 0ps | 70ns |  |
|  | time | memory |  |  |  |
| tCE | Chip Select  Access time | defined by  memory | 0ns | 70ns |  |
| T | Output enable | defined by | 0ns | 30ns |  |
| OE | access time | memory |  |  |  |
| t\_SMC32 |  | to be defined | 4.5ns | 6.8ns |  |
| t\_SMC40 | Data Setup time | to be defined | 7.5ns |  |  |
|  | before NRD |  |  |  |  |
| t\_SMC4 | MCK falling to  CHip Select  Change | to be defined | 4.3ns | 6.5ns |  |
| t\_SMC41 | Data Hold time | to be defined | -3.4ns |  |  |
|  | after NRD rising |  |  |  |  |
| t\_SMC37 | NRD High to  A1-A25 change | to be defined | 0.3ns | 0.6ns |  |
| t | Output Enable | defined by | 0ns | 16ns |  |
| OHZ | High to Output in  High-Z | memory |  |  |  |
| t\_SMC42 | Data Setup before NCS High | to be defined | 7.3ns |  |  |
| t\_SMC43 | Data Hold after | to be defined | -3.2ns |  |  |
|  | NCS High |  |  |  |  |
| Notes:  Device: AM29LV040  Results:  1 wait states | |  |  |  |  |
|

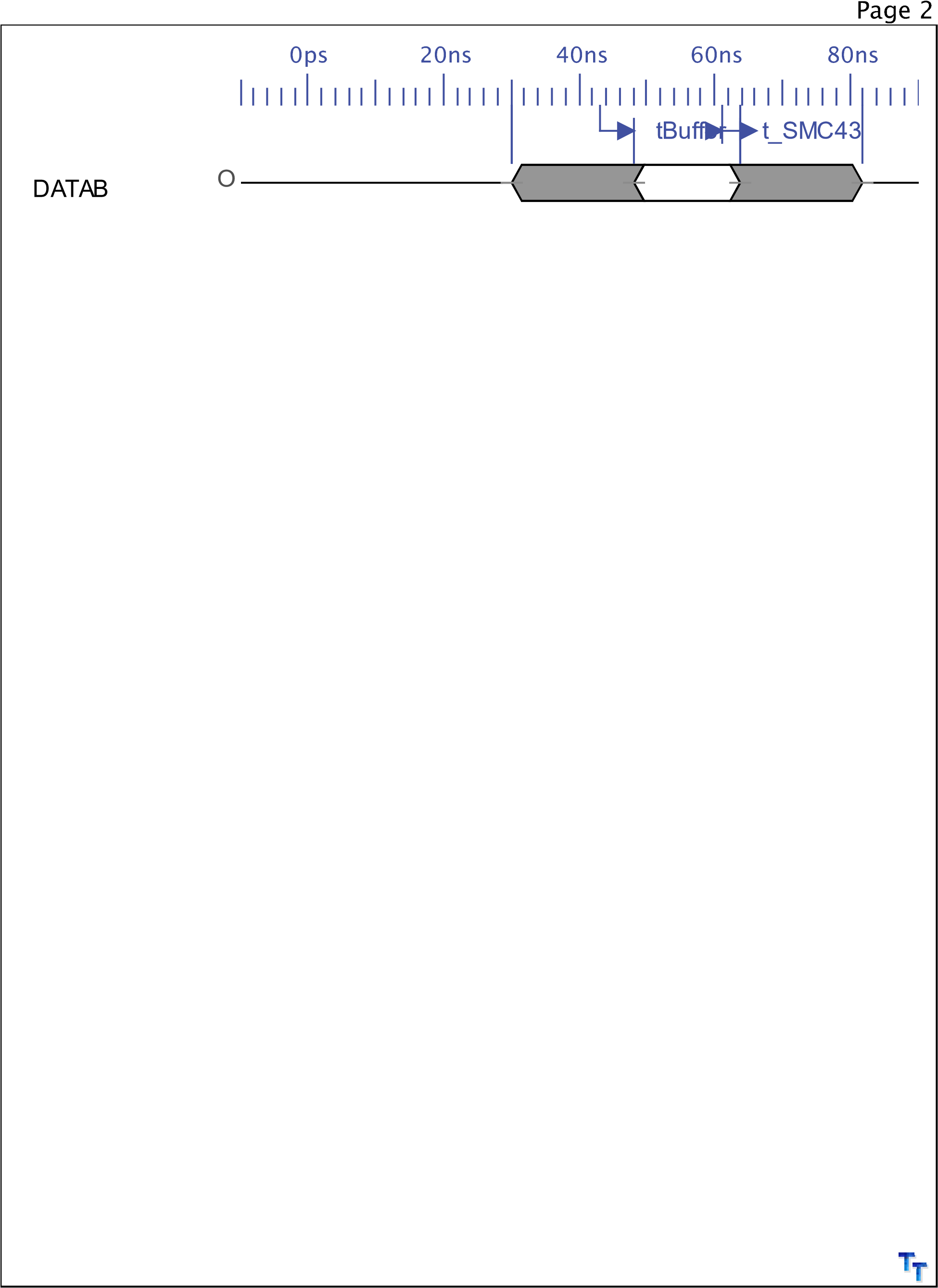


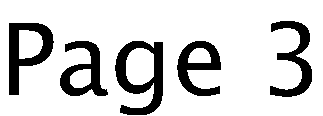


|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| General Data |  |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| t\_SMC3 | MCK Falling to  A1-A25 valid | to be defined | 4.9ns | 7.5ns |  |
| tBuffer |  | to be defined | 1.3ns | 5.1ns |  |
| t\_SMC14 | MCK Rising to  D0-D15 Valid | to be defined | 4.1ns | 7.9ns |  |
| t\_SMC4 | MCK falling to | to be defined | 4.3ns | 6.5ns |  |
|  | CHip Select  Change |  |  |  |  |
| tAS | Address Setup to End of Write | to be defined | 0ns |  |  |
| tDS | Data Setup Time | to be defined | 35ns |  |  |
| tDH | Data Hold Time | to be defined | 0ns |  |  |
| tAH | Address Hold | to be defined | 45ns |  |  |
|  | from End of Write |  |  |  |  |
| tWP | Write Pulse | to be defined | 35ns |  |  |
| t\_SMC11 | MCK Rising to | to be defined | 4.8ns | 7.2ns |  |
|  | NWR Active (with wait states) |  |  |  |  |
| t\_SMC13 | MCK Rising to  NWR Inactive | to be defined | 4.1ns | 7.9ns |  |
| t\_SMC23 | MCK Rising to | to be defined | 55.7ns |  |  |
|  | Data Out Invalid  (1 hold state) |  |  |  |  |
| t\_SMC17 | NWR High to  A1-A25 Change | to be defined | 3.3ns |  |  |
| Notes:  Results:  0 setup   1. wait state (pulse length)   2.5 hold parameter | |  |  |  |  |
|

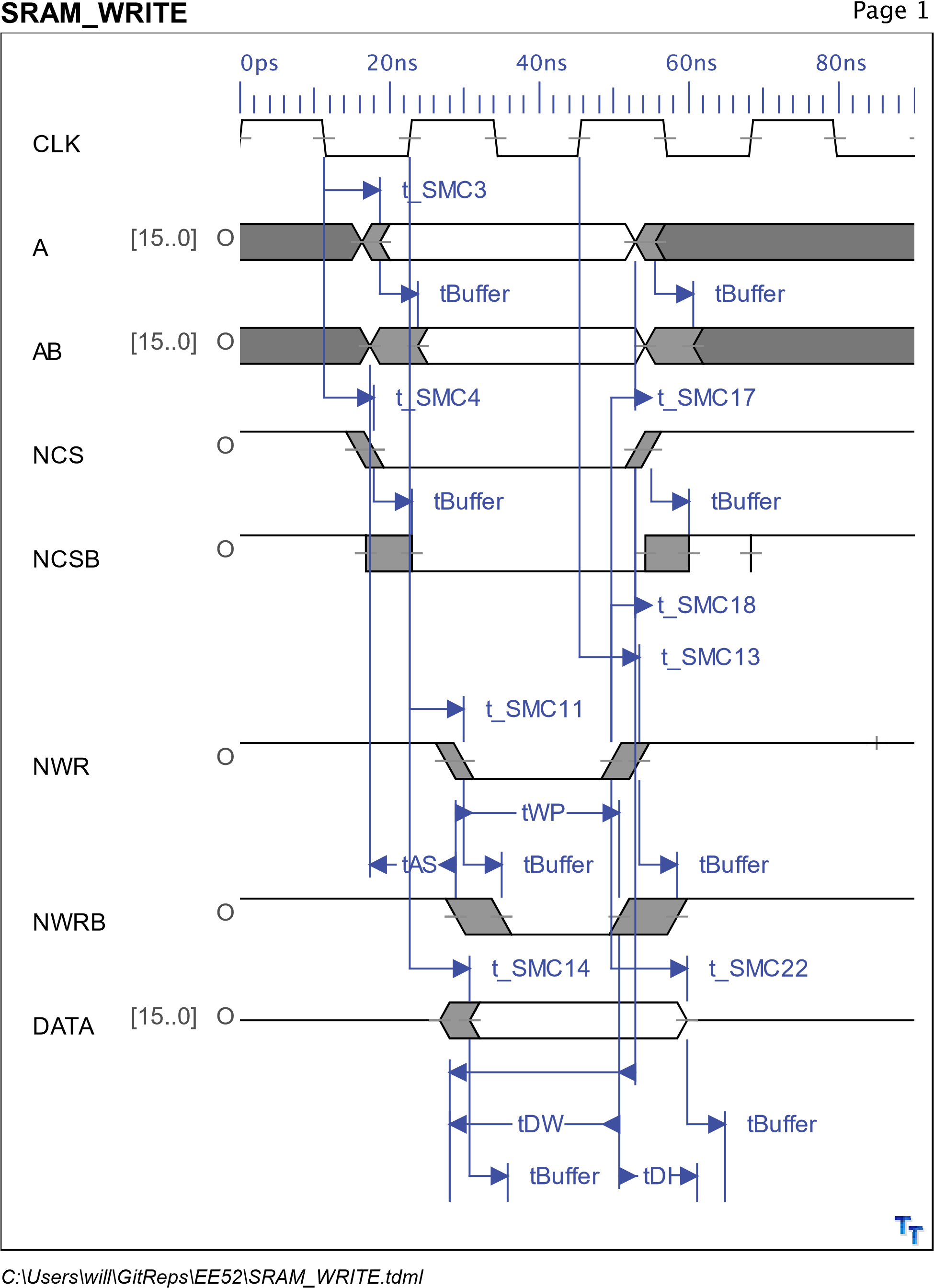
Appendix B (SRAM Timing)

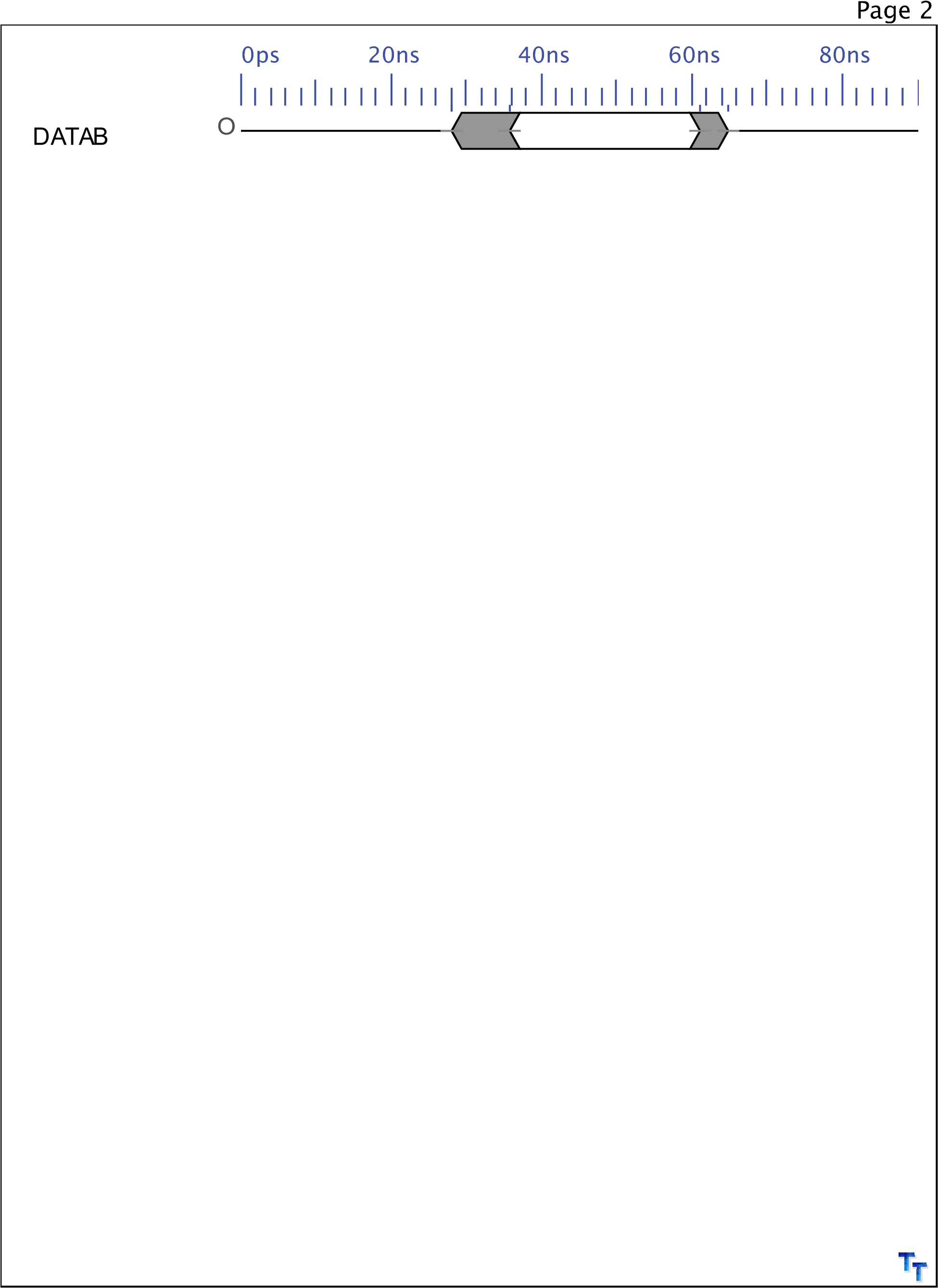


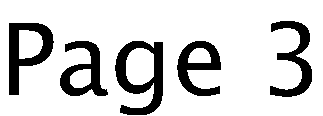




|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| General Data |  |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| t\_SMC3 | MCK Falling to  A1-A25 valid | to be defined | 4.9ns | 7.5ns |  |
| t\_SMC4 | MCK Falling to | to be defined | 4.3ns | 6.5ns |  |
|  | Chip Select |  |  |  |  |
| tBuffer |  | to be defined | 1.3ns | 5.1ns |  |
| t\_SMC1 |  | to be defined |  |  |  |
| t\_SMC30 | MCK Rising to  NRD Active | to be defined | 4.7ns | 7.0ns |  |
| tAA | Address Access | defined by | 0ps | 20ns |  |
|  | time | memory |  |  |  |
| tACS | Chip Select  Access time | defined by  memory | 0ns | 20ns |  |
| T | Output enable | defined by | 0ns | 8ns |  |
| OE | access time | memory |  |  |  |
| t\_SMC32 | MCK falling to  NRD inactive | to be defined | 4.5ns | 6.8ns |  |
| t\_SMC40 | Data Setup time | to be defined | 7.5ns |  |  |
|  | before NRD |  |  |  |  |
| t\_SMC4 | MCK falling to  CHip Select  Change | to be defined | 4.3ns | 6.5ns |  |
| t\_SMC41 | Data Hold time | to be defined | -3.4ns |  |  |
|  | after NRD rising |  |  |  |  |
| t\_SMC37 | NRD High to  A1-A25 change | to be defined | 0.3ns | 0.6ns |  |
| t | Output Enable | to be defined | 0ns | 8ns |  |
| OHZ | High to Output in  High-Z |  |  |  |  |
| t\_SMC42 | Data Setup before NCS High | to be defined | 7.3ns |  |  |
| t\_SMC43 | Data Hold after | to be defined | -3.2ns |  |  |
|  | NCS High |  |  |  |  |
| Notes:  Results:  1 wait states |  |  |  |  |  |
|

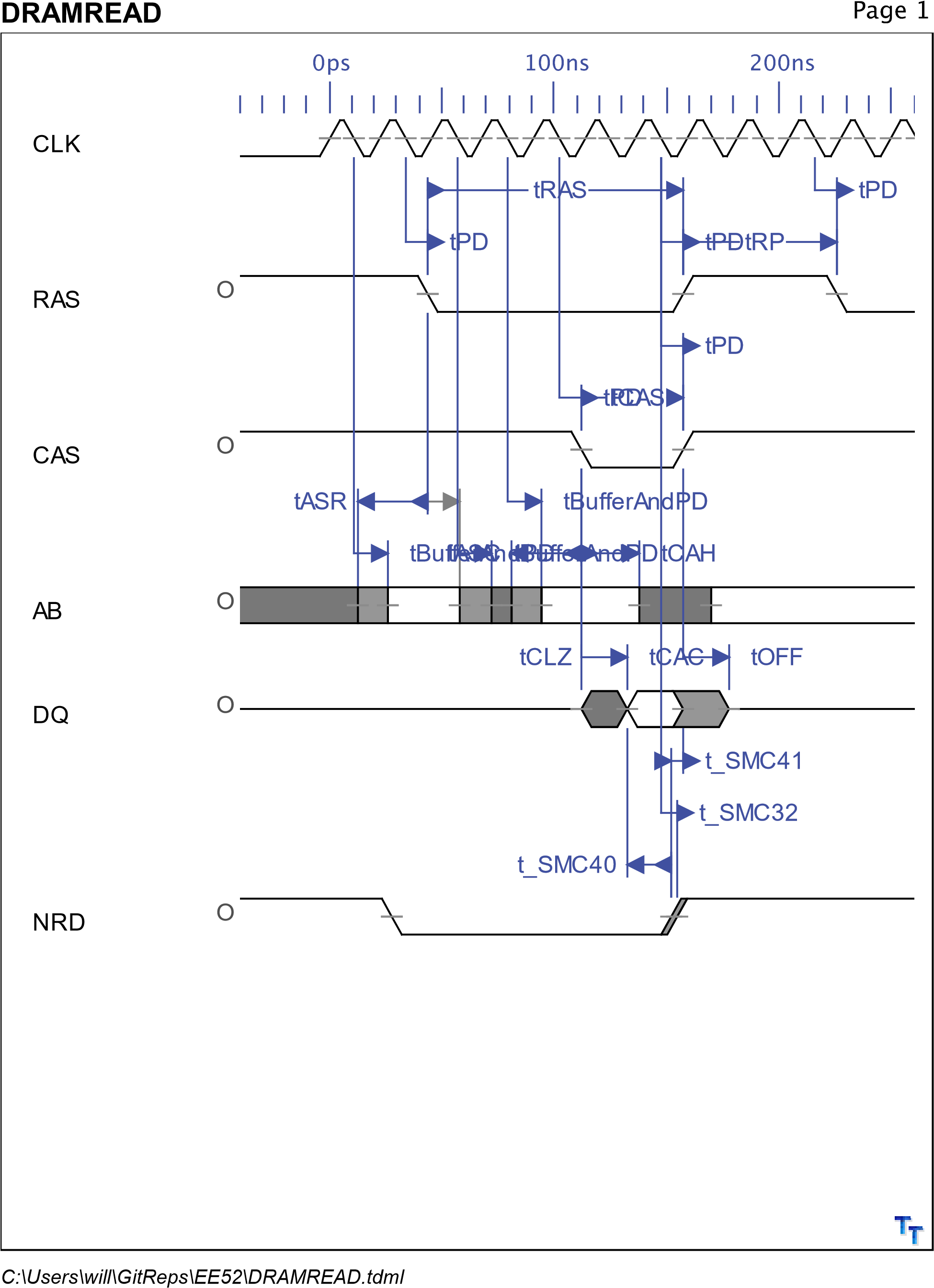


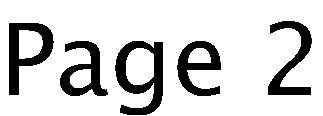




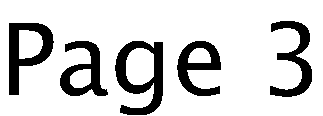
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| General Data |  |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| t\_SMC3 | MCK Falling to  A1-A25 valid | to be defined | 4.9ns | 7.5ns |  |
| tBuffer |  | to be defined | 1.3ns | 5.1ns |  |
| t\_SMC14 | MCK Rising to  D0-D15 Valid | to be defined | 4.1ns | 7.9ns |  |
| t\_SMC4 | MCK falling to | to be defined | 4.3ns | 6.5ns |  |
|  | CHip Select  Change |  |  |  |  |
| tAS | Address Setup to End of Write | to be defined | 0ns |  |  |
| tDW | Data Setup Time | to be defined | 9ns |  |  |
| tDH | Data Hold Time | to be defined | 0ns |  |  |
| tWR | Address Hold | to be defined | 0ns |  |  |
|  | from End of Write |  |  |  |  |
| tWP | Write Pulse | to be defined | 12ns |  |  |
| t\_SMC11 | MCK Rising to | to be defined | 4.8ns | 7.2ns |  |
|  | NWR Active (with wait states) |  |  |  |  |
| t\_SMC13 | MCK Rising to  NWR Inactive | to be defined | 4.1ns | 7.9ns |  |
| t\_SMC22 | MCK Rising to | to be defined | 10.2ns |  |  |
|  | Data Out Invalid |  |  |  |  |
| t\_SMC17 | NWR High to  A1-A25 Change | to be defined | 3.3ns |  |  |
| t\_SMC18 | NWR High to | to be defined | 3.3ns |  |  |
|  | Chip Select  Inactive |  |  |  |  |
| Notes:  Results:   1. setup 2. wait state (pulse length)   0 hold parameter | |  |  |  |  |
|

# Appendix C (DRAM Timing)

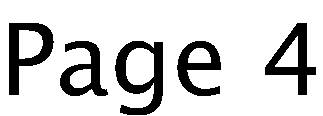




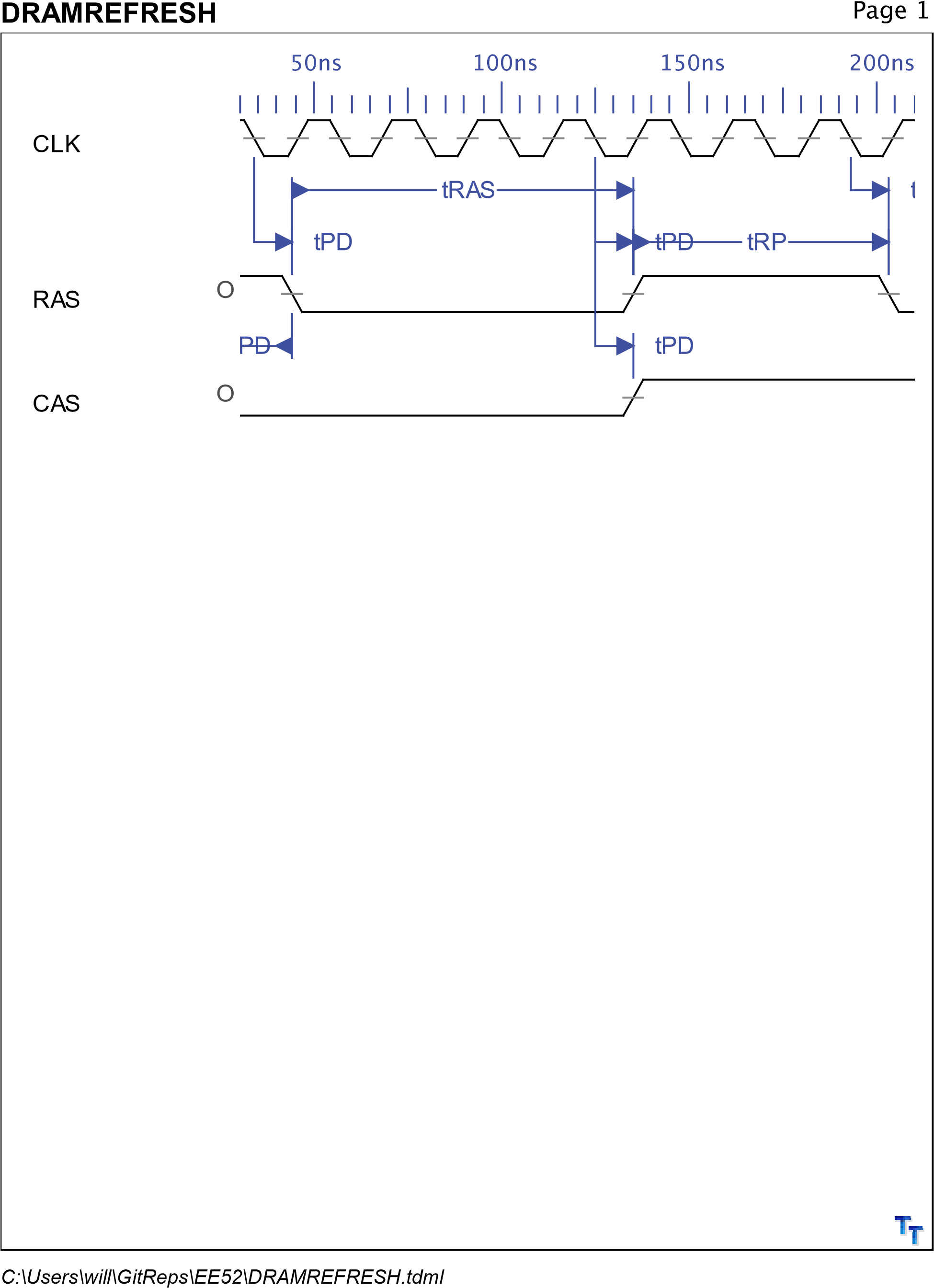
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| General Data |  |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| tASR | Row-address setup time before RAS low | to be defined | 0ns |  |  |
| tASC | Column-address | to be defined | 0ns |  |  |
|  | setup time before CAS low |  |  |  |  |
| tDS | Data setup time | to be defined | 0ns |  |  |
| tRCS | Read setup time | to be defined |  |  |  |
|  | before CAS low |  |  |  |  |
| tCWL | W low setup time before CAS | to be defined | 20ns |  |  |
| tRWL | W low setup | to be defined |  |  |  |
|  | time before RAS |  |  |  |  |
| tWCS | W low setup time before CAS | to be defined | 0ns |  |  |
| tWSR | W high setup | to be defined | 10ns |  |  |
|  | time  (CAS-before-RAS refresh only) |  |  |  |  |
| tCAH | Column-address hold time after  CAS low | to be defined | 15ns |  |  |
| tDHR | Data hold time | to be defined | 60ns |  |  |
|  | after RAS low |  |  |  |  |
| tDH | Data hold time | to be defined | 15ns |  |  |
| tAR | Column-address | to be defined | 60ns |  |  |
|  | hold time after  RAS low |  |  |  |  |
| tRAH | Row-address  hold time after  RAS low | to be defined | 10ns |  |  |
| tRCH | Read hold time | to be defined | 0ns |  |  |
|  | after CAS high |  |  |  |  |
| tRRH | Read hold time after RAS high | to be defined | 0ns |  |  |
| tWCH | Write hold time | to be defined | 15ns |  |  |
|  | after CAS low |  |  |  |  |
| tWCR | Write hold time after RAS low | to be defined | 60ns |  |  |
| tWHR | W high hold time | to be defined | 10ns |  |  |
|  | (CAS-before-RAS refresh only) |  |  |  |  |
| tCHR | Delay time, RAS low to CAS high | to be defined | 20ns |  |  |
|

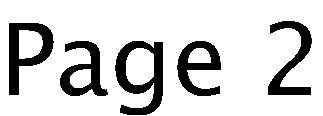


|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| General Data continued... | |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| tCRP | Delay time, CAS high to RAS low | to be defined | 0ns |  |  |
| tCSH | Delay time, RAS | to be defined | 80ns |  |  |
|  | low to CAS high |  |  |  |  |
| tCSR | Delay time, CAS low to RAS low | to be defined | 10ns |  |  |
| tRAD | Delay time, RAS | to be defined | 15ns | 40ns |  |
|  | low to  column-address |  |  |  |  |
| tRAL | Delay time, column-address to RAS high | to be defined | 40ns |  |  |
| tCAL | Delay time, | to be defined | 40ns |  |  |
|  | column-address to CAS high |  |  |  |  |
| tRCD | Delay time, RAS low to CAS low | to be defined | 20ns | 60ns |  |
| tRPC | Delay time, RAS | to be defined | 0ns |  |  |
|  | high to CAS low |  |  |  |  |
| tRSH | Delay time, CAS low to RAS high | to be defined | 20ns |  |  |
| tT | Transition time | to be defined | 2ns | 50ns |  |
| tRAS | Non-page-mode pulse duration,  RAS low | to be defined | 80ns | 10000ns |  |
| tCAS | Pulse duration, | to be defined | 20ns | 10000ns |  |
|  | CAS low |  |  |  |  |
| tCLZ | CAS to output in low Z | to be defined | 0ns |  |  |
| tOFF | output disable | to be defined | 0ns | 20ns |  |
|  | time after CAS high |  |  |  |  |
| tBufferAndPD | Buffer propagation delays | to be defined | 1.3ns | 15.1ns |  |
| tPD | CPLD worst | to be defined |  | 10ns |  |
|  | case path |  |  |  |  |
| tCAC | Access time from CAS low | to be defined |  | 20ns |  |
| tRAC | Access time | to be defined |  | 80ns |  |
|  | from RAS low |  |  |  |  |
| tRP | Pulse duration,  RAS high | to be defined | 60ns |  |  |
|

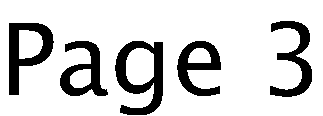


|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| General Data continued... | |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| t\_SMC40 | Data Setup time before NRD | to be defined | 7.5ns |  |  |
| t\_SMC41 | Data Hold time | to be defined | -3.4ns |  |  |
|  | after NRD rising |  |  |  |  |
| t\_SMC32 MCK falling to  NRD inactive | | to be defined | 4.5ns | 6.8ns |  |
|

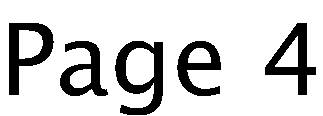




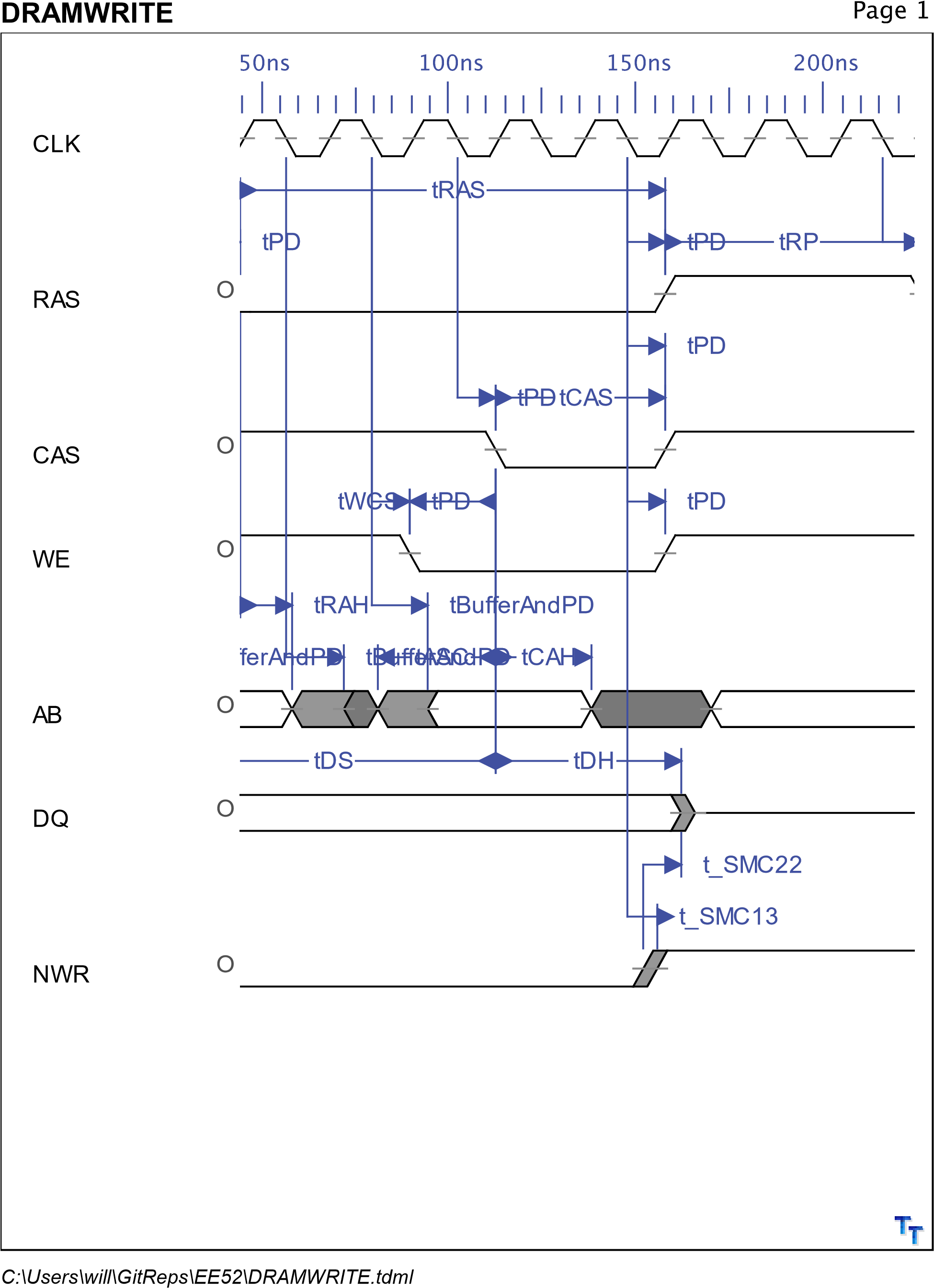
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| General Data |  |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| tASR | Row-address setup time before RAS low | to be defined | 0ns |  |  |
| tASC | Column-address | to be defined | 0ns |  |  |
|  | setup time before CAS low |  |  |  |  |
| tDS | Data setup time | to be defined | 0ns |  |  |
| tRCS | Read setup time | to be defined |  |  |  |
|  | before CAS low |  |  |  |  |
| tCWL | W low setup time before CAS | to be defined | 20ns |  |  |
| tRWL | W low setup | to be defined |  |  |  |
|  | time before RAS |  |  |  |  |
| tWCS | W low setup time before CAS | to be defined | 0ns |  |  |
| tWSR | W high setup | to be defined | 10ns |  |  |
|  | time  (CAS-before-RAS refresh only) |  |  |  |  |
| tCAH | Column-address hold time after  CAS low | to be defined | 15ns |  |  |
| tDHR | Data hold time | to be defined | 60ns |  |  |
|  | after RAS low |  |  |  |  |
| tDH | Data hold time | to be defined | 15ns |  |  |
| tAR | Column-address | to be defined | 60ns |  |  |
|  | hold time after  RAS low |  |  |  |  |
| tRAH | Row-address  hold time after  RAS low | to be defined | 10ns |  |  |
| tRCH | Read hold time | to be defined | 0ns |  |  |
|  | after CAS high |  |  |  |  |
| tRRH | Read hold time after RAS high | to be defined | 0ns |  |  |
| tWCH | Write hold time | to be defined | 15ns |  |  |
|  | after CAS low |  |  |  |  |
| tWCR | Write hold time after RAS low | to be defined | 60ns |  |  |
| tWHR | W high hold time | to be defined | 10ns |  |  |
|  | (CAS-before-RAS refresh only) |  |  |  |  |
| tCHR | Delay time, RAS low to CAS high | to be defined | 20ns |  |  |
|

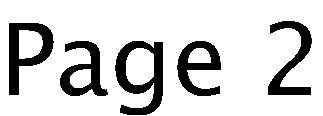


|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| General Data continued... | |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| tCRP | Delay time, CAS high to RAS low | to be defined | 0ns |  |  |
| tCSH | Delay time, RAS | to be defined | 80ns |  |  |
|  | low to CAS high |  |  |  |  |
| tCSR | Delay time, CAS low to RAS low | to be defined | 10ns |  |  |
| tRAD | Delay time, RAS | to be defined | 15ns | 40ns |  |
|  | low to  column-address |  |  |  |  |
| tRAL | Delay time, column-address to RAS high | to be defined | 40ns |  |  |
| tCAL | Delay time, | to be defined | 40ns |  |  |
|  | column-address to CAS high |  |  |  |  |
| tRCD | Delay time, RAS low to CAS low | to be defined | 20ns | 60ns |  |
| tRPC | Delay time, RAS | to be defined | 0ns |  |  |
|  | high to CAS low |  |  |  |  |
| tRSH | Delay time, CAS low to RAS high | to be defined | 20ns |  |  |
| tT | Transition time | to be defined | 2ns | 50ns |  |
| tRAS | Non-page-mode pulse duration,  RAS low | to be defined | 80ns | 10000ns |  |
| tCAS | Pulse duration, | to be defined | 20ns | 10000ns |  |
|  | CAS low |  |  |  |  |
| tCLZ | CAS to output in low Z | to be defined | 0ns |  |  |
| tOFF | output disable | to be defined | 0ns | 20ns |  |
|  | time after CAS high |  |  |  |  |
| tBufferAndPD | Buffer propagation delays | to be defined | 1.3ns | 15.1ns |  |
| tPD | CPLD worst | to be defined |  | 10ns |  |
|  | case path |  |  |  |  |
| tCAC | Access time from CAS low | to be defined |  | 20ns |  |
| tRAC | Access time | to be defined |  | 80ns |  |
|  | from RAS low |  |  |  |  |
| tRP | Pulse duration,  RAS high | to be defined | 60ns |  |  |
|

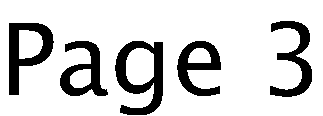


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| --- | --- | --- | --- | --- | --- |
| General Data continued... | |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| tCP Pulse duration,  CAS high | | to be defined | 10ns |  |  |
|

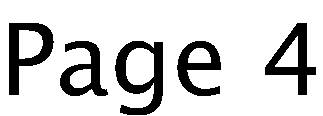




|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| General Data |  |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| tASR | Row-address setup time before RAS low | to be defined | 0ns |  |  |
| tASC | Column-address | to be defined | 0ns |  |  |
|  | setup time before CAS low |  |  |  |  |
| tDS | Data setup time | to be defined | 0ns |  |  |
| tRCS | Read setup time | to be defined |  |  |  |
|  | before CAS low |  |  |  |  |
| tCWL | W low setup time before CAS | to be defined | 20ns |  |  |
| tRWL | W low setup | to be defined |  |  |  |
|  | time before RAS |  |  |  |  |
| tWCS | W low setup time before CAS | to be defined | 0ns |  |  |
| tWSR | W high setup | to be defined | 10ns |  |  |
|  | time  (CAS-before-RAS refresh only) |  |  |  |  |
| tCAH | Column-address hold time after  CAS low | to be defined | 15ns |  |  |
| tDHR | Data hold time | to be defined | 60ns |  |  |
|  | after RAS low |  |  |  |  |
| tDH | Data hold time | to be defined | 15ns |  |  |
| tAR | Column-address | to be defined | 60ns |  |  |
|  | hold time after  RAS low |  |  |  |  |
| tRAH | Row-address  hold time after  RAS low | to be defined | 10ns |  |  |
| tRCH | Read hold time | to be defined | 0ns |  |  |
|  | after CAS high |  |  |  |  |
| tRRH | Read hold time after RAS high | to be defined | 0ns |  |  |
| tWCH | Write hold time | to be defined | 15ns |  |  |
|  | after CAS low |  |  |  |  |
| tWCR | Write hold time after RAS low | to be defined | 60ns |  |  |
| tWHR | W high hold time | to be defined | 10ns |  |  |
|  | (CAS-before-RAS refresh only) |  |  |  |  |
| tCHR | Delay time, RAS low to CAS high | to be defined | 20ns |  |  |
|



|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| General Data continued... | |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| tCRP | Delay time, CAS high to RAS low | to be defined | 0ns |  |  |
| tCSH | Delay time, RAS | to be defined | 80ns |  |  |
|  | low to CAS high |  |  |  |  |
| tCSR | Delay time, CAS low to RAS low | to be defined | 10ns |  |  |
| tRAD | Delay time, RAS | to be defined | 15ns | 40ns |  |
|  | low to  column-address |  |  |  |  |
| tRAL | Delay time, column-address to RAS high | to be defined | 40ns |  |  |
| tCAL | Delay time, | to be defined | 40ns |  |  |
|  | column-address to CAS high |  |  |  |  |
| tRCD | Delay time, RAS low to CAS low | to be defined | 20ns | 60ns |  |
| tRPC | Delay time, RAS | to be defined | 0ns |  |  |
|  | high to CAS low |  |  |  |  |
| tRSH | Delay time, CAS low to RAS high | to be defined | 20ns |  |  |
| tT | Transition time | to be defined | 2ns | 50ns |  |
| tRAS | Non-page-mode pulse duration,  RAS low | to be defined | 80ns | 10000ns |  |
| tCAS | Pulse duration, | to be defined | 20ns | 10000ns |  |
|  | CAS low |  |  |  |  |
| tCLZ | CAS to output in low Z | to be defined | 0ns |  |  |
| tOFF | output disable | to be defined | 0ns | 20ns |  |
|  | time after CAS high |  |  |  |  |
| tBufferAndPD | Buffer propagation delays | to be defined | 1.3ns | 15.1ns |  |
| tPD | CPLD worst | to be defined |  | 10ns |  |
|  | case path |  |  |  |  |
| tCAC | Access time from CAS low | to be defined |  | 20ns |  |
| tRAC | Access time | to be defined |  | 80ns |  |
|  | from RAS low |  |  |  |  |
| tRP | Pulse duration,  RAS high | to be defined | 60ns |  |  |
|



|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| General Data continued... | |  |  |  |  |
| SYMBOL | DEFINITION | DESCRIPTION | MIN | MAX | NOTES |
| tBuffer |  | to be defined | 1.3ns | 5.1ns |  |
| t\_SMC13 | MCK Falling to | to be defined | 4.1ns | 7.9ns |  |
|  | NWR inactive |  |  |  |  |
| t\_SMC22 MCK Rising to  Data out invalid | | to be defined | 10.2ns |  |  |
|

# Appendix D (DRAM Abel Code)

# Appendix E (Software)

# Appendix F (Printed Circuit Board)

# Appendix G (Schematics)