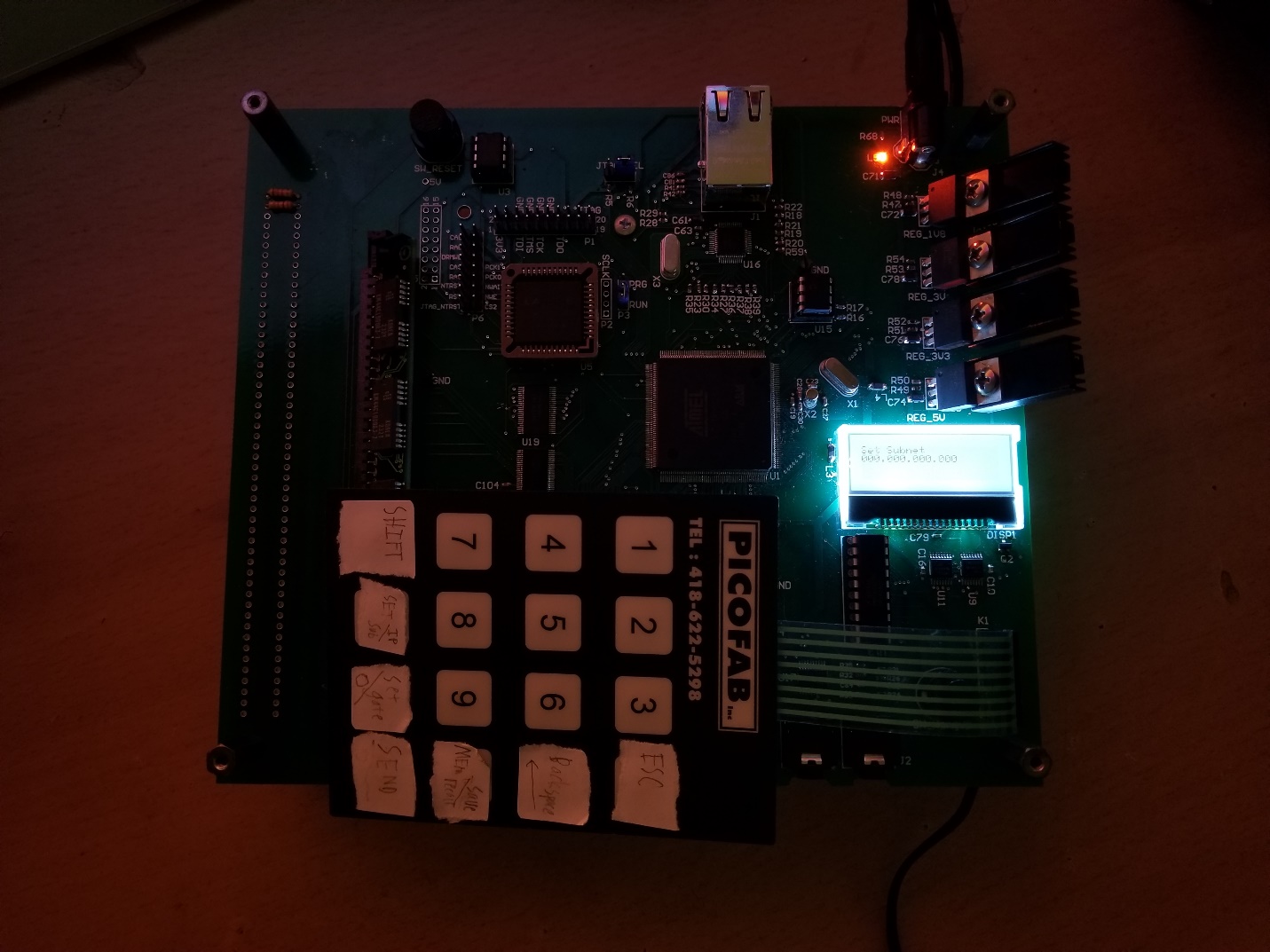
VoIP phone Technical Documentation



The EE52 VoIP phone is a phone that can communicate with other EE52 VoIP phones. The user controls the phone by using a 128x32 display and a 4x4 keypad. There is a headphone and microphone jack that a headset can be plugged into, and there is a button for putting the phone “on-the-hook” to hangup the call.

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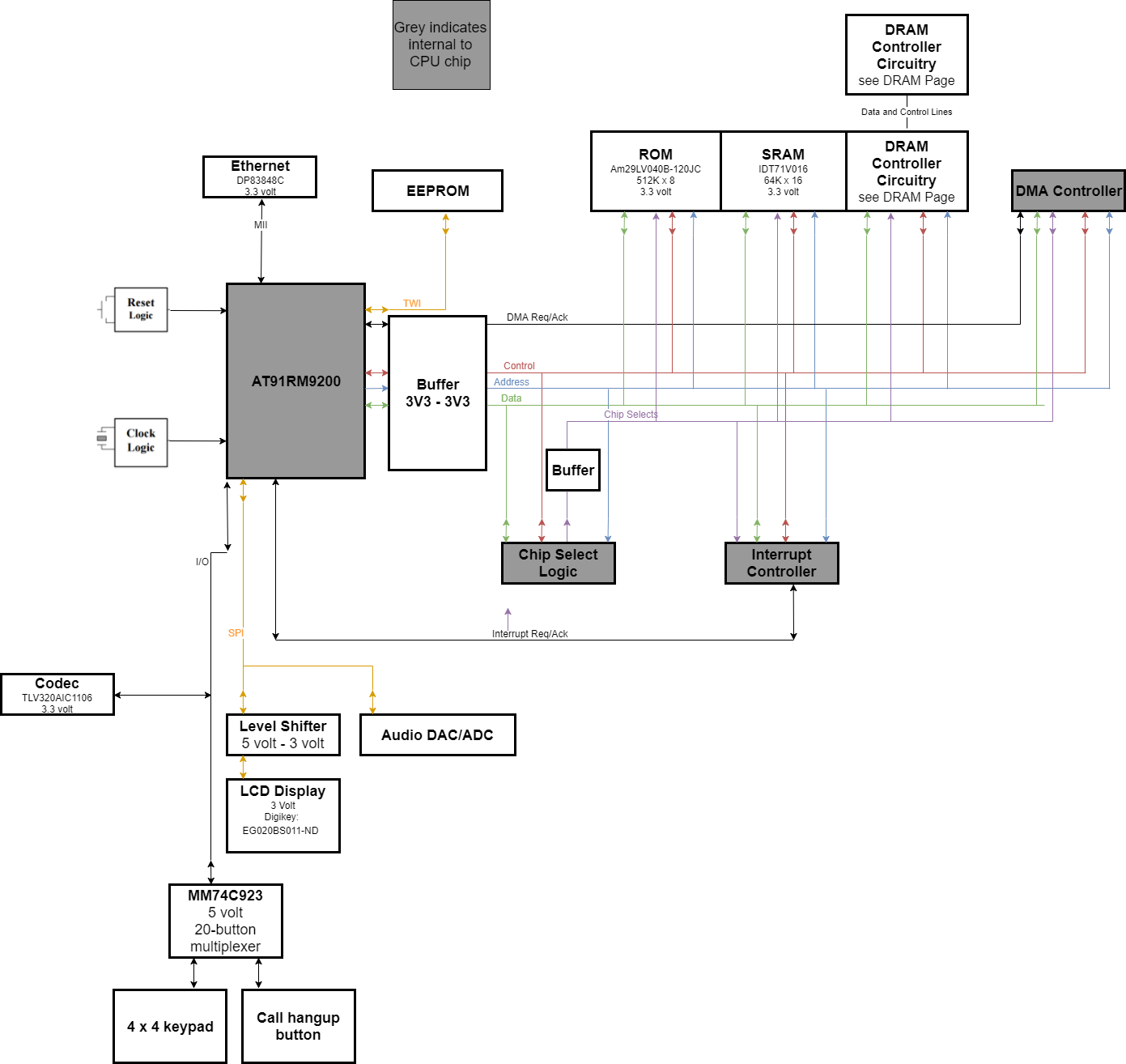
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# Overview

|  |  |
| --- | --- |
| Processor | Atmel AT91RM9200 |
| Input power | 8V-12V DC 5.5mm barrel jack |
| Display | 128x32 |
| Headphone Jack | 3.5mm mono audio jack |
| Microphone Jack | 3.5mm |
| Keypad | 4x4 button keypad |

## Block Diagram



# Power Circuitry

The system takes ~8V-12V DC input. The upper bound is due to thermal dissipation constraints of the linear regulator heatsinks. There are four power rails on this board.

|  |  |
| --- | --- |
| Rail | Uses |
| 5V | Reset circuit, DRAM, CPLD |
| 3V3 | Audio, SRAM, ROM, CPU |
| 3V | Display |
| 1V8 | CPU Core logic |

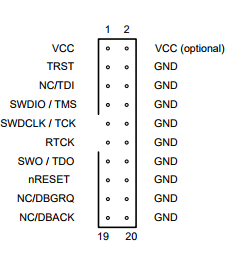
# CPU Support Circuitry

## Reset

The reset circuitry uses a MAX705 chip in the standard configuration. See Appendix G (Schematics)

## JTAG

This board has a JTAG interface routed and populated for the purposes of debugging. It is a 20-pin legacy ARM IDC 0.1” pitch JTAG connector with the following pinout (see <http://infocenter.arm.com/help/topic/com.arm.doc.faqs/attached/13634/cortex_debug_connectors.pdf>):



# Memory

All memory access is done through 74LVT16245 buffers.

## ROM

This board uses a 29LV040 chip for ROM. This chip has an address bus width of 19 bits, and a data bus width of 8 bits. It is on chip select 7.

## SRAM

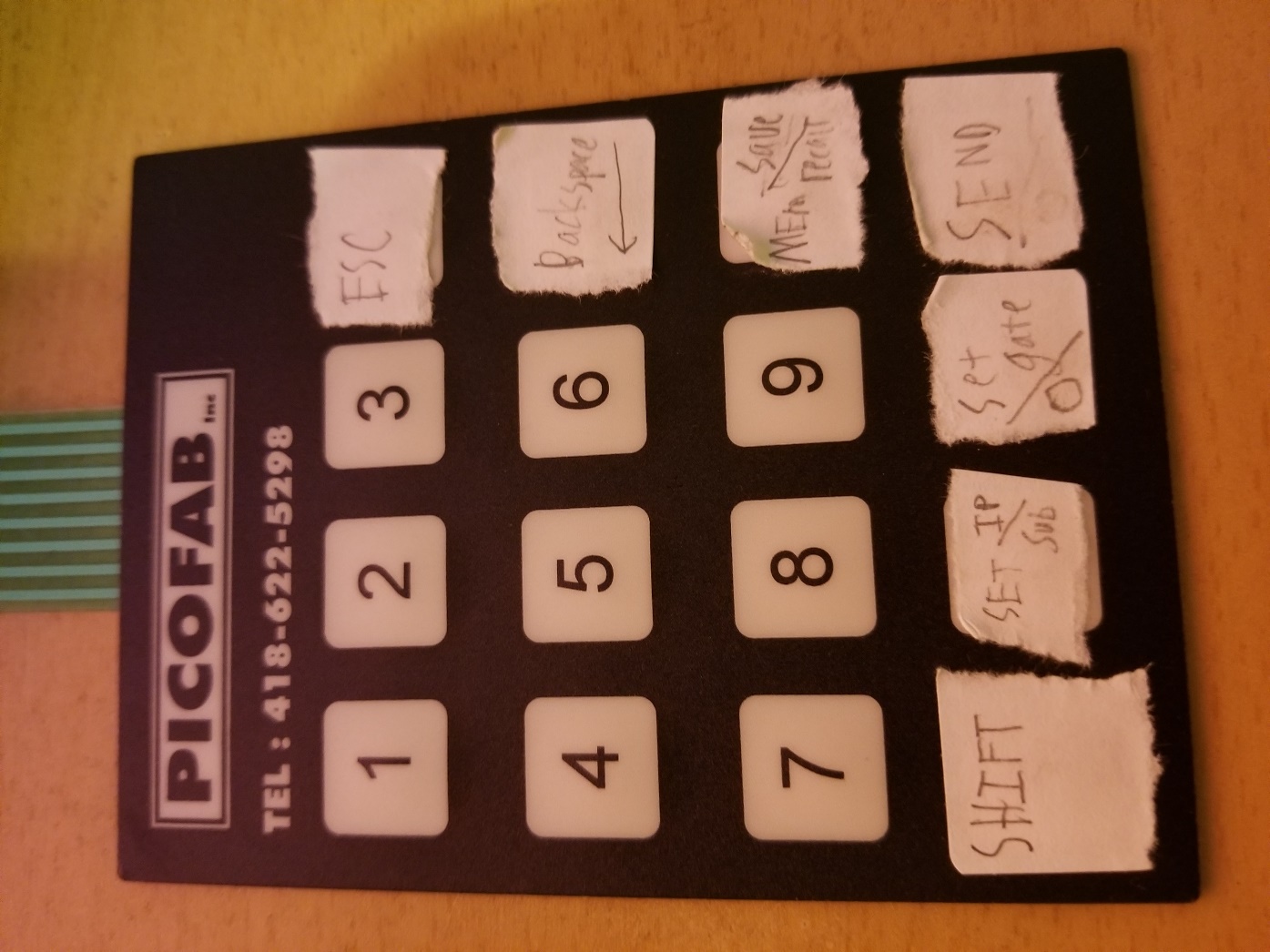
This board uses a IDT71V016 chip for SRAM. This chip has an address bus width of 16 bits, and a data bus width of 16 bits. It is on chip select 1

## DRAM

This board uses a socket mount DRAM module. The DRAM controller is implemented in a CPLD. The address lines are multiplexed to the DRAM via U19 and U21, which are two buffers that can be toggle high-Z and enabled by the CPLD DRAM controller. The data lines are connected to the CPU data bus via a bidirectional buffer that is enabled when the DRAM chip select goes low. The directionality of the buffer is set by the NRD signal.

# User Interface Components

## Keypad



## Display



The display is a 128x32 display, divided into 4 rows. Only the top two rows are used.

The top row displays the current menu the system is in, or the status of the system if a call is in progress.

The 2nd row displays auxiliary information for a menu, such as the IP address being set, the subnet mask, or the memory location for recall.

## Audio

## Ethernet

# Appendix A (ROM Timing)

# Appendix B (SRAM Timing)

# Appendix C (DRAM Timing)

# Appendix D (DRAM Abel Code)

# Appendix E (Software)

# Appendix F (Printed Circuit Board)

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