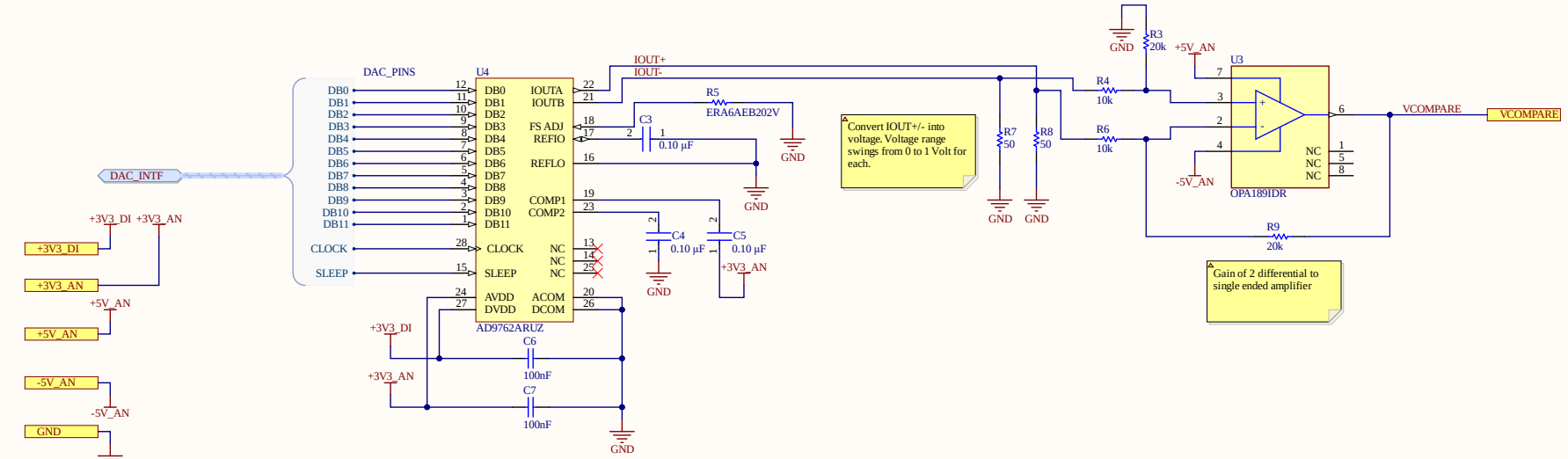

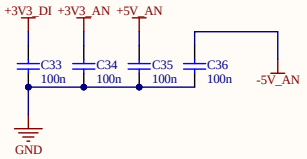

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Date: 11/11/2020		Sheet of
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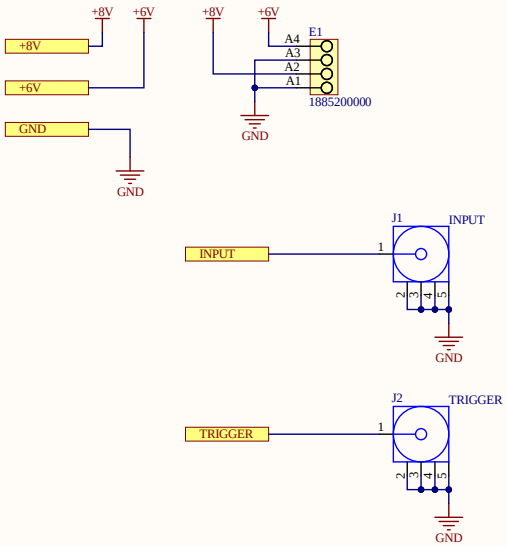

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Date: 11/11/2020		Sheet of	
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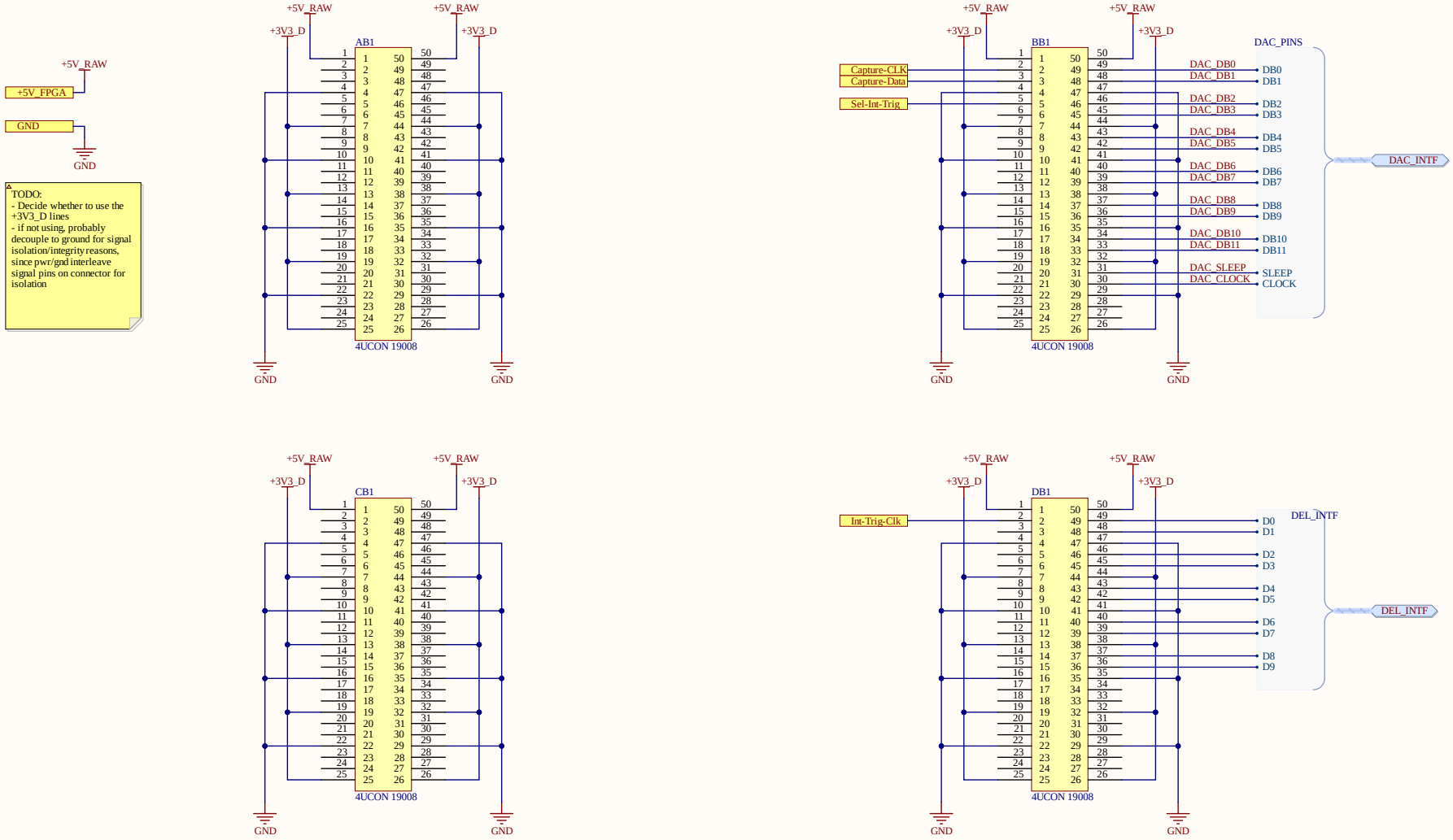
+5V_RAW
+5V_FPGA
GND
GND
TODO:
- Decide whether to use the +3V3_D lines
- if not using, probably decouple to ground for signal isolation/integrity reasons, since pwr/gnd interleave signal pins on connector for isolation
+5V_RAW
+3V3_D
+5V_RAW
+3V3_D
AB1
4UCON 19008
GND
GND
+5V_RAW
+3V3_D
+5V_RAW
+3V3_D
BB1
Capture-CLK
Capture-Data
Sel-Int-Trig
DAC_DB0
DAC_DB1
DAC_DB2
DAC_DB3
DAC_DB4
DAC_DB5
DAC_DB6
DAC_DB7
DAC_DB8
DAC_DB9
DAC_DB10
DAC_DB11
DAC_SLEEP
DAC_CLOCK
DAC_PINS
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
DB11
SLEEP
CLOCK
DAC_INTF
4UCON 19008
GND
GND
+5V_RAW
+3V3_D
+5V_RAW
+3V3_D
CB1
4UCON 19008
GND
GND
+5V_RAW
+3V3_D
+5V_RAW
+3V3_D
DB1
Int-Trig-Clk
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
DEL_INTF
DEL_INTF
4UCON 19008
GND
GND
Title
Size
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Number
Revision
Date: 11/11/2020
Sheet of
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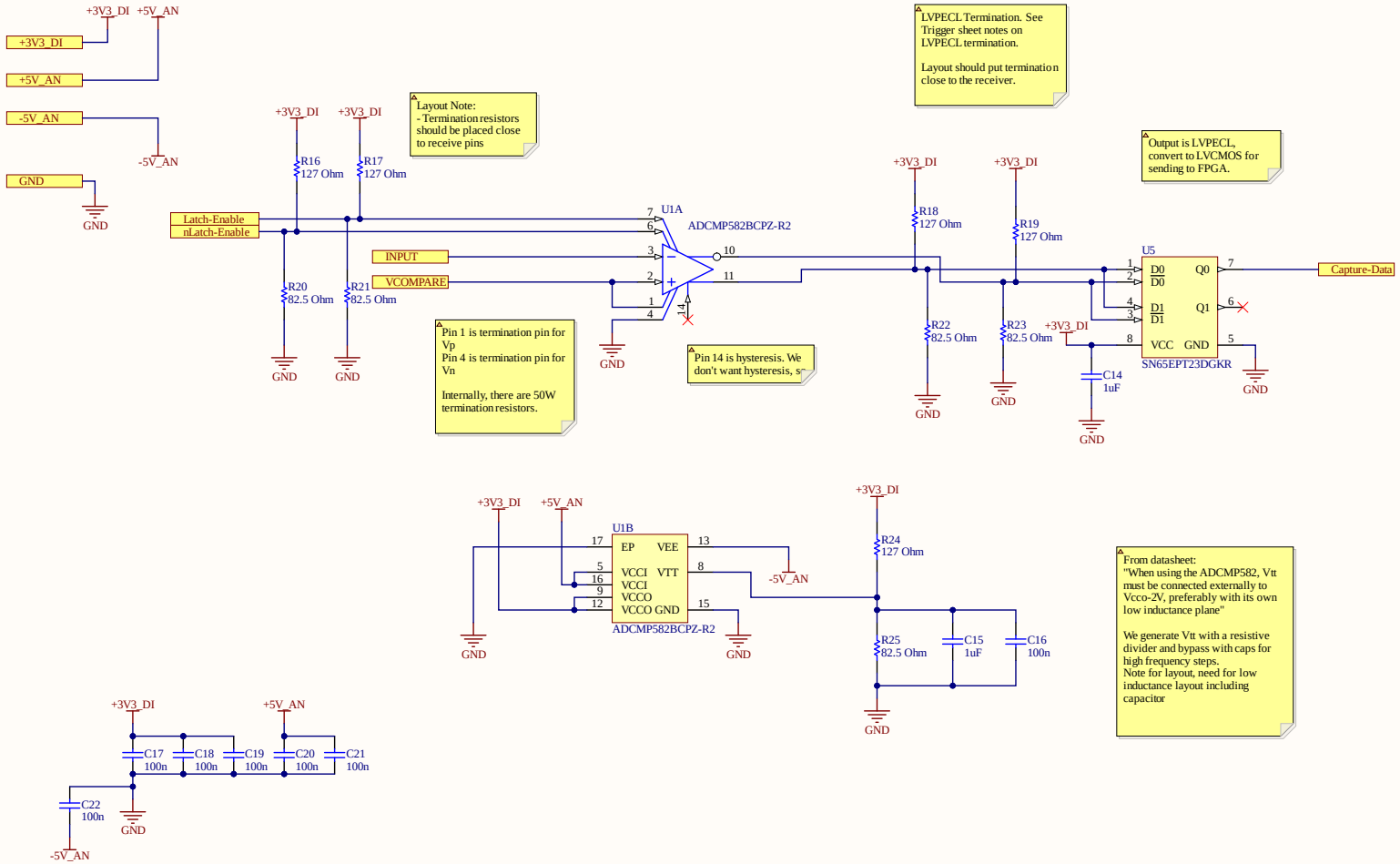

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Date: 11/11/2020		Sheet of
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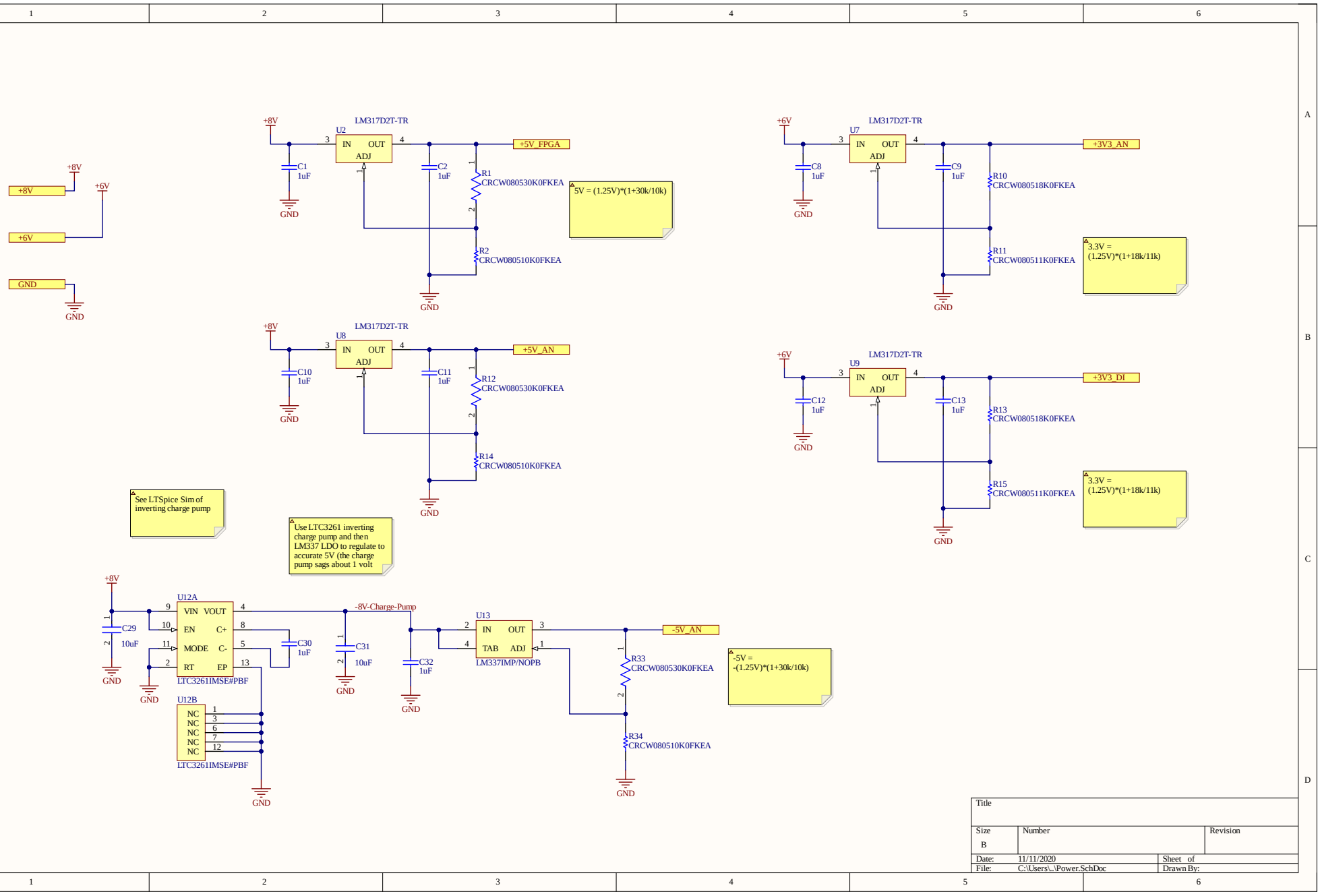
+8V
+6V
GND
U2
LM317D2T-TR
IN
OUT
ADJ
C1
1uF
C2
1uF
R1
CRCW080530K0FKEA
R2
CRCW080510K0FKEA
+5V_FPGA
5V = (1.25V)*(1+30k/10k)
U7
C8
1uF
C9
1uF
R10
CRCW080518K0FKEA
R11
CRCW080511K0FKEA
+3V3_AN
3.3V =
(1.25V)*(1+18k/11k)
U8
C10
1uF
C11
1uF
R12
CRCW080530K0FKEA
R14
CRCW080510K0FKEA
+5V_AN
U9
C12
1uF
C13
1uF
R13
CRCW080518K0FKEA
R15
CRCW080511K0FKEA
+3V3_DI
3.3V =
(1.25V)*(1+18k/11k)
See LTSpice Sim of inverting charge pump
Use LTC3261 inverting charge pump and then LM337 LDO to regulate to accurate 5V (the charge pump sags about 1 volt
U12A
VIN
VOUT
EN
C+
MODE
C-
RT
EP
LTC3261IMSE#PBF
C29
10uF
C30
1uF
C31
10uF
C32
1uF
-8V-Charge-Pump
U12B
NC
LTC3261IMSE#PBF
U13
IN
OUT
TAB
ADJ
LM337IMP/NOPB
-5V_AN
-5V =
-(1.25V)*(1+30k/10k)
R33
CRCW080530K0FKEA
R34
CRCW080510K0FKEA
Title
Size
B
Number
Revision
Date:
11/11/2020
Sheet of
File:
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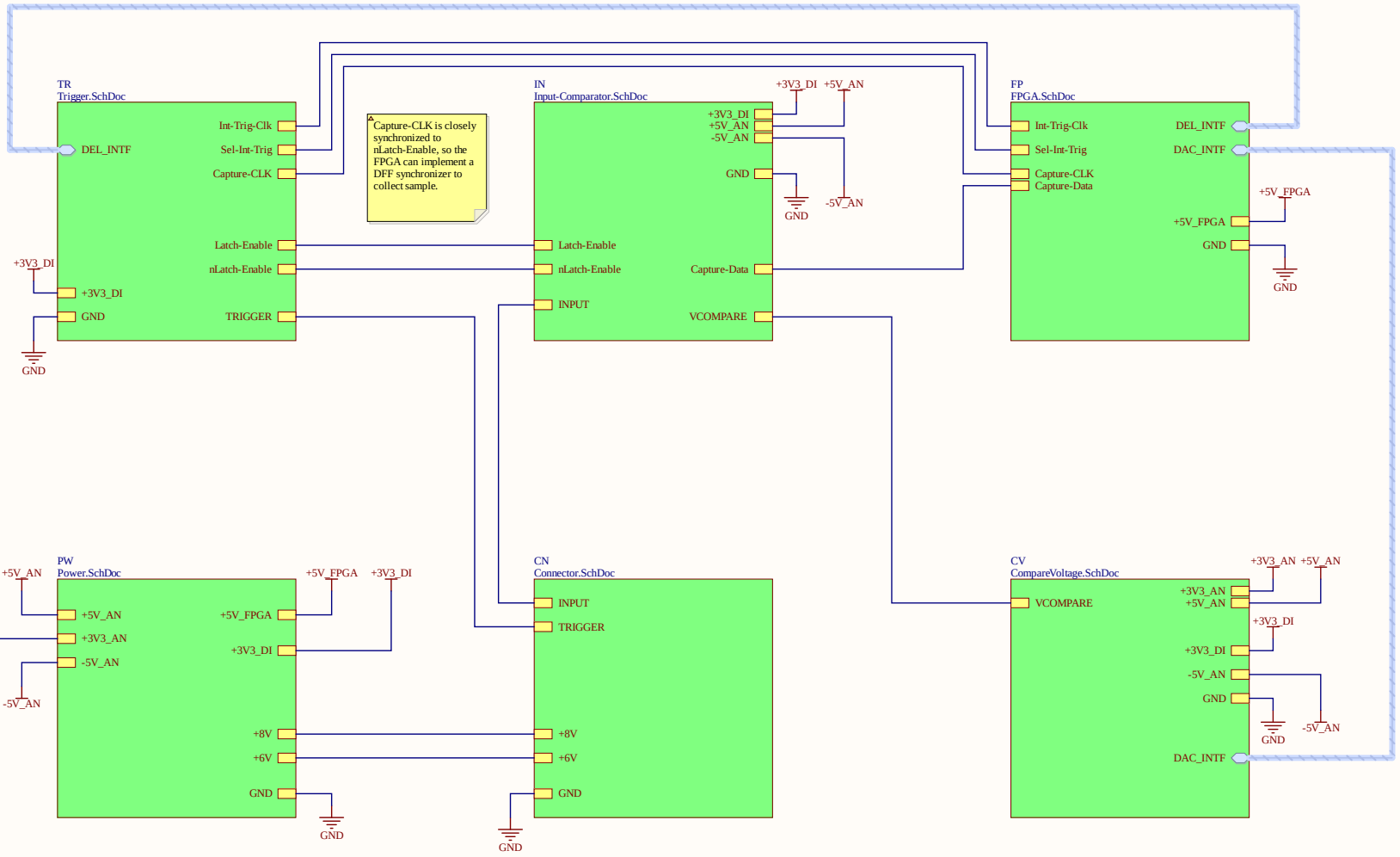
Drawn By:



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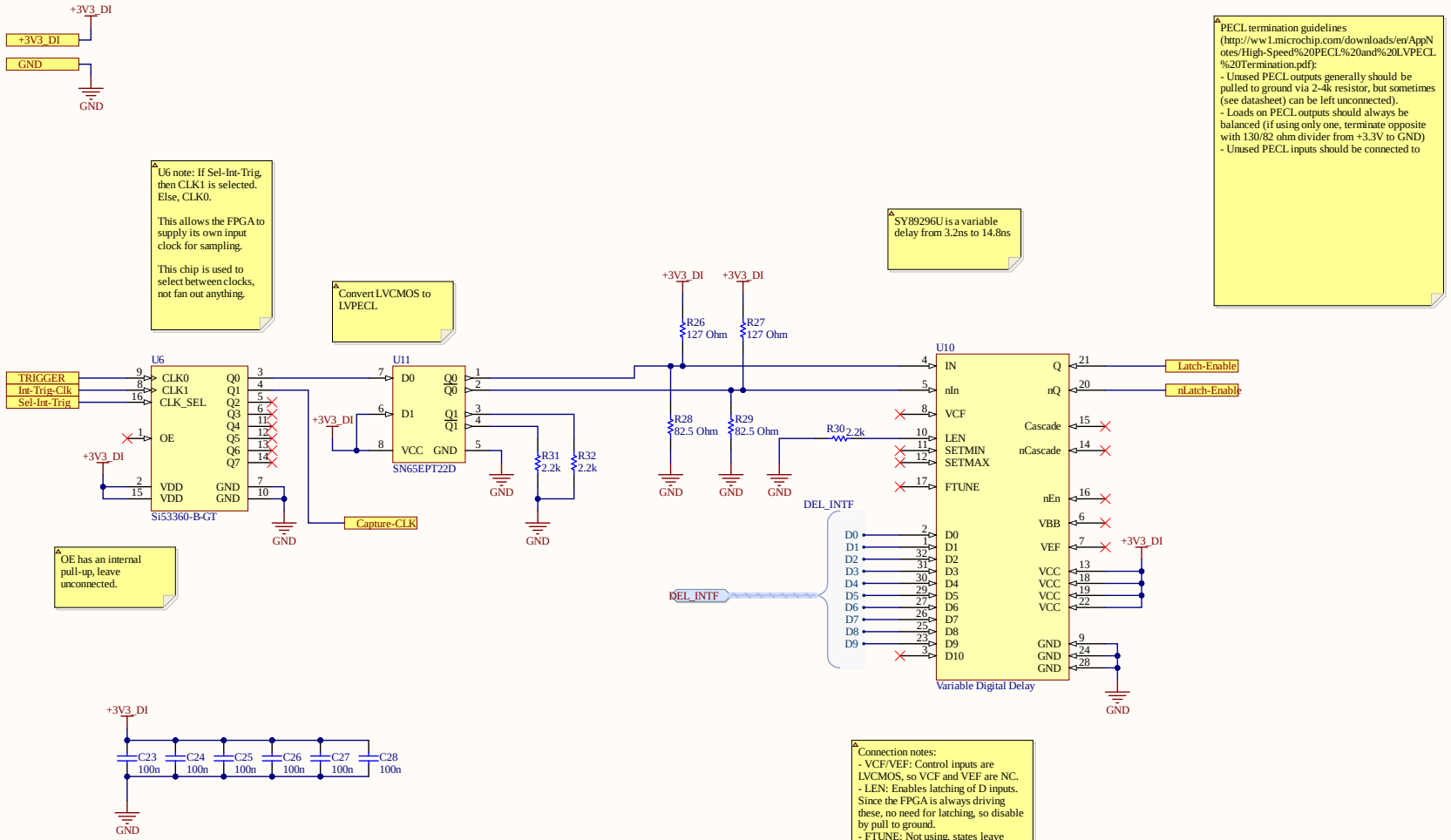

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