Sixteen-Bit Full Adder With Carry Look Ahead

Very Large Scale Integration

University of Nebraska, Lincoln

William Willie Wells

wwells@cse.unl.edu

Abstract

Addition is a fundamental operation required by computational devices. Modern devices are capable of adding significantly more than 16-bits. Simple adder design involves the use of XORs. A more advanced design utilizes transmission gates and reduces the total required transistor count for a single stage full adder with carry look ahead from 44 required transistors to 24 required transistors. This significantly reduces the area required for the overall design.

Logic Diagram

The following schematic is a Cadence realization of a transmission gate full adder.

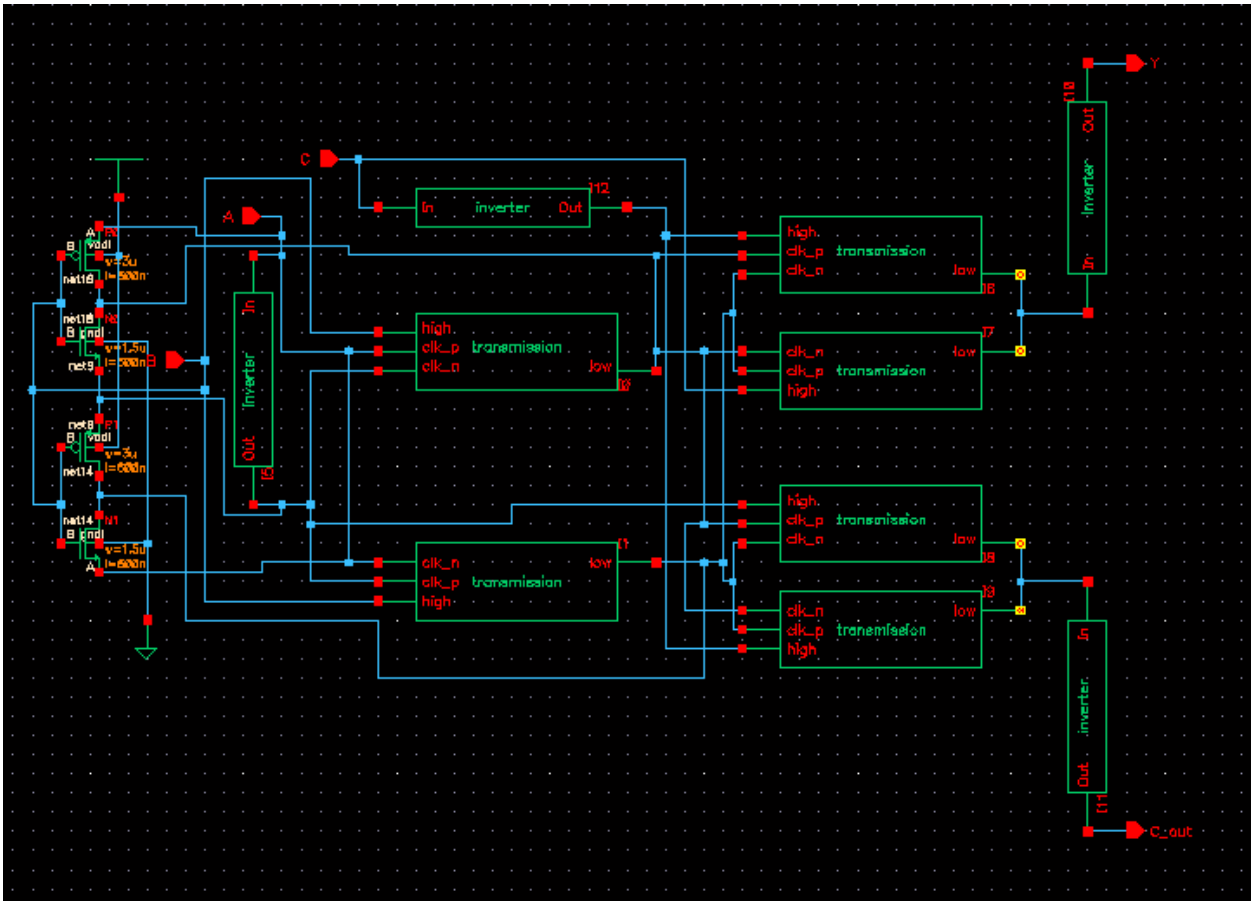

Figure 1: Single stage full adder schematic

Transmission gate full adders use 6 transmission gates, 4 inverters, and 4 inline transistors in alternating PMOS then NMOS order. This is a transmission gate full adder:

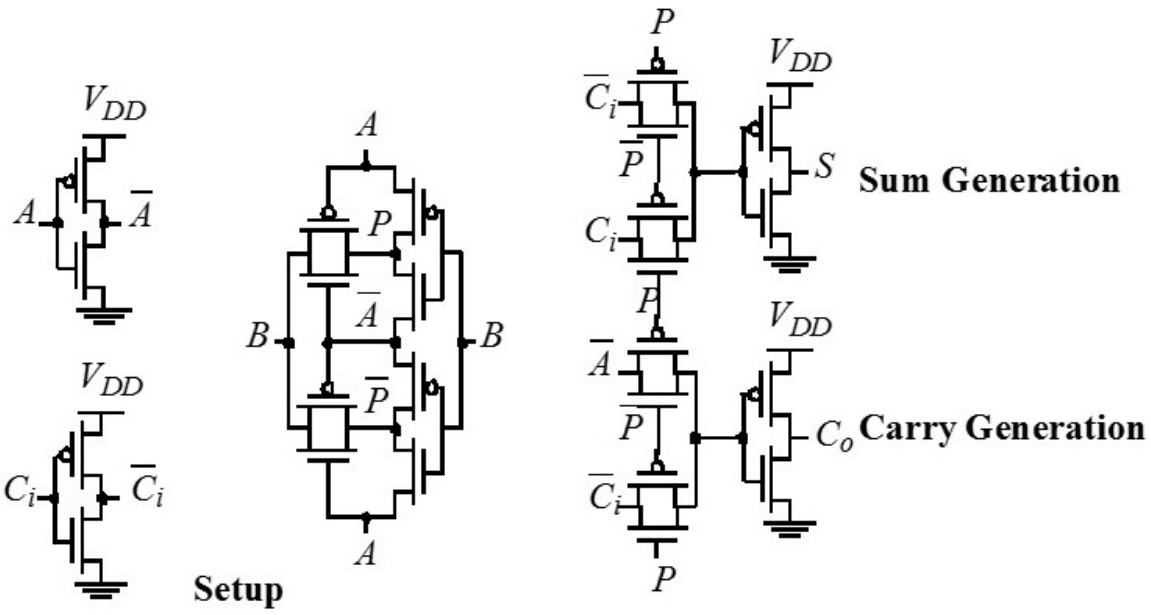

Figure 2: A disconnected basic transmission gate full adder.

The following is a schematic view of a 16-bit full adder with carry look ahead.

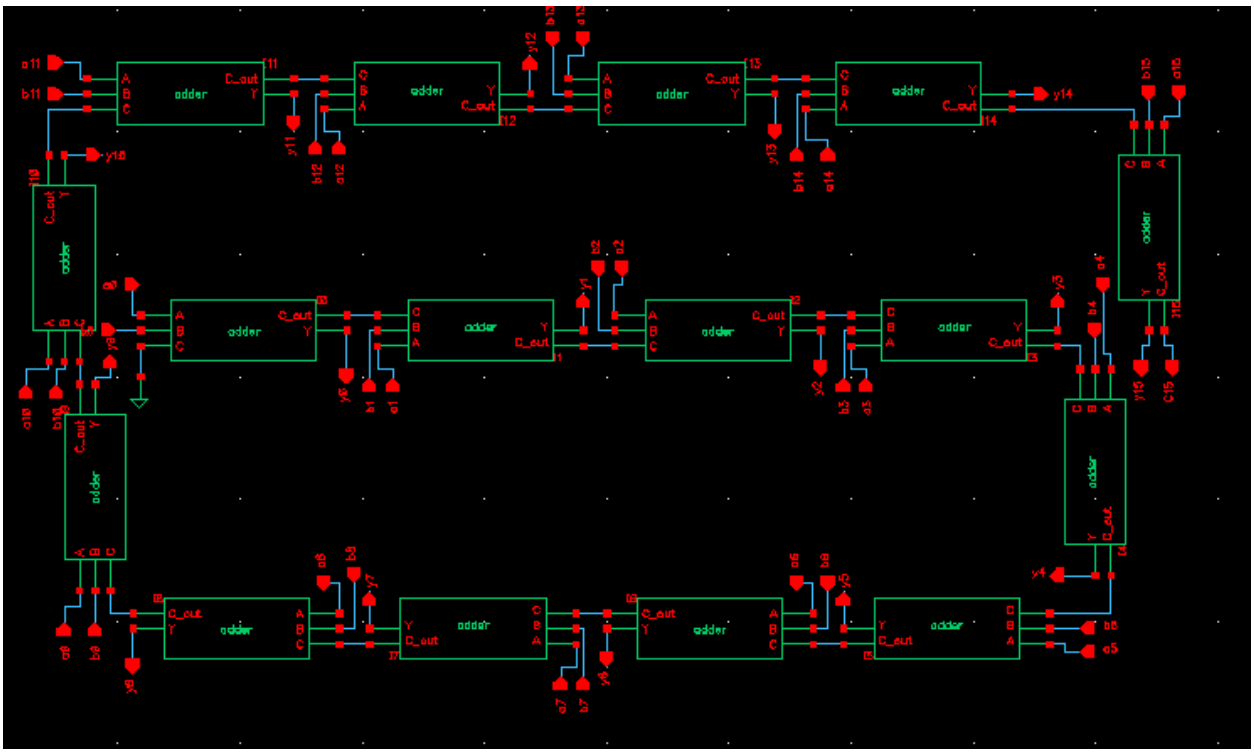

Figure 3: logic level diagram of a 16-bit full adder with carry look ahead.

Transistor Diagram

The following depicts the device sizes of the invertor and transmission gate transistors. All NMOS devices have a W = 1.5 µm while all PMOS devices have a W = 3.0 µm.

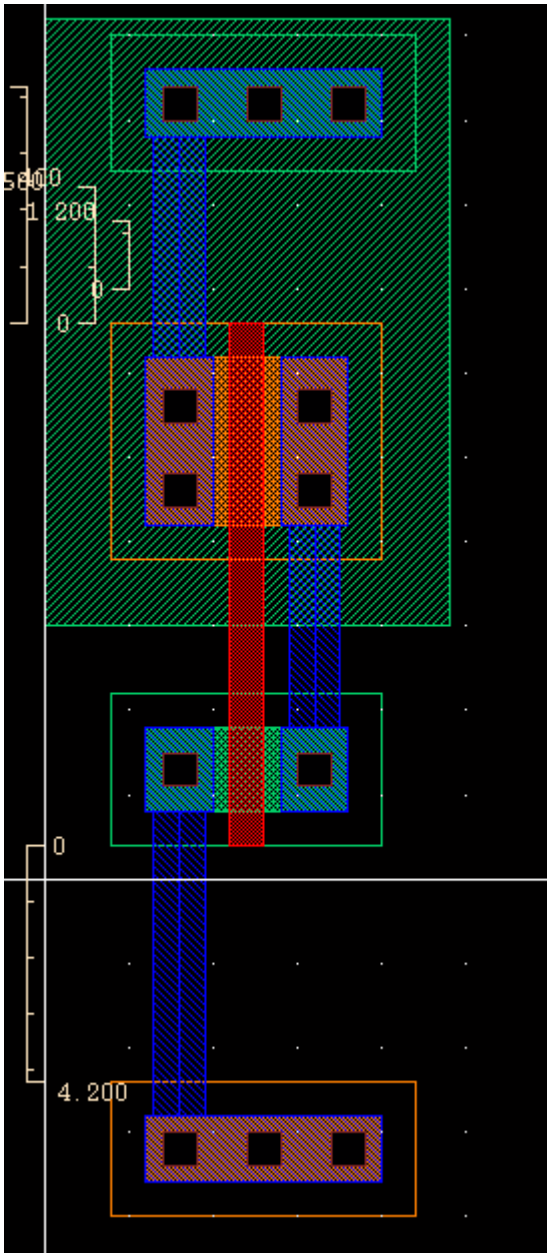

Figure 4: Invertor with power and ground rail.

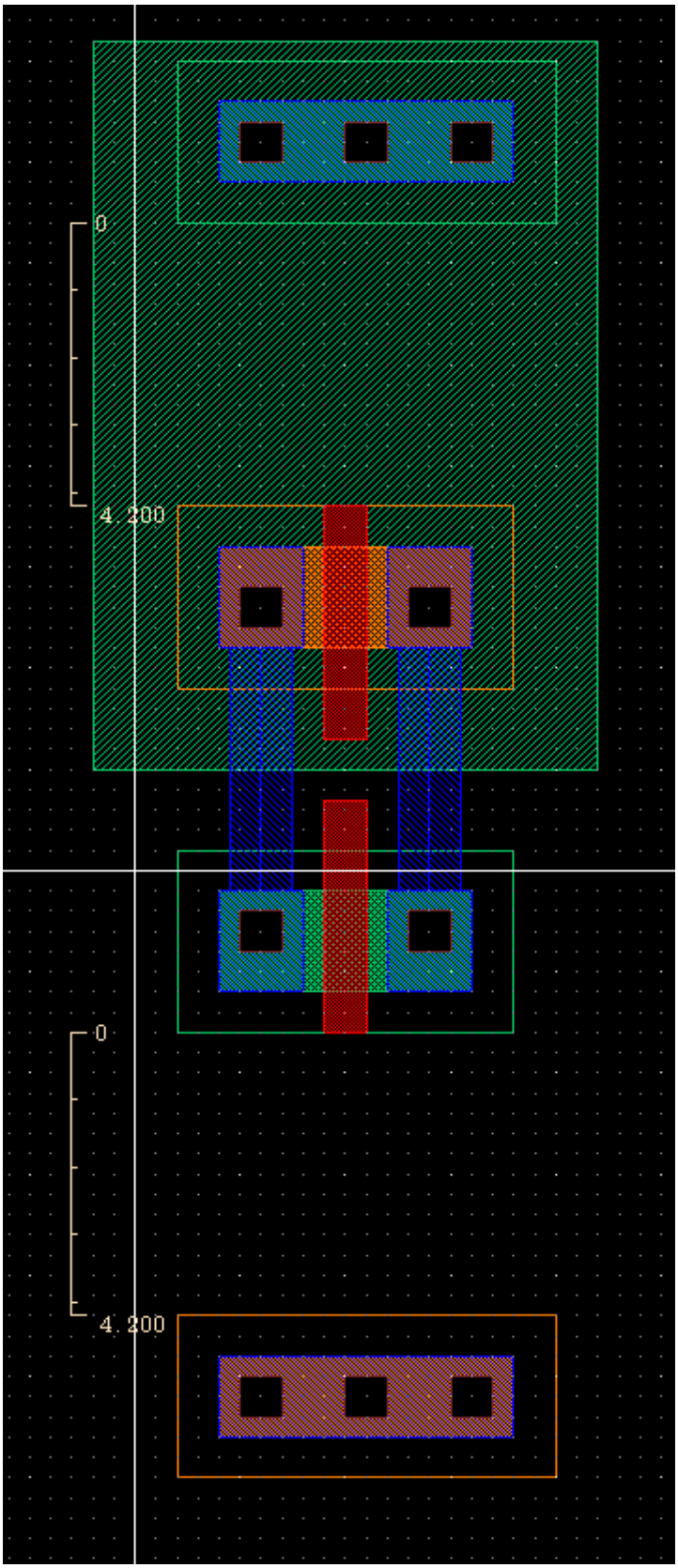

Figure 5: Transmission gate with power and ground rail.

The following timing diagrams show the single stage full adder working for all combinations of inputs including using a null carry in input that would be the logical case for the first stage full adder.

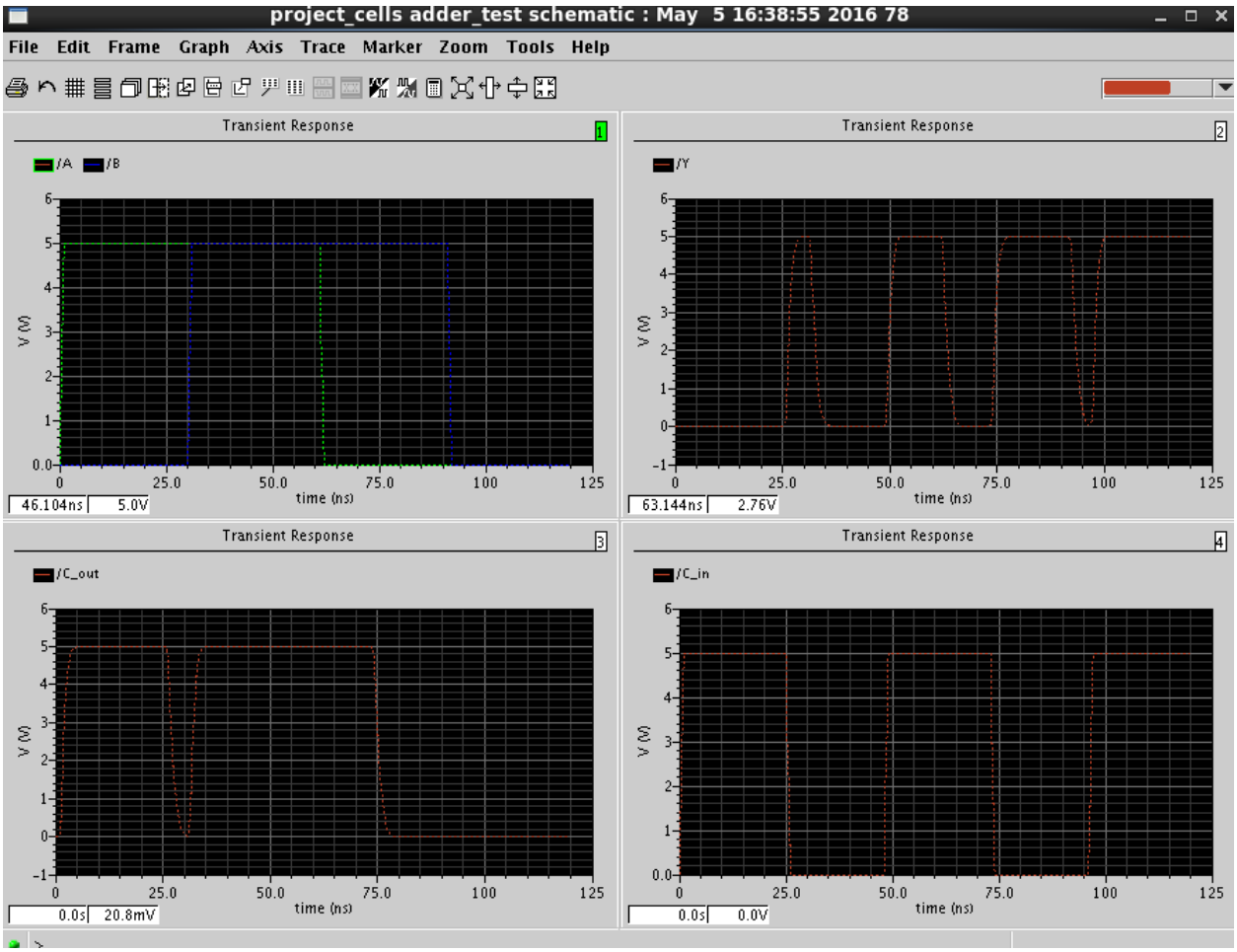

Figure 6: Single stage full adder operation. The top left pulses are inputs A and B. The top right pulse is the result of the sum, labeled Y. The bottom left pulse is the carry out signal. The Bottom right pulse is the carry in signal.

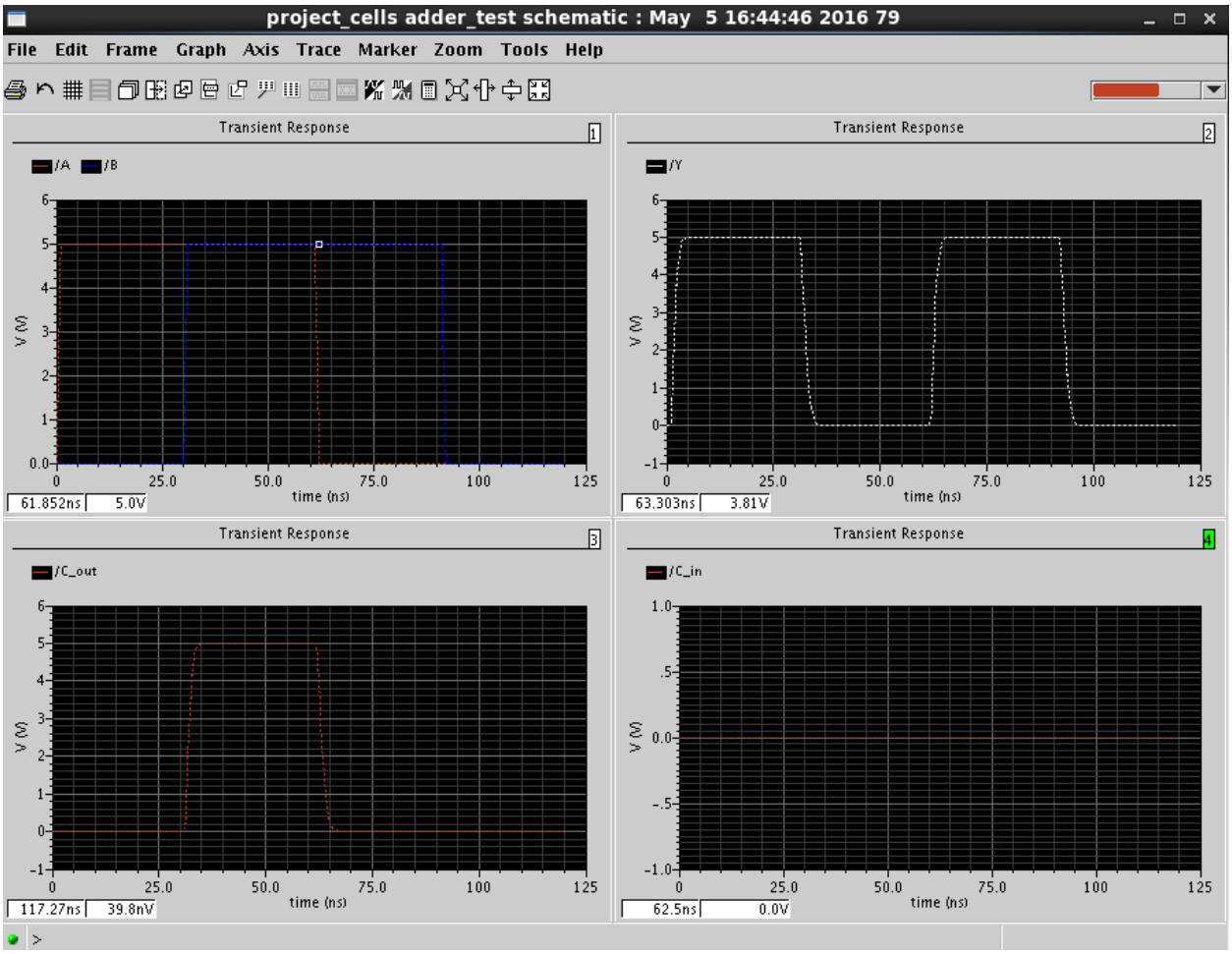

Figure 7: Single stage full adder operation with carry in held low. The top left pulses are inputs A and B. The top right pulse is the result of the sum, labeled Y. The bottom left pulse is the carry out signal. The Bottom right pulse is the carry in signal.

Layout

The following depicts the layout of a single stage full adder with carry look ahead.

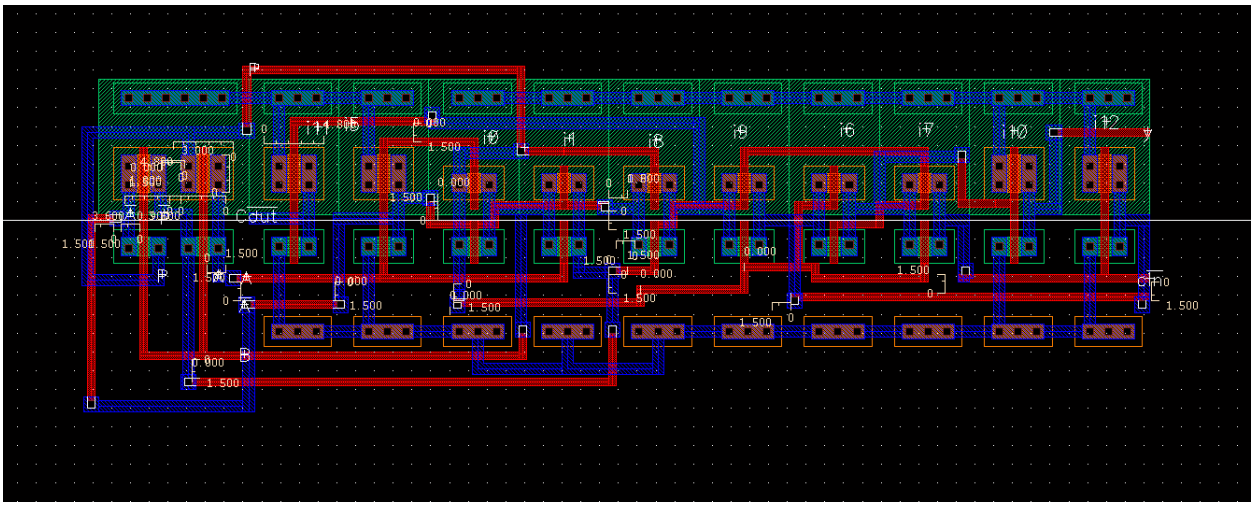

Figure 8: Layout of single stage full adder with carry look ahead.

The following depicts the layout for the full 16-bit adder with carry look ahead.

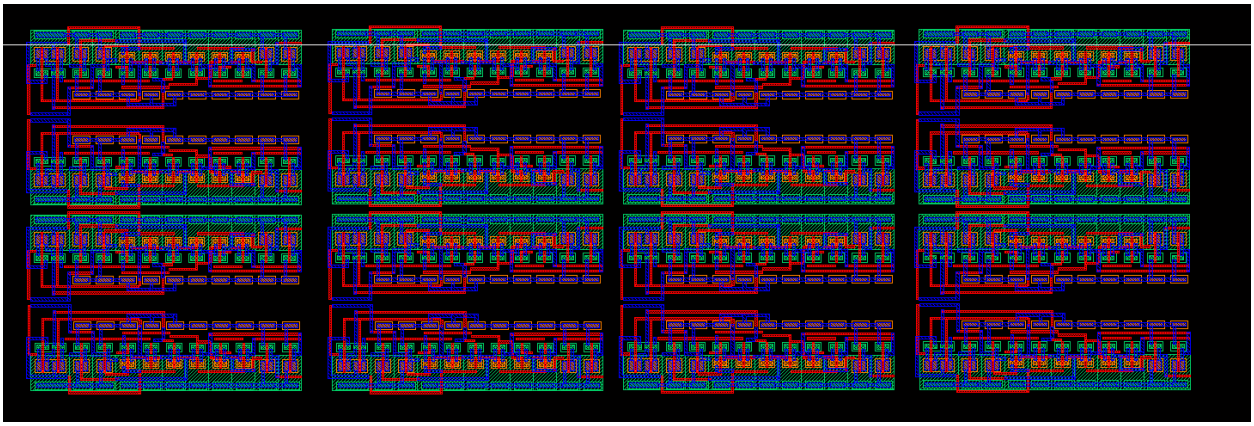

Figure 9: Layout of 16-bit full adder with carry look ahead.

Post-layout

Due to time constraints post-layout simulations were not conducted.

Conclusion

The use of transmission gates nearly halves the number of required transistors to implement a single stage full adder with carry look ahead. With reduced number of transistors per stage the overall area used can be reduced. While constructing standard cells if including power rails the spacing between the transistors and the power rails most be considered and enlarged to fit multiple paths. If only using metal 1 and poly to route paths in a single stage full adder the spacing between power rails and the transistors must be such that 3 metal 1 paths can traverse the gap. Such a design increases overall area but is possible to connect all required connections without using metal 2 or metal 3. Very Large Scale Integration design involves plenty of redesign for the novice of parameter values as well as location of objects within the layout itself.