COMP3511 Operating Systems (Fall 2016) – Supplementary Note

Topic 3: Process-Concept

- **Inter-process Communication**
  - Cache coherency issues in multicore (with multiple cache)
    - Whenever one cache is updated with information that may be used by other processors, the change needs to be reflected to the other processors, otherwise the different processors will be working with incoherent data.
    - Such cache coherence protocols can, when they work well, provide extremely high-performance access to shared information between multiple processors. On the other hand, they can sometimes become overloaded and become a bottleneck to performance.

- **Comparison between shared memory and message passing**
  - Delay
    - There is no delay with shared memory, if one process writes the other processes can read immediately.
    - With message passing, delay can happen, different messages may have different delays.
  - Overriding
    - With shared memory if a process writes to a register, another process may override the value before anyone could read the register (We are going to discuss this in Topic 6).
    - In message passing, this cannot happen. On the other hand, messages may be lost, or the inbox buffer of a process may overflow, leading to similar results.
  - Consistency
    - With shared memory, the value of a register is always the value that was written last.
    - With message passing, several message may be sent at the same time, and the order of arriving message may be messed up.