Lecture 10: language memory model

compiler optimizations, compiler barriers, language memory model, strict consistency, threads cannot be implemented as a library, visibility, volatile

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https://github.com/Svazars/parallel-programming/blob/main/slides/pdf/l10.pdf

In previous episodes: homework

"Is Parallel Programming Hard, And, If So, What Can You Do About It" (perfbook) Appendix B "Why Memory Barriers?"

- section B.1 "Cache Structure". Be ready to draw and explain what is associative hardware cache.
- section B.2.4 "MESI Protocol Example"

In previous episodes

Abstractions and algorithms (high level)

- Race conditions, deadlocks, missed signals, ABA problem
- Events, Precedence, Consistency
- Progress conditions: wait-free, lock-free, obstruction-free, starvation-free, deadlock-free
- Read-Modify-Write operations

Programmers need at least: **Linearizability** (composability of different modules)
Hardware (low level)

- Cache coherency protocol: states, transitions, message passing
- Store buffering, Load buffering, Invalidate Queues, Interconnect topology
- Reorderings of memory operations on independent memory locations
- Weak (relaxed) consistency

Hardware provides at most: **Coherence** (linear order of writes for particular location)

The Gap

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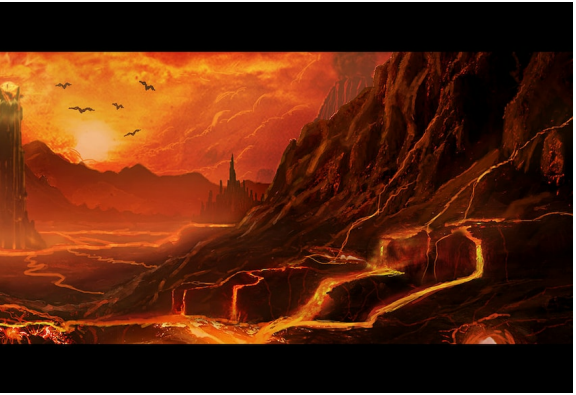

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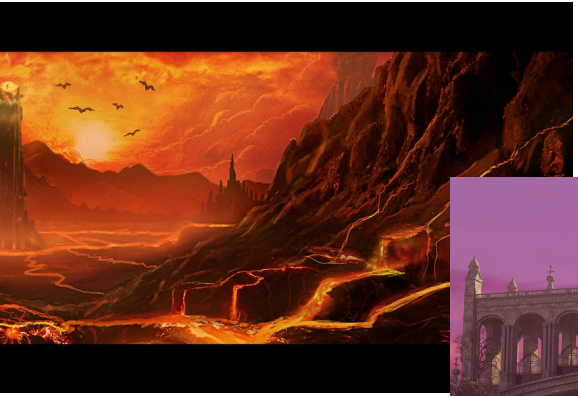

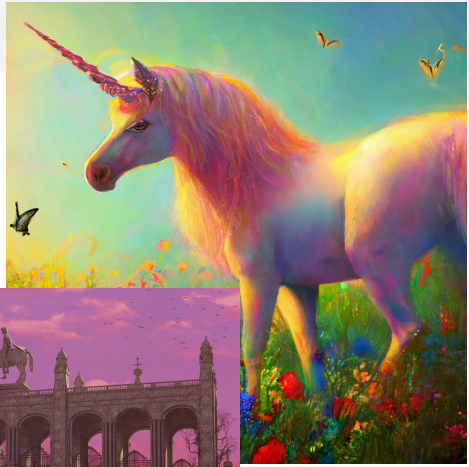

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- effective usage of scheduling quantum
- avoiding false sharing, minimizing true sharing
- replication-friendly data structures
- appropriate and lightweight memory barriers

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- allow to write hardware-agnostic and high-performant concurrent programs

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As a professional, you should be able to use any tool, not only "the favourite" one.

Supplementary materials

Unconditional benefit

- "Threads Cannot be Implemented as a Library" by Hans-J. Boehm[1]
  https://courses.cs.washington.edu/courses/cse590p/05au/HPL-2004-209.pdf
- "Memory Models" series by Russ Cox https://research.swtch.com/mm
- Herb Sutter, C++ and Beyond 2012, "Atomic Weapons" series
  https://youtu.be/A8eCGOqgvH4
- Роман Елизаров, "Многопоточное программирование — теория и практика"
  https://youtu.be/mf4lC6TpclM

Advanced material

- "Using JDK 9 Memory Order Modes" by Doug Lea
  https://gee.cs.oswego.edu/dl/html/j9mm.html
- Aleksey Shipilëv, JMM series https://shipilev.net

[1] https://www.hboehm.info/misc_slides/pldi05_threads.pdf

Lecture plan

1. Compiler optimizations
2. Barriers: kinds and flavours
3. Language memory models
   - Goals and non-goals
   - Partial memory model: bad things can not be expressed
   - Partial memory model: bad things should be avoided
   - Strict consistency: GIL
   - Strict consistency: Event Loop
   - Partial memory model: threading as a service
   - Partial memory model: concurrency-aware language subset
   - Memory model: concurrency embedded into language
4. Advanced topics
   - Visibility
   - Volatile
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Inventing reads

```
static int a;
void foo_1() {
  while (true) {
    int tmp = a;
    if (tmp == 0) break;
    do_something_with(tmp);
  }
}
```

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Could compiler use less registers for intermediate operations?

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}
```

```
static int a;
void foo_2() {
  while (true) {

    if (a == 0) break;
    do_something_with(a);
  }
}
```

Could compiler use less registers for intermediate operations?

Removing reads

```
static int a;
void foo_1() {
  while (true) {
    int tmp = a;
    if (tmp == 0) break;
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  }
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```

Removing reads

```
static int a;
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  }
}
```

Could compiler avoid repated memory loads?

Removing reads

```
static int a;
void foo_1() {
  while (true) {
    int tmp = a;
    if (tmp == 0) break;
    do_something_with(tmp);
  }
}
```

```
static int a;
void foo_2() {
  int tmp = a;
  if (tmp != 0)
    while (true) {
      do_something_with(tmp);
    }
}
```

Could compiler avoid repated memory loads?

Removing reads

```
static int a;
void foo_1() {
  while (true) {
    int tmp = a;
    if (tmp == 0) break;
    do_something_with(tmp);
  }
}
```

x86-64 clang 16.0.0 -O2[2]
x86-64 gcc 13.1 -O2[3]

```
foo_1:
    push    rbx
    mov     ebx, [a]
    test    ebx, ebx
    je      .LBB1_2
.LBB1_1:                            #<-/
    mov     edi, ebx                #  /
    call    do_something_with       #  /
    jmp     .LBB1_1                 #--/
.LBB1_2:
    pop     rbx
    ret
```

[2] https://godbolt.org/z/99j3erzaE
[3] https://godbolt.org/z/fxzGEo1qf

Load hoisting

```
static int a;
void foo_1(bool c, int r1) {
  if (c) {
    r1 = a;
  }
}
```

```
static int a;
void foo_2(bool c, int r1) {
  int t = a;
  r1 = c ? t : r1;
}
```

CSE over lock

```
static int a;
void foo_1(bool c, int r1, int r2) {
   r1 = a;
   lock();
   r2 = a;
}
```

```
static int a;
void foo_2(bool c, int r1, int r2) {
   r1 = a;
   lock();
   r2 = r1;
}
```

Load hoisting + CSE over lock

```
static int a;
void foo_1() {
   if (c) {
     r1 = a;
   }
   lock();
   r2 = a;
}
```

```
static int a;
void foo_2() {
   int t = a;
   r1 = c ? t : r1;
   lock();
   r2 = a;
}
```

```
static int a;
void foo_3() {
  int t = a;
  r1 = c ? t : r1;
  lock();
  r2 = t;
}
```

Load hoisting + CSE over lock

```
static int a;
void foo_1() {
   if (c) {
     r1 = a;
   }
   lock();
   r2 = a;
}
```

```
static int a;
void foo_2() {
   int t = a;
   r1 = c ? t : r1;
   lock();
   r2 = a;
}
```

```
static int a;
void foo_3() {
  int t = a;
  r1 = c ? t : r1;
  lock();
  r2 = t;
}
```

When `c == false`, **a** is moved out of the critical region![4]

[4] https://people.mpi-sws.org/~viktor/slides/2017-09-concur.pdf

Compiler: friend or foe?

Various optimizations of plain memory accesses

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- invent reads or writes

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make concurrent reasoning almost impossible

- no **linearizability**
- no **coherence**
- no **eventual visibility** (a.k.a. **progress**)

Taming compiler optimizations

Compiler reorders language-level constructs

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- do not reorder **this** and **that** operation (low-level consistency)

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We need to inform compiler that some invariants are important for multi-threaded execution:

- do not reorder **this** and **that** operation (low-level consistency)
- do not move operations out of critical sections (high-level consistency)

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We have already encountered such problems with reorderings of memory effects, remember?

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Barriers taxonomy: here we go again

Simplified taxonomy of barriers[5]:

- `Store_Store`, `Store_Load`, `Load_Store`, `Load_Load`

```
int x = static.data1;
Store_Store();
Store_Load();
int y = static.data2;
static.data3 = 17;
```

```
int x = static.data1;
Load_Load();

int y = static.data2;
static.data3 = 17;
```

[5] Could be misleading https://shipilev.net/blog/2016/close-encounters-of-jmm-kind/

Compiler barriers

```
int x, y;
void foo1() {
        x = 1;
        y = 2;
        x = 3;
}
```

```
int x, y;
void foo2() {
        x = 1;
        barrier();
        y = 2;
        x = 3;
}
```

Compiler barriers

```
int x, y;
void foo1() {
      x = 1;
      y = 2;
      x = 3;
}
```

```
foo1:
    mov [y], 2
    mov [x], 3
    ret
```

```
int x, y;
void foo2() {
      x = 1;
      barrier();
      y = 2;
      x = 3;
}
```

```
foo2:
    mov [x], 1
    mov [y], 2
    mov [x], 3
    ret
```

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      y = 2;
      x = 3;
}
```

```
foo1:
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    ret
```

```
int x, y;
void foo2() {
      x = 1;
      barrier();
      y = 2;
      x = 3;
}
```

```
foo2:
    mov [x], 1
    mov [y], 2
    mov [x], 3
    ret
```

Warning: avoid such low-level tricks in modern programming languages![6]

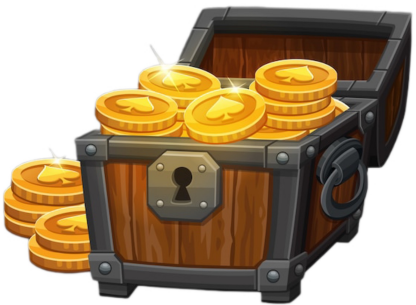
[6] https://preshing.com/20120625/memory-ordering-at-compile-time/

Question time

Question:

- `mov [x], 1`
- `mov [y], 2`
- `mov [x], 3`

Name hardware-level optimizations that will "reorder" these memory operations.



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- current CPU will "emulate" execution of single-threaded program "as if" in program order
- single memory cell is **coherent**
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Compiler

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- optimizations do not violate single-threaded behaviour
- some language constructs are **special** (e.g. `synchronized`)
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Looks like problem is already solved!

Reorderings: everywhere

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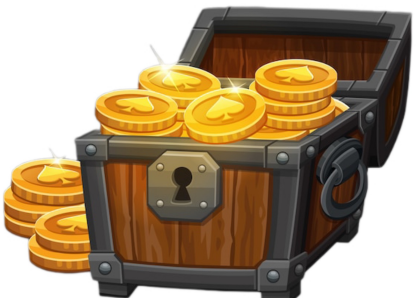
Looks like problem is already solved!

Reasoning about memory locations/compiler optimizations is mundane, complex and fragile, shouldn't we use something better?

Question time

Question: Barriers enforce ordering of operations. But compiler could "invent" or "remove" operations which will break some concurrent invariants. What should we do?



Consistency of memory operations in concurrent environment: challenges

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We need language memory model

Lecture plan

Language Memory Model

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- How to formalize it?
  - Documentation in human language
  - Machine-readable format
  - Executable algorithm
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There is no *perfect* programming language.
Any language tries to be *performant*, *safe*, *user-friendly*, *stable* ...

Lecture plan

No man, no problem

Concurrency is complicated only when we have non-trivial communication

- via shared memory locations
- via concurrent primitives

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Is it about *language* or *programming style*?

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- Overheads for creation of large data structures
- "Publish" data structure for all threads == write to shared memory location

Declarative DSL

java.util.stream[7]

```
int sumOfWeights = widgets.parallelStream()
                          .filter(b -> b.getColor() == RED)
                          .mapToInt(b -> b.getWeight())
                          .sum();
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Implementations of such DSL are concurrently writing to shared memory locations.

Actor model

Programming model with no shared state[8].

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Programming model with no shared state[8].
All computational agents (lightweight processes) are independent and communicate via message passing.

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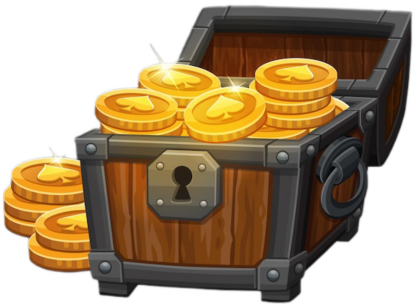
Question time

Question: Name your favourite concurrent message-passing protocol



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Lecture plan

Be in Sync or Die Tryin

Swift[11]

> *Concurrent write/write or read/write access to the same location in memory generally remains undefined/illegal behavior, unless all such access is done through a special set of primitive atomic operations.*

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```
import Foundation
class Bird {}
var S = Bird()
let q = DispatchQueue.global(qos: .default)
q.async { while(true) { S = Bird() } }
while(true) { S = Bird() }
```

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Concurrent writes are violating naive implementation of automatic reference counting[12,13]. Program crashes with `double free or corruption`.

[11] https://github.com/apple/swift-evolution/blob/main/proposals/0282-atomics.md
[12] https://tonygoold.github.io/arcempire/
[13] https://github.com/apple/swift/blob/main/docs/proposals/Concurrency.rst

Lecture plan

Mutex-based strict consistency

Strict consistency – all operations happens atomically and have total order[14].

[14] https://en.wikipedia.org/wiki/Consistency_model#Strict_consistency

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```
void thread1() {

  foo();


  bar();

}
```

```
void thread2() {

  baz();


  foo();

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```

Mutex-based strict consistency

Strict consistency – all operations happens atomically and have total order.

```
void thread1() {
  lock();
  foo();
  unlock();
  lock();
  bar();
  unlock();
}
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void thread2() {
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  baz();
  unlock();
  lock();
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}
```

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```
void thread1() {
  GIL.lock();
  foo();
  GIL.unlock();
  GIL.lock();
  bar();
  GIL.unlock();
}
```

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void thread2() {
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Global mutex guards every "instruction"

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Language do have threads[16], they are "concurrent but not parallel"
GIL is technical decision that may highly influence the whole ecosystem

- Alternative language implementations[17]
- Memory model[18]
- Interoperability with other languages[19]

[15] https://en.wikipedia.org/wiki/Global_interpreter_lock
[16] https://docs.python.org/3/library/threading.html
[17] https://doc.pypy.org/en/latest/faq.html#does-pypy-have-a-gil-why
[18] https://peps.python.org/pep-0583/
[19] https://peps.python.org/pep-0703/

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  Each job is processed completely before any other job is processed. This offers some nice properties when reasoning about your program, including the fact that whenever a function runs, it cannot be preempted and will run entirely before any other code runs (and can modify data the function manipulates).

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[23] https://developer.mozilla.org/en-US/docs/Web/JavaScript/Reference/Global_Objects/SharedArrayBuffer
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As soon as you have concurrent access – you immediately encounter "serious" problems[25]

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[24] https://developer.mozilla.org/en-US/docs/Web/JavaScript/Reference/Global_Objects/Atomics

[25] "Repairing and Mechanising the JavaScript Relaxed Memory Model" https://arxiv.org/abs/2005.10554

Lecture plan

Threads as a library

C/C++ before C++11[26]

[26] https://en.wikipedia.org/wiki/C%2B%2B11#Multithreading_memory_model

Threads as a library

C/C++ before C++11[26]

- There were no threads in language specification
  - There were libraries that implement threading
- Every project was free to invent custom designs, data structures, conventions
  - Compiler-specific
  - CPU-specific
  - OS-specific
- Any data race is undefined behaviour

[26] https://en.wikipedia.org/wiki/C%2B%2B11#Multithreading_memory_model

Threads as universal library

C/C++ before concurrent specifications + POSIX threads[27]

[27] https://en.wikipedia.org/wiki/Pthreads

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> *The Pthreads specification prohibits races, i.e. accesses to a shared variable while another thread is modifying it. ... the problem here is that whether or not a race exists depends on the semantics of the programming language, which in turn requires that we have a properly defined memory model. Thus this definition is circular.*

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Part of a **language**, not just a library!

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Specify subset of programming language that provides consistent multithreaded execution.

- C/C++ atomics
- Swift/ObjC NSLocking
- Java-1996 volatile

Part of a **language**, not just a library!
Not that easy to do: "The Java Memory Model is Fatally Flawed" , William Pugh, 2000[31]

[31] http://www.cs.umd.edu/~pugh/java/broken.pdf

Lecture plan

Formal language memory model

Mathematics to the max

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- An action a is described by a tuple $\langle t, k, v, u \rangle$ comprising ...

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- Adaptation to h/w models[32]

[32] "JSR-133 Cookbook for Compiler Writers" https://gee.cs.oswego.edu/dl/jmm/cookbook.html

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- Every data race is specified: allowed and forbidden outcomes

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- Causality requirements, circular happens-before, out-of-thin-air problem
- Adaptation to h/w models[32]
- Every data race is specified: allowed and forbidden outcomes

Few problems

- Complicated, takes a lot of time, expensive to maintain
- Not ideal[33]
- Hard to explain, hard to use in practice

[32] "JSR-133 Cookbook for Compiler Writers" https://gee.cs.oswego.edu/dl/jmm/cookbook.html

[33] "Java Memory Model Examples: Good, Bad and Ugly" https://groups.inf.ed.ac.uk/request/jmmexamples.pdf

Formal Memory Models: useful?

Goals of our 1-semester introductory course to concurrency

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- Show how to write
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  - **understandable**
  - performant

  concurrent code

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- Study state-of-the art concurrency

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- Study state-of-the art concurrency
- Achieve top performance in our concurrent programs

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Non-goals

- Look smart and mathematically inclined
- Study state-of-the art concurrency
- Achieve top performance in our concurrent programs

Studying concurrent consistency, proving theorems on Lecture 6 and Lecture 7, analyzing cache coherence was enough.

Patterns

Doug Lea, private communication with Aleksey Shipilev, 2013[34]

> *The best way to build up a small repertoire of constructions that you know the answers for and then never think about the JMM rules again unless you are forced to do so! Literally nobody likes figuring things out from the JMM rules as stated, or can even routinely do so correctly. This is one of the many reasons we need to overhaul JMM someday.*

[34] Citation from https://shipilev.net/blog/2014/jmm-pragmatics, slide 109

Concurrent patterns

Could be found in books

- "Java Concurrency in Practice"
- "Effective Java"
- "The Art of Multiprocessor Programming"
- "Is Parallel Programming Hard, And, If So, What Can You Do About It?"

Could be found in documentation `java.util.concurrent`
We studied this

- `Lock, Condition` (Lecture 2)
- advanced concurrent primitives (Lecture 3)
- producer-consumer, load balancing, partitioning, replication (Lecture 3 and Lecture 4)

Lecture plan

Visibility

```
class Data { long x; }
static Data shared;
void threadA() {
  Data d = new Data();
  d.x = 42;
  shared = d;
}
void threadB() {
  System.out.println(shared.x);
}
```

Visibility

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Do you see race condition that prevents `threadB` from printing integer?

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```

Do you see race condition that prevents `threadB` from printing integer?
`NullPointerException`

Visibility

```
class Data { long x; }
static Data shared;
void threadA() {
  Data d = new Data();
  d.x = (1L << 40) + 1;
  shared = d;
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```

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```

- Could program print 1?

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- Could program print 1?
- Could program print 1099511627776 ($1 \ll 40$)?

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- Could program print 1099511627777?

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```

- Program prints 0
- Explain this using some hardware optimization
  - store buffering, load buffering, invalidate queue, interconnect topology

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  d.x = 42;
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```

- Program prints 0
- Explain this using some compiler optimization

Visibility: trust nobody

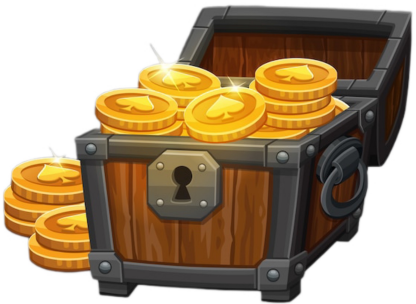
Non-synchronized concurrent access to any memory location

- Static field
- Instance field
- Array element

could lead to subtle and hard-to-diagnose bugs.

Question time

Question: Which Java-specific concepts help you to avoid visibility problems?



Visibility: trust friends only

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could lead to subtle and hard-to-diagnose bugs.
Synchronization operations:

- `Thread.start`, `Thread.join`
- `Lock.lock`, `Lock.unlock` and other `java.util.concurrent` primitives
- `synchronized`
- `AtomicLong`, `AtomicReference` read-modify-write operations

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By default[35] they act as full barrier

[35] Consult with javadoc first

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By default[35] they act as full barrier and as a linearization point

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Lecture plan

Using memory location as synchronization point

```
class LockPreReservedByB { boolean busy = true; }
static LockPreReservedByB lock; static Data data;
void threadA() {  while (lock.busy) { /*await*/ } // lock.lock()
                  Data x = data;
}
void threadB() {  Data d = new Data(); d.x = 42;
                  data = d;
                  lock.busy = false; // lock.unlock()
}
```

Using memory location as synchronization point

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}
```

We need

- `Lock.unlock` to act as publishing memory barrier (store release)
- `Lock.lock` to repair consistency of data being read (load acquire)
- all operations with `lock.busy` to be ordered (linear order)

Using memory location as synchronization point

Roach motel idiom[36]

```
int a; volatile boolean ready = false;
void threadA() {
  a = 41;
  a = 42;
  ready = true; // release data. Every write above will be visible (flushed)
  a = 43;
}
void threadB() {
  while (!ready) {} // acquire data. Every read below will see up-to-date data
  println(a);
}
```

[36] https://shipilev.net/talks/narnia-2555-jmm-pragmatics-en.pdf

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  println(a);
}
```

Possible to see 42 or 43. Impossible to see 0 or 41.

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Volatile

`volatile` variable

- `volatile` mode accesses are totally ordered
  - coherence, visibility (progress)
- not a plain variable, enforces some ordering with other locations
  - load acquire, store release
- not an atomic read-modify-write variable, does not provide full barrier semantics

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- advanced protocols
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Very Java-specific

- `volatile` in C/C++ is **absolutely different**
- `memory_order_acq_rel` in C/C++ is **subtly different** from Java `volatile`
- many languages are OK with plain variables and full-fence variables
- low-level languages allow to use atomic RMW variables with different "strength"

Volatile: rules of thumb

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volatile boolean asleep;
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- the variable does not participate in invariants with other state variables
- locking is not required for any other reason while the variable is being accessed

Summary

Compiler optimizations

- reorder/invent/delete memory operations, prevent it via compiler barriers

Language memory model – bridge between

- chaos of hardware, anarchy of compiler optimizations
- consistency requirements for high-level concurrent algorithms

Useful concepts

- immutability
- DSL for parallel computations
- strict consistency via mutex
- strict consistency via single executor and cooperative multitasking
- threads cannot be implemented as a library
- language memory model is harder to formalize than hardware memory model
- visibility is subtle but critically important
- `volatile` is for hackers

The most efficient and elegant approach to writing concurrent code

https://go.dev/ref/mem

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Don't be clever