

# MIPI Alliance Test Program

D-PHY Physical Layer  
Conformance Test Suite  
*Version 1.00*

*Technical Document*  
*MIPI Confidential*



**NOTICE: This is a living document. Contents are subject to change in subsequent releases,  
as incremental refinements/improvements are made, and supplemental material is added.  
To check for the latest version, always refer to the [MIPI Alliance Testing Page](#)**

*Last Updated September 16, 2010*

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## MODIFICATION RECORD

2010 Sep 16 (v1.00) Final incremental update. First v1.0 release.

Andy Baldman: Entire document: Removed 'NEW' and 'Prev.' indicators from titles of all tests whose test numbers have not changed since the previous revision.

### SECTION 1: (TX TESTS):

Section 1, Group 1 Title Page: Added paragraph to Overview stating that this Group is typically only performed for Master DUTs.

Section 1, Group 2 Title Page: Added paragraph to Overview stating that this Group is N/A for Slave DUTs.

Section 1, Groups 3+4+5 Title Pages: Added statement to Overview stating that Group is N/A for Slave DUTs.

Section 1, Group 6 Title Page: Added paragraph to Overview stating applicability for each test in the group.

All 1.1.x Tests: Changed all Procedures to specify using ULPS Entry sequence.

Test 1.1.6+1.1.7: Fixed major typo/goof-up where maximum trip-level threshold was previously incorrectly calculated/stated in 1.1.6 as "880+50=850mV", instead of 930mV. All references to the 850mV trip level in 1.1.6 and 1.1.7 have been corrected to 930mV. Also, added comments to Possible Problems regarding glitches caused by noise on the input waveforms.

Test 1.1.6: Added clarification that a 'pulse' is defined as rising edge to falling edge.

Tests 1.1.5+1.2.5: Modified methodology so final slew rate results are now averaged over all measured edges (as opposed to reporting the peak measured values as the final result.) Also, changed 1.1.5 Discussion to use a horizontally centered sliding window. Also cleaned up and expanded 1.1.5 Discussion to more clearly describe the separate measurements that are performed for the rising and falling edges. Cleaned up and synchronized both Procedure sections to more clearly show the 2 falling edge and 3 rising edge measurements. Added informative provision to repeat all measurements with the CLOAD board removed, to get a sense of the DUT PCB's CLOAD contribution.

Tests 1.2.1/2/4/5: Modified Discussion and Procedure sections to specify using the Clock ULPS Entry sequence for all measurements (and prohibit using HS Entry.)

Tests 1.2.3: Modified procedure to specify using Clock ULPS Exit sequence.

Test 1.3.4: Added a paragraph to Possible Problems explaining that averaging should be performed starting with the end of the burst (and worked backwards), rather than from the front of the burst.

Test 1.3.5: Added note to Possible Problems pointing to Possible Problems of Test 1.3.4.

Tests 1.3.6+1.4.6: Changed Data/Clock VOHHS methodologies to use the same reference pulse-based approach as 1.3.4/1.4.4 (Data/Clock VOD).

Tests 1.3.7+1.4.7: Added specification that measurements be performed over at least 5K UIs each.

Tests 1.3.11+1.3.12: Updated figures with better looking versions.

Test 1.3.13: Added new observable result to verify that the THS-TRAIL state is actually inverted.

Test 1.4.1: Improved wording/language of Possible Problems section.

Test 1.4.4+1.4.11: Changed minimum averaging factor from 5000 to 128, to be consistent with respective Data Lane pulse-based tests. (Note: This change also applies to Test 1.4.12, however the test description didn't need to be modified, as it just references 1.4.11.)

Test 1.4.4: Updated figures with better looking versions. Added note to Possible Problems pointing to Possible Problems of Test 1.3.4.

Test 1.4.5: Added note to Possible Problems pointing to Possible Problems of Test 1.3.4.

Test 1.4.6: Added note to Possible Problems pointing to Possible Problems of Test 1.3.4.

Test 1.4.11: Updated figure with better looking version. Added note to Possible Problems pointing to Possible Problems of Test 1.3.4.

Test 1.4.12: Added figure showing example measurement. Added note to Possible Problems pointing to Possible Problems of Test 1.3.4.

Test 1.4.13: Added new observable result to verify that the TCLK-TRAIL state is actually HS-0. Also added note to Possible Problems pointing to Possible Problems of Test 1.4.1.

Test 1.4.14: Replaced missing Possible Problems section, and added a note pointing to Possible Problems of Test 1.4.1.

Test 1.4.15: Added note pointing to Possible Problems of Test 1.4.1.

Test 1.4.16: Added note to Discussion stating that test is N/A for continuous-clocking DUTs.

Test 1.4.17: Changed minimum population size from 10K to 5K UIs.

Test 1.5.3: Removed comment from Discussion about using a persistence capture to observe multiple bursts, and added a new figure showing an example measurement.

Test 1.6.1: Added paragraph to discussion stating that this test may be N/A for some DUT types.

Test 1.6.3: Added paragraph to discussion stating that this test may be N/A for some DUT types.

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## SECTION 2: (RX TESTS)

Test 2.1.3: Changed Discussion and Procedure sections to use a ULPS Entry + ULPS Exit + HS Burst as the test sequence, and use reception of the HS Burst data as the observable. (Also added a note regarding using ULPS signal pins as the observable for some PPI-based bare-phy DUTs.)  
Test 2.1.4: Completely overhauled Discussion and Procedure sections, writing mostly all new material. (Defined two different hysteresis methodologies, a Static method, primarily intended for bare-phy and Host DUTs, and a second Dynamic method, mainly for DSI panels.) Also, added test cases to measure hysteresis for VIH and VIL separately. (Previous test only measured VIH).  
Test 2.1.6: Modified procedure slightly so that glitches are added/tested on all Lanes simultaneously.  
Test 2.1.8: Fixed typo regarding ErrContentionLP0 signal. Added note saying all contention events should last at least 1 TLPX length. Added comment about needing to manually observe/verify contention voltages appearing on line, due to DUT LP-TX impedance. Added note saying test is N/A for unidirectional DUTs. Split test case 1 into two cases (1a and 1b) to separately verify LP/LP and LP/HS instances of LP High Fault.  
Test 2.2.1: Added paragraph to discussion stating that this test may be N/A for some DUT types.  
Test 2.2.3: Added a third test case to verify that the Clock Lane will ignore a Data Lane ULPS Entry sequence.  
Tests 2.4.4+2.4.9: Fixed typos in Tables 2.4.4-1 and 2.4.9-1, where Case 2 in both tables incorrectly stated 40ns instead of 60ns. (Typos were only in tables, as values in Discussion were always correct.)  
Test 2.4.5: Fixed typo in Discussion that incorrectly said the minimum THS-TRAIL of 40ns+4\*UI would be used. (The proper value is 60ns+4\*UI.) Also, changed the exact extra data byte that is used to be the same pattern used for THS-SETTLE. Also, added paragraph to discussion stating that this test may be N/A for some DUT types. Also, modified test so verification of the upper THS-SKIP conformance limit is informative. (Lower limit is still normative.)  
Test 2.4.8: Revised Discussion and Procedure sections with a different methodology that simply checks a single case where false clock transitions are present at the beginning of TCLK-ZERO.  
Test 2.4.10: Removed note describing possible alternate measurement method, which wasn't feasible.

## SECTION 3: (S-PARAMETER/IMPEDANCE TESTS):

Changed name of Group 3 from 'Low Frequency Impedance Requirements', to 'LP-TX/RX Impedance Requirements'.  
Test 3.2.1: Updated Figure 3.2.1-1 to the correct version from the v1.0 D-PHY spec (which has different limits.)  
Test 3.3.1: Corrected typo in Procedure. (3<sup>rd</sup> and 2<sup>nd</sup> to last procedure steps accidentally said 'Logic-Low' instead of 'Logic-High'.) Also, revamped terminology so ZOLP(0) and ZOLP(1) now have different names. Also added paragraph to Possible Problems stating how this test is typically only performed for Master DUTs.  
Test 3.3.2: Added paragraph to Possible Problems stating how this test is typically only performed for Slave DUTs.

## APPENDICES:

Appendix A: Added picture of Reference Termination Board (RTB)  
Appendix I: Cleaned up appendix contents, and clarified all spec references.

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2009 Nov 30 (v0.98) Major incremental update. First release based on final approved v1.00 D-PHY spec.

Andy Baldman: Entire document: Removed 'NEW' and 'Prev.' indicators from titles of all tests whose test numbers have not changed since the previous revision.

Acknowledgements: Added Thomas Marik (Agilent), Takuya Otani (Agilent), Laurent Claramond (ST), Steve Kwiatkowski (ST), Rajkumar Nagpal (ST), and Carl Poirier (National) to acknowledgements page.

Changed name of Section 1 Group 3 from 'Data Lane HS-TX Burst Signaling Requirements' to 'Data Lane HS-TX Signaling Requirements', to be consistent with Section 1 Group 4.

Test 1.1.1: Removed option from Discussion allowing test to be performed on a static LP-11 state, and recommended that a ULPS Entry sequence be used. Added requirement that the test be performed for both CLOAD test cases. Also added a picture showing an example measurement, and added paragraph under 'Possible Problems' with recommendations.

Test 1.1.2: (Modified to reflect same changes per 1.1.1.)

Test 1.1.3: Added discussion regarding max/min CLOAD test cases. Modified procedure to include max and min CLOAD cases. Added figure showing example rise time measurement.

Test 1.1.4: (Modified to reflect same changes per 1.1.3.)

Test 1.1.5: Complete overhaul. Updated to reflect new slew rate limits of D-PHY v1.00. Changed procedure to only test the 70pF CLOAD requirements.

Test 1.1.6: Removed nominal trip-level threshold test case (675mV), and added provision for test to be performed both with and without the maximum CLOAD test fixture.

Test 1.1.7: Changed measurement to be performed at both trip levels and both CLOAD cases, to be consistent with Test 1.1.6.

Tests 1.2.1+2: Added requirement for both CLOAD cases (to match 1.1.1+2).

Tests 1.2.3+4: Added requirement for both CLOAD cases (to match 1.1.3+4).

Test 1.2.5: Applied same changes as to 1.1.5.

Test 1.3.1: Added short comments to 'Possible Problems' section explaining how to connect the RTB for DUTs with 3 or 4 Data Lanes.

Test 1.3.2: Fixed incorrect reference to HS UI test (1.4.17), and added comment to Possible Problems.

Test 1.3.3: Added pointer to Possible Problems section of 1.3.1.

Test 1.3.4: Completely rewrote methodology to use reference-pulse-based approach, with averaging. Also added test cases for all three ZID values. Also added comments under Possible Problems explaining the sensitivity of this measurement, and ways to improve accuracy.

Test 1.3.5: Modified to add test cases for all three ZID values.

Test 1.3.6: Added informative paragraph to Discussion explaining relationship of VOD, VCMTX, and VOHHS (which was previously a red-text informal note). Also, modified procedure to add test cases for all three ZID values, and added pointer to Possible Problems section of 1.3.1.

Test 1.3.7: Fixed incorrect figure number. Added figure showing sample measurement. Added test cases for all three ZID values.

Test 1.3.8: Added test cases for all three ZID values.

Test 1.3.9: Fixed incorrect figure number. Added pointer to Possible Problems section of 1.3.1.

Test 1.3.10: Added pointer to Possible Problems section of 1.3.1.

Test 1.3.11+12: Completely rewrote methodology to use reference-pulse-based approach similar to Test 1.3.4. Also added test cases for all three ZID values. Added pointer to Possible Problems section of 1.3.4.

Test 1.3.13: Clarified that the measurement is only performed for ZID = 100 ohms. Added pointer to Possible Problems section of 1.3.1.

Test 1.3.14: Clarified that the measurement is only performed for ZID = 100 ohms. Added pointer to Possible Problems section of 1.3.1.

Test 1.3.15: Fixed incorrect reference number (typo).

Test 1.3.16: Clarified that the measurement is only performed for ZID = 100 ohms. Replaced figure with appropriate figure showing Data Lane example. Added pointer to Possible Problems section of 1.3.1. Also, added discussion under Possible Problems explaining that THS-EXIT need not be explicitly measured in all cases, provided that it can be shown that no bursts violate the minimum 100ns conformance limit.

Tests 1.4.1/2/3: Removed note stating that these tests didn't apply to continuous-clocking devices. (As these tests do apply, as continuous-clocking devices are still required to perform a single valid Clock Lane HS entry sequence upon initialization.) Also clarified that these tests are only performed for ZID = 100 ohms.

Test 1.4.1: Added comments to 'Possible Problems' explaining the measurement for continuous-clocking devices.

Test 1.4.2/3: Added pointer to Possible Problems section of Test 1.4.1.

Test 1.4.4: Completely rewrote methodology to use a reference pattern-based approach, similar to Test 1.3.4, but with a different reference pattern (01/10). Also added test cases for all three ZID values.

Test 1.4.5: Added test cases for all three ZID values.

Test 1.4.6: Added test cases for all three ZID values.

Test 1.4.7: Deleted most of Discussion and replaced with a pointer to Test 1.3.7 (Data Lane test). Added test cases for all three ZID values.

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Test 1.4.8: Added test cases for all three ZID values.

Test 1.4.9: Deleted most of Discussion and replaced with a pointer to Test 1.3.9 (Data Lane test). Added clarification that test is only performed for ZID = 100 ohms.

Test 1.4.10: Deleted most of Discussion and replaced with a pointer to Test 1.3.10 (Data Lane test). Added clarification that test is only performed for ZID = 100 ohms.

Test 1.4.11/12: Completely rewrote methodology to use reference pattern-based approach. Added test cases for all three ZID values.

Test 1.4.13/14/15: Added note stating that this test is similar to the Data Lane case. Added clarification that test is only performed for ZID = 100 ohms.

Test 1.4.16: Added note stating that this test is similar to the Data Lane case. Added clarification that test is only performed for ZID = 100 ohms. Added comment under Possible Problems to point to the Possible Problems comments for Test 1.3.16.

Test 1.4.17: Cleaned up Discussion and added appropriate spec references (which were missing). Added requirement that measurement be performed over at least 10,000 UIs. Added requirement that the minimum stated UI value be obtained from the vendor prior to performing the test, and added a requirement that the measured values be verified against this limit. Also added clarification that the mean UI value be recorded, for use in computing conformance ranges for other parameters that are defined in terms of UI.

Test 1.5.1: Removed statement that said test was only applicable to DUTs that support burst-mode clocking, as the test can technically be performed on the initial HS entry sequence for a continuous-clocking DUT. Added clarification that test is only performed for ZID = 100 ohms. Added comments to Possible Problems.

Test 1.5.2: Added clarification that test is only performed for ZID = 100 ohms. Added comments to Possible Problems.

Test 1.5.3: Added clarification that test is only performed for ZID = 100 ohms. Added comments to Discussion regarding possible implementation approaches.

Test 1.5.4: Added clarification that test is only performed for ZID = 100 ohms. Added comments to Possible Problems.

Test 1.6.1 (prev. 3.1.1): Modified Procedure to test all Lanes, and added comments under Possible Problems.

Test 1.6.2 (prev. 3.5.1): Added details and general polishing to Discussion and Procedure.

Test 1.6.3 (prev. 3.4.1): Modified Procedure to test all Lanes, and added comments under Possible Problems.

Tests 1.6.4, 1.6.5, 1.6.6 (prev. 3.3.3, 3.3.4, 3.3.2): Added details to Discussion and Procedure sections, for clarification. Also, added comments under Possible Problems.

### Section 2:

Test 2.1.1: Removed comment from Possible Problems about more work being needed.

Tests 2.1.1-2.1.4: Changed procedure to remove requirement to test Dp and Dn for all Lanes separately (too time consuming), and allowed all Lanes to be tested simultaneously.

Test 2.1.4: Modified Procedure to start with VOH equal to the DUT's measured VIH level + 50mV

Test 2.1.8: Created entirely new Discussion and Procedure (as none existed before).

Test 2.2.1 (prev. 3.1.2): Added further detail to Discussion.

Test 2.2.2 (prev. 3.4.2): Added further detail to Discussion.

Test 2.2.3 (prev. 3.5.2): Created entirely new Discussion and Procedure (as none really existed before).

Test 2.2.4 (prev. 3.2.1): Changed Discussion and Procedure to use ULPS command instead of Trigger/Reset. Also changed the list of test cases to eliminate sequences with LP-11 to 00 and 00 to 11 transitions, and add several new test cases.

Test 2.2.5 (prev. 3.2.2): Changed Discussion and Procedure to use ULPS command instead of Trigger/Reset.

Test 2.2.6 (prev. 3.2.3): Changed test status to INFORMATIVE. Added detail to Discussion explaining why.

Test 2.2.7 (prev. 3.2.4): Created entirely new Discussion and Procedure (as none really existed before).

Test 2.2.8 (prev. 3.2.5): Modified Discussion/Procedure to use same methodology as other Escape Mode tests.

Test 2.3.6: Deleted editorial note about adding setup and hold test cases.

Test 2.4.1 (prev. 2.2.8): Removed editorial notes.

Test 2.4.2 (prev. 2.2.9): Created entirely new Discussion and Procedure (as none really existed before).

Test 2.4.4 (prev. 2.2.11): Created entirely new Discussion and Procedure.

*(Continued on next page...)*

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### Previous Section 3: (ELIMINATED)

Eliminated old Section 3 (“INIT, Escape, BTA, and ULPS Behaviors”) entirely, mainly by re-assigning existing tests to appropriate TX (Section 1) or RX (Section 2) areas of the test suite. This provides a more logical structure, as the existing Section 3 tests were all either TX or RX-specific measurements anyway, and it didn’t make much sense to have a set of miscellaneous TX and RX tests defined in a separate section. All previous tests were reassigned to other sections, with the following exceptions:

- Eliminated previous test 3.2.6 (Esc. Mode Verification of Supported Functionality), as it was only a verification test, and provided little value for the relative complexity that would have been required.  
(Verification of supported features could be an entire separate test suite.)
- Eliminated previous Test 3.3.1 (TLPX Ratio), as this was a system-level requirement, not a component spec.

### Previous Section 4: (ELIMINATED)

Eliminated entire previous Section 4 (“Error Detection”), for the following reasons:

- The protocol watchdog timers (previously 4.2.x) are informative in the D-PHY spec, are stated in D-PHY as being protocol-specific, and are ambiguously defined in several areas.
- The Sequence Error definitions (previously 4.1.x) are optional in D-PHY, and are also covered in the DSI spec (and hence are covered in the DSI conformance test suite.) Furthermore, it has been discussed in the DSI WG that the Sequence Error specs are ambiguous and poorly defined in some cases, and are not easily testable as currently written in the DSI and D-PHY specs.

### New Section 3 (previously Section 5):

- Reassigned section number, and reordered tests. (See Table of Contents for summary of test renumbering)
- Added example measurement plot figures to most tests.
- Test 3.1.2 (prev. 5.1.2): Changed frequency range lower limit from 0Hz to fLP,MAX, per spec change.
- Eliminated old Test 5.3.2 (common-mode capacitance test), as it was found that Ccm could not be measured accurately for real devices. Until and unless a viable methodology can be identified, this test will be removed.
- Eliminated old Test 5.2.4 (Inter-Lane Matching). Uncertain if test can realistically be performed with enough precision to allow devices to pass the spec. Test removed pending further investigation. (It may be added back later, but will likely be added as an additional observable to the existing S-parameter tests.)

### Appendix A:

- Changed description of LP Capacitive Load fixture under Equipment Requirements.
- Deleted paragraph under HS Burst Mode Configurability that required DUT to source the same packet repeatedly, as DSO averaging is no longer recommended for waveform data acquisition.
- Added note to A.2 that provides a pointer to Appendix G.
- Added comments to A.4 about requirements for LP impedance measurements.
- Deleted A.5 section placeholder as it was no longer needed.

### Appendix B:

- Modified Figure B-1-1 to show only two probes, and new CLOAD fixture.
- Added new section B.1.3 (with figure) to show BTA test setup.

### Appendix C:

- Replaced previous placeholder for ‘test applicability’ appendix with an entirely new appendix that defines the master RX test sequence. (The test applicability appendix may still be added in a future revision as a separate new appendix.)

### Appendix H:

- Renamed previous Appendix H (Vendor DUT Pre-Test Checklist) to Appendix I.
- Created new Appendix H for Automation Software Interface.

2009 Jan 13 (v0.08) Incremental update, to revise Appendix D reference RX/interop test pattern based on WG feedback.

Andy Baldman: Entire document: Removed ‘NEW’ and ‘Prev.’ indicators from titles of all tests whose test numbers have not changed since the previous revision.

Appendix D: Created entirely new appendix based on 8-bar test pattern (to replace previous 6-bar pattern).

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2008 Oct 23 (v0.07) Major incremental update. (Additions to TX tests, major RX test updates, and several major appendix updates.)

Andy Baldman: Entire document: Removed ‘NEW’ and ‘Prev.’ indicators from titles of all tests whose test numbers have not changed since the previous revision.

Added new Test 1.3.15 for Data Lane TEOT (as Clock Lane test already existed in Group 4, but Data Lane test was missing in Group 3). Also, renumbered previous 1.3.15 (THS-EXIT) to 1.3.16.

Added new Test 1.4.14 for Clock Lane TREOT (as one existed already for Data Lane, but Clock Lane test was missing). Also renumbered previous tests 1.3.14/15/16 to 1.3.15/16/17, respectively.

Tests 2.1.1, 2.1.2, 2.1.3: Added major refinements/information to Discussion, Test Procedure, and Possible Problems Sections, based on recent insights gained from performing these tests on various DUT types.

Test 2.1.4: Created new Discussion and Procedure sections for VHYST test.

Tests 2.1.5 and 2.1.6: Created new Discussion and Procedure sections for TMIN-RX and eSPIKE tests, and also swapped numbering of tests, putting TMIN-RX before eSPIKE, as the eSPIKE methodology requires some information from the TMIN-RX test, which must be performed first.

Test 2.1.7: Created Discussion and Procedure sections for LP RF Interference Tolerance test.

Deleted Test 2.2.6 (VTERM-EN), and renumbered previous Tests 2.2.7, 2.2.8 to 2.2.6, 2.2.7 respectively.

Assigned T\_D-TERM-EN test (previously 2.2.x) a formal test number (2.4.1).

Assigned T\_HS-SKIP test (previously 2.2.x) a formal test number (2.2.9).

Assigned T\_CLK-TERM-EN test (previously 2.2.x) a formal test number (2.2.10).

Assigned T\_CLK-MISS test (previously 2.2.x) a formal test number (2.2.11).

Tests 2.2.1 to 2.2.11: Overhauled all tests with expanded Discussions, new test cases, and updated Procedures.

Assigned Clock-Data Skew test (previously x.x.x) a formal test number (2.2.12), and created new extensive test description. Also, changed the test name to “HS-RX Setup/Hold and Jitter Tolerance”, to better reflect the fact that the RX timing requirements are defined in terms of setup/hold, rather than ‘skew’, which generally used to describe the transmitter spec.

Appendix A: Changed DSO and Probe BW requirements from 6GHz to 4GHz.

Appendix B: Removed direct SMA/DSO connection option for TX tests. Created separate new diagrams for LP and HS TX tests. Added new setup diagrams for RX and TDR tests.

Appendix F: Completed documentation for statistical BER test methodology.

Appendix G: Created new appendix to discuss the RX test observables options for different DUT types.

Appendix H: Created new appendix to capture all of the requirements vendors are required to specify for devices. (This will eventually become a form that will need to be provided to testing entities upon submission of DUTs.)

2008 Sep 12 (v0.06) Major update for Lisbon F2F. (Mostly TX updates, with some RX. Additional RX updates to follow shortly...)

Andy Baldman: Acknowledgements Page: Added Jennifer Lampert (ADI) and Jim Ohannes (National).

Section 1, Group 1: Modified all Procedures to repeat LP tests on all Data Lanes.

Section 1: Added new Group (Group 2) for Clock Lane LP tests. Renumbered previous Groups 2, 3, and 4 to Groups 3, 4, and 5, respectively.

Section 1: Added new test (Test 1.4.1) for Clock Lane  $T_{LPX}$  measurement.

Section 1: Renumbered Clock Lane HS-TX tests to mirror Data Lane tests, and put one additional Clock Lane test (UIINST test) at end of Group 4.

Section 1: Deleted the two ‘Setup/Hold times at Receiver’ tests (original tests 9.1.4 and 9.1.5), as they were erroneous, in that they are RX requirements, not TX requirements. They will effectively be addressed by the RX skew/jitter tests.

Section 2, Group 2: Added temporary notes to several tests noting new test cases that have been successfully performed, but still need to be formally written up.

Section 2, Group 2: Added placeholder for forthcoming RX Skew/Jitter tolerance test.

Added new Appendix D for reference RX test pattern.

Added new Appendix E for Logic Analyzer trigger setup for using LA as a BER error counter, for RX conformance and bare D-PHY interop testing.

Added new Appendix F placeholder for RX/System BER test methodology.

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2008 May 29 (v0.05) First ‘beta’ release (i.e., undergoing implementation).

Andy Baldman: Basically overhauled and renumbered/reorganized all tests.  
Replaced all references to ‘D-PHY Standard’ with ‘D-PHY Specification’.  
Added Appendix info regarding requirements and test setups

2007 Sep 27 (v0.03) First public draft posted to Phy WG reflector.

Andy Baldman: Cover page: Cleaned up layout. Removed IOL logo.  
Pretty much overhauled and renumbered all existing tests.  
Most Discussion sections complete.  
Consider this the first ‘official’ draft release.

2007 Sep 16 (v0.02) Draft update to sync to D-PHY v0.89.01, plus major general development (internal, never released to Phy reflector.)

Andy Baldman: Section 5: Renumbered/reorganized Section 5 tests to sync with new alphabetical order in Table 14 of v0.89.  
This included eliminating  $T_{TA-RQST}$ ,  $T_{TA-ACK}$ ,  $T_{TA-FINISH}$ , and  $T_{CLK-SETTLE}$ , and creating new  $T_{CLK-PREPARE}$ ,  $T_{EOT}$ , and  $T_{CLK-TERM-EN}$  tests.  $T_{HS-ZERO}$  test definition was combined into  $T_{HS-PREPARE}$  definition (as per spec).  $T_{CLK-ZERO}$  test definition was renamed  $T_{CLK-PREPARE} + T_{CLK-ZERO}$ .  
Section 7: Completely deleted the three Group 1 tests (channel S-parameter characteristics), as any interconnect tests would eventually be defined in a separate test suite, if ultimately needed. Wrote entirely new Group 1 and Group 2 tests for TX/RX device S-parameters, respectively.  
Section 8: Created entirely new set of Section 8 Electrical Characteristics tests.  
Section 9: Created test specifications for HS data timing.  
Appendix A: Created placeholder for resource requirements and test setups.

2007 Mar 05 (v0.1) Draft release (IOL-Internal, never posted to Phy reflector)

Andy Baldman: Initial draft release

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## **ACKNOWLEDGMENTS**

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## INTRODUCTION

The University of New Hampshire's InterOperability Laboratory (IOL) is an institution designed to improve the interoperability of standards-based products by providing a neutral environment where a product can be tested against other implementations of a common standard, both in terms of interoperability and conformance. This particular suite of tests has been developed to help implementers evaluate the **D-PHY** physical layer functionality of their **MIPI** products. This test suite is aimed at validating products in support of the work being directed by the **MIPI Alliance**.

These tests are designed to determine if a product conforms to specifications defined in the **MIPI Alliance Specification for D-PHY, Version 1.00.00– 14 May 2009** (hereafter referred to as the “D-PHY Specification”). Successful completion of all tests contained in this suite does not guarantee that the tested device will successfully operate with other MIPI products. However, when combined with a satisfactory level of interoperability testing, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many MIPI environments.

The tests contained in this document are organized in order to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are separated into groups, primarily in order to reduce setup time in the lab environment, however the different groups typically also tend to focus on specific aspects of device functionality. A three-number, dot-notated naming system is used to catalog the tests (e.g., “Test 9.3.2 – Differential Output Voltage”), where the first number indicates the section of the test suite (where sections denote major logical groupings of functionality, e.g., TX vs. RX tests, etc). The second and third numbers indicate the test’s group number and test number within that group, respectively. This format allows for the addition of future tests in the appropriate groups without requiring the renumbering of subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. Formally, each test description contains the following sections:

### Purpose

The purpose is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

### References

This section specifies all reference material *external* to the test suite, including the exact specification references for the test in question, and any other references that might be helpful in understanding the test methodology and/or test results. External sources are always referenced by a bracketed number (e.g., [1]) when mentioned in the test description. Any other references in the test description that are not indicated in this manner refer to elements within the test suite document itself (e.g., “Appendix 5.A”, or “Table 5.1.1-1”)

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**Resource Requirements**

The requirements section specifies the test hardware and/or software needed to perform the test. This is generally expressed in terms of minimum requirements, however in some cases specific equipment manufacturer/model information may be provided.

**Last Modification**

This specifies the date of the last modification to this test.

**Discussion**

The discussion covers the assumptions made in the design or implementation of the test, as well as known limitations. Other items specific to the test are covered here as well.

**Test Setup**

The setup section describes the initial configuration of the test environment. Small changes in the configuration should not be included here, and are generally covered in the test procedure section (next).

**Procedure**

The procedure section of the test description contains the systematic instructions for carrying out the test. It provides a cookbook approach to testing, and may be interspersed with observable results.

**Observable Results**

This section lists the specific observables that can be examined by the tester in order to verify that the DUT is operating properly. When multiple values for an observable are possible, this section provides a short discussion on how to interpret them. The determination of a pass or fail outcome for a particular test is generally based on the successful (or unsuccessful) detection of a specific observable.

**Possible Problems**

This section contains a description of known issues with the test procedure, which may affect test results in certain situations. It may also refer the reader to test suite appendices and/or other external sources that may provide more detail regarding these issues.

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## **REFERENCES**

The following documents are referenced in this text:

- MIPI Alliance Specification for D-PHY, Version 1.00.00 - 14 May 2009
- MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.01.00 - 21 Feb 2008

## **SECTION 1: TX TIMERS AND SIGNALING**

### **Overview:**

This section of tests verifies various TX signaling and timing requirements of D-PHY transceivers, defined in the D-PHY Specification.

Group 1 (1.1.x) verifies various requirements specific to Data Lane LP-TX signaling.

Group 2 (1.2.x) verifies various requirements specific to Clock Lane LP-TX signaling.

Group 3 (1.3.x) verifies various requirements specific to Data Lane HS-TX signaling.

Group 4 (1.4.x) verifies various requirements specific to Clock Lane HS-TX signaling.

Group 5 (1.5.x) verifies various requirements specific to HS-TX Clock-to-Data-Lane timing.

Group 6 (1.6.x) verifies various requirements specific to Initialization, ULPS, and BTA behavior.

Comments and questions regarding the documentation and/or implementation of these tests are welcome, and may be sent to [aab@iol.unh.edu](mailto:aab@iol.unh.edu).

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## **GROUP 1: DATA LANE LP-TX SIGNALING REQUIREMENTS**

### **Overview:**

This group of tests verifies various requirements specific to Data Lane LP signaling. The intent of the structure of this Group is to facilitate performing a set of related LP-TX measurements on a single Data Lane LP-TX waveform sequence (e.g., Data Lane ULPS Entry).

Note that this test Group is typically performed on CSI-2 and DSI Master devices only (e.g., camera sensors in the CSI-2 case, and host processors in the DSI case.) It can also be performed on ‘bare-phy’ DUT types. However it is not typically possible to perform this test on Slave devices (e.g., DSI displays), as the Slave’s LP-TX is only active during a Bus Turnaround event, which is not sufficient for test purposes (as the DUT cannot be connected to the required reference LP test loads *and* a link partner to initiate the Turnaround event at the same time.) This test group can be performed if a vendor-specific means exists to force a Slave device’s LP-TX into an enabled state where it can transmit the required LP test patterns, however this option is typically not available for most Slave DUTs.

### **Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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**Test 1.1.1 – Data Lane LP-TX Thevenin Output High Level Voltage ( $V_{OH}$ )**

**Purpose:** To verify that the Thevenin Output High Level Voltage ( $V_{OH}$ ) of the DUT's Data Lane LP transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.2, Line 1397
- [2] Ibid, Section 8.1.2, Table 18

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

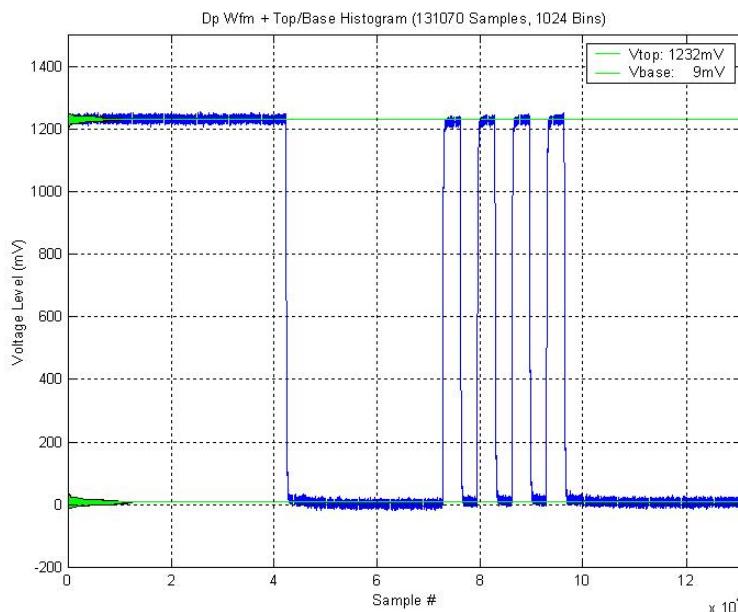
**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{OH}$ , which is a device's LP-TX Thevenin Output High Level Voltage.

The D-PHY Specification states, " $V_{OH}$  is the Thevenin output, high-level voltage in the high-level state, when the pad pin is not loaded." [1].

In this test, the DUTs Data Lane  $V_{OH}$  values will be measured using a high-speed, real-time DSO while the DUT is driving an LP signaling sequence into an open termination. (Note that this test is intended to be performed in conjunction with the other tests in this group on a single captured LP Escape Mode sequence waveform, where the measurement is performed on the output-high bits only.) For the purposes of this measurement,  $V_{OH}$  is measured as the mode of all waveform samples that are greater than 50% of the absolute peak-to-peak  $V_{DP}$  and  $V_{DN}$  signal amplitudes, and should be measured across all LP-1 states in a single LP Escape Mode sequence. (Note that a ULPS Entry sequence is specified for this test, and all other measurements in this Group, as this should normally be supported on all Data Lanes for most DUTs.) This measurement shall be performed separately on both the  $V_{DP}$  and  $V_{DN}$  waveforms, and for each Data Lane.

An example Dp waveform and measurement is shown below.



**Figure 1.1.1-1: Example Dp ULPS Waveform and  $V_{OH}/V_{OL}$  Measurement**

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Also, while the capacitive characteristics of the ‘open’ termination should not affect the static high and low levels, this test will be performed for two test cases, once with the 50pF  $C_{LOAD}$  test fixture (see Discussion, Test 1.1.3, for details), and a second time without the  $C_{LOAD}$  fixture. (Note the results are expected to be identical or nearly identical for the two cases, however the purpose of performing both cases for this test is primarily just for procedural consistency with the other LP tests in this section, as most of the other measurements are performed for both cases.)

For all Data Lanes, the value of  $V_{OH}$  for both the  $V_{DP}$  and  $V_{DN}$  signals must be between 1.1V and 1.3V in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.1.

**Test Procedure:**

- Connect the DUT to the Test Setup, using the 50pF  $C_{LOAD}$  test fixture.
- Create a condition that causes the DUT to source a ULPS Entry sequence on Data Lane 0.
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods, measure  $V_{OH}$  for both the  $V_{DP}$  and  $V_{DN}$  signals as described above.
- Repeat the previous steps with the  $C_{LOAD}$  fixture removed.
- Repeat the previous four steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For both  $C_{LOAD}$  cases, and for all Data Lanes:

- Verify that  $V_{OH}$  for the  $V_{DP}$  waveform is between 1.1 and 1.3 Volts.
- Verify that  $V_{OH}$  for the  $V_{DN}$  waveform is between 1.1 and 1.3 Volts.

**Possible Problems:**

Because the  $V_{OH}$  and  $V_{OL}$  measurements are performed as mode measurements (rather than mean), the measurement will tend to be dominated by the most popular level in the waveform capture. This will often be the ‘static’ LP-0/1 levels occurring before and after the burst of edges. Waveforms should be sure to include these sections of data in order to ensure the most stable and repeatable results.

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**Test 1.1.2 – Data Lane LP-TX Thevenin Output Low Level Voltage ( $V_{OL}$ )**

**Purpose:** To verify that the Thevenin Output Low Level Voltage ( $V_{OL}$ ) of the DUT's Data Lane LP transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.2, Line 1396
- [2] Ibid, Section 8.1.2, Table 18

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{OL}$ , which is a device's LP-TX Thevenin Output Low Level Voltage.

The D-PHY Specification states, " $V_{OL}$  is the Thevenin output, low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low-level state." [1].

In this test, the DUTs Data Lane  $V_{OL}$  values will be measured using a high-speed, real-time DSO while the DUT is driving an LP signaling sequence into two termination cases (both with and without the 50pF  $C_{LOAD}$  test fixture). (Note that this test is intended to be performed in conjunction with the other tests in this group on a single captured LP Escape Mode sequence waveform, where the measurement is performed on the output-low bits only.) For the purposes of this measurement,  $V_{OL}$  is measured as the mode of all waveform samples that are less than 50% of the absolute peak-to-peak  $V_{DP}$  and  $V_{DN}$  signal amplitudes, and should be measured across all LP-0 states in a single LP Escape Mode sequence. (Note that a ULPS Entry sequence is specified for this test, and all other measurements in this Group, as this should normally be supported on all Data Lanes for most DUTs.) This measurement shall be performed separately on both the  $V_{DP}$  and  $V_{DN}$  waveforms, and for each Data Lane.

For all Data Lanes, the value of  $V_{OL}$  for both the  $V_{DP}$  and  $V_{DN}$  signals must be between -50mV and +50mV in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.1.

**Test Procedure:**

- Connect the DUT to the Test Setup, using the 50pF  $C_{LOAD}$  test fixture.
- Create a condition that causes the DUT to source a ULPS Entry sequence on Data Lane 0.
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods, measure  $V_{OL}$  for both the  $V_{DP}$  and  $V_{DN}$  signals as described above.
- Repeat the previous steps with the  $C_{LOAD}$  fixture removed.
- Repeat the previous four steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For both  $C_{LOAD}$  cases, and for all Data Lanes:

- Verify that  $V_{OL}$  for the  $V_{DP}$  waveform is between -50 and +50mV.
- Verify that  $V_{OL}$  for the  $V_{DN}$  waveform is between -50 and +50mV.

**Possible Problems:** None.

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**Test 1.1.3 – Data Lane LP-TX 15%-85% Rise Time ( $T_{RLP}$ )**

**Purpose:** To verify that the 15%-85% Rise Time ( $T_{RLP}$ ) of the DUT's Data Lane LP transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.2, Line 1410
- [2] Ibid, Section 8.1.2, Table 19
- [3] Ibid, Section 8.1.2, Table 19 Note 1, Line 1423

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $T_{RLP}$ , which is a device's LP-TX 15%-85% Rise Time.

The D-PHY Specification states, “*The times  $T_{RLP}$  and  $T_{FLP}$  are the 15%-85% rise and fall times, respectively, of the output signal voltage, when the LP transmitter is driving a capacitive load  $C_{LOAD}$ . The 15%-85% levels are relative to the fully settled  $V_{OH}$  and  $V_{OL}$  voltages.*” [1].

Note that the specification states that the rise/fall times shall be measured into a capacitive load  $C_{LOAD}$ .  $C_{LOAD}$  is a separate parameter defined in the specification, which is used as a reference load for several LP requirements, of which rise/fall time is one.

Because the rise/fall time specification only defines an upper limit, the most meaningful approach would be to measure the rise/fall times using the maximum allowed  $C_{LOAD}$  (as this would result in the slowest edge, i.e., maximum rise time). If a DUT passes the rise/fall requirement with the maximum  $C_{LOAD}$ , it would only pass with greater margin (i.e., a smaller rise time) with a smaller  $C_{LOAD}$  value.

However, in cases where a DUT fails to meet the rise/fall time requirement with maximum  $C_{LOAD}$ , it would be useful to know if the result is different into a smaller  $C_{LOAD}$ . Therefore in this test, two cases will be measured, once using a large  $C_{LOAD}$ , and a second time using a smaller  $C_{LOAD}$ .

Note that choosing the exact values of  $C_{LOAD}$  for LP test purposes is somewhat problematic. The specification defines  $C_{LOAD}$  as having a range of 0 to 70pF [2]. The specification also explains that this load is considered distributed between three parts: 1) The transmitter's TX capacitance (up to 10pF), 2) The receiver's RX capacitance (up to 10pF), and 3) The transmission line between the TX and RX (up to 50pF) [3].

For practical purposes, there are several issues with the way the  $C_{LOAD}$  specification is defined. First, while exact load values (including 0pF) may be possible in a software simulation/design environment, practical measurements pose more of a problem, as the capacitance of the PCB boards and connectors on which the DUT is mounted are often unknown to the tester and cannot be controlled. Furthermore, these elements, even if well-designed, cannot be designed to have zero capacitance. Therefore, testing at 0pF  $C_{LOAD}$  is not possible, and the minimum load will be dictated by the DUT's PCB itself, plus any added capacitance introduced by the test setup (i.e., probes, and any other associated connectors).

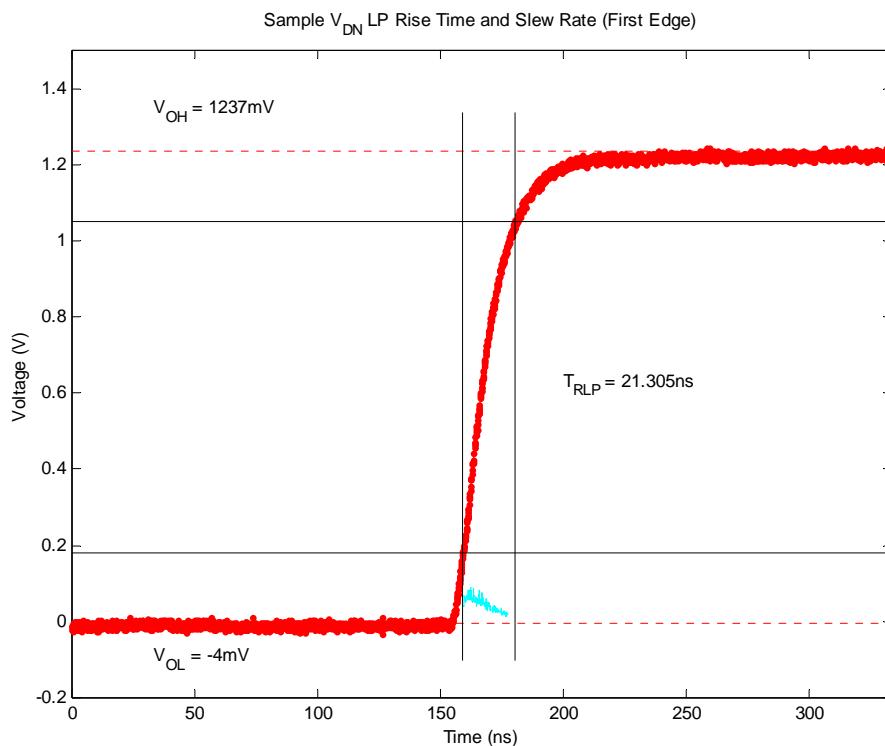
Thus the minimum capacitance is bounded by the DUT itself, and the test setup. For the maximum capacitance, a practical value must be chosen which takes all other factors into account, but still provides a reasonable measurement. It is possible to fabricate a test fixture/PCB that presents a lumped-value capacitance to the DUT transmitter. If this fixture was designed to be 70pF, this might over-stress the TX, as the total applied load including the DUT PCB and connectors would then likely be significantly greater than 70pF.

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Therefore a practical compromise must be determined. For the purpose of conformance testing, a fixture with a capacitive load of 50pF will be used as the “maximum”  $C_{LOAD}$  case. This accounts for the theoretical 10pF allotted for the TX, and also leaves an additional 10pF of ‘margin’, to account for non-ideal test boards, connectors, etc. Under this approach, the benefit of the doubt is given to the DUT, where if a DUT fails the rise/fall time test under a 50pF test load fixture, it would also most certainly fail more severely if measured under a true 70pF load. (This approach may allow marginal devices to pass this test, however that accepted as the preferred case over failing devices that may be close to the limit, and/or mounted on non-ideal evaluation boards.)

In addition to the maximum  $C_{LOAD}$  case, a second test case will be performed, with no external test load fixture applied (i.e., just the bare DUT, probed at the test points on the DUT PCB.)

In this test, the two single-ended  $V_{DP}$  and  $V_{DN}$  signals from the DUTs Data Lane LP transmitter will be captured using two channels of a real-time DSO. Using the measured  $V_{OH}$  and  $V_{OL}$  LP-TX Thevenin Output Voltage Levels as references (See Tests 1.1.1 and 1.1.2, respectively), the 15%-85% Rise Time ( $T_{RLP}$ ) will be measured independently for each rising edge of the  $V_{DP}$  and  $V_{DN}$  waveforms. The mean value across all observed rising edges will be computed to produce the final  $T_{RLP}$  result, and the maximum and minimum observed values will be reported as informative results. A sample measurement on a single edge is shown in the figure below.



**Figure 1.1.3-1: Example  $T_{RLP}$  Measurement**

For all Data Lanes, the value of  $T_{RLP}$  for  $V_{DP}$  and  $V_{DN}$  must be less than 25ns in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.1.

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**Test Procedure:**

- Connect the DUT to the Test Setup, using the 50pF  $C_{LOAD}$  test fixture.
- Create a condition that causes the DUT to source a ULPS Entry sequence on Data Lane 0.
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods, measure  $T_{RLP}$  for both  $V_{DP}$  and  $V_{DN}$  as described above.
- Repeat the previous steps with the  $C_{LOAD}$  fixture removed.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For both  $C_{LOAD}$  cases, and for all Data Lanes:

- Verify that  $T_{RLP}$  for the  $V_{DP}$  waveform is less than 25ns.
- Verify that  $T_{RLP}$  for the  $V_{DN}$  waveform is less than 25ns.

**Possible Problems:** None.

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**Test 1.1.4 – Data Lane LP-TX 15%-85% Fall Time ( $T_{FLP}$ )**

**Purpose:** To verify that the 15%-85% Fall Time ( $T_{FLP}$ ) of the DUT's Data Lane LP transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.2, Line 1410
- [2] Ibid, Section 8.1.2, Table 19

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $T_{FLP}$ , which is a device's LP-TX 15%-85% Fall Time.

The D-PHY Specification states, “*The times  $T_{RLP}$  and  $T_{FLP}$  are the 15%-85% rise and fall times, respectively, of the output signal voltage, when the LP transmitter is driving a capacitive load  $C_{LOAD}$ . The 15%-85% levels are relative to the fully settled  $V_{OH}$  and  $V_{OL}$  voltages.*” [1].

(Note the general methodology for this test is identical to the LP-TX Rise Time test of 1.1.3, except the falling edges will be measured.  $T_{FLP}$  will be measured both with and without the 50pF  $C_{LOAD}$  fixture, and will be measured for all Data Lanes.)

For all Data Lanes, the value of  $T_{FLP}$  for  $V_{DP}$  and  $V_{DN}$  must be less than 25ns in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.1.

**Test Procedure:**

- Connect the DUT to the Test Setup, using the 50pF  $C_{LOAD}$  test fixture.
- Create a condition that causes the DUT to source a ULPS Entry sequence on Data Lane 0.
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods, measure  $T_{FLP}$  for both  $V_{DP}$  and  $V_{DN}$  as described above.
- Repeat the previous steps with the  $C_{LOAD}$  fixture removed.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For both  $C_{LOAD}$  cases, and for all Data Lanes:

- Verify that  $T_{FLP}$  for the  $V_{DP}$  waveform is less than 25ns.
- Verify that  $T_{FLP}$  for the  $V_{DN}$  waveform is less than 25ns.

**Possible Problems:** None.

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**Test 1.1.5 – Data Lane LP-TX Slew Rate vs. C<sub>LOAD</sub> ( $\delta V/\delta t_{SR}$ )**

**Purpose:** To verify that the Slew Rate ( $\delta V/\delta t_{SR}$ ) of the DUT's Data Lane LP transmitter is within the conformance limits, for specific capacitive loading conditions.

**References:**

- [1] D-PHY Specification, Section 8.1.2, Line 1412
- [2] Ibid, Section 8.1.2, Table 19
- [3] Ibid, Section 8.1.2, Figure 45

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $\delta V/\delta t_{SR}$ , which is the DUT LP-TX Slew Rate.

The D-PHY Specification states, “*The slew rate  $\delta V/\delta t_{SR}$  is the derivative of the LP transmitter output signal voltage over time. The LP transmitter output signal transitions shall meet the maximum and minimum slew rate specifications as shown in Table 19, Figure 45 and Figure 46.*” [1]. A copy of the specification Table 19 is reproduced below.

$\delta V/\delta t_{SR}$	Slew rate @ C <sub>LOAD</sub> = 0pF		500	mV/ns	1, 3, 7, 8
	Slew rate @ C <sub>LOAD</sub> = 5pF		300	mV/ns	1, 3, 7, 8
	Slew rate @ C <sub>LOAD</sub> = 20pF		250	mV/ns	1, 3, 7, 8
	Slew rate @ C <sub>LOAD</sub> = 70pF		150	mV/ns	1, 3, 7, 8
	Slew rate @ C <sub>LOAD</sub> = 0 to 70pF (Falling Edge Only)	30		mV/ns	1, 2, 3
	Slew rate @ C <sub>LOAD</sub> = 0 to 70pF (Rising Edge Only)	30		mV/ns	1, 3, 9
	Slew rate @ C <sub>LOAD</sub> = 0 to 70pF (Rising Edge Only)	30 – 0.075 * (V <sub>O,INST</sub> – 700)		mV/ns	1, 10, 11
C <sub>LOAD</sub>	Load capacitance	0	70	pF	1

**Figure 1.1.5-1: Slew Rate vs. C<sub>LOAD</sub> Requirements  
(D-PHY Specification Table 19)**

Note that Table 19 in the specification contains several footnotes [2], which further clarify the limit requirements listed in the table. While the individual notes will not be reproduced here, a summary of the key points as applicable to this test are as follows:

Falling edges:

- (Note 8): The maximum Slew Rate limits are applicable across the entire signal transition/edge.
- (Note 2): The minimum Slew Rate limit (30mV/ns) applies only to the 400-930mV region of falling edges.

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Rising edges:

- (Note 8): The maximum Slew Rate limits are applicable across the entire signal transition/edge.
- (Note 9): The minimum Slew Rate limit (30mV/ns) applies only to the 400-700mV region of rising edges.
- (Note 11): For the 700-930mV region of rising edges, the minimum slew rate limit is defined by the equation  $30 - 0.075 * (V_{O,INST} - 700)$ .

Note also that this specification, as written, presents the same problem regarding  $C_{LOAD}$  as was observed for Test 1.1.3 (see Test 1.1.3 Discussion), where it is difficult to present a precise  $C_{LOAD}$  value to the transmitter under test, as the capacitance of the DUT's evaluation board is not known and may not be well controlled. (Note this is even more critical in this test, as the slew rate specifications are defined for very specific  $C_{LOAD}$  values.) Furthermore, even with very well-designed evaluation boards,  $C_{LOAD}$  values of 0pF and 5pF are not realistically achievable for a practical test PCB.

Therefore, as was the case for Test 1.1.3, some compromise must be made in order to define a realistic and practical conformance test. A summary of the methodology for this test is as follows:

- For the Maximum Slew Rate test, the measurement will be performed using the 50pF  $C_{LOAD}$  test fixture, and the results will be evaluated against the 70pF limit of 150mV/ns across the entire signal edge, for both rising and falling edges.
- For the Minimum Slew Rate test for falling edges, the measurement will be performed using the 50pF  $C_{LOAD}$  test fixture, and the results will be evaluated against the 30mV/ns limit across the voltage range of 400-930mV.
- For the Minimum Slew Rate test for rising edges, the measurement will be performed using the 50pF  $C_{LOAD}$  test fixture, and the results will be evaluated against the 30mV/ns limit across the voltage range of 400-700mV, and against the equation-based limit for the 700-930mV voltage range.
- (Informative): Additionally, the above measurements will be performed a second time, but with the 50pF  $C_{LOAD}$  test fixture removed (i.e., with the DSO probes connected to the unterminated DUT signal lines, with no additional test load applied, thus providing the smallest possible amount of capacitive load, beyond the contribution due to the DUT PCB itself). The measurements will be computed against the same conformance values as for the 50pF  $C_{LOAD}$  case, however the results will be reported as Informative. The purpose of this step is to provide a qualitative estimate of the amount of  $C_{LOAD}$  contributed by the DUT's PCB, as the results measured without the 50pF  $C_{LOAD}$  board should show noticeably faster slew rates compared to the results measured with the 50pF  $C_{LOAD}$  board, if the DUT PCB is designed to have minimal capacitive loading.

In this test, the two single-ended  $V_{DP}$  and  $V_{DN}$  signals from the DUTs Data Lane LP transmitter will be captured using two channels of a real-time DSO. The Slew Rate will be computed and measured independently for each edge of the  $V_{DP}$  and  $V_{DN}$  signals as described above, using a 50mV vertical window. Note that this translates to the rising edge slew rate at time ( $t$ ) being calculated using a centered window around time ( $t$ ), where the  $dv/dt$  is determined using the first sample after time ( $t$ ) that is greater than or equal to  $v(t)+25mV$ , and the last sample before time ( $t$ ) that is less than or equal to  $v(t)-25mV$  (or with opposite slope for the case of a falling edge).

Once the Slew Rate data curve is computed for a single edge using the sliding window technique, the maximum value across the entire edge will be recorded. This process is then repeated for all edges. The results for all rising edges will then be averaged together to produce the final rising edge Maximum Slew Rate result, and the results for all falling edges will then be averaged together to produce the final falling edge Maximum Slew Rate result.

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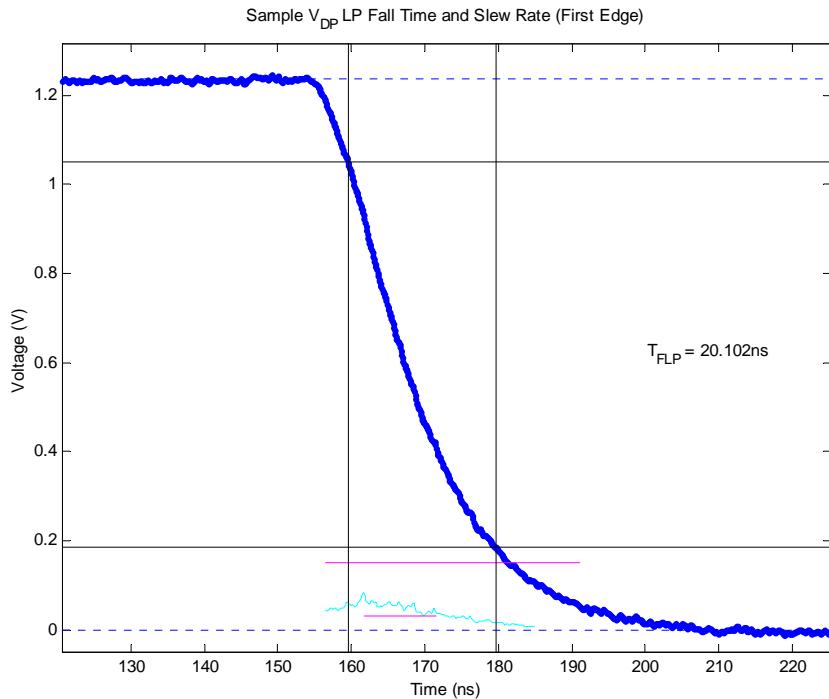
For the Minimum Slew Rate, three cases exist. For falling edges, the minimum slew rate value across the 400-930mV region of each edge will be recorded, and the results for each edge will then be averaged together to produce the final falling edge Minimum Slew Rate result. For rising edges, the minimum slew rate value across the 400-700mV region of each edge will be recorded, and the results for each edge will then be averaged together to produce the final rising edge Minimum Slew Rate result.

For the Minimum Slew Rate across the 700-930mV region, a single minimum value cannot be used to determine conformance, as the conformance limit is not a static value across the entire applicable range, but rather consists of a curved, equation-based limit line (see Figure 1.1.5-5 below), which is inversely proportional to the instantaneous  $V_{DP}$  or  $V_{DN}$  voltage. (Thus the conformance limit line behaves more like a mask.) To quantify the conformance relative to the limit line, the minimum margin between the measured slew rate curve and the Minimum Slew Rate limit line will be calculated for each edge (where the margin value at time(t) is the slew rate value at (t) minus the lower limit line value at (t), and a negative margin value is considered failing). The minimum margin with respect to the limit line will be recorded for each edge, and the results for each edge will then be averaged together to produce the final rising edge Minimum Slew Rate Margin result.

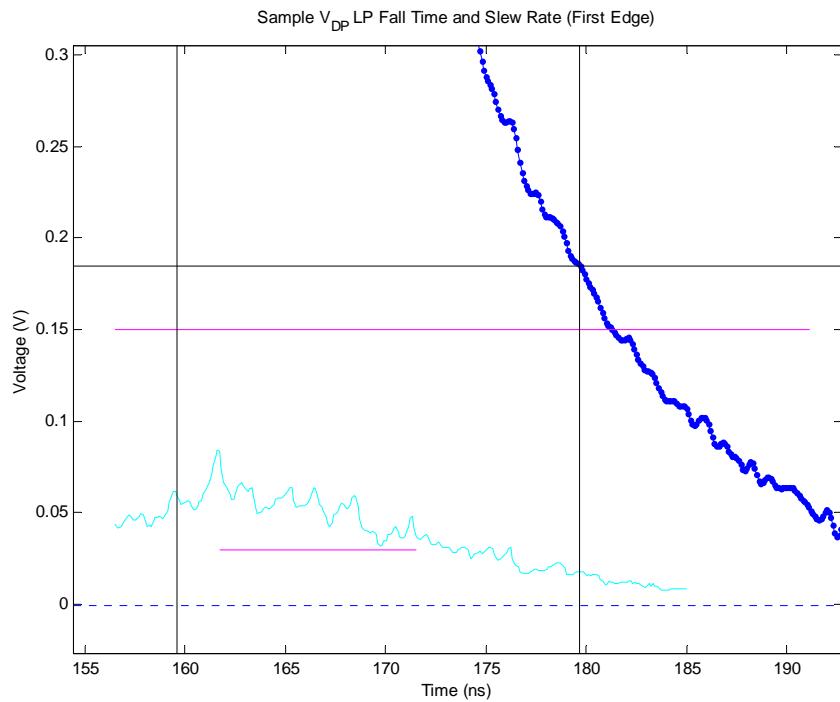
The five measurements above will be measured for both the  $V_{DP}$  and  $V_{DN}$  signals, and for all Data Lanes.

Note an example slew rate measurement is shown in the figures shown on the following pages. The first figure (Figure 1.1.5-2) shows the entire LP edge, where the computed sliding-window slew rate curve is shown in light blue. The Maximum (150mV/ns) and Minimum (30mV/ns) slew rate conformance limits are shown over the horizontal ranges corresponding to the respective vertical ranges over which the limit applies (i.e., the entire vertical region for the Max limit, and the 400-930mV region for the Min limit). Figure 1.1.5-3 shows a zoomed-in view of the slew rate data and conformance limit lines. Figures 1.1.5-4 and 1.1.5-5 show the same concept, but for the rising edge case. (Note the curved Minimum limit in Figure 1.1.5-5.)

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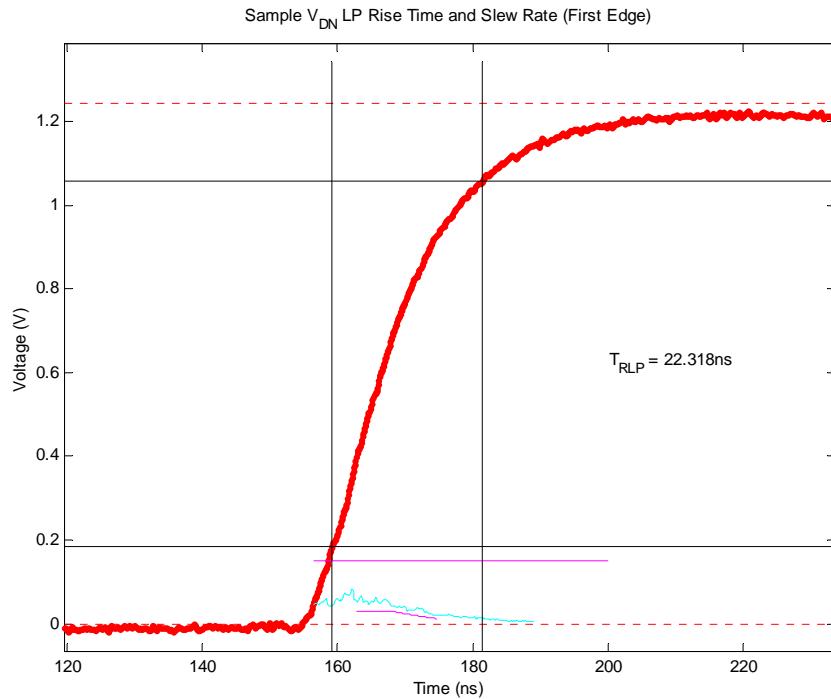


**Figure 1.1.5-2: Sample LP Falling Edge Slew Rate Measurement  
(Slew rate data shown in light blue)**

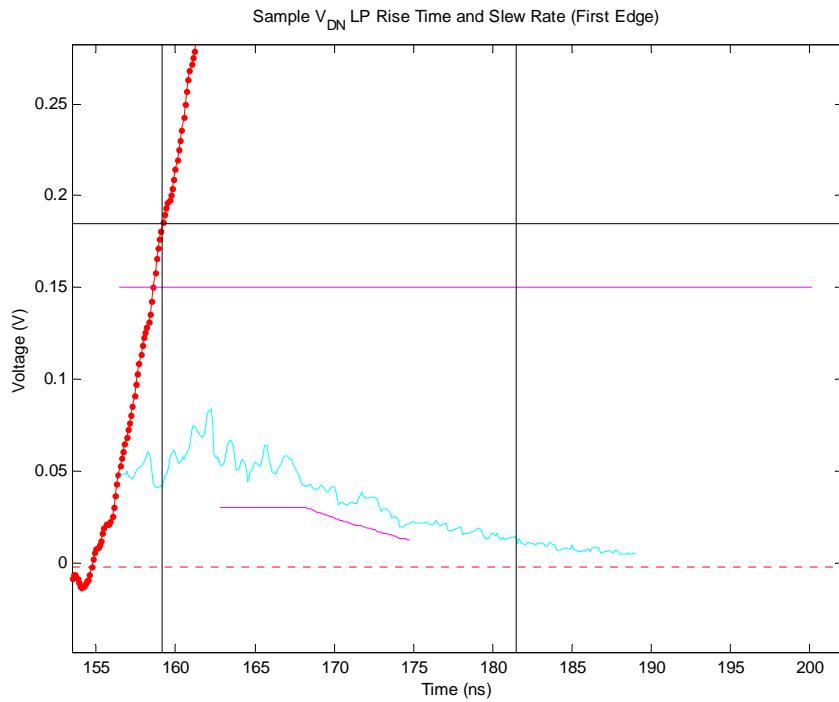


**Figure 1.1.5-3: Zoomed-in View of Slew Rate Data  
(Slew Rate falling edge Max/Min limits shown in pink)**

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**Figure 1.1.5-4: Sample LP Rising Edge Slew Rate Measurement  
(Slew rate data shown in light blue)**



**Figure 1.1.5-5: Zoomed-in View of Slew Rate Data  
(Slew Rate rising edge Max/Min limits shown in pink)**

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**Test Setup:** See Appendix B.1.1.

**Test Procedure:**

- Connect the DUT to the Test Setup, using the 50pF  $C_{LOAD}$  test fixture.
- Create a condition that causes the DUT to source a ULPS Entry sequence on Data Lane 0.
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods, compute the following for the  $V_{DP}$  and  $V_{DN}$  falling edges:
  1. Compute the final averaged Maximum  $\delta V/\delta t_{SR}$  result (over the entire vertical edge region).
  2. Compute the final averaged Minimum  $\delta V/\delta t_{SR}$  result (400-930mV region).
- Using post-processing methods, compute the following for the  $V_{DP}$  and  $V_{DN}$  rising edges:
  1. Compute the final averaged Maximum  $\delta V/\delta t_{SR}$  result (over the entire vertical edge region).
  2. Compute the final averaged Minimum  $\delta V/\delta t_{SR}$  result (400-700mV region)
  3. Compute the final averaged Minimum  $\delta V/\delta t_{SR}$  Margin result (700-930mV region).
- (Informative): Repeat the above procedure a second time, but with the 50pF  $C_{LOAD}$  fixture removed.
- Repeat all above steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

Falling edges:

For the 50pF  $C_{LOAD}$ , for both  $V_{DP}$  and  $V_{DN}$ , and for all Data Lanes:

- Verify that the Maximum  $\delta V/\delta t_{SR}$  is less than 150mV/ns across the entire edge.
- Verify that the Minimum  $\delta V/\delta t_{SR}$  is greater than 30mV/ns across the 400-930mV region.

Rising edges:

For the 50pF  $C_{LOAD}$ , for both  $V_{DP}$  and  $V_{DN}$ , and for all Data Lanes:

- Verify that the Maximum  $\delta V/\delta t_{SR}$  is less than 150mV/ns across the entire edge.
- Verify that the Minimum  $\delta V/\delta t_{SR}$  is greater than 30mV/ns across the 400-700mV region.
- Verify that the Minimum  $\delta V/\delta t_{SR}$  Margin is greater than 0mV/ns across the 700-930mV region.

Also, any measurements made with the 50pF  $C_{LOAD}$  fixture removed will be reported as Informative.

**Possible Problems:** None.

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**Test 1.1.6 – Data Lane LP-TX Pulse Width of Exclusive-OR Clock ( $T_{LP-PULSE-TX}$ )**

**Purpose:** To verify that the pulse width ( $T_{LP-PULSE-TX}$ ) of the DUT's Data Lane LP transmitter XOR Clock is within the conformance limits.

**References:**

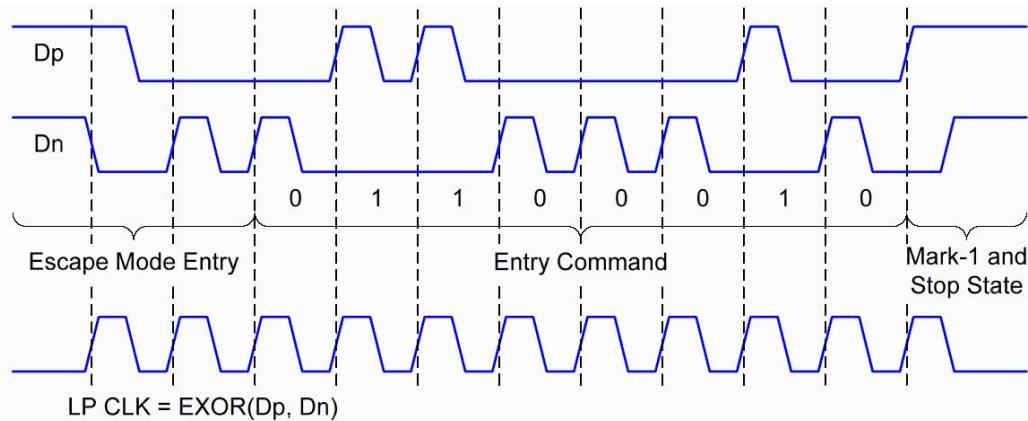
- [1] D-PHY Specification, Section 8.1.2, Line 1444
- [2] Ibid, Section 8.1.2, Table 19

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $T_{LP-PULSE-TX}$ , which is the pulse width of the DUT LP-TX XOR clock. A graphical example of the XOR operation that creates the LP clock, reproduced from the specification, is shown below.



**Figure 1.1.6-1: LP XOR Clock Generation from  $V_{DP}$  and  $V_{DN}$**

The D-PHY Specification separates the  $T_{LP-PULSE-TX}$  specification into two parts [2]:

- The first LP XOR clock pulse after a Stop state, *and* the last LP XOR clock pulse before a Stop state must be wider than 40ns.
- All other LP XOR clock pulses must be wider than 20ns.

The D-PHY Specification also provides specifications regarding how the XOR Clock is to be generated, specifically, “*Using a common trip-level in the range [ $V_{IL,MAX} + V_{OL,MIN}, V_{IH,MIN} + V_{OL,MAX}$ ], the exclusive-OR clock shall not contain pulses shorter than  $T_{MIN-TX}$ .*” [1]. [Ed. Note: As there is actually no other reference for definition of  $T_{MIN-TX}$  appearing anywhere in the spec, the assumption is that this is simply an editorial error and that this text should indicate  $T_{LP-PULSE-TX}$ .]

The provision of a range for the common trip level implies that the measurement should be performed multiple times, using various trip levels spanning the entire specified range. This can potentially result in non-conformant pulse widths at certain threshold levels, particularly in cases where the DUT may have oddly shaped and/or asymmetric signal edges. Using post processing on the captured waveform data, it is possible to perform measurements using any number and range of threshold levels. For the purposes of this test, two trip-level cases will be performed, representing the maximum and minimum allowed trip levels.

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Note that  $V_{IL,MAX} = 550\text{mV}$ ,  $V_{OL,MIN} = -50\text{mV}$ ,  $V_{IH,MIN} = 880\text{mV}$ , and  $V_{OL,MAX} = 50\text{mV}$ . Thus, the minimum trip level becomes  $550 - 50 = 500\text{mV}$ , and the maximum trip level is  $880 + 50 = 930\text{mV}$ .

In this test, the two single-ended  $V_{DP}$  and  $V_{DN}$  signals from the DUTs Data Lane LP transmitter will be captured using two channels of a real-time DSO. Using post-processing methods, the  $V_{DP}$  and  $V_{DN}$  waveform samples will be 2-level quantized (i.e., rounded up/down to either 0 or 1) according to the specified trip-level threshold voltage. The resulting binary arrays will then be XOR'ed to create the sampled LP Clock, on which the  $T_{LP-PULSE-TX}$  measurement will then be performed. Pulse width values (based on the midpoint crossing times of the generated XOR signal) for all XOR Clock pulses will be recorded and verified against their respective conformance limits. (Note that for the purposes of this test, a ‘pulse’ is defined as a positive pulse, i.e., rising edge to falling edge.)

This entire process will be performed twice, once for the maximum trip-level threshold voltage (930mV) and once for the minimum trip-level threshold voltage (500mV). Also note that while the specification does not indicate the  $C_{LOAD}$  value used for this measurement, the test will be performed both with and without the 50pF  $C_{LOAD}$  test fixture, and will be measured for all Data Lanes.

For all cases, the first XOR clock pulse after a Stop state and last XOR clock pulse before a Stop state must be greater than 40ns in order to be considered conformant, and the minimum of all other XOR clock pulses must be greater than 20ns in order to be considered conformant[2].

**Test Setup:** See Appendix B.1.1.

**Test Procedure:**

- Connect the DUT to the Test Setup, using the 50pF  $C_{LOAD}$  test fixture.
- Create a condition that causes the DUT to source a ULPS Entry sequence on Data Lane 0.
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods as described above, compute the LP XOR Clock and measure the three  $T_{LP-PULSE-TX}$  values (first, last, and min of all others) using the maximum trip-level threshold voltage of 930mV.
- Using post-processing methods as described above, compute the LP XOR Clock and measure the three  $T_{LP-PULSE-TX}$  values (first, last, and min of all others) using the minimum trip-level threshold voltage of 500mV.
- Repeat the previous steps, with the 50pF  $C_{LOAD}$  fixture removed.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For both  $C_{LOAD}$  cases, both trip-level voltages, and for all Data Lanes:

- Verify that the first LP XOR Clock pulse after the initial Stop state is greater than 40ns.
- Verify that the last LP XOR Clock pulse before the final Stop state is greater than 40ns.
- Verify that the minimum of all other clock pulses is greater than 20ns.

**Possible Problems:**

When the XOR Clock is computed from the 2-level quantized LP Dp and Dn waveforms, glitches can sometimes result if excessive noise is present on the input waveforms (either DSO sampling noise, or noise from the DUT itself, which can cause multiple short-term excursions across the trip-level threshold voltage, at the threshold crossing point). Care should be taken to ensure that the input waveforms are as smooth and free from noise as possible, however any post-processing algorithms should ensure that any glitches caused by such artifacts are not erroneously counted as XOR Clock pulses.

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**Test 1.1.7 – Data Lane LP-TX Period of Exclusive-OR Clock ( $T_{LP-PER-TX}$ )**

**Purpose:** To verify that the period ( $T_{LP-PER-TX}$ ) of the DUT's Data Lane LP transmitter XOR Clock is within the conformance limits.

**References:**

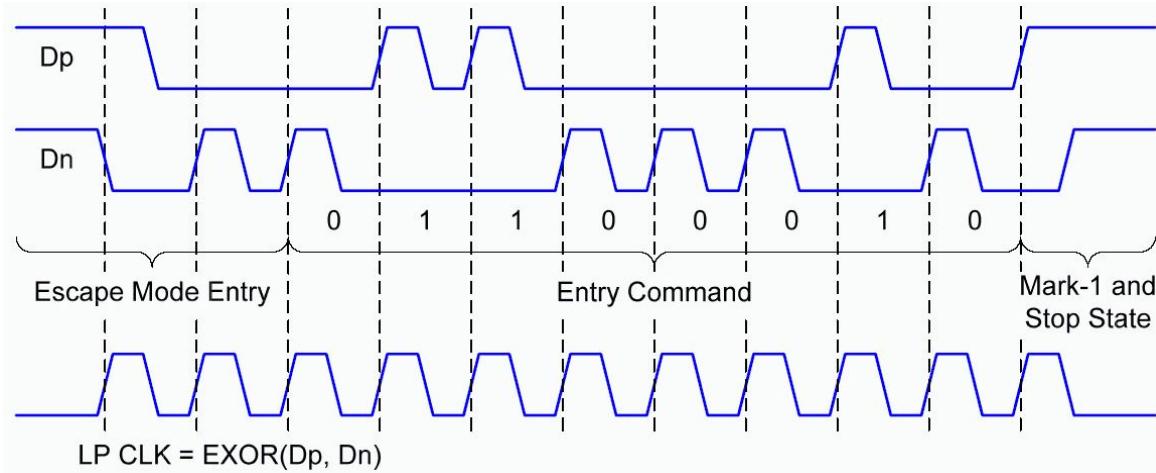
[1] D-PHY Specification, Section 8.1.2, Table 19

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $T_{LP-PER-TX}$ , which is the Period of the DUT LP-TX XOR clock. A graphical representation of the XOR operation that creates the LP clock, reproduced from the specification, is shown below.



**Figure 1.1.7-1: LP XOR Clock Extraction from  $V_{DP}$  and  $V_{DN}$**

Note that  $T_{LP-PER-TX}$  is only mentioned in Table 19 of the specification, and does not have an explicit text description/reference. The definition also does not explicitly state the trip levels and/or  $C_{LOAD}$  values for which the requirement applies. Therefore, values must be chosen for the purpose of conformance testing. For the sake of consistency with the previous test (Test 1.1.6, XOR Clock pulse width), the 500mV and 930mV trip levels will be used, and the measurement will be performed both with and without the 50pF  $C_{LOAD}$  test fixture.

In this test, the LP Clock will be captured and computed using the same process described in the previous test (see Test 1.1.6, Discussion). However, rather than measuring the rising-to-falling and falling-to-rising pulse widths, this test will measure  $T_{LP-PER-TX}$  as the rising-to-rising and falling-to-falling periods of the XOR clock. The reported  $T_{LP-PER-TX}$  result will be minimum of all measured period values, and will be reported separately for the rising-to-rising and falling-to-falling period cases. The measurement will be performed for both trip-level voltages, both with and without the 50pF  $C_{LOAD}$  test fixture, and for all Data Lanes.

For all cases, the value of  $T_{LP-PER-TX}$  must be greater than 90ns in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.1.

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**Test Procedure:**

- Connect the DUT to the Test Setup, using the 50pF  $C_{LOAD}$  test fixture.
- Create a condition that causes the DUT to source a ULPS Entry sequence on Data Lane 0.
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods as described above, compute the LP XOR Clock and measure the  $T_{LP-PER-TX}$  rising-to-rising and falling-to-falling edge periods using the maximum trip-level threshold of 930mV.
- Using post-processing methods as described above, compute the LP XOR Clock and measure the  $T_{LP-PER-TX}$  rising-to-rising and falling-to-falling edge periods using the minimum trip-level threshold of 500mV.
- Repeat the previous steps, with the 50pF  $C_{LOAD}$  fixture removed.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For both  $C_{LOAD}$  cases, both trip-level voltages, and for all Data Lanes:

- Verify that the minimum  $T_{LP-PER-TX}$  rising-edge-to-rising-edge period is greater than 90ns.
- Verify that the minimum  $T_{LP-PER-TX}$  falling-edge-to-falling-edge period is greater than 90ns.

**Possible Problems:**

See Possible Problems comments for Test 1.1.6. The same applies to this test.

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## **GROUP 2: CLOCK LANE LP-TX SIGNALING REQUIREMENTS**

### **Overview:**

This group of tests verifies various requirements specific to Clock Lane LP signaling. The intent of the structure of this Group is to facilitate performing a set of related LP-TX measurements on a single Clock Lane LP-TX waveform sequence (e.g., Clock Lane ULPS Entry/Exit).

Note that this test Group is typically performed on CSI-2 and DSI Master devices only (e.g., camera sensors in the CSI-2 case, and host processors in the DSI case.) It can also be performed on ‘bare-phy’ DUT types. This Group is considered Not Applicable for Slave devices (e.g., DSI displays), as a Slave’s Clock Lane does not contain an LP-TX.

### **Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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**Test 1.2.1 – Clock Lane LP-TX Thevenin Output High Level Voltage ( $V_{OH}$ )**

**Purpose:** To verify that the Thevenin Output High Level Voltage ( $V_{OH}$ ) of the DUT's Clock Lane LP transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.2, Line 1397
- [2] Ibid, Section 8.1.2, Table 18

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{OH}$ , which is a device's LP-TX Thevenin Output High Level Voltage.

The D-PHY Specification states, " $V_{OH}$  is the Thevenin output, high-level voltage in the high-level state, when the pad pin is not loaded." [1].

(Note that this test is nearly identical to Test 1.1.1 (Data Lane LP-TX Thevenin Output High Voltage), however while Test 1.1.1 measured the Data Lane  $V_{OH}$ , this test will measure the Clock Lane  $V_{OH}$ .)

In this test, the DUTs Clock Lane  $V_{OH}$  values will be measured using a high-speed, real-time DSO while the DUT is driving an LP signaling sequence into an open termination (i.e., no  $C_{LOAD}$  test fixture), using the same general methodology as Test 1.1.1. Note however that while Test 1.1.1 recommended that the Data Lane ULPS Entry sequence be used for the  $V_{OH}$  measurement, this sequence is not available on the Clock Lane, and in general the available sequences for LP measurements on the Clock Lane are relatively limited to three options: 1) a Clock Lane ULPS Entry sequence, 2) an HS Request, or 3) static LP-11 or LP-00 levels. (Note the ULPS sequence is generally preferred for the  $V_{OH}/V_{OL}$  measurements, as  $V_{OL}$  can be difficult to measure on an HS Request sequence, and is NOT recommended due to the signaling artifacts present on the line during the LP-00 period caused by the enabling of the HS termination.) Also note that the Clock Lane ULPS Entry sequence is NOT the same as the Data Lane ULPS Entry sequence, and consists of an LP-11/10/00 sequence.

$V_{OH}$  shall be measured using the same mode-based approach described in Test 1.1.1. The measurement will be performed separately on both the  $V_{DP}$  and  $V_{DN}$  Clock Lane waveforms, and will be measured both with and without the 50pF  $C_{LOAD}$  test fixture.

The value of  $V_{OH}$  for both the  $V_{DP}$  and  $V_{DN}$  signals of the Clock Lane shall be between 1.1V and 1.3V in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.1.

**Test Procedure:**

- Connect the DUT to the Test Setup, using the 50pF  $C_{LOAD}$  test fixture.
- Create a condition that causes the DUT to source a ULPS Entry sequence on the Clock Lane.
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods, measure  $V_{OH}$  for both the  $V_{DP}$  and  $V_{DN}$  signals as described above.
- Repeat the previous steps, with the 50pF  $C_{LOAD}$  fixture removed.

**Observable Results:**

For both  $C_{LOAD}$  cases:

- Verify that  $V_{OH}$  for the Clock Lane  $V_{DP}$  waveform is between 1.1 and 1.3 Volts.
- Verify that  $V_{OH}$  for the Clock Lane  $V_{DN}$  waveform is between 1.1 and 1.3 Volts.

**Possible Problems:** None.

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**Test 1.2.2 – Clock Lane LP-TX Thevenin Output Low Level Voltage ( $V_{OL}$ )**

**Purpose:** To verify that the Thevenin Output Low Level Voltage ( $V_{OL}$ ) of the DUT's Clock Lane LP transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.2, Line 1397
- [2] Ibid, Section 8.1.2, Table 18

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{OL}$ , which is a device's LP-TX Thevenin Output Low Level Voltage.

The D-PHY Specification states, " $V_{OL}$  is the Thevenin output, low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low-level state." [1].

(Note this test is effectively identical to the previous test (see Test 1.2.1), except that the  $V_{OL}$  level is measured for the Clock Lane. The measurement is still performed for both  $C_{LOAD}$  cases.)

The value of  $V_{OL}$  for both the  $V_{DP}$  and  $V_{DN}$  Clock Lane signals shall be between -50mV and +50mV in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.1.

**Test Procedure:**

- Connect the DUT to the Test Setup, using the 50pF  $C_{LOAD}$  test fixture.
- Create a condition that causes the DUT to source a ULPS Entry sequence on the Clock Lane.
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods, measure  $V_{OL}$  for both the  $V_{DP}$  and  $V_{DN}$  signals as described above.
- Repeat the previous steps, with the 50pF  $C_{LOAD}$  fixture removed.

**Observable Results:**

For both  $C_{LOAD}$  cases:

- Verify that  $V_{OL}$  for the Clock Lane  $V_{DP}$  waveform is between -50 and +50mV.
- Verify that  $V_{OL}$  for the Clock Lane  $V_{DN}$  waveform is between -50 and +50mV.

**Possible Problems:** None.

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**Test 1.2.3 – Clock Lane LP-TX 15%-85% Rise Time ( $T_{RLP}$ )**

**Purpose:** To verify that the 15%-85% Rise Time ( $T_{RLP}$ ) of the DUT's Clock Lane LP transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.2, Line 1410
- [2] Ibid, Section 8.1.2, Table 19

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $T_{RLP}$ , which is a device's LP-TX 15%-85% Rise Time.

The D-PHY Specification states, “*The times  $T_{RLP}$  and  $T_{FLP}$  are the 15%-85% rise and fall times, respectively, of the output signal voltage, when the LP transmitter is driving a capacitive load  $C_{LOAD}$ . The 15%-85% levels are relative to the fully settled  $V_{OH}$  and  $V_{OL}$  voltages.*” [1].

In this test, the DUT's Clock Lane  $T_{RLP}$  value will be measured using a high-speed, real-time DSO while the DUT is driving an LP signaling sequence into two termination cases. Note that the only potential options for performing this test are either on the initial LP rising edges following power-on, or the rising edges during a ULPS Exit sequence, as these are the only two times where LP rising edges are transmitted under normal operation. A ULPS Exit sequence (Mark-1/Stop, or LP-00/10/11) is recommended (and specified in the procedure below), as it should be supported by most devices, and should produce the most consistent results.

Using the measured Clock Lane  $V_{OH}$  and  $V_{OL}$  LP-TX Thevenin Output Voltage Levels as references (See Tests 1.2.1 and 1.2.2, respectively), the 15%-85% Rise Time ( $T_{RLP}$ ) will be measured independently for the rising edges of the  $V_{DP}$  and  $V_{DN}$  waveforms. (Note the same general methodology is used as for Test 1.1.3.)

The value of  $T_{RLP}$  for  $V_{DP}$  and  $V_{DN}$  shall be less than 25ns in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.1.

**Test Procedure:**

- Connect the DUT to the Test Setup, using the 50pF  $C_{LOAD}$  test fixture.
- Create a condition that causes the DUT to source a ULPS Exit sequence (Mark-1/Stop) on the Clock Lane.
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods, measure  $T_{RLP}$  for both  $V_{DP}$  and  $V_{DN}$  as described above.
- Repeat the previous steps, with the 50pF  $C_{LOAD}$  fixture removed.

**Observable Results:**

For both  $C_{LOAD}$  cases:

- Verify that  $T_{RLP}$  for the Clock Lane  $V_{DP}$  waveform is less than 25ns.
- Verify that  $T_{RLP}$  for the Clock Lane  $V_{DN}$  waveform is less than 25ns.

**Possible Problems:** None.

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**Test 1.2.4 – Clock Lane LP-TX 15%-85% Fall Time ( $T_{FLP}$ )**

**Purpose:** To verify that the 15%-85% Fall Time ( $T_{FLP}$ ) of the DUT's Clock Lane LP transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.2, Line 1410
- [2] Ibid, Section 8.1.2, Table 19

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $T_{FLP}$ , which is a device's LP-TX 15%-85% Fall Time.

The D-PHY Specification states, “*The times  $T_{RLP}$  and  $T_{FLP}$  are the 15%-85% rise and fall times, respectively, of the output signal voltage, when the LP transmitter is driving a capacitive load  $C_{LOAD}$ . The 15%-85% levels are relative to the fully settled  $V_{OH}$  and  $V_{OL}$  voltages.*” [1].

In this test, the DUT's Clock Lane  $T_{FLP}$  value will be measured using a high-speed, real-time DSO while the DUT is driving an LP signaling sequence into two termination cases. Note that the ULPS Entry sequence will be used for this test, as was used for Tests 1.2.1 and 1.2.2.

Using the measured Clock Lane  $V_{OH}$  and  $V_{OL}$  LP-TX Thevenin Output Voltage Levels as references (See Tests 1.2.1 and 1.2.2, respectively), the 15%-85% Fall Time ( $T_{FLP}$ ) will be measured independently for the falling edges of the Clock Lane  $V_{DP}$  and  $V_{DN}$  waveforms.

The value of  $T_{FLP}$  for  $V_{DP}$  and  $V_{DN}$  shall be less than 25ns in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.1.

**Test Procedure:**

- Connect the DUT to the Test Setup, using the 50pF  $C_{LOAD}$  test fixture.
- Create a condition that causes the DUT to source a ULPS Entry sequence on the Clock Lane.
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods, measure  $T_{FLP}$  for both  $V_{DP}$  and  $V_{DN}$  as described above.
- Repeat the previous steps, with the 50pF  $C_{LOAD}$  fixture removed.

**Observable Results:**

For both  $C_{LOAD}$  cases:

- Verify that  $T_{FLP}$  for the Clock Lane  $V_{DP}$  waveform is less than 25ns.
- Verify that  $T_{FLP}$  for the Clock Lane  $V_{DN}$  waveform is less than 25ns.

**Possible Problems:** None.

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**Test 1.2.5 – Clock Lane LP-TX Slew Rate vs.  $C_{LOAD}$  ( $\delta V/\delta t_{SR}$ )**

**Purpose:** To verify that the Slew Rate ( $\delta V/\delta t_{SR}$ ) of the DUT's Clock Lane LP transmitter is within the conformance limits, for specific capacitive loading conditions.

**References:** (See Discussion.)

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Note that this test is identical in terms of specification requirements and references to the Data Lane *Slew Rate vs.  $C_{LOAD}$*  test (see Test 1.1.5). The only difference for the Clock Lane case is that the test waveforms are different, as the ULPS Entry sequence for the Clock Lane is different than the Data Lane, and does not contain any rising edges. Therefore, in order to measure the slew rate of Clock Lane rising edges, the edges must be generated in the same manner as for the Clock Lane rise time tests. (See Discussion sections for previous Tests 1.2.3 and 1.2.4 for the somewhat limited options for generating LP rising edges on the Clock Lane.)

Also, because the Clock ULPS Entry and Exit sequences only generate one rising and falling LP edge for  $V_{DP}$  and  $V_{DN}$ , the averaging of each result over multiple edges often cannot be performed (unless the DUT and scope can be configured to capture and accumulate multiple trigger events in one waveform record, which may not be possible for all DUTs.) Un-averaged measurements may be performed on single rising or falling edges, however care should be taken to ensure that false failures do not occur due to noise or other transient artifacts.

The conformance requirements for this test are the same as the Data Lane case (see Test 1.1.5).

**Test Setup:** See Appendix B.1.1.

**Test Procedure:**

- Connect the DUT to the Test Setup, using the 50pF  $C_{LOAD}$  test fixture.
- Create a condition that causes the DUT to source a Clock Lane ULPS Entry sequence on the Clock Lane. (Note this will produce one falling edge each for  $V_{DP}$  and  $V_{DN}$ .)
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods, compute the following for the  $V_{DP}$  and  $V_{DN}$  falling edges:
  1. Compute the final averaged Maximum  $\delta V/\delta t_{SR}$  result (over the entire vertical edge region).
  2. Compute the final averaged Minimum  $\delta V/\delta t_{SR}$  result (400-930mV region).
- Create a condition that causes the DUT to source a ULPS Exit sequence (Mark-1/Stop) on the Clock Lane. (Note this will produce one rising edge each for  $V_{DP}$  and  $V_{DN}$ .)
- Using post-processing methods, compute the following for the  $V_{DP}$  and  $V_{DN}$  rising edges:
  1. Compute the final averaged Maximum  $\delta V/\delta t_{SR}$  result (over the entire vertical edge region).
  2. Compute the final averaged Minimum  $\delta V/\delta t_{SR}$  result (400-700mV region)
  3. Compute the final averaged Minimum  $\delta V/\delta t_{SR}$  Margin result (700-930mV region). (See Test 1.1.5 for description of Minimum  $\delta V/\delta t_{SR}$  Margin.)
- (Informative): Repeat the above procedure a second time, but with the 50pF  $C_{LOAD}$  fixture removed.

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**Observable Results:**

Falling edges:

For the 50pF C<sub>LOAD</sub>:

- Verify that the Maximum  $\delta V/\delta t_{SR}$  (over the entire vertical edge region) is less than 150mV/ns.
- Verify that the Minimum  $\delta V/\delta t_{SR}$  (over the 400-930mV region) is greater than 30mV/ns.

Rising edges:

For the 50pF C<sub>LOAD</sub>:

- Verify that the Maximum  $\delta V/\delta t_{SR}$  (over the entire vertical edge region) is less than 150mV/ns.
- Verify that the Minimum  $\delta V/\delta t_{SR}$  (over the 400-700mV region) is greater than 30mV/ns.
- Verify that the Minimum  $\delta V/\delta t_{SR}$  Margin (over the 700-930mV region) is greater than 0mV/ns.

Also, any measurements made with the 50pF C<sub>LOAD</sub> fixture removed will be reported as Informative.

**Possible Problems:** None.

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## **GROUP 3: DATA LANE HS-TX SIGNALING REQUIREMENTS**

**Overview:**

This group of tests verifies various TX requirements pertaining to Data Lane HS burst signaling. The structure of this group is intended to facilitate the execution a set of several HS-TX measurements on a single captured HS burst waveform, which includes the LP exit/entry sequences occurring before and after the burst sequence.

This test Group is applicable to Master devices only. (It is considered Not Applicable for Slave devices.)

**Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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**Test 1.3.1 – Data Lane HS Entry: Data Lane  $T_{LPX}$  Value**

**Purpose:** To verify that the duration ( $T_{LPX}$ ) of the final Data Lane LP-01 state immediately before HS transmission is greater than the minimum conformant value.

**References:**

- [1] D-PHY Specification, Section 5.2, Line 751
- [2] Ibid, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

The D-PHY Low-Power (LP) mode of operation is comprised of state transitions occurring at some implementation-specific rate less than 20M transitions/sec. Note that these state transitions may have different meanings depending on the context (Control, Escape, or LPDT mode), and do not equate to ‘bits’ on the wire. The D-PHY Specification specifies that, “All LP state periods shall be at least  $T_{LPX}$  in duration.” [1], and defines the minimum value of  $T_{LPX}$  to be 50ns [2].

In this test, the focus is specifically the duration of the last LP-01 state that occurs immediately before an HS burst sequence. The state will be measured starting at the time where the  $V_{DP}$  falling edge crosses below the maximum low-level LP threshold,  $V_{IL,MAX}$  (550mV), and ending at the time where the  $V_{DN}$  falling edge crosses below the same  $V_{IL,MAX}$  threshold. A picture of the  $T_{LPX}$  interval is shown in the figure below.

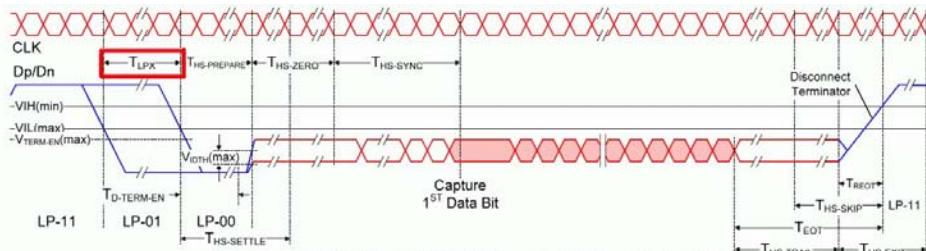


Figure 14 High-Speed Data Transmission in Bursts

Figure 1.3.1-1: Data Lane  $T_{LPX}$  Interval

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board (RTB).
- Create a condition that causes the DUT to source an HS burst sequence on Data Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods, compute the  $V_{DP}$  and  $V_{DN}$   $V_{IL,MAX}$  (550mV) crossing times.
- Measure the  $T_{LPX}$  value as the difference between the two crossing times.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For all Data Lanes:

- Verify that  $T_{LPX}$  is greater than or equal to 50ns.

**Possible Problems:**

This measurement is specified to be made into a  $Z_{ID}$  termination value of 100 ohms. Note that the RTB uses  $Z_{ID} = 100$  ohms for Data Lanes 0 and 1, but Data Lanes 2 and 3 are designed to have  $Z_{ID} = 125$  and 80 ohms, respectively. If a 3- or 4-Data Lane DUT is being tested, Data Lanes 2 and 3 will need to be connected to RTB Data Lanes 0 and 1, respectively, in order to be measured using the proper  $Z_{ID}$  value.

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### Test 1.3.2 – Data Lane HS Entry: $T_{HS-PREPARE}$ Value

**Purpose:** To verify that the duration of the final LP-00 state immediately before HS transmission ( $T_{HS-PREPARE}$ ) is within the conformance limits.

#### References:

- [1] D-PHY Specification, Section 5.14.2, Line 1040
- [2] Ibid, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

#### Discussion:

As part of the process for switching the Data Lane into HS mode, the D-PHY Specification provides a specification for the minimum time interval that a device must transmit the final LP-00 state before enabling HS mode (which occurs at the start of the  $T_{HS-ZERO}$  interval). This interval is defined as  $T_{HS-PREPARE}$ ,[1] and is shown in the figure below.

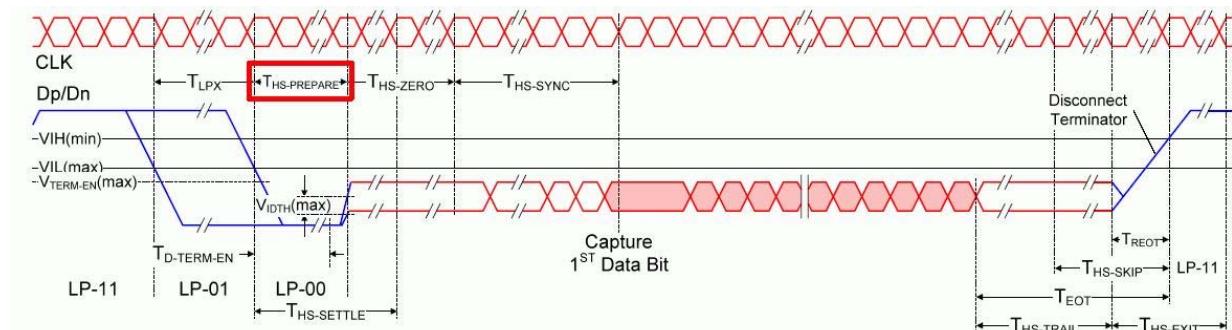


Figure 14 High-Speed Data Transmission in Bursts

Figure 1.3.2-1:  $T_{HS-PREPARE}$  Interval

In this test, the DUT will be configured to source an HS burst sequence, starting and ending with LP-11 states. The  $T_{HS-PREPARE}$  interval begins at the time where the Data Lane  $V_{DN}$  signal crosses below  $V_{IL,MAX}$  (550mV), and ends at the beginning of the extended  $T_{HS-ZERO}$  HS differential state, at the point where the differential waveform crosses above the minimum valid HS-RX differential threshold level (+/-70mV).

The measured duration of  $T_{HS-PREPARE}$  should be between  $(40ns + 4*UI)$  and  $(85ns + 6*UI)$  (where UI is the nominal HS Unit Interval for the DUT, see Test 1.4.17) in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.2.

#### Test Procedure:

- Connect the DUT to the Reference Termination Board (RTB).
- Create a condition that causes the DUT to source an HS burst sequence on Data Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods, compute  $T_{HS-PREPARE}$  as described above.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

#### Observable Results:

For all Data Lanes:

- Verify that  $T_{HS-PREPARE}$  is between  $(40ns + 4*UI)$  and  $(85ns + 6*UI)$ .

**Possible Problems:** See Possible Problems comments for Test 1.3.1. The same applies to this test.

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**Test 1.3.3 – Data Lane HS Entry:  $T_{HS-PREPARE} + T_{HS-ZERO}$  Value**

**Purpose:** To verify that the combined time of  $T_{HS-PREPARE}$  plus the time the DUT Data Lane transmitter drives the HS-0 differential state prior to transmitting the HS Sync sequence ( $T_{HS-ZERO}$ ) is greater than the minimum required duration.

**References:**

- [1] D-PHY Specification, Section 5.14.2, Line 1041
- [2] Ibid, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

As part of the process for switching the Data Lane into HS mode, the D-PHY Specification provides a specification for the minimum duration that a device must drive the extended Data HS-0 differential state prior to starting HS differential data transmission. This interval is defined as  $T_{HS-ZERO}$ ,[1] and is shown in the figure below.

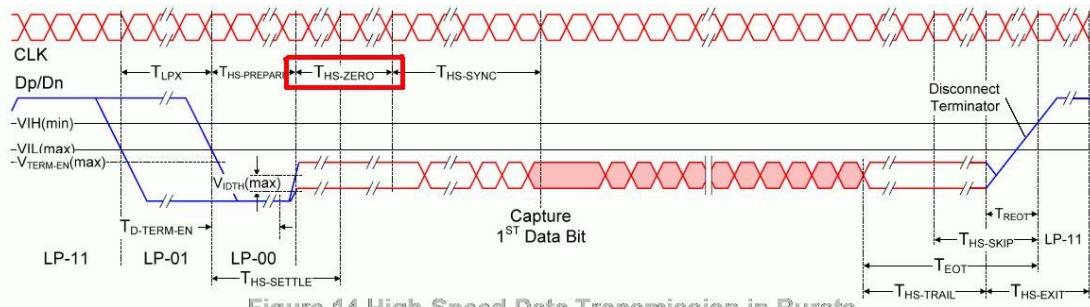


Figure 14 High-Speed Data Transmission in Bursts

Figure 1.3.3-1:  $T_{HS-ZERO}$  Interval

In this test, the DUT will be configured to source an HS burst sequence, starting and ending with LP-11 states. The ( $T_{HS-PREPARE} + T_{HS-ZERO}$ ) interval begins at the time where the Data Lane V<sub>DN</sub> signal crosses below V<sub>IL,MAX</sub> (550mV), and ends at the end of the extended T<sub>HS-ZERO</sub> HS-0 differential state, at the point corresponding to the start of the first bit of the HS Sync sequence. (Note this point is not at the first HS-1 transition, but rather three HS Unit Intervals prior, as the Sync sequence starts with 0001. Thus there is no visible delineation between the extended HS-0 and the first HS-0 of the Sync sequence.)

The measured duration of ( $T_{HS-PREPARE} + T_{HS-ZERO}$ ) should be greater than (145ns + 10\*UI) ns (where UI is the nominal HS Unit Interval for the DUT, see Test 1.4.17) in order to be considered conformance[2].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board (RTB).
- Create a condition that causes the DUT to source an HS burst sequence on Data Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods, measure ( $T_{HS-PREPARE} + T_{HS-ZERO}$ ), as described above.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For all Data Lanes:

- Verify that ( $T_{HS-PREPARE} + T_{HS-ZERO}$ ) is greater than (145ns + 10\*UI) ns.

**Possible Problems:** See Possible Problems comments for Test 1.3.1. The same applies to this test.

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**Test 1.3.4 – Data Lane HS-TX Differential Voltages ( $V_{OD(0)}$ ,  $V_{OD(1)}$ ).**

**Purpose:** To verify that the Differential Voltages ( $V_{OD(0)}$  and  $V_{OD(1)}$ ) of the DUT Data Lane HS transmitter are within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1333
- [2] Ibid, Section 8.1.1, Figure 38
- [3] Ibid, Section 8.1.1, Line 1383
- [4] Ibid, Section 8.1.1, Table 16

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{OD(0)}$  and  $V_{OD(1)}$ , which are a device's HS-TX Differential Voltage levels for the HS-0 and HS-1 states, respectively.

The D-PHY Specification states, “*The differential output voltage  $V_{OD}$  is defined as the difference of the voltages  $V_{DP}$  and  $V_{DN}$  at the  $D_p$  and  $D_n$  pins, respectively.  $V_{OD} = V_{DP} - V_{DN}$ .*” [1].

Note that this definition is potentially ambiguous in that, while it does define how the differential *signal* is computed, it does not specify how the differential voltage *amplitude* is measured for the purposes of conformance testing. (Note that a diagram is presented in [2], but this shows ‘ideal’ signaling, which is not an accurate representation for measurement purposes.) Given that there are multiple possible ways to implement a differential voltage measurement (peak-to-peak, mode-to-mode, average over entire UI, average over 40%-60% UI, etc), a common method must be chosen for consistency. For the purposes of this Test Suite, a reference-pulse-based method is defined, where the reference HS-1 and HS-0 levels are obtained from an averaged waveform corresponding to a defined reference data pattern.

The primary motivation for using a pulse-based methodology is to provide consistency and repeatability, and make the measurement less sensitive to the data-dependencies inherent to HS burst signaling. Because the amplitude of shorter run-length pulses can be noticeably smaller for D-PHY than longer runs of ones or zeros (particularly at higher data rates), and also the fact that D-PHY does not use a DC-balanced signaling/coding scheme as other high-speed serial technologies do (e.g., 8B/10B), the number and frequency of ones and zeroes in a particular HS burst is not guaranteed, and can vary greatly depending on the burst contents. For this reason, simple averaging of the HS-1 and HS-0 levels in a given HS burst can sometimes yield inconsistent results, if the burst contents are not taken into consideration.

Consistent HS-1 and HS-0 amplitude measurements ( $V_{OD(1)}$  and  $V_{OD(0)}$ , respectively) are also important as they serve as reference levels for the HS rise and fall time measurements (see Tests 1.3.11 and 1.3.12). Thus, any variability in the  $V_{OD}$  measurements will translate into variability in the rise/fall measurements.

Also, the HS-1 and HS-0 amplitude measurements are especially sensitive due to several factors (see Possible Problems, below), and must be carefully measured in order to meet the  $\Delta V_{OD}$  requirement of Test 1.3.5.

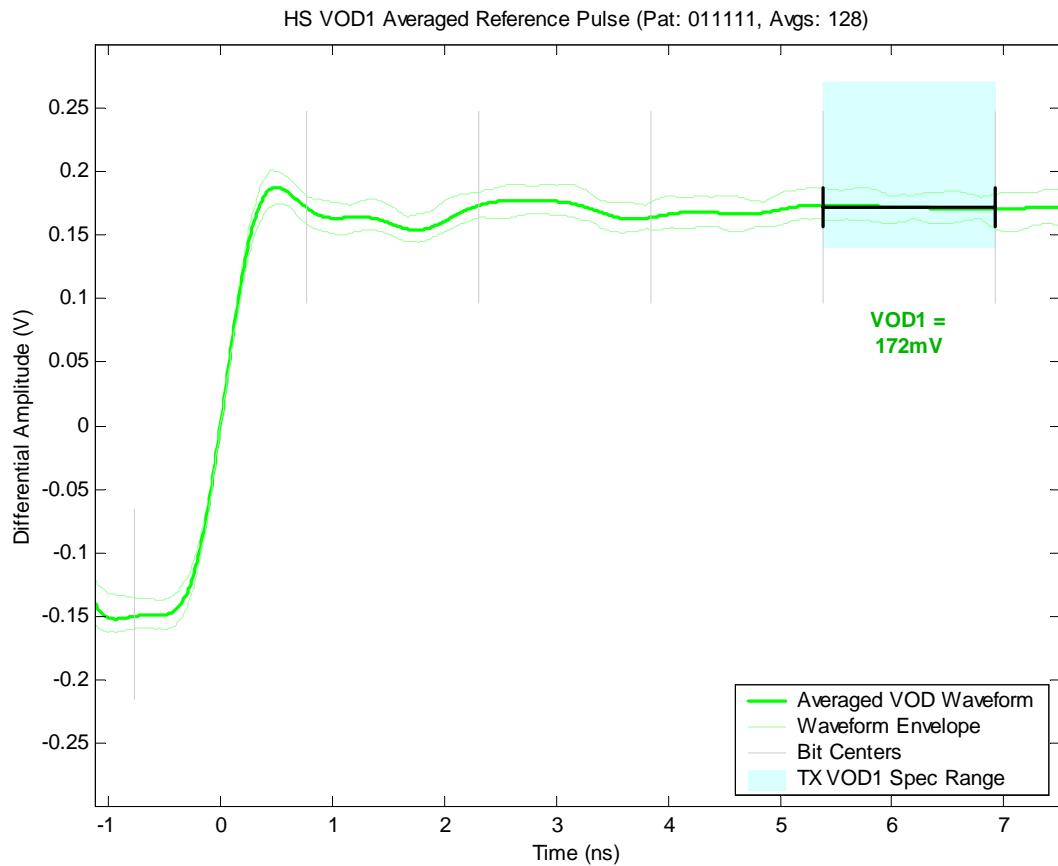
The methodology chosen for this test will measure the  $V_{OD(1)}$  and  $V_{OD(0)}$  amplitudes based on the reference data patterns 011111 and 100000, respectively. These patterns were specifically chosen for several reasons: 1) They have sufficient run length (5 bits) to allow reasonable stabilizing of the steady-state amplitude level, including capacitive charging effects, and reflections caused by impedance discontinuities, and 2) They are relatively prevalent in typical D-PHY HS data sequences, for most CSI/DSI imaging applications and data formats. Longer run-length patterns might yield slightly more consistent measurements, however they are typically less frequent, and thus would make averaging more difficult. The 5-bit run-length sequence was empirically determined to provide a

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suitable run length for stable measurements, while also being common enough to allow for high averaging with a minimum amount of captured waveform data.

In this test, averaged waveforms will be constructed for the two reference patterns, from waveform data extracted from the HS burst data. (Note the HS burst must be separately verified to contain these patterns in order for the measurements to be performed. Also, data from multiple separate bursts may be used if necessary.) The averaged waveform shall be constructed by horizontally aligning a minimum of 128 individual waveforms to a common reference point, which will be the zero crossing time of the first transition. The result should produce an averaged waveform, similar to Figure 1.3.4-1, below.

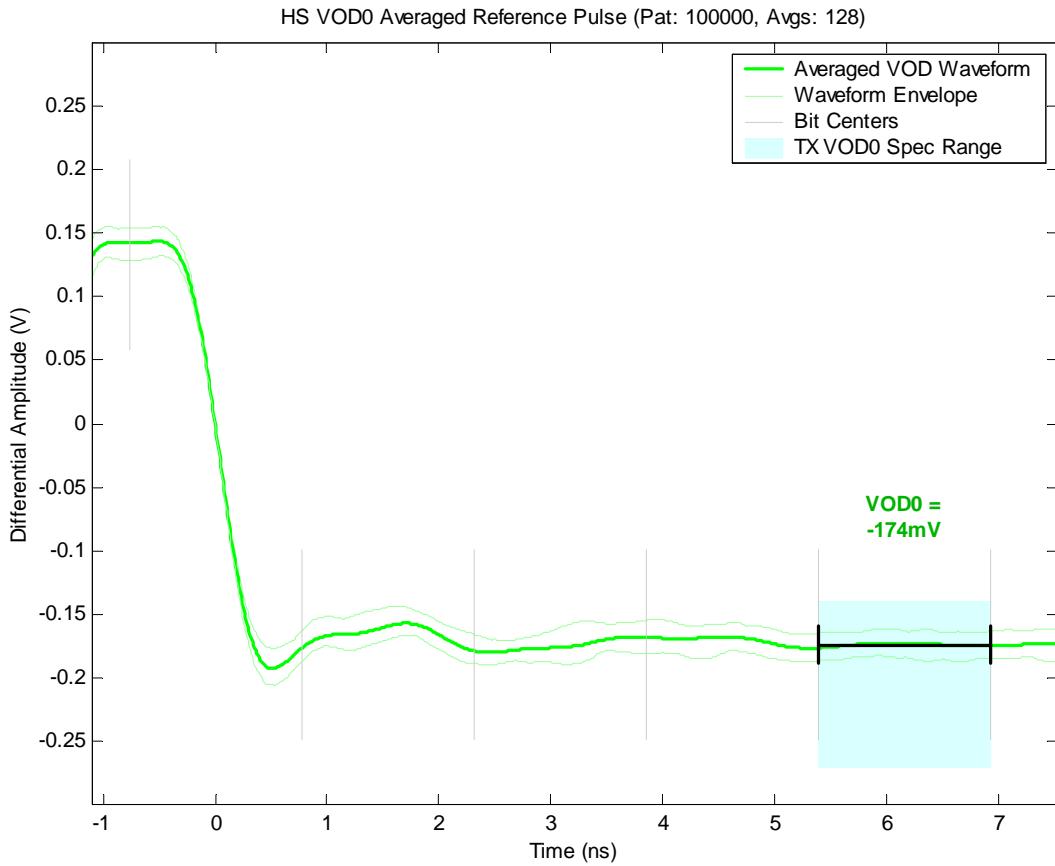
Once the averaged waveform is obtained, the  $V_{OD(1)}$  value will be measured as the mean of all samples for the averaged waveform that fall between the centers of the fourth and fifth ‘1’ bits, as shown in Figure 1.3.4-1 below.



**Figure 1.3.4-1: Sample Data Lane Averaged  $V_{OD(1)}$  Reference Pulse and Measurement**

The measurement will then be repeated for the  $V_{OD(0)}$  reference pattern, averaging the samples between the fourth and fifth ‘1’ bits, as shown in Figure 1.3.4-2, below.

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**Figure 1.3.4-2: Sample Data Lane Averaged  $V_{OD(0)}$  Reference Pulse and Measurement**

Furthermore, the specification also contains a stipulation that the  $V_{OD}$  requirement shall be met “*when driving into load impedance anywhere in the  $Z_{ID}$  range.*”[3]. Therefore, this measurement will be performed for 3  $Z_{ID}$  cases: nominal (100 ohms), maximum (125 ohms), and minimum (80 ohms).

For all  $Z_{ID}$  cases, and all Data Lanes, the averaged  $V_{OD(1)}$  value must be within the range of 140 to 270mV in order to be considered conformant[4]. The averaged  $V_{OD(0)}$  value must be within the range of -140 to -270mV in order to be considered conformant[4]. (Note that this corresponds to a differential peak-to-peak voltage value of 280 to 540mVppd.)

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that Data Lane 0 is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source an HS burst sequence on Data Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods, measure  $V_{OD(1)}$  and  $V_{OD(0)}$  as described above.
- Repeat the previous steps two additional times, once with Data Lane 0 connected to the  $Z_{ID} = 125$  ohms Lane of the RTB, and again with Data Lane 0 connected to  $Z_{ID} = 80$  ohms.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

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**Observable Results:**

For all three  $Z_{ID}$  cases, and for all Data Lanes:

- Verify that  $V_{OD(1)}$  is between 140 and 270mV.
- Verify that  $V_{OD(0)}$  is between -140 and -270mV.

**Possible Problems:**

Both the differential voltage ( $V_{OD}$ ) and differential voltage mismatch ( $\Delta V_{OD}$ ) tests are especially sensitive measurements, and can be greatly affected by the test setup. If a device is found to fail this test, care should be taken to verify and double check the test setup. Ensure that a DSO calibration has been performed, as well as a probe calibration/deskew (as these are often separate procedures on some instruments.) Also, make sure that the probe connections to the DUT are clean and symmetric for the Dp and Dn signals.

Also, the accuracy of these measurements can be affected by the vertical gain setting of the DSO. Typically these measurements are made on a single HS burst waveform, which also contains LP signaling before and after the burst (on which other measurements may be made at the same time, e.g.,  $T_{LPX}$ ,  $T_{HS-PREPARE}$ ,  $T_{HS-ZERO}$ , etc). If the DSO's vertical gain is configured so that the entire height of the LP signaling appears on the screen, the resolution of the HS portions of the signal will be decreased, as compared to the case where the vertical gain is optimized for just the HS signaling (and the LP signaling is allowed to extend off the top off the screen). This configuration will yield greater accuracy for the HS measurements (i.e., lower quantization noise/error), albeit with the tradeoff of having to make separate waveform captures for the LP-related measurements.

Also note that this test contains a similar issue as was detailed in the Possible Problems section for Test 1.3.1. While Test 1.3.1 is only specified to be measured using the 100 ohm  $Z_{ID}$  value, this test requires all three  $Z_{ID}$  cases. Because the RTB is intentionally designed with different  $Z_{ID}$  values for Lanes 2 and 3 (125 and 80 ohms, respectively, versus 100 ohms for Data Lanes 0 and 1, and Clock), the transmitter under test must be moved to the different RTB lanes in order to test the different  $Z_{ID}$  cases. (This may require the use of short SMA cables to connect the Clock Lane to the RTB if the clock is still required for measurements. Note in this case, short, matched-length cables should be used on both the Clock and Data Lanes, to ensure that no added skew is introduced.)

Also note that it is recommended that the averaging for the reference pulse waveforms (for this, as well as all other tests that use reference pulse waveforms, e.g.,  $V_{OHHS}$  and the HS Rise/Fall Time tests, for both Clock and Data Lanes) be performed starting with the waveform data at the end of the burst (and worked backwards toward the beginning of the burst), as it has been observed that in some cases transient effects introduced by some high impedance probes can introduce a small error in the HS common-mode levels at the beginning of the bursts, which can be significant enough in some cases to affect the results for all of the pulse-based HS amplitude measurements ( $V_{OD(0/1)}$ ,  $dV_{OD}$ ,  $V_{OHHS}$ ).

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**Test 1.3.5 – Data Lane HS-TX Differential Voltage Mismatch ( $\Delta V_{OD}$ )**

**Purpose:** To verify that the Differential Voltage Mismatch ( $\Delta V_{OD}$ ) of the DUT Data Lane HS transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1345
- [2] Ibid, Section 8.1.1, Table 16

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $\Delta V_{OD}$ , which is a device's HS-TX Differential Voltage Mismatch.

The D-PHY Specification states, “*The output differential voltage mismatch  $\Delta V_{OD}$  is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state  $V_{OD(1)}$  and the differential output voltage in the Differential-0 state  $V_{OD(0)}$ . This is expressed by  $\Delta V_{OD} = |V_{OD(1)}| - |V_{OD(0)}|$* ” [1].

In this test, the numerical  $V_{OD(0)}$  and  $V_{OD(1)}$  results obtained in the previous test (see Test 1.3.4) will be used to compute the  $\Delta V_{OD}$  result. The difference of the absolute values of these two values will be taken to produce  $\Delta V_{OD}$ . This will be performed using the data from all three  $Z_{ID}$  test cases.

For all cases, the absolute value of  $\Delta V_{OD}$  must be less than 10mV in order to be considered conformant [2].

**Test Setup:** None.

**Test Procedure:**

- Obtain the numerical  $V_{OD(0)}$  and  $V_{OD(1)}$  results from Test 1.3.4, for all three  $Z_{ID}$  cases, and all Data Lanes.
- For each case/Lane, compute the  $\Delta V_{OD}$  result as described above.

**Observable Results:**

For all three  $Z_{ID}$  cases, and for all Data Lanes:

- Verify that the absolute value of  $\Delta V_{OD}$  is less than 10mV.

**Possible Problems:**

See Possible Problems comments for Test 1.3.4. The same applies to this test.

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**Test 1.3.6 – Data Lane HS-TX Single-Ended Output High Voltages ( $V_{OHHS(DP)}$ ,  $V_{OHHS(DN)}$ )**

**Purpose:** To verify that the Single-Ended Output High Voltages ( $V_{OHHS(DP)}$  and  $V_{OHHS(DN)}$ ) of the DUT Data Lane HS transmitter are less than the maximum conformance limit.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1336
- [2] Ibid, Section 8.1.1, Line 1383
- [3] Ibid, Section 8.1.1, Table 16

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{OHHS}$ , which is a device's HS-TX Output High Voltage.

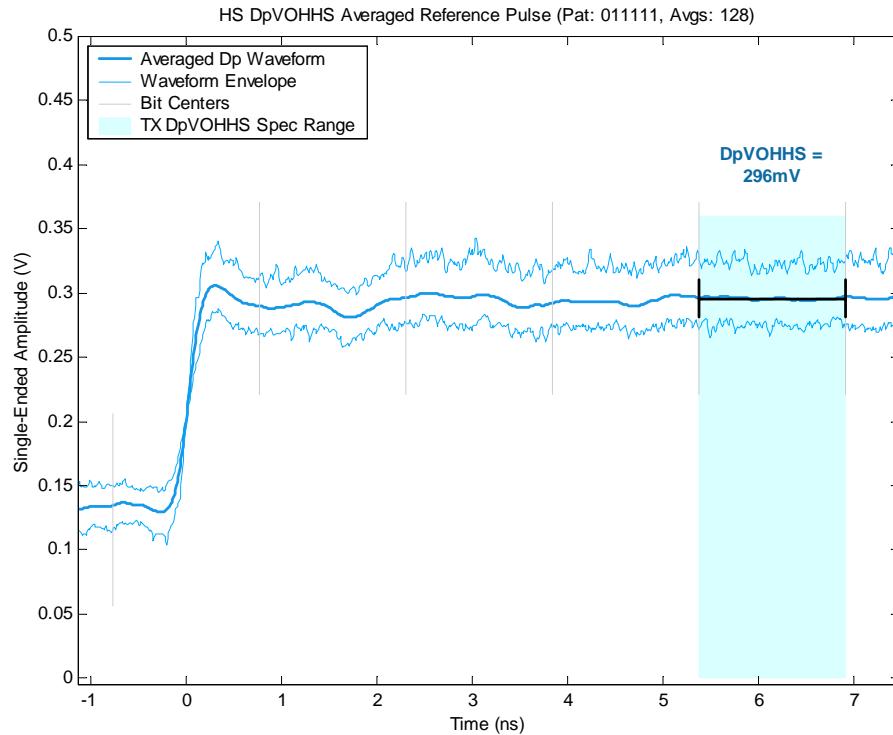
The D-PHY Specification states, “*The output voltages  $V_{DP}$  and  $V_{DN}$  at the  $D_p$  and  $D_n$  pins shall not exceed the High-Speed output high voltage  $V_{OHHS}$ .  $V_{OLHS}$  is the High-Speed output, low voltage on  $D_p$  and  $D_n$  and is determined by  $V_{OD}$  and  $V_{CMTX}$ . The High-Speed  $V_{OUT}$  is bounded by the minimum value of  $V_{OLHS}$  and the maximum value of  $V_{OHHS}$ .*” [1].

It is worth noting that  $V_{OHHS}$  is one of three basic amplitude specifications for D-PHY HS signaling: The HS differential voltage ( $V_{OD}$ ) has a TX conformance range of 140 to 270mVpk (which is 280 to 540mVppd). The HS common-mode voltage ( $V_{CMTX}$ ) has a TX conformance range of 150 to 250mV. Thus, it is interesting to note that a device configured to use the maximum  $V_{OD}$  and  $V_{CMTX}$  values will actually violate the maximum  $V_{OHHS}$  limit of 360mV, as the transmitted  $V_{OHHS}$  in this case would be  $250 + 135 = 385$ mV. Thus, in order to transmit at the maximum  $V_{OHHS}$  level, a device would need to decrease either its  $V_{OD}$  or  $V_{CMTX}$  setting from the maximum value.

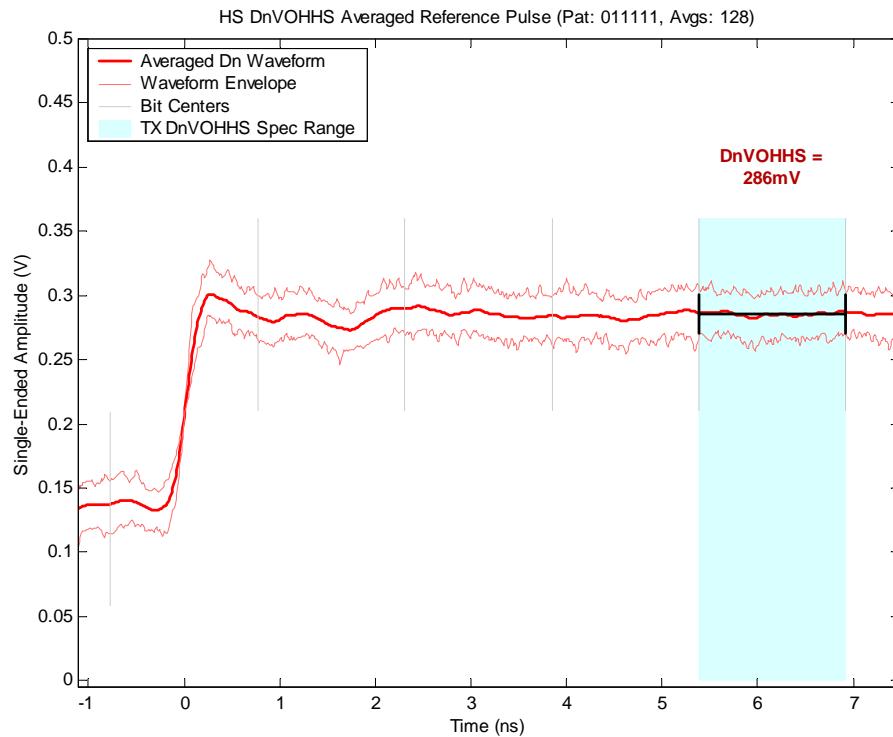
Like the  $V_{OD(0)}$  and  $V_{OD(1)}$  measurements of Test 1.3.4, the exact method used for measuring  $V_{OHHS}$  must be clearly specified, as different amplitude measurement methods will significantly impact the measured result. For consistency, this test will use the same reference-pulse-based approach as Test 1.3.4, and will use the same 011111 reference pattern as the  $V_{OD(1)}$  measurement, except the methodology will be applied separately to the *single-ended*  $V_{DP}$  and  $V_{DN}$  signals (rather than the differential  $V_{OD}$  signal) in order to create averaged 011111 reference pulses for  $D_p$  and  $D_n$ . (Note that in this context, the 011111 pattern refers to the symbol levels of the single-ended signals, and not the differential HS data pattern.)

In this test, a sample of the DUTs HS Data Lane signaling will be captured using a real-time DSO. The  $V_{DP}$  and  $V_{DN}$  single-ended waveforms will be captured using separate channels of the DSO, and processed independently. Averaged reference pulses for the 011111 symbol pattern will be constructed separately for the  $V_{DP}$  and  $V_{DN}$  signals, using the same methodology described in Test 1.3.4, and the same minimum averaging factor of 128. The  $V_{OHHS}$  values for  $V_{DP}$  and  $V_{DN}$  (which will be denoted as  $V_{OHHS(DP)}$  and  $V_{OHHS(DN)}$  for the purposes of this test) will be computed using the same methodology as was used for  $V_{OD(1)}$ , by computing the mean value of all samples for the averaged waveform that fall between the centers of the fourth and fifth ‘1’ bits, as shown in Figures 1.3.6-1 and 1.3.6-2 below, for the  $V_{DP}$  and  $V_{DN}$  cases, respectively.

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**Figure 1.3.6-1: Sample Data Lane Averaged  $V_{OHHS(DP)}$  Reference Pulse and Measurement**



**Figure 1.3.6-2: Sample Data Lane Averaged  $V_{OHHS(DN)}$  Reference Pulse and Measurement**

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The measurement will also be performed for all three  $Z_{ID}$  cases (see Test 1.3.4 Discussion), as conformance over the entire  $Z_{ID}$  range is also specified for this requirement [2].

For all  $Z_{ID}$  cases and all Data Lanes, the  $V_{OHHS}$  results for both  $V_{DP}$  and  $V_{DN}$  must be less than 360mV in order to be considered conformant [3].

**Test Setup:** See Appendix B.1.2

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that Data Lane 0 is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source an HS burst sequence on Data Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods, measure  $V_{OHHS(DP)}$  and  $V_{OHHS(DN)}$  as described above.
- Repeat the previous steps two additional times, once with Data Lane 0 connected to the  $Z_{ID} = 125$  ohms Lane of the RTB, and again with Data Lane 0 connected to  $Z_{ID} = 80$  ohms.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For all three  $Z_{ID}$  cases, and for all Data Lanes:

- Verify that  $V_{OHHS(DP)}$  is less than 360mV.
- Verify that  $V_{OHHS(DN)}$  is less than 360mV.

**Possible Problems:**

See Possible Problems comments for Test 1.3.4. The same applies to this test.

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**Test 1.3.7 – Data Lane HS-TX Static Common-Mode Voltages ( $V_{CMTX(1)}$ ,  $V_{CMTX(0)}$ )**

**Purpose:** To verify that the Static Common-Mode Voltages ( $V_{CMTX(1)}$ , and  $V_{CMTX(0)}$ ) of the DUT Data Lane HS transmitter are within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1340
- [2] Ibid, Section 8.1.1, Figure 39
- [3] Ibid, Section 8.1.1, Line 1383
- [4] Ibid, Section 8.1.1, Table 16

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{CMTX}$ , which is a device's HS-TX Static Common-Mode Voltage.

The common-mode voltage  $V_{CMTX}$  is defined as, “*the arithmetic mean value of the voltages at the  $D_p$  and  $D_n$  pins:  $V_{CMTX} = (V_{DP} + V_{DN})/2$* ” [1].

Because of various types of signal distortions that may occur, it is possible for  $V_{CMTX}$  to have different values when a Differential-1 vs. Differential-0 state is being driven. Because of this,  $V_{CMTX}$  must be measured separately for both the 0 and 1 states, at the “static” value corresponding to the settled voltage at the center of the UI (as opposed to the “dynamic” AC fluctuations that occur at the bit transitions, which are covered by a separate specification, see Tests 1.3.9 and 1.3.10). The specification includes a figure showing various different types of signal distortions that can occur [2]. This figure is reproduced below, with the static common-mode distortion type highlighted in red.

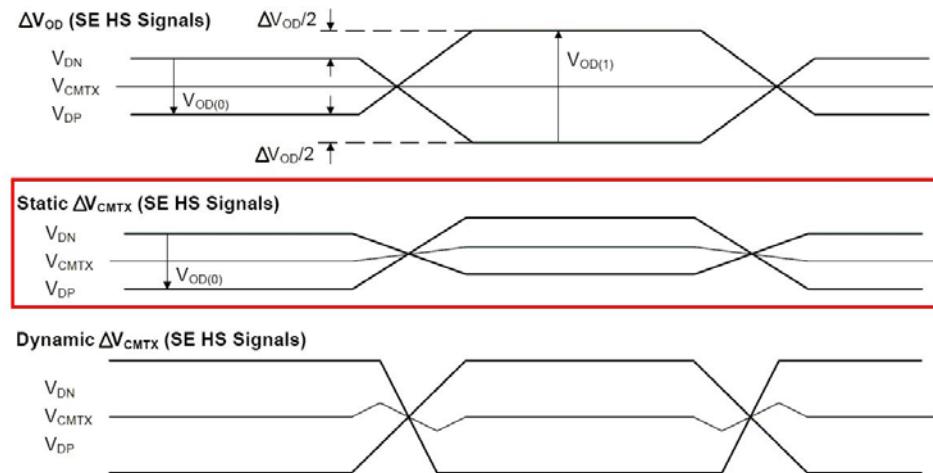


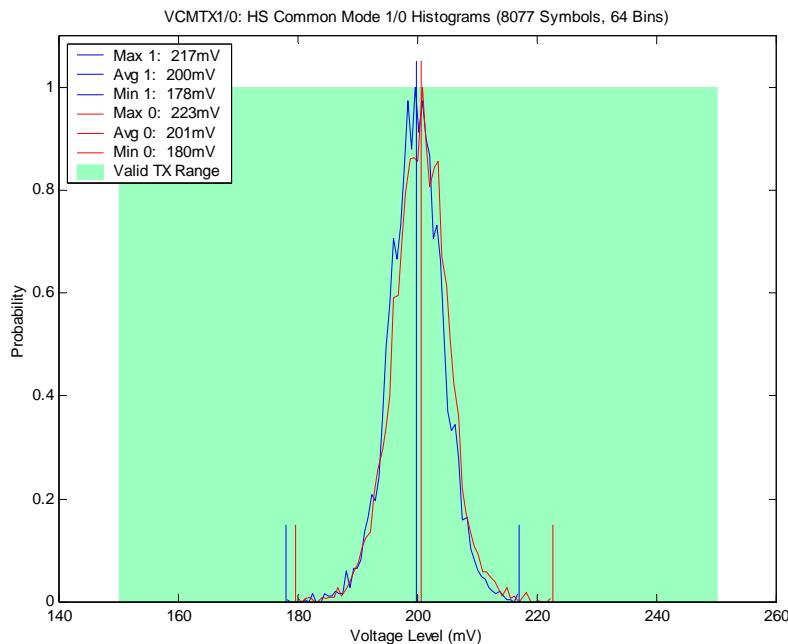
Figure 39 Possible  $\Delta V_{CMTX}$  and  $\Delta V_{OD}$  Distortions of the Single-ended HS Signals

Figure 1.3.7-1: Static  $V_{CMTX}$  Distortion

In this test, a portion of the DUTs HS Data Lane signaling will be captured using a real-time DSO. The  $V_{DP}$  and  $V_{DN}$  single-ended waveforms will be mathematically averaged together (as described above) to create the  $V_{CMTX}$  common-mode waveform. The  $V_{CMTX}$  waveform will be sampled at the center of each UI (using either the Clock Lane waveform as the timing reference, or an ideal linear-fit constant frequency clock recovered from the Data Lane waveform), corresponding to each Differential-1 and Differential-0 state in the HS burst. The average common-mode voltage observed over a minimum of 5,000 Differential-1 UIs will be computed as  $V_{CMTX(1)}$ , and the

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average common-mode voltage observed over a minimum of 5,000 Differential-0 UIs will be computed as  $V_{CMTX(0)}$ . A sample measurement is shown in the figure below, showing the max, min, and mean common-mode levels for the 0 and 1 bits of an HS burst.



**Figure 1.3.7-2: Sample  $V_{CMTX}$  Histograms**

This measurement shall be performed for all three  $Z_{ID}$  cases [3] (see Discussion, Test 1.3.4), and for all Data Lanes.

For all cases, the values for both  $V_{CMTX(1)}$  and  $V_{CMTX(0)}$  must be between 150 to 250mV in order to be considered conformant [4].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that Data Lane 0 is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source an HS burst sequence on Data Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods, measure  $V_{CMTX(1)}$  and  $V_{CMTX(0)}$ , as described above.
- Repeat the previous steps two additional times, once with Data Lane 0 connected to the  $Z_{ID} = 125$  ohms Lane of the RTB, and again with Data Lane 0 connected to  $Z_{ID} = 80$  ohms.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For all three  $Z_{ID}$  cases, and for all Data Lanes:

- Verify that  $V_{CMTX(1)}$  is between 150 and 250mV.
- Verify that  $V_{CMTX(0)}$  is between 150 and 250mV.

**Possible Problems:** See Possible Problems comments for Test 1.3.4. The same applies to this test.

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**Test 1.3.8 – Data Lane HS-TX Static Common-Mode Voltage Mismatch ( $\Delta V_{CMTX(1,0)}$ )**

**Purpose:** To verify that the Static Common-Mode Voltage Mismatch ( $\Delta V_{CMTX(1,0)}$ ) of the DUT Data Lane HS transmitter is less than the maximum conformance limit.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1355
- [2] Ibid, Section 8.1.1, Table 16

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $\Delta V_{CMTX(1,0)}$ , which is a device's HS-TX Static Common-Mode Voltage Mismatch.

In Test 1.3.7, the Data Lane HS-TX static common-mode levels were measured as  $V_{CMTX(1)}$  and  $V_{CMTX(0)}$ . In addition to specifying requirements for the absolute voltages for these two values, the specification also defines a requirement on their symmetry, i.e., how matched they are to each other.

The specification states, “*The static common-mode voltage mismatch between the Differential-1 and Differential-0 state is given by:  $\Delta V_{CMTX(1,0)} = (V_{CMTX(1)} - V_{CMTX(0)})/2$* ”[1].

In this test, the numerical results from Test 1.3.7 for  $V_{CMTX(1)}$  and  $V_{CMTX(0)}$  will be used to compute the Data Lane HS-TX Static Common-Mode Voltage Mismatch,  $\Delta V_{CMTX(1,0)}$ . The result for  $\Delta V_{CMTX(1,0)}$  will be computed as one-half of the difference of  $V_{CMTX(1)}$  minus  $V_{CMTX(0)}$ . The measurement will be computed and reported separately for each  $Z_{ID}$  case, and for each Data Lane.

For all cases, the value for  $\Delta V_{CMTX(1,0)}$  must be less than 5mV in order to be considered conformant [2].

**Test Setup:** None.

**Test Procedure:**

- Obtain the numerical Data Lane 0  $V_{CMTX(1)}$  and  $V_{CMTX(0)}$  results from Test 1.3.7.
- Compute the Data Lane 0  $\Delta V_{CMTX(1,0)}$  result as described above, for each  $Z_{ID}$  case.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For all three  $Z_{ID}$  cases, and for all Data Lanes:

- Verify that  $\Delta V_{CMTX(1,0)}$  is less than 5mV.

**Possible Problems:** None.

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**Test 1.3.9 – Data Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz ( $\Delta V_{CMTX(LF)}$ )**

**Purpose:** To verify that the AC Common-Mode Signal Level Variations between 50 and 450MHz ( $\Delta V_{CMTX(LF)}$ ) of the DUT Data Lane HS transmitter are less than the maximum allowable limit.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1357
- [2] Ibid, Section 8.1.1, Figure 39
- [3] Ibid, Section 8.1.1, Table 17

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $\Delta V_{CMTX(LF)}$ , which is a device's HS-TX Dynamic Common-Level Variations between 50 and 450MHz.

The specification defines several requirements regarding a device's common-mode signaling. These specifications each measure slightly different distortions of the common-mode signal, which can result from very specific and distinct types of waveform asymmetry. "Dynamic" (or AC) variations are typically caused by an asymmetry in the rise/fall times of the single-ended HS signals.

The specification states, "*The transmitter shall send data such that the high frequency and low frequency common-mode voltage variations do not exceed  $\Delta V_{CMTX(HF)}$  and  $\Delta V_{CMTX(LF)}$ , respectively.*" [1].

The specification includes a figure showing various different types of signal distortions that can occur [2]. This figure is reproduced below, with the dynamic common-mode distortion type highlighted in red.

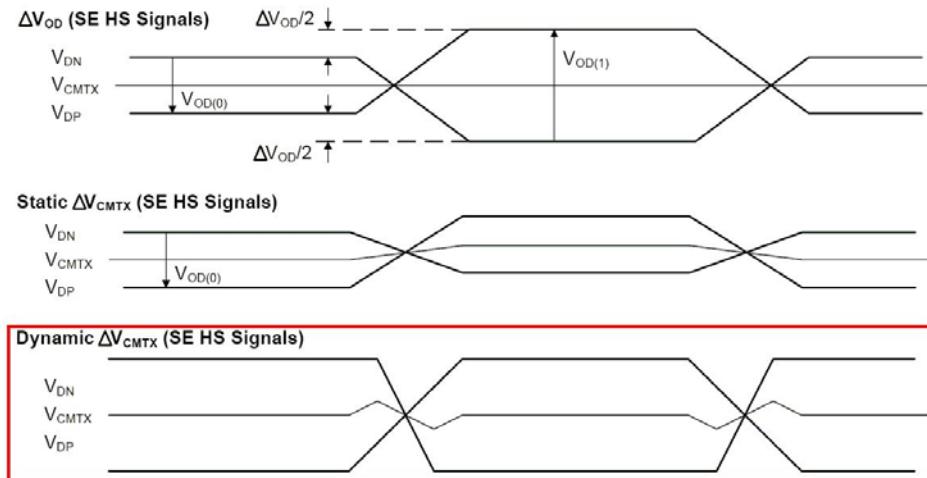


Figure 39 Possible  $\Delta V_{CMTX}$  and  $\Delta V_{OD}$  Distortions of the Single-ended HS Signals

Figure 1.3.9-1: Dynamic  $V_{CMTX}$  Distortion

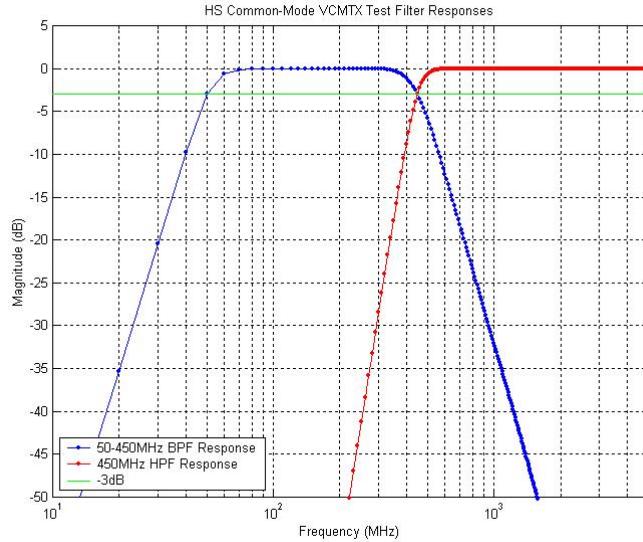
In this test, the  $V_{CMTX}$  common-mode signal will be captured using a real-time DSO, in the same manner as was used for the HS-TX Static Common-Mode Voltages measurement (see Test 1.3.7). However for this test, rather than measuring the average 1/0 DC levels, the AC voltage will be measured, specifically for the frequency range between 50 and 450MHz.

In order to isolate the energy in the frequency band of interest, some methodology must be employed to remove the energy that is above 450MHz and below 50MHz. While there are different possible methods that can

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accomplish this, the chosen implementation for this test is through the use of post-processing filters, which are specifically designed to greatly attenuate the energy outside the band of interest. (Note that because the spec does not define a particular test filter as part of the requirement definition, the measured result may be heavily dependent on the chosen implementation methodology. Nonetheless, a common filter must be chosen for conformance testing purposes.)

The selected implementation uses a 8<sup>th</sup>-order Butterworth IIR bandpass filter as the test filter, with -3dB cutoff frequencies of 50 and 450MHz. The frequency response of the test filter is shown in the figure below. The raw  $V_{CMTX}$  waveform is passed through the filter prior to making the peak voltage measurement. The peak voltage of the bandpass-filtered  $V_{CMTX}$  waveform is measured to produce the final  $V_{CMTX(LF)}$  result.



**Figure 1.3.9-2:  $V_{CMTX}$  Test Filter Responses (50-450MHz BPF shown in blue)**

Note that unlike several of the previous tests that were required to be performed for all three  $Z_{ID}$  values, this requirement is NOT required by the specification for this measurement. Thus, the measurement will be performed using the nominal 100-ohm  $Z_{ID}$  value, for all Data Lanes.

For all Lanes,  $\Delta V_{CMTX(LF)}$  must be less than 25mV<sub>PEAK</sub> in order to be considered conformant [3].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board (RTB).
- Create a condition that causes the DUT to source an HS burst sequence on Data Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods as described above, measure  $V_{CMTX(LF)}$ .
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For  $Z_{ID} = 100\text{ohms}$ , and for all Data Lanes:

- Verify that  $\Delta V_{CMTX(LF)}$  is less than 25mV<sub>PEAK</sub>.

**Possible Problems:** See Possible Problems comments for Test 1.3.1. The same applies to this test.

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**Test 1.3.10 – Data Lane HS-TX Dynamic Common-Level Variations Above 450MHz ( $\Delta V_{CMTX(HF)}$ )**

**Purpose:** To verify that the AC Common-Mode Signal Level Variations above 450MHz ( $\Delta V_{CMTX(HF)}$ ) of the DUT Data Lane HS transmitter are less than the maximum allowable limit.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1357
- [2] Ibid, Section 8.1.1, Table 17

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $\Delta V_{CMTX(HF)}$ , which is a device's HS-TX Dynamic Common-Level Variations above 450MHz.

The specification states, “*The transmitter shall send data such that the high frequency and low frequency common-mode voltage variations do not exceed  $\Delta V_{CMTX(HF)}$  and  $\Delta V_{CMTX(LF)}$ , respectively.*” [1].

Note that the procedure for this test is essentially identical to the previous  $\Delta V_{CMTX(LF)}$  test (see Test 1.3.9), except that a highpass test filter is used rather than a bandpass filter, and the result is measured as  $V_{RMS}$  rather than  $V_{PEAK}$ . The test filter for this test is an 8<sup>th</sup>-order Butterworth highpass filter, with a cutoff frequency of 450MHz, (see Figure 1.3.9-2, Test 1.3.9).  $\Delta V_{CMTX(HF)}$  is measured as the RMS value of the highpass-filtered  $V_{CMTX}$  waveform.

Note that unlike several of the previous tests that were required to be performed for all three  $Z_{ID}$  values, this requirement is NOT required by the specification for this measurement. Thus, the measurement will be performed using the nominal 100-ohm  $Z_{ID}$  value, for all Data Lanes.

For all cases, the value of  $\Delta V_{CMTX(HF)}$  must be less than 15mV<sub>RMS</sub> in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board (RTB).
- Create a condition that causes the DUT to source an HS burst sequence on Data Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods, measure  $\Delta V_{CMTX(HF)}$  as described above.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For  $Z_{ID} = 100\text{ohms}$ , and for all Data Lanes:

- Verify that  $\Delta V_{CMTX(HF)}$  is less than 15mV<sub>RMS</sub>.

**Possible Problems:** See Possible Problems comments for Test 1.3.1. The same applies to this test.

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**Test 1.3.11 – Data Lane HS-TX 20%-80% Rise Time ( $t_R$ )**

**Purpose:** To verify that the 20%-80% Rise Time ( $t_R$ ) of the DUT Data Lane HS transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1376
- [2] Ibid, Section 8.1.1, Table 17

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $t_R$ , which is a device's High-Speed TX 20%-80% Rise Time.

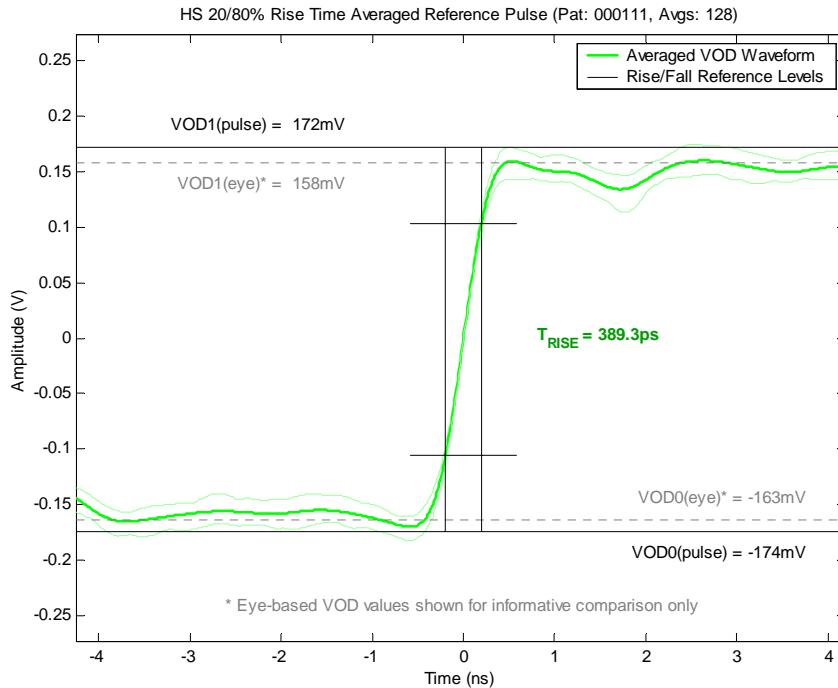
The D-PHY Specification states, “*The rise and fall times,  $t_R$  and  $t_F$ , are defined as the transition time between 20% and 80% of the full HS signal swing. The driver shall meet the  $t_R$  and  $t_F$  specifications for all allowable  $Z_{ID}$ .*” [1].

This test uses a similar methodology to the  $V_{OD}$  amplitude measurement of Test 1.3.4, in that the rise and fall time measurements will be performed on averaged waveforms for defined data patterns. While the  $V_{OD}$  test used a 011111 data pattern (and its inverse) to determine the reference  $V_{OD(0)}$  and  $V_{OD(1)}$  voltage levels, this test will use a 000111 data pattern to measure the HS rise time.

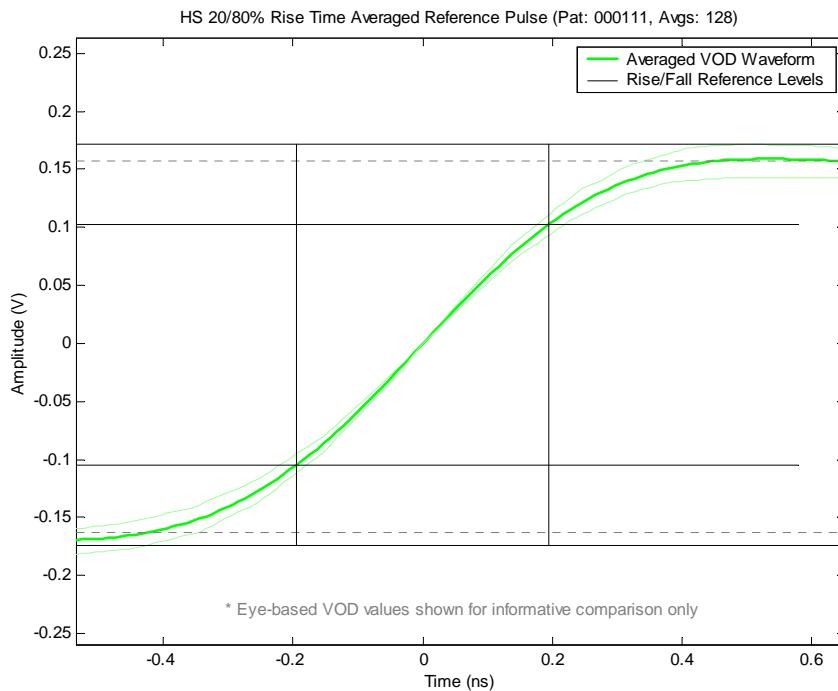
The manner for constructing the averaged rise time waveform is identical to that used for the  $V_{OD}$  test, in that the individual reference waveforms will be horizontally aligned to the 0V crossing point, and then averaged. Again, a minimum of 128 waveforms shall be used to compute the averaged signal. Note that this pattern should be fairly prevalent in typical D-PHY applications, and thus greater averaging may be employed (and across multiple bursts, if desired) in order to improve the consistency and repeatability of the measurement.

The 20/80% rise time of the averaged waveform will be measured with respect to the reference  $V_{OD(0)}$  and  $V_{OD(1)}$  levels that were determined in Test 1.3.4. A sample averaged waveform and measurement is shown in Figure 1.3.11-1, below.

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**Figure 1.3.11-1: Sample HS Rise Time Reference Waveform and Measurement**



**Figure 1.3.11-2: Sample HS Rise Time Reference Waveform and Measurement  
(Zoomed to show transition)**

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(Note that in the examples above, the reference  $V_{OD(0)}$  and  $V_{OD(1)}$  levels are shown as solid black lines, however the mean HS-1 and HS-0 symbol levels (measured at the center of each UI, across the entire burst) are also shown by the dotted gray lines. These are only shown here for informative purposes, however they demonstrate how the averaged HS-1/0 levels can differ from the reference  $V_{OD(0)}$  and  $V_{OD(1)}$  values computed using the reference waveform methodology of Test 1.3.4.)

In this test, a sample of the DUTs HS Data Lane signaling will be captured using a real-time DSO. The differential waveform will be computed as difference of the positive and negative single-ended waveforms ( $V_{DP} - V_{DN}$ ). The averaged rise time waveform will be computed as described above. The 20%-80% Rise Time ( $t_R$ ) of the averaged reference waveform will be measured relative to the reference  $V_{OD(0)}$  and  $V_{OD(1)}$  amplitude levels determined previously (see Test 1.3.4), to produce the final  $t_R$  result.

Note that because the rise/fall time specification includes a condition to be met into all allowable  $Z_{ID}$  values, this measurement will be performed for 3  $Z_{ID}$  cases: nominal (100 ohms), maximum (125 ohms), and minimum (80 ohms).

For all cases, the value of  $t_R$  must be greater than 150ps and less than 0.3 UI (where UI is the nominal HS Unit Interval for the DUT, see Test 1.4.17) in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that Data Lane 0 is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source an HS burst sequence on Data Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods, measure  $t_R$  as described above.
- Repeat the previous steps two additional times, once with Data Lane 0 connected to the  $Z_{ID} = 125$  ohms Lane of the RTB, and again with Data Lane 0 connected to  $Z_{ID} = 80$  ohms.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For all three  $Z_{ID}$  cases, and for all Data Lanes:

- Verify that  $t_R$  is greater than 150ps and less than 0.3UI.

**Possible Problems:**

See Possible Problems comments for Test 1.3.4. The same applies to this test.

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**Test 1.3.12 – Data Lane HS-TX 80%-20% Fall Time ( $t_F$ )**

**Purpose:** To verify that the 80%-20% Fall Time ( $t_F$ ) of the DUT Data Lane HS transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1376
- [2] Ibid, Section 8.1.1, Table 17

**Resource Requirements:** See Appendix A.1.

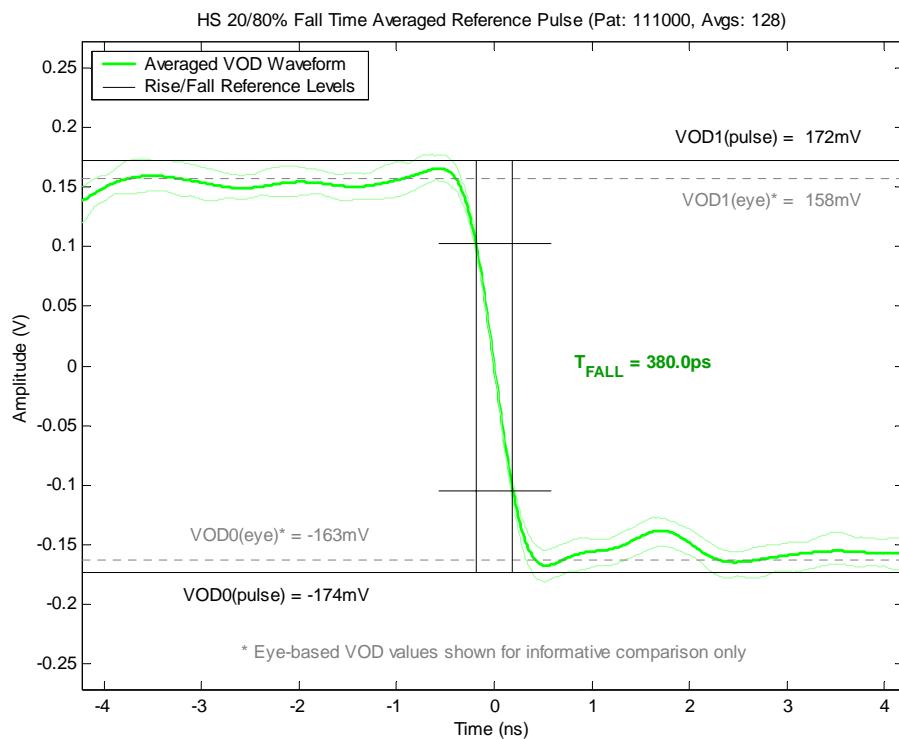
**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $t_F$ , which is a device's High-Speed TX 80%-20% Fall Time.

The D-PHY Specification states, “*The rise and fall times,  $t_R$  and  $t_F$ , are defined as the transition time between 20% and 80% of the full HS signal swing. The driver shall meet the  $t_R$  and  $t_F$  specifications for all allowable  $Z_{ID}$ .*” [1].

Note the methodology for this test is identical to the previous test (see Test 1.3.11), except that the 80%-20% Fall Time ( $t_F$ ) is measured on a 111000 reference pattern. The same averaging approach is used, and the measurement is performed for all three  $Z_{ID}$  cases. A sample measurement is shown in the figure below.



**Figure 1.3.12-1: Sample HS Fall Time Reference Waveform and Measurement**

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In all cases, the value of  $t_F$  must be greater than 150ps and less than 0.3 UI (where UI is the nominal HS Unit Interval for the DUT, see Test 1.4.17) in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that Data Lane 0 is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source an HS burst sequence on Data Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods, measure  $t_F$  as described above.
- Repeat the previous steps two additional times, once with Data Lane 0 connected to the  $Z_{ID} = 125$  ohms Lane of the RTB, and again with Data Lane 0 connected to  $Z_{ID} = 80$  ohms.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For all three  $Z_{ID}$  cases, and for all Data Lanes:

- Verify that  $t_F$  is greater than 150ps and less than 0.3UI.

**Possible Problems:**

See Possible Problems comments for Test 1.3.4. The same applies to this test.

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### Test 1.3.13 – Data Lane HS Exit: $T_{HS-TRAIL}$ Value

**Purpose:** To verify that the duration the DUT Data Lane TX drives the inverted final differential state following the last payload data bit of a HS-TX burst ( $T_{HS-TRAIL}$ ), is greater than the minimum required value.

#### References:

- [1] D-PHY Specification, Section 5.14.2, Line 1044
- [2] Ibid, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

#### Discussion:

As part of the process of completing a HS Data Transmission Burst, the D-PHY Specification provides a requirement for the length of time that a device must drive the final extended HS differential state following the last payload data bit of a HS transmission burst. This interval is defined as  $T_{HS-TRAIL}$ , and is shown in the figure below.

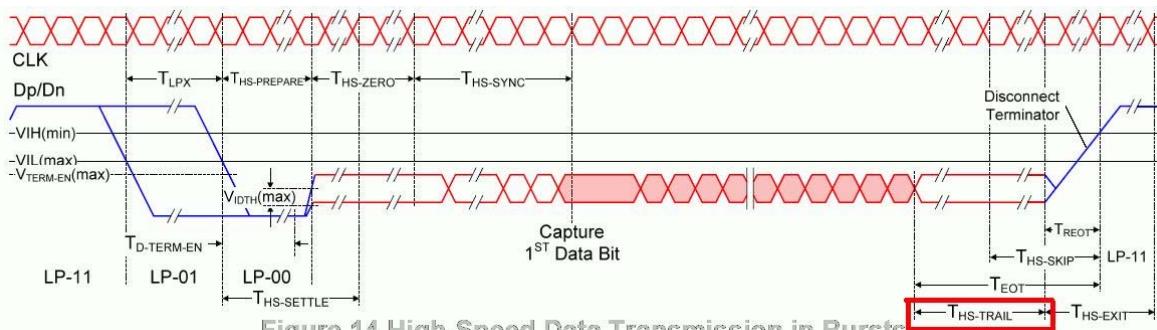


Figure 1.3.13-1:  $T_{HS-TRAIL}$  Interval

The specification states, “ $T_{HS-TRAIL}$  is the time the transmitter must drive the flipped last data bit after sending the last payload data bit of a HS transmission burst. This time is required by the receiver to determine EoT.”[1]. Also, Table 14 of the specification describes  $T_{HS-TRAIL}$  as the, “Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst.”[2]

After transmitting final the payload data bit of a HS Data Transmission Burst, the final extended HS differential state shall be held for a minimum duration of  $(n * 8 * UI)$  or  $(60 \text{ ns} + n * 4 * UI)$ , whichever is greater (where  $n = 1$  for Forward-direction HS mode, and  $n = 4$  for Reverse-direction HS mode.) However it should be noted that no currently MIPI-specified applications of D-PHY utilize the Reverse-direction HS mode, therefore it will not be tested in this test.

Also, for  $n = 1$ , the quantity  $(8 * UI)$  can only be greater than  $(60 \text{ ns} + 4 * UI)$  if UI is greater than 15ns. This corresponds to an HS bit rate of  $(1/15\text{ns}) = 66.667 \text{ Mbps}$  or less. However, because the minimum allowed HS bit rate for D-PHY is defined to be 80 Mbps, this will never occur. Therefore, for the Forward direction, the lower conformance limit for  $T_{HS-TRAIL}$  will always be  $(60 \text{ ns} + 4 * UI)$ .

In this test, an HS-TX Data Lane signaling burst from the DUT transmitter will be captured using a real-time DSO. The measurement will be performed using the  $Z_{ID} = 100 \text{ ohms}$  termination case only. The differential waveform will be computed as difference of the positive and negative single-ended waveforms ( $V_{DP} - V_{DN}$ ). The  $T_{HS-TRAIL}$  interval will be measured for the final extended HS differential state, at the points where the differential waveform enters and exits the minimum valid HS-RX differential range (i.e., when the differential waveform

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crosses +70 or -70mV). The measured  $T_{HS-TRAIL}$  result should be greater than (60 ns + 4\*UI) to be considered conformant [2].

Also, a second observable result is defined for this test, which verifies that the  $T_{HS-TRAIL}$  state is actually inverted from the last bit of the HS burst. (Note this will be performed by comparing the  $T_{HS-TRAIL}$  state to the last bit of the last byte of HS burst data.) The  $T_{HS-TRAIL}$  state should be the inversion of the last bit of the last byte of HS burst data in order to be considered conformant.

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board (RTB).
- Create a condition that causes the DUT to source an HS burst sequence on Data Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods as described above, measure  $T_{HS-TRAIL}$ .
- Using post-processing methods as described above, measure the HS state during  $T_{HS-TRAIL}$  (HS-0, or HS-1), and also determine the value of the last bit of the last byte of HS burst data.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For  $Z_{ID} = 100\text{ohms}$ , and for all Data Lanes:

- Verify that  $T_{HS-TRAIL}$  is greater than (60 ns + 4\*UI).
- Verify that the  $T_{HS-TRAIL}$  state is inverted from the last bit of the last byte of HS burst data.

**Possible Problems:**

See Possible Problems comments for Test 1.3.1. The same applies to this test.

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**Test 1.3.14 – Data Lane HS Exit: 30%-85% Post-EoT Rise Time ( $T_{REOT}$ )**

**Purpose:** To verify that the 30%-85% Post-EoT Rise Time ( $T_{REOT}$ ) of the DUT LP Data Lane transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.2, Line 1431
- [2] Ibid, Section 8.1.2, Table 19

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $T_{REOT}$ , which is a device's LP-TX 30%-85% Rise Time, following an EoT exit from a High-Speed Data Transmission Burst.

The D-PHY Specification states, “*The rise-time of  $T_{REOT}$  starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.*” [1].

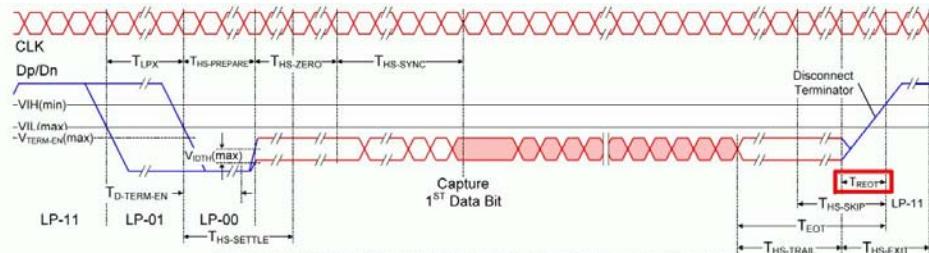


Figure 14 High-Speed Data Transmission in Bursts

Figure 1.3.14-1:  $T_{REOT}$  Rise Time

In this test, an HS-TX Data Lane signaling burst from the DUT transmitter will be captured using a real-time DSO. The measurement will be performed using the  $Z_{ID} = 100$  ohms termination case only. The differential waveform will be computed as difference of the positive and negative single-ended waveforms ( $V_{DP}-V_{DN}$ ). The  $T_{REOT}$  Rise Time will be measured starting at the time where the differential waveform last crosses  $\pm 70$ mV, and ends where  $V_{DP}$  crosses  $V_{IH,\text{MIN}} = 880$ mV. (Note the spec does not differentiate whether  $V_{DP}$  or  $V_{DN}$  should be used, as they are identical from the specification's perspective. However, for real devices the rise times may not be the same.)

The value of  $T_{REOT}$  must be less than 35ns in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board (RTB).
- Create a condition that causes the DUT to source an HS burst sequence on Data Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods as described above, measure  $T_{REOT}$ .
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For  $Z_{ID} = 100$ ohms, and for all Data Lanes:

- Verify that  $T_{REOT}$  is less than 35ns.

**Possible Problems:** See Possible Problems comments for Test 1.3.1. The same applies to this test.

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**Test 1.3.15 – Data Lane HS Exit:  $T_{EOT}$  Value**

**Purpose:** To verify that the combined duration of the  $T_{HS-TRAIL}$  plus  $T_{REOT}$  intervals (a.k.a.  $T_{EOT}$ ) of the DUT Data Lane transmitter is less than the maximum allowed value.

**References:**

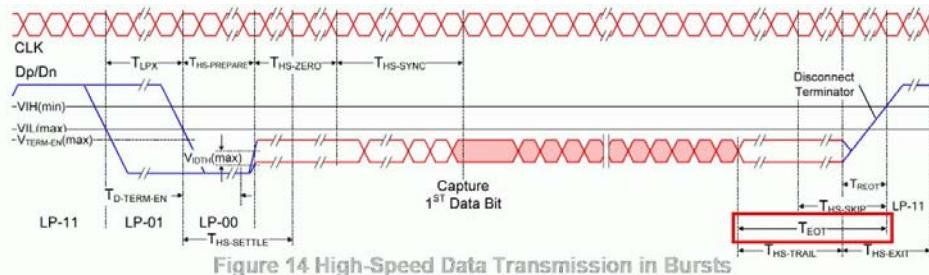
- [1] D-PHY Specification, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

In addition to the specifications and requirements defined separately for the  $T_{HS-TRAIL}$  and  $T_{REOT}$  intervals, there is an additional related parameter defined by the specification, which is effectively the sum of these two values. This interval is defined as  $T_{EOT}$ , and is shown in the figure below.



**Figure 1.3.15-1:  $T_{EOT}$  Interval**

As seen above,  $T_{EOT}$  is measured from the beginning of  $T_{HS-TRAIL}$ , to the start of the LP-11 state following  $T_{REOT}$ . Note that because the start of the LP-11 state is also the same time point that marks the end of  $T_{REOT}$ , the  $T_{EOT}$  interval can also be viewed as the sum of the  $T_{HS-TRAIL}$  and  $T_{REOT}$  intervals.

While the requirement for  $T_{HS-TRAIL}$  only specifies a lower bound, and the requirement for  $T_{REOT}$  only provides an upper bound, the purpose of  $T_{EOT}$  is to provide an upper limit on the combination of these two intervals. (Otherwise, devices would hypothetically be allowed to extend  $T_{HS-TRAIL}$  indefinitely.)

In this test, the previously measured values obtained for  $T_{HS-TRAIL}$  and  $T_{REOT}$  (see previous tests) will be added to create  $T_{EOT}$ . The measured  $T_{EOT}$  result must be less than  $(105 \text{ ns} + n*12*\text{UI})$  in order to be considered conformant [1] (where  $n = 1$  for Forward-direction HS mode and  $n = 4$  for Reverse-direction HS mode, and UI is the nominal HS Unit Interval for the DUT, see Test 1.4.17.) (Note that for the purposes of this test,  $n$  will always be equal to 1, as no currently defined MIPI device types or protocols use the Reverse-direction HS functionality of D-PHY.)

**Test Setup:** None.

**Test Procedure:**

- Obtain the Data Lane 0 numerical values for  $T_{HS-TRAIL}$  and  $T_{REOT}$ , obtained in previous Tests 1.3.13, and 1.3.14, respectively.
- Add the two values together to produce  $T_{EOT}$ .
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For all Data Lanes:

- Verify that  $T_{EOT}$  is less than  $(105 \text{ ns} + 12*\text{UI})$ .

**Possible Problems:** None.

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**Test 1.3.16 – Data Lane HS Exit:  $T_{HS-EXIT}$  Value**

**Purpose:** To verify that the duration that the Data Lane transmitter remains in the LP-11 (Stop) state after exiting HS mode ( $T_{HS-EXIT}$ ), is greater than the minimum required value.

**References:**

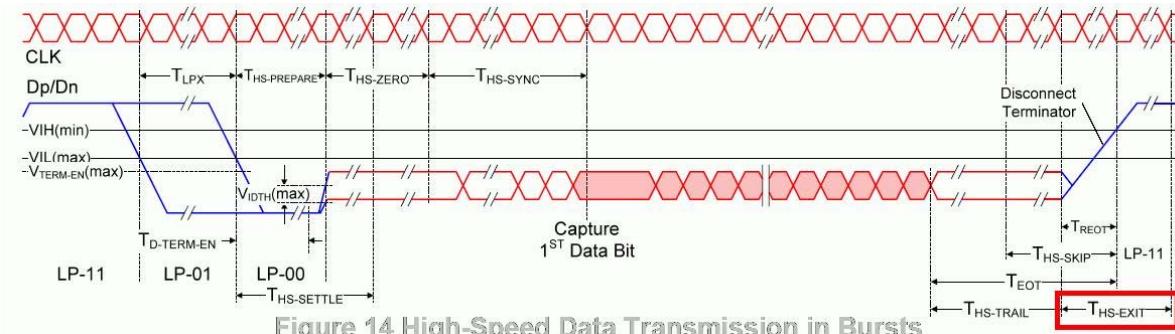
- [1] D-PHY Specification, Section 5.9, Table 14
- [2] Ibid, Section 5.4.4, Figure 14
- [3] Ibid, Section 5.7, Figure 21

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

As part of the process for switching any D-PHY Lane (Clock or Data) out of HS mode, the D-PHY Specification provides a requirement for the minimum time that the Lane must remain in the LP-11 Stop state before initiating any further sequences. This interval is defined as  $T_{HS-EXIT}$ , and is shown in the figure below. (Note that the example figure below shows a Data Lane example, and a figure showing a Clock Lane example can be found in Figure 1.4.16-1 in Test 1.4.16. The  $T_{HS-EXIT}$  specification and conformance limits are identical for Clock and Data Lanes, however they are performed as separate tests in this test suite.)



**Figure 14 High-Speed Data Transmission in Bursts**

**Figure 1.3.16-1:  $T_{HS-EXIT}$  Interval (Data Lane Example Shown)**

In this test, the DUT will be configured to send repeated HS burst sequences, and the Data Lane  $T_{HS-EXIT}$  values will be observed. The values will be observed over multiple HS bursts in order to determine the minimum value. If the DUT sources image data (which is transmitted in many cases using one HS burst per horizontal pixel line, though this is not explicitly true for all D-PHY applications), it is recommended that  $T_{HS-EXIT}$  be observed over a minimum of one entire frame cycle (i.e., all bursts from the start of a 2-D image (frame) to the end of the 2-D image (frame), including all data and control packets).

While the primary description of  $T_{HS-EXIT}$  in the specification states it as the, “*Time that the transmitter drives LP-11 following a HS burst.*” [1], this wording does not explicitly indicate the exact start and end points of the parameter for the purpose of measurement. However, Figure 14 of the specification graphically shows the  $T_{HS-EXIT}$  interval as starting at the end of the  $T_{HS-TRAIL}$  interval (which is defined by the point where the differential waveform crosses below the minimum valid HS-RX differential threshold level of +/-70mV, see Test 1.3.13.)

Also, Figure 21 of the specification shows a Clock Lane example of  $T_{HS-EXIT}$ , which graphically shows the end point as being where the  $V_{DP}$  LP-01 falling edge crosses  $V_{IL,MAX}$  (550mV) during the HS entry sequence of the next successive HS burst. (Note that while the example shows the next successive sequence being another HS burst, it is assumed that the  $T_{HS-EXIT}$  requirement equally applies for any type of sequence that could follow an HS burst (e.g., Escape Mode, Bus Turnaround, etc), however this test will primarily verify the HS burst case. In lieu of any explicit textual definitions for the start and end points for  $T_{HS-EXIT}$ , the measurement start/end points for conformance test purposes must be inferred from the example figures.

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In this test, the  $T_{HS-EXIT}$  interval for a given Lane will be observed, measured starting from the end of the  $T_{HS-TRAIL}$  interval (at the point where the differential waveform crosses below the minimum valid HS-RX differential threshold level of +/-70mV), to the point where the  $V_{DP}$  LP-01 falling edge crosses  $V_{IL,MAX}$  (550mV) during the next successive HS burst. (Alternately, if a burst is followed by some sequence other than another HS burst, the 550mV crossing time of the first LP falling edge (Dp or Dn) of that sequence shall be used as the  $T_{HS-EXIT}$  ending point.)

The measurement will be performed using the  $Z_{ID} = 100$  ohms termination case only, and will be measured for all Data Lanes.

The duration of  $T_{HS-EXIT}$  shall be no less than 100ns for all observed bursts in order to be considered conformant [1].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board (RTB).
- Create a condition that causes the DUT to source repeated HS burst sequences on Data Lane 0.
- Capture the HS burst sequences using the DSO.
- Using post-processing methods, measure  $T_{HS-EXIT}$  as described above.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For  $Z_{ID} = 100$ ohms, and for all Data Lanes:

- Verify that  $T_{HS-EXIT}$  is no less than 100ns for all observed bursts.

**Possible Problems:**

See Possible Problems comments for Test 1.3.1. The same applies to this test.

Also, for DUTs that transmit extremely long bursts (which may occur in the case of some DSI transmitters, which are allowed to combine multiple successive data packets (up to and even including an entire 2-D image) into a single transmitted HS burst), it may not be possible to capture multiple successive bursts in a single DSO capture (depending on the overall burst length, and the memory depth of the DSO). Also, cases may exist where a DUT could potentially transmit extremely long LP periods between bursts, such that an entire  $T_{HS-EXIT}$  period may not be able to fit within the capture depth of the DSO.

In both of these cases, a modified procedure may be used whereby the DSO is configured to observe only the ends of the HS bursts (typically by triggering on the LP  $T_{REOT}$  rising edge at the end of the burst), and the window immediately following the burst may be observed (using a persistence trace/mode of the DSO) to verify that no subsequent bursts begin within a minimum  $T_{HS-EXIT}$  period of 100ns. Provided it can be shown that no bursts violate the minimum 100ns conformance limit, the exact value of  $T_{HS-EXIT}$  does not need to be explicitly measured for every burst in order to demonstrate conformance.

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## **GROUP 4: CLOCK LANE HS-TX SIGNALING REQUIREMENTS**

### **Overview:**

This group of tests verifies various requirements specific to the HS-TX Clock Lane signaling. The intent of this structuring is to facilitate performing a set of TX measurements on a single captured HS-TX Clock Lane signaling sequence, including the LP exit/entry sequences occurring before/after the HS Burst sequence, if the DUT supports burst-mode (i.e., non-continuous) clock behavior on the Clock Lane. Note that for devices that do not support burst-mode clocking (i.e., devices that only support continuous clock behavior), the LP-specific tests in this group may need to be performed separately on the leading/trailing HS entry/exit sequences that occur when the continuous clock mode is enabled/disabled.

This test Group is applicable to Master devices only. (It is considered Not Applicable for Slave devices.)

### **Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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**Test 1.4.1 – Clock Lane HS Entry:  $T_{LPX}$  Value**

**Purpose:** To verify that the duration ( $T_{LPX}$ ) of the final Clock Lane LP-01 state immediately before HS transmission is greater than the minimum conformant value.

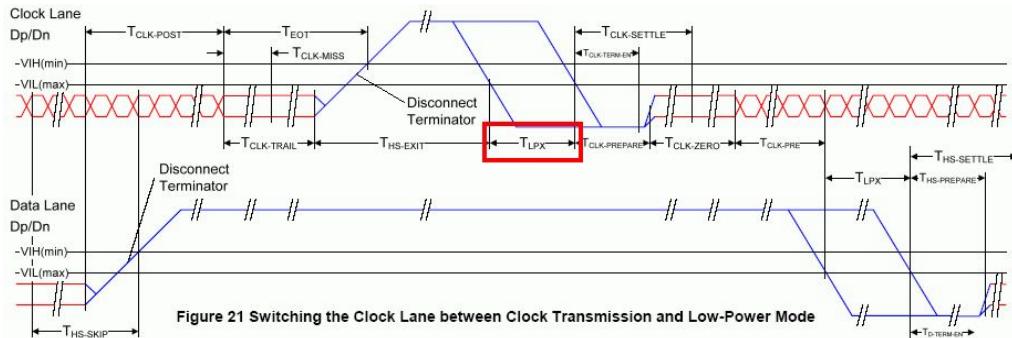
**References:** (See Discussion.)

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

Note that this test is identical in terms of spec requirements and references to the Data Lane  $T_{LPX}$  test of Test 1.3.1, except that it is performed on the Clock Lane  $T_{LPX}$  interval, shown below.



**Figure 1.4.1-1: Clock Lane  $T_{LPX}$  Interval**

The Clock Lane  $T_{LPX}$  value is measured using the same methodology as the Data Lane  $T_{LPX}$  value (see Test 1.3.1), and the same conformance requirements apply (i.e.,  $T_{LPX}$  must be at least 50ns in order to be considered conformant.)

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board (RTB). (Clock Lane,  $Z_{ID} = 100$  ohms.)
- Create a condition that causes the DUT to source an HS entry sequence on the Clock Lane.
- Capture the HS entry sequence using the DSO.
- Using post-processing methods, compute the  $V_{DP}$  and  $V_{DN}$   $V_{IL,MAX}$  (550mV) crossing times.
- Measure the  $T_{LPX}$  value as the difference between the two crossing times.

**Observable Results:**

- Verify that  $T_{LPX}$  is at least 50ns.

**Possible Problems:**

This test is typically performed with the DUT configured for non-continuous clock behavior (i.e., burst-mode clocking) on the Clock Lane. Note that non-continuous clock behavior is considered optional for some DUT types (e.g., CSI-2 devices), however it is frequently supported by these and other DUTs, and is considered the preferred mode for this test suite, as it allows nearly all HS Clock and Data Lane tests to be obtained from a single set of Clock and Data Lane burst-mode waveform data.

If a DUT only supports continuous clock behavior, this test, and the other entry/exit timer tests in this Group must be performed on the HS Entry and HS Exit sequences that occur when continuous clocking operation is manually enabled and disabled from the LP-00 state (which devices implementing continuous clock behavior are required to support).

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### Test 1.4.2 – Clock Lane HS Entry: $T_{CLK-PREPARE}$ Value

**Purpose:** To verify that the time that the DUT Clock Lane transmitter drives LP-00 ( $T_{CLK-PREPARE}$ ) prior to driving  $T_{CLK-ZERO}$  when entering HS mode, is within the conformance limits.

#### References:

[1] D-PHY Specification, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

#### Discussion:

As part of the process for switching the Clock Lane into HS mode, the D-PHY Specification provides a specification for the duration that the Master must transmit the final Clock Lane LP-00 state before enabling HS transmission (which occurs at the start of the  $T_{CLK-ZERO}$  interval). This interval is defined as  $T_{CLK-PREPARE}$ , and is shown in the figure below.

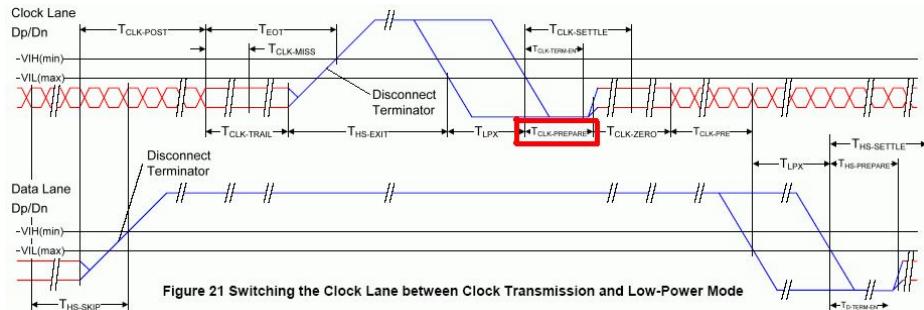


Figure 1.4.2-1:  $T_{CLK-PREPARE}$  Interval

(Note that the methodology for this test is essentially identical to the Data Lane  $T_{HS-PREPARE}$  test of 1.3.2, except the measurement is performed on the Clock Lane, and different conformance limits are applied.)

In this test, the DUT will be configured to source a Clock Lane HS entry sequence, which will be captured using a real-time DSO. The  $T_{HS-PREPARE}$  interval will be measured from the point where the Clock Lane  $V_{DN}$  signal crosses below  $V_{IL,MAX}$  (550mV), to the beginning of the  $T_{CLK-ZERO}$  HS differential state, which starts at the point where the differential waveform crosses the minimum valid HS-RX differential threshold level of +/-70mV.

The value of  $T_{CLK-PREPARE}$  must be between 38 and 95 ns in order to be considered conformant [1].

**Test Setup:** See Appendix B.1.2.

#### Test Procedure:

- Connect the DUT to the Reference Termination Board (RTB). (Clock Lane,  $Z_{ID} = 100$  ohms.)
- Create a condition that causes the DUT to source a Clock Lane HS entry sequence.
- Capture the HS entry sequence using the DSO.
- Using post-processing methods, measure  $T_{CLK-PREPARE}$  as described above.

#### Observable Results:

- Verify that  $T_{CLK-PREPARE}$  is between 38 and 95 ns.

**Possible Problems:** See Possible Problems comments for Test 1.4.1. The same applies to this test.

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### Test 1.4.3 – Clock Lane HS Entry: $T_{CLK-PREPARE}+T_{CLK-ZERO}$ Value

**Purpose:** To verify that the combined time of  $T_{CLK-PREPARE}$  plus the time that the DUT Clock Lane transmitter drives the extended HS-0 differential state prior to starting clock transmission ( $T_{CLK-ZERO}$ ) is greater than the minimum required duration.

#### References:

[1] D-PHY Specification, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

#### Discussion:

As part of the process for switching the Clock Lane into HS mode, the D-PHY Specification provides a specification for the minimum duration that the Master must drive the extended HS-0 differential state ( $T_{CLK-ZERO}$ ) prior to starting clock transmission. This interval is defined as  $T_{CLK-ZERO}$ , and is shown in the figure below.

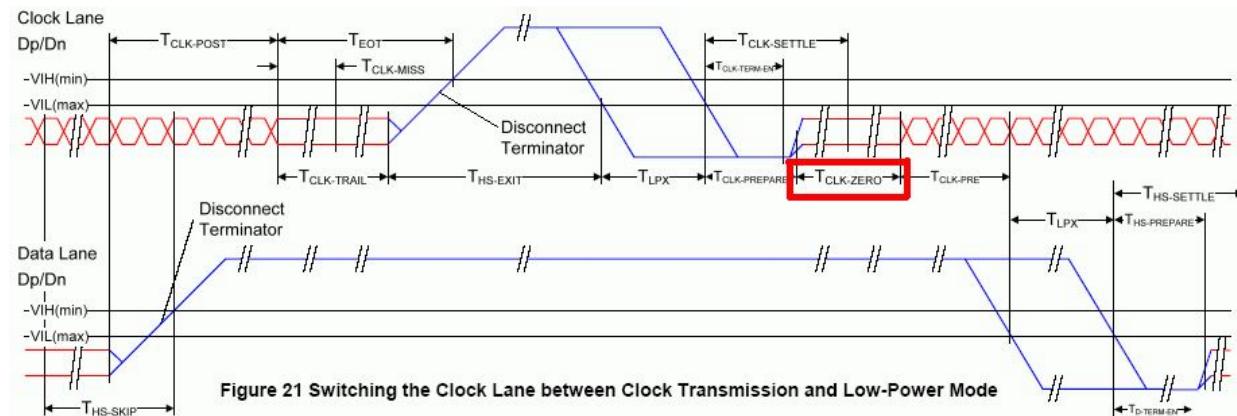


Figure 1.4.3-1:  $T_{CLK-ZERO}$  Interval

(Note that the methodology for this test is essentially identical to the Data Lane  $T_{HS-PREPARE}+T_{HS-ZERO}$  test of 1.3.3, except the measurement is performed on the Clock Lane, and different conformance limits are applied.)

In this test, the DUT will be configured to source a Clock Lane HS entry sequence, which will be captured using a real-time DSO. The ( $T_{CLK-PREPARE} + T_{CLK-ZERO}$ ) interval will be measured from the point where the Clock Lane  $V_{DN}$  signal crosses below  $V_{IL,MAX}$  (550mV), to the end of the  $T_{CLK-ZERO}$  HS differential state, at the point where the differential waveform crosses the minimum valid HS-RX differential threshold level of +/-70mV. The measured duration of ( $T_{CLK-PREPARE} + T_{CLK-ZERO}$ ) must be greater than 300ns in order to be considered conformant[1].

**Test Setup:** See Appendix B.1.2.

#### Test Procedure:

- Connect the DUT to the Reference Termination Board (RTB). (Clock Lane,  $Z_{ID} = 100$  ohms.)
- Create a condition that causes the DUT to source a Clock Lane HS entry sequence.
- Capture the HS entry sequence using the DSO.
- Using post-processing methods, measure ( $T_{CLK-PREPARE} + T_{CLK-ZERO}$ ) as described above.

#### Observable Results:

- Verify that ( $T_{CLK-PREPARE} + T_{CLK-ZERO}$ ) is at least 300ns.

**Possible Problems:** See Possible Problems comments for Test 1.4.1. The same applies to this test.

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**Test 1.4.4 – Clock Lane HS-TX Differential Voltages ( $V_{OD(0)}$ ,  $V_{OD(1)}$ )**

**Purpose:** To verify that the Differential Voltages ( $V_{OD(0)}$  and  $V_{OD(1)}$ ) of the DUT Clock Lane HS transmitter are within the conformance limits.

**References:**

[1] D-PHY Specification, Section 8.1.1, Table 16

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{OD(0)}$  and  $V_{OD(1)}$ , which are a device's HS-TX Differential Voltage levels for the HS-0 and HS-1 states, respectively.

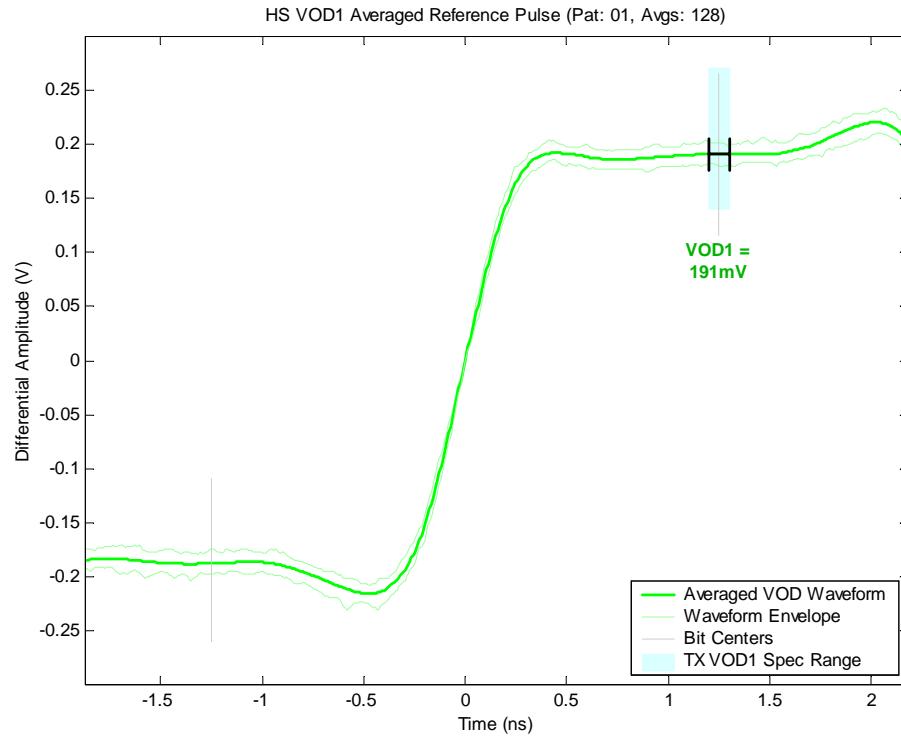
*(Note that the methodology for this test is similar in nature to the Data Lane  $V_{OD}$  test of 1.3.4, with some modifications. The same parameter is measured, with the same conformance range. A similar methodology is used to create an averaged waveform on which the measurements are performed, however a different reference data pattern is used. Because the Clock Lane only contains 1010 data, the reference patterns for measuring the Clock Lane  $V_{OD(1)}$  and  $V_{OD(0)}$  levels are 01 and 10, respectively. Also, rather than averaging the samples between the centers of the 4<sup>th</sup> and 5<sup>th</sup> bits of the reference pattern as was done with the Data Lane reference pattern, the Clock Lane case will simply measure the voltage at the center of the 2<sup>nd</sup> bit of the reference pattern to determine the  $V_{OD(1)}$  and  $V_{OD(0)}$  levels.)*

In this test, a sample of the DUTs Clock Lane HS signaling will be captured using a real-time DSO. The differential waveform will be computed as difference of the positive and negative single-ended waveforms ( $V_{DP}$ - $V_{DN}$ ). An averaged waveform will be constructed from the differential waveform data for the 01 reference pattern. The averaged waveform shall be constructed by horizontally aligning a minimum of 128 individual waveforms to a common reference point, which will be the zero crossing time of the first transition. The result should produce an averaged waveform similar to Figure 1.4.4-1, below.

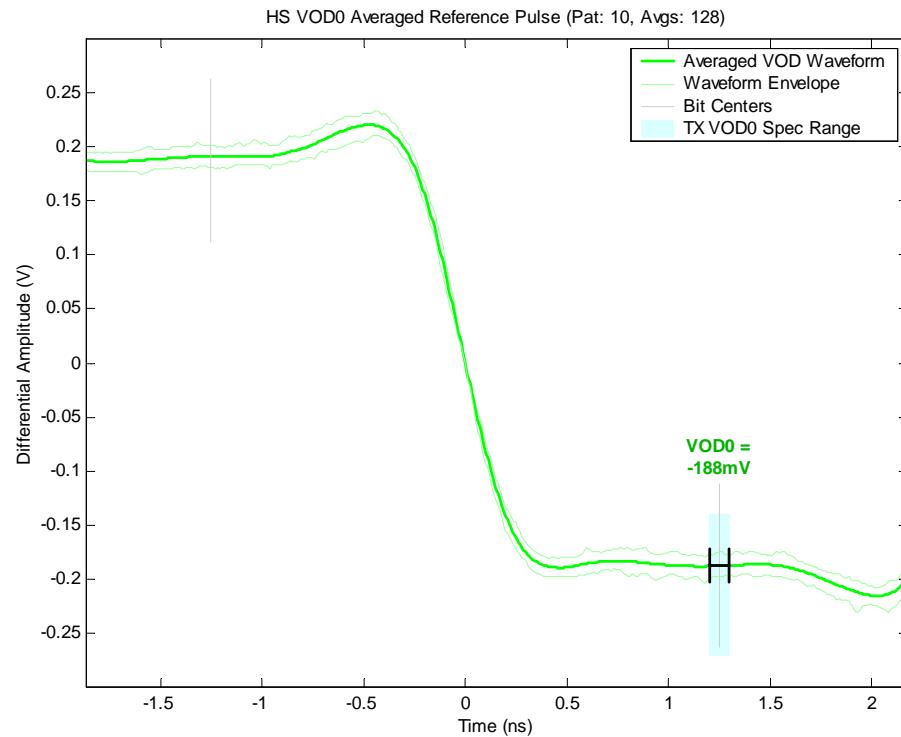
Once the averaged waveform is obtained, the  $V_{OD(1)}$  value will be measured as the voltage at the exact center of the UI corresponding to the '1' bit, also as shown in Figure 1.4.4-1 below.

To determine the  $V_{OD(0)}$  level, the measurement will be repeated using a 10 data pattern, and the amplitude measured at the center of the '0' bit (see Figure 1.4.4-2 below).

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**Figure 1.4.4-1: Sample Clock Lane Averaged  $V_{OD(1)}$  Reference Pulse and Measurement**



**Figure 1.4.4-2: Sample Clock Lane Averaged  $V_{OD(0)}$  Reference Pulse and Measurement**

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Also, both the  $V_{OD(1)}$  and  $V_{OD(0)}$  measurements will be performed for three  $Z_{ID}$  cases: nominal (100 ohms), maximum (125 ohms), and minimum (80 ohms).

In all cases, the averaged  $V_{OD(1)}$  value must be between 140 to 270mV in order to be considered conformant, and the averaged  $V_{OD(0)}$  value must be between -140 to -270mV in order to be considered conformant [1].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that the Clock Lane is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source HS clock signaling on the Clock Lane (either burst or continuous).
- Capture the clock signaling using the DSO.
- Using post-processing methods, measure  $V_{OD(1)}$  and  $V_{OD(0)}$  as described above.
- Repeat the previous steps two additional times, once with the Clock Lane connected to the  $Z_{ID} = 125$  ohms Lane of the RTB, and again with the Clock Lane connected to  $Z_{ID} = 80$  ohms.

**Observable Results:**

For all three  $Z_{ID}$  cases:

- Verify that  $V_{OD(1)}$  is between 140 and 270mV.
- Verify that  $V_{OD(0)}$  is between -140 and -270mV.

**Possible Problems:**

See Possible Problems comments for Test 1.3.4. The same applies to this test.

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**Test 1.4.5 – Clock Lane HS-TX Differential Voltage Mismatch ( $\Delta V_{OD}$ )**

**Purpose:** To verify that the Differential Voltage Mismatch ( $\Delta V_{OD}$ ) of the DUT Clock Lane HS transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1345
- [2] Ibid, Section 8.1.1, Table 16

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $\Delta V_{OD}$ , which is a device's HS-TX Differential Voltage Mismatch.

The D-PHY Specification states, “*The output differential voltage mismatch  $\Delta V_{OD}$  is defined as the difference of the absolute values of the differential output voltage in the Differential-1 state  $V_{OD(1)}$  and the differential output voltage in the Differential-0 state  $V_{OD(0)}$ . This is expressed by  $\Delta V_{OD} = |V_{OD(1)}| - |V_{OD(0)}|$* ” [1].

(Note that the methodology for this test is identical to the Data Lane  $\Delta V_{OD}$  test of 1.3.5, except the measurement is performed using the Clock Lane  $V_{OD}$  results. The conformance limits are the same as the Data Lane case.)

In this test, the numerical  $V_{OD(0)}$  and  $V_{OD(1)}$  results obtained in the previous test (see Test 1.4.4) will be used to compute the Clock Lane  $\Delta V_{OD}$  results. The difference of the absolute values of  $V_{OD(0)}$  and  $V_{OD(1)}$  will be taken to produce  $\Delta V_{OD}$ . The measurement will be performed for all three  $Z_{ID}$  test cases.

In all cases, the absolute value of  $\Delta V_{OD}$  must be less than 10mV in order to be considered conformant [2].

**Test Setup:** None.

**Test Procedure:**

- Obtain the numerical Clock Lane  $V_{OD(0)}$  and  $V_{OD(1)}$  results from Test 1.4.4, for all three  $Z_{ID}$  test cases.
- For each  $Z_{ID}$  test case, compute the Clock Lane  $\Delta V_{OD}$  result as described above.

**Observable Results:**

For all three  $Z_{ID}$  cases:

- Verify that the absolute value of  $\Delta V_{OD}$  is less than 10mV.

**Possible Problems:**

See Possible Problems comments for Test 1.3.4. The same applies to this test.

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**Test 1.4.6 – Clock Lane HS-TX Single-Ended Output High Voltages ( $V_{OHHS(DP)}$ ,  $V_{OHHS(DN)}$ )**

**Purpose:** To verify that the Single-Ended Output High Voltages ( $V_{OHHS(DP)}$  and  $V_{OHHS(DN)}$ ) of the DUT Clock Lane HS transmitter are less than the maximum conformance limit.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1336
- [2] Ibid, Section 8.1.1, Table 16

**Resource Requirements:** See Appendix A.1.

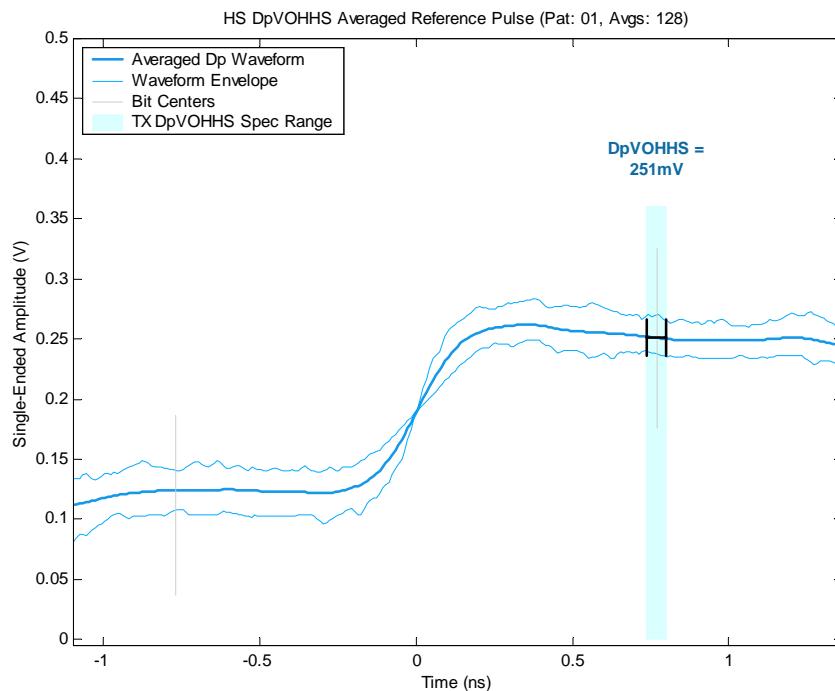
**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{OHHS}$ , which is a device's HS-TX Output High Voltage.

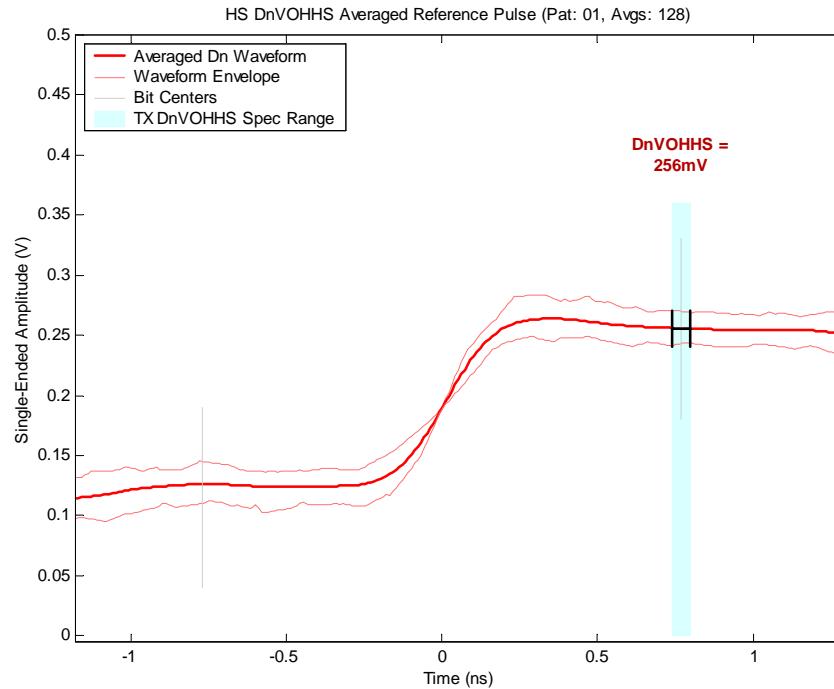
The D-PHY Specification states, “*The output voltages  $V_{DP}$  and  $V_{DN}$  at the  $D_p$  and  $D_n$  pins shall not exceed the High-Speed output high voltage  $V_{OHHS}$ .  $V_{OLHS}$  is the High-Speed output, low voltage on  $D_p$  and  $D_n$  and is determined by  $V_{OD}$  and  $V_{CMTX}$ . The High-Speed  $V_{OUT}$  is bounded by the minimum value of  $V_{OLHS}$  and the maximum value of  $V_{OHHS}$ .*” [1].

(Note that the methodology for this test is similar to the Data Lane  $V_{OHHS(DP/DN)}$  test of 1.3.6, except the measurement is performed on the Clock Lane  $V_{DP}$  and  $V_{DN}$  signals, and a 01 reference pattern is used instead of a 01111 pattern (which does not exist on the Clock Lane). Also, the  $V_{OHHS}$  values are measured as the voltage level at the center of the ‘1’ bit (similar to the Clock Lane  $V_{OD(I)}$  measurement, see Test 1.4.4). The Clock Lane  $V_{OHHS}$  conformance limits are the same as the Data Lane case.) Example measurements for  $V_{OHHS(DP)}$  and  $V_{OHHS(DN)}$  are shown in Figures 1.4.6-1 and 1.4.6-2, below.



**Figure 1.4.6-1: Sample Clock Lane Averaged  $V_{OHHS(DP)}$  Reference Pulse and Measurement**

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**Figure 1.4.6-2: Sample Clock Lane Averaged  $V_{OHHS(DN)}$  Reference Pulse and Measurement**

This measurement will be performed for all three  $Z_{ID}$  cases.

In all cases, the  $V_{OHHS}$  results for both  $V_{DP}$  and  $V_{DN}$  shall be less than 360mV in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that the Clock Lane is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source HS clock signaling on the Clock Lane (either burst or continuous).
- Capture the clock signaling using the DSO.
- Using post-processing methods, measure  $V_{OHHS(DP)}$  and  $V_{OHHS(DN)}$  as described above.
- Repeat the previous steps two additional times, once with the Clock Lane connected to the  $Z_{ID} = 125$  ohms Lane of the RTB, and again with the Clock Lane connected to  $Z_{ID} = 80$  ohms.

**Observable Results:**

For all three  $Z_{ID}$  cases:

- Verify that  $V_{OHHS(DP)}$  is less than 360mV.
- Verify that  $V_{OHHS(DN)}$  is less than 360mV.

**Possible Problems:**

See Possible Problems comments for Test 1.3.4. The same applies to this test.

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**Test 1.4.7 – Clock Lane HS-TX Static Common-Mode Voltages ( $V_{CMTX(1)}$ ,  $V_{CMTX(0)}$ )**

**Purpose:** To verify that the Static Common-Mode Voltages ( $V_{CMTX(1)}$ , and  $V_{CMTX(0)}$ ) of the DUT Clock Lane HS transmitter are within the conformance limits.

**References:**

[1] D-PHY Specification, Section 8.1.1, Table 16

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{CMTX}$ , which is a device's HS-TX Static Common-Mode Voltage.

*(Note that the methodology for this test is identical to the Data Lane  $V_{CMTX}$  test of 1.3.7, except the measurement is performed on the Clock Lane. The conformance limits are the same as the Data Lane case.)*

In this test, a portion of the DUTs HS Clock Lane signaling will be captured using a real-time DSO. The  $V_{DP}$  and  $V_{DN}$  single-ended waveforms will be averaged together (as described above) to create the  $V_{CMTX}$  common-mode waveform. The  $V_{CMTX}$  waveform will be sampled at the center of each UI, corresponding to each Differential-1 and Differential-0 state. The average common-mode voltage observed over a minimum of 5,000 Differential-1 UIs will be computed as  $V_{CMTX(1)}$ , and the average common-mode voltage observed over a minimum of 5,000 Differential-0 UIs will be computed as  $V_{CMTX(0)}$ .

This measurement will be performed for all three  $Z_{ID}$  cases.

For all cases, the values for both  $V_{CMTX(1)}$  and  $V_{CMTX(0)}$  must be between 150 to 250mV in order to be considered conformant [1].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that the Clock Lane is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source HS clock signaling on the Clock Lane (either burst or continuous).
- Capture the clock signaling using the DSO.
- Using post-processing methods, measure  $V_{CMTX(1)}$  and  $V_{CMTX(0)}$ , as described above.
- Repeat the previous steps two additional times, once with the Clock Lane connected to the  $Z_{ID} = 125$  ohms Lane of the RTB, and again with the Clock Lane connected to  $Z_{ID} = 80$  ohms.

**Observable Results:**

For all three  $Z_{ID}$  cases:

- Verify that  $V_{CMTX(1)}$  is between 150 and 250mV.
- Verify that  $V_{CMTX(0)}$  is between 150 and 250mV.

**Possible Problems:** None.

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**Test 1.4.8 – Clock Lane HS-TX Static Common-Mode Voltage Mismatch ( $\Delta V_{CMTX(1,0)}$ )**

**Purpose:** To verify that the Static Common-Mode Voltage Mismatch ( $\Delta V_{CMTX(1,0)}$ ) of the DUT Clock Lane HS transmitter is less than the maximum conformance limit.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Table 16

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $\Delta V_{CMTX(1,0)}$ , which is a device's HS-TX Static Common-Mode Voltage Mismatch.

*(Note that the methodology for this test is identical to the Data Lane  $\Delta V_{CMTX(1,0)}$  test of 1.3.8, except the measurement is performed using the Clock Lane  $V_{CMTX}$  results. The conformance limits are the same as the Data Lane case.)*

In this test, the numerical results from Test 1.4.7 for  $V_{CMTX(1)}$  and  $V_{CMTX(0)}$  will be used to compute the Clock Lane HS-TX Static Common-Mode Voltage Mismatch,  $\Delta V_{CMTX(1,0)}$ . The result for  $\Delta V_{CMTX(1,0)}$  will be computed as one-half of the difference of  $V_{CMTX(1)}$  minus  $V_{CMTX(0)}$ . The measurement will be performed for all three  $Z_{ID}$  cases.

In all cases, the value for  $\Delta V_{CMTX(1,0)}$  must be less than 5mV in order to be considered conformant [1].

**Test Setup:** None.

**Test Procedure:**

- Obtain the numerical Clock Lane  $V_{CMTX(0)}$  and  $V_{CMTX(1)}$  results from Test 1.4.7, for all three  $Z_{ID}$  test cases.
- For each  $Z_{ID}$  test case, compute the Clock Lane  $\Delta V_{CMTX(1,0)}$  result as described above.

**Observable Results:**

For all three  $Z_{ID}$  cases:

- Verify that  $\Delta V_{CMTX(1,0)}$  is less than 5mV.

**Possible Problems:** None.

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**Test 1.4.9 – Clock Lane HS-TX Dynamic Common-Level Variations Between 50-450MHz ( $\Delta V_{CMTX(LF)}$ )**

**Purpose:** To verify that the AC Common-Mode Signal Level Variations between 50 and 450MHz ( $\Delta V_{CMTX(LF)}$ ) of the DUT Clock Lane HS transmitter are less than the maximum allowable limit.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Table 17

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $\Delta V_{CMTX(LF)}$ , which is a device's HS-TX Dynamic Common-Level Variations between 50 and 450MHz.

*(Note that the methodology for this test is identical to the Data Lane  $\Delta V_{CMTX(LF)}$  test of 1.3.9, except the measurement is performed on the Clock Lane. The conformance limits are the same as the Data Lane case.)*

This measurement is performed only for the  $Z_{ID} = 100$  ohms test case.

The value of  $\Delta V_{CMTX(LF)}$  must be less than 25mV<sub>PEAK</sub> in order to be considered conformant [1].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that the Clock Lane is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source HS clock signaling on the Clock Lane (either burst or continuous).
- Capture the clock signaling using the DSO.
- Using post-processing methods, measure  $\Delta V_{CMTX(LF)}$  as described above.

**Observable Results:**

For  $Z_{ID} = 100$ ohms:

- Verify that  $\Delta V_{CMTX(LF)}$  is less than 25mV<sub>PEAK</sub>.

**Possible Problems:** None.

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**Test 1.4.10 – Clock Lane HS-TX Dynamic Common-Level Variations Above 450MHz ( $\Delta V_{CMTX(HF)}$ )**

**Purpose:** To verify that the AC Common-Mode Signal Level Variations above 450MHz ( $\Delta V_{CMTX(HF)}$ ) of the DUT Clock Lane HS transmitter are less than the maximum allowable limit.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Table 17

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $\Delta V_{CMTX(HF)}$ , which is a device's HS-TX Dynamic Common-Level Variations above 450MHz.

*(Note that the methodology for this test is identical to the Data Lane  $\Delta V_{CMTX(HF)}$  test of 1.3.10, except the measurement is performed on the Clock Lane. The conformance limits are the same as the Data Lane case.)*

This measurement is performed only for the  $Z_{ID} = 100$  ohms test case.

The value of  $\Delta V_{CMTX(HF)}$  must be less than 15mV<sub>RMS</sub> in order to be considered conformant [1].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that the Clock Lane is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source HS clock signaling on the Clock Lane (either burst or continuous).
- Capture the clock signaling using the DSO.
- Using post-processing methods, measure  $\Delta V_{CMTX(HF)}$  as described above.

**Observable Results:**

For  $Z_{ID} = 100$ ohms:

- Verify that  $\Delta V_{CMTX(HF)}$  is less than 15mV<sub>RMS</sub>.

**Possible Problems:** None.

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**Test 1.4.11 – Clock Lane HS-TX 20%-80% Rise Time ( $t_R$ )**

**Purpose:** To verify that the 20%-80% Rise Time ( $t_R$ ) of the DUT Clock Lane HS transmitter is within the conformance limits.

**References:**

[1] D-PHY Specification, Section 8.1.1, Table 17

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

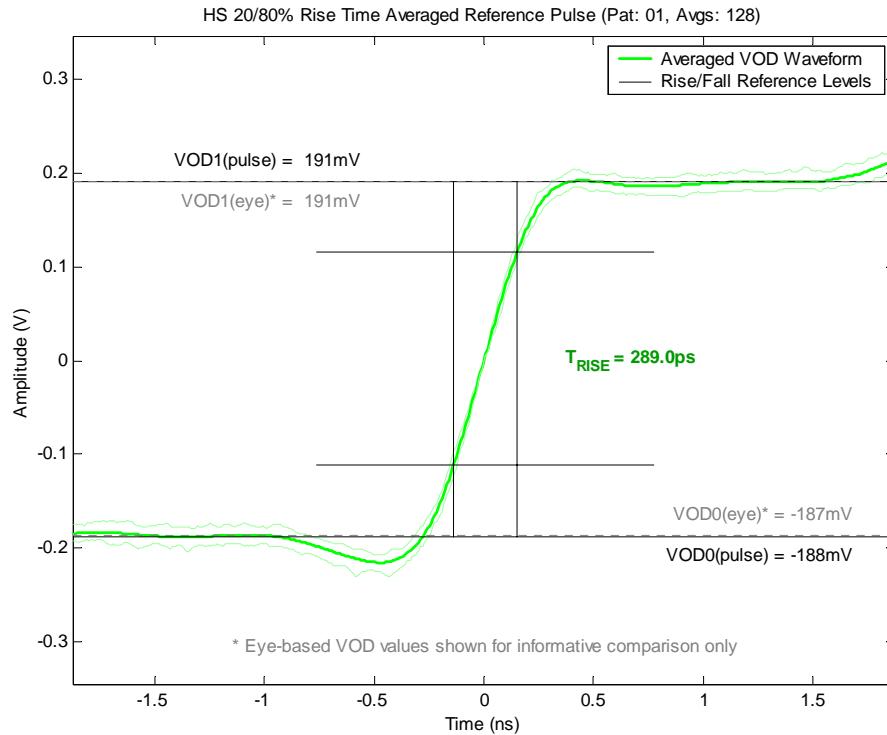
Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $t_R$ , which is a device's High-Speed TX 20%-80% Rise Time.

*(Note that the methodology for this test is similar in nature to the Data Lane rise time test of 1.3.11, with some modifications. The same parameter is measured, with the same conformance range. A similar methodology is used to create an averaged waveform on which the measurement is performed, however rather than using a 000111 reference data pattern, a 01 pattern is used (as the 000111 pattern does not exist on the Clock Lane). The reference top and base levels shall be the Clock Lane  $V_{OD(0)}$  and  $V_{OD(1)}$  values measured in Test 1.4.4.)*

In this test, a sample of the DUTs Clock Lane HS signaling will be captured using a real-time DSO. The differential waveform will be computed as difference of the positive and negative single-ended waveforms ( $V_{DP} - V_{DN}$ ). An averaged waveform will be constructed from the differential waveform data for the 01 reference pattern. The averaged waveform shall be constructed by horizontally aligning a minimum of 128 individual waveforms to a common reference point, which will be the zero crossing time of the first transition. The result should produce an averaged waveform similar to Figure 1.4.11-1, below.

The 20/80% rise time of the averaged waveform will be measured with respect to the reference Clock Lane  $V_{OD(0)}$  and  $V_{OD(1)}$  levels that were determined in Test 1.4.4. A sample averaged waveform and measurement is shown in Figure 1.4.11-1, below.

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**Figure 1.4.11-1: Sample Clock Lane HS Rise Time Reference Waveform and Measurement**

This measurement will be performed for all three  $Z_{ID}$  cases.

In all cases, the value of  $t_R$  must be greater than 150ps and less than 0.3 UI (where UI is the nominal HS Unit Interval for the DUT, see Test 1.4.17) in order to be considered conformant [1].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that the Clock Lane is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source HS clock signaling on the Clock Lane (either burst or continuous).
- Capture the clock signaling using the DSO.
- Using post-processing methods, measure  $t_R$  as described above.
- Repeat the previous steps two additional times, once with the Clock Lane connected to the  $Z_{ID} = 125$  ohms Lane of the RTB, and again with the Clock Lane connected to  $Z_{ID} = 80$  ohms.

**Observable Results:**

For all three  $Z_{ID}$  cases:

- Verify that  $t_R$  is greater than 150ps and less than 0.3UI.

**Possible Problems:**

See Possible Problems comments for Test 1.3.4. The same applies to this test.

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**Test 1.4.12 – Clock Lane HS-TX 80%-20% Fall Time ( $t_F$ )**

**Purpose:** To verify that the 80%-20% Fall Time ( $t_F$ ) of the DUT Clock Lane HS Data Lane transmitter is within the conformance limits.

**References:**

[1] D-PHY Specification, Section 8.1.1, Table 17

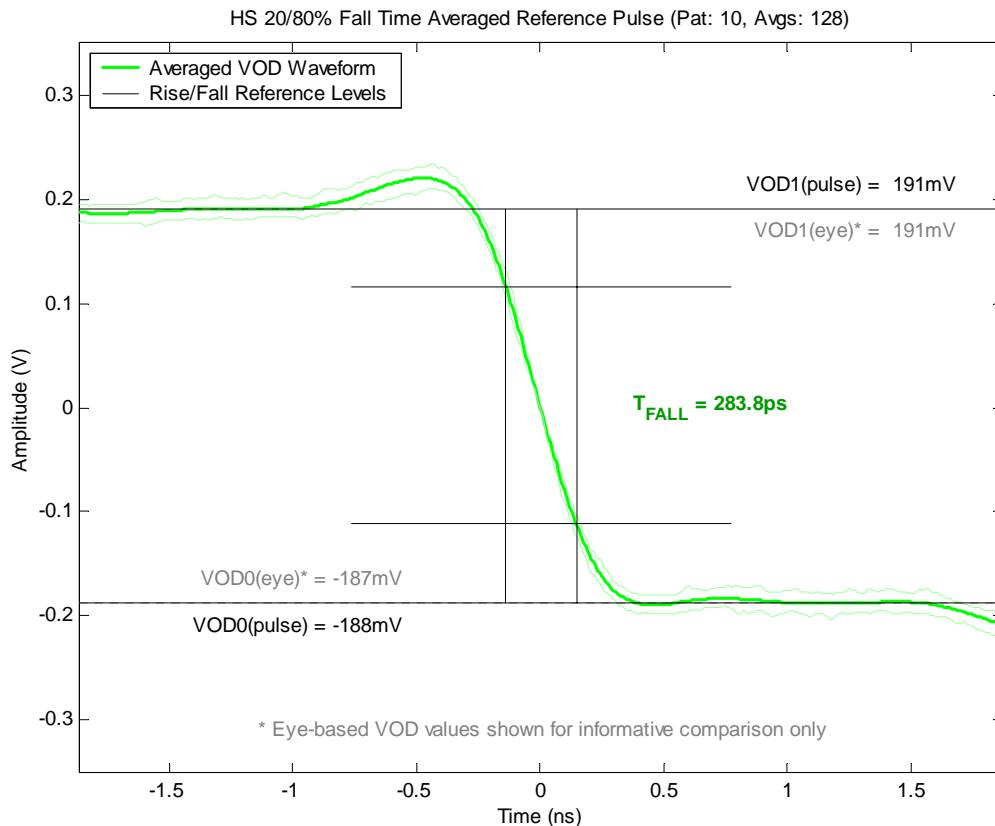
**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $t_F$ , which is a device's High-Speed TX 80%-20% Fall Time.

*(Note that the methodology for this test is identical to the rise time test of 1.4.11, except the fall time is measured on a reference 10 data pattern. The reference top and base levels are still the Clock Lane  $V_{OD(0)}$  and  $V_{OD(1)}$  values measured in Test 1.4.4. An example measurement is shown in Figure 1.4.12-1 below.)*



**Figure 1.4.12-1: Sample Clock Lane HS Fall Time Reference Waveform and Measurement**

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This measurement will be performed for all three  $Z_{ID}$  cases.

The value of  $t_F$  must be greater than 150ps and less than 0.3 UI (where UI is the nominal HS Unit Interval for the DUT, see Test 1.4.17) in order to be considered conformant [1].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that the Clock Lane is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source HS clock signaling on the Clock Lane (either burst or continuous).
- Capture the clock signaling using the DSO.
- Using post-processing methods, measure  $t_F$  as described above.
- Repeat the previous steps two additional times, once with the Clock Lane connected to the  $Z_{ID} = 125$  ohms Lane of the RTB, and again with the Clock Lane connected to  $Z_{ID} = 80$  ohms.

**Observable Results:**

For all three  $Z_{ID}$  cases:

- Verify that  $t_F$  is greater than 150ps and less than 0.3UI.

**Possible Problems:**

See Possible Problems comments for Test 1.3.4. The same applies to this test.

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**Test 1.4.13 – Clock Lane HS Exit:  $T_{CLK-TRAIL}$  Value**

**Purpose:** To verify that the duration that the DUT Clock Lane HS transmitter drives the final HS-0 differential state following the last payload clock bit of a HS transmission burst ( $T_{CLK-TRAIL}$ ) is greater than the minimum required value.

**References:**

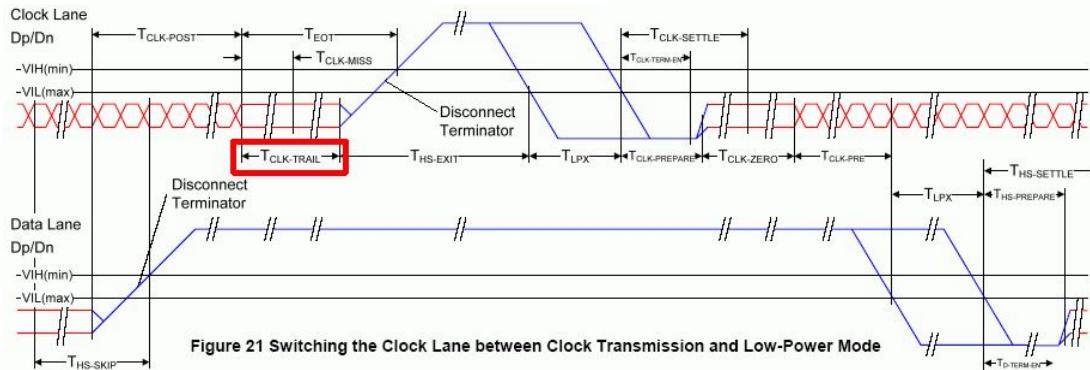
- [1] D-PHY Specification, Section 5.7, Table 10
- [2] Ibid, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

As part of the process for switching the Clock Lane out of HS mode, the D-PHY Specification provides a requirement for the duration of the final extended Clock Lane HS-0 state following the last payload clock bit of a HS transmission burst [1]. This interval is defined as  $T_{CLK-TRAIL}$ , and is shown in the figure below.



**Figure 1.4.13-1:  $T_{CLK-TRAIL}$  Interval**

(Note that the methodology for this test is essentially identical to the Data Lane  $T_{HS-TRAIL}$  test of 1.3.13, except the measurement is performed on the Clock Lane, and different conformance limits are applied.)

In this test, an HS Clock Lane signaling burst from the DUT transmitter will be captured using a real-time DSO. The differential waveform will be computed as difference of the positive and negative single-ended waveforms ( $V_{DP}-V_{DN}$ ). The  $T_{CLK-TRAIL}$  interval will be measured for the final extended HS differential state, at the points where the differential waveform enters and exits the minimum valid HS-RX differential range (i.e., when the differential waveform crosses +70 or -70mV). This measurement is performed only for the  $Z_{ID} = 100$  ohms test case.

The measured  $T_{CLK-TRAIL}$  value must be greater than 60ns in order to be considered conformant [2].

Also, a second observable result is defined for this test, which verifies the proper HS state during  $T_{CLK-TRAIL}$ . The differential HS state should be HS-0 during  $T_{CLK-TRAIL}$  in order to be considered conformant [2].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that the Clock Lane is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source an HS Exit sequence on the Clock Lane.
- Capture the HS Exit sequence using the DSO.

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- Using post-processing methods, measure  $T_{CLK-TRAIL}$  as described above.
- Using post-processing methods as described above, measure the HS state during  $T_{CLK-TRAIL}$  (HS-0 or HS-1).

**Observable Results:**

For  $Z_{ID} = 100\text{ohms}$ :

- Verify that  $T_{CLK-TRAIL}$  is at least 60ns.
- Verify that the  $T_{CLK-TRAIL}$  state is HS-0.

**Possible Problems:**

See Possible Problems comments for Test 1.4.1. The same applies to this test.

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**Test 1.4.14 – Clock Lane HS Exit: 30%-85% Post-EoT Rise Time ( $T_{REOT}$ )**

**Purpose:** To verify that the 30%-85% Post-EoT Rise Time ( $T_{REOT}$ ) of the DUT LP Clock Lane transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.2, Table 19

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $T_{REOT}$ , which is a device's LP-TX 30%-85% Rise Time, following an EoT exit from an HS Burst sequence. This requirement applies to both Clock Lanes (if non-continuous clocking is supported), as well as Data Lanes. (For Data Lane test, see 1.3.14).

*(Note that the methodology for this test is essentially identical to the Data Lane  $T_{REOT}$  test of 1.3.14, except the measurement is performed on the Clock Lane. The conformance limits are the same as the Data Lane case.)*

This measurement is performed only for the  $Z_{ID} = 100$  ohms test case.

The value of  $T_{REOT}$  must be less than 35ns in order to be considered conformant [1].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that the Clock Lane is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source an HS Exit sequence on the Clock Lane.
- Capture the HS Exit sequence using the DSO.
- Using post-processing methods, measure  $T_{REOT}$  as described above.

**Observable Results:**

For  $Z_{ID} = 100$ ohms:

- Verify that  $T_{REOT}$  is less than 35ns.

**Possible Problems:**

See Possible Problems comments for Test 1.4.1. The same applies to this test.

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**Test 1.4.15 – Clock Lane HS Exit:  $T_{EOT}$  Value**

**Purpose:** To verify that the interval measured from the start of the DUT Clock Lane HS transmitter's  $T_{CLK-TRAIL}$  to the start of the first Clock Lane LP-11 state ( $T_{EOT}$ ) is less than the maximum allowed limit.

**References:**

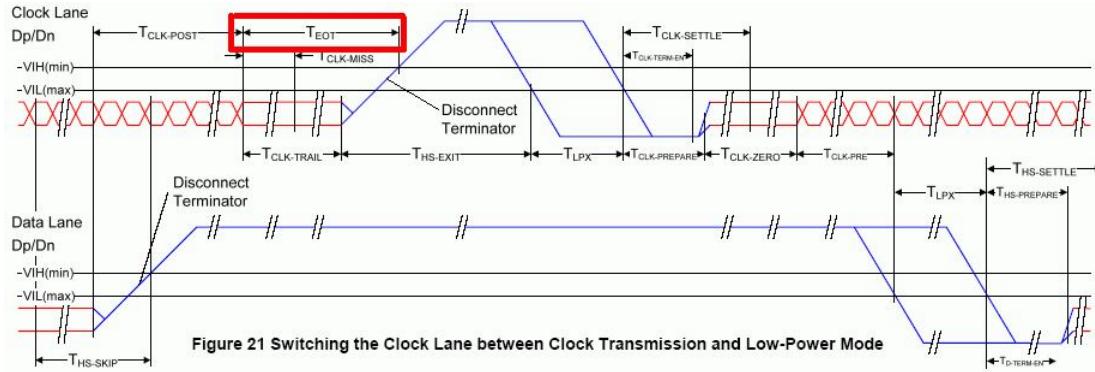
[1] D-PHY Specification, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

As part of the process for switching the Clock Lane out of HS mode, the D-PHY Specification provides a specification for the time interval measured from the start of the Master's  $T_{CLK-TRAIL}$  period to the start of the Clock Lane LP-11 state. This interval is defined as  $T_{EOT}$ , and is shown in the figure below.



**Figure 1.4.15-1:  $T_{EOT}$  Interval**

(Note that the methodology for this test is essentially identical to the Data Lane  $T_{EOT}$  test of 1.3.15, except the measurement is performed on the Clock Lane. The conformance limits are the same as the Data Lane case.)

This measurement is performed only for the  $Z_{ID} = 100$  ohms test case.

The specification defines the maximum conformance limit for  $T_{EOT}$  as  $(105\text{ns} + n \cdot 12\text{*UI})$  (where  $n = 1$  for Forward-direction HS mode, and  $n = 4$  for Reverse-direction HS mode, and UI is the nominal HS Unit Interval for the DUT, see Test 1.4.17). However, note that for this test the value of  $n$  will always be 1, as this test measures the Clock Lane  $T_{EOT}$  value, and the Clock Lane always operates in the Forward direction. Thus, the measured  $T_{EOT}$  result must be less than  $(105\text{ns} + 12\text{*UI})$  ns in order to be considered conformant [1].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Obtain the numerical values for  $T_{CLK-TRAIL}$  and Clock Lane  $T_{EOT}$ , obtained in previous Tests 1.4.13, and 1.4.14, respectively.
- Add the two values together to produce  $T_{EOT}$ .

**Observable Results:**

- Verify that  $T_{EOT}$  is less than  $105\text{ns} + 12\text{*UI}$ .

**Possible Problems:**

See Possible Problems comments for Test 1.4.1. The same applies to this test.

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**Test 1.4.16 – Clock Lane HS Exit:  $T_{HS-EXIT}$  Value**

**Purpose:** To verify that the duration that the Clock Lane transmitter remains in the LP-11 Stop state after exiting HS mode ( $T_{HS-EXIT}$ ), is greater than the minimum required value.

**References:**

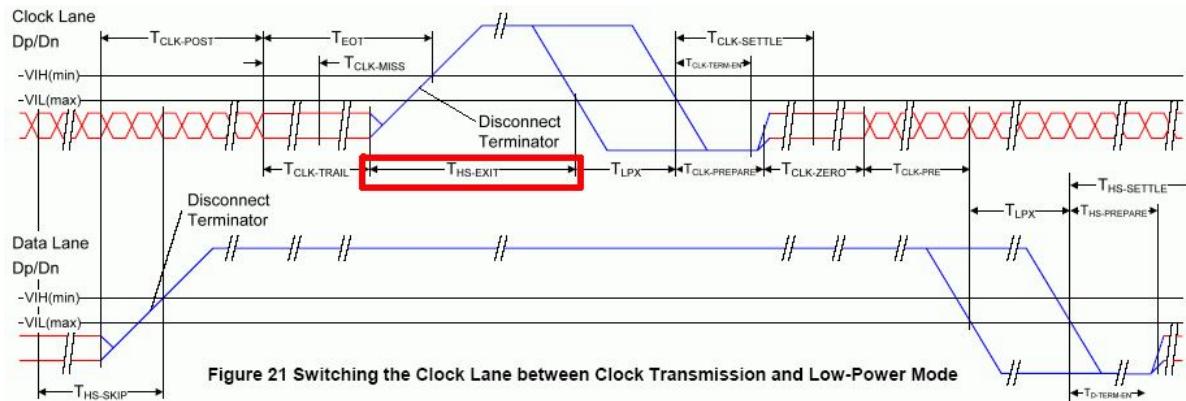
[1] D-PHY Specification, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

As part of the process for switching any D-PHY Lane (Clock or Data) out of HS mode, the D-PHY Specification provides a requirement for the minimum time that the transmitter must remain in the LP-11 Stop state before initiating any further sequences. (Note this test is only applicable to DUTs that support non-continuous clock behavior on the Clock Lane. For DUTs that only support continuous clock behavior, this test is considered Not Applicable.) This interval is defined as  $T_{HS-EXIT}$ , and is shown in the figure below.



**Figure 1.4.16-1:  $T_{HS-EXIT}$  Interval (Clock Lane Example Shown)**

(Note that the methodology for this test is essentially identical to the Data Lane  $T_{HS-EXIT}$  test of 1.3.16, except the measurement is performed on the Clock Lane. The conformance limits are the same as the Data Lane case.)

In this test, the DUT will be configured to send repeated HS burst sequences, and the Clock Lane  $T_{HS-EXIT}$  value will be observed. (Note the value should be observed over the same number of bursts as recommended in Test 1.3.16, and is measured in the same manner).

The measurement will be performed using the  $Z_{ID} = 100$  ohms termination case only.

The duration of  $T_{HS-EXIT}$  shall be no less than 100ns for all observed bursts in order to be considered conformant [1].

**Test Setup:** See Appendix B.1.2.

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**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that the Clock Lane is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source repeated HS burst sequences on the Clock Lane.
- Capture the HS burst sequences using the DSO.
- Using post-processing methods, measure  $T_{HS-EXIT}$  as described above.

**Observable Results:**

For  $Z_{ID} = 100$ ohms:

- Verify that  $T_{HS-EXIT}$  is no less than 100ns for all observed bursts.

**Possible Problems:**

See comments under Possible Problems for the Data Lane test of 1.3.16 regarding the testing of DUTs that transmit either very long HS bursts and/or very long LP intervals between bursts, as the same comments apply to this test.

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**Test 1.4.17 – Clock Lane HS Clock Instantaneous ( $UI_{INST}$ )**

**Purpose:** To verify that the Instantaneous Unit Interval values ( $UI_{INST}$ ) of the DUT HS Clock are within the conformance limits.

**References:**

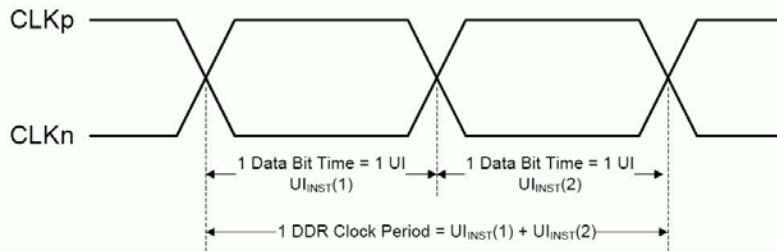
- [1] D-PHY Specification, Section 9.1, Lines 1585-1589 (Including Table 26)
- [2] Ibid, Section 9.2.1, Lines 1605-1607

**Resource Requirements:** See Appendix A.1.

**Last Modification:** September 16, 2010

**Discussion:**

Section 9 of the D-PHY Specification defines the High Speed Data-Clock requirements for D-PHY products. Included in these requirements is a specification for  $UI_{INST}$ , which are a device's instantaneous Clock Lane Unit Interval values. An example figure showing this parameter is provided in the specification, and is reproduced in the figure below.



**Figure 51 DDR Clock Definition**

**Figure 1.4.17-1:  $UI_{INST}$  Interval**

The specification states, “*Implementers shall specify a value  $UI_{INST,MIN}$  that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation.*” [2]. This value must be obtained from the DUT vendor (either directly, or via the DUT’s datasheet) prior to performing this test.

The specification defines an upper conformance limit for  $UI_{INST}$  of 12.5ns, which corresponds to a minimum allowed HS data rate of 80Mbps[1]. There is no lower conformance value defined by the specification, however the specification does state as a note to the table specification for  $UI_{INST}$ , “*The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.*” [1]. Note that this statement is somewhat ambiguous, as the minimum value entry in the table for which the note applies shows an empty value. However, for the purposes of this test, this requirement is interpreted to refer to the  $UI_{INST, MIN}$  value indicated by the DUT vendor, mentioned above.

In this test, a sample of the DUTs HS clock signaling will be captured using a real-time DSO. The measurement will be performed using the  $Z_{ID} = 100$  ohms termination case only. The sample shall contain a minimum of 5,000 UIs (i.e., ‘Data Bit Times’ as shown the figure above), and may be obtained across multiple captures, if needed. The differential Clock Lane waveform will be computed as difference of the positive and negative single-ended Clock Lane waveforms ( $V_{DP}-V_{DN}$ ). The  $UI_{INST}$  values for each UI will be measured as the difference between successive 0V crossing times of the differential waveform. The maximum, minimum, and average  $UI_{INST}$  values will be measured and reported across all observed HS UIs.

The maximum observed  $UI_{INST}$  value must be less than 12.5ns in order to be considered conformant [2]. The minimum observed  $UI_{INST}$  value must be greater than the  $UI_{INST, MIN}$  value indicated by the DUT vendor in order to be considered conformant [1].

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**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Obtain the stated  $UI_{INST, MIN}$  value for the DUT (either directly from the DUT supplier, or via the DUT's datasheet.)
- Connect the DUT to the Reference Termination Board, such that the Clock Lane is connected to an RTB Lane with  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source HS clock signaling on the Clock Lane (either burst or continuous).
- Capture the HS clock signaling using the DSO.
- Using post-processing methods, measure the maximum, minimum, and mean  $UI_{INST}$  values over a minimum of 5,000 UIs, as described above.

**Observable Results:**

- Verify that the maximum  $UI_{INST}$  value is less than 12.5ns.
- Verify that the minimum  $UI_{INST}$  value is greater than or equal to the  $UI_{INST, MIN}$  value.
- The mean  $UI_{INST}$  value is reported for procedural purposes (as it is used in other tests in this test suite to calculate conformance limits for parameters whose ranges are either partially or entirely defined in terms of UI values).

**Possible Problems:** None.

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**GROUP 5: HS-TX CLOCK-TO-DATA LANE TIMING REQUIREMENTS**

**Overview:**

This group of tests verifies various requirements regarding Clock Lane to Data Lane timing.

This test Group is applicable to Master devices only. (It is considered Not Applicable for Slave devices.)

**Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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**Test 1.5.1 – HS Entry:  $T_{CLK-PRE}$  Value**

**Purpose:** To verify that the time that the HS clock is driven prior to an associated Data Lane beginning the transition from LP to HS mode ( $T_{CLK-PRE}$ ), is greater than the minimum required value.

**References:**

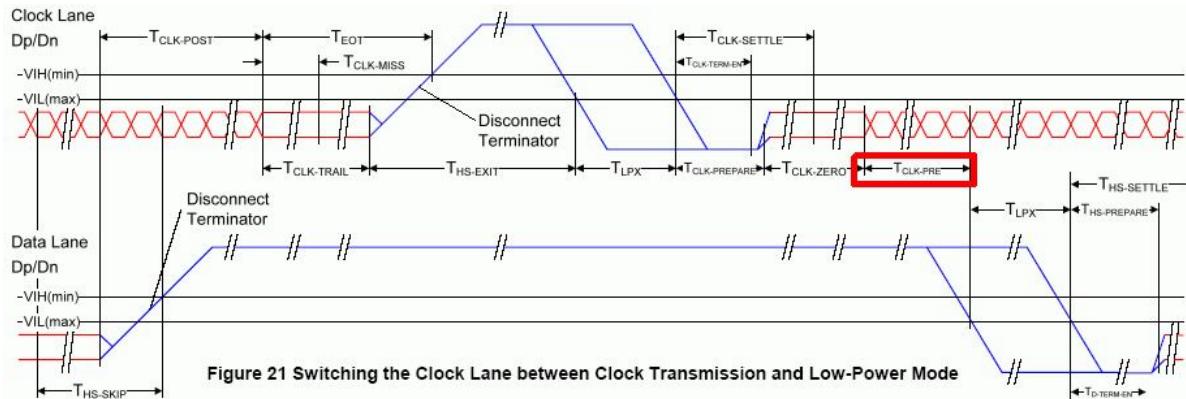
[1] D-PHY Specification, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

As part of the process for initiating an HS data burst transmission, the D-PHY Specification provides a requirement for the minimum duration that the Master must transmit valid HS Clock signaling before driving any Data Lane out of LP mode. This interval is defined as  $T_{CLK-PRE}$ , and is shown graphically in the figure below.



**Figure 1.5.1-1:  $T_{CLK-PRE}$  Interval**

In this test, the DUT will be configured to send repeated HS burst sequences, and the  $T_{CLK-PRE}$  value will be observed. The  $T_{CLK-PRE}$  interval is measured from the end of the Clock Lane  $T_{CLK-ZERO}$  interval (at the point where the Clock Lane differential waveform crosses below the minimum valid HS-RX differential threshold level of  $\pm 70\text{mV}$ ) to the point where the Data Lane's  $V_{DP}$  LP-01 falling edge crosses  $V_{IL,\text{MAX}}$  ( $550\text{mV}$ ). The measurement will be performed using the  $Z_{ID} = 100$  ohms termination case only, and will be measured for all Data Lanes.

For all observed bursts, and all Data Lanes, the measured value of  $T_{CLK-PRE}$  must be greater than  $8*\text{UI}$  ns in order to be considered conformant [1], (where UI is the mean HS Unit Interval value for the DUT, measured in Test 1.4.17).

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that both the Clock Lane and Data Lane 0 are connected to RTB Lanes that have  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source repeated HS burst sequences on Data Lane 0.
- Capture the Clock Lane and Data Lane 0 HS burst sequences using the DSO.
- Using post-processing methods, measure  $T_{CLK-PRE}$  as described above.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

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**Observable Results:**

For all Data Lanes:

- Verify that  $T_{CLK-PRE}$  is greater than  $(8*UI)$  ns.

**Possible Problems:**

See Possible Problems comments for Test 1.4.1 regarding performing this test on continuous-clocking-mode DUTs. The same applies to this test.

Also see Possible Problems comments for Test 1.3.1 regarding performing this test on a DUT that has more than two Data Lanes. The same applies to this test.

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**Test 1.5.2 – HS Exit:  $T_{CLK-POST}$  Value**

**Purpose:** To verify that the DUT Clock Lane HS transmitter continues to transmit clock signaling for the minimum required duration ( $T_{CLK-POST}$ ) after the last Data Lane switches to LP mode.

**References:**

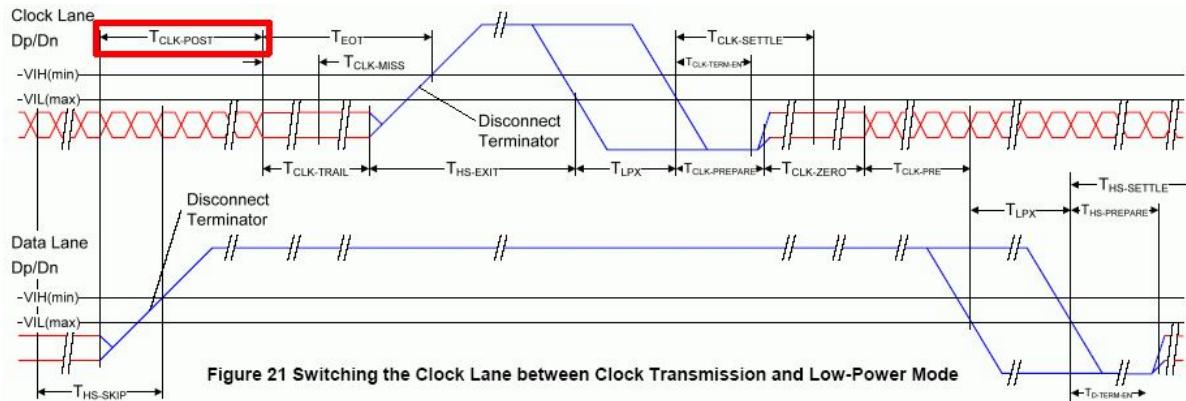
[1] D-PHY Specification, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

As part of the process for completing an HS data burst transmission, the D-PHY Specification provides a requirement for the minimum duration that the Master must continue to transmit HS Clock signaling after the last Data Lane has switched to LP mode. (Note this test is only applicable to DUTs that support non-continuous clock behavior on the Clock Lane). This interval is defined as  $T_{CLK-POST}$ , and is shown graphically in the figure below.



**Figure 1.5.2-1:  $T_{CLK-POST}$  Interval**

In this test, the DUT will be configured to send repeated HS burst sequences, and the  $T_{CLK-POST}$  value will be observed. The  $T_{CLK-POST}$  interval is measured from the end of the Data Lane  $T_{HS-TRAIL}$  period to the start of the Clock Lane  $T_{CLK-TRAIL}$  period. (Note for measurement specifics regarding the  $T_{HS-TRAIL}$  and  $T_{CLK-TRAIL}$  intervals, see Tests 1.3.13 and 1.4.13, respectively.) The measurement will be performed using the  $Z_{ID} = 100$  ohms termination case only, and will be measured for all Data Lanes.

For all observed bursts, and all Data Lanes, the measured value of  $T_{CLK-POST}$  must be greater than  $(60\text{ns} + 52*\text{UI}) \text{ ns}$  in order to be considered conformant [1], (where UI is the mean HS Unit Interval value for the DUT, measured in Test 1.4.17).

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that both the Clock Lane and Data Lane 0 are connected to RTB Lanes that have  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source repeated HS burst sequences on Data Lane 0.
- Capture the Clock Lane and Data Lane 0 HS burst sequences using the DSO.
- Using post-processing methods, measure  $T_{CLK-POST}$  as described above.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

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**Observable Results:**

For all Data Lanes:

- Verify that  $T_{CLK-POST}$  is greater than  $(60\text{ns} + 52*\text{UI}) \text{ ns}$ .

**Possible Problems:**

See Possible Problems comments for Test 1.3.1 regarding performing this test on a DUT that has more than two Data Lanes. The same applies to this test.

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**Test 1.5.3 – HS Clock Rising Edge Alignment to First Payload Bit**

**Purpose:** To verify that the DUT HS Clock is properly aligned to the payload data signaling.

**References:**

- [1] D-PHY Specification, Section 9.2, Line 1594

**Resource Requirements:** See Appendix A.1.

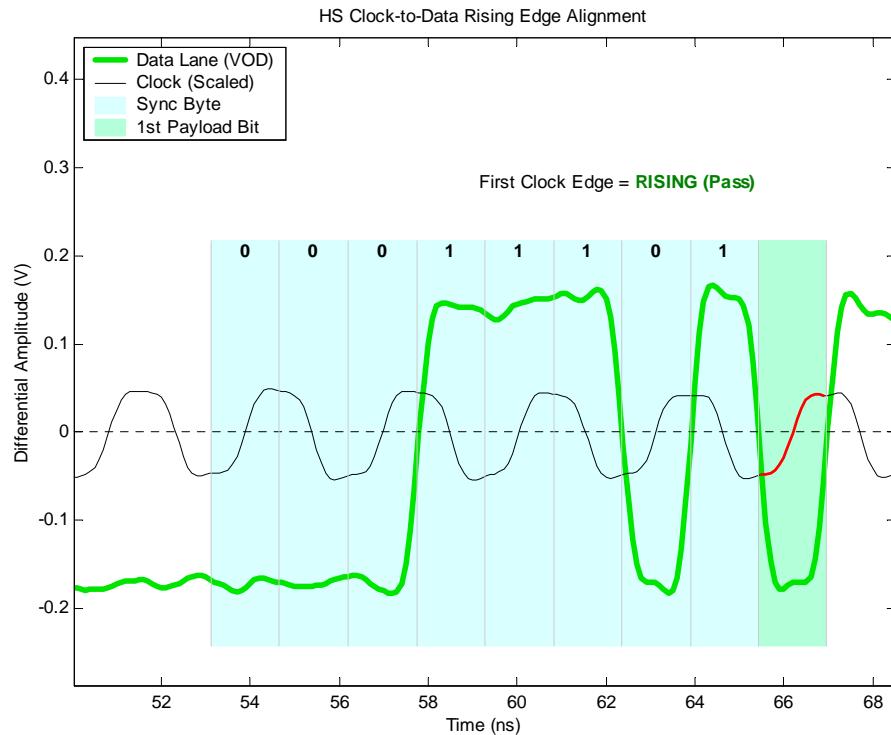
**Last Modification:** September 16, 2010

**Discussion:**

Section 9 of the D-PHY Specification defines the High Speed Data-Clock requirements for D-PHY products. Included in these requirements is a specification regarding the phase relationship between the Clock and Data Lane edges.

The D-PHY Specification states, “*The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.*” [1].

In this test, the DUT will be configured to send repeated Data Lane HS burst sequences, and the Clock and Data Lane signals will be observed using a real-time DSO. The signaling will be observed to verify that the first payload bit of burst data (i.e., the first bit after the Sync byte) aligns with a rising edge of the DDR clock, as shown in Figure 1.5.3-1 below.



**Figure 1.5.3-1: Sample Clock Rising Edge Alignment Measurement**

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The measurement will be performed using the  $Z_{ID} = 100$  ohms termination case only, and will be measured for all Data Lanes.

For all observed bursts, and for all Data Lanes, the first Data Lane payload bit of each transmission burst should align with a rising edge of the DDR clock in order to be considered conformant [1].

**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that both the Clock Lane and Data Lane 0 are connected to RTB Lanes that have  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source repeated HS burst sequences on Data Lane 0.
- Capture the HS burst sequences (and associated Clock Lane signaling) using the DSO.
- Observe (either by visual inspection, or post-processing techniques) the direction of the DDR clock edge (i.e., rising or falling) that corresponds to the first Data Lane payload bit of the transmission burst.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For all Data Lanes:

- Verify that the first payload bit of the burst data aligns with a rising edge of the DDR clock.

**Possible Problems:** None.

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**Test 1.5.4 – Data-to-Clock Skew ( $T_{SKEW[TX]}$ )**

**Purpose:** To verify that the skew between the clock and data signaling, as measured at the transmitter ( $T_{SKEW[TX]}$ ) is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 9.2.1, Line 1607
- [2] Ibid, Section 9.2.1, Table 27

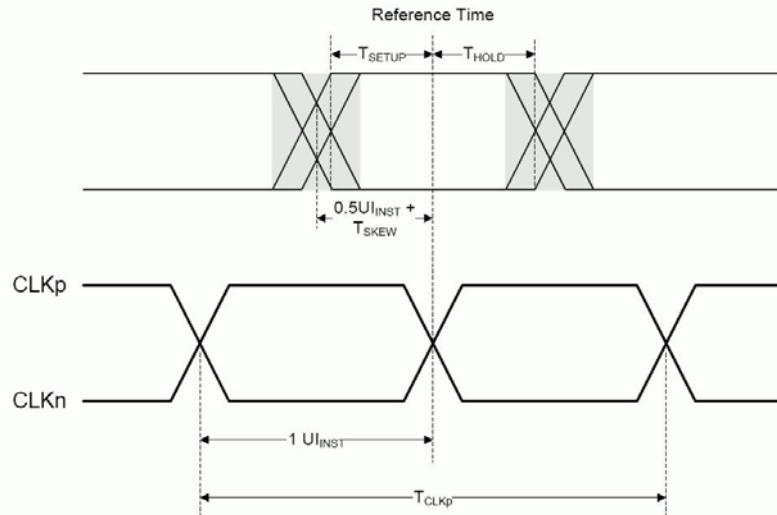
**Resource Requirements:** See Appendix A.1.

**Last Modification:** November 30, 2009

**Discussion:**

Section 9 of the D-PHY Specification defines the High Speed Data-Clock requirements for D-PHY products. Included in these requirements is a specification regarding the skew between the Clock and Data Lane edges.

The specification states, “*The skew specification,  $T_{SKEW[TX]}$ , is the allowed deviation of the data launch time to the ideal  $\frac{1}{2}UI_{INST}$  displaced quadrature clock edge.*”[1]. This relationship is graphically demonstrated via a figure in the specification, which is reproduced in the figure below.



**Figure 52 Data to Clock Timing Definitions**

**Figure 1.5.4-1:  $T_{SKEW[TX]}$  Definition**

In this test, the DUT will be configured to transmit repeated HS burst sequences, and the Clock and Data Lane signals will be observed using a real-time DSO. The timing error,  $T_{SKEW[TX]}$ , between each Data Lane edge and its respective Clock Lane edge will be computed over a minimum of 10,000 edges, to produce an array of timing error values. The maximum, minimum, and mean timing error values measured across all observed edges will be recorded. The measurement will be performed using the  $Z_{ID} = 100$  ohms termination case only, and will be measured for all Data Lanes.

For all observed edges and all Data Lanes, the maximum, minimum, and mean timing error values must be within the range  $(0.50 \pm 0.15) * UI_{INST}$ , in order to be considered conformant[2], (where  $UI_{INST}$  is the mean HS Unit Interval value for the DUT, measured in Test 1.4.17).

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**Test Setup:** See Appendix B.1.2.

**Test Procedure:**

- Connect the DUT to the Reference Termination Board, such that both the Clock Lane and Data Lane 0 are connected to RTB Lanes that have  $Z_{ID} = 100$  ohms.
- Create a condition that causes the DUT to source repeated HS burst sequences on Data Lane 0.
- Capture the HS burst sequences (and associated Clock Lane signaling) using the DSO.
- Compute the  $T_{SKEW[TX]}$  Clock-to-Data timing error values, as described above.
- Record the max, min, and mean timing error values.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

For all Data Lanes:

- Verify that the max, min, and mean Clock-to-Data timing error values are within the range  $(0.50 \pm 0.15) * UI_{INST}$ .

**Possible Problems:**

See Possible Problems comments for Test 1.3.1 regarding performing this test on a DUT that has more than two Data Lanes. The same applies to this test.

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## **GROUP 6: LP-TX INIT, ULPS, AND BTA REQUIREMENTS**

### **Overview:**

This group of tests verifies several miscellaneous LP-TX timing and behavioral requirements pertaining to initialization (INIT), Ultra-Low Power State (ULPS), and Bus Turnaround (BTA).

These tests are applicable to both Master and Slave devices, depending on the test. Tests 1.6.1, 1.6.2, and 1.6.3 are applicable to Master devices only. Tests 1.6.4, 1.6.5, and 1.6.6 are applicable for any devices (Master or Slave) that support bi-directional operation.

### **Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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**Test 1.6.1 – INIT: LP-TX Initialization Period ( $T_{INIT,MASTER}$ )**

**Purpose:** To verify that the duration of the DUT's transmitted LP Initialization period ( $T_{INIT,MASTER}$ ), is greater than the minimum required value.

**References:**

- [1] D-PHY Specification, Section 5.11, Line 985
- [2] Ibid, Section 5.11, Line 991
- [3] Ibid, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.

**Last Modification:** September 16, 2010

**Discussion:**

The D-PHY Specification includes requirements pertaining to the initialization behavior of both Master and Slave devices (where the Master is by definition the side that transmits the HS Clock). Included in these requirements is a specification for  $T_{INIT,MASTER}$ , which is the Master PHY's transmitted initialization period. (Note that this test is only applicable to Master DUTs.)

The specification states, “*After power-up, the Slave side PHY shall be initialized when the Master PHY drives a Stop State (LP-11) for a period longer than  $T_{INIT}$ . The first Stop state longer than the specified  $T_{INIT}$  is called the Initialization period. The Master PHY itself shall be initialized by a system or Protocol input signal (PPI). The Master side shall ensure that a Stop State longer than  $T_{INIT}$  does not occur on the Lines before the Master is initialized. The Slave side shall ignore all Line states during an interval of unspecified length prior to the Initialization period.*” [1]

The specification also states, “*Note that  $T_{INIT}$  is considered a protocol-dependent parameter, and thus the exact requirements for  $T_{INIT,MASTER}$  and  $T_{INIT,SLAVE}$  (transmitter and receiver initialization Stop state lengths, respectively,) are defined by the protocol layer specification and are outside the scope of this document. However, the D-PHY specification does place a minimum bound on the lengths of  $T_{INIT,MASTER}$  and  $T_{INIT,SLAVE}$ , which each shall be no less than 100  $\mu$ s. A protocol layer specification using the D-PHY specification may specify any values greater than this limit, for example,  $T_{INIT,MASTER} \geq 1$  ms and  $T_{INIT,SLAVE} = 500$  to 800  $\mu$ s.*” [2]

The purpose of this test will be to measure the DUT's  $T_{INIT,MASTER}$  value, and verify that it is at least 100us, in order to verify the minimum requirements described by the D-PHY specification. (This test does not verify any additional requirements that may be imposed by an applicable protocol specification.)

Note also that because  $T_{INIT}$  is considered a protocol-dependent parameter by the D-PHY specification, it is possible that the generation and timing control of the  $T_{INIT}$  interval may be implemented in the protocol layer logic for some DUT types. Therefore, if a DUT is not designed to contain this logic (e.g., for a bare-phy DUT with a PPI or other exposed protocol interface), this test is considered Not Applicable.

In this test, the length of the Master's transmitted LP-11 Initialization period ( $T_{INIT,MASTER}$ ) will be observed using a real-time DSO. (Note that the termination environment is not critical to this measurement, and either the  $C_{LOAD}$  fixture, RTB, or no termination fixture may be used.) The length of  $T_{INIT,MASTER}$  will be measured starting from the point where both  $V_{DP}$  and  $V_{DN}$  are first observed to be greater than  $V_{IH,MIN}$  (880mV) following a power-on event, and ending at the first point where either  $V_{DP}$  or  $V_{DN}$  crosses below  $V_{IL,MAX}$  (550mV). The measurement will be performed on all Clock and Data Lanes.

For all Lanes, the value of  $T_{INIT,MASTER}$  must be greater than or equal to 100us in order to be considered conformant [3].

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**Test Setup:** See Appendix B.1.1 (or B.1.2).

**Test Procedure:**

- Connect the DUT to the Test Setup, leaving the DUT power off.
- Configure the DSO to capture the DUT's LP-11 Initialization period on Data Lane 0.
- Power on the DUT.
- Verify that the DSO was able to successfully capture the Initialization period.
- Measure the LP-11 Initialization period duration ( $T_{INIT,MASTER}$ ), as described above.
- Repeat the previous four steps for all other Data Lanes, as well as the Clock Lane.

**Observable Results:**

- For all Lanes, verify that  $T_{INIT,MASTER}$  is no less than 100us.

**Possible Problems:**

Note that because the  $T_{INIT,MASTER}$  period may be much longer than 100us in some cases, it may not be possible to capture the entire LP-11 period within the available memory depth of the DSO. In these cases, other acquisition methods may be used (e.g., segmented capturing) to determine when the LP-11 start and end times occur, without requiring the entire LP-11 state to be captured in a single waveform.

Also, care should be taken to verify that no other unexpected LP transitions or glitches occur before the LP-11 Initialization sequence occurs (as if there are any unexpected sequences sent, they could potentially affect interoperability with other devices.)

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**Test 1.6.2 – ULPS Entry: Verification of Clock Lane LP-TX ULPS support**

**Purpose:** To verify that the DUT's LP-TX properly implements the Clock Lane ULPS entry sequence.

**References:**

- [1] D-PHY Specification, Section 5.8, Line 943

**Resource Requirements:** See Appendix A.

**Last Modification:** November 30, 2009

**Discussion:**

The D-PHY Specification defines requirements for Ultra-Low Power State (ULPS) behavior for both Clock and Data Lanes. The requirements for Clock and Data Lanes are not identical in all cases, as the Clock Lane ULPS behavior is defined to operate differently than a Data Lane, in terms of how the ULPS state is initiated by the Master DUT. (Note that this test is only applicable to Master DUTs.)

The D-PHY Specification states, “*Although a Clock Lane does not include regular Escape mode, the Clock Lane shall support the Ultra-Low Power State. A Clock Lane shall enter Ultra-Low Power State via a Clock Lane Ultra-Low Power State Entry procedure. In this procedure, starting from Stop state, the transmit side shall drive TX-ULPS-Rqst State (LP-10) and then drive TX-ULPS State (LP-00). After this, the Clock Lane shall enter Ultra-Low Power State.*” [1].

The purpose of this test is simply to verify that the DUT's LP-TX implements the proper ULPS entry sequence on the Clock Lane.

In this test, the DUT's Clock Lane LP-TX behavior will be observed while the DUT is configured to source a ULPS request on the Clock Lane. Note that the termination environment is not critical to this measurement, and either the C<sub>LOAD</sub> fixture, RTB, or no termination fixture may be used.

The DUT must source the proper LP-11/10/00 Clock Lane ULPS Entry sequence in order to be considered conformant.

**Test Setup:** See Appendix B.1.1 (or B.1.2).

**Test Procedure:**

- Connect the DUT to the Test Setup.
- Configure the DSO to capture a ULPS Entry sequence on the Clock Lane (e.g., trigger on an LP falling edge on either D<sub>p</sub> or D<sub>n</sub>.)
- Configure the DUT to source a ULPS request on the Clock Lane.
- Capture the Clock Lane ULPS request.

**Observable Results:**

- Verify that the DUT transmits the proper LP-11/10/00 Clock Lane ULPS Entry sequence.

**Possible Problems:** None.

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**Test 1.6.3 – ULPS Exit: Transmitted  $T_{WAKEUP}$  Interval**

**Purpose:** To verify that the DUT transmits Mark-1 for the proper duration ( $T_{WAKEUP}$ ) when initiating a Clock or Data Lane ULPS Exit sequence.

**References:**

- [1] D-PHY Specification, Section 5.6.3, Line 895
- [2] Ibid, Section 5.8, Line 951
- [2] Ibid, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.

**Last Modification:** September 16, 2010

**Discussion:**

The D-PHY Specification defines a mechanism for bringing Lanes out of the ULPS state. This process involves driving a Mark-1 state (LP-10) for a minimum time  $T_{WAKEUP}$ , followed by a Stop state (LP-11), which should be detected by the Slave device. (Note that this test is only applicable to Master DUTs.)

For Data Lanes, the specification states, “*If the Ultra-Low Power State Entry Command is sent after an Escape mode Entry command, the Lane shall enter the Ultra-Low Power State (ULPS). This command shall be flagged to the receive side Protocol. During this state, the Lines are in the Space state (LP-00). Ultra-Low Power State is exited by means of a Mark-1 state with a length  $T_{WAKEUP}$ , followed by a Stop state.*” [1]

For Clock Lanes, the specification states, “*The receiving PHY shall flag the appearance of ULP State to the receive side Protocol. During this state the Lines are in the ULP State (LP-00). Ultra-Low Power State is exited by means of a Mark-1 TX-ULPS-Exit State with a length  $T_{WAKEUP}$ , followed by a Stop State.*” [2]

The purpose of this test is to verify that a DUT transmits Mark-1 for the minimum required duration when initiating a ULPS exit on either a Clock or Data Lane. Note that the termination environment is not critical to this measurement, and either the C<sub>LOAD</sub> fixture, RTB, or no termination fixture may be used. The DUT will be instructed to put both the Clock and Data Lanes into ULPS mode, and then subsequently initiate a ULPS exit on all Lanes, allowing the Mark-1 duration to be observed. For each Lane,  $T_{WAKEUP}$  is measured from the start of the Mark-1 state (at the point where the Dp line of LP-10 transition crosses V<sub>IH,MIN</sub> = 880mV), to the start of the Stop state (at the point where the Dn line of LP-11 transition crosses V<sub>IH,MIN</sub> = 880mV).

Note that the generation and timing control of the  $T_{WAKEUP}$  interval may be implemented in the protocol layer logic for some DUT types. Therefore, if a DUT is not designed to contain this logic (e.g., for a bare-phy DUT with a PPI or other exposed protocol interface), this test is considered Not Applicable.

For each Lane, the measured  $T_{WAKEUP}$  value should be greater than or equal to 1ms.

**Test Setup:** See Appendix B.1.1 (or B.1.2).

**Test Procedure:**

- Connect the DUT to the Test Setup.
- Configure the DSO’s trigger to observe the  $T_{WAKEUP}$  for Data Lane 0.
- Configure the DUT to transmit a ULPS Entry sequence followed by a Mark-1 ULPS Exit sequence.
- Capture the ULPS Exit sequence on the DSO.
- Measure  $T_{WAKEUP}$  for the ULPS Exit sequence as described above.
- Repeat the previous four steps for all other Data Lanes, and the Clock Lane.

**Observable Results:**

- For all Lanes, verify that  $T_{WAKEUP}$  is greater than or equal to 1ms.

**Possible Problems:** See Possible Problems of Test 1.6.1 regarding capturing/measuring of intervals that are longer than the DSO memory depth. The same applies to this test.

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**Test 1.6.4 – BTA: TX-Side  $T_{TA-GO}$  Interval Value**

**Purpose:** To verify that the DUT drives the Bridge state (LP-00) for the proper period ( $T_{TA-GO}$ ), when handing off control of the Link during a Link Turnaround procedure.

**References:**

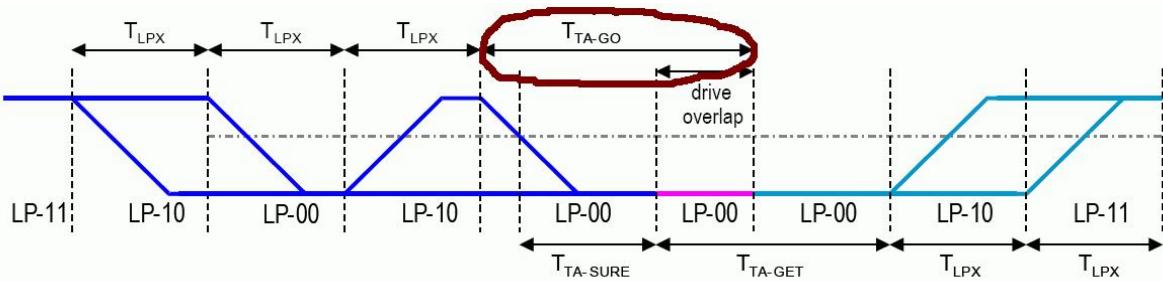
- [1] D-PHY Specification, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.

**Last Modification:** November 30, 2009

**Discussion:**

The Link Turnaround process consists of a LP handshake/handoff procedure between the Master and Slave sides of the Link. (Note that ‘Master’ is defined as the device that supplies the HS Clock.) The controlling (‘TX-Side’) device initiates the handoff process by signaling Stop/LP-Rqst/Bridge/LP-Rqst/Stop (LP-11/10/00/10/00). The receiving (‘RX-Side’) device then assumes control of the link, simultaneously driving the Bridge state (LP-00), followed by its own LP-Rqst and Stop states (LP-10/11), after which the transfer process is considered complete. A picture of the entire Turnaround procedure (reproduced from Figure 16 of the D-PHY Specification), which shows the  $T_{TA-GO}$  interval, is shown below:



**Figure 16 Turnaround Procedure**

**Figure 1.6.4-1:  $T_{TA-GO}$  Interval**

The specification defines  $T_{TA-GO}$  as the, “*Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.*”[1]. Therefore, the  $T_{TA-GO}$  period begins at the start of the last TX-Side LP-00 state (i.e., where  $V_{DP}$  crosses below  $V_{IL,MAX}$  (550mV)), and ends when the TX-Side device ceases transmission (during the ‘drive overlap’ period, above).

If the exact point cannot be observed, an alternative methodology would require measuring the entire time interval from the end of the last TX-Side LP-10 to the beginning of the first RX-Side LP-10, then subtracting one nominal RX-Side  $T_{LPX}$  interval (measured separately). The remaining value would be  $T_{TA-GO}$ . (Note this methodology is not used in the formal test procedure defined below, but is mentioned here only for informative purposes.)

Note also that this test is specific to the device *that is handing off control of the Link*. For Master DUTs (e.g., Host Processors), the measurement can be performed by initiating a single Turnaround operation from the Master device. For Slave DUTs (e.g., displays), the Link must first be turned around once (putting the Slave device in control). Then, a second Turnaround operation must be performed to transfer control back to the Master, where the measurement is made on the Slave’s transmitted signaling while it is acting as the TX-Side device.

The specification states that  $T_{TA-GO}$  must be greater than or equal to  $4*T_{LPX}$  ns in order to be considered conformant [1], where  $T_{LPX}$  is the average LP state duration of the DUT. (Note that for Master DUT’s, this should be the  $T_{LPX}$  result measured in Test 1.3.1. However, in cases where Test 1.3.1 is not performed (e.g., for a Display

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(Slave) DUT),  $T_{LPX}$  can be measured from the LP states of the Turnaround sequence itself, during the states where the DUT is operating as the TX-Side device.)

**Test Setup:** See Appendix B.1.3.

**Test Procedure:**

- Connect the DUT to the Test Setup.
- Create an event that causes the Master to initiate a Turnaround sequence.
- If the DUT is a Master device, capture the Turnaround sequence on the DSO, and measure  $T_{TA-GO}$  for the Master device, as described above. (Otherwise continue to next step.)
- If the DUT is a Slave device, the Slave DUT should eventually initiate another Turnaround sequence on its own, to return control back to the Master. Capture this second Turnaround sequence on the DSO, and measure  $T_{TA-GO}$  for the Slave device, as described above.

**Observable Results:**

- Verify that the DUT's  $T_{TA-GO}$  interval is greater than or equal to  $4*T_{LPX}$  ns.

**Possible Problems:**

Note that in practical situations, the end point of the drive overlap period may not be easily observable, particularly if the Master and Slave devices both use similar LP-0 voltage levels (i.e.,  $V_{OL}$ ). However, the observability of the drive overlap period can be improved by configuring the Master and/or Slave devices to use different (but still valid)  $V_{OL}$  levels, if such configuration capability is available.

Also, this test is generally intended to be performed manually (e.g., using DSO cursors to measure the timings on the captured waveform), as the measurement start/end points may be difficult to reliably determine using algorithmic methods.

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**Test 1.6.5 – BTA: RX-Side  $T_{TA-SURE}$  Interval Value**

**Purpose:** To verify that the DUT waits the required period ( $T_{TA-SURE}$ ) while observing the TX-Side Bridge state (LP-00), when receiving control of the Link during a Link Turnaround procedure.

**References:**

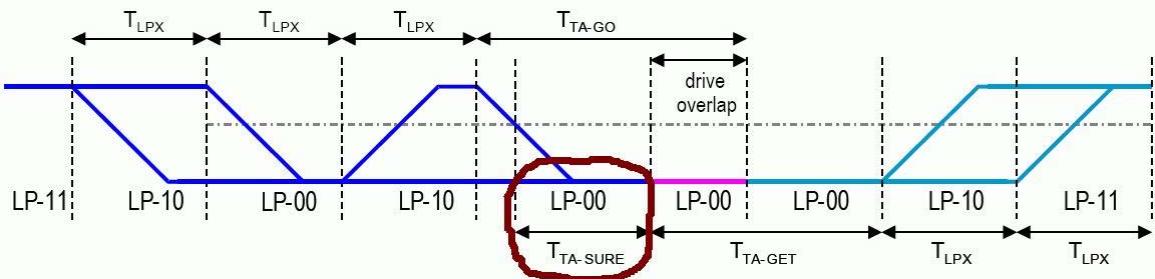
- [1] D-PHY Specification, Section 5.9, Table 14
- [2] Ibid, Section 5.5, Table 6

**Resource Requirements:** See Appendix A.

**Last Modification:** November 30, 2009

**Discussion:**

The Link Turnaround process consists of a LP handshake/handoff procedure between the Master and Slave sides of the Link. (Note that ‘Master’ is defined as the device that supplies the HS Clock.) The controlling (‘TX-Side’) device initiates the handoff process by signaling Stop/LP-Rqst/Bridge/LP-Rqst/Stop (LP-11/10/00/10/00). The receiving (‘RX-Side’) device then assumes control of the link, simultaneously driving the Bridge state (LP-00), followed by its own LP-Rqst and Stop (LP-10/11), after which the transfer process is considered complete. A picture of the entire Turnaround procedure (reproduced from Figure 16 of the D-PHY Specification), showing the  $T_{TA-SURE}$  interval, is shown below:



**Figure 16 Turnaround Procedure**

**Figure 1.6.5-1:  $T_{TA-SURE}$  Interval**

The specification defines  $T_{TA-SURE}$  as the, “*Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.*” [1]. Also, according to the specification, the  $T_{TA-SURE}$  interval begins when the RX-Side “*observes the transition from LP-10 to Bridge state*”[2], and ends when the RX-Side begins transmission during the ‘drive overlap’ period (see above). Note this starting point is technically slightly different from the  $T_{TA-GO}$  interval test, and starts when the RX-Side device *observes the transition to the Bridge state*, not when the transition itself begins. However, as this time point cannot be externally observed, the best reasonable estimate is to use the time point where the voltage crosses the maximum allowable RX Logic 0 threshold (550mV). This is the earliest point at which the RX-Side device could ‘see’ the transition (assuming its actual Logic 0 RX threshold were set to the maximum allowable value of 550mV).

Note also that this test is specific to the device *that is being handed control of the Link*. For Slave DUTs (e.g., displays), the measurement can be performed by initiating a single Turnaround operation from the Master device. For Master DUTs (e.g., host processors), the Link must first be turned around once (putting the Slave device in control). Then, a second Turnaround operation must be performed to transfer control back to the Master, where the measurement is made while the Master is acting as the RX-Side device.

The specification states that  $T_{TA-SURE}$  must be between  $1*T_{LPX}$  and  $2*T_{LPX}$  ns in order to be considered conformant [1], where  $T_{LPX}$  is the average LP state duration of the DUT. (Note that for Master DUT’s, this should be the  $T_{LPX}$  result measured in Test 1.3.1. However, in cases where Test 1.3.1 is not performed (e.g., for a Display (Slave) DUT),  $T_{LPX}$  can be measured from the LP states of the Turnaround sequence itself, during the states where the DUT is operating as the TX-Side device.)

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**Test Setup:** See Appendix B.1.3.

**Test Procedure:**

- Connect the DUT to the Test Setup.
- Create an event that causes the Master to initiate a Turnaround sequence.
- If the DUT is a Slave device, capture the Turnaround sequence on the DSO, and measure  $T_{TA-SURE}$  for the Slave device, as described above. (Otherwise continue to next step.)
- If the DUT is a Master device, the Slave should eventually initiate another Turnaround sequence on its own, to return control back to the Master. Capture this second Turnaround sequence on the DSO, and measure  $T_{TA-SURE}$  for the Master device, as described above.

**Observable Results:**

- Verify that the  $T_{TA-SURE}$  interval is between  $1*T_{LPX}$  and  $2*T_{LPX}$  ns.

**Possible Problems:**

See Possible Problems comments for Test 1.6.4, regarding improving the visibility of the drive overlap period. The same comments apply to this test.

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**Test 1.6.6 – BTA: RX-Side  $T_{TA-GET}$  Interval Value**

**Purpose:** To verify that the DUT drives the Bridge state (LP-00) for the required period ( $T_{TA-GET}$ ), when receiving control of the link during a Link Turnaround procedure.

**References:**

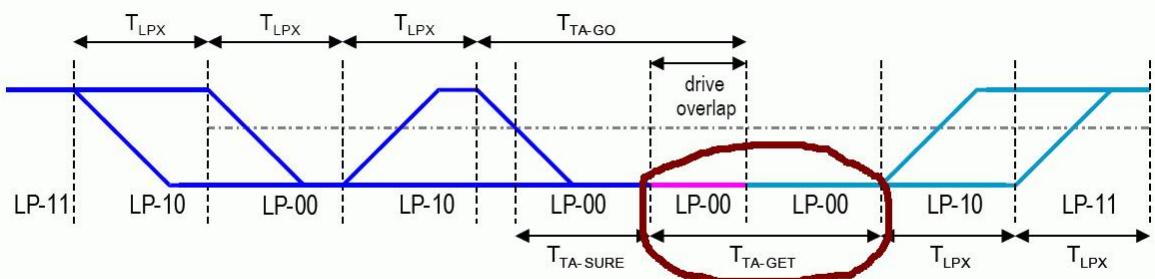
[1] D-PHY Specification, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.

**Last Modification:** November 30, 2009

**Discussion:**

The Link Turnaround process consists of a LP handshake/handoff procedure between the Master and Slave sides of the Link. (Note that ‘Master’ is defined as the device that supplies the HS Clock.) The controlling (‘TX-Side’) device initiates the handoff process by signaling Stop/LP-Rqst/Bridge/LP-Rqst/Stop (LP-11/10/00/10/00). The receiving (‘RX-Side’) device then assumes control of the link, simultaneously driving the Bridge state (LP-00), followed by its own LP-Rqst and Stop (LP-10/11), after which the transfer process is considered complete. A picture of the entire Turnaround procedure (reproduced from Figure 16 of the D-PHY Specification), showing the  $T_{TA-GET}$  interval, is shown below:



**Figure 16 Turnaround Procedure**

**Figure 1.6.6-1:  $T_{TA-GET}$  Interval**

The specification defines  $T_{TA-GET}$  as the, “*Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.*” [1]. Therefore, the  $T_{TA-GET}$  period begins at the point where the RX-Side device begins simultaneous driving of the LP-00 state (i.e., the ‘drive overlap’ period, above), and ends at the end of the LP-00 state (or more accurately, the beginning of the LP-10 state, which begins where the  $V_{DP}$  signal crosses  $V_{IH,MIN}$  (880mV)). (Note that this point is not accurately drawn in the figure above.)

Note also that this test is specific to the device *that is being handed control of the Link*. For Slave DUTs (e.g., displays), the measurement can be performed by initiating a single Turnaround operation from the Master device. For Master DUTs (e.g., host processors), the Link must first be turned around once (putting the Slave device in control). Then, a second Turnaround operation must be performed to transfer control back to the Master, where the measurement is made while the Master is acting as the RX-Side device.

The specification states that  $T_{TA-GET}$  must be greater than  $5*T_{LPX}$  ns in order to be considered conformant [1], where  $T_{LPX}$  is the average LP state duration of the DUT. (Note that for Master DUT’s, this should be the  $T_{LPX}$  result measured in Test 1.3.1. However, in cases where Test 1.3.1 is not performed (e.g., for a Display (Slave) DUT),  $T_{LPX}$  can be measured from the LP states of the Turnaround sequence itself, during the states where the DUT is operating as the TX-Side device.)

**Test Setup:** See Appendix B.1.3.

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**Test Procedure:**

- Connect the DUT to the Test Setup.
- Create an event that causes the Master to initiate a Turnaround sequence.
- If the DUT is a Slave device, capture the Turnaround sequence on the DSO, and measure  $T_{TA-GET}$  for the Slave device, as described above. (Otherwise continue to next step.)
- If the DUT is a Master device, the Slave should eventually initiate another Turnaround sequence on its own, to return control back to the Master. Capture this second Turnaround sequence on the DSO, and measure  $T_{TA-GET}$  for the Master device, as described above.

**Observable Results:**

- Verify that the  $T_{TA-GET}$  interval is greater than or equal to  $5*T_{LPX}$  ns.

**Possible Problems:**

See Possible Problems comments for Test 1.6.4, regarding improving the visibility of the drive overlap period. The same comments apply to this test.

## **SECTION 2: RX TIMERS AND ELECTRICAL TOLERANCES**

### **Overview:**

This section of tests verifies various RX signaling voltage and timing requirements of D-PHY transceivers, defined in the D-PHY Specification.

Group 1 verifies LP-RX voltage and timing requirements.

Group 2 verifies LP-RX behavioral requirements.

Group 3 verifies HS-RX signaling requirements.

Group 4 verifies HS-RX timer requirements.

Comments and questions regarding the documentation and/or implementation of these tests are welcome, and may be sent to [aab@iol.unh.edu](mailto:aab@iol.unh.edu).

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## **GROUP 1: LP-RX VOLTAGE AND TIMING REQUIREMENTS**

**Overview:**

This group of tests verifies the LP-RX voltage and timing electrical requirements defined in Section 8.2.2 of the D-PHY Specification.

**Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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**Test 2.1.1 – LP-RX Logic 1 Input Voltage ( $V_{IH}$ )**

**Purpose:** To verify that the DUT's LP receiver can properly detect Logic 1 voltage levels as low as the minimum required conformance limit ( $V_{IH}$ ).

**References:**

- [1] D-PHY Specification, Section 8.2.2, Line 1494
- [2] Ibid, Section 8.2.2, Table 22

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{IH}$ , or LP-RX Logic 1 Input Voltage.

The specification states, “*The input high-level voltage,  $V_{IH}$ , is the voltage at which the receiver is required to detect a high state in the input signal.*”[1]

The test pattern used for this measurement will be based on the Generic Receiver Test Sequence Template (see Appendix C of this document), which will be used to construct a valid test sequence specific to the DUT. (Note that this test sequence must be created for the DUT prior to performing this test, according to the specific configuration and image data/timing requirements for the DUT. See Appendix C for full details.) This test sequence contains multiple initialization and configuration sections, followed by a repeating image data sequence. For this test, the LP-11 levels for all sections will be set to a nominal value (1.2V), and the sequence will be sent to the DUT. Once the DUT has been verified to be receiving the continuously looping image data sequence properly, the LP-11 voltage level for all Lanes will be decreased simultaneously until the DUT begins to show errors.

Note that the specific observable for this test will vary depending on the DUT type and supported capabilities. An example of an observable behavior for a “bare phy” implementation would be the probing of an internal (or PPI-side) LP data signal using a DSO or Logic Analyzer, and verifying that the received data matches the test pattern data. An example for an integrated CSI-2 or DSI receiver would be to monitor the DUT’s reception of the data via internal error detection capabilities (e.g., CRC counters). For cases where CRC error detection is not available, visual verification of the image itself may be used as the observable (e.g., viewing the image output of an LCD display.) Note that a full discussion of the various options for RX test observables is presented in Appendix G of this document.

The lowest voltage at which the DUT consistently detects LP Logic 1 levels correctly (i.e., receives the image data without error) shall be recorded as the LP-RX Logic-1 Detection Threshold. This value will be varied and measured simultaneously for Dp and Dn of all Clock and Data Lanes.

The DUT’s LP-RX Logic-1 Detection Threshold must be less than or equal to 880mV in order to satisfy the conformance requirements for  $V_{IH}$  [2]. This demonstrates that the DUT can detect logic levels at least as low as 880mV, which is the minimum voltage level a receiver is required to detect as a Logic 1.

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to generate a suitable master test sequence with voltage levels  $V_{OH} = 1.2V$ , and  $V_{OL} = 0V$  on both the Dp and Dn Lines of all Data Lanes.
- Transmit the test sequence to the DUT.
- Verify via any valid observable that the DUT received the image data without errors.
- While the DUT is receiving the continuously looping image data sequence, slowly decreasing the Test System’s  $V_{OH}$  level for Dp and Dn of all Lanes until the DUT indicates errors in the received data.

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- Record the  $V_{IH}$  result for this test case as the lowest Test System  $V_{OH}$  value at which the DUT consistently received the test sequence without errors.

**Observable Results:**

- Verify that  $V_{IH}$  is less than or equal to 880mV.

**Possible Problems:** None.

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**Test 2.1.2 – LP-RX Logic 0 Input Voltage, Non-ULP State ( $V_{IL}$ )**

**Purpose:** To verify that the DUT's LP receiver can correctly detect Logic 0 voltage levels as high as the maximum required conformance limit ( $V_{IL}$ ), when in the non-ULP state.

**References:**

- [1] D-PHY Specification, Section 8.2.2, Line 1490
- [2] Ibid, Section 8.2.2, Table 22

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{IL}$ , or LP-RX Logic 0 Input Voltage.

The specification states, “*The input low-level voltage,  $V_{IL}$ , is the voltage at which the receiver is required to detect a low state in the input signal.*”[1] (Note a different and lower input voltage,  $V_{IL-ULPS}$ , may be used when the receiver is in the ULP state. See Test 2.1.3).

The procedure for this test is similar to the one used for the LP-RX Logic 1 Input Voltage test (see Test 2.1.1), except that the Logic 1 level ( $V_{OH}$ ) of the test stimulus signal will be held fixed for this test, while the Logic 0 level ( $V_{OL}$ ) is slowly increased from a starting value of 0V, to find the point where the DUT no longer consistently detects a Logic 0 correctly. The DUT will not be in ULPS mode when the test stimulus is applied. The maximum voltage level at which the DUT consistently detects all LP Logic 0 levels correctly shall be recorded as the  $V_{IL}$  result. This value will be measured simultaneously for the Dp and Dn lines of all Clock and Data Lanes.

(Note that the exact stimulus pattern and observable mechanism for this test will depend heavily on the DUT type, and the optimal stimulus/observables must be determined in advance for a given DUT before the test can be performed. See Discussion section of Test 2.1.1, and also Appendices C and G for more details.)

For each test case, the measured  $V_{IL}$  result must be greater than or equal to 550mV in order to satisfy the conformance requirements for  $V_{IL}$ , as this demonstrates that the DUT can detect logic 0 levels up to at least 550mV, which is the maximum voltage level a receiver is required to detect as a Logic 0, when *not* in the ULP state. [2]

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to generate a suitable test sequence with LP voltage levels  $V_{OH} = 1.2V$ , and  $V_{OL} = 0V$  on all Clock and Data Lanes.
- Transmit the test sequence to the DUT.
- Verify that the DUT received the test sequence without errors.
- Repeat the previous three steps, slowly increasing the Test System's  $V_{OL}$  level for Dp and Dn of all Clock and Data Lanes for each iteration until the DUT indicates errors.
- Record the  $V_{IL}$  result for this test case as the highest  $V_{OL}$  value at which the DUT consistently received the test sequence without errors.

**Observable Results:**

- Verify that  $V_{IL}$  is greater than or equal to 550mV.

**Possible Problems:**

In some cases for devices with multiple Data Lanes, the procedure described above may not easily be applied to Data Lanes 1, 2, and 3 in the same manner as Data Lane 0. For example, DSI devices only transmit and

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receive LPDT-encoded DSI/DCS commands on Data Lane 0. Data Lanes 1, 2, and 3 are required by the D-PHY spec to support “Escape Mode for ULPS and Triggers in the forward direction”, however DSI modifies this requirement by preventing any reason to send a Trigger on anything but Data Lane 0. All Data Lanes should still support ULPS, however using this as the basis for this test is non-trivial. In these cases it may not be possible to perform this test in a manner that exercises any Lanes other than Data Lane 0.

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**Test 2.1.3 – LP-RX Logic 0 Input Voltage, ULP State ( $V_{IL-ULPS}$ )**

**Purpose:** To verify that the DUT's LP receiver can detect Logic 0 voltage levels as high as the maximum required conformance limit ( $V_{IL-ULPS}$ ), when in the ULP state.

**References:**

- [1] D-PHY Specification, Section 8.2.2, Line 1490
- [2] Ibid, Section 8.2.2, Table 22

**Resource Requirements:** See Appendix A.2.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{IL-ULPS}$ , which is the LP-RX Logic 0 Input Voltage during ULPS. This is the voltage at which the receiver is required to detect a low state in the input signal, when in the ULP state.

The specification states, “*The input low-level voltage,  $V_{IL}$ , is the voltage at which the receiver is required to detect a low state in the input signal. A lower input voltage,  $V_{IL-ULPS}$ , may be used when the receiver is in the Ultra-Low Power State.*”[1] (Note the non-ULPS  $V_{IL}$  case was tested in the previous test, see Test 2.1.2).

The procedure for this test is similar to that used in the previous test, except that the DUT will be placed into the ULPS state as part of the test sequence, by sending a properly formed ULPS entry sequence at nominal LP voltage levels ( $V_{OL} = 0V$ ,  $V_{OH} = 1.2V$ ). (Note this must be done differently for Clock and Data Lanes, as the Clock Lane ULPS entry sequence is a different pattern from the Data Lane case.)

Note that the exact stimulus sequence used for this test will consist of a ULPS Entry sequence, followed by a ULPS Exit sequence (Mark-1 for 1ms followed by Stop), and then any valid HS burst sequence that produces an observable result.

(Note that the exact HS pattern and observable mechanism for this test will depend on the DUT type, and the proper stimulus/observable must be determined in advance for a given DUT before the test can be performed. See Discussion section of Test 2.1.1, and also Appendices C and G for more details.)

The methodology behind this test is based on the fact that the maximum LP-0 voltage that a receiver is *required* to detect as Logic 0 during ULPS is *lower* than the value required during normal operation. For a given DUT, the maximum detectable LP-0 voltage when *not* in ULPS was determined in Test 2.1.2. If a test sequence consisting of a ULPS Entry and Exit sequence followed by a valid HS burst is sent to the DUT using a the maximum detected LP-0 level determined in Test 2.1.2, the DUT should *not* successfully receive the HS burst, if uses a lower  $V_{IL}$  threshold during ULPS than during normal operation. The DUT will continue to *not* receive the HS burst until the LP-0 level is decreased to the maximum value that the DUT will detect during ULPS, as it is at this point that the DUT will properly detect the Mark-1/Stop ULPS Exit, and will exit ULPS in time to successfully receive the HS data burst.

For this test, a slightly different version of the procedure described above will be used, where the test sequence will initially be sent starting at a nominal LP-0 level of 0V (which should result in the DUT successfully receiving the HS burst). The LP-0 voltage will then be increased until the DUT no longer detects the ULPS Exit Mark-1/Stop, and thus does not receive the HS burst.

If the  $V_{OL}$  value where the DUT fails to receive the HS burst is greater than or equal to 300mV, then the DUT satisfies the conformance requirements for  $V_{IL-ULPS}$ , as it has demonstrated that it can properly detect Logic 0 for levels at and below 300mV, which is the maximum voltage level a receiver is *required* to detect as a Logic 0, when in the ULP state. [2]

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**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to generate a ULPS Entry sequence followed by a valid Mark-1/Stop plus valid HS burst data on all Lanes, using nominal LP voltage levels (LP-0 = 0V, and LP-1 = 1.2V) on both the Dp and Dn Lines of all Clock and Data Lanes.
- Transmit the test sequence to the DUT.
- Verify that the DUT received the HS burst data without errors.
- Repeat the previous two steps, slowly increasing the Test System's LP-0 voltage level for Dp and Dn of all Clock and Data Lanes simultaneously for each iteration until the DUT indicates errors in the received HS data.
- Record the  $V_{IL-ULPS}$  result for this test case as the highest LP-0 voltage level for which the DUT consistently received the test sequence without errors.

**Observable Results:**

- Verify that  $V_{IL-ULPS}$  is greater than or equal to 300mV.

**Possible Problems:**

See comments in Possible Problems section for Test 2.1.2, which are also applicable to this test.

Also, for some PPI-based ‘bare-phy’ DUTs, use of the HS Burst data as the observable may not be a valid methodology, as the DUT may present the received HS data at the protocol interface pins regardless of the LP voltage detected during the ULPS Exit sequence. These types of devices rely on the protocol logic to determine whether the HS data should be considered valid, by indicating the phy’s ULPS state to the protocol via dedicated signals at the PPI, and letting the protocol determine whether or not the proper ULPS Exit sequence was received prior the HS data. In these cases, the PPI signals that indicate the ULPS state to the protocol layer may be used as the observable, as these lines will directly indicate the ULPS state of the phy.

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**Test 2.1.4 – LP-RX Input Hysteresis ( $V_{HYST}$ )**

**Purpose:** To verify that the Input Hysteresis value ( $V_{HYST}$ ) of the DUT's LP receiver is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.2.2, Line 1494
- [2] Ibid, Section 8.2.2, Table 22

**Resource Requirements:** See Appendix A.2.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{HYST}$ , or Input Hysteresis. The Hysteresis is incorporated into LP receivers to reduce sensitivity to noise, and prevents Logic state changes due to short-term, low amplitude excursions below the  $V_{IH}$  Logic-1 threshold (or above  $V_{IL}$  Logic-0 threshold), after the instantaneous voltage has initially crossed the threshold for any given bit interval.

The specification states, “*The input high-level voltage,  $V_{IH}$ , is the voltage at which the receiver is required to detect a high state in the input signal. In order to reduce noise sensitivity on the received signal, an LP receiver shall incorporate a hysteresis. The hysteresis voltage is defined as  $V_{HYST}$ .*”[1]

Note that multiple possible methodologies exist for performing this test, depending on the observability and access provided by the DUT to internal state signals for the LP logic levels. This typically will depend heavily on the DUT type, however if the DUT provides suitable access to the proper internal monitoring capability, the test setup and procedure can be greatly simplified. If the DUT does not provide access to this capability, it may still be possible to perform the test using an alternate methodology, which requires a more complex test setup.

For the purposes of this test suite, two different methodologies will be defined, which will be referred to as the Static method, and the Dynamic method. The preferred (and simpler) approach is the Static method, however this approach requires the DUT to provide a proprietary means to instantaneously monitor the internal detected LP logic level for a given line (either physically via a dedicated signal pin, or through software, by monitoring a register or other status indicator in real-time). Dedicated signal pins are almost always available for PPI-based DUT's, or DUTs that have any sort of hardware debug bus capability whereby the internal LP logic state of any given line may be directly monitored using an oscilloscope that is physically connected to the logic signal pin. Host implementations are frequently capable of providing internal LP state monitoring capability via software-driven means.

**Static Method:**

In the Static approach, the voltage of a static LP level presented at the D-PHY LP-RX input pins of the DUT can be set to a nominal LP-0 or LP-1 level (0mV or 1200mV, depending on whether the hysteresis of the  $V_{IH}$  or  $V_{IL}$  threshold is being measured, respectively.) (Note for this example, verification of the Dp  $V_{IH}$  hysteresis will be described, thus the initial applied static LP level will be set to 0mV.) With the applied static voltage set to 0mV, it will then be slowly increased in order to determine the point where the internal LP logic state signal (monitored separately) indicates a change to the opposite LP state (LP-1, in this case). The applied LP voltage that causes this state change will be recorded as  $V_A$ , and the applied LP voltage will be increased approximately another 50-100mV beyond this point. With the internal LP state now indicating LP-1, the applied LP voltage will then be slowly varied back in the opposite direction, to see if the internal LP logic level maintains its state as the applied voltage crosses back below  $V_A$ . At some point less than  $V_A$ , the internal LP logic state will indicate a change back to LP-0, for which the applied voltage will be recorded as  $V_B$ .  $V_{HYST}$  for the  $V_{IH}$  threshold of the Dp line will be mathematically computed and reported as  $V_{HYST-VIH}(Dp) = |V_A - V_B|$ .

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The entire procedure above will then be repeated to measure  $V_{HYST}$  for the Dp  $V_{IL}$  threshold (i.e.,  $V_{HYST-VIL}(Dp)$ ), and then two additional times for the Dn line to get  $V_{HYST-VIH}(Dn)$ , and  $V_{HYST-VIL}(Dn)$ . For all four cases,  $V_{HYST}$  must be  $\geq 25mV$  in order to be considered conformant [2].

*Dynamic Method:*

For cases where the DUT does not provide access to any kind of internal LP logic state monitoring capability (which is typically the case for DSI receivers, e.g., LCD display panels), it may be possible to employ a different methodology to measure  $V_{HYST}$ . This approach uses a simulated noise signal, which is applied additively by the Test System to either the Dp or Dn signal while the Test System is configured to transmit a valid LP sequence that causes an observable result. However in this case the LP-1 and LP-0 levels of the Test System will be set to the minimum/maximum  $V_{IH}/V_{IL}$  values measured for the DUT in Tests 2.1.1 and 2.1.2, respectively. Once the DUT is verified to successfully receive the test sequence without error under these conditions, the additive simulated noise signal will be turned on for either the Dp or Dn line, and the DUT will be observed to determine whether or not it is still able to successfully receive the test sequence in the presence of the additive noise, which is calibrated to cause momentary excursions of approximately 25mV below/above the  $V_{IH}/V_{IL}$  thresholds, respectively. If the DUT does not implement some form of hysteresis on its LP-RX in this case, the presence of the additive noise should cause errors in the received data.

The additive noise signal must be injected into either the Dp or Dn line using a similar test setup to that used for the LP-RX Interference Tolerance test (Test 2.1.7), except that for that test, the interference was added common-mode, i.e., to both Dp and Dn simultaneously. For this test, the simulated noise must be added single-endedly to either Dp or Dn (depending on which line is being tested), otherwise it would be treated as common-mode noise by the LP-RX, and will potentially be filtered out. This filtering should not occur however, if the noise is applied single-endedly.

The recommended characteristics for the additive noise signal is to use a square-wave signal with a period what is approximately 2.3x the  $T_{LPX}$  value of the applied test sequence. This will modulate the phase of the additive noise with respect to the LP data test sequence, for added impact. The amplitude of the additive noise should be calibrated to produce an approximately 25mVpk (50mVpp) deviation from the nominal LP-0/1 levels of the Test System (which will be set to the measured  $V_{IH}$  and  $V_{IL}$  values for the DUT). When the additive noise is enabled, the DUT should still be able to successfully receive the LP test sequence without error, if it employs sufficient hysteresis on its LP-RX.

Note that when the test is performed, the amplitude of the additive noise can be increased to find the actual  $V_{HYST}$  value (i.e., by increasing to the point where the DUT starts to indicate errors, and measuring the peak magnitude of the applied additive noise at the DUT receiver as  $V_{HYST}$ ). However, note that one limitation to this approach is that typically it may not be possible to measure  $V_{HYST}$  for  $V_{IH}$  and  $V_{IL}$  separately, unless the additive noise can be applied selectively to only to the LP-1 or LP-0 states (which would require suitably capable signal generation equipment). Otherwise the measurement will produce a single common  $V_{HYST}$  result for both  $V_{IH}$  and  $V_{IL}$ .

Regardless of the methodology used, the measured  $V_{HYST}$  values for Dp and Dn of all measured Lanes must be greater than 25mV in order to be considered conformant [2].

**Test Setup:** See Appendix B.2.

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**Test Procedure (Option 1: Static Method):**

- Connect the DUT to the Test System.
- Configure the Test System to generate static LP-0 levels with  $V_{OL} = 0\text{mV}$  for both the Dp and Dn lines of Data Lane 0.
- Using the DUT's proprietary capability, monitor the DUT's internal detected LP logic states for the Dp and Dn lines, and verify that they are both reported as LP-0.
- Slowly increase the  $V_{OL}$  level of the Test System to the point where the DUT's reported internal LP logic states change from LP-0 to LP-1 for both Dp and Dn, and record the voltages as  $V_A(Dp)$  and  $V_A(Dn)$ . (Note: This point should be consistent with the  $V_{IH}$  value that was measured in Test 2.1.1.) The values should be measured and recorded separately for Dp and Dn, however the values should typically be nearly identical.
- Continue to increase the Test System's  $V_{OL}$  (now  $V_{OH}$ ) value to approximately 100mV beyond  $V_A$ . Then begin slowly decreasing the  $V_{OH}$  level, while still monitoring the reported internal LP logic state (which should still be reported as LP-1 for both Dp and Dn).
- Continue decreasing  $V_{OH}$  until the reported internal LP logic states for Dp and Dn change from LP-1 to LP-0. Record these voltages as  $V_B(Dp)$  and  $V_B(Dn)$ .
- Compute the  $V_{IH}$  hysteresis for the Dp line as  $V_{HYST-VIH}(Dp) = V_A(Dp) - V_B(Dp)$ .
- Compute the  $V_{IH}$  hysteresis for the Dn line as  $V_{HYST-VIH}(Dn) = V_A(Dn) - V_B(Dn)$ .
- Repeat the above procedure a second time (but starting from a nominal LP-1 level of 1200mV, and working downward) to measure the  $V_{IL}$  hysteresis for Dp and Dn, i.e.,  $V_{HYST-VIL}(Dp)$ , and  $V_{HYST-VIL}(Dn)$ . (Note however in this case  $V_{HYST}$  will be computed as  $|V_A - V_B|$ .)
- Repeat all of the above steps for all Clock and Data Lanes.

**Test Procedure (Option 2: Dynamic Method):**

- Connect the DUT to the Test System.
- Configure the Test System to generate a suitable LP sequence that produces an observable result (e.g., a LPDT command or image data sequence on Data Lane 0), and configure the Test System's  $V_{OH}$  and  $V_{OL}$  levels for all Lanes to the  $V_{IH}$  and  $V_{IL}$  values that were measured in Tests 2.1.1 and 2.1.2, respectively.
- With the additive noise source disabled, transmit the test sequence the DUT, and verify (via the appropriate observable) that the test sequence was received without error.
- Repeat the previous step, but with the additive noise source enabled for the Dp line, using a noise voltage of approximately 5mVpk. Verify again that the test sequence was received without error.
- Repeat the previous step multiple times, slowly increasing the additive noise voltage in 3-5mV steps, until the point is reached where the DUT begins to report errors in the received test sequence.
- Record  $V_{HYST-VIH}(Dp)$  and  $V_{HYST-VIL}(Dp)$  as the maximum additive noise voltage where the test sequence was consistently received without error.
- Repeat the above procedure for the Dn line to determine  $V_{HYST-VIH}(Dn)$  and  $V_{HYST-VIL}(Dn)$ .

**Observable Results:**

For all measured Lanes:

- Verify that  $V_{HYST-VIH}(Dp)$  is greater than or equal to 25mV.
- Verify that  $V_{HYST-VIH}(Dn)$  is greater than or equal to 25mV.
- Verify that  $V_{HYST-VIL}(Dp)$  is greater than or equal to 25mV.
- Verify that  $V_{HYST-VIL}(Dn)$  is greater than or equal to 25mV.

**Possible Problems:** None.

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**Test 2.1.5 – LP-RX Minimum Pulse Width Response ( $T_{MIN-RX}$ )**

**Purpose:** To verify that the DUT's LP receiver can detect LP pulses with the minimum required duration.

**References:**

- [1] D-PHY Specification, Section 8.2.2, Line 1497
- [2] Ibid, Section 5.9, Table 14
- [3] Ibid, Section 8.2.2, Table 23

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $T_{MIN-RX}$ , which defines the minimum-duration LP pulse width that should still be detected as a valid LP state by an LP receiver.

The specification states, “*Signal pulses wider than  $T_{MIN-RX}$  shall propagate through the LP receiver.*”[1]. The specification also provides a graphic (reproduced below), which shows the  $T_{MIN-RX}$  interval in relation to 2X the  $T_{LPX}$  specification (where  $T_{LPX}$  defines the minimum LP pulse width requirement for LP transmitters, i.e., the narrowest pulse one could expect to see out of any conformant LP-TX.)

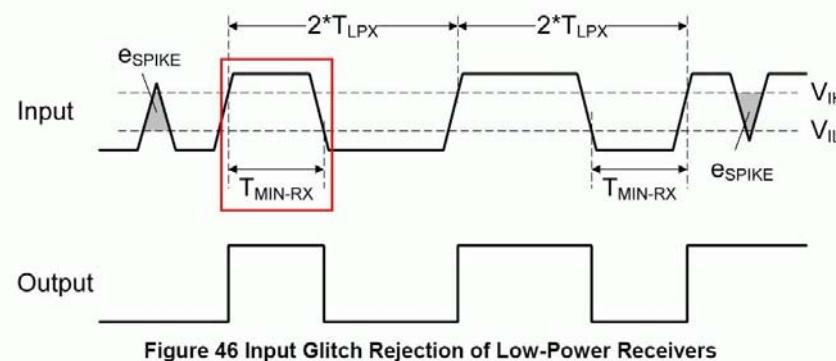


Figure 46 Input Glitch Rejection of Low-Power Receivers

Figure 2.1.5-1:  $T_{MIN-RX}$  Interval

Note that the above picture can be misleading if not interpreted carefully, as it is not exactly drawn to scale. The minimum  $T_{LPX}$  value for LP transmitters is 50ns[2], so twice this value would be 100ns. The minimum  $T_{MIN-RX}$  value is specified to be 20ns[3], whereas in the example picture shown in the spec, the example  $T_{MIN-RX}$  pulse appears more on the order of 1.0\* $T_{LPX}$ , not 0.4\* $T_{LPX}$ . In any case, a conformant LP-RX should be able to detect LP states with durations as short as 20ns[3].

In this test, the DUT's LP-RX will be sent valid LP sequences with states as short as 20ns. The DUT must successfully detect states as short as 20ns in order to be considered conformant.

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to generate a suitable LP test pattern with voltage levels  $V_{OH} = 1.2V$ , and  $V_{OL} = 0V$  on both the Dp and Dn Lines, and with  $T_{LPX} = 50ns$ , on Data Lane 0.
- Transmit the test sequence to the DUT.
- Verify via any valid observable that the DUT received the test sequence without errors.

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- Repeat the previous three steps, slowly decreasing  $T_{LPX}$  for the LP states in the test sequence, until the DUT indicates errors in the received data.
- Record the smallest  $T_{LPX}$  value at which the DUT consistently received the test sequence without errors.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes), and also the Clock Lane.

**Observable Results:**

- Verify that the smallest  $T_{LPX}$  value for which the DUT can consistently receive the test sequence without errors is less than or equal to 20ns.

**Possible Problems:** None.

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**Test 2.1.6 – LP-RX Input Pulse Rejection ( $e_{SPIKE}$ )**

**Purpose:** To verify that the DUT's LP receiver rejects short-term signal glitches that are smaller than the specified conformance limit.

**References:**

- [1] D-PHY Specification, Section 8.2.2, Line 1497
- [2] Ibid, Section 8.2.2, Line 1508
- [3] Ibid, Section 8.2.2, Table 22

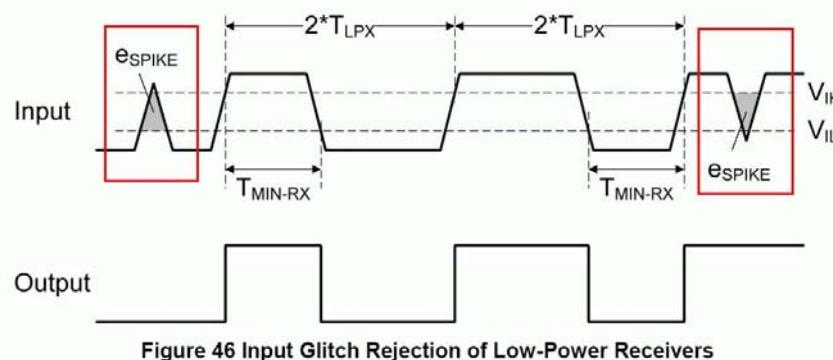
**Resource Requirements:** See Appendix A.2.

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $e_{SPIKE}$ , which describes an LP receiver's ability to reject short-term glitches, i.e., narrow pulses with voltage levels outside of the current Logic state, but that should not change the receiver state, as their widths are sufficiently shorter than the nominal  $T_{LPX}$  interval.

The specification states, “*The LP receiver shall reject any input signal smaller than  $e_{SPIKE}$ .*”[1], and defines  $e_{SPIKE}$  as the, “*Time-voltage integration of a spike above  $V_{IL}$  when being in LP-0 state or below  $V_{IH}$  when being in LP-1.*”[2]. The conformance limit for  $e_{SPIKE}$  is defined in units of Volts times picoseconds, (V\*ps)[3], which allows for multiple potential test cases (high voltage/short-duration, vs. low voltage/long duration).



**Figure 2.1.6-1: Example  $e_{SPIKE}$  Glitch**

The general methodology for this test is similar to other LP-RX tests (e.g., send valid sequence with proper/nominal LP voltage/timing characteristics, then modify sequence to introduce test artifact.) Again there are multiple options for stimulus and observable, however it is beneficial to try to identify, when possible, a sufficiently low-level mechanism that can be used with the widest variety of DUT types, and ideally for both Clock and Data Lanes.

For this test, one such possible mechanism could be the HS-entry sequence, which is common to all Data Lanes (and also technically the Clock Lane as well.) A proper HS entry sequence consists of LP-11, followed by LP-01 (HS-Rqst) for at least  $T_{LPX}$ , then HS-00 (Bridge) for time THS-PREPARE. One possible option for this test would be to introduce a spike during the LP-01 state, in such a way that it would disrupt RX behavior if seen as a valid level/state change by the DUT. Note this must be done with care, and with an awareness of the  $T_{MIN-RX}$  and  $T_{LPX}$  requirements for devices, as the three concepts are interrelated to some degree, with respect to the particular choice of stimulus sequence for this test.

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Generally speaking, the methodology for this test is similar to Test 2.1.5 (LP-RX Minimum Pulse Width Response), with some modifications: The nominal minimum  $T_{LPX}$  value of 50ns will be used for all LP states in the stimulus sequence, and a glitch (of defined duration) will be introduced in the center of all LP states. The approach of adding the glitch to all LP states helps to alleviate potential problems that could arise by affecting only one state in a sequence, in which case the effects of how logical state machines will be affected by the erroneous reception of just one state.

Also, for this test, care must be given to the particular LP voltage levels used for the test. The test will be performed once using nominal LP levels ( $V_{OH} = 1.2V$ , and  $V_{OL} = 0V$ ), and then repeated using worst-case LP levels ( $V_{IH} = 880mV$ , and  $V_{IL} = 550V$ ). Note that the width of the glitch in both cases however is not the same, as the glitch is defined in units of Volts *times* Picoseconds, in terms of time spent *below*  $V_{IH}$  (when in LP-1), and *above*  $V_{IL}$  (when in LP-0). Various cases for the different  $V_{OH}$  and  $V_{OL}$  levels are worked out below.

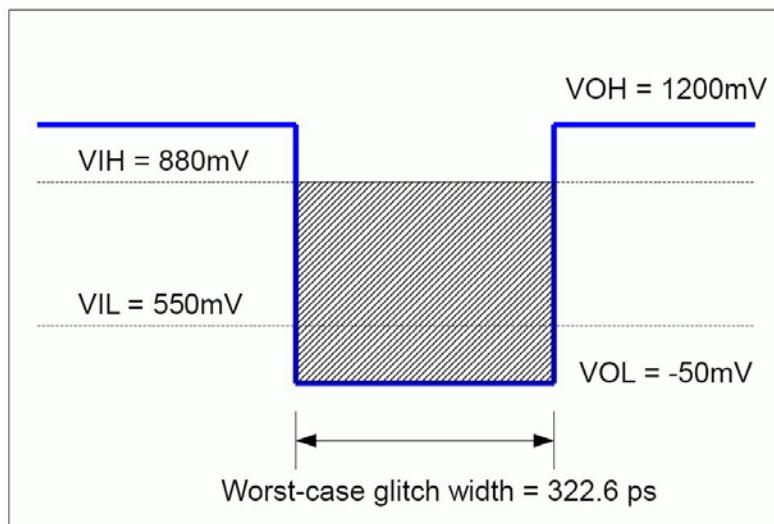
Note for the purposes of this test,  $V_{IH}$  will be taken as  $V_{IH,MIN} = 880mV$ , and  $V_{IL}$  will be taken as  $V_{IL,MAX} = 550mV$ , and for all test cases the magnitude of all glitches will traverse to the opposite LP voltage level. This means a worst-case ‘negative’ glitch while in the LP-1 state would mean dipping below 880mV, down to the whatever  $V_{OL}$  value the Test System is using. The duration of the worst-case glitch will depend on the  $V_{OL}$  value selected. In this test, separate cases will be tested for both the maximum depth/minimum duration, and the minimum depth/maximum duration.

Max Depth / Min Duration Cases:

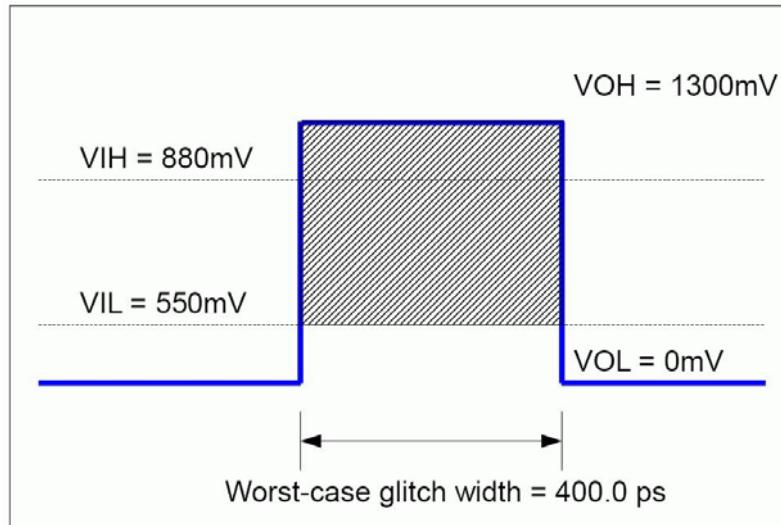
- Negative glitch (880 to -50mV): Min duration is  $300/(880 - -50mV) = 322.6 \text{ ps}$   
Positive glitch (550 to 1300mV): Min duration is  $300/(1300-550mV) = 400 \text{ ps}$

Max Duration / Min Depth Cases:

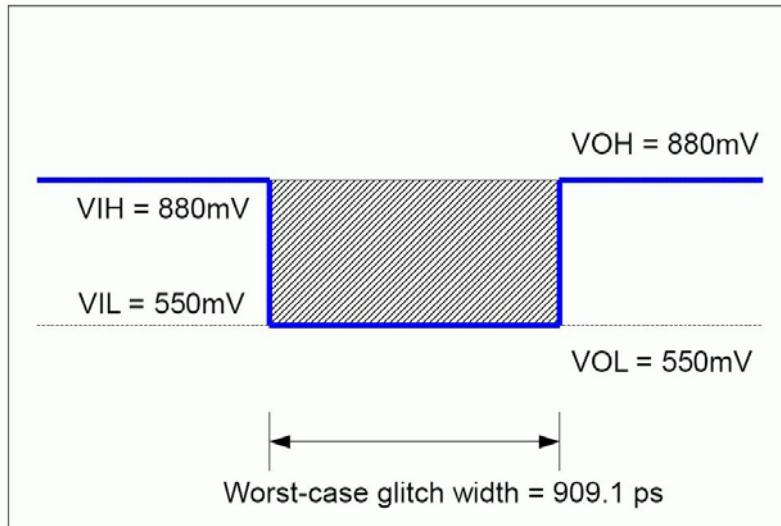
- Negative glitch (880 to 550mV): Min duration is  $300/(880-550) = 909.1 \text{ ps}$   
Positive glitch (550 to 880mV): Min duration is  $300/(880-550) = 909.1 \text{ ps}$



**Figure 2.1.6-2: Max Depth/Min Duration Negative Glitch**



**Figure 2.1.6-3: Max Depth/Min Duration Positive Glitch**



**Figure 2.1.6-4: Min Depth/Max Duration Glitch (Negative)**  
**(Note: Positive Glitch has Same Dimensions)**

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to generate a suitable test pattern with LP voltage levels  $V_{OH} = 1.2\text{V}$ , and  $V_{OL} = 0\text{V}$  on both Dp and Dn of all Clock and Data Lanes, and with glitch addition disabled in the Test System.
- Transmit the test sequence to the DUT.
- Verify via any valid observable that the DUT received the test sequence without errors.
- Reconfigure the Test System to enable the addition of  $300\text{V}\cdot\text{ps}$  LP glitches to all LP states of all Clock and Data Lanes, while still keeping  $V_{OH} = 1.2\text{V}$ , and  $V_{OL} = 0\text{V}$ .
- Transmit the test sequence to the DUT.

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- Verify via any valid observable that the DUT received the test sequence without errors.
- With glitches still enabled, set the Test System's LP levels to  $V_{OH} = 880\text{mV}$ , and  $V_{OL} = 550\text{mV}$ , and adjust the glitch times for the Min Depth/Max Duration values (909.1ps).
- Transmit the test sequence to the DUT.
- Verify via any valid observable that the DUT received the test sequence without errors.

**Observable Results:**

- For all test cases, verify that the DUT receives the LP test sequence without errors.

**Possible Problems:** None.

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**Test 2.1.7 – LP-RX Interference Tolerance ( $V_{INT}$  and  $f_{INT}$ )**

**Purpose:** To verify that the DUT Data Lane LP receiver can tolerate interference with voltage and frequency values within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.2.2, Line 1499
- [2] Ibid, Section 8.2.2, Table 22

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements are specifications for  $V_{INT}$  and  $f_{INT}$ , which together define the voltage and frequency LP-RX interference tolerance requirements (respectively). These requirements describe an LP receiver's ability to reject additive RF disturber signals with frequencies and voltage levels within a given range, such that they do not affect the receiver's ability to properly detect LP-0 and LP-1 states, even at the worst-case LP voltage levels.

The specification states, "*Furthermore, the LP receivers shall be tolerant of super-positioned RF interference on top of the wanted Line signals. This implies an input signal filter. The LP receiver shall meet all specifications for interference with peak amplitude  $V_{INT}$  and frequency  $f_{INT}$ . The interference shall not cause glitches or incorrect operation during signal transitions.*"[1]

This specification implies that an external disturber signal of specified voltage and frequency shall not affect the receiver's ability to detect line states, even in cases where the instantaneous line level with the disturber signal added may cause the voltage to be above/below the  $V_{IL,MAX}/V_{IH,MIN}$  levels, respectively. This implies the presence of some form of filter on the receiver that would effectively remove these disturber signals before the detection circuitry.

Again, the methodology for this test is similar to other LP-RX tests in this section, whereby a nominal LP test sequence is generated for the particular DUT type, and is verified under nominal signal conditions (amplitudes, bit rate, etc). Then, the disturber signal is added to the sequence, and the DUT behavior is observed to verify that the LP-RX can still operate properly in the presence of the interference signal.

The specification defines the maximum peak interference amplitude for  $V_{INT}$  of 200mV, and a minimum interference frequency for  $f_{INT}$  of 450MHz. Note that there is no upper  $f_{INT}$  limit defined however this is likely due to the assumption that the lower bound defines the worst case. Regardless, this test will be performed for several frequencies up to the maximum possible  $f_{MAX}$  value of 1.33GHz.

Note while this test is similar in nature and setup to the HS-RX Common-Mode Interference Tolerance tests of 2.3.6 and 2.3.7, this LP-specific test requires an LP-only sequence to be used as the test stimulus. This is due to the fact that the LP interference amplitude ( $V_{INT}$ ) requirement is larger for LP than it is for HS (200mVpk vs. 100mVpk, respectively). Thus, using an HS burst sequence would overstress the HS-RX requirements (unless there was some way to only apply the disturber signal during the LP states between bursts, which is not possible with most test equipment.) Therefore, any valid LP sequence can be used for Data Lane 0, but for other Lanes, the choices are limited to the ULPS Escape Mode sequence, which has its own practical limitations (see Appendix G.4). Lane remapping (Appendix G.5) may be used in cases where it is available, if the DUT supports this capability.

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.

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- Configure the Test System to generate a suitable LP test pattern with voltage levels  $V_{OH} = 1.2V$ , and  $V_{OL} = 0V$  on both the Dp and Dn Lines of Data Lane 0, and with common-mode RF interference disabled in the Test System.
- Transmit the test sequence to the DUT.
- Verify via any valid observable that the DUT received the test sequence without errors.
- Reconfigure the Test System to enable sinusoidal common-mode RF interference with a peak amplitude of 200mV, and a frequency of 450MHz.
- Transmit the test sequence to the DUT.
- Verify via any valid observable that the DUT received the test sequence without errors.
- Repeat the above steps, increasing the disturber frequency in 10MHz steps, up to a maximum frequency of 1.33GHz. (Note the time spent at each frequency can be minimal, i.e., just long enough to verify that massive failure does not occur.)
- Verify via any valid observable that the DUT received the test sequence without errors.
- Repeat all above steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes), and also the Clock Lane.

**Observable Results:**

- Verify that in all test cases the DUT is able to successfully receive the test sequence in the presence of the interfering signaling.

**Possible Problems:** None.

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**Test 2.1.8 – LP-CD Logic Contention Thresholds ( $V_{IHCD}$  and  $V_{ILCD}$ )**

**Purpose:** To verify that the LP Contention Detector detects the proper high and low contention voltage thresholds.

**References:**

- [1] D-PHY Specification, Section 6.1, Line 1083
- [2] Ibid, Section 8.3, Line 1514
- [3] Ibid, Section 6.1, Line 1095

**Resource Requirements:** See Appendix A.2.

**Last Modification:** September 16, 2010

**Discussion:**

Section 6.1 of the D-PHY specification defines a Contention Detection mechanism, which is used to detect the condition where multiple transmitters attempt to drive a Lane at the same time.

The specification states, “*During normal operation one and only one side of a Link shall drive a Lane at any given time except for certain transition periods. Due to errors or system malfunction a Lane may end up in an undesirable state, where the Lane is driven from two sides or not driven at all. This condition eventually results in a state conflict and is called Contention. All Lane Modules with LP bi-directionality shall include contention detection functions to detect the following contention conditions*”[1].

(Note that the specification states that contention detection functions are only required for devices that support bi-directional operation. Therefore, for DUTs that do not support bi-directional operation, this test is considered Not Applicable.)

The specification further states, “*The Low-Power receiver and a separate Contention Detector (LP-CD) shall be used in a bi-directional Data Lane to monitor the line voltage on each Low-Power signal. This is required to detect line contention as described in section 6.1. The Low-Power receiver shall be used to detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than  $V_{IL}$ . Refer to Table 22. The LP-CD shall be used to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than  $V_{IHCD}$ . Refer to Table 24. An LP low fault shall not be detected when the pin voltage is less than  $V_{ILCD}$ .*”[2].

To break the above paragraph down into its components, there are three behaviors that are specified in this requirement:

- 1) Ensure that an LP-TX detects an LP High Fault when it is transmitting an LP-1 state, and the pin voltage is less than  $V_{IL}$  (550mV).
- 2) Ensure that an LP-TX detects an LP Low Fault when it is transmitting an LP-0 state, and the pin voltage is greater than  $V_{IHCD}$  (min 450mV).
- 3) Ensure that an LP-TX does not detect an LP Low Fault when it is transmitting an LP-0 state, and the pin voltage is less than  $V_{ILCD}$  (max 200mV).

Note that for the first requirement, it is not clear if the specification’s use of the term  $V_{IL}$  is intended to refer to the actual measured  $V_{IL}$  value for the particular DUT, or  $V_{IL,MAX}$ , which is defined as 550mV. However in either case, a test case can be created where the DUT is transmitting LP-1, and a contention event is created that causes the PIN voltage to be 550mV. In this case, all DUTs should detect an LP High Fault (and should also detect an LP High Fault for PIN voltages less than 550mV).

(Note also that for an LP High Fault, there are actually two instances where such an event could occur. One is when both sides of a link are driving opposite LP levels at the same time (LP/LP case). The other instance is when one side tries to drive LP-1 while the other side is driving an HS burst (LP/HS case). For this second case, the specification explicitly states, “*The contention shall be detected at the side that is transmitting the LP-high.*”[3])

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For the second requirement, the intended meaning is such that devices **must** detect an LP Low Fault for all PIN voltages greater than 450mV when the transmitter is driving LP-0. Per the third requirement, all devices must **not** detect an LP Low Fault for all PIN voltages less than 200mV when the transmitter is driving LP-0. For PIN voltages between 200 and 450mV, the DUT **may** detect an LP Low Fault when the transmitter is driving LP-0 (as this is the valid range within which the threshold point is to be set.)

Note also that while the specification is not explicitly clear about the duration of detected contention events, all test cases for this test will ensure that the contention events last for a duration of at least one LP state time (i.e.,  $T_{LPX}$ ).

Also note that because the contention events required for this test will be generated by forcing the Test System to drive a signal simultaneously during an LP transmission from the DUT, the exact voltage levels resulting on the line during the contention cannot be precisely known or calibrated in advance, as they are partially determined by the LP-TX output impedance of the DUT (which will vary for different DUTs). Therefore, in all cases the contention voltage and event must be monitored using an oscilloscope, in order to ensure that the resulting voltage appearing on the line is within the required range for the particular test case.

Also, the observable mechanism for this test will depend on the DUT type. For bi-directional DSI displays, the *Contention Detected* bit (bit 7) of the Error Report packet may be used. For PPI-based DUTs, the ErrContentionLP0 and ErrContentionLP1 PPI signals may be used. Internal vendor-specific error registers may also be used, if available.

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- **Test Case 1a (LP/LP):** Configure the Test System to create a contention event by transmitting an LP-0 while the DUT is transmitting an LP-1 state (on either Dp or Dn) such that the PIN voltage is 550mV during the contention event.
- Determine (via an appropriate observable mechanism) if the DUT detected an LP High Fault.
- **Test Case 1b (LP/HS):** Configure the Test System to create a contention event by transmitting an HS burst while the DUT is transmitting an LP-1 state (on either Dp or Dn) such that the PIN voltage is less than 550mV during the contention event.
- Determine (via an appropriate observable mechanism) if the DUT detected an LP High Fault.
- **Test Case 2:** Configure the Test System to create a contention event while the DUT is transmitting an LP-0 state (on either Dp or Dn) such that the PIN voltage is 450mV during the contention event.
- Determine (via an appropriate observable mechanism) if the DUT detected an LP Low Fault.
- **Test Case 3:** Configure the Test System to create a contention event while the DUT is transmitting an LP-0 state (on either Dp or Dn) such that the PIN voltage is 200mV during the contention event.
- Determine (via an appropriate observable mechanism) if the DUT detected an LP Low Fault.

**Observable Results:**

- For Test Case 1a, verify that the DUT **does** detect an LP High Fault.
- For Test Case 1b, verify that the DUT **does** detect an LP High Fault.
- For Test Case 2, verify that the DUT **does** detect an LP Low Fault.
- For Test Case 3, verify that the DUT **does not** detect an LP Low Fault.

**Possible Problems:** None.

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## **GROUP 2: LP-RX BEHAVIORAL REQUIREMENTS**

**Overview:**

This group of tests verifies several LP-RX behavioral requirements defined in various Sections of the D-PHY Specification.

**Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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**Test 2.2.1 – LP-RX Initialization period ( $T_{INIT}$ )**

**Purpose:** To verify that the Slave DUT's RX Initialization period ( $T_{INIT}$ ), is greater than the minimum conformant value.

**References:**

- [1] D-PHY Specification, Section 5.11, Line 985
- [2] Ibid, Section 5.11, Line 991
- [3] Ibid, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.2.

**Last Modification:** September 16, 2010

**Discussion:**

The D-PHY Specification includes specifications regarding the initialization behavior of both Master and Slave devices. This includes requirements for how Slave devices are initialized, which is accomplished via the  $T_{INIT}$  interval.

The specification states, “*After power-up, the Slave side PHY shall be initialized when the Master PHY drives a Stop State (LP-11) for a period longer than  $T_{INIT}$ . The first Stop state longer than the specified  $T_{INIT}$  is called the Initialization period. The Master PHY itself shall be initialized by a system or Protocol input signal (PPI). The Master side shall ensure that a Stop State longer than  $T_{INIT}$  does not occur on the Lines before the Master is initialized. The Slave side shall ignore all Line states during an interval of unspecified length prior to the Initialization period.*” [1]

The specification also states, “*Note that  $T_{INIT}$  is considered a protocol-dependent parameter, and thus the exact requirements for  $T_{INIT,MASTER}$  and  $T_{INIT,SLAVE}$  (transmitter and receiver initialization Stop state lengths, respectively,) are defined by the protocol layer specification and are outside the scope of this document. However, the D-PHY specification does place a minimum bound on the lengths of  $T_{INIT,MASTER}$  and  $T_{INIT,SLAVE}$ , which each shall be no less than 100  $\mu$ s. A protocol layer specification using the D-PHY specification may specify any values greater than this limit, for example,  $T_{INIT,MASTER} \geq 1$  ms and  $T_{INIT,SLAVE} = 500$  to 800  $\mu$ s.*” [2].

Note that because of the protocol-dependence of this parameter, the proper protocol-specific values must be determined for the DUT, via the respective protocol specifications.

Note also that because  $T_{INIT}$  is considered a protocol-dependent parameter by the D-PHY specification, it is possible that the detection and validation of the  $T_{INIT}$  interval may be implemented in the protocol layer logic for some DUT types. Therefore, if a DUT is not designed to contain this logic (e.g., for a bare-phy DUT with a PPI or other exposed protocol interface), this test is considered Not Applicable.

For Slave DUTs, a test can be designed in order to verify whether or not the DUT ignores all line states prior to receiving a valid Initialization period. This can be done using a wide variety of sequences, by sending any valid LP or HS sequence to the DUT that causes an observable result. If the sequence is not preceded by a valid  $T_{INIT}$  interval, the DUT should ignore the sequence.

For the purposes of this test, all Lanes will be tested simultaneously, by sending  $T_{INIT}$  on all Lanes, prior to the valid sequence.

**Test Setup:** See Appendix B.2.

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**Test Procedure:**

- Connect the Slave DUT to the Test Setup, leaving the DUT power off.
- Power on the DUT.
- Without sending a valid Initialization period, send a valid HS or LP test sequence that would otherwise cause an observable result.
- Verify that the DUT ignores the test sequence.
- Repeat the previous 2 steps multiple times, slowly increasing the duration of the Initialization period until the DUT is observed to accept the test sequence.
- Record  $T_{INIT}$  as the minimum Initialization period that caused the DUT to accept the test sequence.

**Observable Results:**

- Verify that the value of  $T_{INIT}$  is greater than the minimum protocol-specific conformance limit.

**Possible Problems:** None.

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**Test 2.2.2 – ULPS Exit: LP-RX T<sub>WAKEUP</sub> Timer Value**

**Purpose:** To verify that the DUT's LP receiver properly exits ULPS when sent a Mark-1 for minimum time ( $T_{WAKEUP}$ ) followed by a Stop state.

**References:**

- [1] D-PHY Specification, Section 5.6.3
- [1] Ibid, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

The D-PHY Specification defines a mechanism for bringing Lanes out of the ULPS state [1]. This procedure involves driving a Mark-1 state (LP-10) for a minimum time  $T_{WAKEUP}$ , followed by a Stop state (LP-11), which should be detected by the Slave device.

The purpose of this test is to verify that a Slave device properly detects a validly formed ULPS exit sequence that contains a minimum duration Mark-1 state (1ms). The Test System will emulate a Master device, which will put the Clock and Data Lanes into the ULPS state. A test sequence will then be sent which begins with the minimum-duration ULPS exit sequence, followed by any valid HS image data sequence that produces an observable result on the DUT. The DUT will then be observed to determine if the image data sequence was properly received (implying that the DUT did successfully exit the ULPS state.)

(Note that the general methodology for this test is similar to the  $T_{INIT}$  test of 2.2.1, however rather than sending a valid observable sequence that is preceded by a valid  $T_{INIT}$  sequence, the DUT is placed into ULPS mode, and then is sent a valid observable sequence that is preceded by a valid  $T_{WAKEUP}$  sequence.)

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to send a sequence to the DUT that will put the Clock and Data Lanes into the ULPS state.
- With the DUT in the ULPS state, send the test sequence consisting of a Mark-1 (LP-10) state for 1ms, followed by a valid HS image data sequence.
- Observe whether or not the DUT receives the HS image data sequence (implying that if the image data is received, the DUT must have properly exited ULPS mode.)

**Observable Results:**

- Verify that the DUT exits ULPS mode.

**Possible Problems:** None.

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**Test 2.2.3 – Clock Lane LP-RX Invalid/Aborted ULPS Entry**

**Purpose:** To verify that the DUT Clock Lane LP-RX properly aborts the ULPS entry process when it receives an invalid/aborted ULPS entry sequence.

**References:**

- [1] D-PHY Specification, Section 5.7, Line 915
- [2] Ibid, Section 5.8, Line 945

**Resource Requirements:** See Appendix A.2.

**Last Modification:** September 16, 2010

**Discussion:**

The D-PHY Specification defines requirements for Ultra-Low Power State (ULPS) behavior for both Clock and Data Lanes. Because the Clock Lane uses a different ULPS entry sequence than the Data Lane, different requirements are defined, for both the TX and RX sides of the Lane. Included in these is a provision for how a Clock Lane LP-RX should handle an aborted or invalid ULPS Entry sequence.

The specification states, “*A Clock Lane shall be unidirectional and shall not include regular Escape mode functionality. Only ULPS shall be supported via a special entry sequence using the LP-Rqst state. High-Speed Clock Transmission shall start from, and exit to, a Stop state.*”[1].

The specification further states, “*A Clock Lane shall enter Ultra-Low Power State via a Clock Lane Ultra-Low Power State Entry procedure. In this procedure, starting from Stop state, the transmit side shall drive TX-ULPS-Rqst State (LP-10) and then drive TX-ULPS State (LP-00). After this, the Clock Lane shall enter Ultra-Low Power State. If an error occurs, and an LP-01 or LP-11 is detected immediately after the TX-ULPS-Rqst state, the Ultra-Low Power State Entry procedure shall be aborted, and the receive side shall wait for, or return to, the Stop state, respectively.*”[2].

In this test, the DUT’s Clock Lane’s LP-RX will be tested, to determine if it can properly handle invalid Clock Lane ULPS Entry sequences. Additionally, the Clock Lane will also be tested to determine that it does not support (i.e., ignores) a Data Lane ULPS Entry sequence.

As stated above, the proper Clock Lane ULPS Entry sequence consists of LP-11/10/00. The requirement states that if either LP-11/10/01, or LP-11/10/11 is detected by the Clock Lane LP-RX, it shall treat the sequence in a manner such that normal operation shall not be impaired. (Practically speaking, it should effectively ignore the sequence, wait for a return to LP-11, and resume normal operation.)

While there are multiple possible ways this test could be implemented, the easiest method would simply be to start with any valid HS Clock/Data burst sequence that produces an observable result (e.g., a complete image or video sequence), and insert the desired invalid Clock Lane ULPS entry sequences between Clock Lane bursts. If the DUT properly ignores the invalid sequences, the image data (and overall operation of the DUT) should not be negatively affected.

Two different invalid Clock Lane ULPS Entry test cases will be performed. The first case will insert LP-11/10/11 between otherwise validly constructed Clock bursts. The second case will insert LP-11/10/01/11.

A third test case will also be performed, which will insert a properly formed Data Lane ULPS Entry sequence (followed by a Mark-1/Stop) between Clock bursts. (Note the duration of all LP states in this sequence, including the Mark-1/Stop, will be set to the nominal  $T_{LPX}$  value specified for the DUT.)

In all three cases, the DUT’s operation must not be negatively affected in order to be considered conformant.

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**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test Setup.
- Configure the Test Setup to transmit a valid image or video sequence to the DUT, and verify that the image data is properly received by the DUT (via any available observable means).
- Once proper operation has been verified, modify the sequence by inserting an LP-11/10/11 invalid ULPS sequence between bursts on the Clock Lane (keeping all other necessary video timings intact, as needed), and re-transmit the sequence to the DUT.
- Verify that the DUT is still able to successfully receive the image data without impairment.
- Repeat the above procedure a second time, using the LP-11/10/01/11 invalid ULPS sequence.
- Repeat the above procedure a third time, using the Data Lane ULPS sequence.

**Observable Results:**

- In all three cases, verify that the integrity of the received data, as well as the overall operation of the DUT are not negatively affected by the presence of the invalid ULPS Entry sequences.

**Possible Problems:** None.

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**Test 2.2.4 – Data Lane LP-RX Invalid/Aborted Escape Mode Entry**

**Purpose:** To verify that the DUT's Data Lane LP-RX properly aborts the Escape Mode entry process when it receives an unexpected Stop state prior to completion.

**References:**

- [1] D-PHY Specification, Section 5.6.4
- [2] Ibid, Section 5.6, Line 840
- [3] Ibid, Section 5.6, Line 842

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

The D-PHY Specification provides a formal definition of the Escape Mode Entry process in state-machine form [1].

The specification also states in text form, “*A Data Lane shall enter Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape mode in Space state (LP-00).*”[2]. An example of the Escape Mode Entry procedure, reproduced from the D-PHY specification, is shown below.

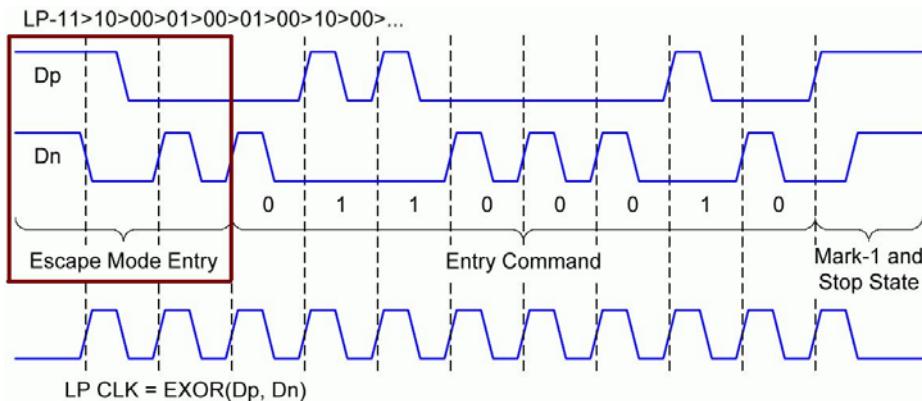


Figure 18 Trigger-Reset Command in Escape Mode

Figure 2.2.4-1: Escape Mode Entry Procedure (with Trigger-Reset Command)

The specification additionally states, “*If an LP-11 is detected at any time before the final Bridge state (LP-00), the Escape mode Entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.*”[3].

In this test, the ability of the DUT's LP-RX to properly detect and handle invalid Escape Mode Entry sequences will be verified. The general methodology for this test is similar to the previous Test 2.2.4 (Clock Lane Invalid ULPS Entry), except invalid Data Lane Escape Mode Entry sequences will be sent between Data Lane HS bursts. The DUT will be observed to determine whether the presence of the invalid sequences causes errors in the received data.

As for which specific test patterns to send for the invalid entry test cases, care must be taken to ensure that the test cases do not contain other valid LP sequences, which could be misinterpreted by the DUT. The following sequences will be sent, where the state deviations from the valid Escape Mode Entry sequence are shown in red:

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**LP-11, LP-10, LP-00, LP-01, LP-00** (valid Escape Mode Entry sequence)

<b>Test Case 1)</b>	<b>LP-11, LP-10, LP-00, LP-01, LP-11</b>
<b>Test Case 2)</b>	<b>LP-11, LP-10, LP-00, LP-11, LP-11</b>
<b>Test Case 3)</b>	<b>LP-11, LP-10, LP-11, LP-11, LP-11</b>

In this test, the 3 above cases of invalid Escape Mode Entry sequences will be sent to the DUT. The sequences will be inserted between HS bursts in the image data sequence, and should be inserted at the end of every line of pixel data. In all cases the presence of the invalid Escape Mode Entry sequences shall not affect the ability of the receiver to properly receive the HS data in order for the DUT to be considered conformant.

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test Setup.
- Configure the Test Setup to transmit a valid image or video sequence to the DUT, and verify that the image data is properly received by the DUT (via any available observable means).
- Once proper operation has been verified, modify the sequence by inserting an LP-11/10/00/01/11 invalid Escape Mode Entry sequence (test case #1 above) between HS bursts on the Data Lane (keeping all other necessary video timings intact, as needed), and re-transmit the sequence to the DUT.
- Verify that the DUT is still able to successfully receive the image data without impairment.
- Repeat the previous two steps for the other two test cases.

**Observable Results:**

- In all cases, verify that the integrity of the received data, as well as the overall operation of the DUT are not negatively affected by the presence of the invalid/aborted Data Lane Escape Mode Entry sequences.

**Possible Problems:** None.

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**Test 2.2.5 – Data Lane LP-RX Invalid/Aborted Escape Mode Command**

**Purpose:** To verify that the DUT's Data Lane LP-RX properly ignores invalid/aborted Escape commands.

**References:**

- [1] D-PHY Specification, Section 5.6, Line 840
- [2] Ibid, Section 5.2, Line 758
- [3] Ibid, Section 5.6, Line 848

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

The previous test (2.2.4) verified a DUTs ability to detect invalidly formed Escape Mode Entry sequences, which were corrupted with LP-11 Stop states at different locations in the Escape Mode Entry sequence. The result of these tests was that the DUT should have effectively ignored the invalid sequence and not have allowed the invalid sequences to negatively impact reception of subsequent valid data.

This test is effectively a continuation of the same idea, extending the LP-11 corruption into the actual command fields. An example showing a validly formed Escape Mode Entry Command (reproduced from the D-PHY Specification) is shown below.

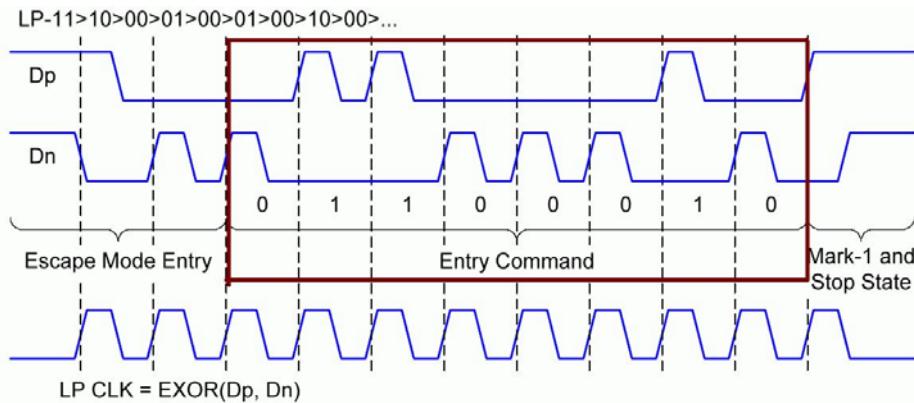


Figure 18 Trigger-Reset Command in Escape Mode

**Figure 2.2.5-1: Complete Escape Mode Sequence (Trigger-Reset Command Shown)**

The specification states, “A Data Lane shall enter Escape mode via an Escape mode Entry procedure (LP-11, LP-10, LP-00, LP-01, LP-00). As soon as the final Bridge state (LP-00) is observed on the Lines the Lane shall enter Escape mode in Space state (LP-00).”[1].

Also, the specification states, “If LP-11 occurs during Escape mode the Lane returns to Stop state (Control Mode LP-11).”[2].

Also, the specification states, “The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.”[3].

In this test, fifteen test cases of a corrupted Entry Command will be sent to the DUT. They will be inserted between HS bursts of an otherwise valid image data stream. All of the test sequences will contain valid Escape Mode Entry sequences, but will abort the Escape Mode command by prematurely returning to LP-11 before the end

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of the command. A ULPS Entry command will be used as the basis for the corrupted command sequences. The following corrupted sequence test cases will be defined:

- 1) [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/00/10/00/10/00/10/00/10/00/11 + [Stop]
- 2) [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/00/10/00/10/00/10/00/11/11 + [Stop]
- 3) [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/00/10/00/10/00/10/11/11/11 + [Stop]
- 4) [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/00/10/00/10/00/11/11/11/11 + [Stop]
- 5) [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/00/10/00/10/11/11/11/11 + [Stop]
- 6) [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/00/10/00/11/11/11/11/11 + [Stop]
- 7) [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/00/10/11/11/11/11/11/11 + [Stop]
- 8) [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/00/11/11/11/11/11/11/11 + [Stop]
- 9) [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/10/11/11/11/11/11/11/11 + [Stop]
- 10) [Valid Escape Mode Entry] + LP-01/00/01/00/01/00/11/11/11/11/11/11/11/11 + [Stop]
- 11) [Valid Escape Mode Entry] + LP-01/00/01/00/11/11/11/11/11/11/11/11/11 + [Stop]
- 12) [Valid Escape Mode Entry] + LP-01/00/01/00/11/11/11/11/11/11/11/11/11/11 + [Stop]
- 13) [Valid Escape Mode Entry] + LP-01/00/11/11/11/11/11/11/11/11/11/11 + [Stop]
- 14) [Valid Escape Mode Entry] + LP-01/00/11/11/11/11/11/11/11/11/11/11 + [Stop]
- 15) [Valid Escape Mode Entry] + LP-01/11/11/11/11/11/11/11/11/11/11/11 + [Stop]

In all test cases the presence of the aborted ULPS command sequences shall not affect the ability of the receiver to properly receive the HS image data, in order for the DUT to be considered conformant.

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test Setup.
- Configure the Test Setup to transmit a valid image or video sequence to the DUT, and verify that the image data is properly received by the DUT (via any available observable means).
- Once proper operation has been verified, modify the sequence by inserting the Test Case #1 (above) aborted ULPS command sequence between HS bursts on the Data Lane (keeping all other necessary video timings intact, as needed), and re-transmit the sequence to the DUT.
- Verify that the DUT is still able to successfully receive the image data without impairment.
- Repeat the previous two steps for the 14 additional Test Cases.

**Observable Results:**

- In all cases, verify that the integrity of the received data, as well as the overall operation of the DUT are not negatively affected by the presence of the invalid/aborted ULPS command sequences.

**Possible Problems:** None.

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#### **Test 2.2.6 – Data Lane LP-RX Escape Mode Invalid Exit (INFORMATIVE)**

**Purpose:** To observe the behavior of the DUT's LP-RX when an invalid Exit Sequence (Mark) is received following the reception of a valid Escape Mode Entry Command.

### References:

- ## [1] D-PHY Specification, Section 5.6

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

### **Discussion:**

*(Note: The issue has been raised that this test may not be a valid test as currently written, as the exact behavior upon reception of these test cases is not explicitly defined in the spec. Therefore this test has been reclassified as informative. The behavior of the DUT will be observed and reported for informational purposes only.)*

In the previous test (2.2.5) the DUTs ability to detect invalidly formed/aborted Escape Mode Commands (which were corrupted with LP-11 Stop states at various offsets) was verified. The result of these tests was that the DUT should have ignored the invalid/aborted commands.

This test is a continuation of the same concept, but applied to the trailing two-state Mark-1/Stop Exit sequence. An example showing a validly formed trailing Mark-1/Stop (based on Figure 18 of the D-PHY specification) is shown below.

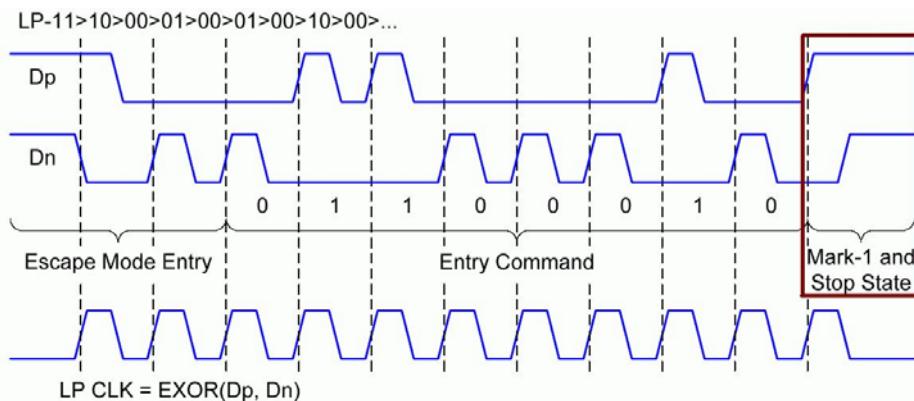


Figure 18 Trigger-Reset Command in Escape Mode

**Figure 2.2.6-1: Complete Escape Mode Sequence (Valid Mark-1/Stop Shown)**

In this test, the DUT will be sent a pattern containing a valid Entry Sequence + valid Command + invalid Exit sequence. Three cases of invalid Exit will be sent: Mark-0/Stop, Space/Stop, and Stop/Stop.

This test will use a different methodology from the previous several tests, where invalid ULPS Entry sequences were inserted into an otherwise valid data stream. Note that in this case the ULPS Entry command cannot be used, as it is not followed by a Mark-1/Stop sequence. Therefore a different sequence must be chosen. However, as all other sequences are restricted to Data Lane 0 for all currently defined D-PHY applications, this measurement will only be able to be performed on Data Lane 0.

The recommended sequence for DSI devices is to send a short packet via LPDT mode, which causes an observable result (e.g., backlight on/off, etc.) For CSI-2 devices, this test cannot be performed with a command that

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produces an observable result (as none exists for CSI), however a modified form of the test can be performed using an unassigned Escape Mode command (which should be ignored by the device), and the device's behavior observed to ensure that normal data reception is not impacted when the test cases are inserted in an otherwise valid image data stream.

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to send a properly formed LP Escape Mode command to the DUT that causes an observable result.
- Verify that the transmitted sequence causes the expected observable result to occur.
- Repeat this process three additional times, using each of the three defined test cases of invalid Exit sequences, and for each case record the resulting behavior of the DUT (i.e., observe whether the DUT received and successfully executed the command, or if the command was ignored.)

**Observable Results:**

- As this test is informative, no pass/fail requirements are defined. The behavior of the DUT upon reception of the three invalid Exit test cases is simply reported for informative purposes.

**Possible Problems:** None.

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**Test 2.2.7 – Data Lane LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits**

**Purpose:** To verify that the DUT LP-RX ignores any extra bits received following a Trigger Command.

**References:**

- [1] D-PHY Specification, Section 5.6.1, Line 873
- [2] Ibid, Section 4.5, Line 561

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

The D-PHY specification defines the Escape Mode behavior for D-PHY transmitters and receivers. This includes a requirement for how receivers treat extra bits that are received after an Escape Mode Trigger command.

The specification states, “*Any bit received after a Trigger Command but before the Lines go to Stop state shall be ignored. Therefore, dummy bytes can be concatenated in order to provide Clock information to the receive side.*”[1].

In this test, several test cases are constructed that include additional extra bits following the Trigger Command and before the Mark-1/Stop Exit sequence, in an otherwise validly formed Escape Command sequence.

Note that according to the specification wording, this requirement explicitly applies to Escape Mode Trigger commands only, and not the ‘Undefined’, ‘ULPS’, or ‘LPDT’ command types. A list of the assigned Escape Entry Codes is reproduced from the specification in the figure below.

**Table 8 Escape Entry Codes**

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

**Figure 2.2.7-1: Assigned Escape Mode Entry Command Codes**

Because the receiver behavior upon reception of an Escape Mode Trigger is mostly protocol-defined and outside the scope of the D-PHY specification, this test will simply verify that normal operation of the receiver is not negatively impacted by the reception of Triggers that have extra post-command bits appended after the Command byte.

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Note also that this requirement will be verified for all Lanes. While many D-PHY applications may restrict most Escape Mode functionality to Data Lane 0, the D-PHY specification explicitly states, “*All Lanes shall include Escape mode support for ULPS and Triggers in the Forward direction.*”[2].

The methodology for this test will follow the same general approach as Tests 2.2.4 and 2.2.5, where the Escape Mode test case sequence will be inserted between the HS bursts of an otherwise valid data stream. However rather than a ULPS Entry command, the Escape Mode sequence for this test will contain a Trigger sequence, followed by extra bits. The Escape Mode sequence will be transmitted on all Data Lanes simultaneously. The DUT behavior will be observed to verify that the presence of the extra post-command bits does not impact proper image data reception. (Because the Trigger command itself should have no impact on normal operation, the default observable in all cases for this test is that the image data should be received without error.)

The choice of the extra post-command bits must be defined for this test. This test will concatenate one extra byte of data after the Trigger command, and will use the ULPS Entry command as this extra byte. As the DUT should ignore this additional byte according the specification, proper DUT behavior should not be impacted, as the ULPS command should effectively be ignored by the receiver.

This test will verify that for each of the four Trigger commands (see Figure 2.2.7-1 above), the presence of an additional ULPS command byte appended after the Trigger will not affect proper reception of the image data stream.

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test Setup to transmit a valid image or video sequence to the DUT, and verify that the image data is properly received by the DUT (via any available observable means).
- Once proper operation has been verified, modify the sequence by inserting a validly formed Escape Mode Entry sequence + Reset-Trigger command (01100010) + ULPS command (00011110) on all Data Lanes, after each horizontal line of pixel data of the image Data Stream, and re-transmit the sequence to the DUT.
- Verify that the DUT does receive the image data stream.
- Repeat this process three additional times, using the Unknown-3, Unknown-4, and Unknown-5 Trigger commands in place of the Reset-Trigger, and for each case verify that the DUT does properly receive the image data stream.

**Observable Results:**

- Verify that in all test cases the DUT ignores all bits occurring after the last bit of the Trigger Command, by observing that the DUT properly received the image data stream without error.

**Possible Problems:** None.

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**Test 2.2.8 – Data Lane LP-RX Escape Mode Unsupported/Unassigned Commands**

**Purpose:** To verify that the DUT's Data Lane LP-RX properly ignores unsupported and unassigned Escape Mode commands.

**References:**

[1] D-PHY Specification, Section 5.6, Line 849

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

The D-PHY specification defines eight ‘assigned’ Escape Mode Command codes, which may or may not be supported by a particular DUT [1]. (Note the terms *assigned* and *supported* are not equivalent, and have two separate meanings. Devices may or may not support any of the 8 assigned Command codes, however devices should always ignore (i.e., never support) any of the 248 unassigned codes.) The list of assigned codes, reproduced from the D-PHY specification, is shown below.

**Table 8 Escape Entry Codes**

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

**Figure 2.2.8-1: Assigned Escape Mode Entry Command Codes**

The specification states, “*If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state*”. [1]

The methodology for this test will be identical to Tests 2.2.4/5/7, where an Escape Mode sequence will be inserted between HS bursts of an otherwise valid image data stream, on all Data Lanes. The Escape Mode sequence will contain an unassigned Escape command byte. The DUT's behavior will be observed to verify that the presence of the unassigned command code does not impact reception of the valid data stream.

In this test, the DUT will be sent all 248 unassigned Command codes, contained in properly formed, valid Escape sequences. It will also be sent the Undefined-1, Undefined-2, Unknown-3, Unknown-4, and Unknown-5 Command codes shown above. In all cases, the DUT should ignore the command code.

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Note that for the sake of test time, multiple test cases may be combined into a single stimulus sequence, provided each of the Escape command codes is transmitted in its own LP burst (i.e., it is preceded by its own Escape Mode Entry sequence and is followed by a return to the Stop state (LP-11) before the next command code is sent.)

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test Setup to transmit a valid image or video sequence to the DUT, and verify that the image data is properly received by the DUT (via any available observable means).
- Once proper operation has been verified, modify the sequence by inserting a validly formed Escape Mode Entry sequence + the Undefined 1 command code (10011111), on all Data Lanes, between the HS bursts of the image Data Stream, and re-transmit the sequence to the DUT.
- Verify that the DUT **does** receive the image data stream.
- Repeat this process 4 additional times, using the Undefined-1, Unknown-3, Unknown-4, and Unknown-5 Trigger commands in place of the Undefined 1 command, and for each case verify that the DUT **does** properly receive the image data stream.
- Repeat this process 248 additional times, using each of the 248 unassigned command codes, and for each case verify that the DUT **does** properly receive the image data stream.

**Observable Results:**

- For all test cases, verify that the DUT ignores the unsupported/unassigned command, and successfully receives the image data stream.

**Possible Problems:** None.

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## **GROUP 3: HS-RX VOLTAGE AND SETUP/HOLD REQUIREMENTS**

**Overview:**

This group of tests verifies various High-Speed RX signaling requirements defined in multiple Sections of the D-PHY Specification (including Sections 8.2.1, 5.x, and 9.2.1).

**Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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**Test 2.3.1 – HS-RX Common Mode Voltage Tolerance ( $V_{CMRX(DC)}$ )**

**Purpose:** To verify that the DUT's HS receiver can successfully receive signaling with common-mode voltage levels ( $V_{CMRX(DC)}$ ) within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.2.1, Line 1459
- [2] Ibid, Section 8.2.1, Table 20

**Resource Requirements:** See Appendix A.2.

**Last Modification:** October 17, 2008

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{CMRX(DC)}$ , which describes the amount of common-mode voltage offset a receiver should be capable of tolerating, and still be able to operate properly.

The specification states, “ $V_{CMRX(DC)}$  is the differential input common-mode voltage. The HS receiver shall be able to detect differential signals at its  $D_p$  and  $D_n$  input signal pins when both signal voltages,  $V_{D_p}$  and  $V_{D_n}$ , are within the common-mode voltage range and if the voltage difference of  $V_{D_p}$  and  $V_{D_n}$  exceeds either  $V_{IDTH}$  or  $V_{IDTL}$ . ”[1]

In this test, HS signaling will be sent to the DUT that contains various common-mode levels. Multiple cases will be tested, which verify the lower and upper limits of the conformance range (which is defined as 70mV to 330mV)[2]. HS data will be sent to the DUT with different common-mode levels, and in all test cases the DUT should be able to receive the data without error. (Note the test pattern can be various HS sequences depending on the DUT type. See Appendix G.)

Note that while this test verifies the HS-RX common mode levels, it is important to consider the differential voltage levels used for each of the test cases. (Note: This concept applies to many of the HS-RX tests, as it is possible that devices may show problems only for combinations of various worst-case parameters (e.g., minimum differential and common mode levels), but not display failures if the worst-case parameters are varied independently.) Good test design practices warrant the inclusion of test cases that will identify interdependencies between potentially interrelated parameters, and this will be especially applicable to all of the HS-RX amplitude-related tests.

Note that there are actually three different amplitude specifications for D-PHY, each with separate conformance ranges. Separate requirements are defined for the HS-RX common-mode levels ( $V_{CMRX(DC)}$ ), the HS-RX differential levels ( $V_{IDTH}$  and  $V_{IDTL}$ ), and also a third set of requirements is defined for the maximum and minimum allowed single-ended levels of the  $D_p$  and  $D_n$  signals ( $V_{IHHS}$  and  $V_{ILHS}$ ). When testing any one of these parameters, it might seem desirable to vary the other two parameters across their entire ranges, however this must be done with caution, as there is some interdependence between the three specifications, which for some cases is mutually exclusive (e.g., it is not possible to create a signal with the maximum TX common-mode level (330mV) and maximum TX differential level (540mVppd) simultaneously, as such a signal would have a single-ended  $D_p/D_n$  value of 465mV, which would violate the upper  $V_{IHHS}$  limit of 460mV.)

When designing any test with potentially interrelated parameters, it is also important to include control cases to help isolate the specific parameter under test. For this test, it has already been mentioned that the maximum differential amplitude cannot be used for the maximum common-mode voltage test case, however it is possible to select a slightly smaller differential voltage, which does not violate the  $V_{IHHS}$  single-ended upper limit. A differential voltage of 520mVppd with a common mode level of 330mV will produce a maximum single-ended voltage of  $330 + (520/4) = 460$ mV. (Where the maximum single-ended voltage for either  $D_p$  or  $D_n$  will be equal to the common mode level plus 1/4 the peak-to-peak differential level.)

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Note however that in this case, we have a test signal that has values for both  $V_{CMRX}$  and  $V_{IHHS}$  that are exactly at the conformance limits. If a DUT is observed to have issues receiving this signal, it is not possible to determine whether the failure is due to a sensitivity to the common mode level, or the maximum single-ended level, which does not isolate the parameter under test.

To address this issue, an additional test case will be added which uses a slightly smaller differential voltage, which leaves some additional margin from the upper  $V_{IHHS}$  limit. A differential voltage of 440mVppd with a common mode level of 330mV will produce a maximum single-ended voltage of  $330 + (440/4) = 440$ mV. This test case will provide an additional piece of data to better isolate the common-mode tolerance characteristics of the receiver.

Note that three similar test cases will be defined for verifying the minimum common mode level requirements. A summary of all test cases is shown in the table below.

**Table 2.3.1-1:  $V_{CMRX}$  Common Mode Level Test Cases**

Test Case #	$V_{CMRX}$ Common-Mode Level	Pk-Pk Differential Voltage ( $2 \cdot V_{OD}$ )	Single-Ended $V_{IHHS}/V_{ILHS}$	Comments
1	70mV	360mVppd	160mV/-20mV	Minimum CM level, with largest possible Vdiff* that <u>almost</u> hits the lower $V_{ILHS}$ limit of -40mV (leaving 20mV margin), so $V_{diff} = 4 \cdot (70 - -20) = 360$ mVppd.
2	70mV	440mVppd	180mV/-40mV	Minimum CM level, but with the largest possible Vdiff that exactly hits the $V_{ILHS}$ lower limit of -40mV (with no margin), so $V_{diff} = 440$ mVppd.
3	70mV	140mVppd	105mV/35mV	Minimum CM level with minimum Vdiff (140mVppd).
4	330mV	440mVppd	440mV/220mV	Maximum CM level, with the largest Vdiff that leaves 20mV of SE margin from the $V_{IHHS}$ upper limit of 460mV, so $V_{diff} = 440$ mVppd (which gives a maximum single-ended $V_{IHHS}$ level of $330 + 110 = 440$ mV.)
5	330mV	520mVppd	460mV/200mV	Maximum CM level, but with the largest possible Vdiff that exactly hits the $V_{IHHS}$ upper limit of 460mV, so $V_{diff} = 520$ mVppd.
6	330mV	140mVppd	365mV/295mV	Maximum CM level with minimum Vdiff (140mVppd).

\*  $V_{diff}$  = Peak-to-peak value of the differential signal (which equals 2x the  $V_{OD(1)}$  value).

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to generate a suitable HS test pattern with the common mode and differential voltage levels specified for Test Case #1 above, for all Clock and Data Lanes.
- Transmit the test sequence to the DUT.
- Verify via any valid observable that the DUT received the test sequence without errors.
- Repeat the previous three steps for Test Cases 2 though 6.

**Observable Results:**

- Verify that for all test cases the test sequence was received by the DUT without error.

**Possible Problems:** None.

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**Test 2.3.2 – HS-RX Differential Input High Threshold ( $V_{IDTH}$ )**

**Purpose:** To verify that the DUT's HS receiver can properly detect HS-1 voltage levels that are at least as small as the minimum required value ( $V_{IDTH}$ ).

**References:**

- [1] D-PHY Specification, Section 8.2.1, Line 1457
- [2] Ibid, Section 8.2.1, Table 20

**Resource Requirements:** See Appendix A.2.

**Last Modification:** October 17, 2008

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{IDTH}$ , or the RS-RX Differential Input High Threshold Voltage. This is the minimum differential signal level seen as a HS-1 by the receiver. (It can also be thought of as a receiver ‘squench level’, below which any activity is not detected by the RX.)

The specification states, “*The differential input high and low threshold voltages of the HS receiver are denoted by  $V_{IDTH}$  and  $V_{IDTL}$ , respectively.  $V_{ILHS}$  and  $V_{IHHS}$  are the single-ended, input low and input high voltages, respectively.  $V_{CMRX(DC)}$  is the differential input common-mode voltage. The HS receiver shall be able to detect differential signals at its  $D_p$  and  $D_n$  input signal pins when both signal voltages,  $V_{DP}$  and  $V_{DN}$ , are within the common-mode voltage range and if the voltage difference of  $V_{DP}$  and  $V_{DN}$  exceeds either  $V_{IDTH}$  or  $V_{IDTL}$ .*”[1]

Note that this test is almost identical to the  $V_{IDTL}$  test of 2.3.3 (which verifies the minimum detectable HS-0 voltage level). While the specification defines  $V_{IDTH}$  and  $V_{IDTL}$  as separate parameters, from a practical standpoint it is nearly impossible to verify these values independently of each other, as for any properly-formed HS signal it is not possible to vary only the HS-1 or HS-0 levels, as they are always symmetric about the  $V_{CMTX}$  level. It is sufficient for the purposes of conformance to verify both parameters simultaneously, however for characterization test purposes, the only way to independently validate the two parameters would require the ability to observe individual bit errors in the received data. A test scenario could be created where both the HS-0 and HS-1 levels were decreased together, and the received bit stream would be monitored to see at what points the 0 bits and 1 bits independently show errors. As all of the observables described in Appendix G for the typical D-PHY DUT types are based on packet error (not bit error) detection mechanisms, such a test scenario cannot be practically implemented.

For this test, an initial verification step will be performed where the high-speed test pattern will be sent to the DUT starting at a nominal differential voltage of  $V_{OD} = 200mV$  (400mV pk-pk differential), to verify proper test setup and DUT operation under ‘normal’ conditions. (Note also that a nominal  $V_{CMTX}$  TX common-mode level of 200mV will be used throughout this entire test. There is no need to test  $V_{IDTH}$  at the max/min  $V_{CMTX}$  levels, as these cases were already verified in Test 2.3.1). Following this, the procedure will be repeated, with the differential amplitude slowly decreased for each iteration until the point is reached where the DUT begins to show errors.  $V_{IDTH}$  is recorded as the minimum  $V_{OD}$  value where the DUT was able to consistently receive the test sequence without error. The  $V_{IDTH}$  result must be less than or equal to 70mVpk (140mV pk-pk differential), in order to be considered conformant [2].

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to generate a suitable HS test pattern with a nominal common mode level of 200mV and peak-to-peak differential amplitude of 400mVppd, for all Clock and Data Lanes.
- Transmit the test sequence to the DUT.
- Verify (via any valid observable) that the DUT received the test sequence without errors.

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- Repeat the previous three steps, slowly decreasing the peak-to-peak differential voltage across all Lanes until the point is reached where the DUT begins to indicate errors.
- Record  $V_{IDTH}$  as 0.5 times the smallest peak-to-peak differential amplitude where the DUT was able to consistently receive the test sequence without errors. (The factor of 0.5 is required to convert the peak-to-peak differential voltage to  $V_{OD(1)}$ , which is defined as the peak value of the differential signal.)

**Observable Results:**

- Verify that  $V_{IDTH}$  is less than or equal to 70mV.

**Possible Problems:** None.

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**Test 2.3.3 – HS-RX Differential Input Low Threshold ( $V_{IDTL}$ )**

**Purpose:** To verify that the DUT's HS receiver can properly detect HS-0 voltage levels that are at least as small as the minimum required value ( $V_{IDTL}$ ).

**References:**

- [1] D-PHY Specification, Section 8.2.1, Line 1457
- [2] Ibid, Section 8.2.1, Table 20

**Resource Requirements:** See Appendix A.2.

**Last Modification:** October 17, 2008

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{IDTL}$ , or the HS-RX Differential Input Low Threshold. This is the minimum differential signal level seen as an HS-0 by the receiver.

The specification states, “*The differential input high and low threshold voltages of the HS receiver are denoted by  $V_{IDTH}$  and  $V_{IDTL}$ , respectively.  $V_{ILHS}$  and  $V_{IHHS}$  are the single-ended, input low and input high voltages, respectively.  $V_{CMRXDC}$  is the differential input common-mode voltage. The HS receiver shall be able to detect differential signals at its  $D_p$  and  $D_n$  input signal pins when both signal voltages,  $V_{DP}$  and  $V_{DN}$ , are within the common-mode voltage range and if the voltage difference of  $V_{DP}$  and  $V_{DN}$  exceeds either  $V_{IDTH}$  or  $V_{IDTL}$ .*”[1]

(Note the procedure for this test is identical to the  $V_{IDTH}$  test of 2.3.2.)

$V_{IDTL}$  is recorded as the minimum  $V_{OD}$  value where the DUT was able to consistently receive the test sequence without error.

The  $V_{IDTL}$  value must be greater than or equal to -70mVpk (140mV pk-pk differential), in order to be considered conformant [2].

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to generate a suitable HS test pattern with a nominal common mode level of 200mV and peak-to-peak differential amplitude of 400mVppd, for all Clock and Data Lanes.
- Transmit the test sequence to the DUT.
- Verify (via any valid observable) that the DUT received the test sequence without errors.
- Repeat the previous three steps, slowly decreasing the peak-to-peak differential voltage across all Lanes until the point is reached where the DUT begins to indicate errors.
- Record  $V_{IDTL}$  as -0.5 times the smallest peak-to-peak differential amplitude where the DUT was able to consistently receive the test sequence without errors. (The factor of -0.5 is required to convert the peak-to-peak differential voltage to  $V_{OD(0)}$ , which is defined as the peak value of the differential signal.)

**Observable Results:**

- Verify that  $V_{IDTL}$  is greater than or equal to -70mV.

**Possible Problems:** None.

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**Test 2.3.4 – HS-RX Single-Ended Input High Voltage ( $V_{IHHS}$ )**

**Purpose:** To verify that the DUT's HS receiver is able to successfully receive HS signaling with the maximum required single-ended voltage levels ( $V_{IHHS}$ ).

**References:**

- [1] D-PHY Specification, Section 8.2.1, Line 1457
- [2] Ibid, Section 8.2.1, Table 20

**Resource Requirements:** See Appendix A.2.

**Last Modification:** October 17, 2008

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{IHHS}$ , which is the maximum high-speed Dp/Dn single-ended voltage level the DUT is required to receive.

The Specification states, “*The differential input high and low threshold voltages of the HS receiver are denoted by  $V_{IDTH}$  and  $V_{IDTL}$ , respectively.  $V_{ILHS}$  and  $V_{IHHS}$  are the single-ended, input low and input high voltages, respectively.  $V_{CMRX(DC)}$  is the differential input common-mode voltage. The HS receiver shall be able to detect differential signals at its Dp and Dn input signal pins when both signal voltages,  $V_{DP}$  and  $V_{DN}$ , are within the common-mode voltage range and if the voltage difference of  $V_{DP}$  and  $V_{DN}$  exceeds either  $V_{IDTH}$  or  $V_{IDTL}$ .*”[1]

For this test, a high-speed signal will be sent to the DUT whose amplitudes are specifically chosen such that the TX  $V_{OHHS}$  single-ended levels are at the maximum RX  $V_{IHHS}$  limit of 460mV.

Note that there are multiple ways to create such a signal. One possible test case would be to use a common-mode level of 330mV (which is technically outside of the 150-250mV  $V_{CMTX}$  range that conformant transmitters are permitted to send, but is at the maximum required receiver  $V_{CMRX}$  limit of 330mV, as the RX tolerance range is intentionally designed to be wider than the TX range), and a near-maximum differential voltage of 520mVppd (where 540mVppd is the max allowed TX value). This combination results in the Dp and Dn single-ended voltages having a  $V_{OHHS}$  value of  $330 + (520/4) = 460$ mV, which is the maximum  $V_{IHHS}$  limit. However, this test case was also used in Test 2.3.1 (HS-RX Common Mode Voltage Tolerance), as it uses the maximum RX common mode level.

Because this test case has already been performed in an earlier test, it is of little value repeating it for this test. However, another option for a test case would be to use a common mode level of 325mV, and the maximum allowed TX differential amplitude of 540mVppd, which also produces a maximum single-ended value of  $325 + (540/4) = 460$ mV. Note that while this test case is really only slightly different from the previous case, it does provide an additional data point for devices that may have problems at the maximum common mode, differential, or single-ended limits. (Unfortunately for the single-ended case, there is no way to generate a signal with maximum  $V_{IHHS}$ , which does not also have either the maximum common mode or differential RX levels.)

The DUT must be able to tolerate single-ended voltage values at or below the  $V_{IHHS}$  limit of 460mV in order to be considered conformant [2].

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to generate a suitable HS test pattern with a nominal common mode level of 200mV and peak-to-peak differential amplitude of 400mVppd, for all Clock and Data Lanes.
- Transmit the test sequence to the DUT.
- Verify (via any valid observable) that the DUT received the test sequence without errors.

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- Repeat the previous three steps, but with the Test System configured to use an HS common mode level of 325mV, and a peak-to-peak differential amplitude of 540mVppd, for all Clock and Data Lanes.
- Verify (via any valid observable) that the DUT received the test sequence without errors.

**Observable Results:**

- In both test cases the DUT should receive the test sequence without errors.

**Possible Problems:** None.

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**Test 2.3.5 – HS-RX Single-Ended Input Low Voltage ( $V_{ILHS}$ )**

**Purpose:** To verify that the DUT's HS receiver is able to successfully receive HS signaling with the minimum required single-ended voltage levels ( $V_{ILHS}$ ).

**References:**

- [1] D-PHY Specification, Section 8.2.1, Line 1457
- [2] Ibid, Section 8.2.1, Table 20

**Resource Requirements:** See Appendix A.2.

**Last Modification:** October 17, 2008

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $V_{ILHS}$ , which is the minimum high-speed Dp/Dn single-ended voltage level the DUT is required to receive.

The Specification states, “*The differential input high and low threshold voltages of the HS receiver are denoted by  $V_{IDTH}$  and  $V_{IDTL}$ , respectively.  $V_{ILHS}$  and  $V_{IHHS}$  are the single-ended, input low and input high voltages, respectively.  $V_{CMRX(DC)}$  is the differential input common-mode voltage. The HS receiver shall be able to detect differential signals at its Dp and Dn input signal pins when both signal voltages,  $V_{DP}$  and  $V_{DN}$ , are within the common-mode voltage range and if the voltage difference of  $V_{DP}$  and  $V_{DN}$  exceeds either  $V_{IDTH}$  or  $V_{IDTL}$ .*”[1]

For this test, a high-speed signal will be sent to the DUT whose amplitudes are specifically chosen such that the TX  $V_{OLHS}$  single-ended levels are at the maximum RX  $V_{ILHS}$  limit of -40mV.

Note that similar to the previous test ( $V_{IHHS}$ ) there is more than one way to create a signal with the desired minimum single-ended voltages. One way would be to use the minimum RX common mode level of 70mV(which is technically outside of the 150-250mV  $V_{CMRX}$  range that conformant transmitters are permitted to send, but is at the minimum required receiver  $V_{CMRX}$  limit of 70mV, as the RX tolerance range is intentionally designed to be wider than the TX range), and a near-maximum RX differential voltage of 440mVppd, which results in a minimum single-ended level of  $70 - (440/4) = -40$ mV. However, this test case was already performed in Test 2.3.1, as it uses the minimum RX common mode level.

A second option for a test case would be to use a common mode level of 95mV, and the maximum allowed TX differential amplitude of 540mVppd, which also yields a minimum single-ended value of  $95 - (540/4) = -40$ mV. Note that while this test case is really only slightly different from the previous case, it does provide an additional data point for devices that may have problems at the minimum common mode or single-ended limits. (Unfortunately for the single-ended case, there is no way to generate a signal with minimum  $V_{ILHS}$ , which does not also have either the minimum common mode or maximum differential RX levels.)

The DUT must be able to tolerate single-ended voltage levels as low as the  $V_{ILHS}$  limit of -40mV in order to be considered conformant [2].

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to generate a suitable HS test pattern with a nominal common mode level of 200mV and peak-to-peak differential amplitude of 400mVppd, for all Clock and Data Lanes.
- Transmit the test sequence to the DUT.
- Verify (via any valid observable) that the DUT received the test sequence without errors.
- Repeat the previous three steps, but with the Test System configured to use an HS common mode level of 95mV, and a peak-to-peak differential amplitude of 540mVppd, for all Clock and Data Lanes.

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- Verify (via any valid observable) that the DUT received the test sequence without errors.

**Observable Results:**

- In both test cases the DUT should receive the test sequence without errors.

**Possible Problems:** None.

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**Test 2.3.6 – HS-RX Common-Mode Interference 50MHz - 450MHz ( $\Delta V_{CMRX(LF)}$ )**

**Purpose:** To verify that the DUT's HS receiver is capable of tolerating worst-case common-mode interference in the 50-450MHz range, with amplitudes as high as the maximum required limit ( $\Delta V_{CMRX(LF)}$ ).

**References:**

- [1] D-PHY Specification, Section 8.2.1, Line 1462
- [2] Ibid, Section 8.2.1, Table 21

**Resource Requirements:** See Appendix A.2.

**Last Modification:** October 17, 2008

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $\Delta V_{CMRX(LF)}$ , which specifies the ability of a High-Speed receiver to tolerate and reject common-mode interference across the 50-450MHz range, of defined amplitude levels.

The Specification states, “*The High-Speed receiver shall receive High-Speed data correctly while rejecting common-mode interference  $\Delta V_{CMRX(HF)}$  and  $\Delta V_{CMRX(LF)}$ .*”[1]

There are actually two specifications for HS-RX common-mode rejection, one for the 50-450MHz frequency range ( $\Delta V_{CMRX(LF)}$ , i.e., this test), and another covering frequencies above 450MHz (See Test 2.3.7,  $\Delta V_{CMRX(HF)}$ ). Both specifications can be tested using the same physical setup, however the frequency and amplitude of the common-mode interference that is combined with the test signal and injected into the receiver is different for the two specifications. This test uses a 50mVpk sinusoidal disturber over the 50-450MHz range, while the  $\Delta V_{CMRX(HF)}$  test uses a 100mVpk sinusoidal disturber over the 450-1330MHz range.

This test uses a similar setup and procedure as has been used for all previous HS-RX tests, where the various common-mode, differential, and single-ended voltage characteristics of the test signal were controlled. However, this test setup includes an additional component, which combines an externally applied common-mode sine wave with the normal Test System output signal, before it is applied to the DUT receiver. This system allows for the controlled application of various types and amounts of common-mode interference to the DUT receiver, independent of the other D-PHY amplitude characteristics.

Note a similar question arises for this test as was found for several other HS-RX tests in terms of what values should be selected for the other analog characteristics of the test stimulus (e.g., common mode/differential amplitudes, timing skew, etc.) Given that the disturber signal adds another dimension to the environment, there can be many combinations and corner cases possible. Practical limitations dictate that this set should be narrowed down to a subset of the most relevant cases.

For this test, several test cases will be performed, with both nominal and worst-case values for HS differential and common mode amplitude. For each test case, the frequency of the sinusoidal common-mode disturber signal will be swept across the 50-450MHz range, and the DUT will be monitored for errors. (Note that this procedure does not define a minimum duration at each frequency, as this test is only looking for gross failures, however the procedure can be modified if needed, if greater confidence is desired at any particular frequency.) The various test cases are listed in the table below.

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**Table 2.3.6-1:  $\Delta V_{CMRX(LF)}$  Test Cases**

Test Case #	HS Common-Mode Level	HS Differential Amplitude	Sinusoidal CM Disturber Amplitude	Comments
1	200mV	400mVppd	50mVpk	Control case. Nominal common mode and differential amplitudes.
2	200mV	140mVppd	50mVpk	Minimum differential amplitude, but still with nominal common mode level.
3	70mV	140mVppd	50mVpk	Minimum differential amplitude and minimum common mode level.
4	330mV	140mVppd	50mVpk	Maximum common mode level and minimum differential amplitude.
5	330mV	520mVppd	50mVpk	Maximum common mode level and maximum allowed differential amplitude within $V_{IHHS}$ limit.

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to generate a suitable HS test pattern with the common mode and differential voltage levels specified for Test Case #1 above, for all Clock and Data Lanes. (Leave the sinusoidal common mode disturber signal disabled for this step.)
- Transmit the test sequence to the DUT.
- Verify (via any valid observable) that the DUT received the test sequence without errors.
- Enable the sinusoidal common mode disturber signal with a frequency of 450MHz, and amplitude of 50mVpk.
- Verify that the DUT can still receive the test sequence without errors.
- Slowly sweep the sinusoidal common mode disturber frequency between 50 and 450MHz, in increments no wider than 10MHz. For all frequencies, verify that the DUT can still receive the test sequence without errors.
- Repeat the previous six steps for Test Cases 2 though 5.

**Observable Results:**

- In all test cases the DUT should receive the test sequence without errors.

**Possible Problems:** None.

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**Test 2.3.7 – HS-RX Common-Mode Interference Beyond 450MHz ( $\Delta V_{CMRX(HF)}$ )**

**Purpose:** To verify that the DUT's HS receiver is capable of tolerating worst-case common-mode interference for frequencies greater than 450MHz, with amplitudes as high as the maximum required limit ( $\Delta V_{CMRX(HF)}$ ).

**References:**

- [1] D-PHY Specification, Section 8.2.1, Line 1462
- [2] Ibid, Section 8.2.1, Table 21

**Resource Requirements:** See Appendix A.2.

**Last Modification:** October 17, 2008

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $\Delta V_{CMRX(HF)}$ , which specifies the ability of a High-Speed receiver to tolerate and reject common-mode interference above 450MHz, with defined amplitude levels.

The Specification states, “*The High-Speed receiver shall receive High-Speed data correctly while rejecting common-mode interference  $\Delta V_{CMRX(HF)}$  and  $\Delta V_{CMRX(LF)}$ .*”[1]

(Note the procedure for this test is nearly identical to the previous  $\Delta V_{CMRX(HF)}$  Test 2.3.6, except that a different common mode disturber frequency range is used.)

While the D-PHY specification does not specify an upper bound on the frequency range for  $\Delta V_{CMRX(HF)}$ , a value of 1.33GHz will be used. (See comments in Discussion of Test 2.1.7 regarding the use of 1.33GHz as the maximum interference frequency.)

This test also uses the same test cases as the  $\Delta V_{CMRX(LF)}$ , test (See 2.3.6), in terms of differential and common mode combinations for the test signal, as well as the amplitude of the sinusoidal disturber. The only difference is the disturber frequency range is swept from 450MHz to 1330MHz (using no greater than 10MHz steps.)

**Test Setup:** See Appendix B.2.

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to generate a suitable HS test pattern with the common mode and differential voltage levels specified for Test Case #1 (see Table 2.3.6-1, in Test 2.3.6), for all Clock and Data Lanes. (Leave the sinusoidal common mode disturber signal disabled for this step.)
- Transmit the test sequence to the DUT.
- Verify (via any valid observable) that the DUT received the test sequence without errors.
- Enable the sinusoidal common mode disturber signal with a frequency of 450MHz, and amplitude of 50mVpk.
- Verify that the DUT can still receive the test sequence without errors.
- Slowly sweep the sinusoidal common mode disturber frequency between 450 and 1330MHz, in increments no wider than 10MHz. For all frequencies, verify that the DUT can still receive the test sequence without errors.
- Repeat the previous six steps for Test Cases 2 though 5.

**Observable Results:**

- In both test cases the DUT should receive the test sequence without errors.

**Possible Problems:** None.

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**Test 2.3.8 – HS-RX Setup/Hold and Jitter Tolerance**

**Purpose:** To verify that the DUT can tolerate signaling with worst-case timing error between the Clock and Data Lane signals.

**References:**

- [1] D-PHY Specification, Section 9.2.1, Line 1612
- [2] Ibid, Section 9.2.1, Table 27
- [3] D-PHY Specification, Section 9.2.1, Line 1615

**Resource Requirements:** See Appendix A.2.

**Last Modification:** October 14, 2008

**Discussion:**

Section 9 of the D-PHY Specification defines the High Speed Data-Clock Timing requirements for D-PHY products. Included in these specifications are requirements for the minimum Data-to-Clock Setup and Hold times an HS receiver must support.

Note that the timing specifications for D-PHY receivers are specified differently than the typical RX jitter tolerance requirements used in other high-speed serial standards. This is mainly due to the fact that D-PHY signaling does not use an embedded clock reference, but rather a dedicated external clock reference signal. Hence, the requirements are specified in terms of the data-to-clock setup and hold times, rather than a peak-to-peak jitter specification.

The specification states: “*The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.*”[1]

The specification also defines the minimum RX setup and hold values in the table of data-clock timing requirements ([2]), reproduced below:

**Table 27 Data-Clock Timing Specifications**

Parameter	Symbol	Min	Typ	Max	Units	Notes
Data to Clock Skew [measured at transmitter]	T <sub>SKEW[TX]</sub>	-0.15		0.15	UI <sub>INST</sub>	1
Data to Clock Setup Time [receiver]	T <sub>SETUP[RX]</sub>	0.15			UI <sub>INST</sub>	2
Clock to Data Hold Time [receiver]	T <sub>HOLD[RX]</sub>	0.15			UI <sub>INST</sub>	2

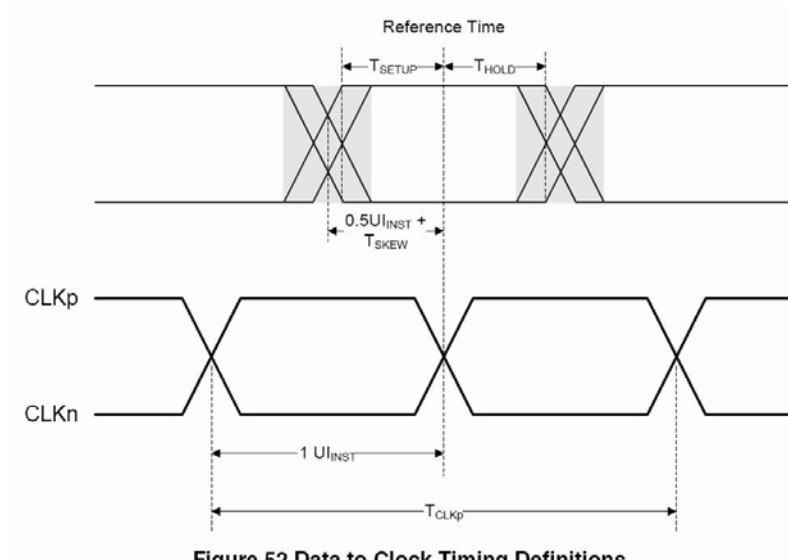
Notes:

1. Total silicon and package delay budget of 0.3\*UI<sub>INST</sub>
2. Total setup and hold window for receiver of 0.3\*UI<sub>INST</sub>

**Figure 2.3.8-1: HS-RX Data-Clock Setup and Hold Requirements**

Note that the setup (T<sub>SETUP</sub>) and hold (T<sub>HOLD</sub>) values are also pictured graphically in the spec, reproduced in the figure below:

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**Figure 52 Data to Clock Timing Definitions**

**Figure 2.3.8-2: Setup and Hold Windows**

The 0.15UI values specified as the minimum RX setup and hold times correspond to a 0.3UI horizontal “eye opening” at the receiver (as mentioned in note 2 under the table above.) Note this also can be viewed as 0.7UI of “eye closure”, if considered in terms of the peak-to-peak timing error. This 0.7UI value is derived from the sum of the worst case skew allowed for a bare transmitter ( $+/- 0.15 = 0.3\text{UI}$ ), plus an additional 0.4UI allowed for degradation contributed by the interconnect (see [3]).

While the specification defines the minimum setup/hold window at the RX, it does not specify any additional requirements for how these parameters are to be tested, and specifically how the minimum setup and hold times should be created. Given that, there are multiple ways this test could be implemented:

Ultimately, the specification is defining the minimum data-to-clock timing difference between the Clock Lane signal edges, and the quadrature-shifted Data Lane signal edges. From one perspective, these requirements could be tested by introducing a static offset (i.e., skew) between the Clock and Data Lane signals, using very clean signals from a reference generator, and slowly increasing the clock-to-data phase offset in the positive and negative directions until the receiver begins to indicate errors. In this case, the setup/hold values for all bits in the received data stream would be varied by the same amount, via the static offset. The phase of the Clock Lane relative to the Data Lane could be varied in small incremental steps, starting from a nominal offset of 0.5UI (i.e., 90-degree offset), and advanced to 0.85UI (i.e.,  $0.5 + 0.35\text{UI}$ ), and also retarded to 0.15UI ( $0.5 - 0.35\text{UI}$ ). A conformant HS receiver would be required to demonstrate error-free operation over this entire range. (Note these limits may also be exceeded for informative purposes until the DUT begins to indicate errors, in order to determine the amount of additional margin.)

Note that the procedure described above could be problematic if the receiver were to possess an ability to automatically adjust/compensate for a static phase offset between the Clock and Data Lane signals. (Note it is not currently known if any D-PHY transceivers actually implement such capability.) In such a hypothetical situation, the receiver could potentially demonstrate error-free operation well beyond the  $+/-0.35\text{UI}$  offset values, when the timing offset is a static fixed value. It is hypothetically possible that in these cases different behavior may be exhibited by the receiver if the setup and hold values are varied dynamically in time. A test in which the setup and hold windows are modulated to the max/min limits in a dynamic fashion would verify a receiver’s ability to tolerate short-term, transient occurrences of the minimum setup/hold conditions, more akin to the jitter/noise conditions occurring in a real-world environment.

In this test, both of the test methodologies described above will be performed in two separate procedures, first with a normative ‘static’ offset test, followed by a separate informative ‘jitter-tolerance-like’ dynamic test. Test

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signals will be applied at the DUT receiver inputs, and the ability for the DUT to properly receive these signals will be monitored via one of several possible observable mechanisms, depending on the DUT type. (For a complete discussion of RX test observables for different DUT types, see Appendix G).

Given that the former ‘static’ offset methodology is technically sufficient to validate the requirements of the specification as written, the first procedure will determine the ‘static’ setup and hold window limits for the DUT. The static data-clock timing offset will be advanced and retarded from the nominal 0.5UI phase offset, to the points where the DUT begins to indicate errors in the received data. Note that a low BER will not be used as the test metric in this case, but rather the threshold will be measured as the first point at which an error is observed (which is roughly equivalent to specifying a relatively high BER threshold, e.g., 1E-3). If the points at which the DUT begins to indicate errors are greater than the -0.35 and +0.35UI values (relative to 0.5UI), the results for the setup and hold requirements will be considered conformant, respectively.

Because there may be additional interest in verifying the RX timing requirements under more “real-world” dynamic conditions, a second test procedure will be performed, where the timing window will be modulated dynamically in time within the -0.35 to +0.35UI limits, and the test will be run for a significantly longer duration, to verify a much lower BER (1E-12), with a certain statistical confidence level (95%). (Note: See Appendix F of this document for a discussion of the statistical BER verification methodology.) This informative procedure is intended to approximate a more traditional receiver jitter tolerance test, however it is worth noting that the D-PHY methodology is not exactly equivalent, primarily due to the fact that the ‘jitter’ in the D-PHY methodology will not include a random (RJ) component, but will rather consist entirely of bounded deterministic jitter (DJ) distributed between the +/- 0.35UI limits.

(Editor’s Note: The exact composition of the DJ is not defined here, and may not be tightly specified, as given the fact that there is no RX PLL in D-PHY transceivers, there is no need to specify whether or not the DJ is Sinusoidal, PJ, DCD, etc, and with what frequency content. The peak-to-peak value is the really the primary significant factor that needs to be specified, and not strictly defining any further requirements allows for a variety of implementations across different test platforms. See comments below however regarding jitter distribution.)

From a test design standpoint, it is desirable to consider what the ‘worst-case’ test conditions would be when choosing the test stimulus signals. While the frequency content of the clock-to-data timing error (jitter) should not matter for D-PHY receivers, it is possible to argue that a more stressful jitter distribution would be biased more toward the peak-to-peak limits (with a majority of the jitter at or near the peak limits), rather than a truncated Gaussian, or other distribution weighted more toward the mean.

With this rationale, one possible candidate for a ‘worst case’ setup/hold test stimulus would be a pair of signals whose clock-to-data timing error oscillates back and forth between the two extreme limits for each bit of the data signal. (This is also referred to as Duty Cycle Distortion (DCD), and represents the highest frequency of deterministic jitter possible in a 2-level NRZ signal.) The probability distribution of pure DCD looks like two delta functions at the positive and negative extremes. This type of jitter is relatively easy to generate digitally, by varying the duty cycle of the pulse/signal source used to generate the test stimulus. Other instruments may incorporate delay lines, which allow for dynamic modulation of the signal edges according to an external signal applied to the delay line input. In these cases, inherent bandwidth limitations of the delay lines prevent very high frequency jitter/DCD from being generated, but they can allow random, pseudo-random, sinusoidal, and other lower-frequency distributions to be generated.

Currently, the suggested methodology for creating a ‘worst-case’ jitter stimulus signal would be to allocate as much of the peak-to-peak budget to DCD as possible, and possibly supplement any additional jitter with pseudo-random Bounded Uncorrelated Jitter (BUJ), via delay line modulation.

Also, for both test methodology procedures it will be useful to perform multiple test cases, with different HS differential amplitude values. While the argument can be made that the ‘worst case’ test conditions should include minimum setup/hold windows and minimum differential amplitude, an additional control case will be performed at nominal differential HS amplitude (and maximum jitter), to determine whether or not amplitude sensitivity is the dominant factor in cases where the DUT exhibits failures during the min amplitude/max jitter test

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case. If the DUT also shows failures with a nominal differential amplitude, this will imply that the dominant factor is a sensitivity to RX setup/hold times.

**Test Setup:** See Appendix B.2.

**Test Procedure I (Static Method, Normative):**

- Connect the DUT to the Test System.
- Configure the RX Test Signal Source to transmit signaling to the DUT with an HS differential amplitude of 140mVpp, an HS common-mode amplitude of 200mV, and an HS Data-to-Clock phase offset calibrated to a nominal 0.5UI value for all Data Lanes.
- Verify (using any valid observable for the given DUT type) that the DUT is able to successfully decode the received HS data stream error-free.
- Advance the phase of the Clock Lane signal relative to the Data Lane (effectively decreasing the  $T_{HOLD}$  time) until the point is reached where the DUT begins to indicate errors in the received data stream.
- Record the maximum Clock Lane phase offset for which the DUT was observed to run error-free. (This value represents the minimum valid  $T_{HOLD}$  value for the DUT.)
- Repeat the previous 4 steps, but instead retard the phase of the Clock Lane signal relative to the Data Lane (effectively decreasing the  $T_{SETUP}$  time), to determine the minimum valid  $T_{SETUP}$  value for the DUT.
- Repeat the previous 5 steps, but instead calibrate the RX Test Signal Source to use an HS differential amplitude of 400mVpp (rather than 140mVpp).

**Observable Results I:**

- (140mVpp amplitude case): Verify that the minimum valid  $T_{HOLD}$  value for the DUT is less than 0.15UI.
- (140mVpp amplitude case): Verify that the minimum valid  $T_{SETUP}$  value for the DUT is less than 0.15UI.
- (400mVpp amplitude case): Verify that the minimum valid  $T_{HOLD}$  value for the DUT is less than 0.15UI.
- (400mVpp amplitude case): Verify that the minimum valid  $T_{SETUP}$  value for the DUT is less than 0.15UI.

**Test Procedure II (Dynamic Method, Informative):**

- Connect the DUT to the Test System.
- Configure the RX Test Signal Source to transmit signaling to the DUT with an HS differential amplitude of 140mVpp, an HS common-mode amplitude of 200mV, and an HS Data-to-Clock phase offset calibrated to a nominal 0.5UI value for all Data Lanes.
- Verify (using any valid observable for the given DUT type) that the DUT is able to successfully decode the received HS data stream error-free.
- Enable jitter generation on the RX Test Signal Source, such that the calibrated peak-to-peak Clock-to-Data Lane jitter is 0.7UI (i.e., +/-0.35UI) on all Data Lanes.
- Run the test for a sufficiently long duration in order to verify a BER of 1E-12 with a statistical confidence level of 95% or greater (see Appendix F), and record the number of errors observed.
- (Optional): If the DUT shows no errors during the previous step, repeat the previous 2 steps with higher peak-to-peak jitter values, until the DUT is observed to show errors.
- Repeat the previous 5 steps, but instead calibrate the RX Test Signal Source to use an HS differential amplitude of 400mVpp (rather than 140mVpp).

**Observable Results II:**

- For all observed test cases, if the DUT indicates zero errors, it can be concluded that a target BER of 1E-12 has been verified for the DUT with a confidence level of 95%.

**Possible Problems:** Note that during any long-duration BER test, spurious signals from nearby RF sources (e.g., cell phones, microwave ovens, etc) can potentially cause unintended intermittent bursts of errors. Care should be taken to minimize the impact of stray RF sources in close proximity to the test setup.

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## **GROUP 4: HS-RX TIMER REQUIREMENTS**

**Overview:**

This group of tests verifies various High-Speed RX timer requirements defined in multiple Sections of the D-PHY Specification.

**Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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### Test 2.4.1 – Data Lane HS-RX $T_{D\text{-TERM-EN}}$ Value

**Purpose:** To verify that the time required for the DUT’s Data Lane receiver to enable its HS line termination ( $T_{D\text{-TERM-EN}}$ ) is within the conformance limits.

#### References:

- [1] D-PHY Specification, Section 5.14.2, Line 1038
- [2] Ibid, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

#### Discussion:

As part of the process for switching the HS Clock Lane out of LP mode, the D-PHY Specification provides a specification for the time required for the Slave to enable its HS Data line termination before the Master enables the HS differential data signal. (Note this test is only applicable to Slave DUTs).

The specification states, “ $T_{D\text{-TERM-EN}}$  is the time to enable Data Lane receiver line termination measured from when  $D_n$  crosses  $V_{IL,\text{MAX}}$ .” [1]. This interval is shown in the figure below.

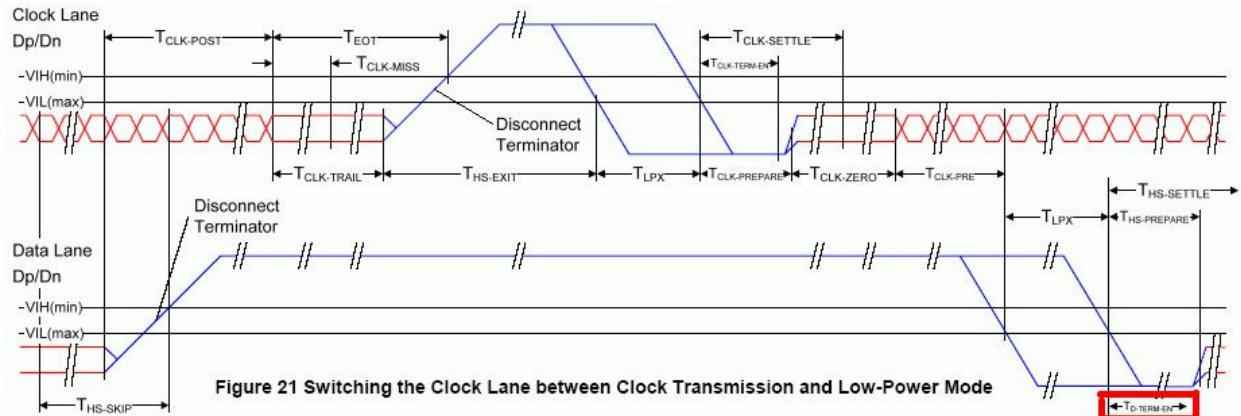


Figure 2.4.1-1:  $T_{D\text{-TERM-EN}}$  Interval

In this test, the Test System will emulate a Master device, and initiate an HS Request sequence on the Data Lane. The  $T_{D\text{-TERM-EN}}$  interval begins at the point where the Data Lane LP-00 falling edge (Dn) crosses  $V_{IL,\text{MAX}}$  (550mV), and ends at the point when the HS line termination is enabled.

Note that the exact point when the HS line termination is considered “enabled” can be somewhat subjective in some cases, as the voltage spike that typically occurs on the line when the termination is enabled does not necessarily have a well-defined shape (and in some cases may not be visible at all). For the purposes of this test, the measurement point for the termination-enable voltage spike is defined as the maximum voltage point of the spike (as opposed to the ‘start’ of the spike, which can be even more difficult to clearly identify.) For devices with sufficient margin in their  $T_{D\text{-TERM-EN}}$  timer values, the impact of any potential measurement uncertainty should be minimal.

The measured duration of  $T_{D\text{-TERM-EN}}$  should be greater than the time required for Dn to reach 450mV (i.e.,  $V_{TERM-EN}$ ) and less than  $(35\text{ns} + 4\text{*UI}) \text{ ns}$  [2].

**Test Setup:** This test uses a hybrid test setup. The DUT is connected to the RX Test System in the same manner as the other HS-RX tests (see Appendix B.2), however the DUT behavior is observed by using a DSO to probe the signaling at the DUT, in a manner similar to the TX test setup shown in Appendix B.1.2.

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**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to emulate a Master device.
- Initiate an HS Request sequence on the DUT's Data Lane 0, and capture the exchange using the DSO.
- Measure  $T_{D\text{-TERM-EN}}$ , as described above.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

**Observable Results:**

- For all Data Lanes, verify that  $T_{D\text{-TERM-EN}}$  is greater than the time for  $D_n$  to reach 450mV, and less than  $(35\text{ns} + 4\text{*UI}) \text{ ns}$ .

**Possible Problems:** None.

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**Test 2.4.2 – Data Lane HS-RX  $T_{HS-PREPARE} + T_{HS-ZERO}$  Tolerance**

**Purpose:** To verify that the DUT's Data Lane HS receiver can tolerate reception of conformant values for  $T_{HS-PREPARE} + T_{HS-ZERO}$ .

**References:**

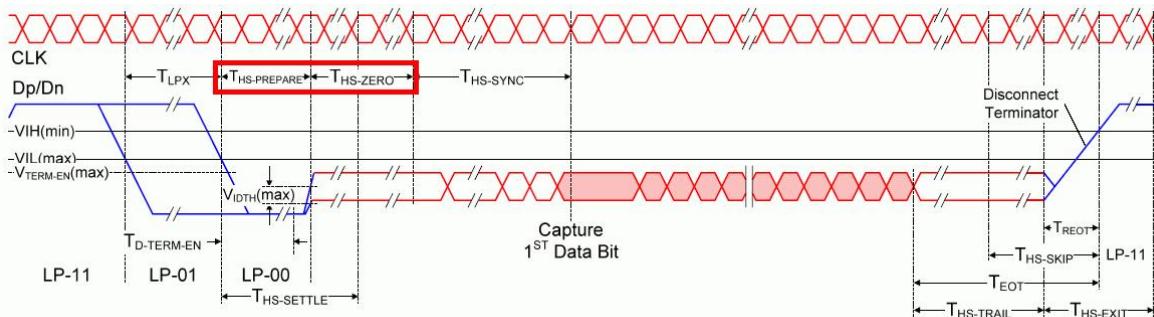
- [1] D-PHY Specification, Section 5.9, Lines 976 + 977
- [2] Ibid, Section 5.9, Line 966

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

As part of the process for switching the Data Lane into HS mode, the D-PHY specification includes requirements for the  $T_{HS-PREPARE}$  and  $T_{HS-ZERO}$  intervals, which are shown in the figure below.



**Figure 14 High-Speed Data Transmission in Bursts**

**Figure 2.4.2-1:  $T_{HS-PREPARE} + T_{HS-ZERO}$  Intervals**

Note that the D-PHY specification defines timing parameters as being either transmitter-specific or receiver-specific[1], and  $T_{HS-PREPARE}$  and  $T_{HS-ZERO}$  are defined as transmitter-specific parameters.

However, the specification also contains a requirement that states, “*Also note that while corresponding receiver tolerances are not defined for every transmitter-specific parameter, receivers shall also support reception of all allowed conformant values for all transmitter-specific timing parameters in Table 14 for all HS UI values up to, and including, the maximum supported HS clock rate specified in the receiver’s datasheet.*”[2]. While the transmitter requirements for  $T_{HS-PREPARE}$  and  $T_{HS-ZERO}$  are verified in separate tests in this test suite, this test will verify whether or not a receiver is capable of tolerating conformant values (and combinations of values) for  $T_{HS-PREPARE}$  and  $T_{HS-ZERO}$ .

The TX conformance range for  $T_{HS-PREPARE}$  is defined as 40ns+4\*UI to 85ns+6\*UI. The lower bound for the TX conformance range for  $T_{HS-PREPARE} + T_{HS-ZERO}$  is defined as 145ns+10\*UI (note that no upper limit is defined.) In this test, HS bursts containing valid image data will be sent to the DUT using different conformant values of  $T_{HS-PREPARE}$  and  $T_{HS-ZERO}$ .

Several test cases will be performed, using combinations of the maximum, minimum, and nominal TX values. The test cases are listed in the table below.

Also, note that all other timing parameters (e.g.,  $T_{HS-TRAIL}$ ,  $T_{CLK-PREPARE/TRAIL}$ ) should be set to nominal values for this test. (Note that exact values are not specified here for all parameters, as flexibility is allowed to choose these values according to potential timing needs of the DUT. All values should be chosen to include sufficient margin from their respective conformance limits.)

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**Table 2.4.2-1: HS Receiver  $T_{HS-PREPARE}$  +  $T_{HS-ZERO}$  Test Cases**

Case #	$T_{HS-PREPARE}$	$T_{HS-ZERO}$	$T_{HS-PREPARE} + T_{HS-ZERO}$	Notes
1	60ns + 4*UI	100ns + 6*UI	160ns + 10*UI	Nominal $T_{HS-PREPARE}$ and nominal $T_{HS-PREP+ZERO}$ . (Control case)
2	40ns + 4*UI	120ns + 6*UI	160ns + 10*UI	Minimum $T_{HS-PREPARE}$ and nominal $T_{HS-PREP+ZERO}$ .
3	40ns + 4*UI	105ns + 6*UI	145ns + 10*UI	Minimum $T_{HS-PREPARE}$ and minimum $T_{HS-PREP+ZERO}$ .
4	85ns + 6*UI	75ns + 4*UI	160ns + 10*UI	Maximum $T_{HS-PREPARE}$ and nominal $T_{HS-PREP+ZERO}$ .
5	85ns + 6*UI	60ns + 4*UI	145ns + 10*UI	Maximum $T_{HS-PREPARE}$ and minimum $T_{HS-PREP+ZERO}$ .

(Key: **Red** = Spec TX minimum, **Green** = Nominal TX value, **Blue** = Spec TX maximum)

For all test cases, the DUT must successfully receive the HS data without error in order to be considered conformant.

**Test Setup:** This test uses a hybrid TX/RX test setup. See Test Setup of Test 2.4.1 (which uses the same setup).

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to transmit an otherwise valid HS image data sequence to the DUT, using the  $T_{HS-PREPARE}$  +  $T_{HS-ZERO}$  Test Case #1 values as described above.
- Verify that the DUT successfully received the HS image data without error.
- Repeat the previous two steps for Test Cases #2 through #5.

**Observable Results:**

- For all test cases, verify that the DUT successfully received the HS burst data without error.

**Possible Problems:** None.

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### Test 2.4.3 – Data Lane HS-RX $T_{HS\text{-SETTLE}}$ Value

**Purpose:** To verify that the DUT's Data Lane receiver incorporates a sufficient timeout interval ( $T_{HS\text{-SETTLE}}$ ) to ignore transition effects that may occur during the HS Entry sequence.

#### References:

- [1] D-PHY Specification, Section 5.9, Table 14
- [2] Ibid, Section 5.4.2, Table 3 (Line 789)

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

#### Discussion:

As part of the process of receiving an HS Data Burst, the D-PHY Specification provides a requirement for a timeout period at the beginning of an HS burst sequence, which allows the Data Lane HS-RX to ignore any potential transition effects of the SoT sequence. This interval is defined as  $T_{HS\text{-SETTLE}}$ , and is shown in the figure below.

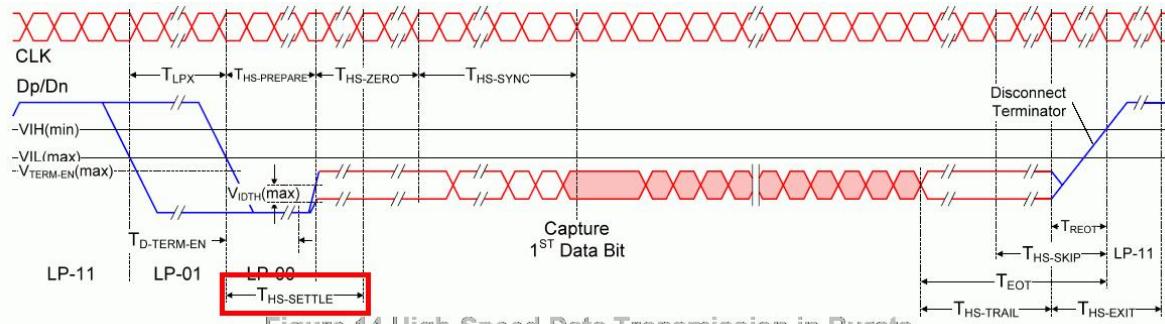


Figure 14 High-Speed Data Transmission in Bursts

Figure 2.4.3-1:  $T_{HS\text{-SETTLE}}$  Timeout Interval

The specification defines  $T_{HS\text{-SETTLE}}$  as the, “Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of  $T_{HS\text{-PREPARE}}$ .” [1].

The conformance range for  $T_{HS\text{-SETTLE}}$  is defined as  $85ns+6*UI$  to  $145ns+10*UI$ . This implies that all conformant devices shall ignore all Data Lane HS transitions for a period of  $85ns+6*UI$  after the start of  $T_{HS\text{-PREPARE}}$ . Devices may ignore Data Lane transitions for window lengths between  $85ns+6*UI$  to  $145ns+10*UI$ , and all devices shall not ignore Data Lane transitions for window lengths of  $145ns+10*UI$  and greater. (Note that  $145ns+10*UI$  is the minimum valid TX conformance value for  $T_{HS\text{-PREPARE}} + T_{HS\text{-ZERO}}$ . Therefore, because this is the minimum time that a conformant transmitter could be expected to wait before sending an HS Sync Sequence, this in turn determines the upper limit on the window during which a receiver is allowed to ignore HS Data Lane transitions.)

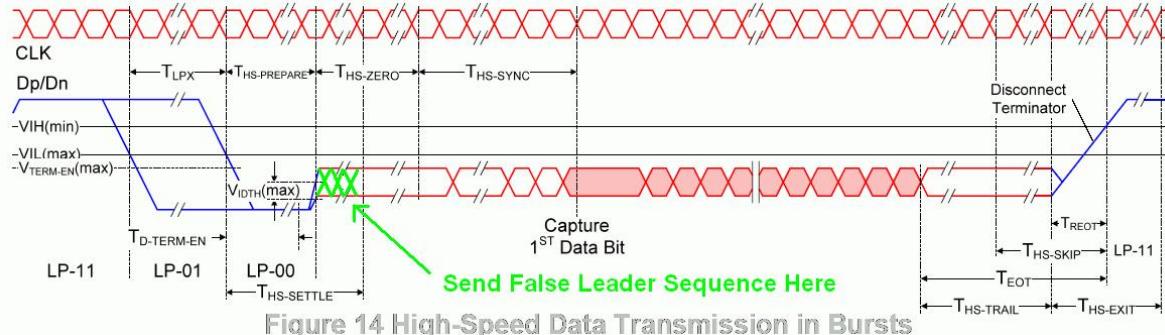
The methodology for this test involves sending HS burst sequences containing valid minimum-length  $T_{HS\text{-PREPARE}}$  intervals ( $40ns+4*UI$ ), followed by a valid minimum-length  $T_{HS\text{-ZERO}}$  ( $105ns+6*UI$ ). However at the beginning of  $T_{HS\text{-ZERO}}$ , an additional HS data byte containing the pattern 01110100 will be inserted in place of the first 8\*UI of  $T_{HS\text{-ZERO}}$ . This pattern contains the ‘Leader Sequence’, 011101, which is defined by the specification as the specific bit sequence that the receiver looks to detect and uses to establish synchronization at the beginning of an HS burst [2]. (Note that the Leader Sequence (011101) is different from the Sync Sequence (00011101), as the two terms are defined and used separately in the specification. The Sync Sequence is used with respect to the HS transmitter, and is the pattern that is transmitted following the end of the  $T_{HS\text{-ZERO}}$  interval. The Leader Sequence is used with respect to the HS receiver, and is the bit pattern that the receiver must detect in order to establish synchronization.)

The position of the ‘False Leader Sequence’ byte can be varied within the  $T_{HS\text{-SETTLE}}$  window by adding additional HS-0 bits before the byte (and deleting HS-0 bits after it), which will keep the  $T_{HS\text{-PREPARE}} + T_{HS\text{-ZERO}}$  length constant. (Note that the beginning of the False Leader Sequence is defined for the purposes of this test as the zero crossing time of the HS Clock rising edge that corresponds to the first ‘0’ in the 01110100 pattern.) Following  $T_{HS\text{-PREPARE}} + T_{HS\text{-ZERO}}$ , a valid Sync Sequence byte (00011101) and valid image data packet will be sent. A conformant DUT should ignore the False Leader Sequence for this initial test sequence, and properly detect the subsequent valid Sync Sequence, receiving the HS image data packet without error.

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If the DUT does detect the False Leader Sequence (due to it falling outside of the DUT's  $T_{HS\text{-SETTLE}}$  window), the HS image data packet will be received and decoded with incorrect synchronization, which will cause errors in the received image data.

The figure below shows the location of the False Leader Sequence in the overall HS burst. (Note that in the diagram below, the False Leader Sequence is not drawn to scale):



**Figure 2.4.3-2:  $T_{HS\text{-SETTLE}}$  Test Sequence, with False Leader Sequence**

The False Leader Sequence will be positioned starting at  $40\text{ns}+4*\text{UI}$  (i.e., following the minimum-length  $T_{HS\text{-PREPARE}}$ ), and will be incrementally moved forward in  $1*\text{UI}$  intervals until errors are observed in the received image data. If the point at which errors begin to occur is greater than  $85\text{ns}+6*\text{UI}$ , the DUT will be considered conformant.

(Note that in order to reduce test time, each individual Data Lane will not be tested separately for this test, and the addition of the False Leader Sequence described above will be applied to all Data Lanes simultaneously. Note however that it is technically possible to test each Data Lane individually if desired, by only adding the False Leader Sequence byte to a single Data Lane, and using a dummy byte of 00000000 on all other Data Lanes, in order to preserve timing consistency.)

**Test Setup:** This test uses a hybrid TX/RX test setup. See Test Setup of Test 2.4.1 (which uses the same setup).

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test Setup to transmit a valid image data sequence to the DUT, which uses a  $T_{HS\text{-PREPARE}}$  value of  $40\text{ns}+4*\text{UI}$ , and contains a False Leader Sequence byte at the start of  $T_{HS\text{-ZERO}}$  as described above.
- Verify that the image data is properly received by the DUT without error (via any valid observable means).
- Advance the position of the False Leader Sequence byte forward by adding one HS-0 UI before the False Leader Sequence, and removing one HS-0 UI after the False Leader Sequence, and transmit the updated sequence to the DUT.
- Observe whether or not the DUT receives the image data without error.
- Repeat the following two steps until the DUT begins to show errors in the received image data.
- Record the final  $T_{HS\text{-SETTLE}}$  result as the maximum value for which the DUT was able to receive the image data *without* errors.

**Observable Results:**

- Verify that  $T_{HS\text{-SETTLE}}$  is greater than  $85\text{ns} + 6*\text{UI}$ .

**Possible Problems:** None.

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**Test 2.4.4 – Data Lane HS-RX  $T_{HS-TRAIL}$  Tolerance**

**Purpose:** To verify that the DUT's Data Lane HS receiver can tolerate reception of conformant values for  $T_{HS-TRAIL}$ .

**References:**

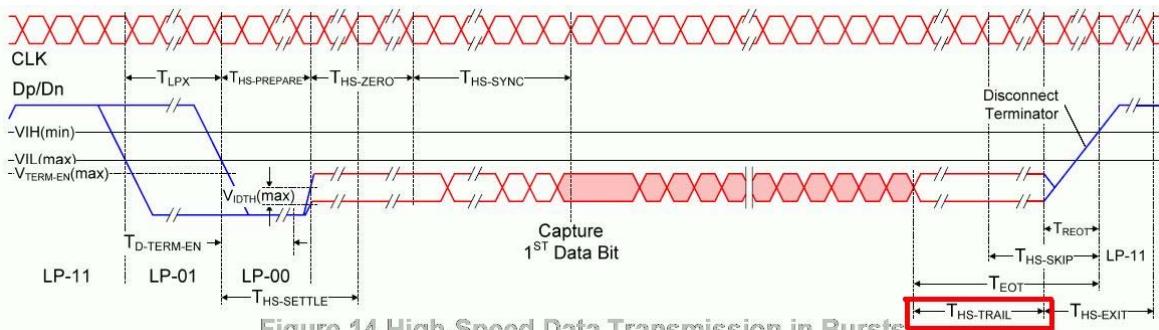
- [1] D-PHY Specification, Section 5.9, Lines 976 + 977
- [2] Ibid, Section 5.9, Line 966

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

As part of the process for switching the Data Lane out of HS mode, the D-PHY specification includes requirements for the  $T_{HS-TRAIL}$  interval, which is shown in the figure below.



**Figure 14 High-Speed Data Transmission in Bursts**

**Figure 2.4.4-1:  $T_{HS-TRAIL}$  Interval**

Note that the D-PHY specification defines timing parameters as being either transmitter-specific or receiver-specific[1], and  $T_{HS-TRAIL}$  is defined as a transmitter-specific parameter.

However, the specification also contains a requirement that states, “*Also note that while corresponding receiver tolerances are not defined for every transmitter-specific parameter, receivers shall also support reception of all allowed conformant values for all transmitter-specific timing parameters in Table 14 for all HS UI values up to, and including, the maximum supported HS clock rate specified in the receiver’s datasheet.*”[2]. While the transmitter requirements for  $T_{HS-TRAIL}$  are verified in a separate test in this test suite, this test will verify whether or not a receiver is capable of tolerating values for  $T_{HS-TRAIL}$  across the entire TX conformance range.

The lower limit for the TX conformance range of  $T_{HS-TRAIL}$  is defined as  $(60\text{ns} + 4*\text{UI})$ . (Note this is always the case for the Forward direction, see comments in Test 1.3.13 Discussion.) An upper bound on  $T_{HS-TRAIL}$  is not explicitly defined, however an implicit upper limit is imposed by the  $T_{EOT}$  specification (which is the sum of the  $T_{HS-TRAIL}$  and  $T_{REOT}$  intervals, and has an upper limit of  $105\text{ns} + 12*\text{UI}$ ). Therefore, a practical TX upper limit for  $T_{HS-TRAIL}$  would be  $(105\text{ ns} + 12*\text{UI})$  minus  $T_{REOT}$  for the respective transmitter (which is required to be less than 35ns, as defined by the  $T_{REOT}$  requirements, see Test 1.3.14). In order to simplify the test procedure and remove any dependence on the actual  $T_{REOT}$  of the test setup, two upper limit test cases will be performed, one normative case assuming the maximum allowed  $T_{REOT}$  of 35ns, and a second informative case where  $T_{REOT}$  is assumed to be 0ns.

Also, note that all other timing parameters (e.g.,  $T_{HS/CLK-PREPARE}$ ,  $T_{HS/CLK-ZERO}$ , etc) should be set to nominal values for this test. (Note that exact values are not specified here for all parameters, as flexibility is allowed to choose these values according to potential timing needs of the DUT. All values should be chosen to include sufficient margin from their respective conformance limits.)

Four total test cases for  $T_{HS-TRAIL}$  will be performed (starting with a nominal  $T_{HS-TRAIL}$  case, for control purposes), which are listed in the table below.

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**Table 2.4.4-1: HS Receiver  $T_{HS-TRAIL}$  Test Cases**

Case #	$T_{HS-TRAIL}$	Notes
1	<b>80ns + 4*UI</b>	Nominal $T_{HS-TRAIL}$ (Control case)
2	<b>60ns + 4*UI</b>	Minimum $T_{HS-TRAIL}$
3	<b>70ns + 12*UI</b>	Maximum $T_{HS-TRAIL}$ (Assuming $T_{REOT} = 35\text{ns}$ )
4	<b>105ns + 12*UI</b> (Informative)	Maximum $T_{HS-TRAIL}$ (Assuming $T_{REOT} = 0\text{ns}$ )

The general methodology for this test will be similar to that used for most of the other HS-RX tolerance tests (e.g., Test 2.4.2), whereby an otherwise valid HS image data sequence will be sent to the DUT, using the various test case values of  $T_{HS-TRAIL}$ , and the DUT will be observed to determine if the image data is received without error.

For all test cases, the DUT must successfully receive the HS image data without error in order to be considered conformant.

**Test Setup:** This test uses a hybrid TX/RX test setup. See Test Setup of Test 2.4.1 (which uses the same setup).

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to transmit an otherwise valid HS image data sequence to the DUT, using the  $T_{HS-TRAIL}$  Test Case #1 values as described above.
- Verify that the DUT successfully received the HS image data without error.
- Repeat the previous two steps for  $T_{HS-TRAIL}$  Test Cases #2, #3, and #4.

**Observable Results:**

- For all test cases, verify that the DUT successfully received the HS image data without error.

**Possible Problems:** None.

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**Test 2.4.5 – Data Lane HS-RX  $T_{HS-SKIP}$  Value**

**Purpose:** To verify that the DUT's Data Lane receiver incorporates a sufficient timeout interval ( $T_{HS-SKIP}$ ) to ignore transition effects that may occur during the EoT sequence.

**References:**

[1] D-PHY Specification, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.2.

**Last Modification:** September 16, 2010

**Discussion:**

As part of the process of completing a HS Data Transmission Burst, the D-PHY Specification provides a requirement for a timeout period at the end of an HS burst sequence, which allows the RX to ignore any potential transition effects of the EoT sequence. This interval is defined as  $T_{HS-SKIP}$ , and is shown in the figure below.

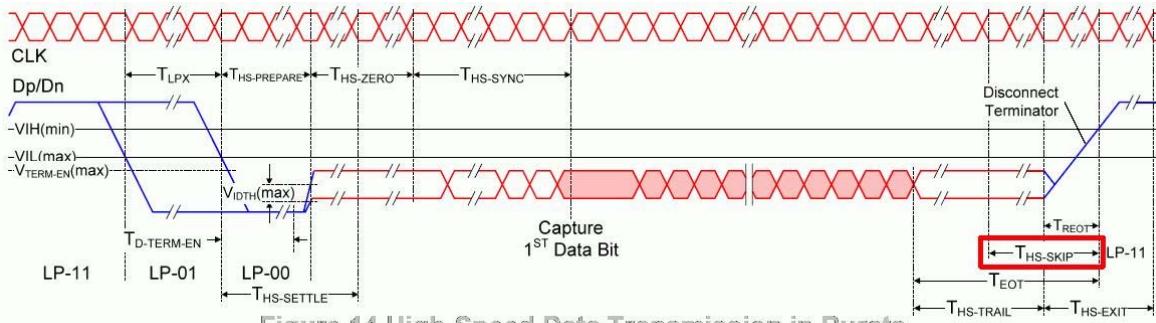


Figure 14 High-Speed Data Transmission in Bursts

Figure 2.4.5-1:  $T_{HS-SKIP}$  Timeout Interval

The specification defines  $T_{HS-SKIP}$  as the, “Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.” [1].

The methodology for this test involves sending HS burst sequences containing valid  $T_{HS-TRAIL}$  intervals, however following the  $T_{HS-TRAIL}$  interval, an additional HS data byte will be sent, before the transition to the LP-11 state occurs. The position of the additional HS data byte will be modified within the  $T_{HS-SKIP}$  window by adding additional HS bits after the extra byte (i.e., repeating the last HS bit of the extra byte) as needed to control the position of the first bit of the extra byte, relative to the point where the LP-11 rising edge crosses  $V_{IH,MIN}$  (880mV), (which is defined as the end of the  $T_{HS-SKIP}$  window).

The test sequence will use a minimum-length  $T_{HS-TRAIL}$  interval (which is defined as  $60\text{ns}+4*\text{UI}$ , see Test 1.3.13). Following this  $T_{HS-TRAIL}$  interval, an extra HS data byte will be added (01110100b, or 0x2E transmitted LSB first onto the wire) as the extra HS data pattern appearing on the line before the final LP-11 transition. (Note the 01110100b sequence above is specifically chosen as it begins with the HS Leader Sequence (011101b), which is relatively easy to identify for calibration purposes. Note also that this is the same pattern that is used for the  $T_{HS-SETTLE}$  measurement in Test 2.4.3.)

This initial sequence shall be sent to the DUT, and the DUT should ignore the extra data byte, and receive the HS packet data successfully.

From this point, additional HS-1 bits will be added after the extra data byte, such that the time measured from the first bit of the extra data byte, to the point where the  $T_{REOT}$  rising edge crosses 880mV is slowly increased. This interval is the  $T_{HS-SKIP}$  window, and all devices should successfully ignore the presence of the extra data byte for all  $T_{HS-SKIP}$  values up to 40ns (which is the  $T_{HS-SKIP}$  lower conformance limit).

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From here, the  $T_{HS-SKIP}$  interval will be increased beyond 40ns, at which point a receiver may still ignore the presence of the extra data byte. However, once the  $T_{HS-SKIP}$  interval is increased to 55ns + 4\*UI, conformant devices should show signs that the extra byte has NOT been ignored (which will typically result in some type of invalid functional behavior, however the exact behavior in this case is not clearly defined. This may be an ECC/CRC error, and/or other error detectable at the protocol level, e.g., any error contained in an Acknowledge and Error Report response for DSI devices.) However, note that because the observability of errored reception for these cases is not clearly defined and cannot be guaranteed for all devices, verification of the upper  $T_{HS-SKIP}$  limit will be considered informative for this test.

Note that for this test, each individual Data Lane will not be tested separately, and the timing modification sequence described above will be applied to all Data Lanes simultaneously. (This is done simply because the process needed to isolate each Lane separately, but still maintain all of the other timing requirements required by many RX devices (e.g. displays) would be a non-trivial task, and would require fairly complex sequences to be generated in many cases.)

Also, note that the D-PHY specification is not clear as to exactly where the  $T_{HS-SKIP}$  functionality is implemented in a given DUT. Therefore, it is possible that the detection and ignoring of post-burst bits may be implemented in the protocol layer logic for some DUT types. Therefore, if a DUT is not designed to contain this logic (e.g., for a bare-phy DUT with a PPI or other exposed protocol interface), this test is considered Not Applicable.

For this test, if the DUT ignores the presence of the extra data byte for  $T_{HS-SKIP}$  intervals up to and including 40ns, a passing result will be issued. Verification that the DUT does NOT ignore the presence of the extra data byte for  $T_{HS-SKIP}$  intervals greater than 55ns + 4\*UI will be considered informative.

**Test Setup:** This test uses a hybrid TX/RX test setup. See Test Setup of Test 2.4.1 (which uses the same setup).

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to transmit the initial  $T_{HS-SKIP}$  test sequence to the DUT, as described above.
- Verify that the DUT successfully ignored the presence of the extra data byte (by verifying that no errors were reported).
- Incrementally increase the number of HS-1 bits after the extra data byte, such that the time period from the first bit of the extra data byte to where the  $T_{REOT}$  rising edge crosses 880mV is incrementally increased to 40ns. For each increment, verify that the DUT continues to ignore the presence of the extra data byte, up to 40ns.
- (Optional, Informative): Continue to increase the  $T_{HS-SKIP}$  interval, up to and beyond 55ns + 4\*UI. Verify that at some point before 55ns + 4\*UI, the DUT does NOT ignore the extra data byte (as observed via the reporting of errors by the DUT via any observable mechanism, as described above).

**Observable Results:**

- Verify that the presence of the extra data byte does not negatively affect proper reception of data for  $T_{HS-SKIP}$  values up to and including 40ns.
- (Optional, Informative): Verify that the presence of the extra data byte does affect proper reception of data (via the observation of errors) for  $T_{HS-SKIP}$  values greater than (55ns + 4\*UI).

**Possible Problems:** None.

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### Test 2.4.6 – Clock Lane HS-RX $T_{CLK-TERM-EN}$ Value

**Purpose:** To verify that the time required for the DUT's Clock Lane receiver to enable its HS line termination ( $T_{CLK-TERM-EN}$ ) is within the conformance limits.

#### References:

[1] D-PHY Specification, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

#### Discussion:

As part of the process for switching the Clock Lane into HS mode, the D-PHY specification provides a requirement for the time required for a receiver to enable its Clock Lane HS line termination before transmission of the HS Clock begins. (Note this test is only applicable to Slave DUTs). This interval is defined as  $T_{CLK-TERM-EN}$ , and is shown in the figure below.

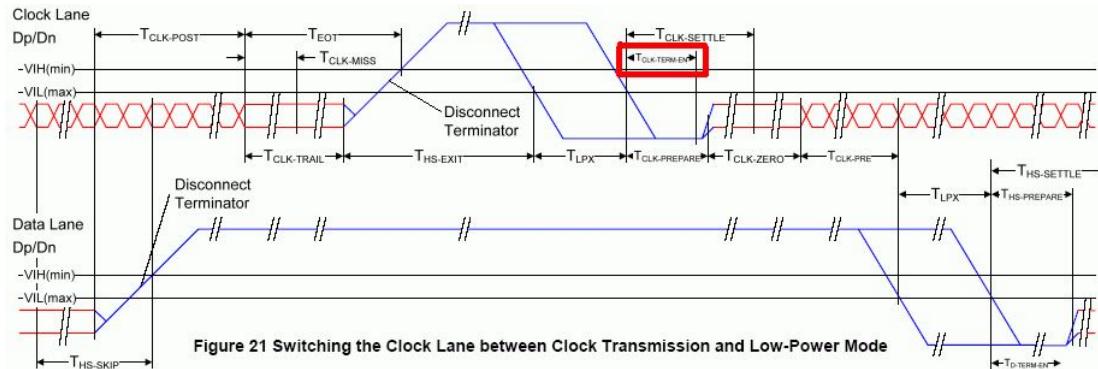


Figure 21 Switching the Clock Lane between Clock Transmission and Low-Power Mode

Figure 2.4.6-1:  $T_{CLK-TERM-EN}$  Interval

In this test, the Test System will emulate a Master device, and initiate an HS Request sequence on the Data Lane. The  $T_{CLK-TERM-EN}$  interval begins at the point where the Clock Lane LP-00 falling edge (Dn) crosses  $V_{IL,MAX}$  (550mV), and ends at the point when the HS line termination is enabled.

(See comments in Test 2.4.1 regarding measurement of the termination enable point. The same comments apply to this test.)

The measured duration of  $T_{CLK-TERM-EN}$  should be greater than the time required for Dn to reach 450mV (i.e.,  $V_{TERM-EN}$ ) and less than 38ns [1].

**Test Setup:** This test uses a hybrid TX/RX test setup. See Test Setup of Test 2.4.1 (which uses the same setup).

#### Test Procedure:

- Connect the DUT to the Test System.
- Configure the Test System to transmit an HS Request sequence on the DUT's Clock Lane, and capture the exchange using the DSO.
- Measure  $T_{CLK-TERM-EN}$ , as described above.

#### Observable Results:

- Verify that  $T_{CLK-TERM-EN}$  is greater than (the time for Dn to reach  $V_{TERM-EN}$ ), and less than 38ns.

**Possible Problems:** None.

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**Test 2.4.7 – Clock Lane HS-RX  $T_{CLK-PREPARE} + T_{CLK-ZERO}$  Tolerance**

**Purpose:** To verify that the DUT's Clock Lane HS receiver can tolerate reception of conformant values for  $T_{CLK-PREPARE} + T_{CLK-ZERO}$ .

**References:**

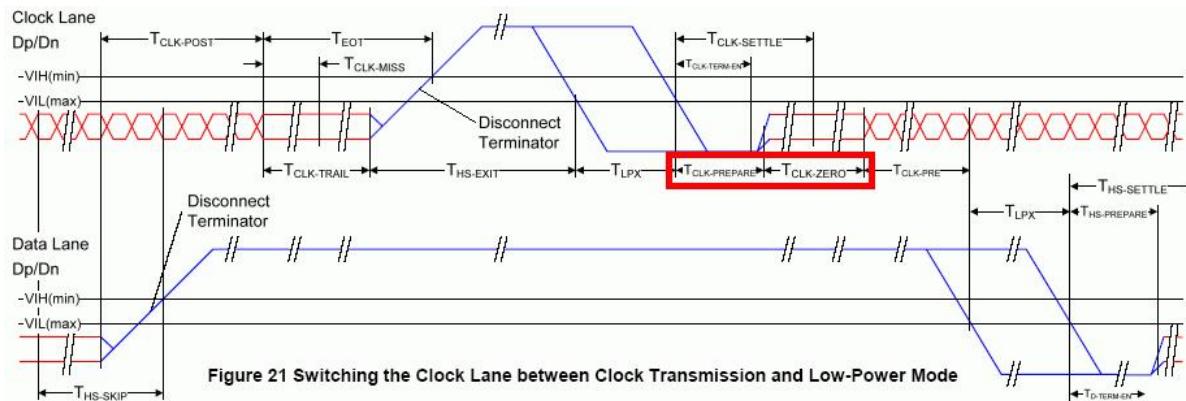
- [1] D-PHY Specification, Section 5.9, Lines 976 + 977
- [2] Ibid, Section 5.9, Line 966

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

As part of the process for switching the Clock Lane into HS mode, the D-PHY specification includes requirements for the  $T_{CLK-PREPARE}$  and  $T_{CLK-ZERO}$  intervals, which are shown in the figure below.



**Figure 2.4.7-1:  $T_{CLK-PREPARE} + T_{CLK-ZERO}$  Interval**

Note that the D-PHY specification defines timing parameters as being either transmitter-specific or receiver-specific[1], and  $T_{CLK-PREPARE}$  and  $T_{CLK-ZERO}$  are defined as transmitter-specific parameters.

However, the specification also contains a requirement that states, “*Also note that while corresponding receiver tolerances are not defined for every transmitter-specific parameter, receivers shall also support reception of all allowed conformant values for all transmitter-specific timing parameters in Table 14 for all HS UI values up to, and including, the maximum supported HS clock rate specified in the receiver’s datasheet.*”[2]. While the transmitter requirements for  $T_{CLK-PREPARE}$  and  $T_{CLK-ZERO}$  are verified in separate tests in this test suite, this test will verify whether or not a receiver is capable of tolerating conformant values (and combinations of values) for  $T_{CLK-PREPARE}$  and  $T_{CLK-ZERO}$ .

The TX conformance range for  $T_{CLK-PREPARE}$  is 38 to 95ns, and the specification for  $T_{CLK-PREPARE} + T_{CLK-ZERO}$  is defined as a minimum of 300ns. (No upper limit is defined). In this test, HS bursts containing valid image data will be sent to the DUT using different conformant values of  $T_{CLK-PREPARE}$  and  $T_{CLK-ZERO}$ .

Several test cases will be performed, using combinations of the maximum, minimum, and nominal TX values. The test cases are listed in the table below.

Also, note that all other timing parameters (e.g.,  $T_{HS-PREPARE/TRAIR}$ ,  $T_{CLK-TRAIL}$ ) should be set to nominal values for this test. (Note that exact values are not specified here for all parameters, as flexibility is allowed to choose these values according to potential timing needs of the DUT. All values should be chosen to include sufficient margin from their respective conformance limits.)

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**Table 2.4.7-1: HS Receiver  $T_{CLK-PREPARE} + T_{CLK-ZERO}$  Test Cases**

Case #	$T_{CLK-PREPARE}$	$T_{CLK-ZERO}$	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	Notes
1	70ns	300ns	370ns	Nominal $T_{CLK-PREPARE}$ and nominal $T_{CLK-PREP+ZERO}$ . (Control case)
2	38ns	332ns	370ns	Minimum $T_{CLK-PREPARE}$ and nominal $T_{CLK-PREP+ZERO}$ .
3	38ns	262ns	300ns	Minimum $T_{CLK-PREPARE}$ and minimum $T_{CLK-PREP+ZERO}$ .
4	95ns	275ns	370ns	Maximum $T_{CLK-PREPARE}$ and nominal $T_{CLK-PREP+ZERO}$ .
5	95ns	205ns	300ns	Maximum $T_{CLK-PREPARE}$ and minimum $T_{CLK-PREP+ZERO}$ .

(Key: **Red** = Spec TX minimum, **Green** = Nominal TX value, **Blue** = Spec TX maximum)

For all test cases, the DUT must successfully receive the HS data without error in order to be considered conformant.

**Test Setup:** This test uses a hybrid TX/RX test setup. See Test Setup of Test 2.4.1 (which uses the same setup).

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to transmit an otherwise valid HS image data sequence to the DUT, using the  $T_{CLK-PREPARE} + T_{CLK-ZERO}$  Test Case #1 values as described above.
- Verify that the DUT successfully received the HS image data without error.
- Repeat the previous two steps for Test Cases #2 through #5.

**Observable Results:**

- For all test cases, verify that the DUT successfully received the HS burst data without error.

**Possible Problems:** None.

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**Test 2.4.8 – Clock Lane HS-RX  $T_{CLK-SETTLE}$  Value**

**Purpose:** To verify that the DUT's Clock Lane receiver incorporates a sufficient timeout interval ( $T_{CLK-SETTLE}$ ) to ignore transition effects that may occur during the HS Entry sequence.

**References:**

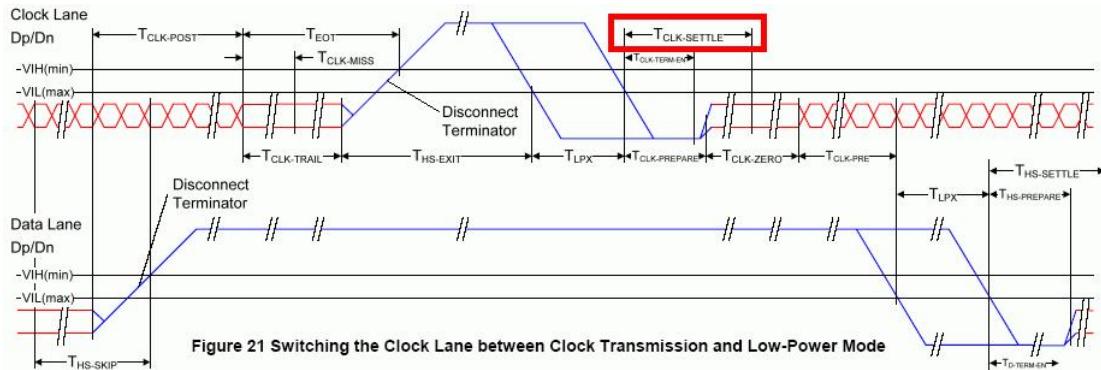
- [1] D-PHY Specification, Section 5.9, Table 14
- [2] Ibid, Section 5.4.2, Table 3 (Line 789)

**Resource Requirements:** See Appendix A.2.

**Last Modification:** September 16, 2010

**Discussion:**

As part of the process of receiving an HS Data Burst, the D-PHY Specification provides a requirement for a timeout period at the beginning of an HS burst sequence, which allows the Clock Lane HS-RX to ignore any potential transition effects of the SoT sequence. This interval is defined as  $T_{CLK-SETTLE}$ , and is shown in the figure below.



**Figure 2.4.8-1:  $T_{CLK-SETTLE}$  Timeout Interval**

The specification defines  $T_{CLK-SETTLE}$  as the, “*Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of  $T_{CLK-PREPARE}$ .*” [1].

The conformance range for  $T_{CLK-SETTLE}$  is defined as 95 to 300ns. This implies that all conformant devices shall ignore all Clock Lane HS transitions for a period of 95ns after the start of  $T_{CLK-PREPARE}$ . Devices may ignore Clock Lane transitions for window lengths between 95 and 300ns, and all devices shall not ignore Clock Lane transitions for window lengths of 300ns and greater. (Note that 300ns is the minimum valid TX conformance value for  $T_{CLK-PREPARE} + T_{CLK-ZERO}$ . Therefore, because this is the minimum time that a conformant transmitter could be expected to wait before sending HS clock signaling, this in turn determines the upper limit on the window during which a receiver is allowed to ignore HS Clock Lane transitions.)

The methodology for this test involves sending HS burst sequences containing valid minimum-length  $T_{CLK-PREPARE}$  values (38ns), followed by a valid minimum-length  $T_{CLK-ZERO}$  (262ns), so that  $T_{CLK-PREPARE} + T_{CLK-ZERO}$  is at the minimum conformant value of 300ns. However at the beginning of  $T_{CLK-ZERO}$ , repeating 1010 HS clock data will be inserted in place of the first 95 - 38 = 57ns of  $T_{CLK-ZERO}$ . This ‘false clock’ sequence is used to create the appearance that the HS clock signal has started, when really there will be another period of HS-0 following this sequence, before the HS clock actually begins.

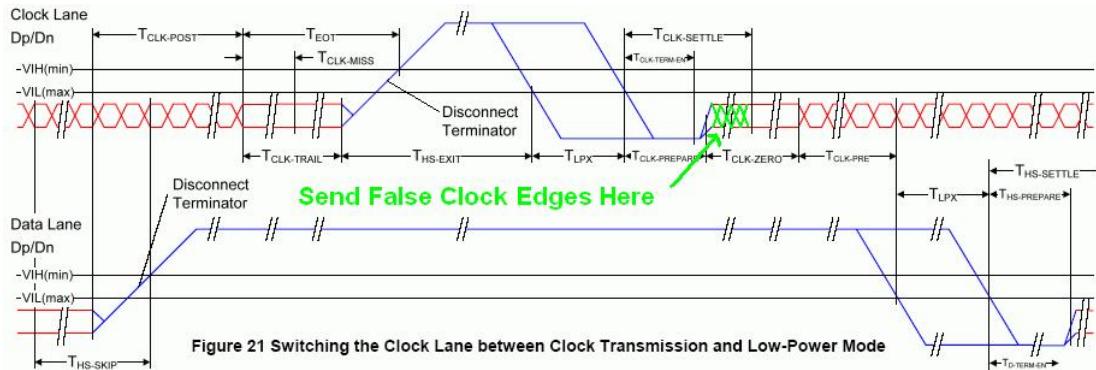
Note the exact behavior upon reception of this ‘false clock’ sequence is not clearly defined by the specification, however one possibility could be that if the DUT does detect the false clock transitions as the start of the HS clock, there exists the potential that the  $T_{CLK-ZERO}$  period following the false clock could be interpreted as a valid  $T_{CLK-MISS}$  interval, which is the mechanism used by the Clock Lane receiver to determine when to disable the Clock Lane HS termination (see Test 2.4.10 for further discussion about  $T_{CLK-MISS}$ ). When the Clock Lane receiver detects the absence of Clock Lane HS transitions for the time  $T_{CLK-MISS}$  (which has maximum conformance limit of 60ns), this triggers the action to disable the Clock Lane HS termination. If this mistakenly happens by misinterpretation of the  $T_{CLK-ZERO}$  period as  $T_{CLK-MISS}$ , the HS clock signal occurring during the HS Data Lane data will likely be corrupted, resulting in errored reception.

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While this test is similar in nature to the Data Lane  $T_{HS\text{-SETTLE}}$  test of 2.4.3, it is not as rigorous, as the options for observability into the inner behavior of the Clock Lane receiver are limited, relative to the Data Lane case. The primary goal of this test will simply be to verify that the presence of HS clock transitions within the minimum  $T_{CLK\text{-SETTLE}}$  window does not negatively affect the operation of the receiver.

The figure below shows the location of the false clock transitions in the overall HS burst. (Note that in the diagram below, the false clock transitions are not drawn to scale):



**Figure 2.4.8-2:  $T_{CLK\text{-SETTLE}}$  Test Sequence, with False Clock Transitions**

The false clock transitions will be positioned starting at 38ns after the start of  $T_{CLK\text{-PREPARE}}$  (i.e., following the minimum-length  $T_{CLK\text{-PREPARE}}$ ), and will extend to 95ns. From here, an additional  $300\text{-}38\text{-}57 = 205$ ns of HS-0 will be added to complete the  $T_{CLK\text{-ZERO}}$  interval. The sequence will also use a minimum-length conformant value of  $8\text{*UI}$  for  $T_{CLK\text{-PRE}}$ . All other timing parameters shall be set to nominal values.

If the DUT successfully receives the test sequence without error, the test result will be considered passing.

**Test Setup:** This test uses a hybrid TX/RX test setup. See Test Setup of Test 2.4.1 (which uses the same setup).

### Test Procedure:

- Connect the DUT to the Test System.
- Configure the Test Setup to transmit a valid image data sequence to the DUT, which uses a  $T_{HS\text{-PREPARE}}$  value of 38ns, and a  $T_{CLK\text{-ZERO}}$  value of  $300\text{-}38 = 262$ ns, but which has the first  $95\text{-}38 = 57$ ns of  $T_{CLK\text{-ZERO}}$  replaced with false clock transitions, as described above.

### Observable Results:

- Verify that the image data is properly received by the DUT without error (via any valid observable means).

**Possible Problems:** None.

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### Test 2.4.9 – Clock Lane HS-RX $T_{CLK-TRAIL}$ Tolerance

**Purpose:** To verify that the DUT's Clock Lane HS receiver can tolerate reception of conformant values for  $T_{CLK-TRAIL}$ .

#### References:

- [1] D-PHY Specification, Section 5.9, Lines 976 + 977
- [2] Ibid, Section 5.9, Line 966

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

#### Discussion:

As part of the process for switching the Clock Lane out of HS mode, the D-PHY specification includes requirements for the  $T_{CLK-TRAIL}$  interval, which is shown in the figure below.

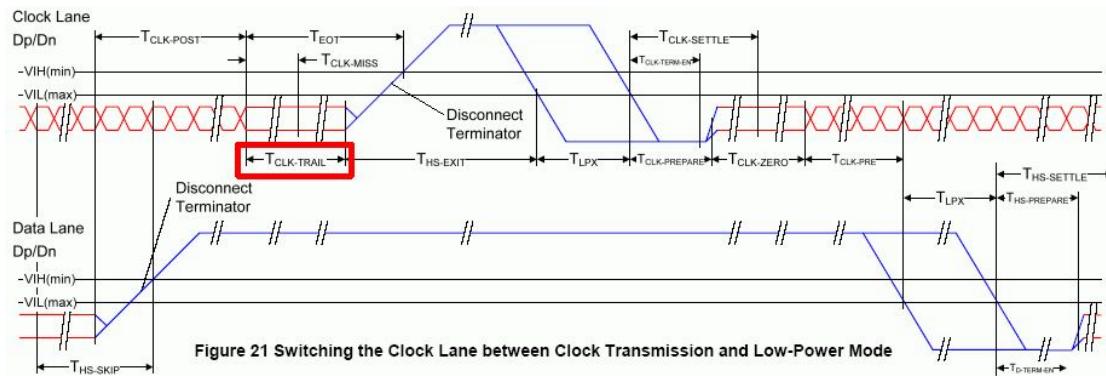


Figure 2.4.9-1:  $T_{CLK-TRAIL}$  Interval

Note that the D-PHY specification defines timing parameters as being either transmitter-specific or receiver-specific[1], and  $T_{CLK-TRAIL}$  is defined as a transmitter-specific parameter.

However, the specification also contains a requirement that states, “*Also note that while corresponding receiver tolerances are not defined for every transmitter-specific parameter, receivers shall also support reception of all allowed conformant values for all transmitter-specific timing parameters in Table 14 for all HS UI values up to, and including, the maximum supported HS clock rate specified in the receiver’s datasheet.*”[2]. While the transmitter requirements for  $T_{CLK-TRAIL}$  are verified in a separate test in this test suite, this test will verify whether or not a receiver is capable of tolerating values for  $T_{CLK-TRAIL}$  across the entire TX conformance range.

The lower limit for the TX conformance range of  $T_{CLK-TRAIL}$  is defined as 60ns. An upper bound on  $T_{CLK-TRAIL}$  is not explicitly defined, however an implicit upper limit is imposed by the  $T_{EOT}$  specification (which is the sum of the  $T_{CLK-TRAIL}$  and  $T_{REOT}$  intervals, and has an upper limit of 105ns + 12\*UI). Therefore, a practical TX upper limit for  $T_{CLK-TRAIL}$  would be (105 ns + 12\*UI) minus  $T_{REOT}$  for the respective transmitter (which is required to be less than 35ns, as defined by the  $T_{REOT}$  requirements, see Test 1.3.14). In order to simplify the test procedure and remove any dependence on the actual  $T_{REOT}$  of the test setup, two upper limit test cases will be performed, one normative case assuming the maximum allowed  $T_{REOT}$  of 35ns, and a second informative case where  $T_{REOT}$  is assumed to be 0ns.

Also, note that all other timing parameters (e.g.,  $T_{HS/CLK-PREPARE}$ ,  $T_{HS/CLK-ZERO}$ , etc) should be set to nominal values for this test. (Note that exact values are not specified here for all parameters, as flexibility is allowed to choose these values according to potential timing needs of the DUT. All values should be chosen to include sufficient margin from their respective conformance limits.)

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Four total test cases for  $T_{CLK-TRAIL}$  will be performed (starting with a nominal  $T_{CLK-TRAIL}$  case, for control purposes), which are listed in the table below.

**Table 2.4.9-1: HS Receiver  $T_{CLK-TRAIL}$  Test Cases**

Case #	$T_{CLK-TRAIL}$	Notes
1	<b>80ns</b>	Nominal $T_{CLK-TRAIL}$ (Control case)
2	<b>60ns</b>	Minimum $T_{CLK-TRAIL}$
3	<b>70ns + 12*UI</b>	Maximum $T_{CLK-TRAIL}$ (Assuming $T_{REOT} = 35\text{ns}$ )
4	<b>105ns + 12*UI</b> (Informative)	Maximum $T_{CLK-TRAIL}$ (Assuming $T_{REOT} = 0\text{ns}$ )

The general methodology for this test will be similar to that used for most of the other HS-RX tolerance tests (e.g., Test 2.4.2), whereby an otherwise valid HS image data sequence will be sent to the DUT, using the various test case values of  $T_{CLK-TRAIL}$ , and the DUT will be observed to determine if the image data is received without error.

For all test cases, the DUT must successfully receive the HS image data without error in order to be considered conformant.

**Test Setup:** This test uses a hybrid TX/RX test setup. See Test Setup of Test 2.4.1 (which uses the same setup).

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to transmit an otherwise valid HS image data sequence to the DUT, using the  $T_{CLK-TRAIL}$  Test Case #1 value described above.
- Verify that the DUT successfully received the HS image data without error.
- Repeat the previous two steps for  $T_{CLK-TRAIL}$  Test Cases #2, #3, and #4.

**Observable Results:**

- For all test cases, verify that the DUT successfully received the HS image data without error.

**Possible Problems:** None.

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### Test 2.4.10 – Clock Lane HS-RX $T_{CLK-MISS}$ Value

**Purpose:** To verify that the DUT's Clock Lane HS receiver correctly detects the cessation of clock activity and disconnects its line termination within the maximum allowed interval ( $T_{CLK-MISS}$ ).

#### References:

- [1] D-PHY Specification, Section 5.7, Table 10
- [2] Ibid, Section 5.9, Table 14

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

#### Discussion:

As part of the process for switching the Clock Lane out of HS mode, the D-PHY Specification provides a specification for the maximum time allowed for the Slave DUT to detect that the clock has stopped toggling, and disconnect its HS line termination. This timer is defined as  $T_{CLK-MISS}$ , and is shown in the figure below.

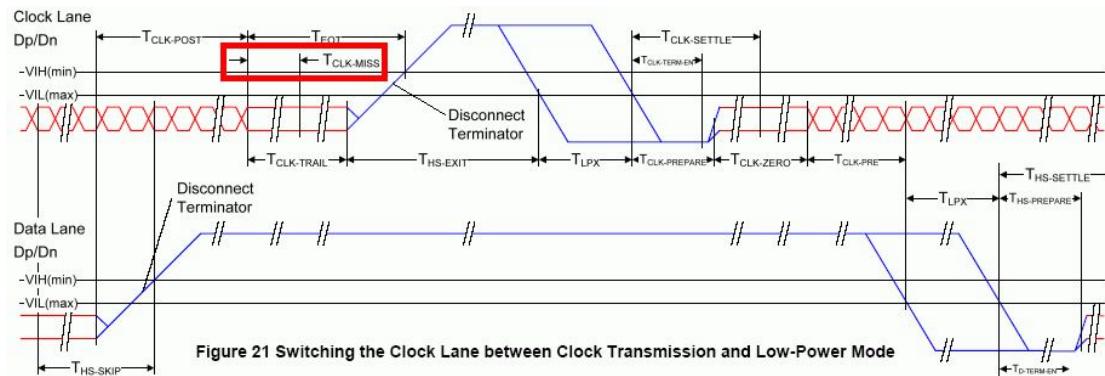


Figure 21 Switching the Clock Lane between Clock Transmission and Low-Power Mode

Figure 2.4.10-1:  $T_{CLK-MISS}$  Interval

In the process of bringing the Clock Lane out of HS mode, the Master will stop toggling the HS Clock, and hold the inverse of the last toggled state for a period of  $T_{CLK-TRAIL}$ , which is held for a minimum of 60ns. At some time less than 60ns, the Slave device “*Detects absence of Clock transitions within a time  $T_{CLK-MISS}$ , disables HS-RX then waits for a transition to the Stop state.*”[1]

The methodology for this test involves the construction of a test sequence whereby a ‘clock gap’ is inserted in the middle of a valid HS burst sequence. This involves transmitting a false  $T_{CLK-TRAIL}$  period on the Clock Lane, in the middle of an HS burst (by excessively ‘stretching’ the length of a single clock UI), while simultaneously extending the corresponding UI on the Data Lane. If the length of this ‘stretched’ UI is less than  $T_{CLK-MISS}$ , then the receiver should continue to operate properly. However, once the interval exceeds the receiver’s  $T_{CLK-MISS}$  limit, the receiver should proceed to disconnect its HS termination following the stretched UI (which would corrupt the remainder of the HS burst data.)

In this test, an otherwise valid HS sequence will be constructed, which has a single ‘stretched’ UI on both the Clock and Data Lanes. The value of this stretched UI will be increased until the DUT no longer received the HS burst data properly.  $T_{CLK-MISS}$  will be measured as the maximum ‘stretched’ UI value for which the DUT continues to operate without error.

The measured  $T_{CLK-MISS}$  value must be less than 60 ns in order to be considered conformant [2].

**Test Setup:** This test uses a hybrid TX/RX test setup. See Test Setup of Test 2.4.1 (which uses the same setup).

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**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to emulate a Master device.
- Send the test sequence containing the ‘stretched’ UI to the DUT, where the stretched UI is equal to 2\*UI.
- Verify that the DUT successfully received the sequence without error.
- Incrementally increase the length of the stretched UI until the DUT starts to indicate errors.
- Record  $T_{CLK-MISS}$  as the maximum stretched UI value for which the DUT successfully operates without error.

**Observable Results:**

- Verify that  $T_{CLK-MISS}$  is less than 60ns.

**Possible Problems:** None.

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**Test 2.4.11 – Clock Lane HS-RX  $T_{CLK-PRE}$  and  $T_{CLK-POST}$  Tolerance**

**Purpose:** To verify that the DUT's Clock Lane HS receiver can tolerate reception of bursts that have minimum-duration  $T_{CLK-PRE}$  and  $T_{CLK-POST}$  values.

**References:**

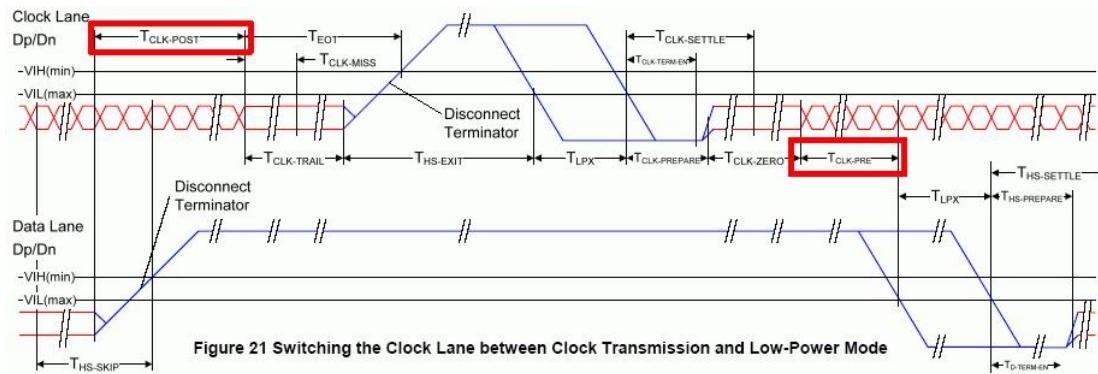
- [1] D-PHY Specification, Section 5.9, Lines 976 + 977
- [2] Ibid, Section 5.9, Line 966

**Resource Requirements:** See Appendix A.2.

**Last Modification:** November 30, 2009

**Discussion:**

As part of the process for switching the Clock and Data Lanes into and out of HS mode, the D-PHY specification includes requirements for the  $T_{CLK-PRE}$  and  $T_{CLK-POST}$  intervals, which are shown in the figure below.



**Figure 2.4.11-1:  $T_{CLK-PRE}$  and  $T_{CLK-POST}$  Intervals**

Note that the D-PHY specification defines timing parameters as being either transmitter-specific or receiver-specific [1], and  $T_{CLK-PRE}$  and  $T_{CLK-POST}$  are defined as transmitter-specific parameters.

However, the specification also contains a requirement that states, “*Also note that while corresponding receiver tolerances are not defined for every transmitter-specific parameter, receivers shall also support reception of all allowed conformant values for all transmitter-specific timing parameters in Table 14 for all HS UI values up to, and including, the maximum supported HS clock rate specified in the receiver’s datasheet.*”[2]. While the transmitter requirements for  $T_{CLK-PRE}$  and  $T_{CLK-POST}$  are verified in separate tests in this test suite, this test will verify whether a receiver is capable of tolerating the minimum-length conformant values of  $T_{CLK-PRE}$  and  $T_{CLK-POST}$ .

The minimum TX conformant value for  $T_{CLK-PRE}$  is  $8*UI$ . The minimum TX conformant value for  $T_{CLK-POST}$  is  $60ns+52*UI$ . Note that no upper limits are specified for either parameter, therefore the purpose of this test is simply to verify proper reception of these minimum-length values.

In this test, HS image data will be sent to the DUT using these minimum  $T_{CLK-PRE}$  and  $T_{CLK-POST}$  values for all HS bursts. In addition, the values of  $T_{HS/CLK-PREPARE}$ ,  $T_{HS/CLK-ZERO}$ , and  $T_{HS/CLK-TRAIL}$  will also be set to their respective minimum TX conformance values for this test. A summary of the specific timing values used for this test is provided in the table below.

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**Table 2.4.11-1:  $T_{CLK-PRE/POST}$  Test Sequence Timing Values  
(All values are minimum-length TX conformance values)**

Parameter	Value
$T_{CLK-PRE}$	8*UI
$T_{CLK-POST}$	60ns + 52*UI
$T_{CLK-PREPARE}$	38ns
$T_{CLK-PREPARE} + T_{CLK-ZERO}$	300ns
$(T_{CLK-ZERO})$	262ns
$T_{HS-PREPARE}$	40ns + 4*UI
$T_{HS-PREPARE} + T_{HS-ZERO}$	145ns + 10*UI
$(T_{HS-ZERO})$	105ns + 6*UI

The general methodology for this test will be similar to that used for most of the other HS-RX tolerance tests (e.g., Test 2.4.2), whereby an otherwise valid HS image data sequence will be sent to the DUT, using the worst-case minimum-length timing values listed above. The DUT will be observed to determine if the image data is received without error.

The DUT must successfully receive the HS image data without error in order to be considered conformant.

**Test Setup:** This test uses a hybrid TX/RX test setup. See Test Setup of Test 2.4.1 (which uses the same setup).

**Test Procedure:**

- Connect the DUT to the Test System.
- Configure the Test System to transmit an otherwise valid HS image data sequence to the DUT, using the timing values specified in Table 2.4.11-1 above.
- Verify that the DUT successfully received the HS image data without error.

**Observable Results:**

- Verify that the DUT successfully received the HS image data without error.

**Possible Problems:** None.

## **SECTION 3: INTERFACE IMPEDANCE AND S-PARAMETERS**

### **Overview:**

This selection of tests verifies various S-parameter and low-frequency impedance requirements of D-PHY products defined in Sections 7 and 8 of the D-PHY Specification.

Group 1 verifies the S-parameter characteristics of the HS-TX interface.

Group 2 verifies the S-parameter characteristics of the HS-RX interface.

Group 3 verifies several impedance-related requirements of the LP-TX and LP-RX interfaces.

Comments and questions regarding the documentation and/or implementation of these tests are welcome, and may be sent to [aab@iol.unh.edu](mailto:aab@iol.unh.edu).

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**GROUP 1: HS-TX S-PARAMETERS**

**Overview:**

This group of tests verifies the HS-TX interface S-Parameter requirements defined in Section 7.7 of the D-PHY Specification.

**Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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**Test 3.1.1 – HS-TX Differential Return Loss (SDD22)**

**Purpose:** To verify that the Differential Return Loss of the DUT's Clock and Data Lane HS transmitters exceeds the minimum conformance limits.

**References:**

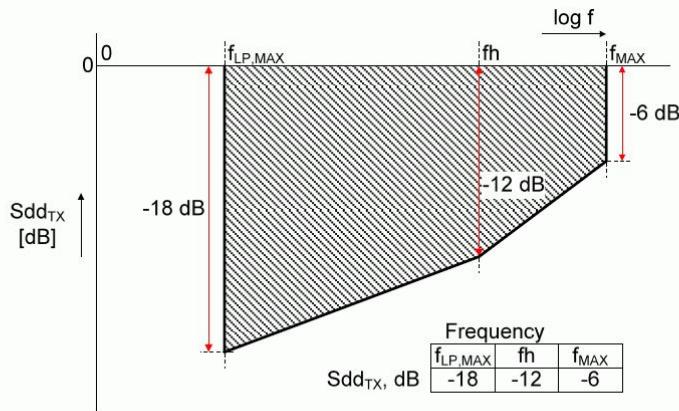
- [1] D-PHY Specification, Section 7.7.1, Line 1276
- [2] Ibid, Section 7.3, Line 1198
- [3] Ibid, Section 7.3, Line 1195

**Resource Requirements:** See Appendix A.3.

**Last Modification:** November 30, 2009

**Discussion:**

Section 7 of the D-PHY Specification defines the general interconnect and lane configuration requirements for D-PHY products. Section 7.7 defines the HS Driver and Receiver S-parameter specifications, which includes a specification for TX Differential Return Loss. The specification is defined in terms of a scalable frequency-domain template, reproduced in the figure below:



**Figure 33 Differential Reflection Template for Lane Module Transmitters**

**Figure 3.1.1-1: HS-TX Differential Return Loss Conformance Limits**

The specification states, “The differential reflection of a Lane Module in High-Speed TX mode is specified by the template shown in Figure 33.”[1].

Note that the specification is intentionally defined to be scalable relative to the operating speed of the DUT, which is indirectly related to the signal rise/fall times for a particular DUT. The parameter  $f_{MAX}$  shown above is defined as the maximum of  $(1/t_{F,MIN}, 1/t_{R,MIN})$ [2], where  $t_R$  and  $t_F$  are the rise and fall times of the High-Speed signaling, which must be separately determined prior to performing this test. Note that this test will be performed for all Clock and Data Lanes, however for simplicity, a single  $f_{MAX}$  value will be used for all Lanes, which will be taken as the maximum  $f_{MAX}$  value for any single Lane, based on the measured HS-TX rise and fall times that were obtained in Tests 1.3.11 and 1.3.12.

The value  $f_{LP,MAX}$  is defined in the specification as, “the maximum toggle frequency for Low-Power mode.”[3]. While this is defined term similar to  $f_{MAX}$ , it is not intended as a DUT-specific variable, but rather a fixed value, which is 20MHz.

Also, given that this is a transmitter specification, it is necessary to have the DUT in a normal powered-on and operational state where it is actively transmitting HS data signaling during the measurement. However, care must be taken to ensure that the signaling emitted from the active transmitter does not adversely impact the

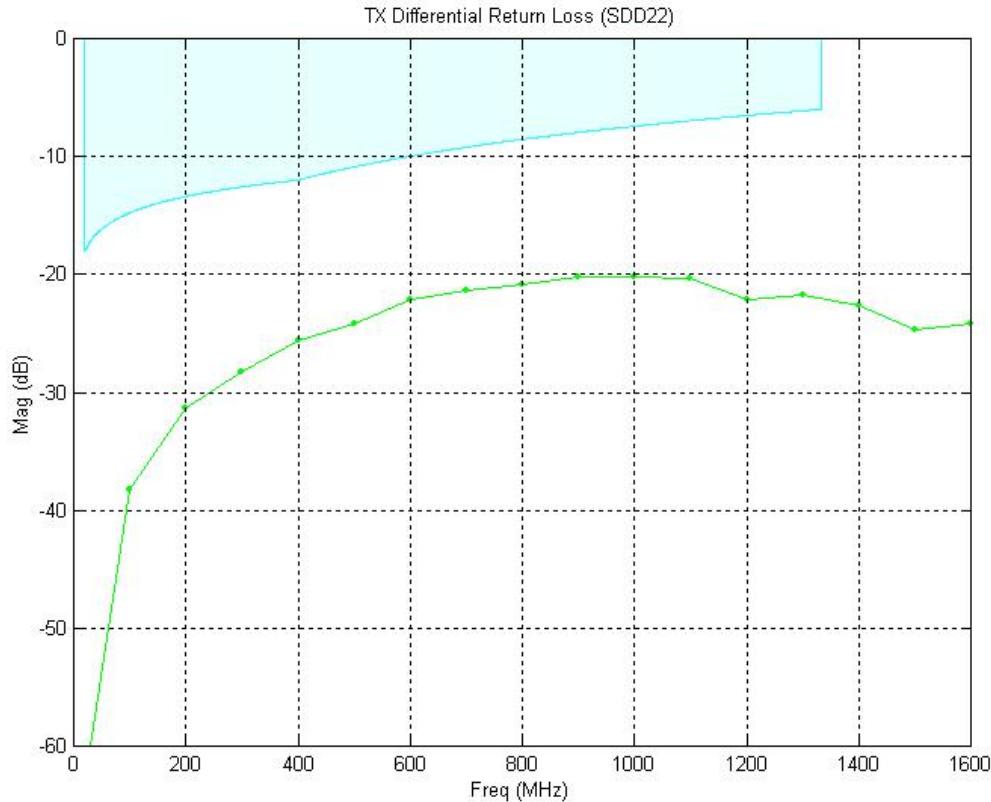
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measurement results, and is suitably removed from the measurement. If a Vector Network Analyzer (VNA) is used for the measurement, this can be accomplished by setting a sufficiently high output power level and narrow IFBW setting on the VNA, and configuring the DUT to transmit a non-periodic (i.e., pseudo-random) data pattern, in order to minimize the transmitted energy in any particular narrow IF band.

If a Time-Domain Reflectometer (TDR) is used for the measurement, time-domain averaging can be used to cancel out the energy being transmitted by the DUT. Because the DUT's transmitted HS signaling is not time-correlated to the incident TDR stimulus pulses (and hence the pulse reflections from the DUT interface), the DUT's signaling will average out over time if averaging is enabled on the TDR. Note that for the TDR case, a high-frequency repeating HS pattern (e.g., 1010, 1100, etc) is preferred over a pseudo-random pattern, as this type of pattern is more easily removed by the averaging operation. (Note that 1010 is the recommended pattern D-PHY measurements.)

Also note that this Test Suite adopts the S-parameter naming convention such that an HS-RX is always described as differential Port 1, and an HS-TX is differential Port 2. (Hence SDD22 for HS-TX Differential Return Loss.)

The HS-TX Differential Return Loss response must fall below the grayed out region shown in the figure above in order to be considered conformant (e.g., there must be *at least* 18dB of return loss at  $f_{LP,MAX}$ , etc). An example measurement result showing a conformant Differential Return Loss response is shown in the figure below.



**Figure 3.1.1-2: Example Conformant HS-TX Differential Return Loss Result**

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**Test Setup:** See Appendix B.3.1.

**Test Procedure:**

- Compute the value of  $f_{MAX}$  for the DUT as described above, based on the measured HS-TX rise and fall times obtained in Tests 1.3.11 and 1.3.12.
- Power on and configure the DUT to force its HS-TX into a fixed HS state, transmitting a continuous, repeating pattern (1010 for TDR-based measurements, or pseudo-random for VNA measurements) on all Clock and Data Lanes.
- Calibrate and configure the Test System for a Differential Return Loss measurement (SDD22) over the frequency range  $f_{LP,MAX}$  (20MHz) to  $f_{MAX}$ .
- Connect the DUT's Data Lane 0 transmitter to the Test System.
- Measure the SDD22 HS-TX Differential Return Loss.
- Repeat the previous two steps for all other Data Lanes, and the Clock Lane.

**Observable Results:**

- For all Clock and Data Lanes, verify that the SDD22 HS-TX Differential Return Loss meets or exceeds the limits shown in the figure above.

**Possible Problems:**

This measurement requires the DUT to be able to force its HS-TX Lanes into a continuous HS-only mode. This is considered vendor-specific functionality, and is outside the scope of normal operating behavior. However, it is necessary in order to make the proper measurements on the HS-TX. If the DUT does not support this type of functionality, the measurement may not be able to be performed.

Note also that some DUTs have the ability to programmatically remap the order of their Clock and Data Lanes. If this is the case, AND the DUT supports continuous clocking on the Clock Lane, it is possible to leverage these features to allow measurement of all HS-TX transceivers for a given DUT, by separately mapping each Lane transceiver to operate as a Clock Lane in continuous-clocking mode, and performing the measurement in this mode. (Note that the measurement will technically not be performed while the transceiver is operating as a Data Lane in this case, however the consequences of this should be minimal, as it is the physical transceiver circuitry that is being measured under HS operation, regardless of the HS data being transmitted (i.e., clock vs. data)).

As stated in the Discussion section above, it may be possible in some cases for the TX signaling of the DUT to introduce error into the measurement. Improperly configured DUTs (i.e., not transmitting the optimal HS pattern, or being forced into HS-only operation, etc) can produce erroneous measurement results, which could lead to false failures. Care should be taken to ensure that all sources of error have been minimized.

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**Test 3.1.2 – HS-TX Common-Mode Return Loss (SCC22)**

**Purpose:** To verify that the Common-Mode Return Loss of the DUT's Clock and Data Lane HS transmitters exceeds the minimum conformance limits.

**References:**

- [1] D-PHY Specification, Section 7.7.2, Line 1281

**Resource Requirements:** See Appendix A.3.

**Last Modification:** November 30, 2009

**Discussion:**

Section 7 of the D-PHY Specification defines the general interconnect and lane configuration requirements for D-PHY products. Section 7.7 defines the Driver and Receiver S-parameter specifications, which includes a specification for TX Common-Mode Return Loss.

The specification states, “*The common-mode return loss specification is different for a High-Speed TX and RX mode, because the RX is not DC terminated to ground. For an active TX the common-mode reflection shall be less than -6dB from  $f_{LP,MAX}$  up to  $f_{MAX}$ . For an RX reflection shall be less than -6 dB for the frequency range  $f_{INT,MIN}$  -  $f_{MAX}$ .*”[1]. This test verifies the TX requirement.

Note that because the TX Common-Mode Return Loss specification is defined simply as a straight 6dB limit across the range ( $f_{LP,MAX}$  to  $f_{MAX}$ ), no template is defined for the TX case. (Note that  $f_{LP,MAX}$  is taken to be a fixed value of 20MHz, see Discussion of Test 3.1.1.)

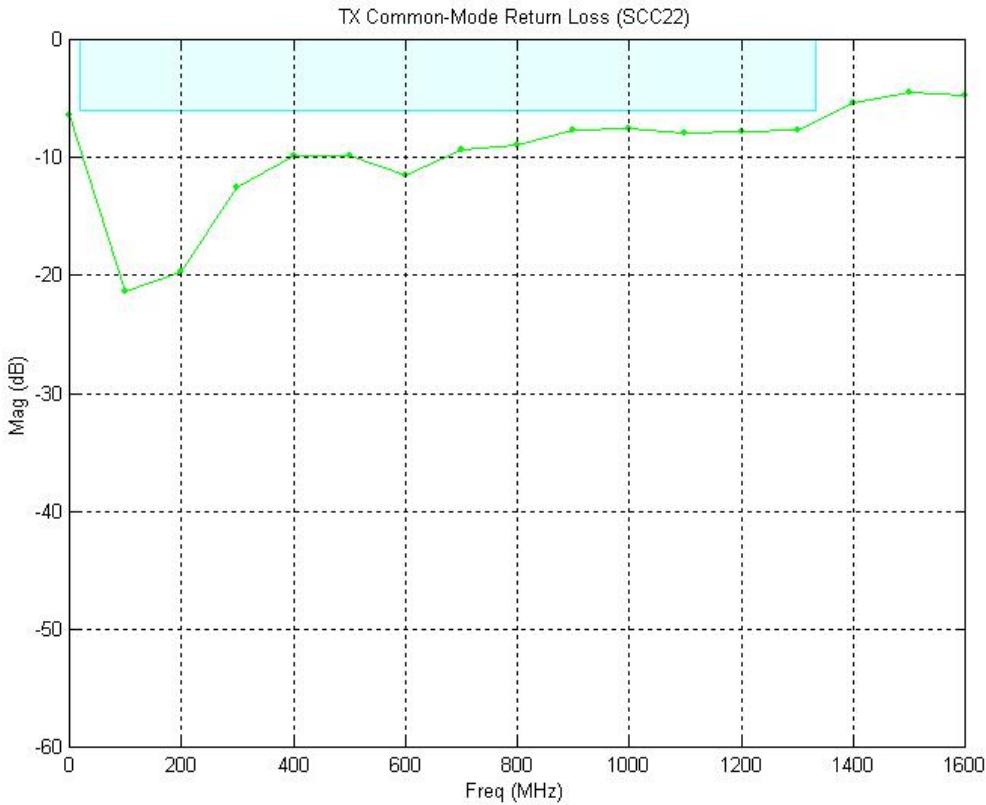
Also, given that this is a transmitter specification, it is necessary to have the DUT in a normal powered-on and operational state where it is actively transmitting data signaling during the measurement. (See comments in Test 3.1.1 Discussion regarding transmitted data patterns.)

Also, this test will be performed for all Clock and Data Lanes, and will use the same  $f_{MAX}$  value for all Lanes, which was computed in the previous test. (See Test 3.1.1 Discussion.)

Also, note that this Test Suite adopts the S-parameter naming convention such that an HS-RX is always described as differential Port 1, and an HS-TX is differential Port 2. (Hence SCC22 for HS-TX Common-Mode Return Loss.)

For all Clock and Data Lanes, the HS-TX Common-Mode Return Loss must be greater than 6dB across the range ( $f_{LP,MAX}$  to  $f_{MAX}$ ) in order to be considered conformant. An example measurement result showing a conformant Common-Mode Return Loss response is shown in the figure below.

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**Figure 3.1.2-1: Example Conformant HS-TX Common-Mode Return Loss Result**

**Test Setup:** See Appendix B.3.1.

**Test Procedure:**

- Obtain the value of  $f_{MAX}$  for the DUT that was used in Test 3.1.1.
- Power on and configure the DUT to force its HS-TX into a fixed HS state, transmitting a continuous, repeating pattern (1010 for TDR-based measurements, or pseudo-random for VNA measurements) on all Clock and Data Lanes.
- Calibrate and configure the Test System for a Common-Mode Return Loss measurement (SCC22) over the frequency range ( $f_{LP,MAX}$  to  $f_{MAX}$ ).
- Connect the DUT's Data Lane 0 transmitter to the Test System.
- Measure the SCC22 HS-TX Common-Mode Return Loss.
- Repeat the previous two steps for all other Data Lanes, and the Clock Lane.

**Observable Results:**

- For all Clock and Data Lanes, verify that the SCC22 HS-TX Common-Mode Return Loss is greater than 6dB across the frequency range  $f_{LP,MAX}$  to  $f_{MAX}$ .

**Possible Problems:**

See Possible Problems comments for Test 3.1.1. The same applies to this test.

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**Test 3.1.3 – HS-TX Mode Conversion Limits (SDC22)**

**Purpose:** To verify that the Mode Conversion S-parameters of the DUT's Clock and Data Lane HS transmitters exceed the minimum conformance limits.

**References:**

[1] D-PHY Specification, Section 7.7.3, Line 1291

**Resource Requirements:** See Appendix A.3.

**Last Modification:** November 30, 2009

**Discussion:**

Section 7 of the D-PHY Specification defines the general interconnect and lane configuration requirements for D-PHY products. Section 7.7 defines the Driver and Receiver S-parameter specifications, which includes a specification for TX Mode Conversion Limits.

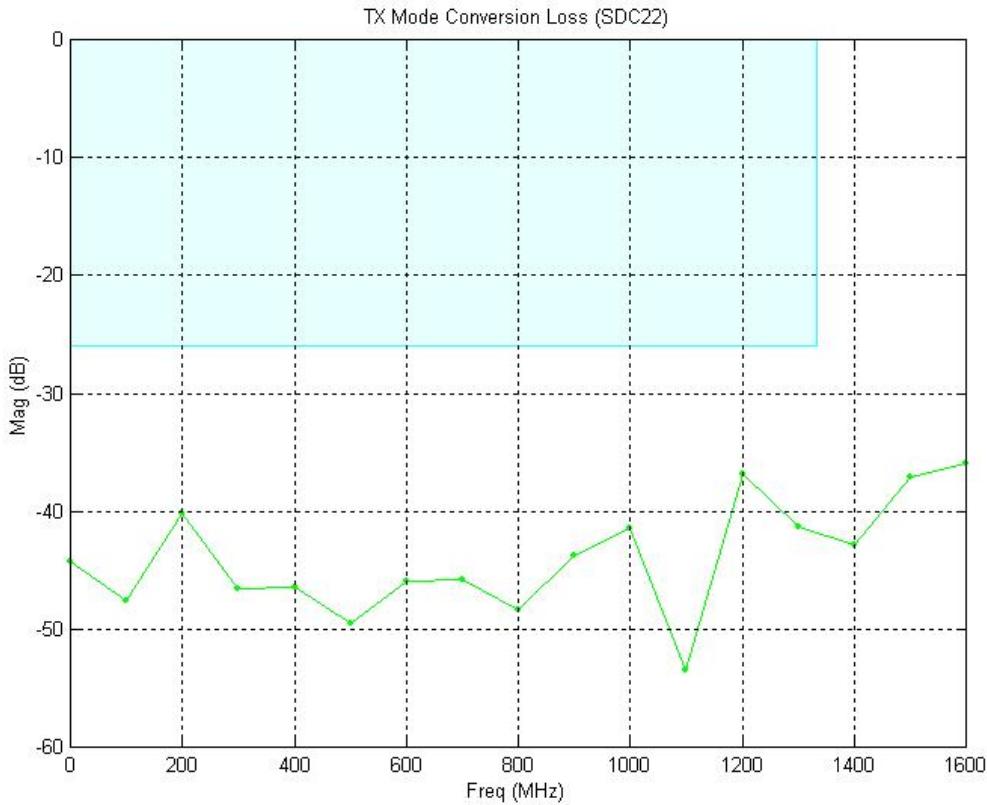
The specification states, “*The differential to common-mode conversion limits of TX and RX shall be -26dB up to  $f_{MAX}$ .*”[1].

Note that mode conversion S-parameters include SDC22 and SCD22 (assuming the TX port of the DUT is considered Differential Port 2, which is the convention used in this test suite, see Test 3.1.1 Discussion.) SDC22 involves launching a common-mode incident stimulus at the DUT interface and measuring the differential reflected energy. SCD22 involves launching a differential incident stimulus at the DUT interface and measuring the common-mode reflected energy. Both measurements offer a measure of the asymmetry or imbalance between the two single-ended trace responses that make up the differential pair (e.g., in the SDC22 case, any imbalance will result in a difference in the reflected energy on each single-ended conductor when stimulated with the same common-mode input.) For the purposes of this measurement, SDC22 and SCD22 will yield identical results, hence only SDC22 will be measured.

(The methodology for this test is otherwise identical to Tests 3.1.1 and 3.1.2, except that the SDC22 S-parameter will be measured over the frequency range 0 to  $f_{MAX}$ .)

The HS-TX Mode Conversion Loss shall be greater than 26dB over the frequency range 0 to  $f_{MAX}$  in order to be considered conformant. An example measurement result showing a conformant Mode Conversion Loss response is shown in the figure below.

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**Figure 3.1.3-1: Example Conformant HS-TX Mode Conversion Loss Result**

**Test Setup:** See Appendix B.1.3.

**Test Procedure:**

- Obtain the value of  $f_{MAX}$  for the DUT that was used in Test 3.1.1.
- Power on and configure the DUT to force its HS-TX into a fixed HS state, transmitting a continuous, repeating pattern (1010 for TDR-based measurements, or pseudo-random for VNA measurements) on all Clock and Data Lanes.
- Calibrate and configure the Test System for an SDC22 measurement over the frequency range 0 to  $f_{MAX}$ .
- Connect the DUT's Data Lane 0 transmitter to the Test System.
- Measure the SDC22 HS-TX Mode Conversion Loss.
- Repeat the previous two steps for all other Data Lanes, and the Clock Lane.

**Observable Results:**

- For all Clock and Data Lanes, verify that the SDC22 HS-TX Mode Conversion Loss is greater than 26dB across the frequency range 0 to  $f_{MAX}$ .

**Possible Problems:**

See Possible Problems comments for Test 3.1.1. The same applies to this test.

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**Test 3.1.4 – HS-TX Single-Ended Output Impedance ( $Z_{os}$ )**

**Purpose:** To verify that the Single-Ended Output Impedance ( $Z_{os}$ ) of the DUT's HS transmitters is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1366
- [2] Ibid, Section 8.1.1, Line 1374
- [2] Ibid, Section 8.1, Table 16

**Resource Requirements:** See Appendix A.3.

**Last Modification:** November 30, 2009

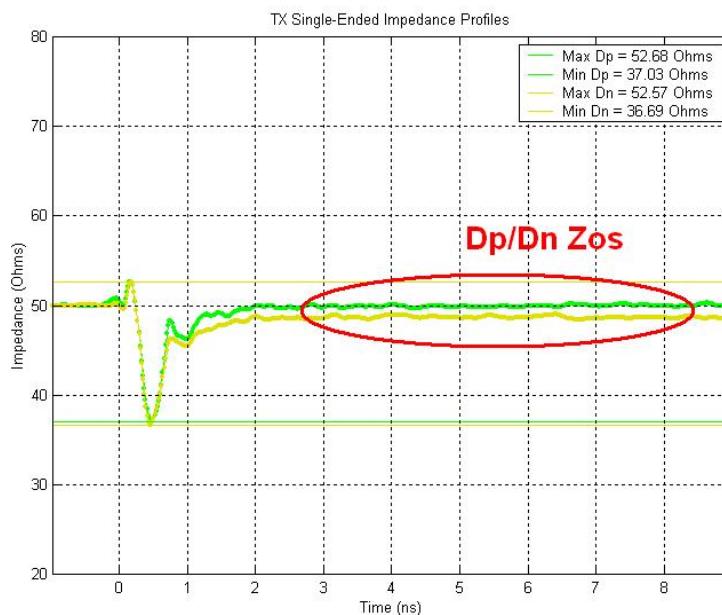
**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $Z_{os}$ , which is a device's High-Speed Single-Ended Output Impedance.

The D-PHY Specification states, “*The single-ended output impedance of the transmitter at both the D<sub>p</sub> and D<sub>n</sub> pins is denoted by  $Z_{os}$* ”[1].

The specification also states that, “*The output impedance  $Z_{os}$  can be determined by injecting an AC current into the D<sub>p</sub> and D<sub>n</sub> pins and measuring the peak-to-peak voltage amplitude.*” [2]. While this is one possible valid methodology for this measurement, a TDR-based approach is used for the purposes of this test suite. (This approach is chosen primarily because it allows all of the HS-TX and HS-RX S-parameter and impedance tests to be performed using a single setup.)

The TDR-based approach involves measuring the single-ended impedance profiles for the D<sub>p</sub> and D<sub>n</sub> pins of the HS transceiver, and measuring  $Z_{os}$  as the final, settled single-ended termination value for each line. An example measurement is shown in the figure below.



**Figure 3.1.4-1: Example HS-TX  $Z_{os}$  Measurement**

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The measured  $Z_{OS}$  for both the Dp and Dn pins for all Clock and Data Lanes shall be within the range of 40 to 62.5 Ohms in order to be considered conformant [3].

**Test Setup:** See Appendix B.1.3.

**Test Procedure:**

- Power on and configure the DUT to force its HS-TX into a fixed HS state, transmitting a continuous, repeating pattern (1010 for TDR-based measurements, or pseudo-random for VNA measurements) on all Clock and Data Lanes.
- Calibrate and configure the Test System for a single-ended impedance profile measurement for both the Dp and Dn pins.
- Connect the DUT's Data Lane 0 transmitter to the Test System.
- Measure  $Z_{OS}$  for both the Dp and Dn pins, as described above.
- Repeat the previous two steps for all other Data Lanes, and the Clock Lane.

**Observable Results:**

- For all Clock and Data Lanes, verify that  $Z_{OS}$  is between 40 and 62.5 Ohms for both the Dp and Dn pins.

**Possible Problems:**

See Possible Problems comments for Test 3.1.1. The same applies to this test.

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**Test 3.1.5 – HS-TX Single-Ended Output Impedance Mismatch ( $\Delta Z_{OS}$ )**

**Purpose:** To verify that the Single-Ended Output Impedance Mismatch ( $\Delta Z_{OS}$ ) of the DUT's HS transmitter is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.1.1, Line 1366
- [2] Ibid, Section 8.1, Table 16

**Resource Requirements:** None.

**Last Modification:** November 30, 2009

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $\Delta Z_{OS}$ , which is a device's High-Speed Single-Ended Output Impedance Mismatch. A copy of the specification text [1] is reproduced below.

The single-ended output impedance of the transmitter at both the Dp and Dn pins is denoted by  $Z_{OS}$ .  $\Delta Z_{OS}$  is the mismatch of the single ended output impedances at the Dp and Dn pins, denoted by  $Z_{OSDP}$  and  $Z_{OSDN}$  respectively. This mismatch is defined as the ratio of the absolute value of the difference of  $Z_{OSDP}$  and  $Z_{OSDN}$  and the average of those impedances:

$$\Delta Z_{OS} = 2 \frac{|Z_{OSDP} - Z_{OSDN}|}{Z_{OSDP} + Z_{OSDN}}$$

The output impedance  $Z_{OS}$  and the output impedance mismatch  $\Delta Z_{OS}$  shall be compliant with Table 16 for both the Differential-0 and Differential-1 states for all allowed loading conditions. It is recommended that implementations keep the output impedance during state transitions as close as possible to the steady state value. The output impedance  $Z_{OS}$  can be determined by injecting an AC current into the Dp and Dn pins and measuring the peak-to-peak voltage amplitude.

**Figure 3.1.5-1:  $\Delta Z_{OS}$  Specification**

The procedure for this test simply involves computing  $\Delta Z_{OS}$  from the measured  $Z_{OS}$  values obtained in Test 3.1.4. The  $\Delta Z_{OS}$  value will be computed for each Clock and Data Lane.

For all Clock and Data Lanes, the computed  $\Delta Z_{OS}$  value shall be less than 10% in order to be considered conformant [2].

**Test Setup:** None.

**Test Procedure:**

- Obtain the  $Z_{OS}$  values for each Clock and Data Lane from Test 3.1.4.
- For each lane, compute  $\Delta Z_{OS}$  as described above.

**Observable Results:**

- For all Clock and Data Lanes, verify that  $\Delta Z_{OS}$  is less than 10%.

**Possible Problems:** None.

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**GROUP 2: HS-RX S-PARAMETERS**

**Overview:**

This group of tests verifies the HS-RX interface S-parameter requirements defined in Section 7.7 of the D-PHY Specification.

**Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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**Test 3.2.1 – HS-RX Differential Return Loss (SDD11)**

**Purpose:** To verify that the Differential Return Loss of the DUT's Clock and Data Lane HS receivers exceeds the minimum conformance limits.

**References:**

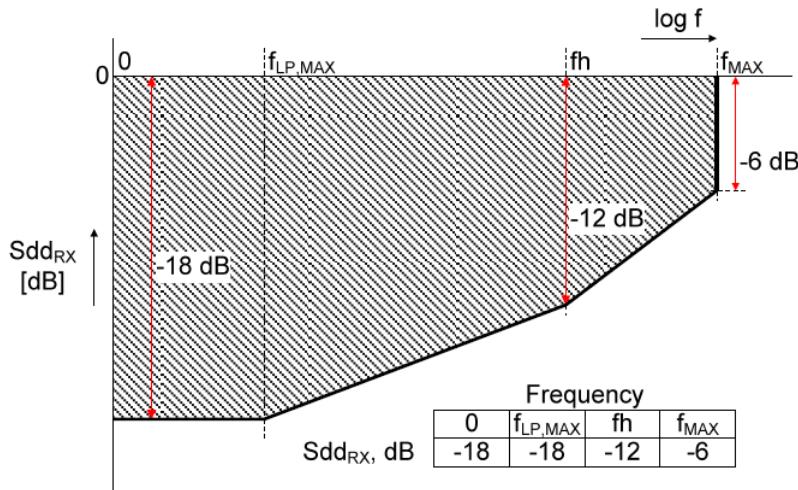
[1] D-PHY Specification, Section 7.7.1

**Resource Requirements:** See Appendix A.3.

**Last Modification:** September 16, 2010

**Discussion:**

Section 7 of the D-PHY Specification defines the general interconnect and lane configuration requirements for D-PHY products. Section 7.7 defines the Driver and Receiver S-parameter specifications, which includes a specification for RX Differential Return Loss. The specification is defined in terms of a scalable frequency-domain template, reproduced in the figure below.



**Figure 32 Differential Reflection Template for Lane Module Receivers**

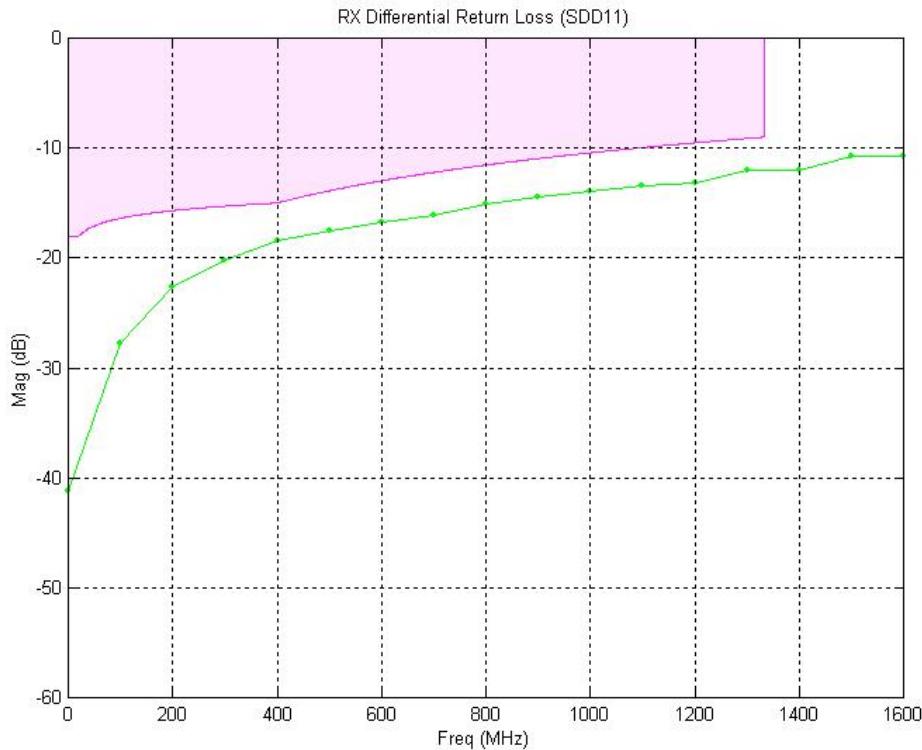
**Figure 3.2.1-1: HS-RX Differential Return Loss Conformance Limits**

Note that the methodology for this test is essentially the same as the HS transmitter measurement of Test 3.1.1, except the measurement is performed on an HS receiver, and the frequency range is 0 to  $f_{MAX}$ , rather than  $f_{LP,MAX}$  to  $f_{MAX}$ .

Also, rather than requiring the DUT to be forced into a continuous HS transmitting state as was required for the TX measurement, this test requires that the DUT be forced into a state where its HS-RX termination is permanently enabled for the duration of the measurement. This functionality is also considered a vendor-specific feature, and is outside the scope of normal operating behavior, however it is necessary in order for the measurement to be performed.

The Differential Return Loss response must fall below the grayed out region shown in the template in order to be deemed conformant (e.g., there must be *at least* 18dB of return loss at  $f_{LP,MAX}$ , etc). An example measurement result showing a conformant Differential Return Loss response is shown in the figure below.

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**Figure 3.2.1-2: Example Conformant HS-RX Differential Return Loss Result**

**Test Setup:** See Appendix B.3.1.

**Test Procedure:**

- Obtain the value of  $f_{MAX}$  for the DUT that was used in Test 3.1.1.
- Power on and configure the DUT to force its RX into fixed state where the HS-RX termination is enabled.
- Calibrate and configure the Test System for a Differential Return Loss measurement (SDD11) over the frequency range 0 to  $f_{MAX}$ .
- Connect the DUT's Data Lane 0 receiver to the Test System.
- Measure the SDD11 HS-RX Differential Return Loss.
- Repeat the previous two steps for all other Data Lanes, and the Clock Lane.

**Observable Results:**

- For all Clock and Data Lanes, verify that the SDD11 HS-RX Differential Return Loss meets or exceeds the limits shown in the figure above.

**Possible Problems:**

As mentioned in the Discussion above, it is mandatory that the DUT's HS-RX termination be forced into a fixed enabled state in order to properly perform the measurement. Erroneous results may occur if the DUT is incorrectly configured for any other D-PHY state other than High-Speed (e.g., LP Control or Escape).

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**Test 3.2.2 – HS-RX Common-Mode Return Loss (SCC11)**

**Purpose:** To verify that the Common-Mode Return Loss of the DUT's Clock and Data Lane HS receivers exceeds the minimum conformance limits.

**References:**

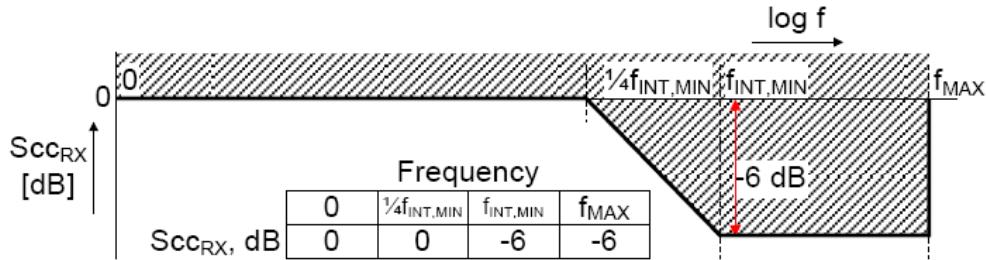
- [1] D-PHY Specification, Section 7.7.2
- [2] Ibid, Section 7.3, Line 1196
- [3] Ibid, Section 8.2.2, Table 23

**Resource Requirements:** See Appendix A.3.

**Last Modification:** November 30, 2009

**Discussion:**

Section 7 of the D-PHY Specification defines the general interconnect and lane configuration requirements for D-PHY products. Section 7.7 defines the Driver and Receiver S-parameter specifications, which includes a specification for RX Common-Mode Return Loss. The specification is defined in terms of a scalable frequency-domain template, reproduced in the figure below.



**Figure 34 Template for RX Common-Mode Return Loss**

**Figure 3.2.2-1: Common-Mode Return Loss Conformance Limits**

The specification states, “*For an RX reflection shall be less than -6 dB for the frequency range  $f_{INT,MIN}$  -  $f_{MAX}$ .*”[1].

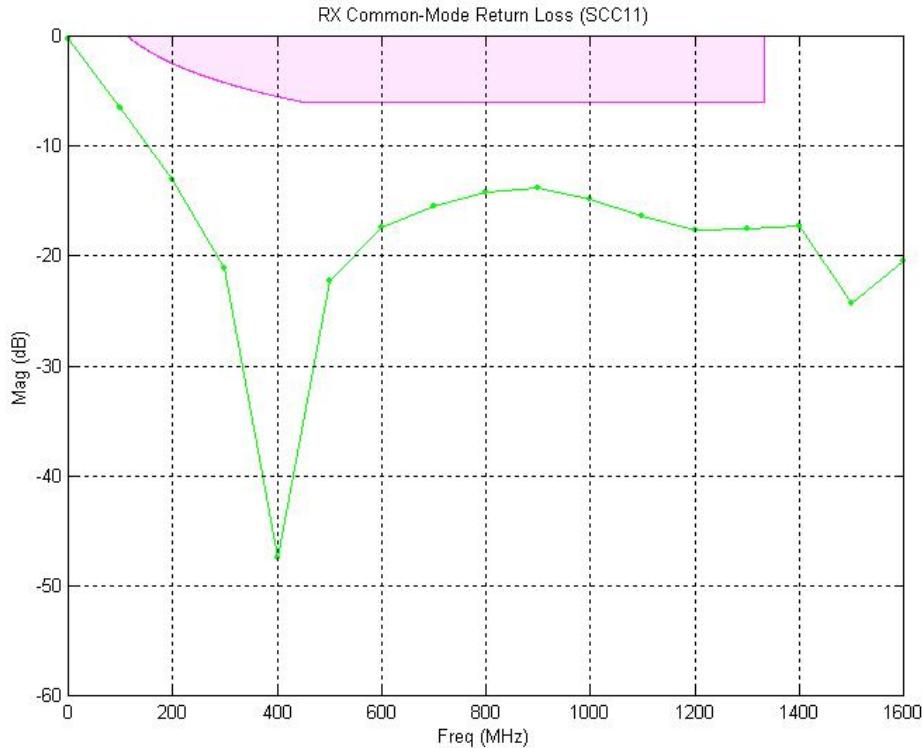
Note that an apparent contradiction exists between the specification text and the conformance template shown in the specification figure. While the text defines a -6dB limit from  $f_{INT,MIN}$  to  $f_{MAX}$ , the figure shows an additional sloping line from  $f_{INT,MIN}$  down to  $\frac{1}{4}f_{INT,MIN}$ . For the purposes of this test, the limits shown in the template will be assumed to be the correct limits.

Regarding the definition of  $f_{INT}$ , the specification states, “*RF interference frequencies are denoted by ‘ $f_{INT}$ ’, where  $f_{INT,MIN}$  defines the lower bound for the band of relevant RF interferers.*”[2]. The value of  $f_{INT,MIN}$  is specified in Table 23 of the specification as a fixed value of 450MHz. [3]

The general methodology for this test is otherwise identical to Test 3.2.1, except the SCC11 S-parameter is measured, and different conformance frequencies/limits are applied.

The RX Common-Mode Return Loss response must fall below the grayed out region shown in the template in order to be considered conformant (e.g., there must be *at least* 6dB of return loss at  $f_{INT,MIN}$ , etc). An example measurement result showing a conformant Common-Mode Return Loss response is shown in the figure below.

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**Figure 3.2.2-2: Example Conformant HS-RX Common-Mode Return Loss Result**

**Test Setup:** See Appendix B.3.1.

**Test Procedure:**

- Obtain the value of  $f_{MAX}$  for the DUT that was used in Test 3.1.1.
- Power on and configure the DUT to force its RX into fixed state where the HS-RX termination is enabled.
- Calibrate and configure the Test System for a Common-Mode Return Loss measurement (SCC11) over the frequency range 0 to  $f_{MAX}$ .
- Connect the DUT's Data Lane 0 receiver to the Test System.
- Measure the SCC11 HS-RX Common-Mode Return Loss.
- Repeat the previous two steps for all other Data Lanes, and the Clock Lane.

**Observable Results:**

- For all Clock and Data Lanes, verify that the SCC11 HS-RX Common-Mode Return Loss meets or exceeds the limits shown in the figure above.

**Possible Problems:**

See Possible Problems comments for Test 3.2.1. The same applies to this test.

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**Test 3.2.3 – HS-RX Mode Conversion Limits (SDC11)**

**Purpose:** To verify that the Mode Conversion S-parameters of the DUT's Clock and Data Lane HS receivers exceed the minimum conformance limits.

**References:**

[1] D-PHY Specification, Section 7.7.3, Line 1291

**Resource Requirements:** See Appendix A.3.

**Last Modification:** November 30, 2009

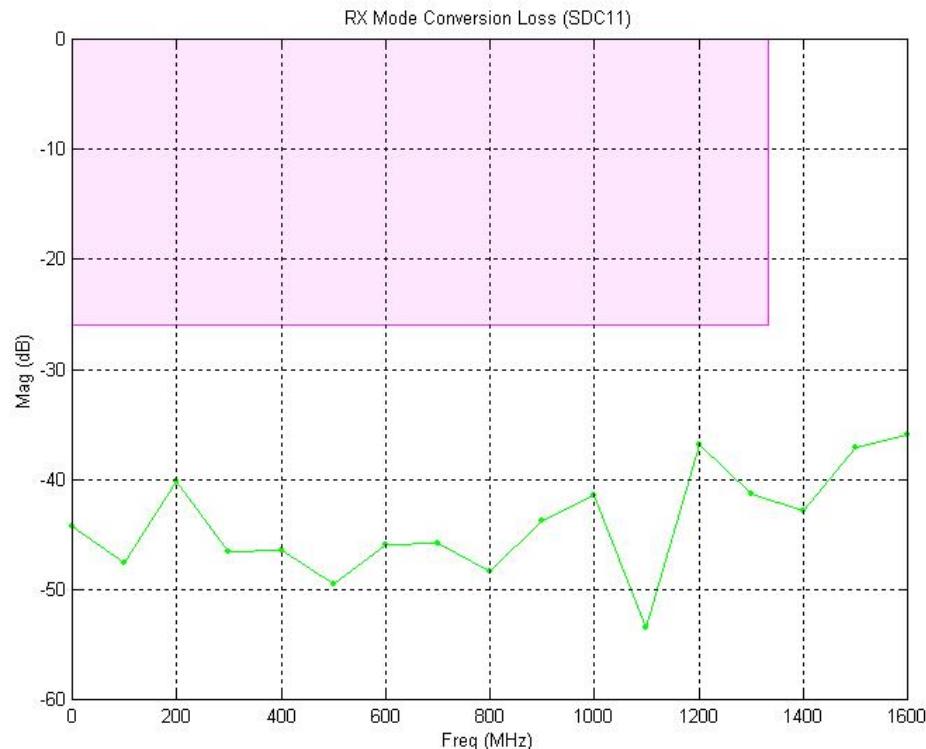
**Discussion:**

Section 7 of the D-PHY Specification defines the general interconnect and lane configuration requirements for D-PHY products. Section 7.7 defines the Driver and Receiver S-parameter specifications, which includes a specification for RX Mode Conversion Limits.

The specification states, “*The differential to common-mode conversion limits of TX and RX shall be -26dB up to  $f_{MAX}$ .*”[1].

(The general methodology for this test is otherwise identical to Test 3.2.2, except the SDC11 S-parameter is measured, and different conformance frequencies/limits are applied.)

The HS-RX Mode Conversion Loss shall be greater than 26dB over the frequency range 0 to  $f_{MAX}$  in order to be considered conformant. An example measurement result showing a conformant Mode Conversion Loss response is shown in the figure below.



**Figure 3.2.3-1: Example Conformant HS-RX Mode Conversion Loss Result**

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**Test Setup:** See Appendix B.3.1.

**Test Procedure:**

- Obtain the value of  $f_{MAX}$  for the DUT that was used in Test 3.1.1.
- Power on and configure the DUT to force its RX into fixed state where the HS-RX termination is enabled.
- Calibrate and configure the Test System for an SDC11 measurement over the frequency range 0 to  $f_{MAX}$ .
- Connect the DUT's Data Lane 0 receiver to the Test System.
- Measure the SDC11 HS-RX Mode Conversion Loss.
- Repeat the previous two steps for all other Data Lanes, and the Clock Lane.

**Observable Results:**

- For all Clock and Data Lanes, verify that the SDC11 HS-RX Mode Conversion Loss is greater than 26dB across the frequency range 0 to  $f_{MAX}$ .

**Possible Problems:**

See Possible Problems comments for Test 3.2.1. The same applies to this test.

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**Test 3.2.4 – HS-RX DC Differential Input Impedance ( $Z_{ID}$ )**

**Purpose:** To verify that DC Differential Input Impedance ( $Z_{ID}$ ) of the DUT's HS-RX line termination is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 7.7, Line 1269
- [2] Ibid, Section 8.2.1, Line 1464
- [3] Ibid, Section 8.2.1, Table 20

**Resource Requirements:** See Appendix A.3.

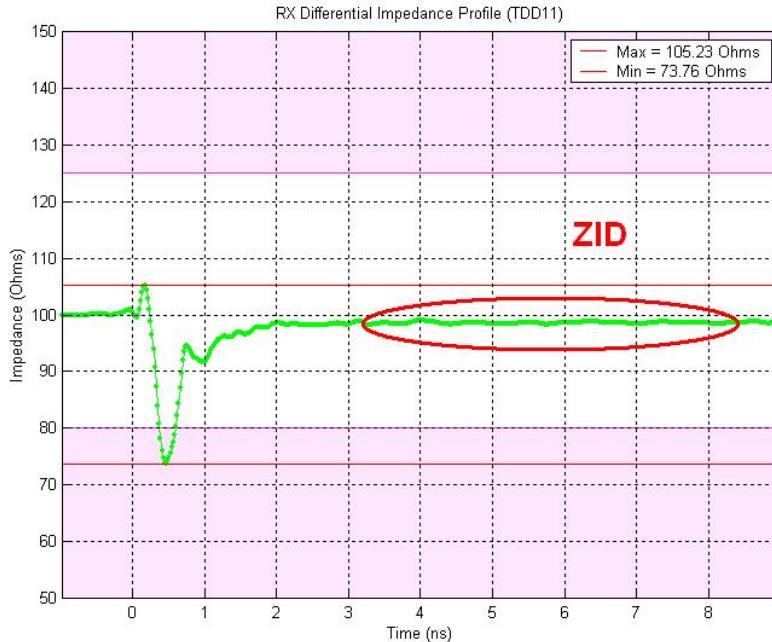
**Last Modification:** November 30, 2009

**Discussion:**

The D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $Z_{ID}$ , which is the DC Differential Input Impedance, and is the impedance of the receiver's HS-RX line termination.

Note there are two references to the HS-RX low-frequency impedance requirements found in the specification. The first is found included with the return loss specifications, which states, "*The low-frequency impedance range for line terminations at Transmitter and Receiver is 80-125 Ohm.*"[1]. However, the main specification is for the  $Z_{ID}$  parameter, for which the specification states, "*During operation of the HS receiver, termination impedance  $Z_{ID}$  is required between the Dp and Dn pins of the HS receiver.  $Z_{ID}$  shall be disabled when the module is not in the HS receive mode.*"[2].

In this test, the  $Z_{ID}$  value of the DUT's Clock and Data Lane HS receivers will be measured. While multiple valid methods may be used to measure  $Z_{ID}$ , this test suite uses a TDR-based approach, where the HS-RX line termination value is determined from the measured TDR impedance profile. The value of  $Z_{ID}$  is measured as the final, settled value of the differential impedance profile. An example measurement is shown in the figure below.



**Figure 3.2.4-1: Example HS-RX  $Z_{ID}$  Measurement**

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The setup for this test is identical to Tests 3.2.1 - 3.2.3, in that the DUT must be configured such that its HS-RX line termination is forced on for the duration of the measurement (see Test 3.2.1 Discussion).

For all Clock and Data Lanes, the value of  $Z_{ID}$  shall be within the range of 80 to 125 Ohms in order to be considered conformant [3].

**Test Setup:** See Appendix B.3.1.

**Test Procedure:**

- Power on and configure the DUT to force its RX into fixed state where the HS-RX termination is enabled.
- Calibrate and configure the Test System for a differential impedance profile measurement.
- Connect the DUT's Data Lane 0 receiver to the Test System.
- Measure  $Z_{ID}$ , as described above.
- Repeat the previous two steps for all other Data Lanes, and the Clock Lane.

**Observable Results:**

- For all Clock and Data Lanes, verify that  $Z_{ID}$  is between 80 and 125 Ohms.

**Possible Problems:**

See Possible Problems comments for Test 3.2.1. The same applies to this test.

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## **GROUP 3: LP-TX/RX IMPEDANCE REQUIREMENTS**

**Overview:**

This group of tests verifies several LP-TX and LP-RX low-frequency (DC) impedance requirements defined in Section 8 of the D-PHY Specification.

**Status:**

The test descriptions contained in this group are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

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**Test 3.3.1 – LP-TX Output Impedance ( $Z_{OLP}$ )**

**Purpose:** To verify that the Low-Power Output Impedance ( $Z_{OLP}$ ) of the DUT's LP transmitters are greater than the minimum allowed value.

**References:**

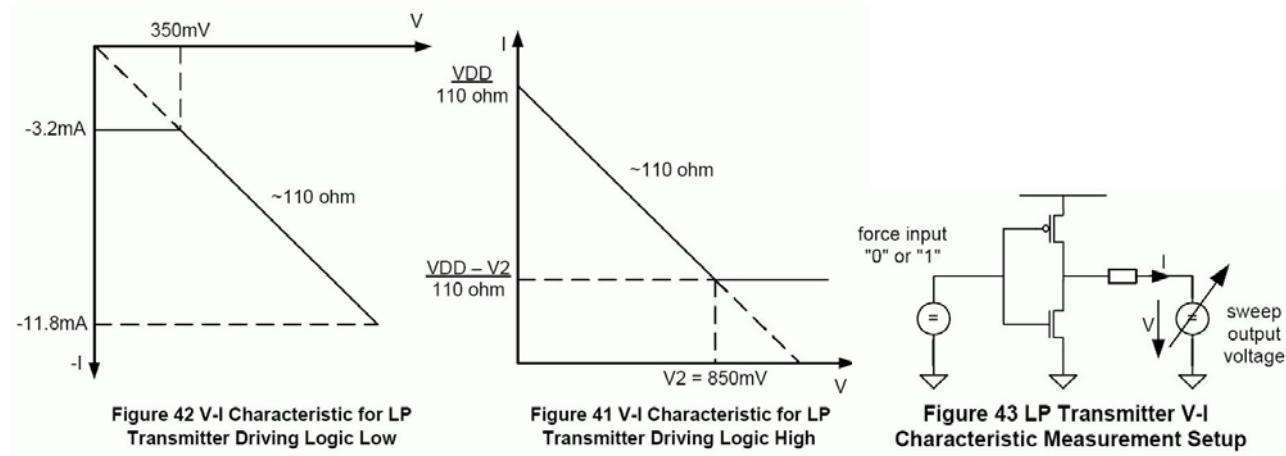
- [1] D-PHY Specification, Section 8.1.2
- [2] Ibid, Section 8.1.2, Table 18

**Resource Requirements:** See Appendix A.3

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $Z_{OLP}$ , which is a device's LP Output Impedance. The D-PHY Specification defines the LP Output Impedance as  $Z_{OLP} = |(V_{THEVENIN} - V_{PIN}) / I_{OUT}|$ . It also defines the circuit below to be used for measuring  $Z_{OLP}$ , which is used to create the following I-V curves for the Logic-High and Logic-Low states, also shown below.



**Figure 3.3.1-1: VI Characteristic Plots, and Setup for  $Z_{OLP}$  Measurement**

In this test, the DUTs  $Z_{OLP}$  for both the Dp and Dn LP transmitters of each Lane will be measured using a voltage source and a current meter while the DUT is driving a constant LP-00 and LP-11 state.

For the Logic-Low case, the V-I characteristic will be determined by measuring two data points, while the LP-TX is sourcing a continuous LP-00 state. These will be the measured currents  $I_1$  and  $I_2$ , for applied voltage values 350mV and 450mV, respectively. These two voltage/current pairs will determine a line on the V-I graph (as shown above), the slope of which will be the  $Z_{OLP}$  Output Impedance, and will be computed as  $Z_{OLP(0)} = (450-350) / \text{abs}(I_1 - I_2)$ . This measurement will be performed separately for the Dp and Dn LP transmitters.

For the Logic-High case, a similar procedure will be applied, where the currents  $I_1$  and  $I_2$  for applied voltage levels of 850mV and 550mV will be measured, and used to plot/compute the  $Z_{OLP}$  value for the LP-11 case, where  $Z_{OLP(1)} = (850-550) / \text{abs}(I_1 - I_2)$ .

For all Lanes, the values of  $Z_{OLP(0)}$  and  $Z_{OLP(1)}$  for both Dp and Dn must be greater than 110 Ohms in order to be considered conformant [2].

**Test Setup:** See Appendix B.3.2

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**Test Procedure:**

- Power on the DUT and connect the DUT's Data Lane 0 to the Test Setup.
- Create a condition that causes the DUT to source a continuous LP-00 state.
- Measure the V-I Characteristic, and compute  $Z_{OLP(0)}$  for the Dp LP-0 state, as described above.
- Measure the V-I Characteristic, and compute  $Z_{OLP(0)}$  for the Dn LP-0 state, as described above.
- Create a condition that causes the DUT to source a continuous LP-11 state.
- Measure the V-I Characteristic, and compute  $Z_{OLP(1)}$  for the Dp LP-1 state, as described above.
- Measure the V-I Characteristic, and compute  $Z_{OLP(1)}$  for the Dn LP-1 state, as described above.
- Repeat all of the above steps for all other Data Lanes, and the Clock Lane.

**Observable Results:**

For all Clock and Data Lanes:

- Verify that  $Z_{OLP(0)}$  for Dp is greater than 110 Ohms.
- Verify that  $Z_{OLP(0)}$  for Dn is greater than 110 Ohms.
- Verify that  $Z_{OLP(1)}$  for Dp is greater than 110 Ohms.
- Verify that  $Z_{OLP(1)}$  for Dn is greater than 110 Ohms.

**Possible Problems:**

Note that this test is typically performed on CSI-2 and DSI Master devices only (e.g., camera sensors in the CSI-2 case, and host processors in the DSI case.) It can also be performed on ‘bare-phy’ DUT types. However it is not typically possible to perform this test on Slave devices (e.g., DSI displays), as the Slave’s LP-TX is only active during a Bus Turnaround event, which is not sufficient for test purposes. The measurement could be performed in these cases if a vendor-specific means exists to force a Slave device’s LP-TX into the fixed LP-11 and LP-00 states required for this test.

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**Test 3.3.2 – LP-RX Input Leakage Current ( $I_{LEAK}$ )**

**Purpose:** To verify that the leakage current of the DUT's LP receiver is within the conformance limits.

**References:**

- [1] D-PHY Specification, Section 8.4, Line 1534
- [2] Ibid, Section 8.4, Line 1544
- [3] Ibid, Section 8.4, Table 25

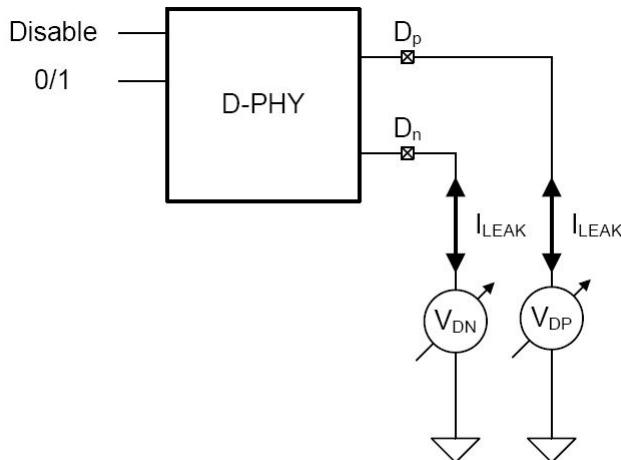
**Resource Requirements:** See Appendix A.3

**Last Modification:** September 16, 2010

**Discussion:**

Section 8 of the D-PHY Specification defines the Electrical Characteristic requirements for D-PHY products. Included in these requirements is a specification for  $I_{LEAK}$ , which is a device's LP-RX leakage current.

The specification states, “*When the PHY is in the Low-Power receive mode the pad pin leakage current shall be  $I_{LEAK}$  when the pad signal voltage is within the signal voltage range of  $V_{PIN}$ . The specification of  $I_{LEAK}$  assures interoperability of any PHY in the LP mode by restricting the maximum load current of an LP transmitter. An example test circuit for leakage current measurement is shown in Figure 50.*”[1]. A copy of the specification figure is provided below.



**Figure 50 Pin Leakage Measurement Example Circuit**

**Figure 3.3.2-1: Example  $I_{LEAK}$  Measurement Diagram  
(copied from D-PHY specification)**

The specification also states that the leakage requirements are to be met, “*When the pad voltage is in the signal voltage range from  $V_{GNDSH,MIN}$  to  $V_{OH} + V_{GNDSH,MAX}$  and the Lane Module is in LP receive mode.*”[2]. This corresponds to a range of -50mV to 1350mV.

In this test, the leakage current of the DUT's LP-RX Lanes will be measured using an ammeter with picoamp resolution (or smaller), while a voltage is applied at the RX, and varied across the range of -50mV to 1350mV.

For all Lanes, the leakage current,  $I_{LEAK}$ , should be between -10uA and +10uA for all applied voltage values between -50mV and 1350mV (inclusive)[3].

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**Test Setup:** See Appendix B.3.3

**Test Procedure:**

- Power on the DUT and connect DUT Data Lane 0 to the Test Setup.
- Set the applied voltage to -50mV.
- Observe the leakage current  $I_{LEAK}$ .
- Slowly increase the applied voltage, in increments no greater than 50mV.
- For each incremental applied voltage level, observe the leakage current  $I_{LEAK}$ .
- Repeat the previous two steps for all applied voltage levels up to and including 1350mV.
- Report the maximum observed current (positive or negative), and respective applied voltage level, as the final  $I_{LEAK}$  result for the given Lane.
- Repeat the previous seven steps for all other Data Lanes, and the Clock Lane.

**Observable Results:**

- For all Clock and Data Lanes, verify that  $I_{LEAK}$  is between -10 and +10uA.

**Possible Problems:**

Note that this test is typically performed on CSI-2 and DSI Slave devices only (e.g., host processors in the CSI-2 case, and LCD display panels in the DSI case.) It can also be performed on ‘bare-phy’ DUT types. However it is not typically possible to perform this test on Master devices (e.g., DSI host processors), as the Master’s LP-RX is only active during a Bus Turnaround event, which is not sufficient for test purposes. The measurement could be performed in these cases if a vendor-specific means exists to force a Master DUT’s LP-RX into the state required for this test.

## APPENDICES

**Overview:**

Test suite appendices are intended to provide additional low-level technical detail pertinent to specific tests contained in this test suite. These appendices often cover topics that are outside of the scope of the standard, and are specific to the methodologies used for performing the measurements in this test suite. Appendix topics may also include discussion regarding a specific interpretation of the standard (for the purposes of this test suite), for cases where a particular specification may appear unclear or otherwise open to multiple interpretations.

**Scope:**

Test suite appendices are considered informative supplements, and pertain solely to the test definitions and procedures contained in this test suite.

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## Appendix A – Resource Requirements (DUT and Test Equipment)

**Purpose:** To define the test equipment and DUT requirements necessary for performing the tests in this test suite.

**References:** None.

**Last Modification:** September 16, 2010

**Discussion:**

### A.1: LP/HS Transmitter Tests:

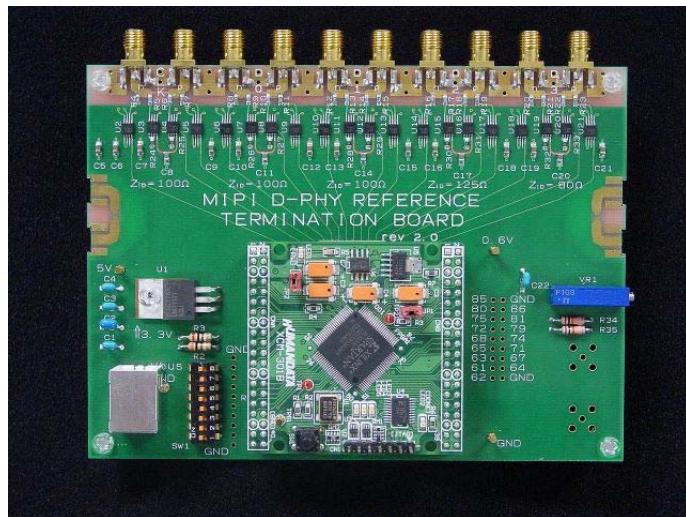
The LP and HS Transmitter tests of Section 1 are designed and organized to be performed in groups, using several test setups. Currently, different setups are used for the HS versus LP measurements, as more accurate results can be obtained using configurations that are optimized for each case, rather than trying to perform all tests using a single setup. The reasons for this pertain to, 1) the difference in termination requirements for the LP vs. HS signaling cases, and 2) the difference in signal amplitude levels between the LP and HS signals. (More information on this topic appears below.)

#### Equipment Requirements

In order to perform the LP and HS Clock and Data Lane transmitter tests of Section 1, the following resources are required:

- 1 x DUT, properly mounted on an SMA-based evaluation PCB that meets the Test Vehicle Board (TVB) guidelines. (See *DUT Requirements* section below).
- 1 x Four-Channel Real-Time Digital Storage Oscilloscope (DSO), 4GHz bandwidth or greater
- 4 x High-Impedance, Low Capacitive Load Differential Probes, 4GHz bandwidth or greater
- 4 x SMA Test Cables
- 1 x MIPI D-PHY Reference Termination Board (RTB) (*See MIPI Test Program Page*, and Figure A.1-1 below)
- 1 x MIPI D-PHY LP Capacitive Load (CLOAD) Fixture (*See MIPI Test Program Page*)
- Post-processing software. (e.g., [DPHYGUI](#), or equivalent DSO-specific software.)

These components will be used in the various test setup diagrams shown in Appendix B of this document.



**Figure A.1-1: MIPI D-PHY Reference Termination Board (RTB)**

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*DUT Requirements*

In addition to test equipment requirements, it is also necessary to specify requirements for the Device Under Test (DUT). These requirements are necessary to ensure accurate and consistent measurements in a proper test environment, and to provide configuration support for all required operating modes needed for performing the various tests.

**Test PCB Requirements:** In order to measure the DUT characteristics under proper test conditions, and also to interface the DUT to the measurement equipment, there are several requirements for how the DUT is mounted.

The DUT should be mounted on a signal-integrity-grade evaluation board, with all D-PHY signals brought out to individual SMA connectors. The individual + and – signals for each Lane pair should be decoupled and routed to 50-ohm single-ended PCB traces as near to the DUT IC as possible. All high-speed D-PHY signal trace lengths must be matched (i.e., Clock Lane matched to Data Lane). Measurement-grade, controlled-impedance end-launch SMA connectors should be used.

In addition to the routing of the SMA signals, probing points are also required, in order to access the D-PHY signals as close to the IC pins as possible. Each single-ended PCB trace must have test points that will allow a differential probe to be used in order to measure the signal with respect to ground. Thus, each test point must have an associated ground point.

The UNH IOL has created a freely available PCB design template for MIPI test purposes, known as the Test Vehicle Board, which includes the necessary high-speed SMA and probing point requirements, and may be freely modified by vendors to suit their individual D-PHY-based devices. (Note this is only a generic design template, which vendors must customize and fabricate themselves, prior to submitting products for testing.) The Gerber files for the TVB (along with schematics, design guidelines, and other information) are available on the [MIPI Alliance Testing Program Page](#).

Note that the recommended approach of using a high-quality evaluation PCB which is optimized for signal integrity is intended as a practical and reasonably cost-effective method for performing reasonable conformance measurements across a variety of DUT types. The methods described in this test suite are geared toward demonstrating conformance of CSI and DSI products, and are by no means optimal, but rather seek a balance between measurement accuracy and cost/complexity. It is possible to obtain higher-accuracy results (e.g., for characterization purposes) for many tests through the use of more sophisticated PCB/fixturing designs, termination methods, and probing techniques. Also, de-embedding of test fixturing can also improve measurement accuracy. Use of these techniques is not discouraged if such resources are available.

**HS Burst Mode Configurability:** Devices desiring HS-TX testing must be capable of being configured to transmit arbitrary CSI or DSI traffic via HS bursts. While there is currently no specific test pattern or test mode defined for TX testing, devices must be able to source a repeated HS burst sequence of approximately 20K-50K HS bits in length, containing a high-transition-density data pattern (i.e., a burst containing many edges, and with a wide distribution of run-lengths). Pseudo-random pixel data is ideal. For best results, frames should not have ‘long’ sequences of all-zero or all-one data, whereby the maximum run length during the packet data should be less than the  $T_{HS-ZERO}$  or  $T_{HS-TRAIL}$  periods for a given DUT. Longer HS bursts are preferable to shorter ones, however the HS-TX must return to the LP-11 Stop state between HS bursts, and the HS bursts should be transmitted as frequently as possible.

**LP Escape Mode Configurability:** Devices desiring LP-TX testing must be capable of being configured to transmit Escape Mode entry codes for all supported commands (DSI devices). CSI devices must be able to transmit a ULPS Escape Mode sequence on all Data Lanes, as well as the Clock Lane ULPS entry sequence on the Clock Lane, in order for LP-TX measurements to be performed.

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**A.2: Receiver Tests:**

*Equipment Requirements*

In order to perform the HS-RX and LP-RX tests of Section 2, the following resources are required:

- A multichannel, programmable lab-grade signal source, capable of generating appropriate HS and LP signaling. (Note that the HS and LP signaling components can be generated by separate sources, and combined externally using resistive splitters/combiners.)

Also, a receiver test setup additionally requires all of the resources necessary for performing TX measurements (see Appendix A.1), which are necessary for measuring and calibrating the output of the signal source used to generate the RX test signals.

*DUT Requirements*

Furthermore, for receiver testing, DUTs must provide a suitable observation mechanism that allows for verification of the received data that is transmitted to the DUT during a receiver test. Note that the exact observation mechanism will depend on the type of DUT, and may require additional supporting hardware, depending on the DUT type. A detailed description of RX observation mechanisms for several different DUT types is presented in Appendix G of this document.

**A.3: S-Parameter and Impedance Tests:**

*Equipment Requirements*

In order to perform the HS and LP TX/RX impedance tests of Section 3, the following resources are required:

- A Time-Domain Reflectometer (TDR) with S-parameter capability.
- A lab-grade variable voltage source
- An ammeter with milliamp resolution
- An ammeter with picoamp resolution

*DUT Requirements*

The HS S-parameter/return loss tests require measurement of the DUT's HS termination, which is typically only enabled during an HS burst. As this time is not long enough to perform an S-parameter measurement, DUTs must support a vendor-specific mechanism for manually enabling and disabling the HS-RX termination. Also, to measure S-parameters for HS transmitters, the DUT must be placed into a state where it can transmit a continuous HS data pattern. The ideal pattern for this purpose depends on the instrument being used to perform the S-parameter measurements. If a VNA is used, a long, pseudo-random pattern is preferred in order to minimize error in the measurement. If a TDR/TDNA is used, a ‘clock pattern’ (e.g., repeating 1010 or 1100) will yield the best results. (Also, ‘static’ test modes that transmit a continuous HS-1 and HS-0 can be used with either a VNA or TDR to isolate the static impedance of the HS-TX, however the recommended methodology for performing S-parameter measurements is to test the interface while in a dynamic transmitting state.)

Also, for the low-frequency LP-TX impedance tests ( $Z_{OLP}$ ), it must be possible to configure the LP-TX to fixed LP-11 and LP-00 states for the measurements. While this may be done using vendor-specific methods, the LP-11 state can typically be measured during the Stop state during normal operation (if the DUT can be configured to not transmit any other data, i.e., disabling HS burst transmission.) Also, the LP-00 state can be measured during the LP-00 Space state following a ULPS entry sequence. (Note that DUTs are required to support the ULPS entry command on all Lanes in order to perform the LP-TX signaling measurements anyway, so this should not be a problem.)

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**Appendix B – Test Setups**

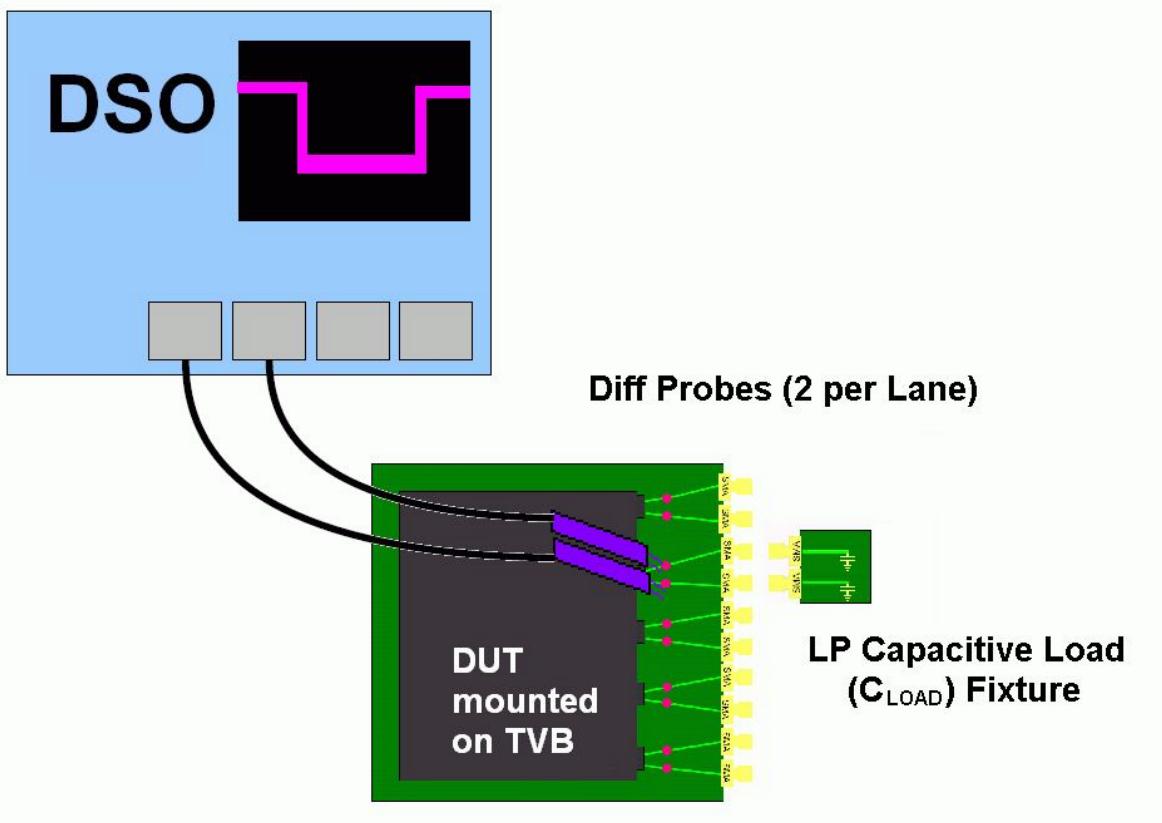
**Purpose:** To define the basic test setups used for performing the tests in this test suite.

**References:** None.

**Last Modification:** November 30, 2009

**Discussion:**

**B.1.1: LP Transmitter Tests:**

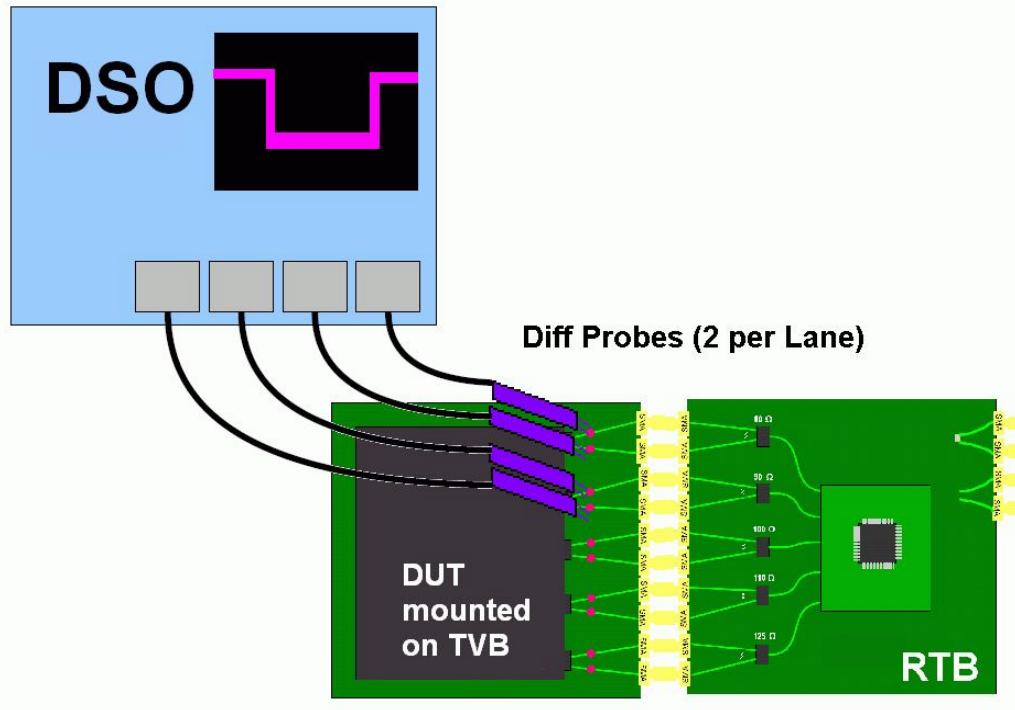


**Figure B-1-1: LP Transmitter Test Setup**

Notes on the above setup:

- The DUT is connected to the DSO using two high-bandwidth differential probes.
- Differential probes are connected to the test points on the DUT Test Vehicle Board (TVB), and each differential probe measures the single-ended + or - signal with respect to PCB ground.
- The DUT should be configured to transmit a ULPS entry sequence on all Lanes.
- The DSO vertical gain should be optimized so that the LP signaling spans as much of the vertical height of the DSO screen as possible.
- Capacitive Test Load Fixture is either connected to TVB (maximum  $C_{LOAD}$ ), or left disconnected (minimum  $C_{LOAD}$ ), according to specific LP test requirements.

**B.1.2: HS Transmitter Tests:**



**Figure B-1-2: HS Transmitter Test Setup**

Notes on the above setup:

- The DUT is connected to the DSO using four high-bandwidth, low capacitance differential probes.
- Differential probes are connected to the test points on the DUT Test Vehicle Board (TVB), and each differential probe measures the single-ended + or - signal with respect to PCB ground.
- The Reference Termination Board (RTB) provides a reference termination environment, and actively switches in/out a precision HS resistive termination ( $Z_{ID}$ ), simulating an ‘ideal’ D-PHY receiver.
- The RTB is designed to have a resistive termination ( $Z_{ID}$ ) value of 100 ohms on the Clock, Data 0, and Data 1 Lanes. Data Lanes 2 and 3 of the RTB have  $Z_{ID}$  values of 125 and 80 ohms, respectively. This provides reference terminations with maximum and minimum  $Z_{ID}$  values, which are required for some tests. However note that for these tests, the RTB must be repositioned to connect the desired  $Z_{ID}$  Lane to the DUT Lane being measured.
- The DUT should be configured to transmit a continuous stream of HS bursts.
- The DSO vertical gain should be optimized so that the DUT signaling spans as much of the vertical height of the screen as possible.

**B.1.3: Bus Turnaround Tests:**

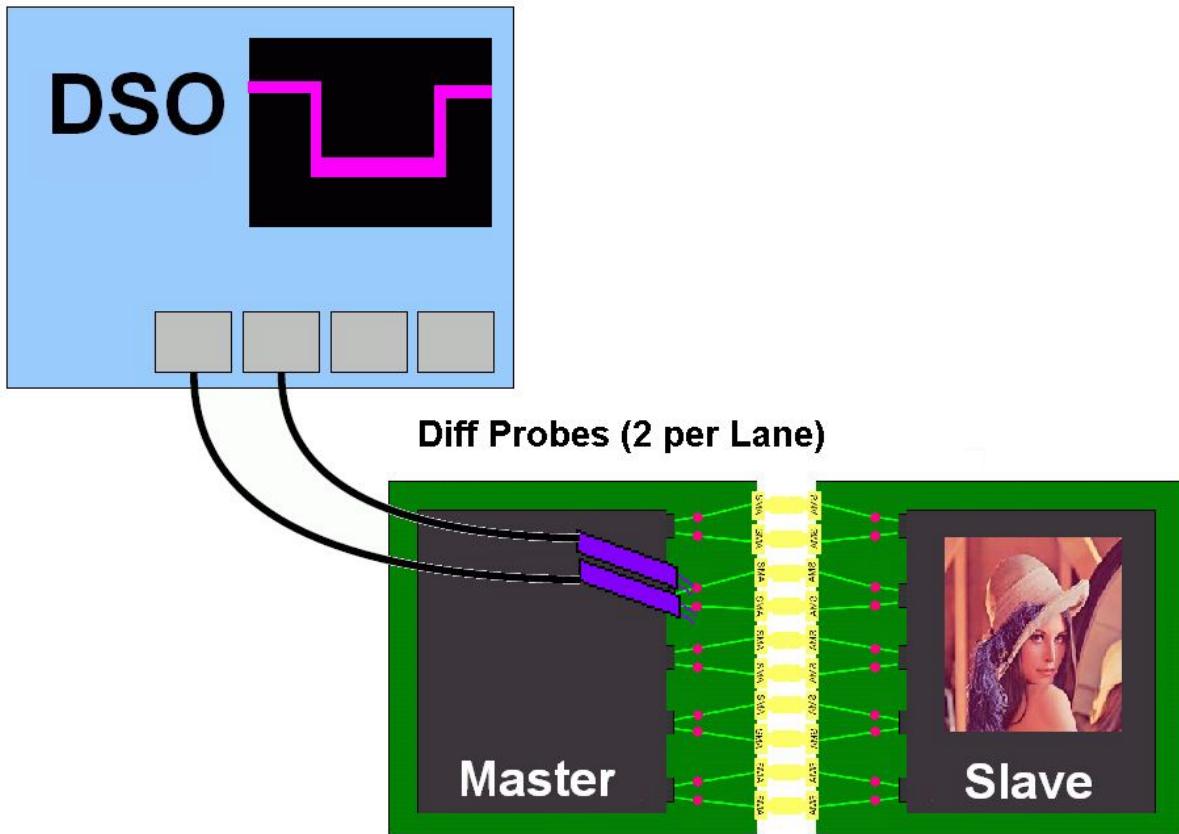


Figure B-1-3: Bus Turnaround Test Setup

Notes on the above setup:

- Note the figure above is only for reference (see further below).
- The general purpose of this setup is to probe the link between a Master and Slave device in order to observe a Bus Turnaround event. For the BTA tests, it is possible for the DUT be either the Master or the Slave in the above diagram, depending on the DUT type (see further below).
- If the DUT is a MASTER device, the tests are performed using either of the following as the Slave device:
  - 1) An actual Slave device that supports Bus Turnaround, or
  - 2) A piece of test equipment (e.g., signal source, protocol generator) that can implement a Bus Turnaround.
- If the DUT is a SLAVE device, the tests can be performed using either of the following as the Master:
  - 1) An actual Master device that supports Bus Turnaround, or
  - 2) A piece of test equipment (e.g., signal source, protocol generator) that can implement a Bus Turnaround.
- The Data Lane 0 link between Master and Slave is probed using two high-bandwidth, low capacitance differential probes.
- Differential probes may be connected at any point between the Master and Slave, and each differential probe measures the single-ended + or - signal with respect to PCB ground.
- In order to best observe the drive overlap period during the turnaround event, it is recommended that the Master and Slave be configured to use different (but still valid)  $V_{OL}$  (LP-0) levels, if possible.

**B.2: Receiver Tests:**

(Note: In addition to the diagrams below, also see Appendix G for a more complete discussion regarding the different options for RX test observables for various DUT types.)

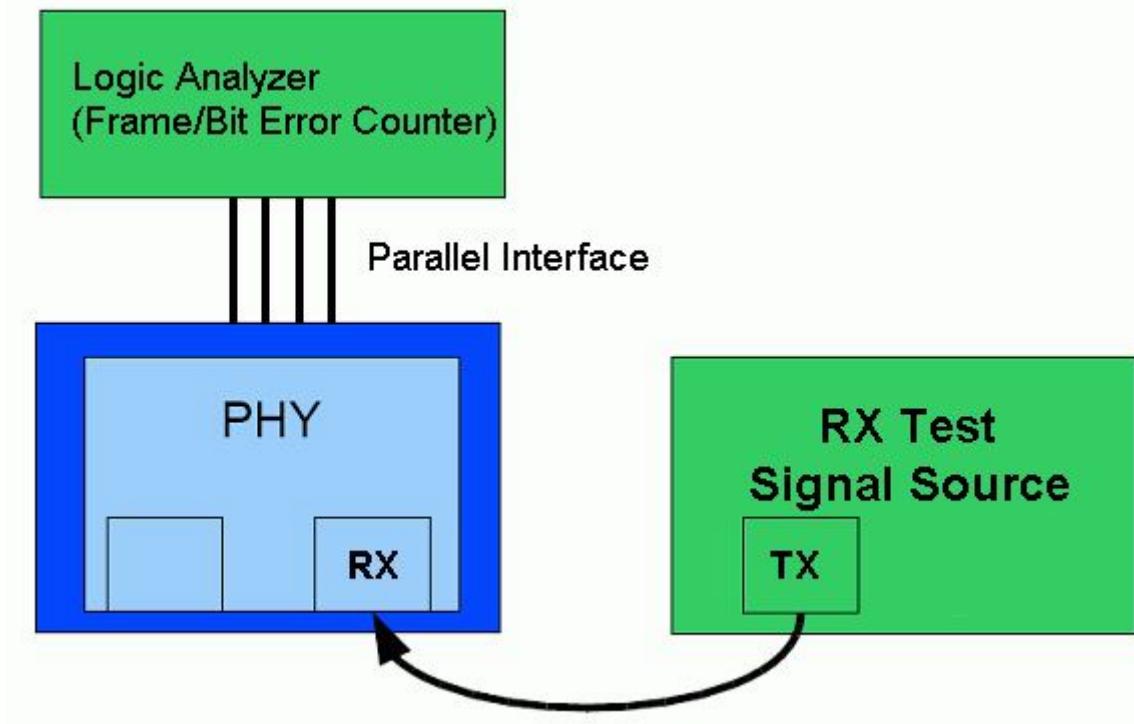


Figure B-2a: LP/HS-RX Test Setup (Bare Phy)

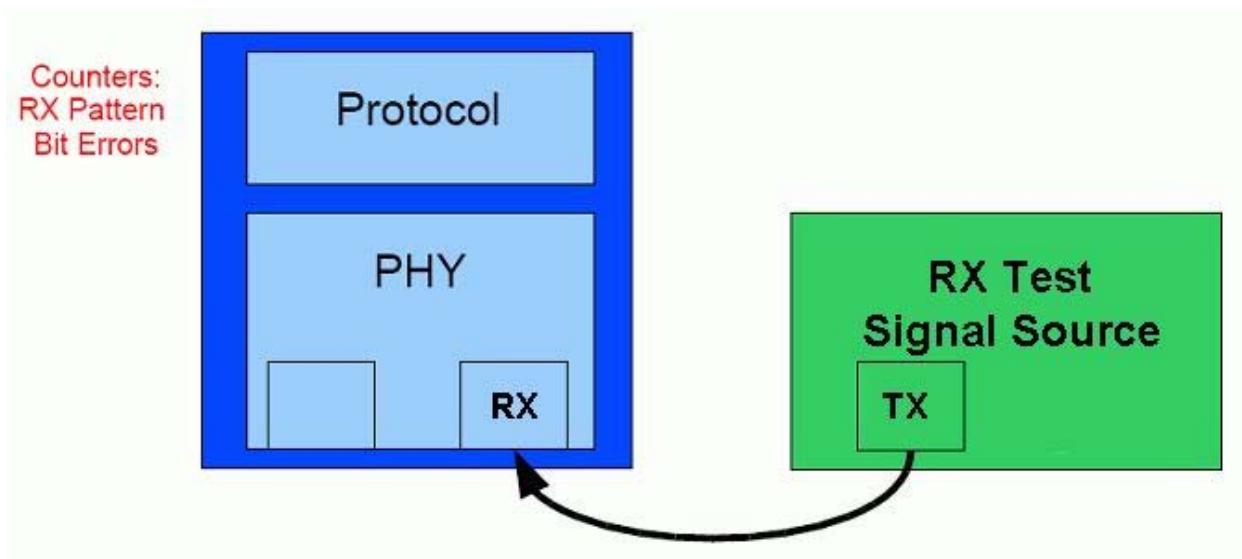
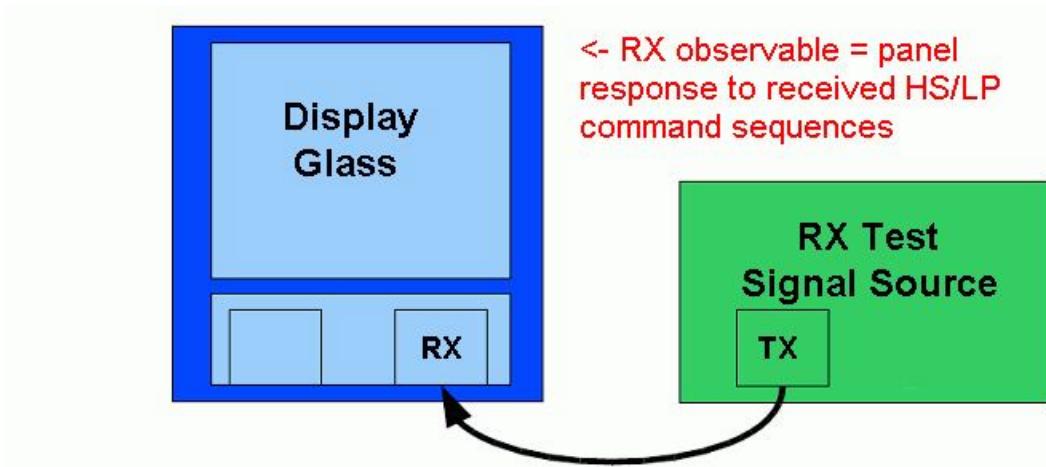
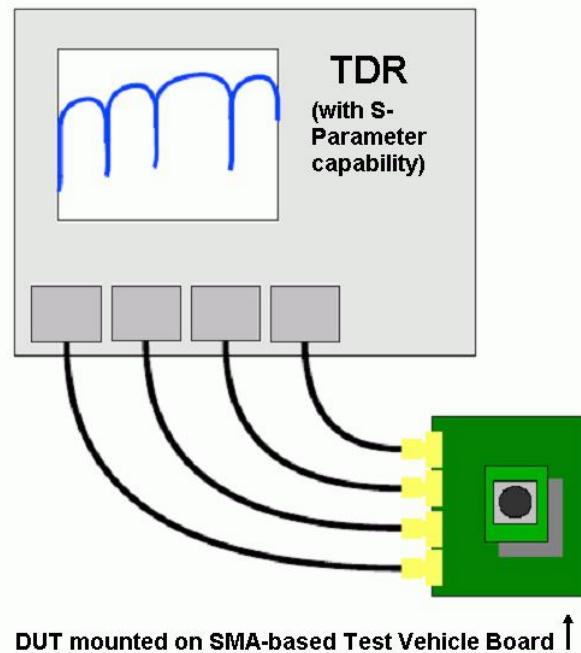


Figure B-2b: LP/HS-RX Test Setup (Combined IC with Phy + Protocol Layers)



**Figure B-2c: LP/HS-RX Test Setup (Complete Display Device)**

**B.3.1: Impedance and S-Parameter Tests:**



**Figure B-3-1: S-Parameter/Return Loss Test Setup**

B.3.2: LP-TX Output Impedance:

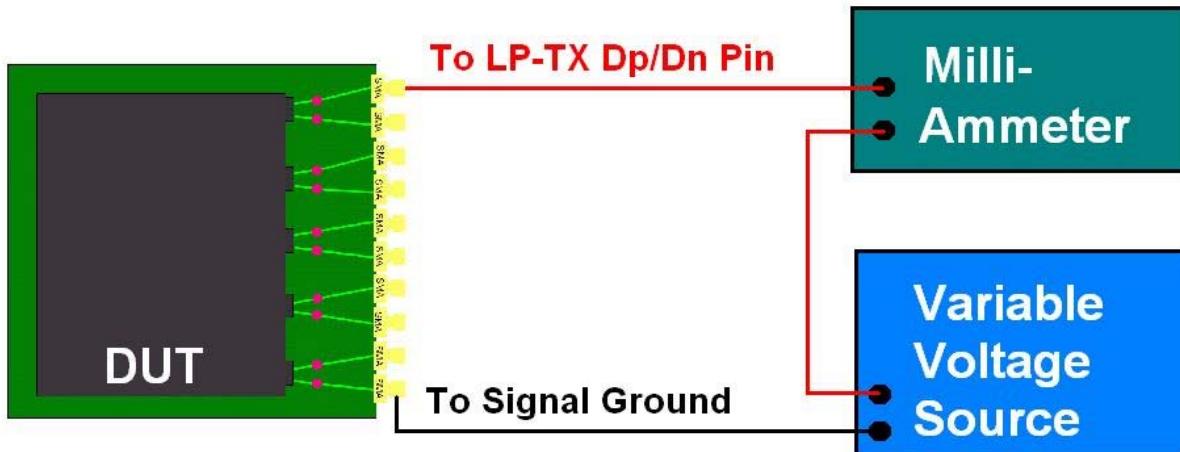


Figure B-3-2: LP-TX Output Impedance ( $Z_{OLP}$ ) Test Setup

B.3.3: LP-RX Input Leakage Current:

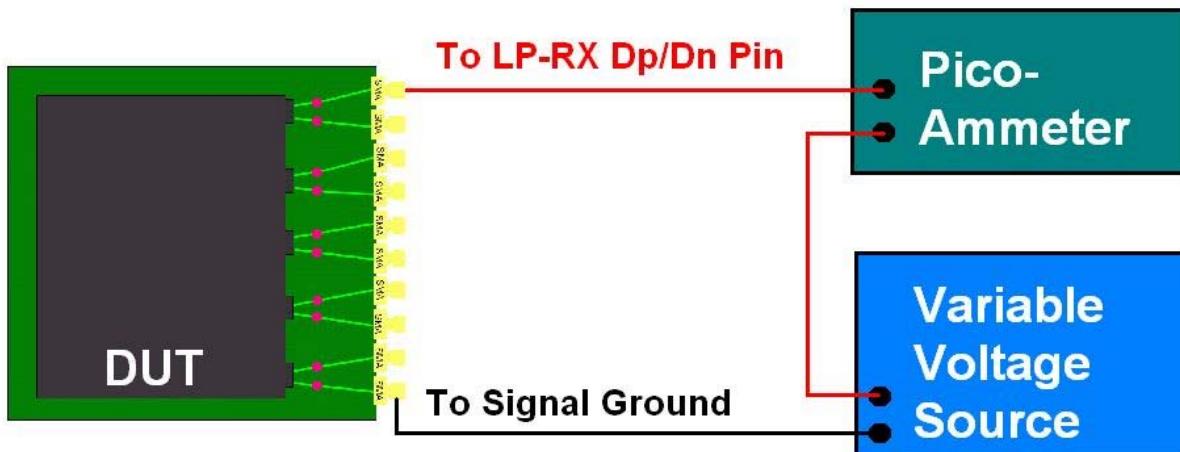


Figure B-3-3: LP-RX Input Leakage Current ( $I_{LEAK}$ ) Test Setup

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## Appendix C – Generic Receiver Test Sequence Template

**Purpose:** To define a generic reference test sequence framework, which may be used as a template for creating a specific ‘master’ receiver test pattern for a particular DUT, which can then be modified to perform various receiver tolerance tests.

**References:** None.

**Last Modification:** November 30, 2009

**Discussion:**

### C.1: Introduction:

The receiver tolerance tests of Section 2 of this document require specific test patterns in order to be performed. Due to the wide variety of D-PHY-based products, and different protocols used, it is generally difficult to define single, simple test patterns for each test. In most cases the test patterns involve slight modifications to an otherwise valid (i.e., protocol-conformant) image data stream.

However, there are several common factors to many of the test pattern and protocol requirements for different types of D-PHY-based DUTs. Because of this, it is possible to combine many of the test elements into a ‘Master’ modular test sequence, which can then be customized according to each individual test’s requirements. This customization is typically accomplished by inserting, deleting, or otherwise modifying various aspects of the master test sequence’s data, and/or analog signaling characteristics.

The purpose of this appendix is to define the general structure of the master test sequence, and explain its various components. The first step in performing receiver tolerance testing will involve the construction of a valid protocol sequence for the DUT, based on this initial framework, as well as any specific protocol, timing, and configuration requirements that may be required by the DUT.

### C.2: General Test Sequence Framework:

The general structure of the master test sequence is shown in the table below. (See detailed explanation following the table.)

**Table C-1: Generic Test Sequence Structure**

Lane	LP-00	INIT	CONFIG	ESCAPE/ULPS	WAKEUP	IMAGE DATA
Clock:	LP-00 on all Clock	LP-11 on all Clock	Vendor-specific DUT configuration. (Valid HS frames, or LPDT frames on Data0.)	LP-11 + Clock ULPS Entry + LP-00	LP-00 + Mark-1 (LP- 10) for TWAKEUP (1ms) + LP- 00, on all Clock and Data Lanes	Valid repeating CSI-2 or DSI HS image data sequence/ stream, containing all necessary protocol and timing requirements for the DUT, and appropriate clocking (burst or continuous mode, burst preferred if supported).
Data0:						
...						
DataN:			Optional, if required by DUT	LP-11 + Escape Mode Entry + ULPS command + LP-00, on all Data Lanes		

The master test sequence consists of six distinct sub-sequences (labeled LP-00, INIT, CONFIG, ESCAPE/ULPS, WAKEUP, and IMAGE DATA above). Note that the structure of this sequence, and the names of the various sub-blocks are specific to this test suite, and are not part of any MIPI specifications. Each sub-sequence is explained in further detail below.

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LP-00:

The ‘LP-00’ block is first component of the master sequence. In this sequence, the Test System sends a continuous LP-00 sequence of indefinite length (e.g., by looping/repeating a single LP-00 state.) The purpose of this state is to emulate the behavior of a Master D-PHY device before or during powerup, during which LP-00 will be sent on all Clock and Data Lanes until the Master has completed its own initialization. This is the default initial starting state of the Test System, and is what is transmitted to the DUT prior to DUT initialization (which occurs in the next block).

INIT:

The INIT sub-sequence is the second block of the master sequence. In this block, LP-11 is transmitted to the DUT on all Clock and Data Lanes for a duration determined by  $T_{INIT}$ . Note that the duration of  $T_{INIT}$  is protocol-specific, and should be specified in the DUT’s datasheet. The specified value should be no less than 100us (which is the minimum allowed  $T_{INIT}$  value defined by the D-PHY specification.)

CONFIG:

Many DSI devices require some amount of configuration before they will be ready to receive image data. This often consists of a series of one to several dozen (or more) short or long generic frames, which write device-specific configuration data to various areas of the device’s memory. This information is vendor-specific, and must be obtained from the DUT vendor. This information may be required to be sent as either validly formed HS frames (i.e., striped across all Data Lanes, with appropriate Clock Lane signaling), or they may be specifically required to be sent as LPDT frames (in which case they will be sent on Data Lane 0 only.)

This third block of the master sequence is intended for any of this device-specific configuration information, and may not be required at all by some devices (in which case it can be omitted). Also, CSI-2 receivers should not normally require this block, as control and configuration for CSI-2 devices is performed through the CCI interface.

ESCAPE/ULPS:

The fourth block of the master sequence consists of a ULPS entry sequence. This block works in conjunction with the following WAKEUP block, where each of the Lanes is put into, and taken out of the ULPS state prior to the following IMAGE DATA block. These blocks are used to test various requirements related to ULPS (e.g.,  $V_{IL}$  during ULPS, see Test 2.1.3), and for tests where ULPS is not the focus of the test, these blocks are still included in the master sequence, but have no practical impact on the overall behavior of the device, as the Lanes are simply briefly brought in and out of ULPS prior to the IMAGE DATA block.

The exact contents of the ESCAPE/ULPS block are slightly different for the Clock vs. Data Lanes, due to the fact that the Clock Lane will use the Clock Lane ULPS entry sequence (LP-11/10/00), and the Data Lanes will use the full Escape Mode Entry + ULPS Command sequence (see Test 2.2.5). Both cases will be followed by LP-00 for the remainder of the block.

WAKEUP:

Once the Lanes have been placed into the ULPS state by the ESCAPE/ULPS block, the purpose of the WAKEUP block is to bring the Clock and Data Lanes out of ULPS, which is accomplished by sending a Mark-1

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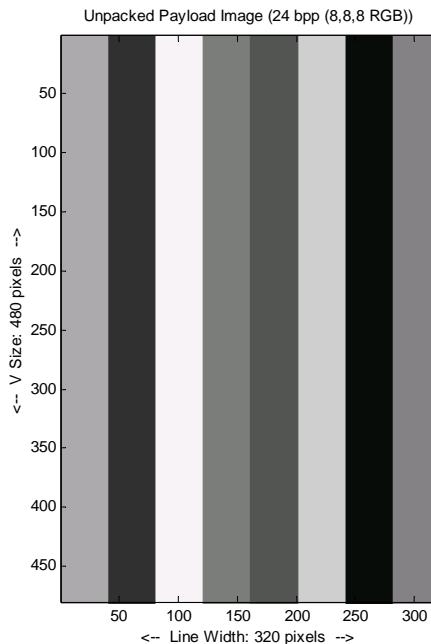
(LP-10) for the minimum TX T<sub>WAKEUP</sub> duration (1ms), followed by LP-11 for the remainder of the block. This sequence should be identical for the Clock and Data Lanes.

**IMAGE DATA:**

The final block of the master test sequence is the IMAGE DATA block. This block starts and ends with LP-11, and contains a validly constructed image data sequence. This sequence will be DUT-specific, and for DSI devices may be a Command Mode or Video Mode sequence, which in either case follows all of the relevant protocol and video timing characteristics that are required by the DUT. (Note that the exact requirements must be provided by the vendor). For CSI devices, the video timing requirements will not apply, but the sequence must be a validly formed image, of any supported image data format, and must contain at least one complete frame (i.e., 2-D image).

For both the CSI and DSI cases, the image data sequence should be designed such that the entire IMAGE DATA block will be transmitted repeatedly, in a continuous loop, in a manner that produces an observable image that is refreshed as frequently as possible.

For the specific contents of the image, it is recommended that the reference HS Test Pattern/Image be used (see Appendix D of this document). (Note that UNH-IOL has created a free utility, called PATGUI, which can be used to generate test patterns and images for various resolutions and formats, which use the reference HS test pattern. This utility may be freely obtained via the [MIPI Test Program Page](#) of the MIPI Alliance website.) An example image showing the reference HS Test Pattern for the RGB888 format is shown in the figure below.



**Figure C-1: Sample Reference Pattern Colorbar (320x640, 24bpp , 888RGB)**

The IMAGE DATA block should also contain appropriate Clock Lane signaling for the image data. If the DUT supports reception of burst-mode clock signaling (which is optional for both DSI and CSI-2 receivers), this mode should be used, as it will allow the most testing to be performed. (The supported clock modes must also be specified by the DUT vendor.)

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## **Appendix D – Reference HS Test Pattern for RX BER Verification and Interoperability Testing**

**Purpose:** To define a pseudo-worst-case HS test pattern for the purposes of performing receiver Bit Error Rate (BER) verification testing, as well as device-to-device system interoperability testing.

### **References:**

- [1] IEEE Std 802.3-2005, Section Four, Annex 48A.5, Continuous jitter test pattern (CJPAT)
- [2] UNH IOL Fast Ethernet Consortium, [Clause 25 Physical Medium Dependent \(PMD\) Test Suite](#), Test 25.2.3, Baseline Wander Correction.
- [3] Serial ATA International Organization, Serial ATA Revision 2.6 (15 Feb, 2007), Section 7.2.4.3.6, Composite Pattern (COMP).

**Last Modification:** January 13, 2009

### **Discussion:**

#### **D.1: Introduction:**

When performing BER verification testing (either between two devices during an interoperability test, or between a device and a test instrument during a receiver conformance test), the particular data pattern used can have an impact on the measured performance, primarily due to data-dependent signaling artifacts, which may be more pronounced with some data patterns than others. Many standards define reference test patterns designed to approximate ‘worst case’ conditions for stressing a receiver. In this appendix, a scalable-length reference test pattern is described, which can be used both for verifying proper receiver operation at a specified target BER (i.e., conformance testing), as well as verifying the physical link performance between two MIPI D-PHY products (interoperability testing).

#### **D.2: Background / Overview:**

The construction of a ‘worst case’, or ‘stressful’ data pattern for any given physical layer technology is partly technology-specific, and also depends on the transceiver architecture, and the particular characteristic one is seeking to isolate and stress. Depending on the technology and desired intent, patterns may specifically stress the receiver’s PLL and clock recovery circuitry (e.g., CJPAT[1]), or baseline wander/droop rejection[2]. Other patterns may be defined as composite sequences containing subsections of low-, mid-, and high-frequency patterns (see the COMP pattern used by Serial ATA[3]), which in addition to stressing the RX clock recovery circuitry, also exercises amplitude distortion (at the TX) and sensitivity (at the RX).

Pseudorandom binary sequence (PRBS) patterns may also be used for test purposes, however for most 8B/10B-based high-speed serial standards, these patterns are not appropriate, as they do not obey standard 8B/10B encoding rules and therefore can not be successfully interpreted by an 8B/10B-based receiver.

In general, the following considerations should be taken into account (or at least considered) when designing a reference test pattern:

- 1) It should isolate and stress specific physical layer characteristics.
- 2) It should be comprised of validly encoded data (if encoding is used).
- 3) It should be sufficiently long to yield statistically rich behavior (but not so long as to become impractical from an architecture or test equipment standpoint.)
- 4) It is desirable (though not mandatory) for the pattern to be able to be generated and observed “in system”, i.e., using normal device functionality, during normal device operation, and without requiring special test features or modes.

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**D.3: Considerations for D-PHY:**

For the case of D-PHY (and more specifically CSI/DSI-based devices), the concept of a worst-case test pattern is somewhat different from other high-speed serial standards, as some of the characteristics that apply to those other standards are not relevant to D-PHY due to its architecture. Specifically, the externally-clocked nature of D-PHY (and lack of line coding e.g., 8B/10B), means that there is no need to stress RX clock recovery functionality, as none exists. This simplifies the task in one sense, however it also raises the question as to exactly what physical layer characteristic(s) would be desirable to exercise via a stressing pattern.

One characteristic that is of particular significance in D-PHY-based systems is amplitude. Being a low-power system by nature, D-PHY transceivers are designed with low amplitudes in mind, both on the TX and RX sides of the link. Given the relatively small amplitudes used in D-PHY (and the decreased design margins that result), it is plausible to consider amplitude as being an especially meaningful parameter in D-PHY systems.

Furthermore, in addition to bare transceiver amplitude levels and sensitivity, another related factor with respect to amplitude is the frequency-dependent loss characteristics of the D-PHY interconnect.

Due to the nature of typical D-PHY-based camera and display systems, there are few practical restrictions on the frequency content of a typical CSI/DSI HS burst/frame (in terms of the transition density of the Data Lane signaling). It is possible (and not uncommon) to have valid CSI/DSI frames that contain very few transitions (i.e., consist of almost entirely all ones or all zeros). It is also possible within the scope of typical operation for frames to be generated that contain very high transition densities (e.g., 101010...), or even alternating sections of both high and low transition density data, often within a single burst.

Because of the frequency-dependent loss characteristics of the D-PHY interconnect, higher transition density (i.e., higher frequency) data patterns will have a tendency to be more attenuated by the interconnect than lower-transition-density patterns. This can result in a significant difference in signal amplitude observed at the receiver. It is important that a receiver be able to handle these ranges of amplitude, as well as the potentially abrupt instantaneous changes in amplitude that can vary with frequency content.

Because of this, one desirable quality for a reference D-PHY test pattern would be to stress this frequency-dependent amplitude characteristic of the link.

**D.4: Scalability:**

Another consideration that must be taken into account for a D-PHY test pattern is scalability. The CSI and DSI protocols are based on packet-based HS burst transmissions, where a burst will typically contain a single horizontal line of image data. Thus, the image data packet size is dependent on the image/display dimensions, and will vary from system to system. This precludes the use of a fixed-length pattern for testing purposes, as any reference pattern must be scalable if it is to be used during normal device operation (i.e., device-to-device interoperability).

**D.5: Scalable CSI/DSI Composite Pattern:**

Given the desire for a scalable pattern that contains varied transition density data content, one can begin to envision what a suitable reference pattern might look like.

Borrowing from the COMP (composite) pattern defined and used by the Serial ATA Standard [3], the following pattern is proposed as a reference stressing pattern for D-PHY. It is intended to be used as the image data payload of a CSI/DSI frame, and contains high-, mid-, and low-frequency subpatterns, as well as ‘lone bit’ sections (i.e., single bits preceded and followed by long sequences of the opposite bit value). It is designed to be scaled to any CSI/DSI line length, and can effectively be treated as image data, for various data formats. This allows the

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pattern to be implemented at the system level, as well as the bit level, and supports being detected at either the system level (via software, etc), or at the physical layer (via hardware, see Appendix E for one possible method using a Logic Analyzer, when testing “bare phy” implementations).

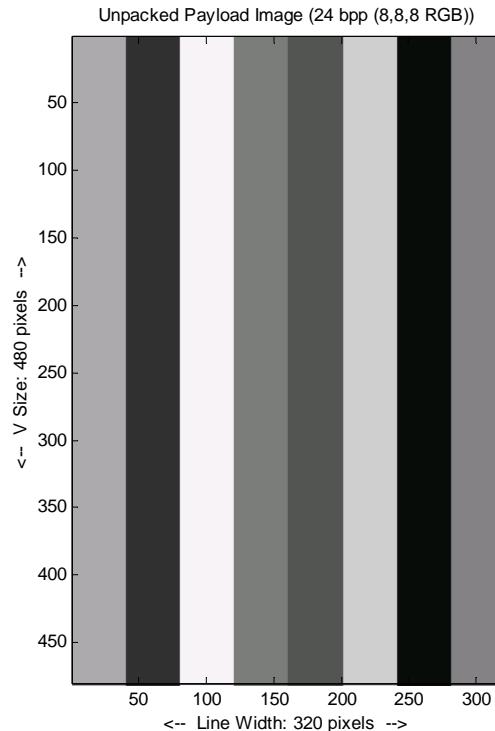
The general payload structure is as follows:

X bytes of 0xAA (high-frequency pattern, inverted)  
X bytes of 0x33 (mid-frequency pattern)  
X bytes of 0xF0 (low-frequency pattern, inverted)  
X bytes of 0x7F (lone 0 pattern)  
X bytes of 0x55 (high-frequency pattern)  
X bytes of 0xCC (mid-frequency pattern, inverted)  
X bytes of 0x0F (low-frequency pattern)  
Y bytes of 0x80 (lone 1 pattern)

Note that in this structure, the first seven sections are of equal length (X bytes), while the last section is allowed to be a different length (Y bytes). In most practical cases Y will be equal to X, however depending on the particular line length and datatype used when the payload is properly framed, there will be some cases where Y will need to be a different value than X in order to satisfy the formatting constraints required by certain datatypes. (Note this is discussed in further detail below.)

All bytes are transmitted onto the wire **LSB first**.

When unpacked and interpreted as 24-bit RGB pixel data (and duplicated vertically for a given number of lines), the above sequence translates to an eight-bar grayscale colorbar pattern. A sample 320x480 colorbar is shown below (where X = Y = 120 bytes per bar).



**Figure D-1: Sample Reference Pattern Colorbar (24bpp , 888RGB)**

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**D.6: Notes on Pattern Structure and Subpattern Ordering:**

The proposed pattern was the result of several iterations, incorporating feedback received from several CSI/DSI vendors, as well as experience gained from practical use. There are several design choices inherent to the above structure that are worth noting:

- 1) The choice of eight vertical bars (as opposed to some other number) was partly influenced by the fact that most common image/display resolutions have pixel widths that are evenly divisible by 8 (which is convenient from an implementation standpoint.) Also, eight bars conveniently supports the four primary subpatterns of interest (high-, mid-, low-frequency, and lone bit), as well as their respective inverses.
- 2) The selected ordering of the eight subpatterns was partly designed to highlight the visual contrast between adjacent bars, so that eight distinct bars would be visible (i.e., similarly-shaded bars are not placed next to each other, but rather are spatially separated with contrasting bars).
- 3) In addition to the visual contrast of adjacent bars, there is also a second motivation behind the selected ordering, which becomes apparent when the binary bit sequences are observed on the wire. Consider the following example pattern, where each bar is only three bytes wide ( $X=Y=3$ ). When each byte is transmitted LSB first, the resulting pattern appearing on the wire (read left-to-right, top to bottom) is:

010101010101010101010101	(0xAA)
110011001100110011001100	(0x33)
000011110000111100001111	(0xF0)
111111101111111011111110	(0x7F)
101010101010101010101010	(0x55)
001100110011001100110011	(0xCC)
111100001111000011110000	(0x0F)
000000010000000100000001	(0x80)

Note that in addition to the run-lengths of 1, 2, 4, and 7, which naturally result from the chosen subpattern values, the design choice of alternating polarities for each bar also produces additional run-length values of 3, 6, and 11, occurring at the boundaries between adjacent bars. These are highlighted in color, below:

010101010101010101010101	(0xAA)
110011001100110011001100	(0x33)
000011110000111100001111	(0xF0)
111111101111111011111110	(0x7F)
101010101010101010101010	(0x55)
001100110011001100110011	(0xCC)
111100001111000011110000	(0x0F)
000000010000000100000001	(0x80)

Thus, with this simple 8-bar structure and specific choice/ordering of subpatterns, a controlled sequence with a diverse range of run lengths can be produced.

**D.7: Datatype-Specific Payload Formatting:**

The method as defined thus far allows for the construction of a variable-length payload pattern, however additional requirements must be taken into account when the pattern is intended to be framed according to a particular CSI/DSI datatype.

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In the CSI and DSI specifications, each datatype definition includes requirements on the line lengths that are allowable for that given datatype. Each datatype introduces the concept of a data **word**, where a word is an n-bit data block that contains both an integer number of bytes, **and** an integer number of pixels. Each datatype requires that the line length (in pixels) contain an integer number of *words* (thus guaranteeing that each line will also then contain an integer number of bytes).

For example, the CSI-defined RAW7 datatype employs 7 bits per pixel. Because there must be an integer number of bytes in a line, the RAW7 specification groups the 7-bit pixels into blocks of 8 pixels, which results in a 56-bit (i.e., 7-byte) word. Thus, all allowable line lengths for the RAW7 datatype must be integer multiples of 8 pixels.

While there are several “non-byte-based” datatypes that impose these added restrictions on the number of pixels per line (e.g., RAW7, RAW12, RGB666), most of the datatypes are “byte based”, in that each pixel comprises an integer number of bytes, thus there is no need to group multiple pixels together to form integer-byte-length words, as each pixel already satisfies this requirement. In these cases (e.g., RGB888, RGB565, RAW8, etc) the “word” length is equal to the pixel length, and each line is allowed to be any number of pixels.

The reason all of this is relevant to test pattern generation is because this “word packing” aspect of some datatypes can introduce an additional level of complexity when trying to construct an 8-bar pattern, where each bar contains an equal number of bytes **and** pixels. There are cases for certain datatypes where a given line length in pixels may technically be valid for that datatype, but may not be evenly divisible into 8 equal-pixel-length colorbars, where each bar also contains an integer number of bytes. (One example case is RAW7 with a line length of 144 pixels. 144 pixels is an integer multiple of 8 pixels (as required for RAW7), however if we divide this into 8 equal-pixel-length bars, each bar will contain  $144/8 = 18$  pixels. However 18 pixels (times 7 bits/pixel) equals 126 bits/bar, which does not produce an integer number of **bytes per bar**. This introduces a problem for test pattern generation, because all of our subpatterns are all based on 8-bit data patterns, and we need each bar to contain an integer number of pixels **as well as bytes**, so we can construct our pattern based on bytes.

Fortunately, there is a solution to this problem that is relatively straightforward, and involves two parts: First, if we always work in terms of **words** (as opposed to pixels or bytes), we will guarantee that sequences containing integer numbers of words will also have integer numbers of pixels and bytes (as a word always contains integer pixels/bytes, by definition).

Second, we will adopt a rule whereby we will round the width of the first 7 bars down to the nearest word (in cases where the line length divided by 8 is not an integer number of words), then we will increase the width of the 8<sup>th</sup> bar to make up the difference. This results in a universal algorithm that can handle all possible cases for all datatypes.

Thus, the universal reference pattern generation algorithm consists of the following steps:

- 1) Select a desired datatype, and a valid line length for that datatype (in pixels).
- 2) Convert the number of pixels/line to words/line (by dividing by the number of pixels/word, as defined by the datatype specification.)
- 3) Divide the words/line result by 8. (This yields words/bar.)
- 4) If the result is an integer, then all bars will have equal length, and you can convert the words/bar value back to bytes/bar, and construct the 8-bar pattern accordingly.
- 5) If the result is not an integer, round the result down to the nearest integer number of words/bar. (This will be the width of bars 1-7). Increase the width of the 8<sup>th</sup> bar accordingly to make up the difference. Convert each bar width to bytes/bar, and assemble test pattern.

The resulting sequence then becomes:

N-**word** sequence of 0xAA (high-frequency pattern, inverted)  
N-**word** sequence of 0x33 (mid-frequency pattern)  
N-**word** sequence of 0xF0 (low-frequency pattern, inverted)  
N-**word** sequence of 0x7F (lone 0 pattern)

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- N-**word** sequence of 0x55 (high-frequency pattern)
- N-**word** sequence of 0xCC (mid-frequency pattern, inverted)
- N-**word** sequence of 0x0F (low-frequency pattern)
- M-**word** sequence of 0x80 (lone 1 pattern)

Where:

$$\begin{aligned}N &= \text{floor}(\text{wordsperline}/8) \\M &= \text{wordsperline} - (7*N)\end{aligned}$$

**D.8: Framing of the Payload Pattern:**

Note that for normal system operation, the properly constructed payload for a given datatype must then be properly framed. This involves the addition of an 8-bit sync pattern (sync byte), 4-byte CSI/DSI header, and 2-byte footer (containing the CRC).

The Sync pattern (as defined in the D-PHY spec) is always 0xB8. The exact 4-byte header pattern will depend on the exact datatype being used (see respective definitions in the CSI/DSI specifications), and the 2-byte footer will contain the correct CRC16 checksum for the specified payload data.

Note that for some testing applications (e.g., when testing a ‘bare phy’ implementation with no CSI/DSI protocol layer), the exact values of the header and footer are not critical to device operation, and dummy values may be used. (In this case, 0xFF’s are recommended for the header, and 0x00’s for the footer. Note that 0x00 is actually the proper footer value that should be used by transmitters that do not support checksum generation, per the DSI spec.)

Our fully framed pattern then becomes:

- 1 x 0xB8 (sync byte)
- 4 x 0xFF (dummy 32-bit frame header) (*or, actual frame header*)
- N-**word** sequence of 0xAA (high-frequency pattern, inverted)
- N-**word** sequence of 0x33 (mid-frequency pattern)
- N-**word** sequence of 0xF0 (low-frequency pattern, inverted)
- N-**word** sequence of 0x7F (lone 0 pattern)
- N-**word** sequence of 0x55 (high-frequency pattern)
- N-**word** sequence of 0xCC (mid-frequency pattern, inverted)
- N-**word** sequence of 0x0F (low-frequency pattern)
- M-**word** sequence of 0x80 (lone 1 pattern)
- 2 x 0x00 (dummy 16-bit frame footer) (*or actual CRC value*)

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**Appendix E – Logic Analyzer Trigger Setup for Frame Error Counting (Informative)**

**Purpose:** To define the basic trigger setup used for operating a Logic Analyzer as a Frame Error Counter for the purposes of RX Bit Error Rate (BER) testing of “bare phy” DUTs.

**References:**

None.

**Last Modification:** September 10, 2008

**Discussion:**

**E.1: Introduction:**

When performing RX BER testing on a device that has a parallel interface (e.g., bare D-PHY), it is possible to use a Logic Analyzer (LA) as a Frame Error Counter, to monitor for received bits that are incorrect. This is accomplished by implementing a state machine in using the trigger logic of the LA. The LA monitors the received bitstream via a parallel output on the device, and verifies the observed packet data against an expected test pattern. Using this method, packet and byte errors can be detected, which allows for verification of a target RX or System BER. (See Appendix F for a more complete discussion of the BER verification methodology.)

**E.2: Trigger Setup:**

The basic structure of the triggering state machine is shown below. (This example was taken from an Agilent 16702B, but the basic syntax may be translated to work with other analyzers.)

*(Note: The sequence below is based on the 6-bar RX test pattern defined in version v0.07 of the Test Suite, not the latest 8-bar pattern defined as of v0.08. However, the general concept below may be modified as needed to support any desired test pattern, limited only by the maximum number of states and variables allowed by the logic analyzer’s trigger.)*

(‘MIPI Free Run Trigger’)

```
1:  
If Counter 1 >= 16000000  
    occurs 1 time  
then Counter 2 Increment  
    Counter 1 Reset  
    Goto Next  
Else if Anything  
    then turn on default storing  
    Flag 4 Clear  
    Goto 2  
  
2:  
If lp-n = 1 Hex And  
    lp-p = 1 Hex  
    occurs 1 time  
then Timer 1 Resume  
    Goto 3  
Else if Anything  
then Goto 2  
  
3:  
If lp-n = 1 Hex And  
    lp-p = 1 Hex
```

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occurs 1 time  
then Goto 3  
Else if lp-n = 1 Hex And  
    lp-p = 0 Hex  
then Goto 4  
Else if Anything  
then Turn on default storing  
    Flag 2 Set  
    Goto 14

4:  
If lp-n = 1 Hex And  
    lp-p = 0 Hex  
    occurs 1 time  
then Goto 4  
Else if lp-n = 0 Hex And  
    lp-p = 0 Hex  
then Goto 5  
Else if Anything  
then turn on default storing  
    Flag 3 Set  
    Goto 14

5:  
If lp-n = 0 Hex And  
    lp-p = 0 Hex And  
    lane0 = 00 Hex  
    occurs 5 times consecutively  
then Goto Next  
Else if Anything  
then Goto 5

6:  
If lp-n = 0 Hex And  
    lp-p = 0 Hex And  
    lane0 = 00 Hex  
    lane0 = 1D Hex  
    occurs 1 time  
then Counter 1 Increment  
    Goto Next  
Else if lane0 = 00 Hex  
then Goto 6  
Else if Anything  
then turn on default storing  
    Flag 4 Set  
    Goto 14

7:  
If Anything  
    occurs 4 times consecutively  
then Goto Next

8:  
If lane0 = 55 Hex  
    occurs 56 times consecutively  
then Goto Next

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Else if lane0 != 55 Hex  
then Store sample  
    Goto 14

9:  
If lane0 = 33 Hex  
    occurs 60 times consecutively  
then Goto Next  
Else if lane0 != 33 Hex  
then Store sample  
    Goto 14

10:  
If lane0 = 0F Hex  
    occurs 60 times consecutively  
then Goto Next  
Else if lane0 != 0F Hex  
then Store sample  
    Goto 14

11:  
If lane0 = 08 Hex  
    occurs 60 times consecutively  
then Goto Next  
Else if lane0 != 08 Hex  
then Store sample  
    Goto 14

12:  
If lane0 = F7 Hex  
    occurs 240 times consecutively  
then Goto Next  
Else if lane0 != F7 Hex  
then Store sample  
    Goto 14

13:  
If lane0 = 55 Hex  
    occurs 130 times consecutively  
then Goto Next  
Else if lane0 != 55 Hex  
then Store sample  
    Goto 14

14:  
If Anything  
    occurs 1 time  
then Flag 1 Pulse set Pulse width 500ns  
    Store sample  
    Goto 1

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## **Appendix F – Statistical Methodology for Bit Error Rate (BER) Verification**

**Purpose:** To develop a procedure for Bit Error Rate (BER) measurement through the application of statistical methods.

**References:**

- [1] Miller, Irwin and John E. Freund, Probability and Statistics for Engineers (Second Edition), Prentice-Hall, 1977, pp. 194-210, 240-245.

**Last Modification:** October 17, 2008

**Discussion:**

### **F.1: Introduction:**

One key performance parameters for all digital communication systems is the bit error rate (BER). The bit error rate is the probability that a given bit will be received in error. The BER may also be interpreted as the average number of errors that would occur in a sequence of n bits.

While the bit error rate concept is quite simple, the measurement of this parameter poses some significant challenges. The first challenge is deciding the number of bits, n, that must be sent in order to make a reliable measurement. For example, if 10 bits were sent and no errors were observed, it would be foolish to conclude that the bit error rate is zero. However, common sense tells us that the more bits that are sent without error, the more reasonable this conclusion becomes. In the interest of keeping the test duration as short as possible, we want to send the smallest number of bits that provides us with an acceptable margin of error.

This brings us to the second challenge of BER measurement. Given that we send n bits, what reasonable statements can be made about the bit error rate based on the number of errors observed? Returning to the previous example, if 10 bits are sent and no errors are observed, it is unreasonable to say that the BER is zero. However, it may be more reasonable to say that the BER is  $10^{-1}$  or better. Furthermore, you are absolutely certain that the bit error rate is not 1.

In this appendix, two statistical methods, hypothesis testing and confidence intervals, are applied to help us answer the questions of how many bits we should be sent and what conclusions can be made from the test results.

### **F.2 – Statistical Model**

A statistical model for the number of errors that will be observed in a sequence of n bits must be developed before we apply the aforementioned statistical methods. For this model, we will assume that every bit received is an independent Bernoulli trial. A Bernoulli trial is a test for which there are only two possible outcomes (i.e. a coin toss). Let us say that p is the probability that a bit error will occur. This implies that the probability that a bit error will not occur is (1-p).

The property of independence implies that the outcome of one Bernoulli trial has no effect on the outcomes of the other Bernoulli trials. While this assumption is not necessarily true for all digital communications systems, it is still used to simplify the analysis.

The number of successful outcomes, k, in n independent Bernoulli trials is taken from a binomial distribution. The binomial distribution is defined in equation F-1.

$$b(k; n, p) = C_{n,k} p^k (1 - p)^{n-k} \quad (\text{Equation F-1})$$

Note that in this case, a successful outcome is a bit error. The coefficient  $C_{n,x}$  is referred to as the binomial coefficient or “n-choose-k”. It is the number of combinations of k successes in n trials. Returning to coin toss

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analogy, there are 3 ways to get 2 heads from 3 coin tosses: (tails, heads, heads), (heads, tails, heads), and (heads, heads, tails). Therefore,  $C_{3,2}$  would be 3. A more precise mathematical definition is given in equation F-2.

$$C_{n,k} = \frac{n!}{k!(n-k)!} \quad (\text{Equation F-2})$$

This model reflects the fact that for a given probability,  $p$ , a test in which  $n$  bits are sent could yield many possible outcomes. However, some outcomes are more likely than others and this likelihood principle allows us to make conclusions about the BER for a given test result.

### **F.3 – Hypothesis Test**

The statistical method of hypothesis testing will allow us to establish a value of  $n$ , the number of bits to be sent, for the BER measurement. Naturally, the test begins with a hypothesis. In this case, we will hypothesize that the probability of a bit error,  $p$ , for the system is less than some target BER,  $P_0$ . This hypothesis is stated formally in equation F-3.

$$H_0 : p \leq P_0 \quad (\text{Equation F-3})$$

We now construct a test for this hypothesis. In this case, we will take the obvious approach of sending  $n$  bits and counting the number errors,  $k$ . We will interpret the test results as shown in table F-1.

Table F-1: Acceptance and rejections regions for  $H_0$

Test Result	Conclusion
$k = 0$	$H_0$ is true
$k > 0$	$H_0$ is false

We now acknowledge the possibility that our conclusion is in error. Statisticians define two different categories of error. A type I error is made when the hypothesis is rejected even though it is true. A type II error is made when the hypothesis is accepted even though it is false. The probability of a type I and a type II error are denoted as  $\alpha$  and  $\beta$  respectively. Table F-2 defines type I and type II errors in the context of this test.

Table F-2: Definitions of type I and type II errors

Type I Error	$k > 0$ even though $p \leq \text{BER}$
Type II Error	$k = 0$ even though $p > \text{BER}$

A type II error is arguably more serious and we will define  $n$  so that the probability of a type II error,  $\beta$ , is acceptable. The probability of a type II error is given in equation F-4.

$$\beta = (1 - p)^n < (1 - P_0)^n \quad (\text{Equation F-4})$$

Equation F-4 illustrates that the upper bound on the probability of a type II error is a function of the target bit error rate and  $n$ . By solving this equation for  $n$ , we can determine the minimum number of bits that need to be sent in order to verify that  $p$  is less than a given  $P_0$  for a given probability of type II error.

$$n > \frac{\ln(\beta)}{\ln(1 - P_0)} \quad (\text{Equation F-5})$$

Let us now examine the probability of a type I error. The definition of  $\alpha$  is given in equation F-6.

$$\alpha = 1 - (1 - p)^n \leq 1 - (1 - P_0)^n \quad (\text{Equation F-6})$$

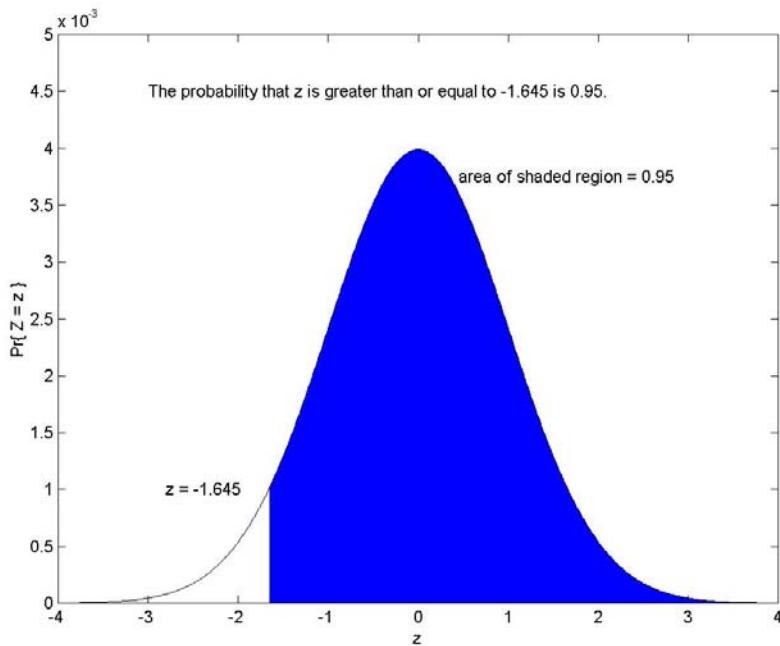
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Equation F-6 shows that while we increase  $n$  to make  $\beta$  small, we simultaneously raise the upper bound on  $\alpha$ . This makes sense since the likelihood of observing a bit error increases with the number of bits that you send, no matter how small bit error rate is. Therefore, while the hypothesis test is very useful in determining a reasonable value for  $n$ , we must be very careful in interpreting the results. Specifically, if we send  $n$  bits and observe no errors, we are confident that  $p$  is less than our target bit error rate (our level of confidence depends on how small we made  $\beta$ ). However, if we do observe bit errors, we cannot be quick to assume that the system did not meet the BER target since the probability of a type I error is so large. In the case of  $k > 0$ , a confidence interval can be used to help us interpret  $k$ .

#### F.4 – Confidence Interval

The statistical method of confidence intervals will be used to establish a lower bound on the bit error rate given that  $k > 0$ . A confidence interval is a range of values that is likely to contain the actual value of some parameter of interest. The interval is derived from the measured value of the parameter, referred to as the point estimate, and the confidence level,  $(1-\alpha)$ , the probability that the parameter's actual value lies within the interval.

A confidence interval requires a statistical model of the parameter to be bounded. In this case, we use the statistical model for  $k$  given in equation F-1. If we were to compute the area under the binomial curve for some interval, we would be computing the probability that  $k$  lies within that interval. This concept is shown in figure F-1.



**Figure F-1: Computing the probability that  $z \geq -1.645$  (standard normal distribution).**

To compute the area under the binomial curve, we need a value for the parameter  $p$ . To compute a confidence interval for  $k$ , you assume that  $k/n$ , the point estimate for  $p$ , is the actual value of  $p$ .

Note that figure F-1 illustrates the computation of the lower tolerance bound for  $k$ , a special case where the confidence interval is  $[k_l, +\infty]$ . A lower tolerance bound implies that in a percentage of future tests, the value of  $k$  will be greater than  $k_l$ . In other words, actual value of  $k$  is greater than  $k_l$  with probability equal to the confidence level. Therefore, if  $k_l/n$  is greater than  $P_0$ , we can say that the system does not meet the target bit error rate with probability  $(1-\alpha)$ . By reducing  $\alpha$ , we reduce the probability of making a type I error.

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To determine the value of  $k_l$ , it is useful to assume that the binomial distribution can be approximated by a normal (Gaussian) distribution when  $n$  is large. The mean and variance of this equivalent distribution are the mean and variance of the corresponding binomial distribution (given in equations F-7 and F-8).

$$\mu_K = np \quad (\text{Equation F-7})$$

$$\sigma_K^2 = np(1 - p) \quad (\text{Equation F-8})$$

Now, let  $\alpha$  be the probability that  $Z \leq z_\alpha$  where  $Z$  is a standard normal random variable. A standard random variable is one whose mean is zero and whose variance is one. The random variable  $K$  can be standardized as shown in equation F-9.

$$Z = \frac{K - \mu_K}{\sigma_K} \quad (\text{Equation F-9})$$

Note that  $Z$  is greater than  $z_\alpha$  with probability  $(1-\alpha)$ , the confidence level. We apply this inequality to equation F-9 and solve for  $K$  to get equation F-10.

$$K > \mu_K + z_\alpha \sigma_K \quad (\text{Equation F-10})$$

$$K > np + z_\alpha \sqrt{np(1 - p)}$$

As mentioned before, we assume that  $p$  is  $k/n$ . We can now generate an expression for  $k_l$ , the value that  $K$  will exceed with probability  $(1-\alpha)$ . This expression is given in equation F-11.

$$k_l = k + z_\alpha n \sqrt{\frac{(k/n)(1-k/n)}{n}} \quad (\text{Equation F-11})$$

Finally, we argue that if  $K$  exceeds  $k_l$ , then the actual value of  $p$  must exceed  $k_l/n$ . Therefore, we can generate an expression for  $p_l$ , the value that  $p$  will exceed with probability  $(1-\alpha)$ , and compare it to the target bit error rate. By applying this comparison (given in equation F-12) the probability of a type I error can be greatly reduced. For example, by setting  $z_\alpha$  to  $-1.645$ , the probability of a type I error is reduced to 5%.

$$P_0 \geq p_l = \frac{k_l}{n} = \frac{k}{n} + z_\alpha \sqrt{\frac{(k/n)(1-k/n)}{n}} \quad (\text{Equation F-12})$$

## **F.5 – Sample Test Construction**

We now compress the theory presented in sections F-2 through F-4 into two inequalities that may be used to construct a bit error rate test. First, we take equation F-5 and assume that  $\ln(1-P_0)$  is  $-P_0$  (valid for  $P_0$  much less than one). The results is equation F-13.

$$n > \frac{-\ln(\beta)}{P_0} \quad (\text{Equation F-13})$$

Second, we examine equation F-12. Assuming that  $(1-k/n)$  is very close to 1 and substituting  $-\ln(\beta)/P_0$  for  $n$ , we get equation F-14.

$$-\ln(\beta) \geq k + z_\alpha \sqrt{k} \quad (\text{Equation F-14})$$

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The largest value of  $k$  that satisfies equation F-14 is  $k_l$ . The benefit of these two equations is that a bit error rate test is uniquely defined by  $\beta$  and  $\alpha$  and that the test scales with  $P_0$ . Table F-3 defines  $n$  and  $k_l$  in terms of  $\beta$  and  $\alpha$ .

Table F-3:  $n$  and  $k_l$  as a function of  $\beta$  and  $\alpha$ .

$\beta$	$-\ln(\beta)$	$n$	$\alpha$	$z_\alpha$	$k_l$
0.10	2.30	$2.30/P_0$	0.10	-1.29	5
0.10	2.30	$2.30/P_0$	0.05	-1.65	6
0.05	3.00	$3.00/P_0$	0.05	-1.65	7
0.05	3.00	$3.00/P_0$	0.01	-2.33	10
0.01	4.60	$4.60/P_0$	0.05	-1.65	9
0.01	4.60	$4.60/P_0$	0.01	-2.33	13

As an example, let us construct a test to determine if a given system is operating at a bit error rate of  $10^{-12}$  or better. Given that a 5% chance of a type I error is acceptable, the test would take the form of sending  $3 \times 10^{12}$  bits and counting the number of errors. If no errors are counted, we are confident that the BER was  $10^{-12}$  or better.

Given that a 5% chance of a type II error is acceptable, we find that  $k_l$  is 7. If more than 7 errors are counted, we are confident that the bit error rate is greater than  $10^{-12}$ . However, what if between 1 and 7 errors are counted? These cases may be handled several different ways. One option is to make a statement about the bit error rate (whether it is less than or greater than  $10^{-12}$ ) at a lower level of confidence. Another option would be to state that the test result is success since we cannot establish with an acceptable probability of error that the BER is greater than  $10^{-12}$ . Such a statement implies that we failed to meet the burden of proof for the conjecture that the BER exceed  $10^{-12}$ . Of course, the burden of proof could be shifted to the device under test which would imply that any outcome other than  $k = 0$  would correspond to failure (the device under test failed to prove to us that the BER no more than  $10^{-12}$ ). If neither of these solutions is acceptable, it is always an option to perform a more vigorous bit error rate test in order to clarify the result.

## **F.6 – Packet Error Rate Measurement**

It is often easier to measure packet errors than it is to measure bit errors. In these cases, it is helpful to have some linkage between the packet error rate and the bit error rate. To make this linkage, we assume that the bit error rate is low enough and the packet size is small enough so that each packet error contains exactly one bit error.

To complete the linkage, some care must be taken regarding how many packets to send. A bit error is only detectable in the region of the packet that is covered by the cyclic redundancy check (CRC). In the context of MIPI CSI/DSI, this applies to the payload portions of all Long Packet types. There is no guarantee that errors in the frame headers (for either Short or Long packets), and inter-packet gap will be detected. Therefore, we must translate  $n$  from the number of bits are sent to the number of “observable” bits that are sent. This will increase the test duration since a portion of the time will be spent sending unobservable bits.

For packets of length  $x$  bits, at least  $n/x$  packets must be sent to perform the equivalent bit error rate test. If no packet errors are observed, the conclusion is that the bit error rate is less than  $P_0$ . If more than  $k_l$  packet errors are observed, the conclusion is that the bit error rate is greater than  $P_0$ .

Note that  $x$  is the length of the packet after encoding (if line coding is used, which is optional for D-PHY). In other words, in an 8B/9B encoding environment, a 64-byte packet is 576 bits in length after encoding. Also note that to reinforce the assumption that there is only one bit error per packet error, a test should be run with the shortest possible packets. However, if extremely low bit error rates are to be verified, it may be favorable to use long packets to increase the percentage of observable bits and reduce the test duration.

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## Appendix G – RX Test Observables for DUT Device Types

**Purpose:** To discuss various options for DUT observable behavior for performing LP/HS-RX testing, for different types and classes of D-PHY-based DUTs.

### References:

- [1] D-PHY Specification, Section 4.5, Line 561
- [2] DSI Specification (v1.01.00), Section 5.3, Line 571

**Last Modification:** October 17, 2008

### Discussion:

#### G.1: Introduction:

For performing the RX tolerance tests of Section 2, almost all test procedures involve variations of the same basic theme:

- Generate and transmit a controlled test stimulus sequence that is specifically designed to isolate the parameter of interest.
- Verify successful (or unsuccessful) reception of the test stimulus by the DUT.

Note that depending on the test, the stimulus may be a “pure” LP sequence (e.g., Escape Mode Command), or an HS Burst sequence (which inherently contains LP signaling, as the LP-11 Stop state and HS Entry process are valid and defined LP sequences.)

Because there is no built-in test mode functionality used for D-PHY receiver testing, RX tests must utilize some aspect of basic device operation as an observable mechanism in order to determine whether or not a particular test stimulus was successfully received. The difficulty of this however, is that there is no single common observable that is guaranteed to be supported by all MIPI product classes (e.g., CSI, DSI, UniPro, etc). In addition, because this test suite supports testing of different D-PHY DUT types (e.g., bare phy, phy + protocol test IC’s, finished products, hosts, peripherals, etc), identification of a suitable observable may depend heavily on the DUT type and implementation. In this Appendix, options for several different device types and classes will be discussed. While this Appendix is not intended as an exhaustive list, it does describe a set of options that should cover a majority of cases.

#### G.2: Bare D-PHY:

In the case of a “bare phy” (meaning a test IC which does not include a protocol layer, and includes some type of parallel PPI-like interface), the most common approach is to probe the HS and LP signals of the parallel interface to verify that the stimulus sent into the D-PHY LP/HS interface is accurately received.

Typically, two slightly different configurations are used for performing LP vs. HS tests. Because of the simpler nature of the LP output of the parallel interface, a DSO may be used to monitor the interface’s LP output, while a repeated LP stimulus is presented at the D-PHY interface. Differential probes may be connected at the D-PHY and parallel interfaces, and the logical output observed at the parallel interface can be directly verified against the LP stimulus presented at the D-PHY input, by overlaying the two traces on a DSO screen. Typically the input parameter can be varied to find the threshold point at which the parallel interface output no longer matches the D-PHY input. (Note it is also not uncommon for there to be an ‘intermittent’ region, prior to total failure, where behavior may show sporadic errors, but not totally failing. It may be of informative use to note these cases, however in most test procedures, the last point at which ‘consistent’ valid behavior was observed is take to be the measured threshold point.)

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For HS tests, it is not practical to verify the parallel data by observation using a DSO. In this case however, a Logic Analyzer can be used to verify the parallel output stream against a known D-PHY HS input.

The specific HS data pattern used as the test stimulus should be chosen to isolate the parameter under test. For the purposes of most HS-RX tests (e.g., common mode/differential amplitude tests, etc), it is advisable to use a test pattern that lends itself to accurate amplitude measurements (e.g., a repeating 1010, 11001100, or 11110000 pattern, etc.) versus a ‘stressful’ worst-case pattern such as the BER test pattern defined in Appendix D. While the worst-case pattern might seem like a better choice, it actually complicates the test methodology, as it can be more difficult to measure (and thus calibrate an accurate amplitude level for the RX Test System signal source). Also, it contains frequency-dependent subsections, which may behave differently as they are affected by the frequency-dependent losses occurring between the point where the signals are injected into the DUT (e.g., SMA connectors on the test PCB), and the point corresponding to the D-PHY IC pins. The added factors of decreased calibration accuracy and unknown/uncontrollable frequency-dependent effects can decrease overall test repeatability and accuracy.

For all HS-RX tests (except the informative RX jitter test), a repeating 11001100 data pattern will be used for the HS burst payload data. (Note an explicit HS burst length is not specified here, however it is recommended that the test pattern be roughly as long as a typical Long Packet, i.e., several thousand bits.)

### **G.3: DSI Display Device (D-PHY + DSI Protocol + Display Driver + Glass, Integrated):**

In the case of a finished DSI display product, all of the components are typically integrated into a single package, and no access to any parallel interface is available. In this case, there are multiple potential observable mechanisms:

- The displayed image (i.e., visual inspection of HS pixel data)
- For DCS (i.e., Command Mode) displays, observation of panel behavior in response to LP- or HS-issued DCS commands (e.g., toggling display backlight, power, color mode, invert mode, etc.)
- For non-DCS (Video Mode) displays, observation of panel behavior in response to LP- or HS-issued DSI commands (e.g., *Color Mode On/Off*, *Turn On Peripheral/Shutdown Peripheral*, etc.)
- For Command Mode displays (and optionally Video Mode displays that support bi-directional communication), acknowledgement of a variety of defined error types can be observed via presence of an *Acknowledge and Error Report* packet from the display, which can be triggered by initiating a Bus Turn-Around (BTA) event from the host. If any of the defined error types have been detected by the display, an *Acknowledge and Error Report* packet will be sent by the display following a BTA.
- Access to vendor-specific internal registers and status indicators through the D-PHY interface (if the display supports bi-directional communication), which may be queried in order to determine the result of a previous stimulus.

#### **Command Mode Displays:**

For LP tests, if the DUT supports the DCS command set, the easiest stimulus/observable vehicle is to transmit the DCS **set\_display\_on** and **set\_display\_off** commands to the DUT using LP signaling. This involves transmitting the following sequence:

Escape Mode Entry Sequence + Escape Mode LPDT Command + LPDT-encoded DCS Command Packet

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Using this sequence as a test vehicle, all of the LP electrical parameters can be varied, and the on/off behavior of the display can be used as the observable to determine whether or not the stimulus was received correctly. Note however that because LP commands are only transmitted on Data Lane 0 for DSI devices, this technique only allows for exercising the full set of D-PHY LP-RX characteristics for Data Lane 0 of a DSI display device.

For HS-RX testing of Command Mode displays, it is possible to leverage the fact that Command Mode displays will always support reverse direction capability. Thus, any series of HS packets can be followed by a Bus Turn-Around (BTA) assertion, after which a display will respond is required to respond with an *Acknowledge and Error Report* packet, if any of the defined error types were observed since the last peripheral-to-host transaction. While many of the error types can be used as observables for various tests, the *Checksum Error* type (bit 10) is of primary interest, as it provides observability across an arbitrarily long series of HS bits/packets sent to the DUT. If a checksum error was detected for any HS packet since the last peripheral-to-host transaction, it will be identified by the peripheral via the transmission of an *Acknowledge and Error Report* packet. This mechanism allows system and component Bit Error Rate verification tests to be performed. (See Test 2.3.8, and Appendix F of this document for more about BER tests.)

Also, another option that can be used for nearly all of the HS-RX tests (particularly any measurement that requires finding the failure point of the DUT, e.g., amplitude or timing thresholds) would be to use the same methodology described above for the LP tests (e.g., DCS `set_display_on` and `set_display_off` commands to the DUT), but send them using HS signaling. The success or failure of reception can readily and easily be determined by visual inspection of the DUT's behavior.

### Video Mode Displays:

To perform LP-RX tests on Video-Mode-only displays, a modified version of the Command Mode methodology above can be used. While Video Mode displays are not *required* to support all of the defined DSI commands, it is likely that most Video-Mode-only displays will support the *Shutdown Peripheral* and *Turn On Peripheral* commands. These commands are similar in nature to the DCS `set_display_on` and `set_display_off` counterparts, and can be used in the same fashion as a vehicle for performing LP-RX tests on displays that only support Video Mode. (Though again, the same issue applies to Video Mode displays, in that these commands are only received on Data Lane 0, leaving the same remaining question of how to test LP-RX functionality on Data Lanes 1-3, as well as the Clock Lane.)

In the event that a Video-Mode-only display does not support the *Shutdown Peripheral* and *Turn On Peripheral* commands, an alternative supported command will have to be determined (preferably a simple non-image-data command, which produces a visible behavior on the panel), however the general methodology will otherwise be the same.

HS-RX testing of Video-Mode-only displays can be performed using the same method described in the previous paragraph for LP-RX, but by sending the commands using HS signaling. (Again, this applies primarily to amplitude and timing threshold measurements.)

For BER-style HS-RX tests, the same methodology described above for Command Mode displays can be used, but only if the Video Mode display supports bi-directional communication (which is possible and allowed by the specification, however not likely to be the case for most typical Video Mode displays).

Unfortunately, for Video-Mode-only displays that only support unidirectional communication, the only real observable for performing a BER-type test is the display glass itself. In this case, visual inspection of the displayed image for distortion or other artifacts can be used, however depending on the test time (and the reliability of the human observer), this is more of a qualitative observable, rather than a quantitative one.

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**G.4: Lane-Dependent Limitations of LP Test Patterns:**

For most LP-RX tests, it would be desirable to use a test sequence that contained only LP-based signaling (e.g., Escape Mode commands, or DSI/DCS packets sent via LPDT). However, one limitation of this approach is that for CSI and DSI implementations (i.e., non-bare-phy DUT types), LPDT communication is restricted to Data Lane 0 only. This means LPDT test sequences cannot be used on Data Lanes 1,2, and 3. Also, they cannot be used for the Clock Lane.

Furthermore, Escape Mode behavior is also restricted for the different Lanes. The D-PHY spec states that “*All Lanes shall include Escape mode support for ULPS and Triggers in the Forward direction.*”[1], however the DSI spec states that, “*All Trigger messages shall be communicated across Data Lane 0.*”[2]. This means that for many DUT cases, the available options for LP test patterns for use on Data Lanes 1, 2, and 3 will be severely restricted.

One pattern that may offer some opportunity is the ULPS Escape Mode command, as all Data Lanes are still required to support this command, as Lanes must still be put into ULPS individually via this command. Technically this should offer attractive potential as a test mechanism, however the difficulty comes in terms of observability, as there is no easy way to visually determine if a Lane has entered the ULPS state by visual inspection. Lanes should technically not accept any LP/HS traffic while in ULPS, until they have been brought out of ULPS via a proper ULPS exit sequence. This fact could be used as a test mechanism, (e.g., send test ULPS sequence, then verify acceptance of some other valid command to see if ULPS command was successful).

One other option exists for exercising different Lanes of a DUT, which is referred to as Lane Remapping, and is described below.

**G.5: Lane Remapping:**

For some DUT types, one additional option exists, which can be leveraged to allow testing of various HS- and LP-RX parameters for different Lanes of a multi-Lane DUT. It is somewhat of a trick, and is called Lane Remapping.

Many DUTs, particularly Hosts, support the capability to reprogram their Lane configuration, such that the number and ordering of the Data Lanes can be arbitrarily assigned, in addition to the position of the Clock Lane also being programmable. In this case, any of the DUT ports can be configured to serve as Data Lane 0, thus allowing the full set of LPDT test patterns to be used to test the LP-RX characteristics of that DUT port. Granted, the Lane will always be tested as a Data Lane 0, however from the perspective of validating D-PHY LP- and HS-RX physical layer characteristics, this should be irrelevant, as it is the specific silicon circuitry of each of the DUT ports that is being tested.

While this methodology can typically be applied to Host DUTs, it unfortunately cannot be applied to most peripherals, as they typically do not support custom remapping of the D-PHY lanes.

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## Appendix H – Standardized Software Interface for Test Automation

**Purpose:** To define a common software interface that allows DUTs to provide access to error and fault information for the purposes of test automation, particularly RX tolerance testing.

**References:** None.

**Last Modification:** November 30, 2009

**Discussion:**

### H.1: Introduction:

For some DUT types, proprietary tools exist, which allow access to checksum error counters, burst counters or other indicators that indicate if a receiver is able to receive data properly. To allow integration of such proprietary tools in an automated test environment the following interface can be implemented which acts as wrapper for such tools (definition given in C#.Net).

### H.2: Software Interface Definition:

```
using System;
using System.Collections.Generic;
using System.Text;

namespace Mipi
{
    public enum MipiChannelE
    {
        Clock = 0,
        Data0 = 1,
        Data1 = 2,
        Data2 = 3,
        Data3 = 4,
        _NA = 100,
    }
    public enum MipiModeE
    {
        HS=0,
        LP=1,
        ULP=2,
    }
    public interface IMipiBerReader
    {
        /// <summary>
        /// This method will be called once to connect your BER reader.
        /// </summary>
        /// <param name="address">The address string can be used by your implementation
        /// to configure the connection to the MipiBerReader interface</param>
        void Connect(string address);

        /// <summary>
        /// This method will be called once the connection should be closed
        /// </summary>
        void Disconnect();

        /// <summary>
        /// This method will be called prior the individual tests to tell the device
        /// what channel and what mode is tested. This can be used to load appropriate
        /// setups.
        /// </summary>
        /// <param name="channel">number of data lane or clock lane (see MipiChannelE
        /// enum)</param>
        /// <param name="mode">High speed, low power or ultra low power (see MipiModeE
        /// enum)</param>
    }
}
```

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```
/// <param>
void Init(MipiChannelE channel, MipiModeE mode);

/// <summary>
/// Will be called at the beginning of the BER measurement and allows to
/// implement a reset for a DUT.
/// </summary>
void ResetDut();

/// <summary>
/// Start the counters. This method MUST reset the counters!
/// </summary>
void Start();

/// <summary>
/// Stop the DUT to read out the counters (see
/// GetReadCounterWithoutStopSupported()).
/// </summary>
void Stop();

/// <summary>
/// This method should return counters, one counting the bits/frames/lines
/// or bursts and one counting the errors detected by the MipiBerReader.
/// The automation software will compute the BER using the following
/// equiation BER=errorCounter/bitCounter. If bitCounter stays at 0 even
/// if the stimmulus is sending data then this will also interpreted as fail.
/// </summary>
/// <param name="bitCounter">Contains the number of bits which are received
/// by the DUT. If it is not possible to count bits the value can also contain
/// frames, or bursts. It is just a matter of the value defined as target BER.
/// If it is not possible to get the number of bits/frames/bursts then the
/// method can return a value of -1 and the automation software can compute
/// the number of bits by the data rate and the time of running.</param>
/// <param name="errorCounter">Total number of errors since the last start.
/// </param>
void GetCounter(out int bitCounter, out int errorCounter);

/// <summary>
/// This method should return a boolean value depending if the device supports
/// reading the counters while it is running or not. In case of this method
/// returns a false then the device needs to be stopped for reading the counters.
/// In this case the automation software will stop data transmission
/// before calling the GetCounter() function, and starting the system after
/// that again.
/// </summary>
/// <returns>false if device needs to be stopped before reading the counters,
/// and true if the counters can be read on the fly.</returns>
bool GetReadCounterWithoutStopSupported();
}
```

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**Appendix I – Vendor DUT Pre-Test Checklist**

**Purpose:** To provide a list of required information a vendor must specify when submitting a DUT for D-PHY physical layer conformance testing.

**References:**

- [1] D-PHY Specification (see references below)
- [2] DSI Specification (see references below)

**Last Modification:** September 16, 2010

**Discussion:**

**I.1: Introduction:**

The following is a non-exhaustive list of information vendors should provide (either directly, or via the DUT's datasheet) when submitting a DUT to a test lab for D-PHY physical layer conformance testing. (Note that references are provided for cases where the information is explicitly required by the specification to be provided by the vendor):

**General Requirements:**

- Specify whether or not the DUT supports bi-directional communication.
- Indicate whether continuous and non-continuous (i.e., burst mode) HS clocking modes are supported for transmission. (Also, if both modes are supported, indicate the mechanism used to configure the mode.)
- (D-PHY v1.00, Sec. 7.3): Indicate  $UI_{INST}$  and  $UI_{INST,MIN}$  (Nominal and max supported data rates.) (“*Implementers shall specify a value  $UI_{INST,MIN}$  that represents the minimum instantaneous UI possible within a high speed data transfer for a given implementation.*”)

**DSI-Specific Requirements:**

- (DSI v01.01.00, Sec. 8.9.5): Specify the peripheral's vendor-specific register values for reading additional protocol violation error information. (“*Peripheral vendors shall specify an implementation-specific error status register where a Host can obtain additional information regarding what type of protocol violation occurred by issuing a read request.*”)
- (DSI v01.01.00, Sec. 5.6.1): Specify the peripheral's nominal LP clock frequency and the guaranteed accuracy. (“*The host processor LP clock frequency shall be in the range of 67% to 150% of peripheral LP clock frequency. Therefore, the peripheral implementer shall specify a peripheral's nominal LP clock frequency and the guaranteed accuracy.*”)
- (DSI v01.01.00, Sec. 5.7): Specify the peripheral's minimum required  $T_{INIT}$ . (“*If the peripheral requires a longer period after power-up than the  $T_{INIT}$  period driven by the host processor, this requirement shall be declared in peripheral product information or data sheets.*”)
- (DSI v01.01.00, Sec. 10.9): Indicate whether EoTp is supported. If so, indicate the mechanism used to enable/disable EoTp support. (“*In order to ensure interoperability with earlier devices, current devices shall provide a means to enable or disable EoTp generation or detection.*”)
- (DSI v01.01.00, Sec. 8.9.2): Indicate whether or not the DUT implements checksum (CRC). (“*A peripheral shall implement ECC, and may optionally implement checksum.*”)