



Conformance Test Suite for C-PHYSM v1.0

**CTS Version 1.0
12 February 2016**

MIPI Board Approved 12 February 2016

This is an informative document, not a MIPI Specification.
Various rights and obligations that apply solely to MIPI Specifications (as defined in the MIPI Membership Agreement and MIPI Bylaws) including, but not limited to, patent license rights and obligations, do not apply to this document.

This document is subject to further editorial and technical development.

To check for the latest version, always refer to the MIPI Alliance Specifications Page:
<https://members.mipi.org/wg/All-Members/home/approved-specs>

NOTICE OF DISCLAIMER

The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled by any of the authors or developers of this material or MIPI®. The material contained herein is provided on an “AS IS” basis and to the maximum extent permitted by applicable law, this material is provided AS IS AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of negligence.

All materials contained herein are protected by copyright laws, and may not be reproduced, republished, distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related trademarks, tradenames, and other intellectual property are the exclusive property of MIPI Alliance and cannot be used without its express prior written permission.

ALSO, THERE IS NO WARRANTY OF CONDITION OF TITLE, QUIET ENJOYMENT, QUIET POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD TO THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT. IN NO EVENT WILL ANY AUTHOR OR DEVELOPER OF THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT OR MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL, CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR ANY OTHER AGREEMENT, SPECIFICATION OR DOCUMENT RELATING TO THIS MATERIAL, WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Without limiting the generality of this Disclaimer stated above, the user of the contents of this Document is further notified that MIPI: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the contents of this Document; (b) does not monitor or enforce compliance with the contents of this Document; and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance with the contents of this Document. The use or implementation of the contents of this Document may involve or require the use of intellectual property rights (“IPR”) including (but not limited to) patents, patent applications, or copyrights owned by one or more parties, whether or not Members of MIPI. MIPI does not make any search or investigation for IPR, nor does MIPI require or request the disclosure of any IPR or claims of IPR as respects the contents of this Document or otherwise.

Questions pertaining to this document, or the terms or conditions of its provision, should be addressed to:

MIPI Alliance, Inc.
c/o IEEE-ISTO
445 Hoes Lane
Piscataway, NJ 08854
Attn: Board Secretary

Contents

Contents	iii
Figures	vi
Tables	xii
Release History	xiii
Introduction	1
Terminology	3
Use of Special Terms	3
Abbreviations	3
Acronyms	3
References	4
Section 1 TX Timers and Signaling	5
Overview	5
Group 1 LP-TX Signaling Requirements	6
Test 1.1.1 Thevenin Output High Level Voltage (V_{OH})	7
Test 1.1.2 LP-TX Thevenin Output Low Level Voltage (V_{OL})	10
Test 1.1.3 LP-TX 15%-85% Rise Time (T_{RLP})	12
Test 1.1.4 LP-TX 15%-85% Fall Time (T_{FLP})	15
Test 1.1.5 LP-TX Slew Rate vs. C_{LOAD} ($\delta V/\delta t_{SR}$)	17
Test 1.1.6 LP-TX Pulse Width of Exclusive-OR Clock ($T_{LP-PULSE-TX}$)	23
Test 1.1.7 LP-TX Period of Exclusive-OR Clock ($T_{LP-PER-TX}$)	26
Group 2 HS-TX Burst Signaling Requirements	28
Test 1.2.1 T_{LPX} Duration	29
Test 1.2.2 $T_{3-PREPARE}$ Duration	31
Test 1.2.3 $T_{3-PREBEGIN}$ Duration	33
Test 1.2.4 $T_{3-PROGSEQ}$ Duration	35
Test 1.2.5 $T_{3-PREEND}$ Duration	37
Test 1.2.6 T_{3-SYNC} Duration	39
Test 1.2.7 HS-TX Differential Voltages (V_{OD-AB} , V_{OD-BC} , V_{OD-CA})	41
Test 1.2.8 HS-TX Differential Voltage Mismatch (ΔV_{OD})	45
Test 1.2.9 HS-TX Single-Ended Output High Voltages ($V_{OHHS(VA)}$, $V_{OHHS(VB)}$, $V_{OHHS(VC)}$)	47
Test 1.2.10 HS-TX Static Common-Point Voltages (V_{CPTX})	50
Test 1.2.11 HS-TX Static Common-Point Voltage Mismatch ($\Delta V_{CPTX(HS)}$)	54
Test 1.2.12 HS-TX Dynamic Common-Point Variations Between 50-450MHz ($\Delta V_{CPTX(LF)}$)	56
Test 1.2.13 HS-TX Dynamic Common-Point Variations Above 450MHz ($\Delta V_{CPTX(HF)}$)	59
Test 1.2.14 HS-TX Rise Time (t_R)	61
Test 1.2.15 HS-TX Fall Time (t_F)	63
Test 1.2.16 T_{3-POST} Duration	65
Test 1.2.17 30%-85% Post-EoT Rise Time (T_{REOT})	67
Test 1.2.18 $T_{HS-EXIT}$ Value	69
Test 1.2.19 HS Clock Instantaneous UI (UI_{INST})	71
Test 1.2.20 HS Clock Delta UI (ΔUI)	73
Group 3 LP-TX INIT, ULPS, and BTA Requirements	75
Test 1.3.1 INIT: LP-TX Initialization Period ($T_{INIT,MASTER}$)	76

Test 1.3.2	ULPS Exit: Transmitted T _{WAKEUP} Interval	78
Test 1.3.3	BTA: TX-Side T _{TA-GO} Interval Value	80
Test 1.3.4	BTA: RX-Side T _{TA-SURE} Interval Value	82
Test 1.3.5	BTA: RX-Side T _{TA-GET} Interval Value	84
Section 2	RX Timers and Electrical Tolerances	87
Overview	87	
Group 1	LP-RX Voltage and Timing Requirements.....	88
Test 2.1.1	LP-RX Logic 1 Input Voltage (V _{IH})	89
Test 2.1.2	LP-RX Logic 0 Input Voltage, Non-ULP State (V _{IL})	91
Test 2.1.3	LP-RX Input Hysteresis (V _{HYST})	93
Test 2.1.4	LP-RX Minimum Pulse Width Response (T _{MIN-RX})	97
Test 2.1.5	LP-RX Input Pulse Rejection (e _{SPIKE}).....	99
Group 2	LP-RX Behavioral Requirements	103
Test 2.2.1	LP-RX Initialization period (T _{INIT}).....	104
Test 2.2.2	ULPS Exit: LP-RX T _{WAKEUP} Timer Value	106
Test 2.2.3	LP-RX Invalid/Aborted Escape Mode Entry	108
Test 2.2.4	LP-RX Invalid/Aborted Escape Mode Command.....	110
Test 2.2.5	LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits.....	113
Test 2.2.6	LP-RX Escape Mode Unsupported/Unassigned Commands	116
Group 3	HS-RX Voltage and Jitter Tolerance Requirements	118
Test 2.3.1	HS-RX Amplitude Tolerance (V _{CPRX(DC)} , V _{IHHS} , V _{ILHS})	119
Test 2.3.2	HS-RX Differential Input High/Low Thresholds (V _{IDTH} , V _{IDTL}).....	123
Test 2.3.3	HS-RX Jitter Tolerance	125
Group 4	HS-RX Timer Requirements	131
Test 2.4.1	HS-RX T _{3-TERM-EN} Duration	132
Test 2.4.2	HS-RX T _{3-PREPARE} Tolerance	134
Test 2.4.3	HS-RX T _{3-PREBEGIN} Tolerance	136
Test 2.4.4	HS-RX T _{3-PROGSEQ} Tolerance	138
Test 2.4.5	Test 2.4.5 HS-RX T _{3-POST} Tolerance	140
Section 3	Interface Impedance and S-Parameters	143
Overview	143	
Group 1	HS-TX S-Parameters and Impedance	144
Test 3.1.1	HS-TX Differential Return Loss (SDD22).....	145
Test 3.1.2	HS-TX Common-Mode Return Loss (SCC22)	148
Test 3.1.3	HS-TX Mode Conversion Limits (SDC22).....	150
Test 3.1.4	HS-TX Single-Ended Output Impedance (Z _{OS}).....	152
Test 3.1.5	HS-TX Single-Ended Output Impedance Mismatch (ΔZ _{OS})	154
Group 2	HS-RX S-Parameters and Impedance	156
Test 3.2.1	HS-RX Differential Return Loss (SDD11).....	157
Test 3.2.2	HS-RX Common-Mode Return Loss (SCC11)	160
Test 3.2.3	HS-RX Mode Conversion Limits (SDC11).....	163
Test 3.2.4	HS-RX Differential Input Impedance (Z _{ID}).....	165
Test 3.2.5	HS-RX Differential Input Impedance Mismatch (ΔZ _{ID})	167
Group 3	LP-TX/RX Impedance Requirements.....	169
Test 3.3.1	LP-TX Output Impedance (Z _{OLOP})	170
Test 3.3.2	LP-RX Input Leakage Current (I _{LEAK})	173

Annexes	175
Overview	175
Scope of Tests	175
Annex A Resource Requirements (DUTs and Test Equipment).....	177
A.1 LP/HS Transmitter Tests.....	178
A.2 Receiver Tests.....	179
A.3 S-Parameter and Impedance Tests.....	180
Annex B Test Setups	181
B.1 Transmitter Tests	182
B.1.1 LP Transmitter Tests	182
B.1.2 HS Transmitter Tests.....	183
B.1.3 Bus Turnaround Tests	185
B.2 Receiver Tests	186
B.3 Other Tests.....	187
B.3.1 Impedance and S-Parameter Tests	187
B.3.2 LP-TX Output Impedance	187
B.3.3 LP-RX Input Leakage Current	188
Annex C Statistical Methodology for Bit Error Rate (BER) Verification	189
C.1 Introduction.....	190
C.2 Statistical Model.....	190
C.3 Hypothesis Test.....	191
C.4 Confidence Interval	192
C.5 Sample Test Construction	194
C.6 Packet Error Rate Measurement.....	195
Annex D Standardized Software Interface for Test Automation	197
D.1 Introduction.....	198
D.2 Software Interface Definition	198
Annex E MIPI Product Registry Requirements for C-PHY	201
Annex F RX Test Observables for DUT Device Types	205
F.1 Introduction.....	205
F.2 Bare C-PHY	205
F.3 DSI-2 Display Device (C-PHY + DSI-2 Protocol + Display Driver + Glass, Integrated)	206
F.4 CSI-2 Image Sensor (C-PHY + CSI-2 Protocol + Image Sensor Module)	208
F.5 Lane-Dependent Limitations of LP Test Patterns.....	208
F.6 Lane Remapping.....	208
Contributing Individuals.....	211

Figures

Figure 1.1.1-1: V _{OH} Specification Definition	7
Figure 1.1.1-2: V _{OH} Specification Conformance Limits.....	7
Figure 1.1.1-3: Example V _A ULPS Waveform and V _{OH} /V _{OL} Measurement.....	8
Figure 1.1.2-1: V _{OL} Specification Definition.....	10
Figure 1.1.2-2: V _{OL} Specification Conformance Limits.....	10
Figure 1.1.3-1: T _{RLP} Specification Definition.....	12
Figure 1.1.3-2: T _{RLP} Specification Conformance Limits	12
Figure 1.1.3-3: Example T _{RLP} Measurement	13
Figure 1.1.4-1: T _{RLP} Specification Definition.....	15
Figure 1.1.5-1: $\delta V/\delta t_{SR}$ Specification Definition.....	17
Figure 1.1.5-2: Slew Rate vs. C _{LOAD} Requirements	17
Figure 1.1.5-3: Sample LP Falling Edge Slew Rate Measurement	20
Figure 1.1.5-4: Zoomed-in View of Slew Rate Data.....	20
Figure 1.1.5-5: Sample LP Rising Edge Slew Rate Measurement	21
Figure 1.1.5-6: Zoomed-in View of Slew Rate Data.....	21
Figure 1.1.6-1: LP XOR Clock Generation from V _A and V _C	23
Figure 1.1.6-2: LP XOR Clock Pulse Conformance Requirements	24
Figure 1.1.6-3: T _{LP-PULSE-TX} Specification Definition.....	24
Figure 1.1.7-1: LP XOR Clock Extraction from V _A and V _C	26
Figure 1.1.7-2: T _{LP-PER-TX} Conformance Requirements	27
Figure 1.2.1-1: T _{LPX} Specification Definition.....	29
Figure 1.2.1-2: Data Lane T _{LPX} Interval	29
Figure 1.2.2-1: T _{3-PREPARE} Interval	31
Figure 1.2.2-2: T _{3-PREPARE} Interval Definition and Conformance Range	31
Figure 1.2.3-1: T _{3-PREBEGIN} Interval.....	33
Figure 1.2.3-2: T _{3-PREBEGIN} Conformance Requirements	33
Figure 1.2.4-1: T _{3-PROGSEQ} Interval.....	35
Figure 1.2.4-2: T _{3-PROGSEQ} Definition.....	35
Figure 1.2.4-3: T _{3-PROGSEQ} Length Requirements.....	36
Figure 1.2.5-1: T _{3-PREEND} Interval	37
Figure 1.2.5-2: T _{3-PREEND} Definition and Conformance Requirements.....	37

Figure 1.2.6-1: T _{3-SYNC} Interval	39
Figure 1.2.6-2: T _{3-SYNC} Definition	39
Figure 1.2.6-3: T _{3-SYNC} Length Requirements	39
Figure 1.2.7-1: V _{OD} Specification Definition	41
Figure 1.2.7-2: V _{OD} Specification Conformance Requirements	41
Figure 1.2.7-3: Sample V _{OD} Measurement at 20% UI Width	42
Figure 1.2.7-4: Zoomed-In View Showing Max/Min Measurements	43
Figure 1.2.8-1: ΔV _{OD} Specification Definition	45
Figure 1.2.8-2: ΔV _{OD} Specification Conformance Requirements	45
Figure 1.2.9-1: V _{OHHS} Specification Definition	47
Figure 1.2.9-2: V _{OHHS} Specification Conformance Requirements	47
Figure 1.2.9-3: Sample Single-Ended V _{OHHS(VA)} Eye Diagram and Measurement	48
Figure 1.2.9-4: Zoomed-In View Showing Mean Measurement	49
Figure 1.2.10-1: V _{CPTX} Specification Definition	50
Figure 1.2.10-2: V _{CPTX} Specification Conformance Requirements	50
Figure 1.2.10-3: Static V _{CPTX} Distortion	51
Figure 1.2.10-4: Sample +x, +y, +z V _{CPTX} Histograms	51
Figure 1.2.10-5: Sample -x, -y, -z V _{CPTX} Histograms	52
Figure 1.2.11-1: ΔV _{CPTX(HS)} Specification Definition	54
Figure 1.2.11-2: ΔV _{CPTX(HS)} Specification Conformance Requirements	54
Figure 1.2.12-1: ΔV _{CPTX(LF)} Specification Definition	56
Figure 1.2.12-2: ΔV _{CPTX(LF)} Specification Conformance Requirements	56
Figure 1.2.12-3: Dynamic V _{CPTX} Distortion	57
Figure 1.2.12-4: ΔV _{CPTX} Test Filter Responses (50-450MHz BPF shown in blue)	57
Figure 1.2.13-1: ΔV _{CPTX(HF)} Specification Definition	59
Figure 1.2.13-2: ΔV _{CPTX(HF)} Specification Conformance Requirements	59
Figure 1.2.14-1: t _R Specification Definition	61
Figure 1.2.14-2: t _R Conformance Limits	61
Figure 1.2.15-1: t _F Specification Definition	63
Figure 1.2.16-1: T _{3-POST} Interval	65
Figure 1.2.16-2: T _{3-POST} Specification Definition	65
Figure 1.2.16-3: T _{3-POST} Length Requirements	66
Figure 1.2.17-1: T _{REOT} Specification Definition	67

Figure 1.2.17-2: T _{REOT} Rise Time	67
Figure 1.2.18-1: T _{HS-EXIT} Interval.....	69
Figure 1.2.18-2: T _{HS-EXIT} Specification Definition	69
Figure 1.2.19-1: UI _{INST} Interval.....	71
Figure 1.2.19-2: UI _{INST,MIN} Specification Definition.....	71
Figure 1.2.19-3: UI _{INST} Specification Conformance Requirements	72
Figure 1.2.20-1: ΔUI Specification and Limits	73
Figure 1.3.1-1: T _{INIT,MASTER} Specification Definition.....	76
Figure 1.3.1-2: T _{INIT,MASTER} Specification Minimum Requirement	76
Figure 1.3.1-3: T _{INIT} Conformance Limits.....	76
Figure 1.3.2-1: T _{WAKEUP} Specification Definition.....	78
Figure 1.3.2-2: T _{WAKEUP} Conformance Limits	78
Figure 1.3.3-1: T _{TA-GO} Interval.....	80
Figure 1.3.3-2: T _{TA-GO} Specification Definition and Conformance Requirements	80
Figure 1.3.4-1: T _{TA-SURE} Interval.....	82
Figure 1.3.4-2: T _{TA-SURE} Specification Definition.....	82
Figure 1.3.4-3: T _{TA-SURE} Specification Definition.....	83
Figure 1.3.5-1: T _{TA-GET} Interval	84
Figure 1.3.5-2: T _{TA-GET} Definition and Conformance Limits.....	84
Figure 2.1.1-1: V _{IH} Specification Definition	89
Figure 2.1.1-2: V _{IH} Conformance Requirements	89
Figure 2.1.2-1: V _{IL} Specification Definition.....	91
Figure 2.1.3-1: V _{HYST} Specification Definition	93
Figure 2.1.3-2: V _{HYST} Conformance Requirements	93
Figure 2.1.4-1: T _{MIN-RX} Specification Requirement	97
Figure 2.1.4-2: T _{MIN-RX} Conformance Limits	97
Figure 2.1.4-3: T _{MIN-RX} Interval	98
Figure 2.1.5-1: eSPIKE Specification Definition.....	99
Figure 2.1.5-2: eSPIKE Specification Requirements	99
Figure 2.1.5-3: Example eSPIKE Glitch	100
Figure 2.1.5-4: Max Depth/Min Duration Negative Glitch.....	101
Figure 2.1.5-5: Max Depth/Min Duration Positive Glitch	101
Figure 2.2.1-1: T _{INIT} Specification Requirement	104

Figure 2.2.1-2: T_{INIT} Minimum Conformance Limit	104
Figure 2.2.3-1: Escape Mode Entry Specification Definition	108
Figure 2.2.3-2: Escape Mode Entry Procedure (with Trigger-Reset Command)	108
Figure 2.2.3-3: Escape Mode Entry Abort Specification Definition	109
Figure 2.2.4-1: Complete Escape Mode Sequence (Trigger-Reset Command Shown).....	110
Figure 2.2.4-2: Space State Specification Requirement	111
Figure 2.2.4-3: Escape Mode LP-11 Specification Requirement	111
Figure 2.2.4-4: Stop State Specification Requirement	111
Figure 2.2.5-1: Escape Mode Trigger Extra Bits Specification Requirement	113
Figure 2.2.5-2: Assigned Escape Mode Entry Command Codes.....	114
Figure 2.2.5-3: Escape Mode ULPS Specification Requirement	114
Figure 2.2.6-1: Assigned Escape Mode Entry Command Codes.....	116
Figure 2.2.6-2: Escape Mode Unspecified Command Specification Requirement	116
Figure 2.3.1-1: $V_{CPRX(DC)}$, V_{IHHS} , V_{ILHS} Specification Definitions	119
Figure 2.3.1-2: $V_{CPRX(DC)}$, V_{IHHS} , V_{ILHS} Specification Conformance Requirements	119
Figure 2.3.1-3 Illustration Showing Differential and Single-Ended Levels	121
Figure 2.3.2-1: V_{IDTH} Specification Definition.....	123
Figure 2.3.2-2: V_{IDTH} , V_{IDTL} Conformance Limits.....	123
Figure 2.3.3-1: RX Timing Specification Requirement	125
Figure 2.3.3-2: HS-RX Eye Diagram	126
Figure 2.3.3-3: HS-RX Eye Diagram Timing Values	126
Figure 2.3.3-4: Template for Differential Insertion Losses, C-PHY Legacy Channel	127
Figure 2.3.3-5: HS-RX ‘Triggered Eye’ Diagram	127
Figure 2.3.3-6: HS-RX Final Calibrated Eye	128
Figure 2.4.1-1: $T_{3-TERM-EN}$ Specification Definition and Conformance Requirements	132
Figure 2.4.1-2: $T_{3-TERM-EN}$ Interval	132
Figure 2.4.2-1: $T_{3-PREPARE}$ Interval	134
Figure 2.4.2-2: $T_{3-PREPARE}$ Interval Conformance Requirements.....	134
Figure 2.4.2-3: $T_{3-PREPARE}$ RX Specification Definition.....	135
Figure 2.4.3-1: $T_{3-PREBEGIN}$ Interval	136
Figure 2.4.3-2: $T_{3-PREBEGIN}$ Interval Recommended Length Requirements.....	136
Figure 2.4.4-1: $T_{3-PROGSEQ}$ Interval.....	138
Figure 2.4.4-2: $T_{3-PROGSEQ}$ Interval Description	138

Figure 2.4.4-3: T ₃ -PROGSEQ Length.....	138
Figure 2.4.5-1: T ₃ -POST Interval	140
Figure 2.4.5-2: T ₃ -POST Interval Definition.....	140
Figure 2.4.5-3: T ₃ -POST Interval Length.....	140
Figure 3.1.1-1: HS-TX Differential Return Loss Conformance Limits	145
Figure 3.1.1-2: Differential Return Loss Specification Requirement.....	146
Figure 3.1.1-3: f _{MAX} Definition	146
Figure 3.1.1-4: f _h Definition	146
Figure 3.1.1-5: f _{LP,MAX} Definition	146
Figure 3.1.1-6: Example Conformant HS-TX Differential Return Loss Result.....	147
Figure 3.1.2-1: TX Common-Mode Return Loss Specification Requirement	148
Figure 3.1.2-2: Example Conformant HS-TX Common-Mode Return Loss Result.....	149
Figure 3.1.3-1: Mode Conversion Specification Requirement.....	150
Figure 3.1.3-2: Example Conformant HS-TX Mode Conversion Loss Result.....	151
Figure 3.1.4-1: Z _{OS} Specification Definition	152
Figure 3.1.4-2: Z _{OS} Specification Measurement.....	152
Figure 3.1.4-3: Z _{OS} Conformance Requirements.....	152
Figure 3.1.4-4: Example HS-TX Z _{OS} Measurement.....	153
Figure 3.1.5-1: ΔZ _{OS} Specification	154
Figure 3.1.5-2: ΔZ _{OS} Conformance Requirements	154
Figure 3.2.1-1: HS-RX Differential Return Loss Conformance Limits	157
Figure 3.2.1-2: HS-RX Differential Return Loss Conformance Requirement.....	157
Figure 3.2.1-3: Example Conformant HS-RX Differential Return Loss Result.....	158
Figure 3.2.2-1: Common-Mode Return Loss Conformance Limits	160
Figure 3.2.2-2: Common-Mode Reflection Specification Requirement	160
Figure 3.2.2-3: f _{INT} Specification Definition	160
Figure 3.2.2-4: f _{INT} Specification Value.....	161
Figure 3.2.2-5: Example Conformant HS-RX Common-Mode Return Loss Result.....	161
Figure 3.2.3-1: Mode Conversion Specification Requirement.....	163
Figure 3.2.3-2: Example Conformant HS-RX Mode Conversion Loss Result	164
Figure 3.2.4-1: Z _{ID} Specification Definition.....	165
Figure 3.2.4-2: Z _{ID} Conformance Requirements	165
Figure 3.2.4-3: Example HS-RX Z _{ID} Measurement	166

Figure 3.2.5-1: ΔZ_{ID} Specification.....	167
Figure 3.2.5-2: ΔZ_{ID} Conformance Requirements	167
Figure 3.3.1-1: VI Characteristic Plots, and Setup for Z_{OLP} Measurement.....	170
Figure 3.3.1-2: Z_{OLP} Conformance Requirements	171
Figure 3.3.2-1: I_{LEAK} Specification Definition.....	173
Figure 3.3.2-2: Example I_{LEAK} Measurement Diagram	173
Figure 3.3.2-3: V_{PIN} , I_{LEAK} Conformance Requirements	174
Figure A.1-1: MIPI C-PHY Reference Termination Board (RTB).....	178
Figure B-1-1: LP Transmitter Test Setup.....	182
Figure B-1-2a: HS Transmitter Test Setup (Differential Probes, with RTB).....	183
Figure B-1-2b: HS Transmitter Test Setup	184
Figure B-1-3: Bus Turnaround Test Setup.....	185
Figure B-2a: LP/HS-RX Test Setup (Bare Phy)	186
Figure B-2b: LP/HS-RX Test Setup (Combined IC with Phy + Protocol Layers)	186
Figure B-2c: LP/HS-RX Test Setup (Complete Display Device).....	186
Figure B-3-1: S-Parameter/Return Loss Test Setup	187
Figure B-3-2: LP-TX Output Impedance (Z_{OLP}) Test Setup	187
Figure B-3-3: LP-RX Input Leakage Current (I_{LEAK}) Test Setup	188
Figure C-1: Computing the Probability that $z \geq -1.645$ (Standard Normal Distribution).	192

Tables

Table 2.3.1-1: Differential/Common-Mode Amplitude Test Cases	120
Table 2.4.2-1: HS Receiver T _{3-PREPARE} Test Cases	135
Table 2.4.2-2: HS-RX T _{3-PREPARE} Test Nominal Timer Values.....	135
Table 2.4.3-1: HS-RX T _{3-PREBEGIN} Test Nominal Timer Values	137
Table 2.4.4-1: HS-RX T _{3-PROGSEQ} Test Cases	139
Table 2.4.4-2: HS-RX T _{3-PROGSEQ} Test Nominal Timer Values	139
Table 2.4.5-1: HS-RX T _{3-POST} Test Nominal Timer Values.....	141
Table C-1 Acceptance and Rejections Regions for H ₀	191
Table C-2 Definitions of Type I and Type II Errors.....	191
Table C-3 n and k _l as a Function of β and α.....	194
Table E-1: Product Registry Test Applicability	201

Release History

Date	Version	Description
2016-02-13	v1.0	Initial Board approved release.

This page intentionally left blank.

Introduction

The Phy working group of MIPI Alliance has developed this Conformance Test Suite (CTS) in an effort to improve the interoperability of MIPI Specification-based products. This document defines a set of conformance or interoperability tests whereby a product can be tested against other implementations of a common Specification.

It is important to recognize that this document is not a compliance test suite. In contrast to other industry consortia, MIPI does not approve or certify that any products are in compliance with its specifications, and MIPI does not currently define an official Qualification Program.

This particular suite of tests has been developed to help implementers evaluate the C-PHY v1.0 functionality of their products. The test suite is a tool to help member companies evaluate the conformance of products according to Specifications developed by MIPI Alliance.

These tests are designed to determine if a product conforms to specifications defined in the MIPI Alliance Specification for C-PHY v1.0 (hereafter referred to as the “C-PHY Specification”). Successful completion of all tests contained in this suite does not guarantee that the tested device will successfully operate with other products. However, when combined with satisfactory level of interoperability testing, these tests provide a reasonable level of confidence that the Device Under Test (DUT) will function properly in many environments.

Tests contained in this document are organized in order to simplify the identification of information related to a test, and to facilitate in the actual testing process. Tests are separated into groups, primarily in order to reduce setup time in the lab environment, though the different test groups typically also tend to focus on specific aspects of device functionality. A three-number, dot-notated naming system, <S>.<G>.<N>, is used to catalog the tests, where the first number, <S>, indicates the specific section of the Specification on which the test suite is based. The second number, <G>, indicates the test group number, and the third number, <N>, indicates the test number within that group. This format allows for the addition of future tests in the appropriate groups without requiring renumbering of subsequent tests.

The test definitions themselves are intended to provide a high-level description of the motivation, resources, procedures, and methodologies specific to each test. Formally, each test description contains the following sections.

Purpose

The “Purpose” is a brief statement outlining what the test attempts to achieve. The test is written at the functional level.

References

The “References” section specifies all reference material external to the test suite, including a reference to the Specification for the test in question and any other references that might be helpful in understanding the test methodology or test results. External sources are always referenced by a bracketed indicator, e.g., [MIPI01], when mentioned in the test description. Any other references in the test description that are not indicated in this manner refer to elements within the test suite document itself, e.g., “Annex A”, or “Table 5”).

Resource Requirements

The “Resource Requirements” section specifies the test hardware and software needed to perform the test. These requirements are expressed in terms of minimum test equipment needed, and do not include specific mention of particular makes and models of test equipment.

Last Modification

The “Last Modification” section specifies the date of the last modification to this test.

44 Discussion

45 The “Discussion” section describes the assumptions made in the design or implementation of the test, as
46 well as any known limitations. Other items specific to the test are described here as well.

47 Test Setup

48 The “Test Setup” section describes the initial configuration of the test environment. Small changes in the
49 configuration should not be included here and should generally be covered in the “Procedure” section.

50 Procedure

51 The “Procedure” section of the test description contains the systematic instructions for carrying out the test.
52 This section provides a step-by-step approach to testing, and it may contain observable results interspersed
53 with the test steps.

54 Observable Results

55 The “Observable Results” section lists the specific observable values and conditions that can be examined
56 by the tester in order to verify that the DUT is operating properly. When multiple values for an observable
57 result are possible, this section provides a short discussion on how to interpret them. The determination of a
58 pass or fail outcome for a particular test is generally based on the successful, or unsuccessful, detection of a
59 specific observable result.

60 Possible Problems

61 The “Possible Problems” section contains a description of known issues with the test procedure, which
62 might affect test results in certain situations. This section might also refer the reader to a test suite annex or
63 other external source that provides more detail regarding these issues.

Terminology

64 Also see Section 2 in [*MIPI01*].

Use of Special Terms

66 The MIPI Alliance has adopted Section 13.1 of the *IEEE Standards Style Manual*, which dictates use of the
67 words “shall”, “should”, “may”, and “can” in the development of documentation, as follows:

68 The word *shall* is used to indicate mandatory requirements strictly to be followed in order
69 to conform to the Specification and from which no deviation is permitted (*shall* equals *is*
70 *required to*).

71 The use of the word *must* is deprecated and shall not be used when stating mandatory
72 requirements; *must* is used only to describe unavoidable situations.

73 The use of the word *will* is deprecated and shall not be used when stating mandatory
74 requirements; *will* is only used in statements of fact.

75 The word *should* is used to indicate that among several possibilities one is recommended
76 as particularly suitable, without mentioning or excluding others; or that a certain course
77 of action is preferred but not necessarily required; or that (in the negative form) a certain
78 course of action is deprecated but not prohibited (*should* equals *is recommended that*).

79 The word *may* is used to indicate a course of action permissible within the limits of the
80 Specification (*may* equals *is permitted to*).

81 The word *can* is used for statements of possibility and capability, whether material,
82 physical, or causal (*can* equals *is able to*).

83 All sections are normative, unless they are explicitly indicated to be informative.

Abbreviations

85 e.g. For example (Latin: exempli gratia)

86 i.e. That is (Latin: id est)

Acronyms

87 ISTO Industry Standards and Technology Organization

References

- 89 [MIPI01] *Specification for C-PHY*, version 1.0, MIPI Alliance, Inc., 5 August 2014.
90 [MIPI02] *MIPI Product Registry*, <<http://mipi.org/>>, MIPI Alliance, Inc., (In press).
91 [MIPI03] *Policy and Procedures for the MIPI Product Registry Program*, version 1.0, MIPI
92 Alliance, Inc., (In press).

Section 1 TX Timers and Signaling

Overview

This section of tests verifies various signaling and timing requirements of C-PHY transceivers [*MIPI01*].

- Group 1 (Tests 1.1.x) verifies various requirements specific to LP-TX signaling.
- Group 2 (Tests 1.2.x) verifies various requirements specific to HS-TX signaling.
- Group 3 (Tests 1.3.x) verifies various requirements specific to Initialization, ULPS, and BTA behavior.

Comments and questions regarding the documentation and/or implementation of these tests are welcome, and can be sent to test-wg@mipi.org.

Group 1 LP-TX Signaling Requirements

Overview

This group of tests verifies various requirements specific to LP signaling. The intent of the structure of this Group is to facilitate performing a set of related LP-TX measurements on a single Lane LP-TX waveform sequence (e.g., ULPS Entry).

Status

The test names, Discussion sections, and Procedures are sufficiently defined to reflect the current state of implementation, and most tests have been successfully performed on multiple devices.

Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

Test 1.1.1 Thevenin Output High Level Voltage (V_{OH})

Purpose

To verify that the Thevenin Output High Level Voltage (V_{OH}) of the DUT's LP transmitter is within the conformance limits.

References

- [1] C-PHY Specification, Section 9.1.2
- [2] Ibid, Table 24

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for V_{OH} , which is a device's LP-TX Thevenin Output High Level Voltage.

The specification states[1],

1072 V_{OL} is the Thevenin output, low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad
1073 pin in the low-level state. V_{OH} is the Thevenin output, high-level voltage in the high-level state, when the pad
1074 pin is not loaded. The LP transmitter shall not drive the pad pin potential statically beyond the maximum
1075 value of V_{OH} . The pull-up and pull-down output impedances of LP transmitters shall be as described in Figure
1076 45 and Figure 46, respectively. The circuit for measuring V_{OL} and V_{OH} is shown in Figure 47.

Figure 1.1.1-1: V_{OH} Specification Definition

Furthermore, the limits for V_{OH} are defined via the following table.

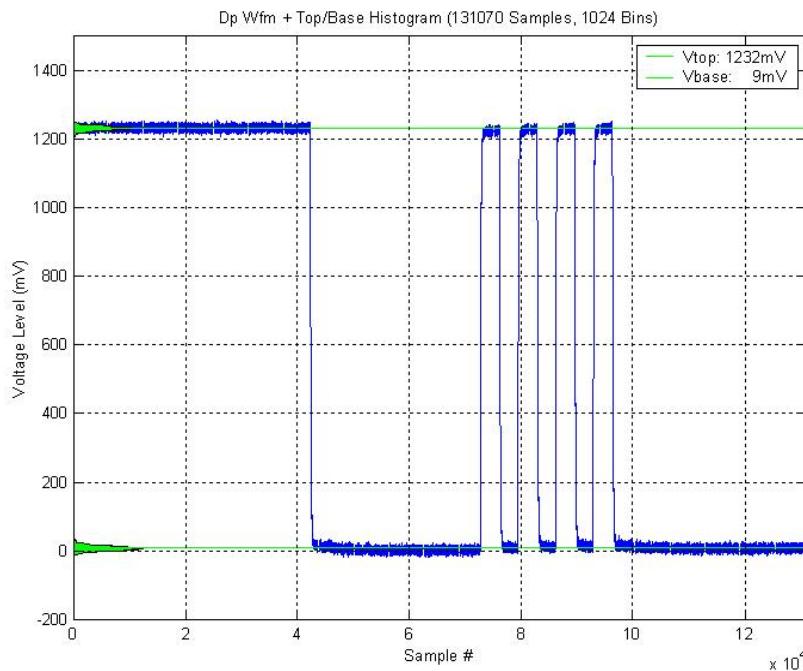
Table 24 LP Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{OH}	Thevenin output high level	0.95		1.3	V	

Figure 1.1.1-2: V_{OH} Specification Conformance Limits

In this test, the DUTs V_{OH} values will be measured using a high-speed, real-time DSO while the DUT is driving an LP signaling sequence into an open termination. (Note that this test is intended to be performed in conjunction with the other tests in this group on a single captured LP Escape Mode sequence waveform, where the measurement is performed on the output-high states only.) For the purposes of this measurement, V_{OH} is measured as the mode of all waveform samples that are greater than 50% of the absolute peak-to-peak V_{DP} and V_{DN} signal amplitudes, and should be measured across all LP-1 states in a single LP Escape Mode sequence. (Note that a ULPS Entry sequence is specified for this test, and all other measurements in this Group, as this should normally be supported on all Lanes for most DUTs.) This measurement shall be performed separately on the V_A , V_B , and V_C waveforms, and for each Lane.

An example V_A waveform and measurement is shown below.



138

Figure 1.1.1-3: Example V_A ULPS Waveform and V_{OH}/V_{OL} Measurement

139 Also, while the capacitive characteristics of the termination should not affect the static high and low levels,
 140 this test will be performed with the 50pF C_{LOAD} test fixture (see Discussion, Test 1.1.3, for details). Note
 141 that the results are expected to be independent of the termination capacitance, however the purpose of using
 142 the 50pF test load for this test is primarily just for procedural consistency with the other LP tests in this
 143 section, as all of the other measurements are performed using the 50pF load.

144 Also, to reduce measurement noise, a 400-MHz, 4th-order Butterworth lowpass test filter will be applied to
 145 the source waveform prior to performing the measurement. (See Test 1.1.5 Discussion for details.)

146 For all Lanes, the value of V_{OH} for both the V_A , V_B , and V_C signals must be between 0.95V and 1.3V in
 147 order to be considered conformance[2].

148 **Test Setup**

149 See Annex B.1.1.

150 **Test Procedure**

- 151 • Connect the DUT's Lane 0 to the Test Setup, using the 50pF C_{LOAD} test fixture.
- 152 • Create a condition that causes the DUT to source a ULPS Entry sequence on Lane 0.
- 153 • Capture the LP signaling sequence using the DSO.
- 154 • Using post-processing methods, measure V_{OH} for both the V_A , V_B , and V_C signals as described
 155 above.
- 156 • Repeat the previous four steps for all other Lanes (if the DUT implements multiple Lanes).

157 **Observable Results**

158 For all Lanes:

- 159 • Verify that V_{OH} for the V_A waveform is between 0.95 and 1.3 Volts.
- 160 • Verify that V_{OH} for the V_B waveform is between 0.95 and 1.3 Volts.

- 161 • Verify that V_{OH} for the V_C waveform is between 0.95 and 1.3 Volts.

162 **Possible Problems**

163 Because the V_{OH} and V_{OL} measurements are performed as mode measurements (rather than mean), the
164 measurement will tend to be dominated by the most popular level in the waveform capture. This will often
165 be the ‘static’ LP-0/1 levels occurring before and after the burst of edges. Waveforms should be sure to
166 include these sections of data in order to ensure the most stable and repeatable results.

Test 1.1.2 LP-TX Thevenin Output Low Level Voltage (V_{OL})

Purpose

To verify that the Thevenin Output Low Level Voltage (V_{OL}) of the DUT's LP transmitter is within the conformance limits.

References

- [1] C-PHY Specification, Section 9.1.2
- [2] Ibid, Table 24

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for V_{OL} , which is a device's LP-TX Thevenin Output Low Level Voltage.

The specification states[1],

1072 V_{OL} is the Thevenin output, low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad
1073 pin in the low-level state. V_{OH} is the Thevenin output, high-level voltage in the high-level state, when the pad

Figure 1.1.2-1: V_{OL} Specification Definition

The specification also defines limits for V_{OL} in the following table[2],

V_{OL}	Thevenin output low level	-50		50	mV	
Z_{OLP}	Output impedance of LP transmitter	110			Ω	1, 2

Figure 1.1.2-2: V_{OL} Specification Conformance Limits

In this test, the DUTs V_{OL} values will be measured using a high-speed, real-time DSO while the DUT is driving an LP signaling sequence into a 50pF C_{LOAD} test fixture. (Note that this test is intended to be performed in conjunction with the other tests in this group on a single captured LP Escape Mode sequence waveform, where the measurement is performed on the output-low bits only.)

For the purposes of this measurement, V_{OL} is measured as the mode of all waveform samples that are less than 50% of the absolute peak-to-peak V_A , V_B , and V_C signal amplitudes, and should be measured across all LP-0 states in a single LP Escape Mode sequence. (Note that a ULPS Entry sequence is specified for this test, and all other measurements in this Group, as this should normally be supported on all Data Lanes for most DUTs.) This measurement shall be performed separately on the V_A , V_B , and V_C waveforms, and for each Lane.

Also, to reduce measurement noise, a 400-MHz, 4th-order Butterworth lowpass test filter will be applied to the source waveform prior to performing the measurement. (See Test 1.1.5 Discussion for details.)

For all Lanes, the value of V_{OL} for the V_A , V_B , and V_C signals must be between -50mV and +50mV in order to be considered conformant[2].

199 **Test Setup**

200 See Annex B.1.1.

201 **Test Procedure**

- 202 • Connect the DUT's Lane 0 to the Test Setup, using the 50pF C_{LOAD} test fixture.
- 203 • Create a condition that causes the DUT to source a ULPS Entry sequence on Lane 0.
- 204 • Capture the LP signaling sequence using the DSO.
- 205 • Using post-processing methods, measure V_{OL} for both the V_A , V_B , and V_C signals as described above.
- 207 • Repeat the previous four steps for all other Lanes (if the DUT implements multiple Lanes).

208 **Observable Results:**

209 For all Lanes:

- 210 • Verify that V_{OL} for the V_A waveform is between -50 and +50mV.
- 211 • Verify that V_{OL} for the V_B waveform is between -50 and +50mV.
- 212 • Verify that V_{OL} for the V_C waveform is between -50 and +50mV.

213 **Possible Problems**

214 See Possible Problems of Test 1.1.1. The same applies to this test.

Test 1.1.3 LP-TX 15%-85% Rise Time (T_{RLP})

Purpose

To verify that the 15%-85% Rise Time (T_{RLP}) of the DUT's LP transmitter is within the conformance limits.

References

- [1] C-PHY Specification, Section 9.1.2
- [2] Ibid, Table 25
- [3] Ibid, Table 25, Note 1

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for T_{RLP} , which is a device's LP-TX 15%-85% Rise Time.

The specification states[1],

1082 The times t_{RLP} and t_{FLP} are the 15%-85% rise and fall times, respectively, of the output signal voltage, when
 1083 the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled
 1084 V_{OH} and V_{OL} voltages. The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over

Figure 1.1.3-1: T_{RLP} Specification Definition

The specification also provides limits in the following table[2].

Table 25 LP Transmitter AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
t_{RLP}/t_{FLP}	15% - 85% rise time and fall time			25	ns	1

Figure 1.1.3-2: T_{RLP} Specification Conformance Limits

Note that the specification states that the rise/fall times shall be measured into a capacitive load C_{LOAD} . C_{LOAD} is a separate parameter defined in the specification, which is used as a reference load for several LP requirements, of which rise/fall time is one.

Because the rise/fall time specification only defines an upper limit, the most meaningful approach would be to measure the rise/fall times using the maximum allowed C_{LOAD} (as this would result in the slowest edge, i.e., maximum rise time). If a DUT passes the rise/fall requirement with the maximum C_{LOAD} , it would only pass with greater margin (i.e., a smaller rise time) with a smaller C_{LOAD} value.

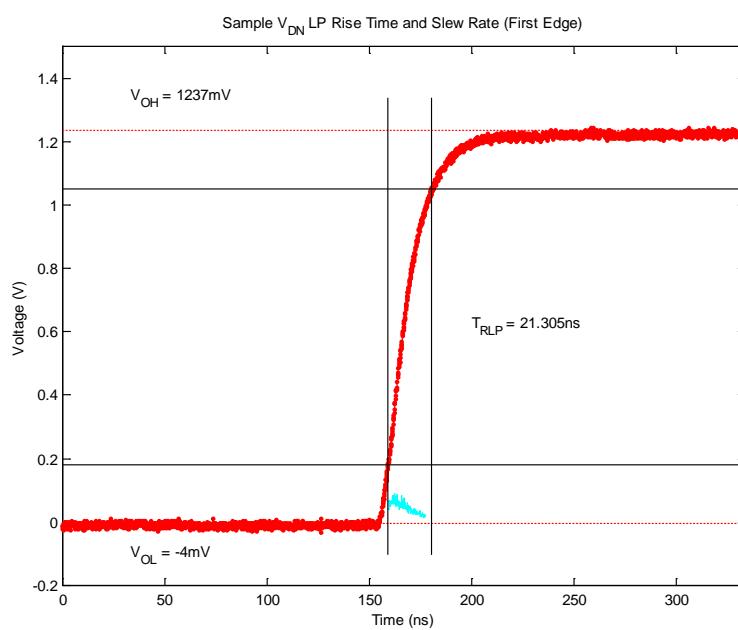
Note that choosing the exact values of C_{LOAD} for LP test purposes is somewhat challenging. The specification defines C_{LOAD} as having a range of 0 to 70pF[2]. The specification also explains that this load is considered distributed between three parts: 1) The transmitter's TX capacitance (up to 10pF), 2) The receiver's RX capacitance (up to 10pF), and 3) The transmission line between the TX and RX (up to 50pF)[3].

For practical purposes, there are several issues with the way the C_{LOAD} specification is defined. First, while exact load values (including 0pF) may be possible in a software simulation/design environment, practical measurements pose more of a problem, as the capacitance of the PCB boards and connectors on which the DUT is mounted are often unknown to the tester and cannot be controlled or removed. Furthermore, these elements, even if well-designed, cannot be designed to have zero capacitance. Therefore, testing at 0pF C_{LOAD} is not possible, and the minimum theoretical load will be dictated by the DUT's PCB itself, plus any added capacitance introduced by the test setup (i.e., probes, and any other associated connectors).

Thus the minimum capacitance is bounded by the DUT itself, and the test setup. For the maximum capacitance, a practical value must be chosen which takes all other factors into account, but still provides a reasonable measurement. It is possible to fabricate a test fixture/PCB that presents a lumped-value capacitance to the DUT transmitter. If this fixture was designed to be 70pF, this might over-stress the TX, as the total applied load including the DUT PCB and connector capacitance would then likely be greater than 70pF.

Therefore a practical compromise must be determined. For the purpose of conformance testing, a fixture with a capacitive load of 50pF will be used as the “maximum” C_{LOAD} . This accounts for the theoretical 10pF allotted for the TX, and also leaves an additional 10pF of ‘margin’, to account for non-ideal test boards, connectors, etc. Under this approach, the benefit of the doubt is given to the DUT, where if a DUT fails the rise/fall time test under a 50pF test load fixture, it would also most certainly fail more severely if measured under a true 70pF load. (Note that this approach may allow a marginal or slightly out-of-spec device to pass this test, however that accepted as the preferred case over failing a device that may be close to the limit, and/or mounted on a non-ideal evaluation board.)

In this test, the three single-ended V_A , V_B , and V_C signals from the DUTs LP transmitter will be captured using three channels of a real-time DSO. Using the measured V_{OH} and V_{OL} LP-TX Thevenin Output Voltage Levels as references (See Tests 1.1.1 and 1.1.2, respectively), the 15%-85% Rise Time (T_{RLP}) will be measured independently for each rising edge of the V_A , V_B , and V_C waveforms. The mean value across all observed rising edges will be computed to produce the final T_{RLP} result, and the maximum and minimum observed values will be reported as informative results. A sample measurement on a single edge is shown in the figure below.



273

Figure 1.1.3-3: Example T_{RLP} Measurement

274 Also, to reduce measurement noise, a 400-MHz, 4th-order Butterworth lowpass test filter will be applied to
275 the source waveform prior to performing the measurement. (See Test 1.1.5 Discussion for further details.)

276 For all Lanes, the value of T_{RLP} for V_A , V_B , and V_C must be less than 25ns in order to be considered
277 conformant[2].

278 **Test Setup**

279 See Annex B.1.1.

280 **Test Procedure**

- 281 • Connect the DUT's Lane 0 to the Test Setup, using the 50pF C_{LOAD} test fixture.
- 282 • Create a condition that causes the DUT to source a ULPS Entry sequence on Lane 0.
- 283 • Capture the LP signaling sequence using the DSO.
- 284 • Using post-processing methods, measure T_{RLP} for both V_{DP} and V_{DN} as described above.
- 285 • Repeat the previous steps for all other Lanes (if the DUT implements multiple Lanes).

286 **Observable Results**

287 For all Lanes:

- 288 • Verify that T_{RLP} for the V_A waveform is less than 25ns.
- 289 • Verify that T_{RLP} for the V_B waveform is less than 25ns.
- 290 • Verify that T_{RLP} for the V_C waveform is less than 25ns.

291 **Possible Problems**

292 Note that if a ULPS sequence is used for the measurement, there will be no rising edge present for V_B (as
293 this edge does not rise again until the ULPS exit sequence T_{WAKEUP} is transmitted). Therefore a risetime
294 measurement may not be possible for the V_B waveform.

Test 1.1.4 LP-TX 15%-85% Fall Time (T_{FLP})**Purpose**

To verify that the 15%-85% Fall Time (T_{FLP}) of the DUT's LP transmitter is within the conformance limits.

References

[1] C-PHY Specification, Section 9.1.2

[2] Ibid, Table 25

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for T_{FLP} , which is a device's LP-TX 15%-85% Fall Time.

The specification states[1],

1082 The times t_{RLP} and t_{FLP} are the 15%-85% rise and fall times, respectively, of the output signal voltage, when
1083 the LP transmitter is driving a capacitive load C_{LOAD} . The 15%-85% levels are relative to the fully settled
1084 V_{OH} and V_{OL} voltages. The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over

Figure 1.1.4-1: T_{RLP} Specification Definition

310 (Note the methodology for this test is identical to the LP-TX Rise Time test of 1.1.3, except the falling
311 edges will be measured. T_{FLP} will be measured with the 50pF C_{LOAD} fixture, and will be measured for all
312 Lanes.)

313 For all Lanes, the value of T_{FLP} for V_A , V_B , and V_C must be less than 25ns in order to be considered
314 conformant[2].

Test Setup

See Annex B.1.1.

Test Procedure

- 318 • Connect the DUT's Lane 0 to the Test Setup, using the 50pF C_{LOAD} test fixture.
- 319 • Create a condition that causes the DUT to source a ULPS Entry sequence on Lane 0.
- 320 • Capture the LP signaling sequence using the DSO.
- 321 • Using post-processing methods, measure T_{FLP} for V_A , V_B , and V_C as described above.
- 322 • Repeat the previous steps for all other Lanes (if DUT implements multiple Lanes).

Observable Results

For all Lanes:

- 325 • Verify that T_{FLP} for the V_A waveform is less than 25ns.
- 326 • Verify that T_{FLP} for the V_B waveform is less than 25ns.

327 • Verify that T_{FLP} for the V_C waveform is less than 25ns.

328 **Possible Problems**

329 None.

Test 1.1.5 LP-TX Slew Rate vs. C_{LOAD} ($\delta V/\delta t_{SR}$)

Purpose

To verify that the Slew Rate ($\delta V/\delta t_{SR}$) of the DUT's LP transmitter is within the conformance limits, for specific capacitive loading conditions.

References

- [1] C-PHY Specification, Section 9.1.2
- [2] Ibid, Table 25

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for $\delta V/\delta t_{SR}$, which is the DUT LP-TX Slew Rate.

The specification states[1],

1084 V_{OH} and V_{OL} voltages. The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over
 1085 time. The LP transmitter output signal transitions shall meet the maximum and minimum slew rate
 1086 specifications as shown in Table 25, Figure 48 and Figure 49. The intention of specifying a maximum slew
 1087 rate value is to limit EMI.

Figure 1.1.5-1: $\delta V/\delta t_{SR}$ Specification Definition

A copy of the specification table of slew rate requirements is reproduced below.

$\delta V/\delta t_{SR}$	Slew rate @ $C_{LOAD} = 0\text{pF}$		500	mV/ns	1, 3, 7, 8
	Slew rate @ $C_{LOAD} = 5\text{pF}$		300	mV/ns	1, 3, 7, 8
	Slew rate @ $C_{LOAD} = 20\text{pF}$		250	mV/ns	1, 3, 7, 8
	Slew rate @ $C_{LOAD} = 70\text{pF}$		150	mV/ns	1, 3, 7, 8
	Slew rate @ $C_{LOAD} = 0$ to 70pF (Falling Edge Only)	25		mV/ns	1, 2, 3
	Slew rate @ $C_{LOAD} = 0$ to 70pF (Rising Edge Only)	25		mV/ns	1, 3, 9
	Slew rate @ $C_{LOAD} = 0$ to 70pF (Rising Edge Only)	$25 - 0.0625 \cdot (V_{O,INST} - 550)$		mV/ns	1, 3, 10, 11
C_{LOAD}	Load capacitance	0	70	pF	1

Figure 1.1.5-2: Slew Rate vs. C_{LOAD} Requirements

348 Note that the above table in the specification contains several footnotes[2], which further clarify the limit
349 requirements listed in the table. While the individual notes are not reproduced here, a summary of the key
350 points as applicable to this test are as follows:

351 Falling edges:

- (Note 8): The maximum Slew Rate limits are applicable across the entire signal transition/edge.
- (Note 2): The minimum Slew Rate limit (30mV/ns) applies only to the 400-790mV region of falling edges.

355 Rising edges:

- (Note 8): The maximum Slew Rate limits are applicable across the entire signal transition/edge.
- (Note 9): The minimum Slew Rate limit (25mV/ns) applies only to the 400-550mV region of rising edges.
- (Note 11): For the 550-790mV region of rising edges, the minimum slew rate limit is defined by the equation $25 - 0.0625 * (V_{O-INST} - 550)$.

361 Note also that this specification, as written, presents the same problem regarding C_{LOAD} as was observed for
362 Test 1.1.3 (see Test 1.1.3 Discussion), where it is difficult to present a precise C_{LOAD} value to the transmitter
363 under test, as the capacitance of the DUT's evaluation board is not known and may not be well controlled.
364 (Note this is even more critical in this test, as the slew rate specifications are defined for very specific
365 C_{LOAD} values.) Furthermore, even with very well-designed evaluation boards, C_{LOAD} values of 0pF and 5pF
366 are not realistically achievable for a practical test PCB.

367 Therefore, as was the case for Test 1.1.3, some compromise must be made in order to define a realistic and
368 practical conformance test. A summary of the methodology for this test is as follows:

- For the Maximum Slew Rate test, the measurement will be performed using the 50pF C_{LOAD} test fixture, and the results will be evaluated against the 70pF limit of 150mV/ns across the entire signal edge, for both rising and falling edges.
- For the Minimum Slew Rate test for falling edges, the measurement will be performed using the 50pF C_{LOAD} test fixture, and the results will be evaluated against the 25mV/ns limit across the voltage range of 400-790mV.
- For the Minimum Slew Rate test for rising edges, the measurement will be performed using the 50pF C_{LOAD} test fixture, and the results will be evaluated against the 25mV/ns limit across the voltage range of 400-550mV, and against the equation-based limit for the 550-790mV voltage range.

375 In this test, the three single-ended V_A , V_B , and V_C signals from the DUTs LP transmitter will be captured
376 using three channels of a real-time DSO. A 400MHz test filter will be applied (described below). The Slew
377 Rate will be computed and measured independently for each edge of the V_A , V_B , and V_C signals as
378 described above, using a 50mV vertical window. Note that this translates to the rising edge slew rate at time
379 (t) being calculated using a centered window around time (t), where the dv/dt is determined using the first
380 sample after time (t) that is greater than or equal to $v(t)+25mV$, and the last sample before time (t) that is
381 less than or equal to $v(t)-25mV$ (or with opposite slope for the case of a falling edge).

386 Once the Slew Rate data curve is computed for a single edge using the sliding window technique, the
387 maximum value across the entire edge will be recorded. This process is then repeated for all edges. The
388 results for all rising edges will then be averaged together to produce the final rising edge Maximum Slew
389 Rate result, and the results for all falling edges will then be averaged together to produce the final falling
390 edge Maximum Slew Rate result.

391 Note that this slew rate measurement is very sensitive to high-frequency noise (contributed primarily by the
392 DSO), which can translate to high-frequency deviations in the slew rate curve data. Because it is not
393 desirable to include these deviations in the measurement, it is advantageous to filter the source waveform
394 prior to performing the slew rate measurement, which will remove the high-frequency deviations. To
395 reduce the measurement noise, a 400-MHz, 4th-order Butterworth lowpass filter will be applied to the

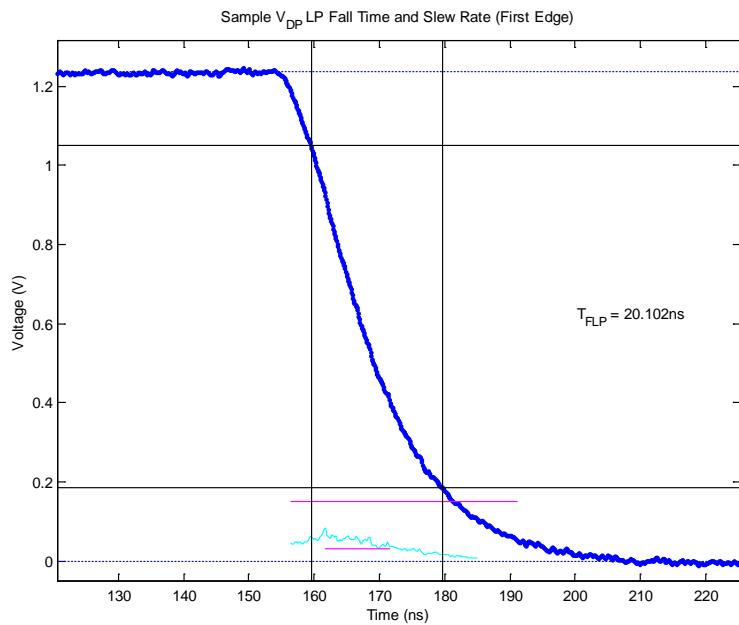
396 source waveform prior to performing the measurement. (Note that for simplicity, the test filter will be used
397 for all tests 1.1.x and 1.2.x, however the benefit will most impact the slew rate tests.) The 400MHz cutoff
398 value is chosen specifically to preserve as much of the desired signaling characteristics as possible (which
399 for a 20Mstate/sec signal should be well below 400MHz), and isolate the high-frequency noise. (Note this
400 is similar in concept to averaging the source waveform in order to reduce measurement noise, which is a
401 different but related technique). This cutoff value is high enough to result in minimal impact to the
402 measured rise time, while improving the slew rate result.

403 For the Minimum Slew Rate, three cases exist. For falling edges, the minimum slew rate value across the
404 400-790mV region of each edge will be recorded, and the results for each edge will then be averaged
405 together to produce the final falling edge Minimum Slew Rate result. For rising edges, the minimum slew
406 rate value across the 400-550mV region of each edge will be recorded, and the results for each edge will
407 then be averaged together to produce the final rising edge Minimum Slew Rate result.

408 For the Minimum Slew Rate across the 550-790mV region, a single minimum value cannot be used to
409 determine conformance, as the conformance limit is not a static value across the entire applicable range, but
410 rather consists of a curved, equation-based limit line (see Figure 1.1.5-6, below) which is inversely
411 proportional to the instantaneous V_A , V_B , and V_C voltage. (Thus the conformance limit line behaves more
412 like a mask.) To quantify the conformance relative to the limit line, the minimum margin between the
413 measured slew rate curve and the Minimum Slew Rate limit line will be calculated for each edge, where the
414 margin value at time (t) is the slew rate value at (t) minus the lower limit line value at (t) , and a negative
415 margin value is considered failing. The minimum margin with respect to the limit line will be recorded for
416 each edge, and the results for each edge will then be averaged together to produce the final rising edge
417 Minimum Slew Rate Margin result.

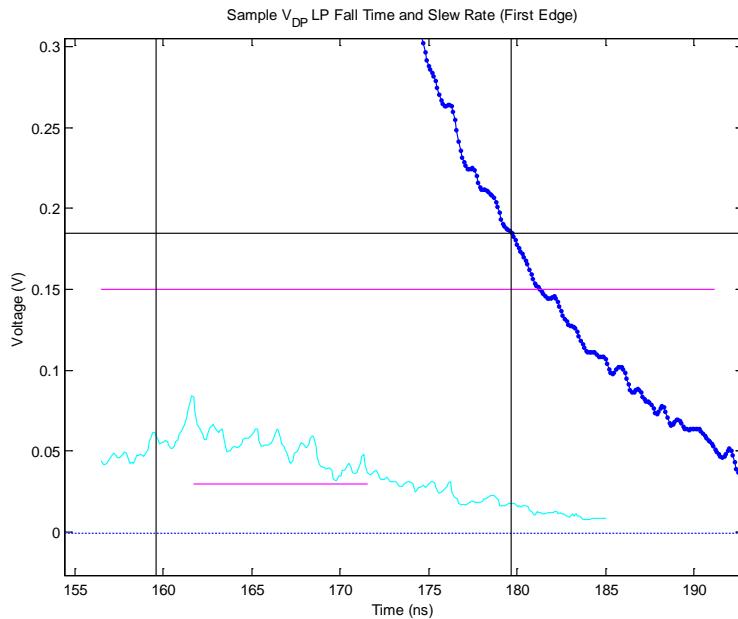
418 The five measurements above will be measured for the V_A , V_B , and V_C signals, and for all Lanes.

419 Note an example slew rate measurement is shown in the figures shown on the following pages. The first
420 figure (Figure 1.1.5-3) shows the entire LP edge, where the computed sliding-window slew rate curve is
421 shown in light blue. The Maximum (150mV/ns) and Minimum (25mV/ns) slew rate conformance limits are
422 shown over the horizontal ranges corresponding to the respective vertical ranges over which the limit
423 applies (i.e., the entire vertical region for the Max limit, and the 400-790mV region for the Min limit).
424 Figure 1.1.5-4 shows a zoomed-in view of the slew rate data and conformance limit lines. Figures 1.1.5-5
425 and 1.1.5-6 show the same concept, but for the rising edge case. (Note the curved Minimum limit in Figure
426 1.1.5-6.)



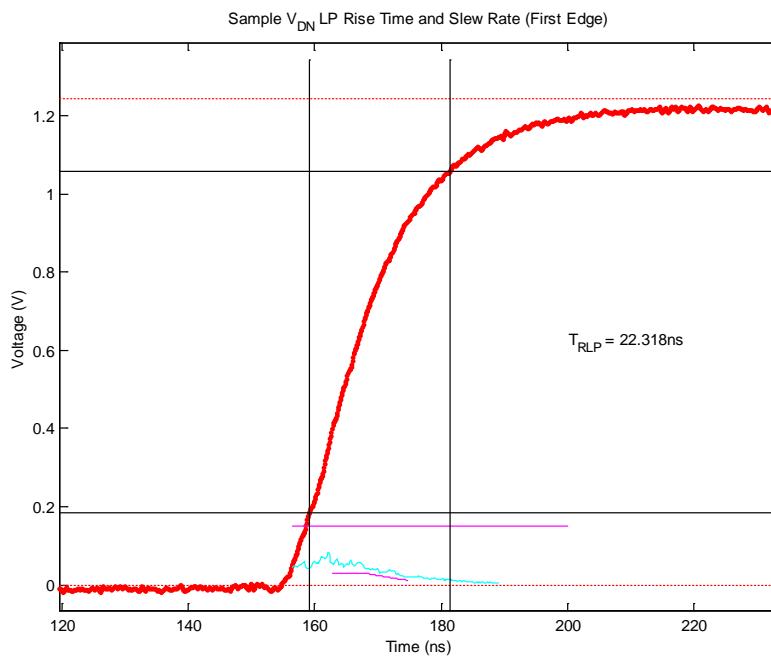
427

**Figure 1.1.5-3: Sample LP Falling Edge Slew Rate Measurement
(Slew rate data shown in light blue)**



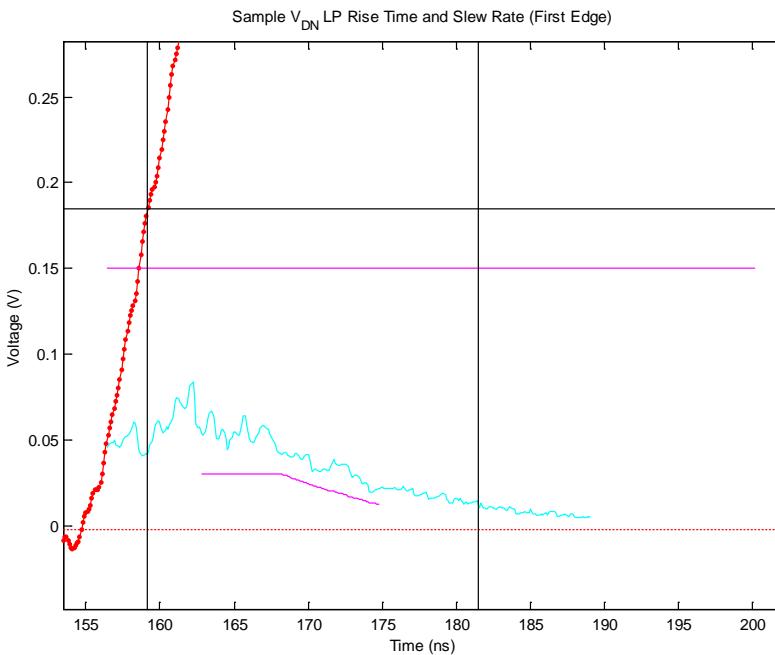
428

**Figure 1.1.5-4: Zoomed-in View of Slew Rate Data
(Slew Rate falling edge Max/Min limits shown in pink)**



429

**Figure 1.1.5-5: Sample LP Rising Edge Slew Rate Measurement
(Slew rate data shown in light blue)**



**Figure 1.1.5-6: Zoomed-in View of Slew Rate Data
(Slew Rate rising edge Max/Min limits shown in pink)**

431 **Test Setup**
432 See Annex B.1.1.

433 Test Procedure

- 434 • Connect the DUT's Lane 0 to the Test Setup, using the 50pF C_{LOAD} test fixture.
- 435 • Create a condition that causes the DUT to source a ULPS Entry sequence on Lane 0.
- 436 • Capture the LP signaling sequence using the DSO.
- 437 • Using post-processing methods, compute the following for the V_{DP} and V_{DN} falling edges:
 - 438 • Compute the final averaged Maximum $\delta V/\delta t_{SR}$ result (over the entire vertical edge region).
 - 439 • Compute the final averaged Minimum $\delta V/\delta t_{SR}$ result (400-790mV region).
- 440 • Using post-processing methods, compute the following for the V_{DP} and V_{DN} rising edges:
 - 441 • Compute the final averaged Maximum $\delta V/\delta t_{SR}$ result (over the entire vertical edge region).
 - 442 • Compute the final averaged Minimum $\delta V/\delta t_{SR}$ result (400-550mV region)
 - 443 • Compute the final averaged Minimum $\delta V/\delta t_{SR}$ Margin result (550-790mV region).

444 Repeat all above steps for all other Lanes (if the DUT implements multiple Lanes).

445 Observable Results

446 Falling edges:

- 447 For the 50pF C_{LOAD} , for V_A , V_B , and V_C , and for all Lanes:
- 448 • Verify that the Maximum $\delta V/\delta t_{SR}$ is less than 150mV/ns across the entire edge.
 - 449 • Verify that the Minimum $\delta V/\delta t_{SR}$ is greater than 25mV/ns across the 400-790mV region.

450 Rising edges:

- 451 For the 50pF C_{LOAD} , for V_A , V_B , and V_C , and for all Lanes:
- 452 • Verify that the Maximum $\delta V/\delta t_{SR}$ is less than 150mV/ns across the entire edge.
 - 453 • Verify that the Minimum $\delta V/\delta t_{SR}$ is greater than 25mV/ns across the 400-550mV region.
 - 454 • Verify that the Minimum $\delta V/\delta t_{SR}$ Margin is greater than 0mV/ns across the 550-790mV region.

455 Possible Problems

456 None.

Test 1.1.6 LP-TX Pulse Width of Exclusive-OR Clock ($T_{LP-PULSE-TX}$)

Purpose

To verify that the pulse width ($T_{LP-PULSE-TX}$) of the DUT's LP transmitter XOR Clock is within the conformance limits.

References

- [1] C-PHY Specification, Figure 28
- [2] Ibid, Table 25
- [3] Ibid, Section 9.1.2

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for $T_{LP-PULSE-TX}$, which is the pulse width of the DUT LP-TX XOR clock. A graphical example of the XOR operation that creates the LP clock, reproduced from the specification, is shown below.

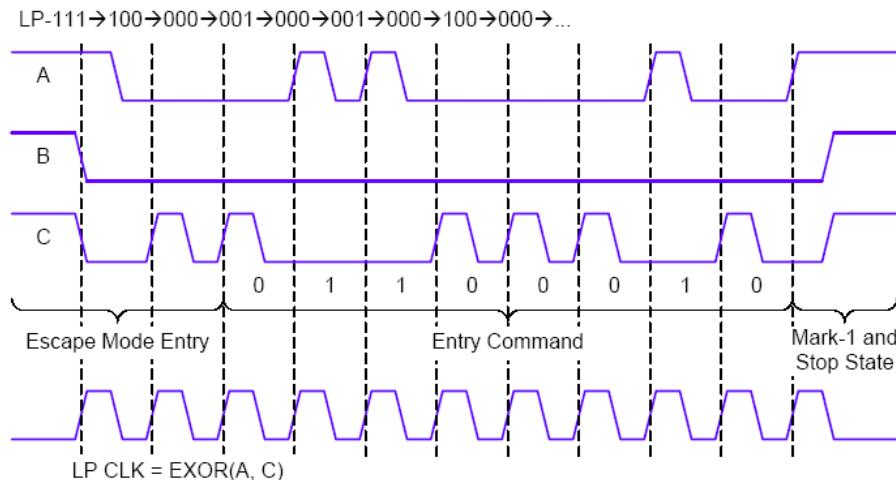


Figure 28 Trigger-Reset Command in Escape Mode

Figure 1.1.6-1: LP XOR Clock Generation from V_A and V_C

The specification separates the $T_{LP-PULSE-TX}$ specification into two parts[2]:

$t_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40			ns	4
	All other pulses		20			ns	4

Figure 1.1.6-2: LP XOR Clock Pulse Conformance Requirements

These requirements are summarized as follows:

- The first LP XOR clock pulse after a Stop state, *and* the last LP XOR clock pulse before a Stop state must be wider than 40ns.
- All other LP XOR clock pulses must be wider than 20ns.

The specification also provides specifications regarding how the XOR Clock is to be generated, specifically[3],

- 1094 Using a common trip-level in the range $[V_{IL,MAX} + V_{OL,MIN}, V_{IH,MIN} + V_{OL,MAX}]$, the exclusive-OR clock shall
 1095 not contain pulses shorter than $t_{LP-PULSE-TX}$.

Figure 1.1.6-3: $t_{LP-PULSE-TX}$ Specification Definition

The provision of a range for the common trip level implies that the measurement should be performed multiple times, using various trip levels spanning the entire specified range. This can potentially result in non-conformant pulse widths at certain threshold levels, particularly in cases where the DUT may have oddly shaped and/or asymmetric signal edges, or particularly slow rise times. Using post processing on the captured waveform data, it is possible to perform measurements using any number and range of threshold levels. For the purposes of this test, two trip-level cases will be performed, representing the maximum and minimum allowed trip levels.

Note that $V_{IL,MAX} = 550\text{mV}$, $V_{OL,MIN} = -50\text{mV}$, $V_{IH,MIN} = 740\text{mV}$, and $V_{OL,MAX} = 50\text{mV}$. Thus, the minimum trip level becomes $550 - 50 = 500\text{mV}$, and the maximum trip level is $740 + 50 = 790\text{mV}$.

In this test, the two single-ended V_A and V_C signals from the DUTs Data Lane LP transmitter will be captured using two channels of a real-time DSO. Using post-processing methods, the V_A and V_C waveform samples will be 2-level quantized (i.e., rounded up/down to either 0 or 1) according to the specified trip-level threshold voltage. The resulting binary arrays will then be XOR'ed to create the sampled LP Clock, on which the $t_{LP-PULSE-TX}$ measurement will then be performed. Pulse width values (based on the midpoint crossing times of the generated XOR signal) for all XOR Clock pulses will be recorded and verified against their respective conformance limits. (Note that for the purposes of this test, a ‘pulse’ is defined as a positive pulse, i.e., rising edge to falling edge.)

Also, to reduce measurement noise, a 400-MHz, 4th-order Butterworth lowpass test filter will be applied to the source waveforms prior to performing the measurement. (See Test 1.1.5 Discussion for details.)

This entire process will be performed twice, once for the maximum trip-level threshold voltage (790mV) and once for the minimum trip-level threshold voltage (500mV). Also note that while the specification does not indicate the C_{LOAD} value used for this measurement, the test will be performed with the 50pF C_{LOAD} test fixture, and will be measured for all Lanes.

For all cases, the first XOR clock pulse after a Stop state must be greater than 40ns in order to be considered conformant, and the minimum of all other XOR clock pulses must be greater than 20ns in order to be considered conformant[2].

(*Note that while the specification includes a provision for the last XOR clock pulse before a stop state being greater than 40ns, this requirement only applies to LP Escape Mode sequences that end with a Stop state (e.g., LPDT packets or Triggers on Data Lane 0 for DSI devices.) Because this test uses a ULPS Entry*

512 sequence (as this is the only LP Escape Mode sequence available on all Lanes), the 40ns requirement does
513 not apply, as the ULPS sequence ends with LP-00, not a Stop state. Therefore, this requirement cannot be
514 verified using this procedure, and is omitted from the Observable Results.)

515 **Test Setup**

516 See Annex B.1.1.

517 **Test Procedure**

- 518 • Connect the DUT's Lane 0 to the Test Setup, using the 50pF C_{LOAD} test fixture.
- 519 • Create a condition that causes the DUT to source a ULPS Entry sequence on Lane 0.
- 520 • Capture the LP signaling sequence using the DSO.
- 521 • Using post-processing methods as described above, compute the LP XOR Clock and measure the
522 two T_{LP-PULSE-TX} values (first, and min of all others) using the maximum trip-level threshold
523 voltage of 790mV.
- 524 • Using post-processing methods as described above, compute the LP XOR Clock and measure the
525 two T_{LP-PULSE-TX} values (first, and min of all others) using the minimum trip-level threshold
526 voltage of 500mV.
- 527 • Repeat the previous steps for Data Lanes 1, 2, and 3 (if the DUT implements multiple Data
528 Lanes).

529 **Observable Results**

530 For both trip-level voltages, and for all Lanes:

- 531 • Verify that the first LP XOR Clock pulse after the initial Stop state is greater than 40ns.
- 532 • Verify that the minimum of all other clock pulses is greater than 20ns.

533 **Possible Problems**

534 When the XOR Clock is computed from the 2-level quantized LP V_A and V_C waveforms, glitches can
535 sometimes result if excessive noise is present on the input waveforms (either DSO sampling noise, or noise
536 from the DUT itself, which can cause multiple short-term excursions across the trip-level threshold voltage,
537 at the threshold crossing point). Care should be taken to ensure that the input waveforms are as smooth and
538 free from noise as possible, however any post-processing algorithms should ensure that any glitches caused
539 by such artifacts are not erroneously counted as XOR Clock pulses.

Test 1.1.7 LP-TX Period of Exclusive-OR Clock ($T_{LP-PER-TX}$)

Purpose

To verify that the period ($T_{LP-PER-TX}$) of the DUT's LP transmitter XOR Clock is within the conformance limits.

References

- [1] C-PHY Specification, Figure 28
- [2] Ibid, Table 25

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for $T_{LP-PER-TX}$, which is the Period of the DUT LP-TX XOR clock. A graphical representation of the XOR operation that creates the LP clock, reproduced from the specification, is shown below[1].

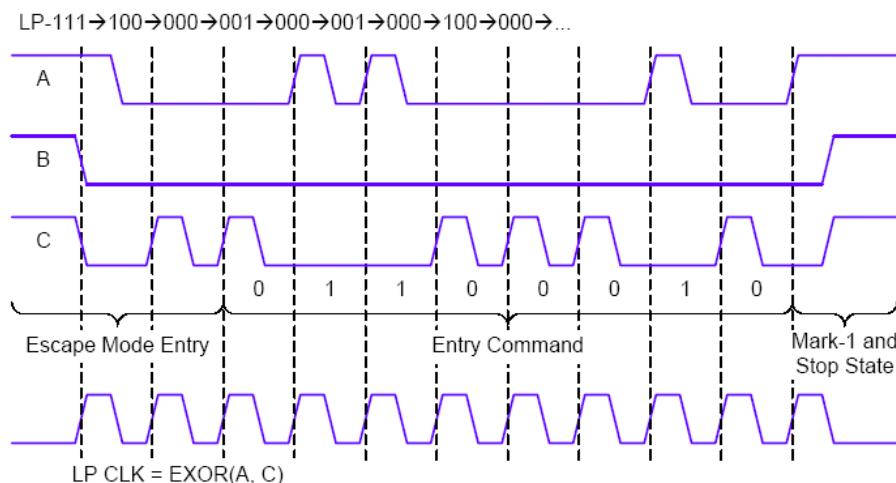


Figure 28 Trigger-Reset Command in Escape Mode

Figure 1.1.7-1: LP XOR Clock Extraction from V_A and V_C

Note that $T_{LP-PER-TX}$ is only mentioned in Table 25 of the specification (shown below), and does not have an explicit text description/reference. The definition also does not explicitly state the trip levels and/or C_{LOAD} values for which the requirement applies. Therefore, values must be chosen for the purpose of conformance testing. For the sake of consistency with the previous test (Test 1.1.6, XOR Clock pulse width), the 500mV and 790mV trip levels will be used, and the measurement will be performed with the 50pF C_{LOAD} test fixture.

T _{LP-PER-TX}	Period of the LP exclusive-OR clock	90			ns	
------------------------	-------------------------------------	----	--	--	----	--

Figure 1.1.7-2: T_{LP-PER-TX} Conformance Requirements

In this test, the LP Clock will be captured and computed using the same process described in the previous test (see Test 1.1.6, Discussion). However, rather than measuring the rising-to-falling and falling-to-rising pulse widths, this test will measure T_{LP-PER-TX} as the rising-to-rising and falling-to-falling periods of the XOR clock. The reported T_{LP-PER-TX} result will be minimum of all measured period values, and will be reported separately for the rising-to-rising and falling-to-falling period cases. The measurement will be performed for both trip-level voltages, with the 50pF C_{LOAD} test fixture and 400MHz test filter, and for all Data Lanes.

For all cases, the value of T_{LP-PER-TX} must be greater than 90ns in order to be considered conformant[2].

Test Setup

See Annex B.1.1.

Test Procedure

- Connect the DUT's Lane 0 to the Test Setup, using the 50pF C_{LOAD} test fixture.
- Create a condition that causes the DUT to source a ULPS Entry sequence on Lane 0.
- Capture the LP signaling sequence using the DSO.
- Using post-processing methods as described above, compute the LP XOR Clock and measure the T_{LP-PER-TX} rising-to-rising and falling-to-falling edge periods using the maximum trip-level threshold of 790mV.
- Using post-processing methods as described above, compute the LP XOR Clock and measure the T_{LP-PER-TX} rising-to-rising and falling-to-falling edge periods using the minimum trip-level threshold of 500mV.
- Repeat the previous steps for all other Lanes (if the DUT implements multiple Lanes).

Observable Results

For both trip-level voltages, and for all Lanes:

- Verify that the minimum T_{LP-PER-TX} rising-edge-to-rising-edge period is greater than 90ns.
- Verify that the minimum T_{LP-PER-TX} falling-edge-to-falling-edge period is greater than 90ns.

Possible Problems

See Possible Problems comments for Test 1.1.6. The same applies to this test.

Group 2 HS-TX Burst Signaling Requirements

Overview

This group of tests verifies various TX requirements pertaining to HS burst signaling. The structure of this group is intended to facilitate the execution a set of several HS-TX measurements on a single captured HS burst waveform, which includes the LP exit/entry sequences occurring before and after the burst sequence.

This test Group is applicable to Master devices only. (It is considered Not Applicable for Slave devices.).

Status

The test names, Discussion sections, and Procedures are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on at least one device. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

Test 1.2.1 T_{LPX} Duration

Purpose

To verify that the duration (T_{LPX}) of the final LP-001 state immediately before HS transmission is greater than the minimum conformant value.

References

- [1] C-PHY Specification, Section 6.2
- [2] Ibid, Table 14
- [3] Ibid, Figure 23

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

The C-PHY Low-Power (LP) mode of operation is comprised of state transitions occurring at some implementation-specific rate less than 20M transitions/sec. Note that these state transitions may have different meanings depending on the context (Control, Escape, or LPDT mode), and do not equate to ‘bits’ on the wire.

The specification states[1],

553 All LP state periods shall be at least t_{LPX} in duration. State transitions shall be smooth and exclude glitch

Figure 1.2.1-1: T_{LPX} Specification Definition

Also, the specification further defines the minimum value of T_{LPX} to be 50ns[2].

In this test, the focus is specifically the duration of the last LP-001 state that occurs immediately before an HS burst sequence. The state will be measured starting at the time where the V_A falling edge crosses below the maximum low-level LP threshold, $V_{IL,MAX}$ (550mV), and ending at the time where the V_C falling edge crosses below the same $V_{IL,MAX}$ threshold. A picture of the T_{LPX} interval is shown in the figure below[3].

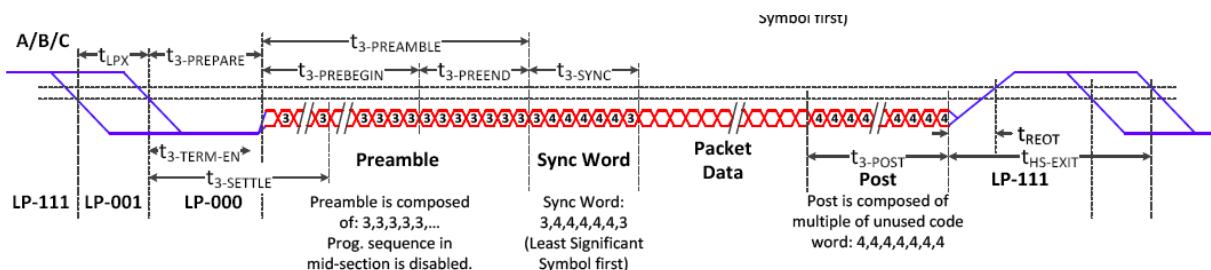


Figure 23 High-Speed Data Transmission in Burst

Figure 1.2.1-2: Data Lane T_{LPX} Interval

Test Setup

See Annex B.1.2.

626 Test Procedure

- 627 • Connect the DUT's Lane 0 to the Reference Termination Board (RTB).
- 628 • Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
- 629 • Capture the HS burst sequence using the DSO.
- 630 • Using post-processing methods, compute the V_A and V_C $V_{IL,MAX}$ (550mV) crossing times.
- 631 • Measure the T_{LPX} value as the difference between the two crossing times.
- 632 • Repeat the previous steps for all other Lanes (if DUT implements multiple Lanes).

633 Observable Results

634 For all Lanes:

- 635 • Verify that T_{LPX} is greater than or equal to 50ns.

636 Possible Problems

637 None.

Test 1.2.2 T_{3-PREPARE} Duration

Purpose

To verify that the duration of the final LP-000 state immediately before HS transmission (T_{3-PREPARE}) is within the conformance limits.

References

- [1] C-PHY Specification, Figure 23
- [2] Ibid, Table 18

Resource Requirements

See Annex A.1.

Last Technical Modification

April 14, 2015

Discussion

As part of the process for switching the Data Lane into HS mode, the C-PHY Specification provides a specification for the minimum time interval that a device must transmit the final LP-000 state before enabling HS mode. This interval is defined as T_{3-PREPARE}, and is shown in the figure below[1].

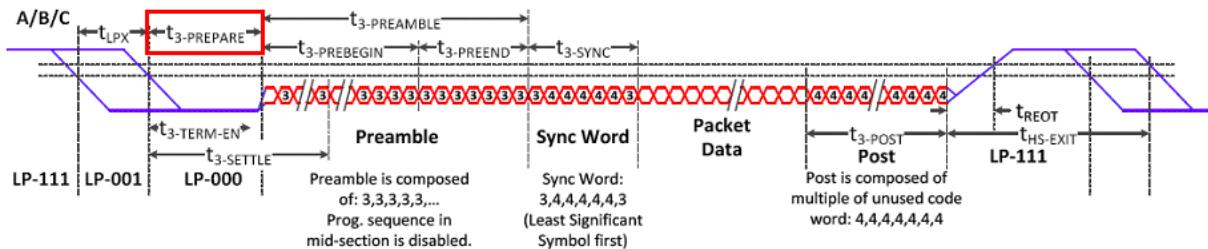


Figure 23 High-Speed Data Transmission in Burst

Figure 1.2.2-1: T_{3-PREPARE} Interval

The interval is formally described in the table below[2].

Table 18 Global Operation Timing Parameters

Parameter	Description	Min	Max	Unit	Notes
t _{3-PREPARE}	Time that the transmitter drives the 3-wire LP-000 line state immediately before the HS_+x line state starting the HS transmission.	38	95	ns	2

Figure 1.2.2-2: T_{3-PREPARE} Interval Definition and Conformance Range

In this test, the DUT will be configured to source an HS burst sequence, starting and ending with LP-111 states. The T_{3-PREPARE} interval begins at the time where the Data Lane V_C signal crosses below V_{IL,MAX} (550mV), and ends at the beginning of the first HS state, at the point where the differential waveform crosses above the minimum valid HS-0 differential threshold level (+/-40mV).

The measured duration of T_{3-PREPARE} should be between 38 and 95 ns in order to be considered conformant[2].

661 Test Setup

662 See Annex B.1.2.

663 Test Procedure

- 664 • Connect the DUT's Lane 0 to the Reference Termination Board (RTB).
- 665 • Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
- 666 • Capture the HS burst sequence using the DSO.
- 667 • Using post-processing methods, compute $T_{3\text{-PREPARE}}$ as described above.
- 668 • Repeat the previous steps for all other Lanes (if DUT implements multiple Lanes).

669 Observable Results

670 For all Lanes:

- 671 • Verify that $T_{3\text{-PREPARE}}$ is between 38 and 95 ns.

672 Possible Problems

673 None.

Test 1.2.3 T₃-PREBEGIN Duration

Purpose

To verify that the time of T₃-PREBEGIN is within the conformance limits.

References

[1] C-PHY Specification, Figure 23

[2] Ibid, Section 6.9

Resource Requirements

See Annex A.1.

Last Technical Modification

April 14, 2015

Discussion

As part of the process for switching the Lane into HS mode, the C-PHY Specification provides a specification for the duration that a device must drive the initial preamble prior to starting HS data transmission. This interval is defined as T₃-PREBEGIN, and is shown in the figure below[1].

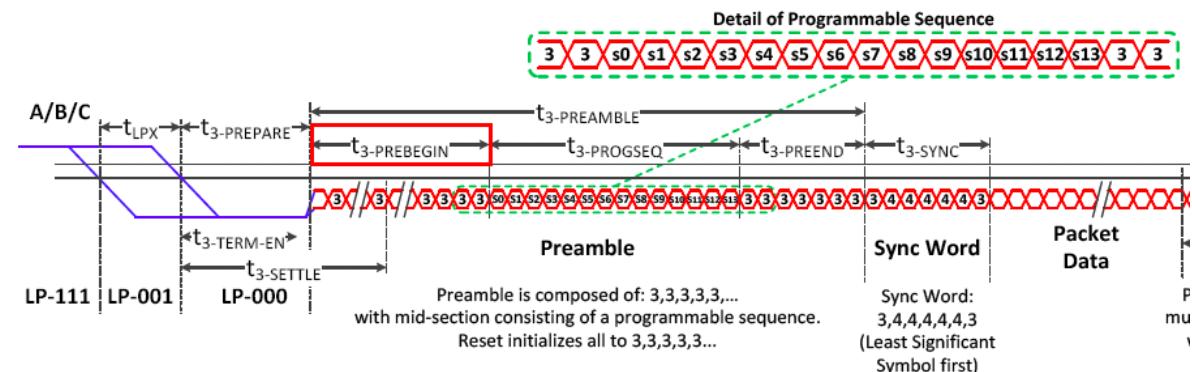


Figure 1.2.3-1: T₃-PREBEGIN Interval

In this test, the DUT will be configured to source an HS burst sequence, starting and ending with LP-111 states. The T₃-PREBEGIN interval begins at the first differential state (where the differential signal crosses +/- 40mV), and ends at the first bit of the T₃-PROGSEQ sequence. (Note that this measurement requires the optional T₃-PROGSEQ to be enabled, in order to see the endpoint of T₃-PREBEGIN).

The specification defines the length of T₃-PREBEGIN as shown below[2].

755 t₃-PREBEGIN should be adjustable from 7 UI minimum to 448 UI maximum in increments of 7 UI.

Figure 1.2.3-2: T₃-PREBEGIN Conformance Requirements

Note that measurement of these requirements can be difficult, due to the fact that when the transmitter begins transmitting HS symbols, the first symbol or symbols may be malformed, due to startup transients and other impairments. Therefore it may not be possible to accurately measure or count all HS states, in which case the measured number of states may not be an integer multiple of seven. Because of this, the ‘multiple of seven’ requirement will not be enforced for this test.

699 The measured duration of $T_{3-PREBEGIN}$ should be between 7 and 448 UI (where UI is the nominal HS Unit
700 Interval for the DUT, see Test 1.2.17) in order to be considered conformant[2].

701 **Test Setup**

702 See Annex B.1.2.

703 **Test Procedure**

- 704 • Connect the DUT's Lane 0 to the Reference Termination Board (RTB).
705 • Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
706 • Capture the HS burst sequence using the DSO.
707 • Using post-processing methods, measure $T_{3-PREBEGIN}$, as described above.
708 • Repeat the previous steps for all other Lanes (if DUT implements multiple Lanes).

709 **Observable Results**

710 For all Lanes:

- 711 • Verify that $T_{3-PREBEGIN}$ is between 7 and 448 UI.

712 **Possible Problems**

713 This test requires the $T_{3-PROGSEQ}$ to be enabled. If it is not enabled, this measurement will not be possible.

Test 1.2.4 T₃-PROGSEQ Duration

Purpose

To verify that the length of T₃-PROGSEQ is within the conformance limits.

References

- [1] C-PHY Specification, Figure 23
- [2] Ibid, Section 6.4.4
- [3] Ibid, Section 6.9

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

As part of the process for switching the Lane into HS mode, the C-PHY Specification provides a specification for the duration that a device must drive the programmable preamble sequence prior to starting HS data transmission. This interval is defined as T₃-PROGSEQ, and is shown in the figure below[1].

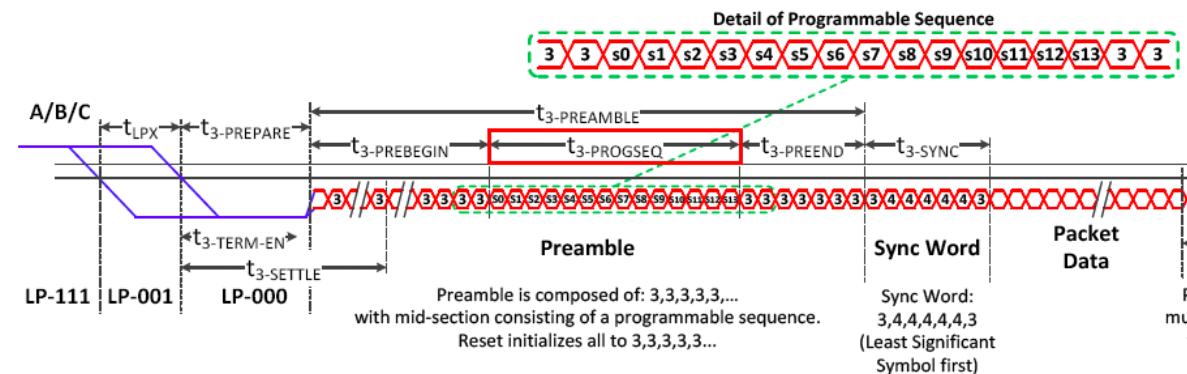


Figure 1.2.4-1: T₃-PROGSEQ Interval

In this test, the DUT will be configured to source an HS burst sequence, starting and ending with LP-111 states. The T₃-PROGSEQ interval begins at the end of T₃-PREBEGIN, and ends at the first bit of the T₃-PREEND sequence. (Note that this measurement requires the optional T₃-PROGSEQ to be enabled, in order to measure it. If it is not enabled, this test is considered Not Applicable.)

The specification describes the T₃-PROGSEQ as shown below[2],[3].

- 608 The master may output a programmable sequence during t₃-PROGSEQ of the preamble, if it is enabled using a
609 programmable sequence enable bit such as the MSB of the control register described in section 12.5.3. The
610 symbol values transmitted in the programmable sequence, or whether the programmable sequence is used at
611 all, is a choice of the system designer.

Figure 1.2.4-2: T₃-PROGSEQ Definition

	$t_{3\text{-SETTLE}} > t_{3\text{-PREPARE}}$	$t_{3\text{-PROGSEQ}} = 14 \text{ UI or } 0 \text{ UI}$
	$t_{3\text{-SETTLE}} < t_{3\text{-PREPARE}} + t_{3\text{-PREAMBLE}}$	$t_{3\text{-PREEND}} = 7 \text{ UI}$
735	$t_{3\text{-PREAMBLE}} = t_{3\text{-PREBEGIN}} + t_{3\text{-PROGSEQ}} + t_{3\text{-PREEND}}$	$t_{3\text{-SYNC}} = 7 \text{ UI}$

Figure 1.2.4-3: $T_{3\text{-PROGSEQ}}$ Length Requirements

736 The measured duration of $T_{3\text{-PROGSEQ}}$, if enabled, should be 14 UI (where UI is the nominal HS Unit Interval
737 for the DUT, see Test 1.2.17) in order to be considered conformant[3].

738 **Test Setup**

739 See Annex B.1.2.

740 **Test Procedure**

- 741 • Connect the DUT's Lane 0 to the Reference Termination Board (RTB).
- 742 • Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
- 743 • Capture the HS burst sequence using the DSO.
- 744 • Using post-processing methods, measure $T_{3\text{-PROGSEQ}}$, as described above.
- 745 • Repeat the previous steps for all other Lanes (if DUT implements multiple Lanes).

746 **Observable Results**

747 For all Lanes:

- 748 • Verify that $T_{3\text{-PROGSEQ}}$ is 14 UI.

749 **Possible Problems**

750 This test requires the $T_{3\text{-PROGSEQ}}$ to be enabled. If it is not enabled, this measurement will not be possible.

Test 1.2.5 T₃-PREEND Duration

Purpose

To verify that the duration of T₃-PREEND is correct.

References

[1] C-PHY Specification, Figure 23

[2] Ibid, Section 6.9

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

As part of the process for switching the Lane into HS mode, the C-PHY Specification provides a specification for the minimum duration that a device must drive the final preamble prior to starting HS data transmission. This interval is defined as T₃-PREEND, and is shown in the figure below[1].

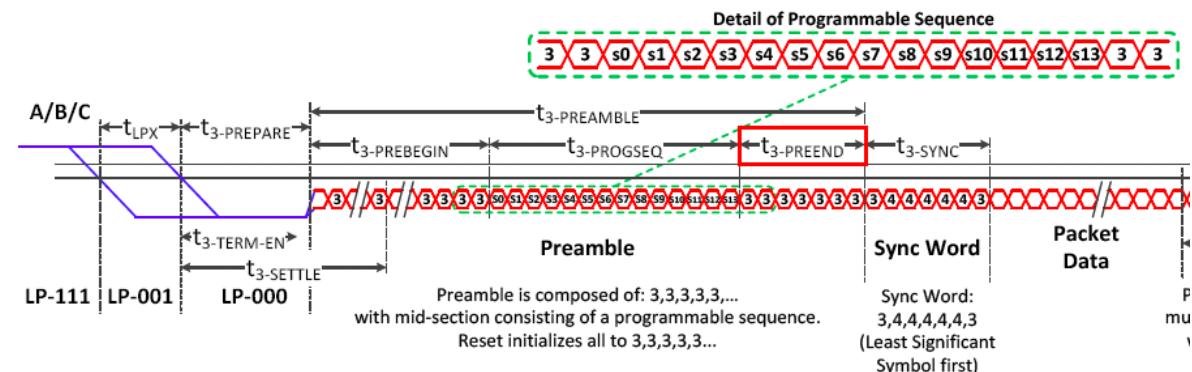


Figure 1.2.5-1: T₃-PREEND Interval

In this test, the DUT will be configured to source an HS burst sequence, starting and ending with LP-111 states. The T₃-PREEND interval begins at the end of T₃-PROGSEQ, and ends at the first bit of the T₃-SYNC sequence. (Note that this measurement requires the optional T₃-PROGSEQ to be enabled, in order to see the start point of T₃-PREEND).

The specification defines the length of T₃-PREEND as shown below[2].

- 612 Figure 23 shows examples of the preamble with and without the programmable sequence. Seven symbols of
613 value "3" are sent during t₃-PREEND just prior to sending the Sync Word.

Figure 1.2.5-2: T₃-PREEND Definition and Conformance Requirements

The measured duration of T₃-PREEND should be 7 UI (where UI is the nominal HS Unit Interval for the DUT, see Test 1.2.17), in order to be considered conformant[2].

773 Test Setup

774 See Annex B.1.2.

775 Test Procedure

- 776 • Connect the DUT's Lane 0 to the Reference Termination Board (RTB).
- 777 • Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
- 778 • Capture the HS burst sequence using the DSO.
- 779 • Using post-processing methods, measure $T_{3\text{-PREEND}}$, as described above.
- 780 • Repeat the previous steps for all other Lanes (if DUT implements multiple Lanes).

781 Observable Results

782 For all Lanes:

- 783 • Verify that $T_{3\text{-PREEND}}$ is 7 UI.

784 Possible Problems

785 This test requires the $T_{3\text{-PROGSEQ}}$ to be enabled. If it is not enabled, this measurement will not be possible.

Test 1.2.6 T₃-SYNC Duration

Purpose

To verify that the duration of T₃-SYNC is correct.

References

[1] C-PHY Specification, Figure 23

[2] Ibid, Section 6.9

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

As part of the process for switching the Lane into HS mode, the C-PHY Specification provides a specification for the minimum duration that a device must drive the Sync sequence prior to starting HS data transmission. This interval is defined as T₃-SYNC, and is shown in the figure below[1].

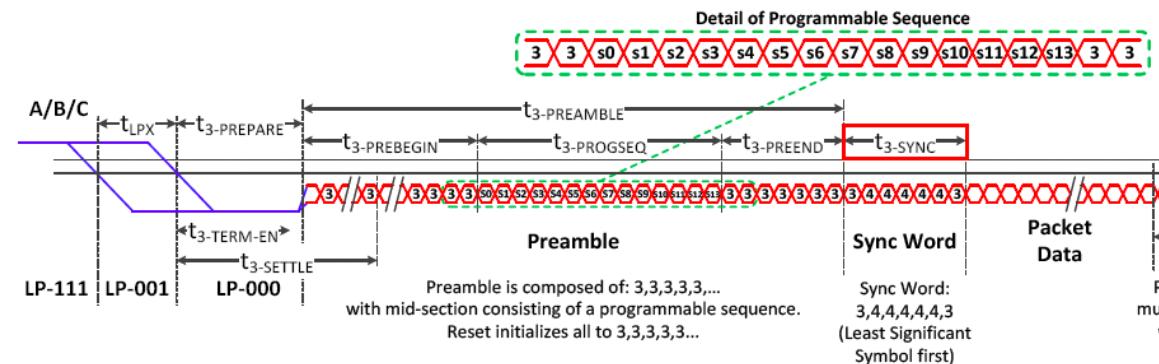


Figure 1.2.6-1: T₃-SYNC Interval

In this test, the DUT will be configured to source an HS burst sequence, starting and ending with LP-111 states. The T₃-SYNC interval begins at the end of T₃-PREEND, and ends at the first bit of the packet data.

The specification defines the length of T₃-SYNC as shown below[2][3].

- 614 The Sync Word precisely identifies the beginning of the Packet Data and also identifies the timing alignment
- 615 of word boundaries in the Packet Data. The Sync Word contains a sequence of five “4” symbols which does
- 616 not occur in any sequence of symbols generated by the Mapper. The Sync Word may also be transmitted later
- 617 in the burst to mark the beginning of redundant Packet Headers transmitted by the upper layer protocol.

Figure 1.2.6-2: T₃-SYNC Definition

$$\begin{aligned} t_{3\text{-SETTLE}} &> t_{3\text{-PREPARE}} \\ t_{3\text{-SETTLE}} &< t_{3\text{-PREPARE}} + t_{3\text{-PREAMBLE}} \\ t_{3\text{-PREAMBLE}} &= t_{3\text{-PREBEGIN}} + t_{3\text{-PROGSEQ}} + t_{3\text{-PREEND}} \end{aligned}$$

$$\begin{aligned} t_{3\text{-PROGSEQ}} &= 14 \text{ UI or } 0 \text{ UI} \\ t_{3\text{-PREEND}} &= 7 \text{ UI} \\ t_{3\text{-SYNC}} &= 7 \text{ UI} \end{aligned}$$

Figure 1.2.6-3: T₃-SYNC Length Requirements

805 The measured duration of T_{3-SYNC} should be 7 UI (where UI is the nominal HS Unit Interval for the DUT,
806 see Test 1.2.17), and should contain the symbol sequence, ‘3,4,4,4,4,4,3’ in order to be considered
807 conformant[2].

808 **Test Setup**

809 See Annex B.1.2.

810 **Test Procedure**

- 811 • Connect the DUT’s Lane 0 to the Reference Termination Board (RTB).
- 812 • Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
- 813 • Capture the HS burst sequence using the DSO.
- 814 • Using post-processing methods, measure T_{3-SYNC} , as described above.
- 815 • Using post-processing methods, verify the symbol sequence of T_{3-SYNC} .
- 816 • Repeat the previous steps for all other Lanes (if DUT implements multiple Lanes).

817 **Observable Results**

818 For all Lanes:

- 819 • Verify that T_{3-SYNC} is 7 UI.
- 820 • Verify that T_{3-SYNC} contains the symbol sequence, ‘3,4,4,4,4,4,3’.

821 **Possible Problems**

822 This test requires the $T_{3-PROGSEQ}$ to be enabled. If it is not enabled, this measurement will not be possible.

Test 1.2.7 HS-TX Differential Voltages (V_{OD-AB} , V_{OD-BC} , V_{OD-CA})

Purpose

To verify that the Differential Voltages (V_{OD-AB} , V_{OD-BC} , V_{OD-CA}) of the DUT HS transmitter are within the conformance limits.

References

- [1] C-PHY Specification, Section 9.1.1
- [2] Ibid, Table 22
- [3] Ibid, Figure 41

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for V_{OD-AB} , V_{OD-BC} , and V_{OD-CA} , which are a device's HS-TX Differential Voltage levels for the AB, BC, and CA pairs, respectively.

The specification states[1],

1009 The single-ended output voltages are defined V_A , V_B and V_C at the A, B and C pins, respectively. The
 1010 differential output voltages V_{OD_AB} , V_{OD_BC} and V_{OD_CA} are defined as the difference of the voltages: V_A
 1011 minus V_B , V_B minus V_C , and V_C minus V_A , respectively.

$$1012 \quad V_{OD_AB} = V_A - V_B; V_{OD_BC} = V_B - V_C; V_{OD_CA} = V_C - V_A;$$

Figure 1.2.7-1: V_{OD} Specification Definition

840 The specification also provides conformance limits for V_{OD} , for both the Strong and Weak states[2].

Table 22 HS Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$ V_{OD} $ strong	HS transmit differential voltage of the differential strong one and strong zero specified in Table 21.			300	mV	1
$ V_{OD} $ weak	HS transmit differential voltage of the differential weak one and weak zero specified in Table 21.	97			mV	1

Note:

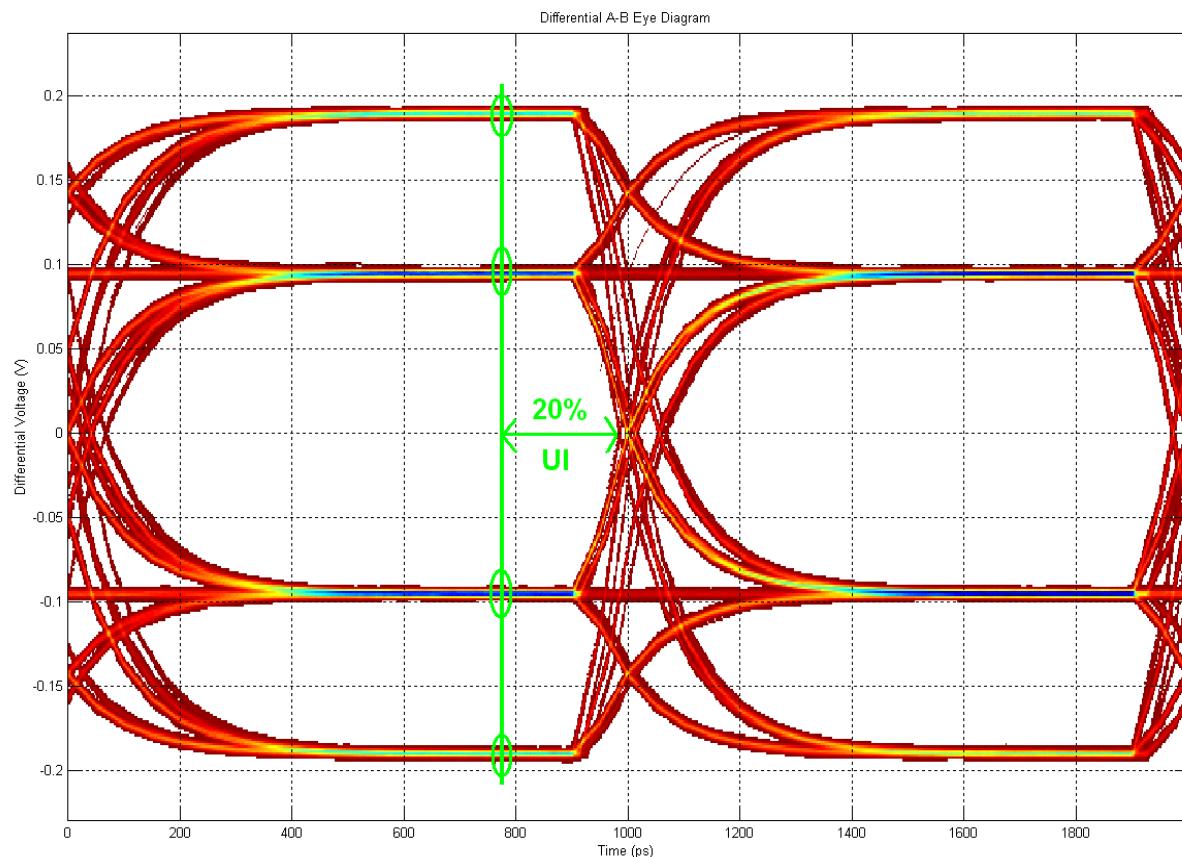
1. Value when driving into load impedance, Z_{ID} , equal to 100 ohms.

Figure 1.2.7-2: V_{OD} Specification Conformance Requirements

842 Note that this definition is potentially ambiguous in that, while it does define how the differential signal is
 843 computed, it does not specify how the differential voltage amplitude is measured for the purposes of

844 conformance testing. (Note that a diagram is presented in the specification[3], but this shows ‘ideal’
 845 signaling, which is not an accurate representation for measurement purposes.) Given that there are multiple
 846 possible ways to implement a differential voltage measurement (peak-to-peak, mode-to-mode, average over
 847 entire UI, average over 40%-60% UI, etc), a common method must be chosen for consistency. For the
 848 purposes of this Test Suite, an eye-based method is defined, where the reference V_{OD-AB} , V_{OD-BC} , and V_{OD-CA}
 849 levels are obtained from an eye diagram measured at a slow symbol rate, in order to measure the ‘DC’,
 850 or steady-state amplitude. (Note that the exact symbol rate is not specified, but should be slow enough to
 851 ensure that the eye diagram levels are fully settled towards the right side of the UI, as shown below.)

852 The methodology chosen for this test will measure the V_{OD} amplitudes based on an accumulated eye
 853 diagram for each of the three differential signals $V_{OD-AB} = V_A - V_B$, $V_{OD-BC} = V_B - V_C$, and $V_{OD-CA} = V_C - V_A$.
 854 Because the signal tends to settle more toward the right side of the UI, the amplitudes for the Strong 1,
 855 Weak 1, Weak 0, and Strong 0 will be measured at a point that is at a 20% UI width before the trigger point,
 856 where the waveform eye should be settled. (See figure below). Vertical histograms should be used to
 857 measure each amplitude, and the max and min values will be recorded for each histogram. (See second
 858 figure below.)



859

Figure 1.2.7-3: Sample V_{OD} Measurement at 20% UI Width

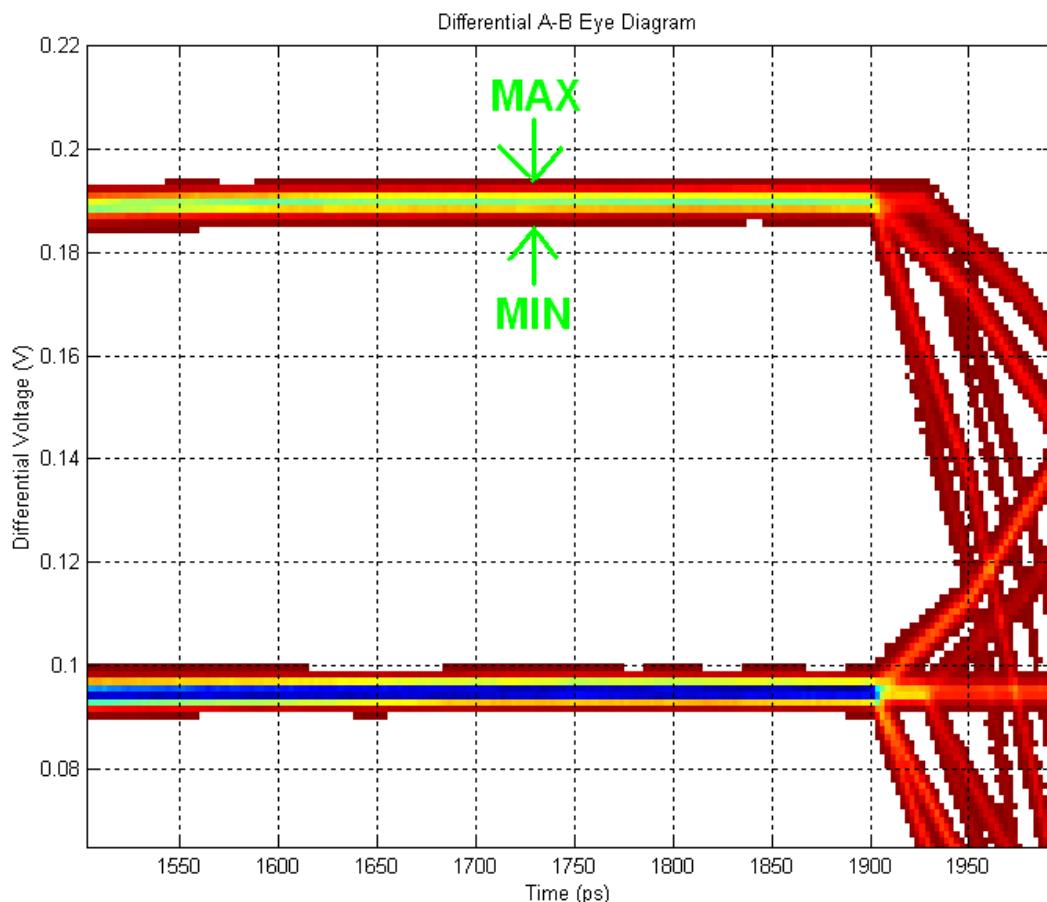


Figure 1.2.7-4: Zoomed-In View Showing Max/Min Measurements

861 The measurement will be performed for the $V_{OD-AB} = V_A - V_B$, $V_{OD-BC} = V_B - V_C$, and $V_{OD-CA} = V_C - V_A$ signals,
 862 and the Strong 1, Weak 1, Weak 0, and Strong 0 max and min values will be measured for each.

863 For all 3 differential pairs and all Lanes, the maximum Strong 1 V_{OD} value must be less than 300mV in
 864 order to be considered conformant. The minimum Weak 1 V_{OD} value must be greater than 97mV in order to
 865 be considered conformant. The maximum Weak 0 V_{OD} value must be less than -97mV in order to be
 866 considered conformant. The minimum Strong 0 V_{OD} value must be greater than -300mV in order to be
 867 considered conformant.

868 **Test Setup**

869 See Annex B.1.2.

870 **Test Procedure**

- 871 • Connect the DUT to the Reference Termination Board, such that Lane 0 is connected to $Z_{ID} = 100$
 ohms.
- 873 • Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
- 874 • Capture the HS burst sequence using the DSO.
- 875 • Using post-processing methods, measure the maximum and minimum V_{OD-AB} values for the
 876 Strong 1, Weak 1, Weak 0, and Strong 0 levels of the AB pair, as described above.
- 877 • Repeat the previous step for the BC and CA pairs.
- 878 • Repeat the previous steps for Lanes 1, 2, and 3 (if DUT implements multiple Lanes).

879 Observable Results

880 For all Lanes:

- 881 • Verify that $V_{OD-AB(MAX)}$ for the Strong 1 is less than 300mV.
- 882 • Verify that $V_{OD-AB(MIN)}$ for the Weak 1 is greater than 97mV.
- 883 • Verify that $V_{OD-AB(MAX)}$ for the Weak 0 is less than -97mV.
- 884 • Verify that $V_{OD-AB(MIN)}$ for the Strong 0 is greater than -300mV.

885

- 886 • Verify that $V_{OD-BC(MAX)}$ for the Strong 1 is less than 300mV.
- 887 • Verify that $V_{OD-BC(MIN)}$ for the Weak 1 is greater than 97mV.
- 888 • Verify that $V_{OD-BC(MAX)}$ for the Weak 0 is less than -97mV.
- 889 • Verify that $V_{OD-BC(MIN)}$ for the Strong 0 is greater than -300mV.

890

- 891 • Verify that $V_{OD-CA(MAX)}$ for the Strong 1 is less than 300mV.
- 892 • Verify that $V_{OD-CA(MIN)}$ for the Weak 1 is greater than 97mV.
- 893 • Verify that $V_{OD-CA(MAX)}$ for the Weak 0 is less than -97mV.
- 894 • Verify that $V_{OD-CA(MIN)}$ for the Strong 0 is greater than -300mV.

895 Possible Problems

896 Both the differential voltage (V_{OD}) and differential voltage mismatch (ΔV_{OD}) tests are especially sensitive
897 measurements, and can be greatly affected by the test setup. If a device is found to fail this test, care should
898 be taken to verify and doublecheck the test setup. Ensure that a DSO calibration has been performed, as
899 well as a probe calibration/deskew (as these are often separate procedures on some instruments.) Also,
900 make sure that the probe connections to the DUT are clean and symmetric for the V_A , V_B , and V_C signals.

Test 1.2.8 HS-TX Differential Voltage Mismatch (ΔV_{OD})

Purpose

To verify that the Differential Voltage Mismatch (ΔV_{OD}) of the DUT HS transmitter is within the conformance limits.

References

- [1] C-PHY Specification, Section 9.1.1
- [2] Ibid, Table 22

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for ΔV_{OD} , which is a device's HS-TX Differential Voltage Mismatch.

The specification states[1],

The output differential voltage mismatch, ΔV_{OD} , is defined as the difference of the maximum and minimum of: the absolute values of the differential strong one and strong zero output voltages of the three possible wire pairs. This is expressed by the following equations that consider the V_{OD} for a particular wire pair in a specific state as described in Table 21:

$$V_{OD_MAX} = \max(V_{OD_AB_+X}, |V_{OD_AB_ -X}|, V_{OD_BC_+Y}, |V_{OD_BC_ -Y}|, V_{OD_CA_+Z}, |V_{OD_CA_ -Z}|)$$

$$V_{OD_MIN} = \min(V_{OD_AB_+X}, |V_{OD_AB_ -X}|, V_{OD_BC_+Y}, |V_{OD_BC_ -Y}|, V_{OD_CA_+Z}, |V_{OD_CA_ -Z}|)$$

$$\Delta V_{OD} = V_{OD_MAX} - V_{OD_MIN}$$

Figure 1.2.8-1: ΔV_{OD} Specification Definition

The specification also provides conformance limits for ΔV_{OD} .

$ \Delta V_{OD} $	V_{OD} mismatch between the absolute values of the differential strong one and strong zero output voltages in any of the six possible high-speed states.			17	mV	2
-------------------	--	--	--	----	----	---

Figure 1.2.8-2: ΔV_{OD} Specification Conformance Requirements

In this test, the numerical V_{OD} results obtained in the previous test (see Test 1.2.7) will be used to compute the ΔV_{OD} results. V_{OD_MAX} in the equation above will be taken as the maximum of the three Strong 1 maximum V_{OD} values for AB, BC, and CA pairs. V_{OD_MIN} will be taken as the minimum of the three Strong 0 minimum V_{OD} values for AB, BC, and CA pairs. The difference of the absolute values of V_{OD_MAX} and V_{OD_MIN} will be taken to produce ΔV_{OD} .

For all cases, the absolute value of ΔV_{OD} must be less than 17mV in order to be considered conformant[2].

925 **Test Setup**

926 None.

927 **Test Procedure**

- 928 • Obtain the numerical V_{OD} results from Test 1.2.7, for all three differential pairs, and all Lanes.
- 929 • For each Lane, compute the ΔV_{OD} result as described above.

930 **Observable Results**

931 For all Lanes:

- 932 • Verify that the absolute value of ΔV_{OD} is less than 17mV.

933 **Possible Problems:**

934 See Possible Problems comments for Test 1.2.7. The same applies to this test.

Test 1.2.9 HS-TX Single-Ended Output High Voltages ($V_{OHHS(VA)}$, $V_{OHHS(VB)}$, $V_{OHHS(VC)}$)

Purpose

To verify that the Single-Ended Output High Voltages ($V_{OHHS(VA)}$, $V_{OHHS(VB)}$, and $V_{OHHS(VC)}$) of the DUT HS transmitter are less than the maximum conformance limit.

References

- [1] C-PHY Specification, Section 9.1.1
- [2] Ibid, Table 22

Resource Requirements

See Annex A.1.

Last Technical Modification

August 4, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for V_{OHHS} , which is a device's HS-TX Output High Voltage.

The specification states[1],

- 1013 The output voltages V_A , V_B and V_C at the A, B and C pins shall not exceed the high-speed output high voltage
- 1014 V_{OHHS} . V_{OLHS} is the high-speed output, low voltage on A, B and C, and is determined by V_{OD_AB} , V_{OD_BC} ,

Figure 1.2.9-1: V_{OHHS} Specification Definition

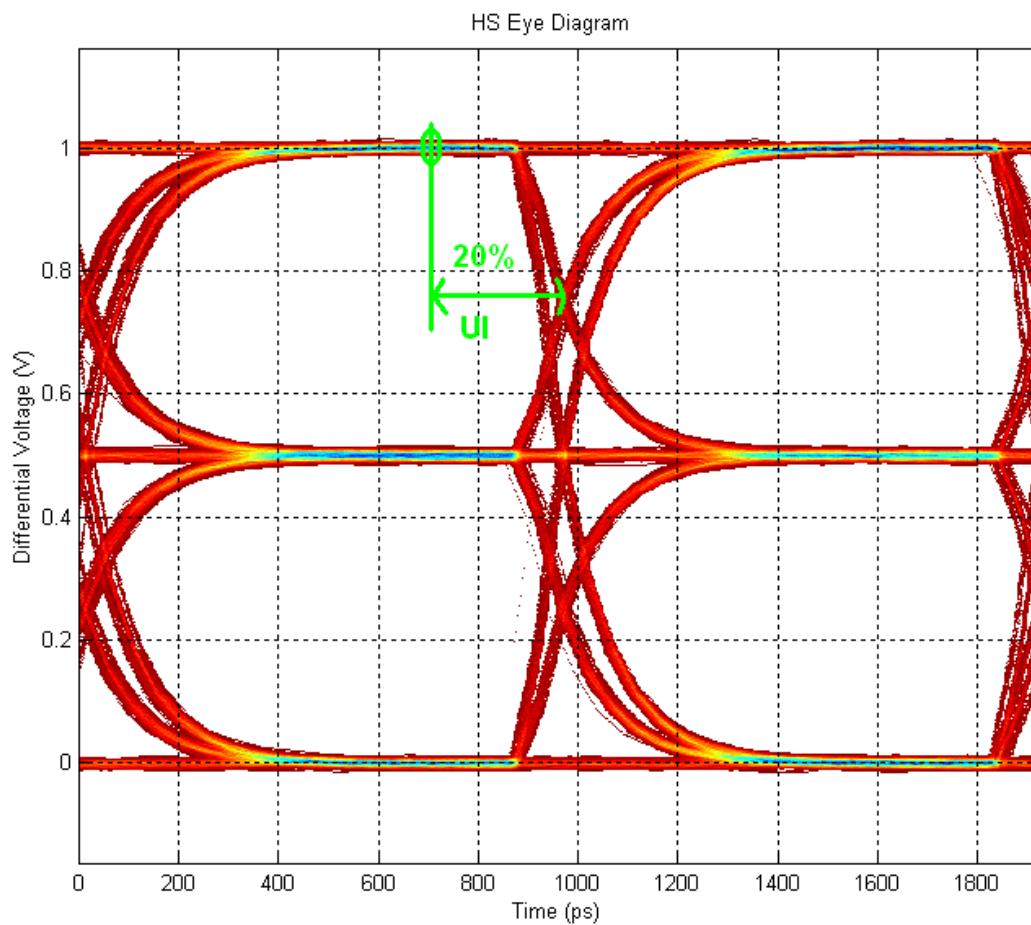
The specification also provides conformance limits for V_{OHHS} [2].

V_{OHHS}	HS output high voltage			425	mV	1
------------	------------------------	--	--	-----	----	---

Figure 1.2.9-2: V_{OHHS} Specification Conformance Requirements

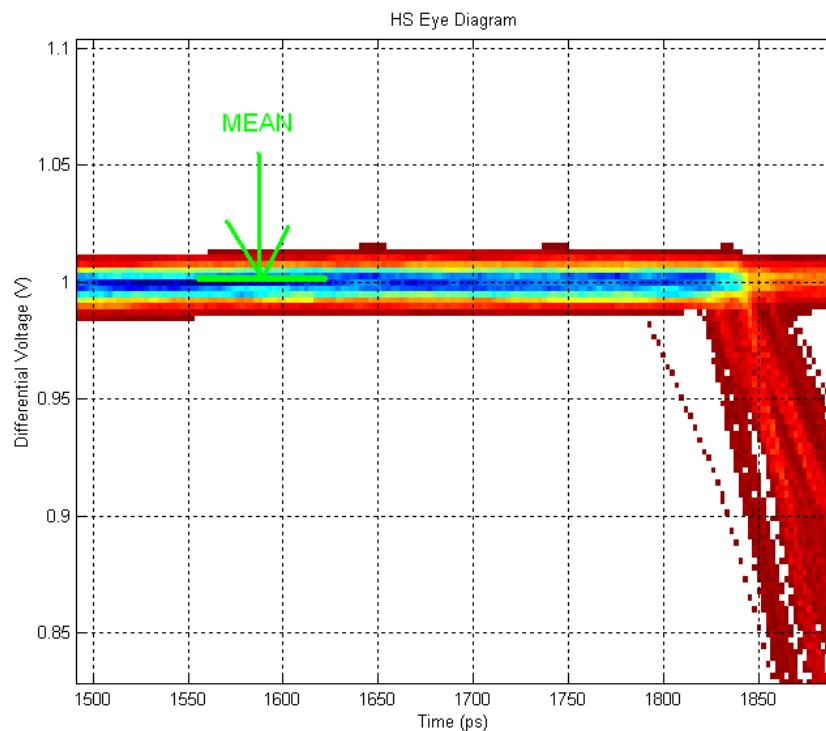
Like the V_{OD} measurements of Test 1.2.7, the exact method used for measuring V_{OHHS} must be clearly specified, as different amplitude measurement methods will significantly impact the measured result. For consistency, this test will use a similar approach as Test 1.2.7, and will use the same eye-based technique, except the methodology will be applied separately to the single-ended V_A , V_B , and V_C signals (rather than the differential $V_{OD_AB/BC/CA}$ signals) in order to create the eye diagram.

In this test, a sample of the DUTs HS signaling will be captured using a real-time DSO. The V_A , V_B , and V_C single-ended waveforms will be captured using separate channels of the DSO, and processed independently. Single-ended eye diagrams will be constructed separately for the V_A , V_B , and V_C signals, using the same methodology described in Test 1.2.7. The V_{OHHS} values for V_A , V_B , and V_C (which will be denoted as $V_{OHHS(VA)}$, $V_{OHHS(VB)}$, and $V_{OHHS(VC)}$ for the purposes of this test) will be computed using the same methodology as was used for V_{OD} , except the mean value of the histogram corresponding to the upper level of the 3-level single-ended eye diagram will be used (instead of the maximum).



965

Figure 1.2.9-3: Sample Single-Ended $V_{OHHS(VA)}$ Eye Diagram and Measurement



966

Figure 1.2.9-4: Zoomed-In View Showing Mean Measurement

967 For all Lanes, the V_{OHHS} results for V_A , V_B , and V_C must be less than 425mV in order to be considered
968 conformant[2].

969 **Test Setup**

970 See Annex B.1.2

971 **Test Procedure**

- 972 • Connect the DUT to the Reference Termination Board, such that Lane 0 is connected to $Z_{ID} = 100$
973 ohms.
974 • Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
975 • Capture the HS burst sequence using the DSO.
976 • Using post-processing methods, measure $V_{OHHS(VA)}$, $V_{OHHS(VB)}$, and $V_{OHHS(VC)}$ as described above.
977 • Repeat the previous steps for Lanes 1, 2, and 3 (if DUT implements multiple Lanes).

978 **Observable Results**

979 For all Lanes:

- 980 • Verify that $V_{OHHS(VA)}$ is less than 425mV.
981 • Verify that $V_{OHHS(VB)}$ is less than 425mV.
982 • Verify that $V_{OHHS(VC)}$ is less than 425mV.

983 **Possible Problems**

984 None.

Test 1.2.10 HS-TX Static Common-Point Voltages (V_{CPTX})

Purpose

To verify that the Static Common-Point Voltages (V_{CPTX}) of the DUT HS transmitter are within the conformance limits.

References

- [1] C-PHY Specification, Section 9.1.1
- [2] Ibid, Table 22
- [3] Ibid, Figure 43

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for V_{CPTX} , which is a device's HS-TX Static Common-Point Voltage.

The specification states[1],

- 1017 The common-point voltage V_{CPTX} is defined as the arithmetic mean value of the voltages at the A, B and C
 1018 pins:

$$1019 \quad V_{CPTX} = \frac{V_A + V_B + V_C}{3}$$

Figure 1.2.10-1: V_{CPTX} Specification Definition

1002 The specification also provides conformance limits for V_{CPTX} [2].

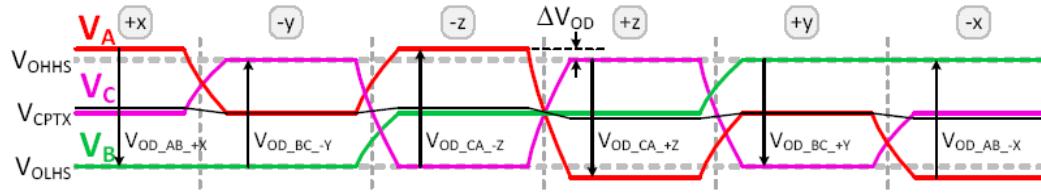
Table 22 HS Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{CPTX}	HS transmit static common-point voltage	175	225 to 250	310	mV	1, 3

Figure 1.2.10-2: V_{CPTX} Specification Conformance Requirements

1004 Because of various types of signal distortions that may occur, it is possible for V_{CPTX} to have different
 1005 values when a +x, -x, +y, -y, +z or -z state is being driven. Because of this, V_{CPTX} must be measured
 1006 separately for each state, at the "static" value corresponding to the settled voltage at the center of the UI (as
 1007 opposed to the "dynamic" AC fluctuations that occur at the symbol transitions, which are covered by a
 1008 separate specification, see Tests 1.2.12 and 1.2.13). The specification includes a figure showing various
 1009 different types of signal distortions that can occur[3]. This figure is reproduced below.

Large V_A Amplitude (single-ended high-speed signals)

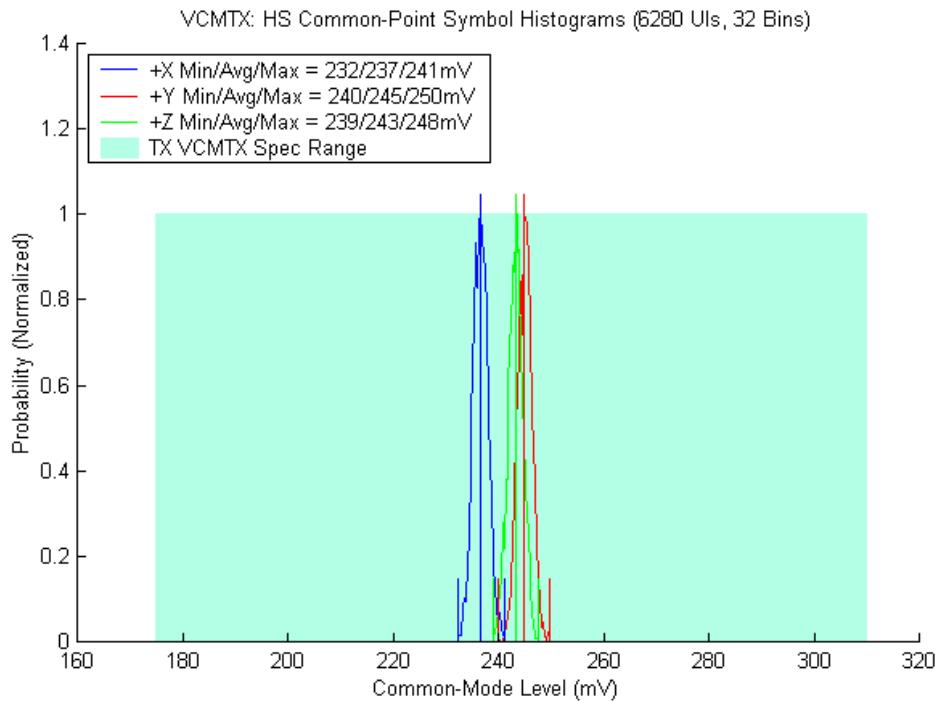


1010

Figure 1.2.10-3: Static V_{CPTX} Distortion

In this test, a portion of the DUTs HS signaling will be captured using a real-time DSO. The V_A , V_B , and V_C single-ended waveforms will be mathematically averaged together (as described above) to create the V_{CPTX} common-mode waveform. The V_{CPTX} waveform will be sampled at the center of each UI, corresponding to each state in the HS burst. The average common-point voltage observed over a minimum of 1,000 +x UIs will be computed as $V_{CPTX(HS_+x)}$, and the average common-mode voltage observed over a minimum of 1,000 -x UIs will be computed as $V_{CPTX(HS_x)}$. The average common-point voltage observed over a minimum of 1,000 +y UIs will be computed as $V_{CPTX(HS_+y)}$, and the average common-point voltage observed over a minimum of 1,000 -y UIs will be computed as $V_{CPTX(HS_y)}$. The average common-point voltage observed over a minimum of 1,000 +z UIs will be computed as $V_{CPTX(HS_+z)}$, and the average common-mode voltage observed over a minimum of 1,000 -z UIs will be computed as $V_{CPTX(HS_z)}$.

A sample measurement is shown in the figures below, showing the max, min, and mean common-mode levels for the +x, +y, +z, and -x, -y, -z states of an HS burst.



1023

Figure 1.2.10-4: Sample +x, +y, +z V_{CPTX} Histograms

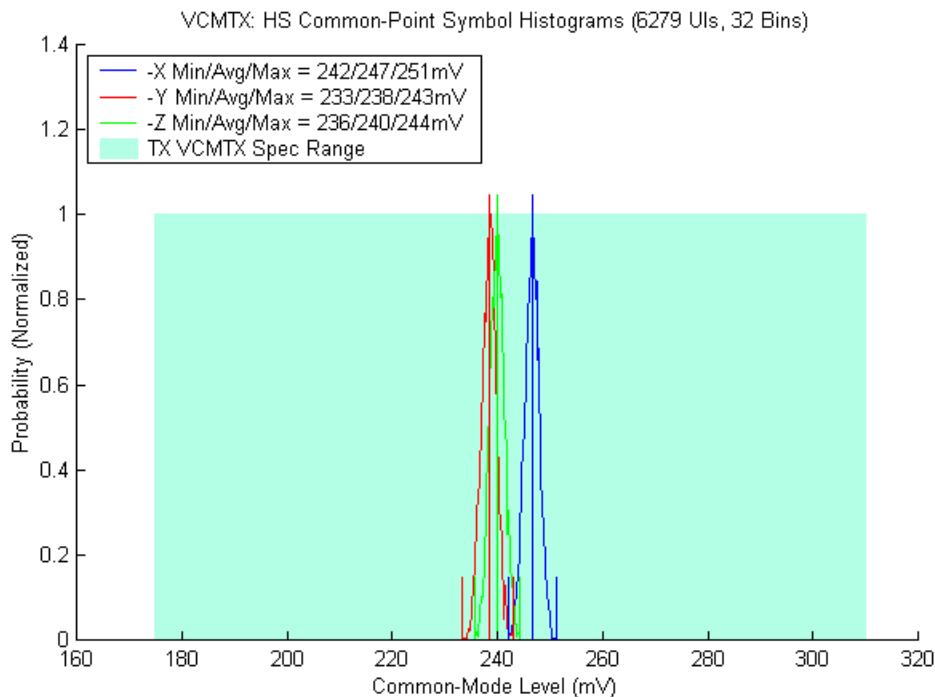


Figure 1.2.10-5: Sample -x, -y, -z V_{CPTX} Histograms

This measurement shall be performed for all Lanes.

For all cases, the mean values for V_{CPTX} for each of the +x, +y, +z, -x, -y, and -z states must be between 175 to 310mV in order to be considered conformant[2].

Test Setup

See Annex B.1.2.

Test Procedure

- Connect the DUT to the Reference Termination Board, such that Lane 0 is connected to Z_{ID} = 100 ohms.
- Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods, measure V_{CPTX}, for all six states, as described above.
- Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Lanes).

Observable Results

For all Lanes:

- Verify that the mean value of V_{CPTX(HS_+X)} is between 175 and 310mV.
- Verify that the mean value of V_{CPTX(HS_-X)} is between 175 and 310mV.
- Verify that the mean value of V_{CPTX(HS_+Y)} is between 175 and 310mV.
- Verify that the mean value of V_{CPTX(HS_-Y)} is between 175 and 310mV.
- Verify that the mean value of V_{CPTX(HS_+Z)} is between 175 and 310mV.
- Verify that the mean value of V_{CPTX(HS_-Z)} is between 175 and 310mV.

1045 **Possible Problem**
1046 None.

Test 1.2.11 HS-TX Static Common-Point Voltage Mismatch ($\Delta V_{CPTX(HS)}$)

Purpose

To verify that the Static Common-Point Voltage Mismatch ($\Delta V_{CPTX(HS)}$) of the DUT HS transmitter is less than the maximum conformance limit.

References

- [1] C-PHY Specification, Section 9.1.1
- [2] Ibid, Table 22

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for $\Delta V_{CPTX(HS)}$, which is a device's HS-TX Static Common-Point Voltage Mismatch.

In Test 1.2.10, the HS-TX static common-mode levels were measured as $V_{CPTX(HS_+X)}$, $V_{CPTX(HS_X)}$, $V_{CPTX(HS_+Y)}$, $V_{CPTX(HS_Y)}$, $V_{CPTX(HS_+Z)}$, and $V_{CPTX(HS_Z)}$. In addition to specifying requirements for the absolute voltages for these six values, the specification also defines a requirement on their symmetry, i.e., how matched they are to each other.

The specification states[1],

1041 The static common-point voltage mismatch between the six high-speed states is defined as:

$$1042 \quad V_{MAXCP} = \max(V_{CPTX(HS_+X)}, V_{CPTX(HS_X)}, V_{CPTX(HS_+Y)}, V_{CPTX(HS_Y)}, V_{CPTX(HS_+Z)}, V_{CPTX(HS_Z)})$$

$$1043 \quad V_{MINCP} = \min(V_{CPTX(HS_+X)}, V_{CPTX(HS_X)}, V_{CPTX(HS_+Y)}, V_{CPTX(HS_Y)}, V_{CPTX(HS_+Z)}, V_{CPTX(HS_Z)})$$

$$1044 \quad \Delta V_{CPTX(HS)} = \frac{V_{MAXCP} - V_{MINCP}}{2}$$

Figure 1.2.11-1: $\Delta V_{CPTX(HS)}$ Specification Definition

1067 The specification also provides conformance limits for $\Delta V_{CPTX(HS)}$ [2].

$ \Delta V_{CPTX(HS)} $	V _{CPTX} mismatch when output is in any of the six high-speed states	9	mV	2
-------------------------	---	---	----	---

Figure 1.2.11-2: $\Delta V_{CPTX(HS)}$ Specification Conformance Requirements

1069 In this test, the numerical results from Test 1.2.10 for $V_{CPTX(HS_+X)}$, $V_{CPTX(HS_X)}$, $V_{CPTX(HS_+Y)}$, $V_{CPTX(HS_Y)}$, $V_{CPTX(HS_+Z)}$, and $V_{CPTX(HS_Z)}$ will be used to compute the HS-TX Static Common-Point Voltage Mismatch, $\Delta V_{CPTX(HS)}$. The result for $\Delta V_{CPTX(HS)}$ will be computed as shown above. The measurement will be computed and reported separately for each Lane.

1073 For all cases, the value for $\Delta V_{CPTX(HS)}$ must be less than 9mV in order to be considered conformant[2].

1074 **Test Setup**

1075 None.

1076 **Test Procedure**

- 1077 • Obtain the numerical Lane 0 $V_{CPTX(HS_+X)}$, $V_{CPTX(HS_X)}$, $V_{CPTX(HS_+Y)}$, $V_{CPTX(HS_Y)}$, $V_{CPTX(HS_+Z)}$, and
1078 $V_{CPTX(HS_Z)}$ results from Test 1.2.10.
- 1079 • Compute the Lane 0 $\Delta V_{CPTX(HS)}$ result as described above.
- 1080 • Repeat the previous steps for Lanes 1, 2, and 3 (if DUT implements multiple Lanes).

1081 **Observable Results**

1082 For all Lanes:

- 1083 • Verify that $\Delta V_{CPTX(HS)}$ is less than 9mV.

1084 **Possible Problems**

1085 None.

Test 1.2.12 HS-TX Dynamic Common-Point Variations Between 50-450MHz ($\Delta V_{CPTX(LF)}$)

Purpose

To verify that the AC Common-Point Signal Level Variations between 50 and 450MHz ($\Delta V_{CPTX(LF)}$) of the DUT HS transmitter are less than the maximum allowable limit.

References

- [1] C-PHY Specification, Section 9.1.1
- [2] Ibid, Table 23
- [3] Ibid, Figure 42

Resource Requirements

See Annex A.1.

Last Technical Modification

August 4, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for $\Delta V_{CPTX(LF)}$, which is a device's HS-TX Dynamic Common-Point Variations between 50 and 450MHz.

The specification defines several requirements regarding a device's common-mode signaling. These specifications each measure slightly different distortions of the common-mode signal, which can result from very specific and distinct types of waveform asymmetry. "Dynamic" (or AC) variations are typically caused by an asymmetry in the rise/fall times of the single-ended HS signals.

The specification states[1],

- 1045 The transmitter shall send data such that the high frequency and low frequency common-point voltage
- 1046 variations do not exceed $\Delta V_{CPTX(HF)}$ and $\Delta V_{CPTX(LF)}$, respectively. An example test circuit for the measurement

Figure 1.2.12-1: $\Delta V_{CPTX(LF)}$ Specification Definition

1107 The specification also provides conformance limits for $\Delta V_{CPTX(LF)}$ [2].

$\Delta V_{CPTX(LF)}$	Common-level variation between 50 MHz and 450 MHz			25	mV _{PEAK}	
-----------------------	---	--	--	----	--------------------	--

Figure 1.2.12-2: $\Delta V_{CPTX(LF)}$ Specification Conformance Requirements

1109 The specification includes a figure showing various different types of signal distortions that can occur[3].
 1110 This figure is reproduced below.

Slow Rise/Fall V_A (single-ended high-speed signals)

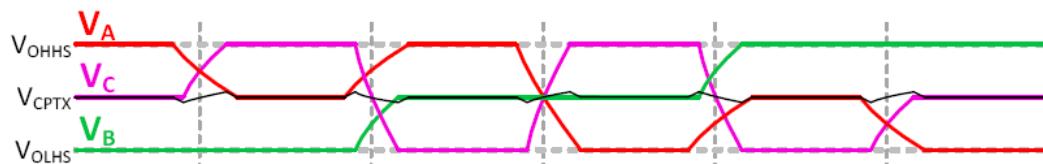


Figure 42 Possible V_{CPTX} and ΔV_{OD} Distortions of the Single-ended HS Signals

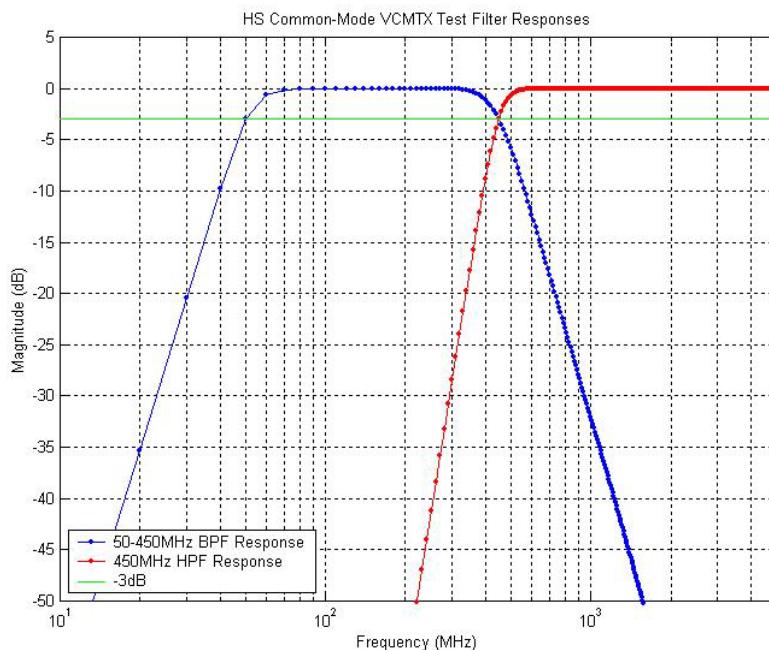
1111

Figure 1.2.12-3: Dynamic V_{CPTX} Distortion

1112 In this test, the V_{CPTX} common-mode signal will be captured using a real-time DSO, in the same manner as
1113 was used for the HS-TX Static Common-Point Voltages measurement (see Test 1.2.10). However for this
1114 test, rather than measuring the average DC state levels, the AC voltage will be measured, specifically for
1115 the frequency range between 50 and 450MHz.

1116 In order to isolate the energy in the frequency band of interest, some methodology must be employed to
1117 remove the energy that is above 450MHz and below 50MHz. While there are different possible methods
1118 that can accomplish this, the chosen implementation for this test is through the use of post-processing
1119 filters, which are specifically designed to greatly attenuate the energy outside the band of interest. (Note
1120 that because the spec does not define a particular test filter as part of the requirement definition, the
1121 measured result may be heavily dependent on the chosen implementation methodology. Nonetheless, a
1122 common filter must be chosen for conformance testing purposes.)

1123 The selected implementation uses a 8th-order Butterworth IIR bandpass filter as the test filter, with -3dB
1124 cutoff frequencies of 50 and 450MHz. The frequency response of the test filter is shown in the figure
1125 below. The raw V_{CPTX} waveform is passed through the filter prior to making the peak voltage measurement.
1126 The peak voltage of the bandpass-filtered V_{CPTX} waveform is measured to produce the final $V_{CPTX(LF)}$ result.



1127

Figure 1.2.12-4: ΔV_{CPTX} Test Filter Responses (50-450MHz BPF shown in blue)

1128 For all Lanes, $\Delta V_{CPTX(LF)}$ must be less than 25mV_{PEAK} in order to be considered conformant[2].

1129 Test Setup

1130 See Annex B.1.2.

1131 Test Procedure

- 1132 • Connect the DUT Lane 0 to the Reference Termination Board (RTB).
- 1133 • Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
- 1134 • Capture the HS burst sequence using the DSO.
- 1135 • Using post-processing methods as described above, measure $V_{CPTX(LF)}$.
- 1136 • Repeat the previous steps for Lanes 1, 2, and 3 (if DUT implements multiple Lanes).

1137 Observable Results

1138 For all Lanes:

- 1139 • Verify that $\Delta V_{CPTX(LF)}$ is less than 25mV_{PEAK}.

1140 Possible Problems

1141 None

Test 1.2.13 HS-TX Dynamic Common-Point Variations Above 450MHz ($\Delta V_{CPTX(HF)}$)

Purpose

To verify that the AC Common-Mode Signal Level Variations above 450MHz ($\Delta V_{CPTX(HF)}$) of the DUT HS transmitter are less than the maximum allowable limit.

References

- [1] C-PHY Specification, Section 9.1.1
- [2] Ibid, Table 23

Resource Requirements

See Annex A.1.

Last Technical Modification

August 4, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for $\Delta V_{CPTX(HF)}$, which is a device's HS-TX Dynamic Common-Point Variations above 450MHz.

The specification states[1],

- 1045 The transmitter shall send data such that the high frequency and low frequency common-point voltage
 1046 variations do not exceed $\Delta V_{CPTX(HF)}$ and $\Delta V_{CPTX(LF)}$, respectively. An example test circuit for the measurement

Figure 1.2.13-1: $\Delta V_{CPTX(HF)}$ Specification Definition

1158 The specification also provides conformance limits for $\Delta V_{CPTX(HF)}$ [2].

Table 23 HS Transmitter AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CPTX(HF)}$	Common-level variations above 450 MHz			15	mV _{RMS}	

Figure 1.2.13-2: $\Delta V_{CPTX(HF)}$ Specification Conformance Requirements

1160 Note that the procedure for this test is essentially identical to the previous $\Delta V_{CPTX(F)}$ test (see Test 1.2.12),
 1161 except that a highpass test filter is used rather than a bandpass filter, and the result is measured as V_{RMS}
 1162 rather than V_{PEAK} . The test filter for this test is an 8th-order Butterworth highpass filter, with a cutoff
 1163 frequency of 450MHz, (see Figure 1.2.12-4, Test 1.2.12). $\Delta V_{CPTX(HF)}$ is measured as the RMS value of the
 1164 highpass-filtered V_{CPTX} waveform.

1165 For all Lanes, the value of $\Delta V_{CPTX(HF)}$ must be less than 15mV_{RMS} in order to be considered conformant[2].

Test Setup

1167 See Annex B.1.2.

Test Procedure

- Connect the DUT Lane 0 to the Reference Termination Board (RTB).
- Create a condition that causes the DUT to source an HS burst sequence on Lane 0.

- 1171 • Capture the HS burst sequence using the DSO.
1172 • Using post-processing methods, measure $\Delta V_{CPTX(HF)}$ as described above.
1173 • Repeat the previous steps for Lanes 1, 2, and 3 (if DUT implements multiple Lanes).

1174 **Observable Results**

1175 For all Lanes:

- 1176 • Verify that $\Delta V_{CPTX(HF)}$ is less than 15mV_{RMS}.

1177 **Possible Problems**

1178 None.

Test 1.2.14 HS-TX Rise Time (t_R)

Purpose

To verify that the Rise Time (t_R) of the DUT HS transmitter is within the conformance limits.

References

[1] C-PHY Specification, Section 9.1.1

[2] Ibid, Table 23

Resource Requirements

See Annex A.1.

Last Technical Modification

November 10, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for t_R , which is a device's HS-TX Rise Time.

The specification states[1],

1061 The driver shall meet the t_R and t_F specifications as specified in Table 23. The specifications for TX common-

Figure 1.2.14-1: t_R Specification Definition

The specification also provides the conformance limits (which are different for different HS symbol rates) in a summary table[2],

Table 23 HS Transmitter AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
t_R and t_F	Rise time and fall time from -58 mV to +58 mV			0.285	UI	1, 2, 3, 5, 6
				0.4 (Note 4)	UI	1, 3, 4, 5, 6
$t_{RISE-FALL-MAX}$	Rise time and fall time limit from -58 mV to +58 mV			360 ps	ps	4, 5

Note:

1. UI is equal to $1/(2 \cdot f_h)$. Refer to Section 8.3 for the definition of f_h .
2. Applicable for all HS symbol rates > 1.5 Gsps
3. To avoid excessive radiation, devices operating at symbol rates ≤ 1.5 Gsps should not use values below 100 ps.
4. The maximum absolute time limit of rise and fall times, $t_{RISE-FALL-MAX}$, establishes an upper time limit that is not UI-based. This upper bound that constrains the rise and fall time is useful for implementation of the clock recovery circuit. For rates ≤ 1.5 Gsps the rise and fall time shall be $\leq \min(0.4 \cdot UI, t_{RISE-FALL-MAX})$.
5. Value when driving into load impedance, Z_{ID} , equal to 100 ohms.
6. The rise time measurement applies only to the strong zero to weak one transition, and the fall time measurement applies only to the strong one to weak zero transition.

Figure 1.2.14-2: t_R Conformance Limits

The main challenge to performing this test relates to the fact (as stated in table Note 6 above) that the rise time measurement must be performed on the strong zero to weak one transition, and the fall time must be performed on the strong one to weak zero transition. Due to the complexity of C-PHY signaling, these

1199 transitions may be difficult to isolate. The transitions can be isolated using advanced DSO triggering
1200 techniques (e.g., zone triggering). However if these techniques are not available, it is also possible to use a
1201 test mode that isolates only the strong zero to weak one transition.

1202 In this test, a sample of the DUTs HS signaling will be captured using a real-time DSO. The differential
1203 waveform will be computed as difference of the V_A and V_B single-ended waveforms ($V_A - V_B$). The
1204 averaged rise time waveform will be computed for the strong zero to weak one transition, averaging at least
1205 128 waveforms. The Rise Time (t_R) of the averaged reference waveform between the -58 and $+58mV$
1206 levels will be measured to produce the final t_R result.

1207 For devices operating at a maximum rate $\leq 1.5Gsp$ s, the value of t_R must be less than $\max(0.4 \text{ UI}, 360\text{ps})$
1208 and should be greater than 100ps (where UI is the nominal HS Unit Interval for the DUT, see Test 1.2.19)
1209 in order to be considered conformant. For devices operating at a rate $> 1.5Gsp$ s, the value of t_R must be less
1210 than 0.285 UI in order to be considered conformant[2].

1211 **Test Setup**

1212 See Annex B.1.2.

1213 **Test Procedure**

- 1214 • Connect the DUT to the Reference Termination Board, such that Lane 0 is connected to $Z_{ID} = 100$
1215 ohms.
- 1216 • Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
- 1217 • Capture the HS burst sequence using the DSO.
- 1218 • Using post-processing methods, measure t_R as described above.
- 1219 • Repeat the previous steps for Lanes 1, 2, and 3 (if DUT implements multiple Lanes).

1220 **Observable Results**

1221 For all Lanes:

- 1222 • (*For DUTs operating $\leq 1.5Gsp$ s*): Verify that t_R is less than $\max(0.4 \text{ UI}, 360) \text{ ps}$.
- 1223 • (*For DUTs operating $> 1.5Gsp$ s*): Verify that t_R is less than 0.285UI .

1224 **Possible Problems**

1225 Note that in some cases (particularly at higher symbol rates), the test setup itself may adversely impact the
1226 measurement. The use of high-impedance, solder-in probes on the RTB may result in slightly slower
1227 rise/fall time measured values, compared to the expected design values. In these cases, it may be beneficial
1228 to use an alternate test setup, whereby the DUT is connected directly to the DSO's 50-ohm inputs. This
1229 alternate setup is permitted only for this test, as it does not provide a true switched-termination
1230 environment, and presents an incorrect termination environment for making common-mode measurements.
1231 However it may produce better (faster) results for differential rise/fall times. See Annex B for this alternate
1232 test setup.

Test 1.2.15 HS-TX Fall Time (t_F)**Purpose**

To verify that the Fall Time (t_F) of the DUT HS transmitter is within the conformance limits.

References

[1] C-PHY Specification, Section 9.1.1

[2] Ibid, Table 23

Resource Requirements

See Annex A.1.

Last Technical Modification

November 10, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for t_F , which is a device's HS-TX Fall Time.

The specification states[1],

1061 The driver shall meet the t_R and t_F specifications as specified in Table 23. The specifications for TX common-

Figure 1.2.15-1: t_F Specification Definition

Note the methodology for this test is identical to the previous test (see Test 1.2.14), except that the Fall Time (t_F) is measured on a weak one to strong zero transition. The same averaging approach is used.

Note also that the minimum conformance limits are described with a 'should', and are therefore informative. (See Figure 1.2.14-2, Note 3, in the previous test). Note also that the conformance limits are the same as the previous test.

For devices operating at a maximum rate $\leq 1.5\text{GspS}$, the value of t_F must be less than $\max(0.4 \text{ UI}, 360\text{ps})$ and should be greater than 100ps (where UI is the nominal HS Unit Interval for the DUT, see Test 1.2.19) in order to be considered conformant. For devices operating at a rate $> 1.5\text{GspS}$, the value of t_F must be less than 0.285 UI in order to be considered conformant[2].

Test Setup

See Annex B.1.2.

Test Procedure

- Connect the DUT to the Reference Termination Board, such that Lane 0 is connected to $Z_{ID} = 100 \text{ ohms}$.
- Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
- Capture the HS burst sequence using the DSO.
- Using post-processing methods, measure t_F as described above.
- Repeat the previous steps for Lanes 1, 2, and 3 (if DUT implements multiple Lanes).

1265 **Observable Results**

1266 For all Lanes:

1267 • (*For DUTs operating <= 1.5Gbps*): Verify that t_F is less than max(0.4 UI, 360) ps.

1268 • (*For DUTs operating > 1.5Gbps*): Verify that t_F is less than 0.285UI.

1269 **Possible Problems**

1270 See Possible Problems for Test 1.2.14. The same applies to this test.

Test 1.2.16 T₃-POST Duration

Purpose

To verify that the duration the DUT TX drives the final differential states following the payload data of a HS-TX burst (T₃-POST), is greater than the minimum required value.

References

- [1] C-PHY Specification, Figure 23
- [2] Ibid, Section 6.4.4
- [3] Ibid, Section 6.9

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

As part of the process of completing a HS Data Transmission Burst, the C-PHY Specification provides a requirement for the length of time that a device must drive the final HS differential states following the last payload data bit of a HS transmission burst. This interval is defined as T₃-POST, and is shown in the figure below[1].

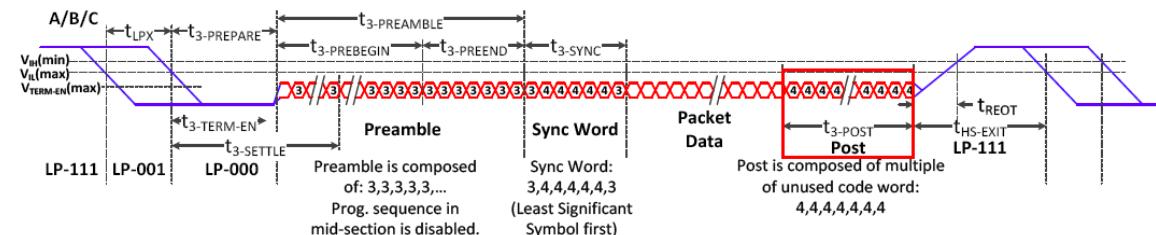


Figure 23 High-Speed Data Transmission in Burst

Figure 1.2.16-1: T₃-POST Interval

The specification states[2],

- 618 The end of Packet Data is identified by a unique sequence of “4” symbols in t₃-POST. The receiver identifies the end of Packet Data when it detects a sequence of seven consecutive “4” symbols. The Post field may often consist of multiple groups of seven “4” symbols to provide a sufficient number of clocks to the upper layer protocol to clear out any pipeline stages that may contain received data. The length of the Post field is a programmable value set in the master, for example: the post length field of the register described in section 12.5.4.

Figure 1.2.16-2: T₃-POST Specification Definition

1290 Also, the specification states[3],

756 example method to specify the length of $t_{3\text{-POST}}$ is provided in section 12.5.3. $t_{3\text{-POST}}$ should be
757 adjustable from 7 UI minimum to 224 UI maximum in increments of 7 UI. An example method to specify
758 the length of $t_{3\text{-POST}}$ is provided in section 12.5.4.

Figure 1.2.16-3: $T_{3\text{-POST}}$ Length Requirements

1292 The measured length of $T_{3\text{-POST}}$ should be between 7 and 224 UI (where UI is the nominal HS Unit Interval
1293 for the DUT, see Test 1.2.17), and should consist of all ‘4’ symbols in order to be considered
1294 conformant[2].

1295 **Test Setup**

1296 See Annex B.1.2.

1297 **Test Procedure**

- 1298 • Connect the DUT’s Lane 0 to the Reference Termination Board (RTB).
- 1299 • Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
- 1300 • Capture the HS burst sequence using the DSO.
- 1301 • Using post-processing methods as described above, measure $T_{3\text{-POST}}$ in units of UI.
- 1302 • Using post-processing methods as described above, measure the symbol values during $T_{3\text{-POST}}$.
- 1303 • Repeat the previous steps for Data Lanes 1, 2, and 3 (if DUT implements multiple Data Lanes).

1304 **Observable Results**

1305 For all Lanes:

- 1306 • Verify that $T_{3\text{-POST}}$ is between 7 and 224 UI.
- 1307 • Verify that the $T_{3\text{-POST}}$ value consists of all ‘4’ symbols.

1308 **Possible Problems**

1309 See Possible Problems comments for Test 1.3.1. The same applies to this test.

Test 1.2.17 30%-85% Post-EoT Rise Time (T_{REOT})

Purpose

To verify that the 30%-85% Post-EoT Rise Time (T_{REOT}) of the DUT LP transmitter is within the conformance limits.

References

- [1] C-PHY Specification, Table 25 Note 5
- [2] Ibid, Figure 23
- [3] Ibid, Section Table 25

Resource Requirements

See Annex A.1.

Last Technical Modification

April 14, 2015

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for T_{REOT} , which is a device's LP-TX 30%-85% Rise Time, following an EoT exit from a High-Speed Data Transmission Burst.

The specification states[1],

5. *The rise-time of T_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.*

Figure 1.2.17-1: T_{REOT} Specification Definition

The specification also shows an example of T_{REOT} [2].

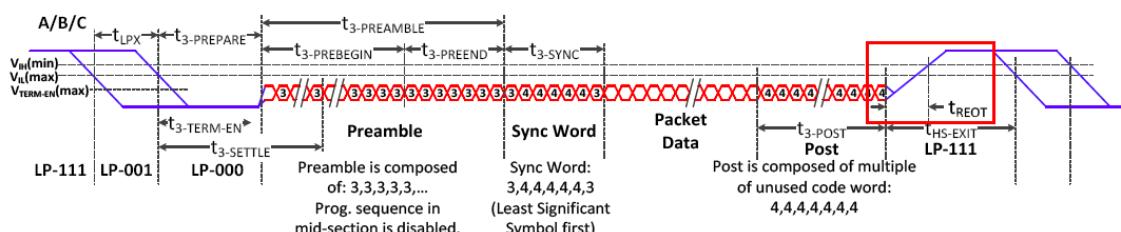


Figure 23 High-Speed Data Transmission in Burst

Figure 1.2.17-2: T_{REOT} Rise Time

In this test, an HS-TX Data Lane signaling burst from the DUT transmitter will be captured using a real-time DSO. The differential waveform will be computed as difference of the positive and negative single-ended waveforms ($V_C - V_A$). The T_{REOT} Rise Time will be measured starting at the time where the differential waveform last crosses $\pm 40\text{mV}$, and ends where V_A crosses $V_{IH,\text{MIN}} = 740\text{mV}$. (Note the spec does not differentiate whether V_A or V_C should be used, as they are identical from the specification's perspective. However, for real devices the rise times may not be the same. However for this test, V_A will be used.)

The value of T_{REOT} must be less than 35ns in order to be considered conformant[3].

1337 Test Setup

1338 See Annex B.1.2.

1339 Test Procedure

- 1340 • Connect the DUT's Lane 0 to the Reference Termination Board (RTB).
- 1341 • Create a condition that causes the DUT to source an HS burst sequence on Lane 0.
- 1342 • Capture the HS burst sequence using the DSO.
- 1343 • Using post-processing methods as described above, measure T_{REOT} .
- 1344 • Repeat the previous steps for all other Lanes (if DUT implements multiple Lanes).

1345 Observable Results

1346 For all Lanes:

- 1347 • Verify that T_{REOT} is less than 35ns.

1348 Possible Problems

1349 None

Test 1.2.18 $T_{HS-EXIT}$ Value

Purpose

To verify that the duration that the Data Lane transmitter remains in the LP-111 (Stop) state after exiting HS mode ($T_{HS-EXIT}$), is greater than the minimum required value.

References

[1] C-PHY Specification, Figure 23

[2] Ibid, Table 14

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

As part of the process for switching a C-PHY Lane out of HS mode, the C-PHY Specification provides a requirement for the minimum time that the Lane must remain in the LP-111 Stop state before initiating any further sequences. This interval is defined as $T_{HS-EXIT}$, and is shown in the figure below[1].

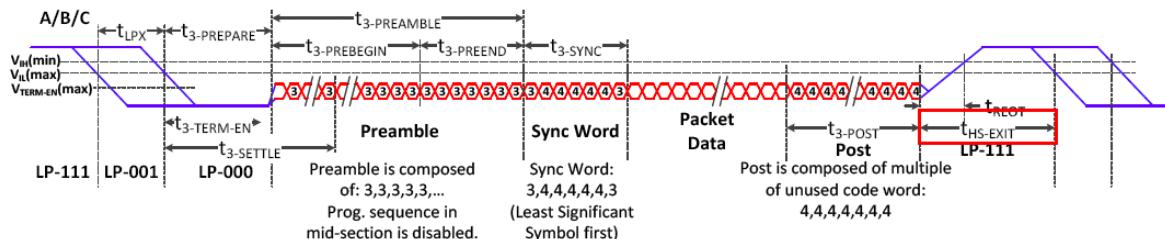


Figure 23 High-Speed Data Transmission in Burst

Figure 1.2.18-1: $T_{HS-EXIT}$ Interval

In this test, the DUT will be configured to send repeated HS burst sequences, and the $T_{HS-EXIT}$ values will be observed. The values will be observed over multiple HS bursts in order to determine the minimum value. If the DUT sources image data (which is transmitted in many cases using one HS burst per horizontal pixel line, though this is not explicitly true for all applications), it is recommended that $T_{HS-EXIT}$ be observed over a minimum of one entire frame cycle (i.e., all bursts from the start of a 2-D image (frame) to the end of the 2-D image (frame), including all data and control packets).

While the primary description of $T_{HS-EXIT}$ in the specification states[2],

$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.
---------------	--

Figure 1.2.18-2: $T_{HS-EXIT}$ Specification Definition

This wording does not explicitly indicate the exact start and end points of the parameter for the purpose of measurement. However, Figure 23 of the specification graphically shows the $T_{HS-EXIT}$ interval as starting at the end of the t_3-POST interval (which is defined by the point where the differential waveform crosses below the minimum valid HS-RX differential threshold level of +/-70mV, see Test 1.2.16.)

1377 Also, Figure 23 of the specification graphically shows the $T_{HS-EXIT}$ end point as being where the V_A LP-001
1378 falling edge crosses $V_{IL,MAX}$ (550mV) during the HS entry sequence of the next successive HS burst. (Note
1379 that while the example shows the next successive sequence being another HS burst, it is assumed that the
1380 $T_{HS-EXIT}$ requirement equally applies for any type of sequence that could follow an HS burst (e.g., Escape
1381 Mode, Bus Turnaround, etc), however this test will primarily verify the HS burst case. In lieu of any
1382 explicit textual definitions for the start and end points for $T_{HS-EXIT}$, the measurement start/end points for
1383 conformance test purposes must be inferred from the example figures.

1384 In this test, the $T_{HS-EXIT}$ interval for a given Lane will be observed, measured starting from the end of the
1385 $T_{HS-POST}$ interval (at the point where the $V_C - V_A$ differential waveform crosses below the minimum valid
1386 HS-RX differential threshold level of +/-70mV), to the point where the V_A LP-001 falling edge crosses
1387 $V_{IL,MAX}$ (550mV) during the next successive HS burst. (Alternately, if a burst is followed by some sequence
1388 other than another HS burst, the 550mV crossing time of the first LP falling edge (V_A , V_B , or V_C) of that
1389 sequence shall be used as the $T_{HS-EXIT}$ ending point.)

1390 The duration of $T_{HS-EXIT}$ shall be no less than 100ns for all observed bursts and for all Lanes in order to be
1391 considered conformant[2].

1392 **Test Setup**

1393 See Annex B.1.2.

1394 **Test Procedure**

- 1395 • Connect the DUT to the Reference Termination Board (RTB).
- 1396 • Create a condition that causes the DUT to source repeated HS burst sequences on Lane 0.
- 1397 • Capture the HS burst sequences using the DSO.
- 1398 • Using post-processing methods, measure $T_{HS-EXIT}$ as described above.
- 1399 • Repeat the previous steps for Lanes 1, 2, and 3 (if DUT implements multiple Lanes).

1400 **Observable Results**

1401 For all Lanes:

- 1402 • Verify that $T_{HS-EXIT}$ is no less than 100ns for all observed bursts.

1403 **Possible Problems**

1404 See Possible Problems comments for Test 1.3.1. The same applies to this test.

1405 Also, for DUTs that transmit extremely long bursts (which may occur in the case of some DSI transmitters,
1406 which are allowed to combine multiple successive data packets (up to and even including an entire 2-D
1407 image) into a single transmitted HS burst), it may not be possible to capture multiple successive bursts in a
1408 single DSO capture (depending on the overall burst length, and the memory depth of the DSO). Also, cases
1409 may exist where a DUT could potentially transmit extremely long LP periods between bursts, such that an
1410 entire $T_{HS-EXIT}$ period may not be able to fit within the capture depth of the DSO.

1411 In both of these cases, a modified procedure may be used whereby the DSO is configured to observe only
1412 the ends of the HS bursts (typically by triggering on the LP T_{REOT} rising edge at the end of the burst), and
1413 the window immediately following the burst may be observed (using a persistence trace mode of the DSO)
1414 to verify that no subsequent bursts begin within a minimum $T_{HS-EXIT}$ period of 100ns. Provided it can be
1415 shown that no bursts violate the minimum 100ns conformance limit, the exact value of $T_{HS-EXIT}$ does not
1416 need to be explicitly measured for every burst in order to demonstrate conformance.

Test 1.2.19 HS Clock Instantaneous UI (UI_{INST})

Purpose

To verify that the Instantaneous Unit Interval values (UI_{INST}) of the DUT HS transmitter are within the conformance limits.

References

- [1] C-PHY Specification, Figure 55
- [2] Ibid, Section 8.3
- [3] Ibid, Table 32

Resource Requirements

See Annex A.1.

Last Technical Modification

October 27, 2014

Discussion

Section 10 of the C-PHY Specification defines the High Speed Timing requirements for C-PHY products. Included in these requirements is a specification for UI_{INST} , which are a device's instantaneous Unit Interval values. An example figure showing this parameter is provided in the specification, and is reproduced in the figure below[1].

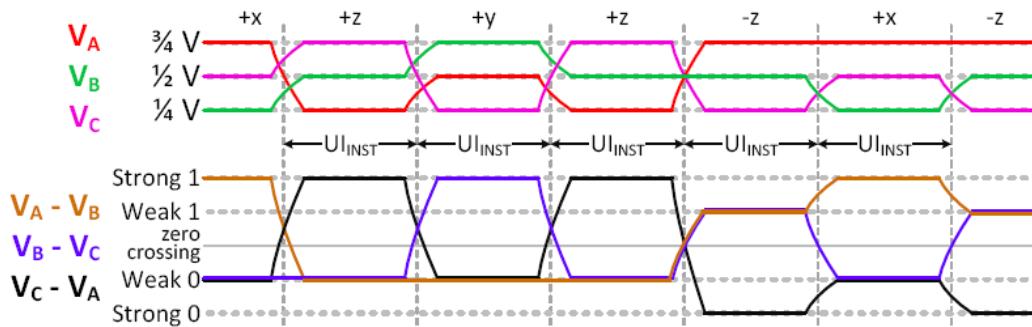


Figure 55 Example of Wire State Transitions at Symbol (UI) Boundaries

Figure 1.2.19-1: UI_{INST} Interval

The specification states[2],

- 906 The frequency 'fh' is the highest fundamental frequency for data transmission and is equal to $1/(2*UI_{INST,\text{MIN}})$.
- 907 Implementers should specify a value $UI_{INST,\text{MIN}}$ that represents the minimum instantaneous UI possible within a high-speed data transfer for a given implementation.

Figure 1.2.19-2: $UI_{INST,\text{MIN}}$ Specification Definition

This value would typically be obtained from the DUT vendor (either directly, or via the DUT's datasheet) prior to performing this test, but is not necessary for performing the test.

The specification also provides conformance limits for UI_{INST} [3].

Table 32 Unit Interval (UI) Specification

Parameter	Description	Min	Nom	Max	Units	Notes
UI _{INST}	UI instantaneous			12.5	ns	1, 2
ΔUI	UI variation	-10%		10%	UI	3
		-5%		5%	UI	4

Note:

1. This value corresponds to a minimum 80 Msps data rate.
2. The minimum UI shall not be violated for any single bit period. The allowed instantaneous UI variation can cause instantaneous data rate variations. Therefore, slave devices should be able to accommodate these instantaneous variations of the UI interval.
3. When $UI \geq 1\text{ns}$, within a single burst.
4. When $UI < 1\text{ns}$, within a single burst.

1439

Figure 1.2.19-3: UI_{INST} Specification Conformance Requirements

The specification defines an upper conformance limit for UI_{INST} of 12.5ns, which corresponds to a minimum allowed HS symbol rate of 80Msps. There is no explicit lower conformance value defined by the specification, however the specification does state as a note to the table above that the vendor-specified minimum UI shall not be violated for any single bit period. The purpose of this test is primarily to measure the DUT's average instantaneous UI (as it is referenced by other tests in this Test Suite), and to verify that this value is less than 12.5ns.

In this test, a sample of the DUT's HS signaling will be captured using a real-time DSO. The sample should contain at least several thousand UIs. The A-B, B-C, and C-A differential waveforms will be computed, in order to observe the zero crossings between each UI. The UI_{INST} values for each UI will be measured as the difference between successive 0V crossing times of the differential waveforms. For cases where multiple crossings occur between UIs, the first crossing shall be used, and the others ignored. The maximum, minimum, and average UI_{INST} values will be measured and reported across all observed UIs.

The maximum observed UI_{INST} value must be less than 12.5ns in order to be considered conformant[3].

Test Setup

See Annex B.1.2.

Test Procedure

- Connect the DUT to the Reference Termination Board.
- Create a condition that causes the DUT to source HS signaling (either burst or continuous).
- Capture the HS clock signaling using the DSO.
- Using post-processing methods, measure the maximum, minimum, and mean UI_{INST} values, as described above.

Observable Results

- Verify that the maximum UI_{INST} value is less than 12.5ns.
- Verify that the minimum UI_{INST} value is greater than or equal to the UI_{INST, MIN} value.
- The mean UI_{INST} value is reported for procedural purposes (as it is used in other tests in this test suite to calculate conformance limits for parameters whose ranges are either partially or entirely defined in terms of UI values).

Possible Problems

None.

Test 1.2.20 HS Clock Delta UI (Δ UI)

Purpose

To verify that the frequency stability of the DUT HS Clock during a single burst is within the conformance limits.

References:

[1] C-PHY Specification, Table 32

Resource Requirements

See Annex A.1.

Last Technical Modification

August 4, 2014

Discussion

Section 10 of the C-PHY Specification defines the High Speed Timing requirements for C-PHY products. Included in these requirements is a specification for Δ UI, which is a device's Unit Interval variation within a single HS burst.

The specification states[1],

Table 32 Unit Interval (UI) Specification

Parameter	Description	Min	Nom	Max	Units	Notes
UI _{INST}	UI instantaneous			12.5	ns	1, 2
Δ UI	UI variation	-10%		10%	UI	3
		-5%		5%	UI	4

Note:

1. This value corresponds to a minimum 80 Msps data rate.
2. The minimum UI shall not be violated for any single bit period. The allowed instantaneous UI variation can cause instantaneous data rate variations. Therefore, slave devices should be able to accommodate these instantaneous variations of the UI interval.
3. When $UI \geq 1\text{ns}$, within a single burst.
4. When $UI < 1\text{ns}$, within a single burst.

Figure 1.2.20-1: Δ UI Specification and Limits

Note that this specification is somewhat ambiguous, as it does not provide sufficient detail regarding how this parameter is to be measured. For the purposes of this test, a methodology must be defined that can yield reproducible results, which is provided below.

In this test, a single-burst sample of the DUTs HS signaling will be captured using a real-time DSO. The A-B, B-C, and C-A differential waveforms will be computed. The widths for each UI will be measured as the difference between successive 0V crossing times of the differential waveforms. For cases where multiple crossings occur between UIs, the first crossing shall be used, and the others ignored.

Note that because of the relatively low resolution of the sampled waveform (i.e., the number of samples per UI) relative to the high resolution of the conformance limits, the computed UI values at this point will contain a certain amount of error. If the inverse of these UI values is computed, one could consider the result to reflect the instantaneous bitrate of the transmitter. This is partially correct, however the results would contain a high degree of high-frequency error, caused by the limited resolution of the sampling rate, and hence the UI accuracy (as any underestimation of the UI width for one bit caused by the limited DSO

1497 sample rate, will translate into an overestimation of the width of the following UI, and vice-versa).
1498 However, it is possible to remove this error by filtering the data using a lowpass filter, which will reveal the
1499 underlying lower-frequency variation of the link rate with greater clarity.

1500 One important detail to note however is that the cutoff frequency, as well as the exact implementation of
1501 the filter can have a significant impact on the result. For the purposes of this measurement, a double-pole
1502 (second-order) Butterworth lowpass filter with a -3dB cutoff frequency of 2.0MHz will be used to filter the
1503 UI data to remove the high frequency noise/error components.

1504 The inverse of the measured UI values (obtained from the zero crossings) will be taken to produce an array
1505 of instantaneous frequency values. The test filter will then be applied to the inverse of the UI values. (Note
1506 that in this case the ‘sample rate’ of the data is one value per UI, so the test filter must be designed
1507 accordingly in order to produce the desired 2.0MHz cutoff. Also, it is recommended that a duplicate
1508 dummy copy of the data array be prepended to the data prior to filtering (and removed after filtering), in
1509 order to prevent errors caused by filter startup transients, if the filtering is performed in the time domain.)
1510 The resulting waveform that is produced at the output of the test filter will then be converted to units of
1511 percent, to produce the Δ UI values. The peak maximum and peak minimum values will be observed, and
1512 the one with the greater absolute value will be reported as the result for that burst. (Note if multiple bursts
1513 are observed, the peak value across all bursts will be reported as the final result.)

1514 For devices operating at a rate \leq 1GspS the maximum peak Δ UI variation value must be between -10%
1515 and +10% in order to be considered conformant[2]. For devices operating at a rate >1 GspS, the maximum
1516 peak Δ UI variation value must be between -5% and +5% in order to be considered conformant[2].

1517 **Test Setup**

1518 See Annex B.1.2.

1519 **Test Procedure**

- 1520 • Connect the DUT to the Reference Termination Board.
- 1521 • Create a condition that causes the DUT to source burst-mode HS signaling on Lane 0.
- 1522 • Capture the HS signaling using the DSO.
- 1523 • Using post-processing methods, measure the peak Δ UI value, as described above.

1524 **Observable Results**

- 1525 • (*For DUTs operating \leq 1GspS*): Verify that the peak Δ UI is between -10% and +10%.
- 1526 • (*For DUTs operating $>$ 1GspS*): Verify that the peak Δ UI is between -5% and +5%.

1527 **Possible Problems**

1528 None.

Group 3 LP-TX INIT, ULPS, and BTA Requirements

Overview

This group of tests verifies several miscellaneous LP-TX timing and behavioral requirements pertaining to initialization (INIT), Ultra-Low Power State (ULPS), and Bus Turnaround (BTA).

These tests are applicable to both Master and Slave devices, depending on the test. Tests 1.3.1 and 1.3.2 are applicable to Master devices only. Tests 1.3.3, 1.3.4, and 1.3.5 are applicable for any devices (Master or Slave) that support bi-directional operation.

Status

The test names, Discussion sections, and Procedures are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

Test 1.3.1 INIT: LP-TX Initialization Period ($T_{INIT,MASTER}$)

Purpose

To verify that the duration of the DUT's transmitted LP Initialization period ($T_{INIT,MASTER}$), is greater than the minimum required value.

References

- [1] C-PHY Specification, Section 6.11
- [2] Ibid, Table 18

Resource Requirements

See Annex A.

Last Technical Modification

October 27, 2014

Discussion

The C-PHY Specification includes requirements pertaining to the initialization behavior of both Master and Slave devices (where the Master is by definition the side that transmits the HS Clock). Included in these requirements is a specification for $T_{INIT,MASTER}$, which is the Master PHY's transmitted initialization period. (Note that this test is only applicable to Master DUTs.)

The specification states[1],

- 762 After power-up, the slave side PHY shall be initialized when the master PHY drives a Stop state (LP-111) for
 763 a period longer than t_{INIT} . The first Stop state longer than the specified t_{INIT} is called the initialization period.
 764 The master PHY itself shall be initialized by a system or protocol layer input signal (PPI). The master side
 765 shall ensure that a Stop state longer than t_{INIT} does not occur on the lines before the master is initialized. The
 766 slave side shall ignore all line states during an interval of unspecified length prior to the initialization period.
 767 In multi-lane configurations, all lanes shall be initialized simultaneously.

Figure 1.3.1-1: $T_{INIT,MASTER}$ Specification Definition

The specification also states[1],

- 768 Note that t_{INIT} is considered a protocol-dependent parameter, and thus the exact requirements for $t_{INIT,MASTER}$
 769 and $t_{INIT,SLAVE}$ (transmitter and receiver initialization Stop state lengths, respectively,) are defined by the
 770 protocol layer specification and are outside the scope of this document. However, the C-PHY specification
 771 does place a minimum bound on the lengths of $t_{INIT,MASTER}$ and $t_{INIT,SLAVE}$, which each shall be no less than
 772 100 μ s. A protocol layer specification using the C-PHY specification may specify any values greater than this
 773 limit, for example, $t_{INIT,MASTER} \geq 1$ ms and $t_{INIT,SLAVE} = 500$ to 800 μ s.

Figure 1.3.1-2: $T_{INIT,MASTER}$ Specification Minimum Requirement

The specification also gives conformance limits for T_{INIT} [2],

t_{INIT}	See Section 6.11.	100	μ s	2
------------	-------------------	-----	---------	---

Figure 1.3.1-3: T_{INIT} Conformance Limits

The purpose of this test will be to measure the DUT's $T_{INIT,MASTER}$ value, and verify that it is at least 100us, in order to verify the minimum requirements described by the C-PHY specification. (This test does not verify any additional requirements that may be imposed by an applicable protocol specification.)

12-Feb-2016

1564 Note also that because T_{INIT} is considered a protocol-dependent parameter by the C-PHY specification, it is
1565 possible that the generation and timing control of the T_{INIT} interval may be implemented in the protocol
1566 layer logic for some DUT types. Therefore, if a DUT is not designed to contain this logic (e.g., for a bare-
1567 phy DUT with a PPI or other exposed protocol interface), this test is considered Not Applicable.

1568 In this test, the length of the Master's transmitted LP-111 Initialization period ($T_{INIT,MASTER}$) will be
1569 observed using a real-time DSO. (Note that the termination environment is not critical to this measurement,
1570 and either the C_{LOAD} fixture, RTB, or no termination fixture may be used.) The length of $T_{INIT,MASTER}$ will be
1571 measured starting from the point where V_A is first observed to be greater than $V_{IH,MIN}$ (740mV) following a
1572 power-on event, and ending at the first point where V_A crosses below $V_{IL,MAX}$ (550mV). (Note this
1573 methodology assumes all 3 lines, V_A , V_B , and V_C switch at the same time, so it is only necessary to measure
1574 any one line.) The measurement will be performed on all Lanes.

1575 For all Lanes, the value of $T_{INIT,MASTER}$ must be greater than or equal to 100us in order to be considered
1576 conformant[2].

1577 **Test Setup**

1578 See Annex B.1.1 (or B.1.2).

1579 **Test Procedure**

- 1580 • Connect the DUT Lane 0 to the RTB, leaving the DUT power turned off.
- 1581 • Configure the DSO to capture the DUT's LP-111 Initialization period on Lane 0.
- 1582 • Power on the DUT.
- 1583 • Verify that the DSO was able to successfully capture the Initialization period.
- 1584 • Measure the LP-111 Initialization period duration ($T_{INIT,MASTER}$), as described above.
- 1585 • Repeat the previous five steps for all other Lanes.

1586 **Observable Results**

- 1587 • For all Lanes, verify that $T_{INIT,MASTER}$ is no less than 100us.

1588 **Possible Problems**

1589 Note that because the $T_{INIT,MASTER}$ period may be much longer than 100us in some cases, it may not be
1590 possible to capture the entire LP-111 period within the available memory depth of the DSO. In these cases,
1591 other acquisition methods may be used (e.g., segmented capturing) to determine when the LP-111 start and
1592 end times occur, without requiring the entire LP-111 state to be captured in a single waveform.

1593 Also, care should be taken to verify that no other unexpected LP transitions or glitches occur before the LP-
1594 111 Initialization sequence occurs (as if there are any unexpected sequences sent, they could potentially
1595 affect interoperability with other devices.)

Test 1.3.2 ULPS Exit: Transmitted T_{WAKEUP} Interval

Purpose

To verify that the DUT transmits Mark-1 for the proper duration (T_{WAKEUP}) when initiating a ULPS Exit sequence.

References

- [1] C-PHY Specification, Section 6.6.3
- [2] Ibid, Table 18

Resource Requirements

See Annex A.

Last Technical Modification

October 27, 2014

Discussion

The C-PHY Specification defines a mechanism for bringing Lanes out of the ULPS state. This process involves driving a Mark-1 state (LP-100) for a minimum time T_{WAKEUP} , followed by a Stop state (LP-111), which should be detected by the Slave device. (Note that this test is only applicable to Master DUTs.)

The specification states[1],

If the Ultra-Low Power State entry command is sent after an escape mode entry command, the lane shall enter the Ultra-Low Power State (ULPS). This command shall be flagged to the receive side protocol. During this state, the lines are in the space state (LP-000). Ultra-Low Power State is exited by means of a Mark-1 state with a length t_{WAKEUP} followed by a Stop state. Annex A describes an example of an exit procedure and a procedure to control the length of time spent in the Mark-1 state. *{paragraph copied from D-PHY}*

Figure 1.3.2-1: T_{WAKEUP} Specification Definition

The specification also gives conformance limits for T_{WAKEUP} [2],

t_{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1		ms	2
--------------	---	---	--	----	---

Figure 1.3.2-2: T_{WAKEUP} Conformance Limits

The purpose of this test is to verify that a DUT transmits Mark-1 for the minimum required duration when initiating a ULPS exit on any Lane. Note that the termination environment is not critical to this measurement, and either the CLOAD fixture, RTB, or no termination fixture may be used. The DUT will be instructed to put all Lanes into ULPS mode, and then subsequently initiate a ULPS exit on all Lanes, allowing the Mark-1 duration to be observed. For each Lane, T_{WAKEUP} is measured from the start of the Mark-1 state (at the point where the V_A line of LP-100 transition crosses $V_{IH,MIN} = 740mV$), to the start of the Stop state (at the point where the V_C line of LP-111 transition crosses $V_{IH,MIN} = 740mV$).

Note that the generation and timing control of the T_{WAKEUP} interval may be implemented in the protocol layer logic for some DUT types. Therefore, if a DUT is not designed to contain this logic (e.g., for a bare-phy DUT with a PPI or other exposed protocol interface), this test is considered Not Applicable.

For each Lane, the measured T_{WAKEUP} value should be greater than or equal to 1ms.

1625 Test Setup

1626 See Annex B.1.1 (or B.1.2).

1627 Test Procedure

- 1628 • Connect the DUT Lane 0 to the RTB.
- 1629 • Configure the DSO's trigger to observe the T_{WAKEUP} for Lane 0.
- 1630 • Configure the DUT to transmit a ULPS Entry sequence followed by a Mark-1 ULPS Exit
- 1631 sequence.
- 1632 • Capture the ULPS Exit sequence on the DSO.
- 1633 • Measure T_{WAKEUP} for the ULPS Exit sequence as described above.
- 1634 • Repeat the previous five steps for all other Lanes.

1635 Observable Results

- 1636 • For all Lanes, verify that T_{WAKEUP} is greater than or equal to 1ms.

1637 Possible Problems

1638 See Possible Problems of Test 1.3.1 regarding capturing/measuring of intervals that are longer than the
1639 DSO memory depth. The same applies to this test.

Test 1.3.3 BTA: TX-Side T_{TA-GO} Interval Value

Purpose

To verify that the DUT drives the Bridge state (LP-000) for the proper period (T_{TA-GO}), when handing off control of the Link during a Link Turnaround procedure.

References

[1] C-PHY Specification, Figure 26

[2] Ibid, Table 18

Resource Requirements

See Annex A.

Last Technical Modification

June 18, 2014

Discussion

The Link Turnaround process consists of a LP handshake/handoff procedure between the Master and Slave sides of the Link. The controlling ('TX-Side') device initiates the handoff process by signaling Stop/LP-Rqst/Bridge/LP-Rqst/Stop (LP-111/100/000/100/000). The receiving ('RX-Side') device then assumes control of the link, simultaneously driving the Bridge state (LP-000), followed by its own LP-Rqst and Stop states (LP-100/111), after which the transfer process is considered complete. A picture of the entire Turnaround procedure, which shows the T_{TA-GO} interval, is shown below[1]:

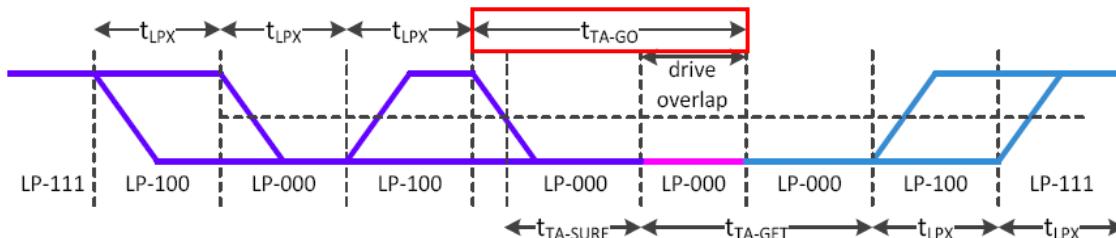


Figure 1.3.3-1: T_{TA-GO} Interval

The specification defines T_{TA-GO} as[2],

t_{TA-GO}	Time that the transmitter drives the Bridge state (LP-000) before releasing control during a link turnaround.	$4 \cdot t_{LPX}$		2
-------------	---	-------------------	--	---

Figure 1.3.3-2: T_{TA-GO} Specification Definition and Conformance Requirements

Therefore, the T_{TA-GO} period begins at the start of the last TX-Side LP-000 state (i.e., where V_{DP} crosses below $V_{IL,MAX}$ (550mV)), and ends when the TX-Side device ceases transmission (during the 'drive overlap' period, above).

If the exact point cannot be observed, an alternative methodology would require measuring the entire time interval from the end of the last TX-Side LP-100 to the beginning of the first RX-Side LP-100, then subtracting one nominal RX-Side t_{LPX} interval (measured separately). The remaining value would be T_{TA-GO} .

12-Feb-2016

1666 GO. (Note this methodology is not used in the formal test procedure defined below, but is mentioned here
1667 only for informative purposes.)

1668 Note also that this test is specific to the device *that is handing off control of the Link*. For Master DUTs
1669 (e.g., Host Processors), the measurement can be performed by initiating a single Turnaround operation from
1670 the Master device. For Slave DUTs (e.g., displays), the Link must first be turned around once (putting the
1671 Slave device in control). Then, a second Turnaround operation must be performed to transfer control back
1672 to the Master, where the measurement is made on the Slave's transmitted signaling while it is acting as the
1673 TX-Side device.

1674 The specification states that T_{TA-GO} must be greater than or equal to $4*T_{LPX}$ ns in order to be considered
1675 conformant [2], where T_{LPX} is the average LP state duration of the DUT. (Note that for Master DUT's, this
1676 should be the T_{LPX} result measured in Test 1.2.1. However, in cases where Test 1.2.1 is not performed (e.g.,
1677 for a Display (Slave) DUT), T_{LPX} can be measured from the LP states of the Turnaround sequence itself,
1678 during the states where the DUT is operating as the TX-Side device.)

1679 **Test Setup**

1680 See Annex B.1.3.

1681 **Test Procedure**

- 1682 • Connect the DUT to the Test Setup.
- 1683 • Create an event that causes the Master to initiate a Turnaround sequence.
- 1684 • If the DUT is a Master device, capture the Turnaround sequence on the DSO, and measure T_{TA-GO}
1685 for the Master device, as described above. (Otherwise continue to next step.)
- 1686 • If the DUT is a Slave device, the Slave DUT should eventually initiate another Turnaround
1687 sequence on its own, to return control back to the Master. Capture this second Turnaround
1688 sequence on the DSO, and measure T_{TA-GO} for the Slave device, as described above.

1689 **Observable Results**

- 1690 • Verify that the DUT's T_{TA-GO} interval is greater than or equal to $4*T_{LPX}$ ns.

1691 **Possible Problems**

1692 Note that in practical situations, the end point of the drive overlap period may not be easily observable,
1693 particularly if the Master and Slave devices both use similar LP-0 voltage levels (i.e., V_{OL}). However, the
1694 observability of the drive overlap period can be improved by configuring the Master and/or Slave devices
1695 to use different (but still valid) V_{OL} levels, if such configuration capability is available.

1696 Also, this test is generally intended to be performed manually (e.g., using DSO cursors to measure the
1697 timings on the captured waveform), as the measurement start/end points may be difficult to reliably
1698 determine using algorithmic methods.

Test 1.3.4 BTA: RX-Side $T_{TA-SURE}$ Interval Value

Purpose

To verify that the DUT waits the required period ($T_{TA-SURE}$) while observing the TX-Side Bridge state (LP-000), when receiving control of the Link during a Link Turnaround procedure.

References

- [1] C-PHY Specification, Figure 26
- [2] Ibid, Table 18
- [3] Ibid, Table 14

Resource Requirements

See Annex A.

Last Technical Modification

June 18, 2014

Discussion

The Link Turnaround process consists of a LP handshake/handoff procedure between the Master and Slave sides of the Link. (Note that ‘Master’ is defined as the device that supplies the HS Clock.) The controlling (‘TX-Side’) device initiates the handoff process by signaling Stop/LP-Rqst/Bridge/LP-Rqst/Stop (LP-111/100/000/100/000). The receiving (‘RX-Side’) device then assumes control of the link, simultaneously driving the Bridge state (LP-000), followed by its own LP-Rqst and Stop (LP-100/111), after which the transfer process is considered complete. A picture of the entire Turnaround procedure (reproduced from the C-PHY specification), showing the $T_{TA-SURE}$ interval, is shown below[1].

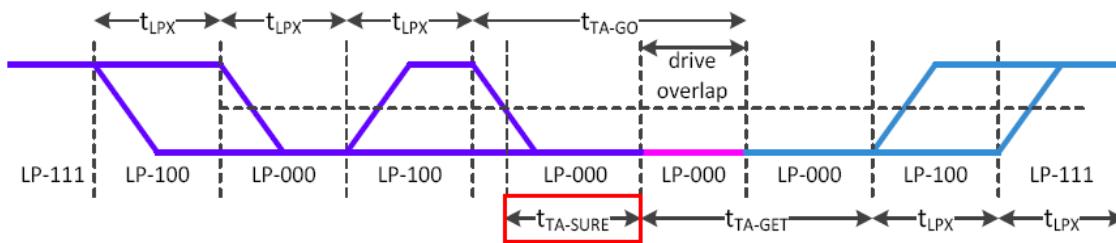


Figure 1.3.4-1: $T_{TA-SURE}$ Interval

The specification defines $T_{TA-SURE}$ as[2],

$t_{TA-SURE}$	Time that the new transmitter waits after the LP-100 state before transmitting the Bridge state (LP-000) during a link turnaround.	t_{LPX}	$2 \cdot t_{LPX}$	ns	2
---------------	--	-----------	-------------------	----	---

Figure 1.3.4-2: $T_{TA-SURE}$ Specification Definition

1721 Also, according to the specification, the $T_{TA-SURE}$ interval start is defined as[3],

1722 Drives Bridge state (LP-000) for time t_{TA-GO}	Observes the transition from LP-100 to Bridge state and waits for time $t_{TA-SURE}$. After correct completion of this time-out this side knows it is in control.
---	--

Figure 1.3.4-3: $T_{TA-SURE}$ Specification Definition

1723 $T_{TA-SURE}$ ends when the RX-Side begins transmission during the ‘drive overlap’ period (see above). Note
 1724 this starting point is technically slightly different from the T_{TA-GO} interval test, and starts when the RX-Side
 1725 device *observes the transition to the Bridge state*, not when the transition itself begins. However, as this
 1726 time point cannot be externally observed, the best reasonable estimate is to use the time point where the
 1727 voltage crosses the maximum allowable RX Logic 0 threshold (550mV). This is the earliest point at which
 1728 the RX-Side device could ‘see’ the transition (assuming its actual Logic 0 RX threshold were set to the
 1729 maximum allowable value of 550mV).

1730 Note also that this test is specific to the device *that is being handed control of the Link*. For Slave DUTs
 1731 (e.g., displays), the measurement can be performed by initiating a single Turnaround operation from the
 1732 Master device. For Master DUTs (e.g., host processors or camera sensors), the Link must first be turned
 1733 around once (putting the Slave device in control). Then, a second Turnaround operation must be performed
 1734 to transfer control back to the Master, where the measurement is made while the Master is acting as the
 1735 RX-Side device.

1736 The specification states that $T_{TA-SURE}$ must be between $1*T_{LPX}$ and $2*T_{LPX}$ ns in order to be considered
 1737 conformant [1], where T_{LPX} is the average LP state duration of the DUT. (Note that for Master DUT’s, this
 1738 should be the T_{LPX} result measured in Test 1.2.1. However, in cases where Test 1.2.1 is not performed (e.g.,
 1739 for a Display (Slave) DUT), T_{LPX} can be measured from the LP states of the Turnaround sequence itself,
 1740 during the states where the DUT is operating as the TX-Side device.)

1741 **Test Setup**

1742 See Annex B.3.1.

1743 **Test Procedure**

- 1744 • Connect the DUT Lane 0 to the RTB.
- 1745 • Create an event that causes the Master to initiate a Turnaround sequence.
- 1746 • If the DUT is a Slave device, capture the Turnaround sequence on the DSO, and measure $T_{TA-SURE}$
 1747 for the Slave device, as described above. (Otherwise continue to next step.)
- 1748 • If the DUT is a Master device, the Slave should eventually initiate another Turnaround sequence
 1749 on its own, to return control back to the Master. Capture this second Turnaround sequence on the
 1750 DSO, and measure $T_{TA-SURE}$ for the Master device, as described above.

1751 **Observable Results**

- 1752 • Verify that the $T_{TA-SURE}$ interval is between $1*T_{LPX}$ and $2*T_{LPX}$ ns.

1753 **Possible Problems**

1754 See Possible Problems comments for Test 1.3.3, regarding improving the visibility of the drive overlap
 1755 period. The same comments apply to this test.

Test 1.3.5 BTA: RX-Side T_{TA-GET} Interval Value

Purpose

To verify that the DUT drives the Bridge state (LP-000) for the required period (T_{TA-GET}), when receiving control of the link during a Link Turnaround procedure.

References

[1] C-PHY Specification, Figure 26

[2] Ibid, Table 18

Resource Requirements

See Annex A.

Last Technical Modification

June 18, 2014

Discussion

The Link Turnaround process consists of a LP handshake/handoff procedure between the Master and Slave sides of the Link. (Note that ‘Master’ is defined as the device that supplies the HS Clock.) The controlling (‘TX-Side’) device initiates the handoff process by signaling Stop/LP-Rqst/Bridge/LP-Rqst/Stop (LP-111/100/000/100/000). The receiving (‘RX-Side’) device then assumes control of the link, simultaneously driving the Bridge state (LP-000), followed by its own LP-Rqst and Stop (LP-100/111), after which the transfer process is considered complete. A picture of the entire Turnaround procedure (reproduced from the C-PHY Specification), showing the T_{TA-GET} interval, is shown below[1].

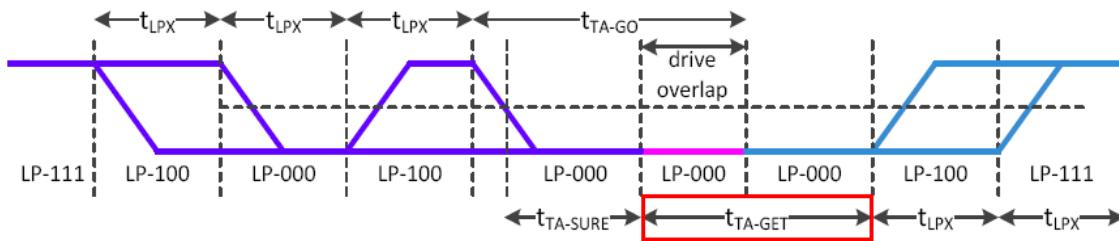


Figure 1.3.5-1: T_{TA-GET} Interval

The specification defines T_{TA-GET} as[2],

t_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-000) after accepting control during a link turnaround.	$5 \cdot t_{LPX}$		2
--------------	--	-------------------	--	---

Figure 1.3.5-2: T_{TA-GET} Definition and Conformance Limits

Therefore, the T_{TA-GET} period begins at the point where the RX-Side device begins simultaneous driving of the LP-00 state (i.e., the ‘drive overlap’ period, above), and ends at the end of the LP-00 state (or more accurately, the beginning of the LP-10 state, which begins where the V_{DP} signal crosses $V_{IH,MIN}$ (880mV)). (Note that this point is not accurately drawn in the figure above.)

Note also that this test is specific to the device *that is being handed control of the Link*. For Slave DUTs (e.g., displays), the measurement can be performed by initiating a single Turnaround operation from the

1783 Master device. For Master DUTs (e.g., host processors), the Link must first be turned around once (putting
1784 the Slave device in control). Then, a second Turnaround operation must be performed to transfer control
1785 back to the Master, where the measurement is made while the Master is acting as the RX-Side device.

1786 The specification states that T_{TA-GET} must be greater than $5*T_{LPX}$ ns in order to be considered
1787 conformant[2], where T_{LPX} is the average LP state duration of the DUT. (Note that for Master DUT's, this
1788 should be the T_{LPX} result measured in Test 1.2.1. However, in cases where Test 1.2.1 is not performed (e.g.,
1789 for a Display (Slave) DUT), T_{LPX} can be measured from the LP states of the Turnaround sequence itself,
1790 during the states where the DUT is operating as the TX-Side device.)

1791 **Test Setup**

1792 See Annex B.1.3.

1793 **Test Procedure**

- 1794 • Connect the DUT Lane 0 to the RTB.
- 1795 • Create an event that causes the Master to initiate a Turnaround sequence.
- 1796 • If the DUT is a Slave device, capture the Turnaround sequence on the DSO, and measure T_{TA-GET}
1797 for the Slave device, as described above. (Otherwise continue to next step.)
- 1798 • If the DUT is a Master device, the Slave should eventually initiate another Turnaround sequence
1799 on its own, to return control back to the Master. Capture this second Turnaround sequence on the
1800 DSO, and measure T_{TA-GET} for the Master device, as described above.

1801 **Observable Results**

- 1802 • Verify that the T_{TA-GET} interval is greater than or equal to $5*T_{LPX}$ ns.

1803 **Possible Problems**

1804 See Possible Problems comments for Test 1.3.3, regarding improving the visibility of the drive overlap
1805 period. The same comments apply to this test.

This page intentionally left blank.

Section 2 RX Timers and Electrical Tolerances

Overview

This section of tests verifies various RX signaling voltage and timing requirements of C-PHY transceivers, defined in [\[MIPI01\]](#).

Comments and questions regarding the documentation and/or implementation of these tests are welcome, and can be sent to test-wg@mipi.org.

Group 1 LP-RX Voltage and Timing Requirements

Overview

This group of tests verifies the LP-RX voltage and timing electrical requirements defined in Section 9.2.2 of the C-PHY Specification.

Status

The test names, Discussion sections, and Procedures are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

Test 2.1.1 LP-RX Logic 1 Input Voltage (V_{IH})

Purpose

To verify that the DUT's LP receiver can properly detect Logic 1 voltage levels as low as the minimum required conformance limit (V_{IH}).

References

- [1] C-PHY Specification, Section 9.2.2
- [2] Ibid, Table 25

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for V_{IH} , or LP-RX Logic 1 Input Voltage.

The specification states[1],

1142 The input high-level voltage, V_{IH} , is the voltage at which the receiver is required to detect a high state in the
 1143 input signal. In order to reduce noise sensitivity on the received signal, an LP receiver shall incorporate a

Figure 2.1.1-1: V_{IH} Specification Definition

1834 The specification also provides a table, which shows the V_{IH} requirements[2].

Table 28 LP Receiver DC specifications {copy of D-PHY Table 22}

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IH}	Logic 1 input voltage	740			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
V_{IL-ULP}	Logic 0 input voltage, ULP State			300	mV	
V_{HYST}	Input hysteresis	25			mV	

Figure 2.1.1-2: V_{IH} Conformance Requirements

1836 The test pattern used for this measurement will be based on a generic valid data stream, which will be used
 1837 to construct a valid test sequence specific to the DUT. (Note that this test sequence must be created for the
 1838 DUT prior to performing this test, according to the specific configuration and image data/timing
 1839 requirements for the DUT.) This test sequence contains any necessary initialization and configuration
 1840 sections, followed by a repeating image data sequence. For this test, the LP-111 levels for all sections will
 1841 be set to a nominal value (1.2V), and the sequence will be sent to the DUT. Once the DUT has been
 1842 verified to be receiving the continuously looping image data sequence properly, the LP-111 voltage level
 1843 for all Lanes will be decreased simultaneously until the DUT begins to show errors.

1844 Note that the specific observable for this test will vary depending on the DUT type and supported
 1845 capabilities. An example of an observable behavior for a “bare phy” implementation would be the probing
 1846 of an internal (or PPI-side) LP data signal using a DSO or Logic Analyzer, and verifying that the received

1847 data matches the test pattern data. An example for an integrated CSI-2 or DSI receiver would be to monitor
1848 the DUT's reception of the data via internal error detection capabilities (e.g., CRC counters). For cases
1849 where CRC error detection is not available, visual verification of the image itself may be used as the
1850 observable (e.g., viewing the image output of an LCD display.) Note that a full discussion of the various
1851 options for RX test observables is presented in Annex F of this document.

1852 The lowest voltage at which the DUT consistently detects LP Logic 1 levels correctly (i.e., receives the
1853 image data without error) shall be recorded as the LP-RX Logic-1 Detection Threshold. This value will be
1854 varied and measured simultaneously for V_A , V_B , and V_C of all Lanes.

1855 The DUT's LP-RX Logic-1 Detection Threshold must be less than or equal to 740mV in order to satisfy the
1856 conformance requirements for V_{IH} [2]. This demonstrates that the DUT can detect logic levels at least as
1857 low as 740mV, which is the minimum voltage level a receiver is required to detect as a Logic 1.

1858 **Test Setup**

1859 See Annex B.2.

1860 **Test Procedure**

- 1861 • Connect the DUT to the Test System.
- 1862 • Configure the Test System to generate a suitable master test sequence with voltage levels $V_{OH} =$
1863 1.2V, and $V_{OL} = 0V$ on the V_A , V_B , and V_C Lines of all Lanes.
- 1864 • Transmit the test sequence to the DUT.
- 1865 • Verify via any valid observable that the DUT received the image data without errors.
- 1866 • While the DUT is receiving the continuously looping image data sequence, slowly decreasing the
1867 Test System's V_{OH} level for V_A , V_B , and V_C of all Lanes until the DUT indicates errors in the
1868 received data.
- 1869 • Record the V_{IH} result for this test case as the lowest Test System V_{OH} value at which the DUT
1870 consistently received the test sequence without errors.

1871 **Observable Results**

- 1872 • Verify that V_{IH} is less than or equal to 740mV.

1873 **Possible Problems**

1874 None.

Test 2.1.2 LP-RX Logic 0 Input Voltage, Non-ULP State (V_{IL})**Purpose**

To verify that the DUT's LP receiver can correctly detect Logic 0 voltage levels as high as the maximum required conformance limit (V_{IL}), when in the non-ULP state.

References

[1] C-PHY Specification, Section 9.2.2

[2] Ibid, Table 25

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for V_{IL} , or LP-RX Logic 0 Input Voltage.

The specification states[1],

1138 The input low-level voltage, V_{IL} , is the voltage at which the receiver is required to detect a low state in the
1139 input signal. A lower input voltage, $V_{IL-ULPS}$, may be used when the receiver is in the Ultra-Low Power State.

Figure 2.1.2-1: V_{IL} Specification Definition

(Note a different and lower input voltage, $V_{IL-ULPS}$, may be used when the receiver is in the ULP state. See Test 2.1.3).

The procedure for this test is similar to the one used for the LP-RX Logic 1 Input Voltage test (see Test 2.1.1), except that the Logic 1 level (V_{OH}) of the test stimulus signal will be held fixed for this test, while the Logic 0 level (V_{OL}) is slowly increased from a starting value of 0V, to find the point where the DUT no longer consistently detects a Logic 0 correctly. The DUT will not be in ULPS mode when the test stimulus is applied. The maximum voltage level at which the DUT consistently detects all LP Logic 0 levels correctly shall be recorded as the V_{IL} result. This value will be measured simultaneously for the V_A , V_B , and V_C lines of all Lanes.

(Note that the exact stimulus pattern and observable mechanism for this test will depend heavily on the DUT type, and the optimal stimulus/observables must be determined in advance for a given DUT before the test can be performed. See Discussion section of Test 2.1.1, and also Appendices C and G for more details.)

For each test case, the measured V_{IL} result must be greater than or equal to 550mV in order to satisfy the conformance requirements for V_{IL} , as this demonstrates that the DUT can detect logic 0 levels up to at least 550mV, which is the maximum voltage level a receiver is required to detect as a Logic 0, when *not* in the ULP state[2].

Test Setup

See Annex B.2.

1909 Test Procedure

- 1910 • Connect the DUT to the Test System.
- 1911 • Configure the Test System to generate a suitable test sequence with LP voltage levels $V_{OH} = 1.2V$,
1912 and $V_{OL} = 0V$ on all Lanes.
- 1913 • Transmit the test sequence to the DUT.
- 1914 • Verify that the DUT received the test sequence without errors.
- 1915 • Repeat the previous three steps, slowly increasing the Test System's V_{OL} level for V_A , V_B , and V_C
1916 of all Lanes for each iteration until the DUT indicates errors.
- 1917 • Record the V_{IL} result for this test case as the highest V_{OL} value at which the DUT consistently
1918 received the test sequence without errors.

1919 Observable Results

- 1920 • Verify that V_{IL} is greater than or equal to 550mV.

1921 Possible Problems

1922 None.

Test 2.1.3 LP-RX Input Hysteresis (V_{HYST})

Purpose

To verify that the Input Hysteresis value (V_{HYST}) of the DUT's LP receiver is within the conformance limits.

References

- [1] C-PHY Specification, Section 9.2.2
- [2] Ibid, Table 28

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for V_{HYST} , or Input Hysteresis. The Hysteresis is incorporated into LP receivers to reduce sensitivity to noise, and prevents Logic state changes due to short-term, low amplitude excursions below the V_{IH} Logic-1 threshold (or above V_{IL} Logic-0 threshold), after the instantaneous voltage has initially crossed the threshold for any given bit interval.

The specification states[1],

- 1143 input signal. In order to reduce noise sensitivity on the received signal, an LP receiver shall incorporate a
- 1144 hysteresis. The hysteresis voltage is defined as V_{HYST} .

Figure 2.1.3-1: V_{HYST} Specification Definition

The specification also provides limits for V_{HYST} , as shown below[2].



Figure 2.1.3-2: V_{HYST} Conformance Requirements

Note that multiple possible methodologies exist for performing this test, depending on the observability and access provided by the DUT to internal state signals for the LP logic levels. This typically will depend heavily on the DUT type, however if the DUT provides suitable access to the proper internal monitoring capability, the test setup and procedure can be greatly simplified. If the DUT does not provide access to this capability, it may still be possible to perform the test using an alternate methodology, which requires a more complex test setup.

For the purposes of this test suite, two different methodologies will be defined, which will be referred to as the Static method, and the Dynamic method. The preferred (and simpler) approach is the Static method, however this approach requires the DUT to provide a proprietary means to instantaneously monitor the internal detected LP logic level for a given line (either physically via a dedicated signal pin, or through software, by monitoring a register or other status indicator in real-time). Dedicated signal pins are almost always available for PPI-based DUT's, or DUTs that have any sort of hardware debug bus capability whereby the internal LP logic state of any given line may be directly monitored using an oscilloscope that is physically connected to the logic signal pin. Host implementations are frequently capable of providing internal LP state monitoring capability via software-driven means.

1958 Static Method:

1959 In the Static approach, the voltage of a static LP level presented at the C-PHY LP-RX input pins of the
1960 DUT can be set to a nominal LP-0 or LP-1 level (0mV or 1200mV, depending on whether the hysteresis of
1961 the V_{IH} or V_{IL} threshold is being measured, respectively.) (Note for this example, verification of the V_A V_{IH}
1962 hysteresis will be described, thus the initial applied static LP level will be set to 0mV.) With the applied
1963 static voltage set to 0mV, it will then be slowly increased in order to determine the point where the internal
1964 LP logic state signal (monitored separately) indicates a change to the opposite LP state (LP-1, in this case).
1965 The applied LP voltage that causes this state change will be recorded as V_1 , and the applied LP voltage will
1966 be increased approximately another 50-100mV beyond this point. With the internal LP state now indicating
1967 LP-1, the applied LP voltage will then be slowly varied back in the opposite direction, to see if the internal
1968 LP logic level maintains its state as the applied voltage crosses back below V_1 . At some point less than V_1 ,
1969 the internal LP logic state will indicate a change back to LP-0, for which the applied voltage will be
1970 recorded as V_2 . V_{HYST} for the V_{IH} threshold of the V_A line will be mathematically computed and reported as
1971 $V_{HYST-VIH}(V_A) = |V_1 - V_2|$.

1972 The entire procedure above will then be repeated to measure V_{HYST} for the V_A V_{IL} threshold (i.e., $V_{HYST-VIL}(V_A)$), and then two additional times each for the V_B and V_C lines to get $V_{HYST-VIH}(V_B)$, $V_{HYST-VIL}(V_B)$,
1973 $V_{HYST-VIH}(V_C)$, $V_{HYST-VIL}(V_C)$. For all six cases, V_{HYST} must be $\geq 25mV$ in order to be considered
1974 conformant[2].

1976 Dynamic Method:

1977 For cases where the DUT does not provide access to any kind of internal LP logic state monitoring
1978 capability (which is typically the case for DSI receivers, e.g., display panels), it may be possible to employ
1979 a different methodology to measure V_{HYST} . This approach uses a simulated noise signal, which is applied
1980 additively by the Test System to either the V_A , V_B , or V_C signals while the Test System is configured to
1981 transmit a valid LP sequence that causes an observable result. However in this case the LP-1 and LP-0
1982 levels of the Test System will be set to the minimum/maximum V_{IH}/V_{IL} values measured for the DUT in
1983 Tests 2.1.1 and 2.1.2, respectively. Once the DUT is verified to successfully receive the test sequence
1984 without error under these conditions, the additive simulated noise signal will be turned on for either the V_A ,
1985 V_B , or V_C line, and the DUT will be observed to determine whether or not it is still able to successfully
1986 receive the test sequence in the presence of the additive noise, which is calibrated to cause momentary
1987 excursions of approximately 25mV below/above the V_{IH}/V_{IL} thresholds, respectively. If the DUT does not
1988 implement some form of hysteresis on its LP-RX in this case, the presence of the additive noise should
1989 cause errors in the received data.

1990 The additive noise signal must be injected into the V_A , V_B , or V_C lines using a similar test setup to that used
1991 for an LP-RX Interference Tolerance test, except that for that test, the interference is added common-mode,
1992 i.e., to V_A , V_B , or V_C simultaneously. For this test, the simulated noise must be added single-endedly to
1993 either V_A , V_B , or V_C (depending on which line is being tested), otherwise it would be treated as common-
1994 mode noise by the LP-RX, and will potentially be filtered out. This filtering should not occur however, if
1995 the noise is applied single-endedly.

1996 The recommended characteristics for the additive noise signal is to use a square-wave or sine-wave signal
1997 with a period what is approximately 2.3x the T_{LPX} value of the applied test sequence. This will modulate the
1998 phase of the additive noise with respect to the LP data test sequence, for added impact. The amplitude of
1999 the additive noise should be calibrated to produce an approximately 25mVpk (50mVpp) deviation from the
2000 nominal LP-0/1 levels of the Test System (which will be set to the measured V_{IH} and V_{IL} values for the
2001 DUT). When the additive noise is enabled, the DUT should still be able to successfully receive the LP test
2002 sequence without error, if it employs sufficient hysteresis on its LP-RX.

2003 Note that when the test is performed, the amplitude of the additive noise can be increased to find the actual
2004 V_{HYST} value (i.e., by increasing to the point where the DUT starts to indicate errors, and measuring the peak
2005 magnitude of the applied additive noise at the DUT receiver as V_{HYST}). However, note that one limitation to
2006 this approach is that typically it may not be possible to measure V_{HYST} for V_{IH} and V_{IL} separately, unless the
2007 additive noise can be applied selectively to only to the LP-1 or LP-0 states (which would require suitably

2008 capable signal generation equipment). Otherwise the measurement will produce a single common V_{HYST}
 2009 result for both V_{IH} and V_{IL} .

2010 Regardless of the methodology used, the measured V_{HYST} values for V_A , V_B , and V_C of all measured Lanes
 2011 must be greater than 25mV in order to be considered conformant [2].

2012 **Test Setup**

2013 See Annex B.2.

2014 **Test Procedure (Option 1: Static Method)**

- 2015 • Connect the DUT to the Test System.
- 2016 • Configure the Test System to generate static LP-0 levels with $V_{OL} = 0\text{mV}$ for the V_A , V_B , and V_C
 2017 lines of Lane 0.
- 2018 • Using the DUT's proprietary capability, monitor the DUT's internal detected LP logic states for
 2019 the V_A , V_B , and V_C lines, and verify that they are both reported as LP-0.
- 2020 • Slowly increase the V_{OL} level of the Test System to the point where the DUT's reported internal
 2021 LP logic states change from LP-0 to LP-1 for V_A , V_B , and V_C , and record the voltages as $V_1(V_A)$,
 2022 $V_1(V_B)$, and $V_1(V_C)$. (Note: This point should be consistent with the V_{IH} value that was measured
 2023 in Test 2.1.1.) The values should be measured and recorded separately for V_A , V_B , and V_C ,
 2024 however the values should typically be nearly identical.
- 2025 • Continue to increase the Test System's V_{OL} (now V_{OH}) value to approximately 100mV beyond V_1 .
 2026 Then begin slowly decreasing the V_{OH} level, while still monitoring the reported internal LP logic
 2027 state (which should still be reported as LP-1 for V_A , V_B , and V_C).
- 2028 • Continue decreasing V_{OH} until the reported internal LP logic states for V_A , V_B , and V_C change
 2029 from LP-1 to LP-0. Record these voltages as $V_2(V_A)$, $V_2(V_B)$ and $V_2(V_C)$.
- 2030 • Compute the V_{IH} hysteresis for the V_A line as $V_{HYST-VIH}(V_A) = V_1(V_A) - V_2(V_A)$.
- 2031 • Compute the V_{IH} hysteresis for the V_B line as $V_{HYST-VIH}(V_B) = V_1(V_B) - V_2(V_B)$.
- 2032 • Compute the V_{IH} hysteresis for the V_C line as $V_{HYST-VIH}(V_C) = V_1(V_C) - V_2(V_C)$.

2033 Repeat the above procedure a second time (but starting from a nominal LP-1 level of 1200mV, and working
 2034 downward) to measure the V_{IL} hysteresis for V_A , V_B , and V_C , i.e., $V_{HYST-VIL}(V_A)$, $V_{HYST-VIL}(V_B)$, and $V_{HYST-
 2035 VIL}(V_C)$. (Note however in this case V_{HYST} will be computed as $|V_1 - V_2|$.)

2036 Repeat all of the above steps for all Lanes.

2037 **Test Procedure (Option 2: Dynamic Method)**

- 2038 • Connect the DUT to the Test System.
- 2039 • Configure the Test System to generate a suitable LP sequence that produces an observable result
 2040 (e.g., a LPDT command or image data sequence on Data Lane 0), and configure the Test System's
 2041 V_{OH} and V_{OL} levels for all Lanes to the V_{IH} and V_{IL} values that were measured in Tests 2.1.1 and
 2042 2.1.2, respectively.
- 2043 • With the additive noise source disabled, transmit the test sequence the DUT, and verify (via the
 2044 appropriate observable) that the test sequence was received without error.
- 2045 • Repeat the previous step, but with the additive noise source enabled for the V_A line, using a noise
 2046 voltage of approximately 5mVpk. Verify again that the test sequence was received without error.
- 2047 • Repeat the previous step multiple times, slowly increasing the additive noise voltage in 3-5mV
 2048 steps, until the point is reached where the DUT begins to report errors in the received test
 2049 sequence.
- 2050 • Record $V_{HYST-VIH}(V_A)$ and $V_{HYST-VIL}(V_A)$ as the maximum additive noise voltage where the test
 2051 sequence was consistently received without error.
- 2052 • Repeat the above procedure for the V_B line to determine $V_{HYST-VIH}(V_B)$ and $V_{HYST-VIL}(V_B)$.

- 2053 • Repeat the above procedure for the V_C line to determine $V_{HYST\cdot VIH}(V_C)$ and $V_{HYST\cdot VIL}(V_C)$.
2054 • Repeat all of the above steps for all Lanes.

2055 **Observable Results**

2056 For all measured Lanes:

- 2057 • Verify that $V_{HYST\cdot VIH}(V_A)$ is greater than or equal to 25mV.
2058 • Verify that $V_{HYST\cdot VIH}(V_B)$ is greater than or equal to 25mV.
2059 • Verify that $V_{HYST\cdot VIH}(V_C)$ is greater than or equal to 25mV.
2060 • Verify that $V_{HYST\cdot VIL}(V_A)$ is greater than or equal to 25mV.
2061 • Verify that $V_{HYST\cdot VIL}(V_B)$ is greater than or equal to 25mV.
2062 • Verify that $V_{HYST\cdot VIL}(V_C)$ is greater than or equal to 25mV.

2063 **Possible Problems**

2064 None.

Test 2.1.4 LP-RX Minimum Pulse Width Response (T_{MIN-RX})

Purpose

To verify that the DUT's LP receiver can detect LP pulses with the minimum required duration.

References

[1] C-PHY Specification, Section 9.2.2

[2] Ibid, Table 29

[3] Ibid, Figure 51

[4] Ibid, Table 18

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for T_{MIN-RX} , which defines the minimum-duration LP pulse width that should still be detected as a valid LP state by an LP receiver.

The specification states[1],

1145 The LP receiver shall reject any input signal smaller than e_{SPIKE} . Signal pulses wider than T_{MIN-RX} shall
 1146 propagate through the LP receiver.

Figure 2.1.4-1: T_{MIN-RX} Specification Requirement

The specification also provides conformance limits for T_{MIN-RX} [2],

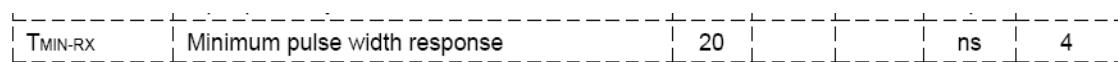


Figure 2.1.4-2: T_{MIN-RX} Conformance Limits

The specification also provides a graphic (reproduced below)[3], which shows the T_{MIN-RX} interval in relation to 2X the T_{LPX} specification (where T_{LPX} defines the minimum LP pulse width requirement for LP transmitters, i.e., the narrowest pulse one could expect to see out of any conformant LP-TX.).

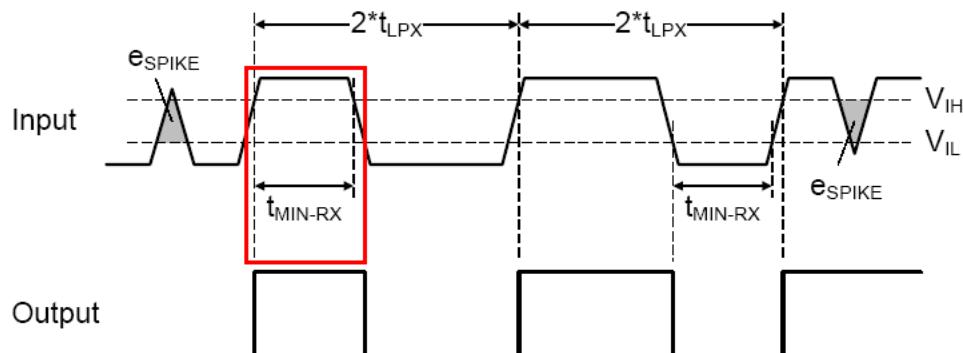


Figure 51 Input Glitch Rejection of Low-Power Receivers

Figure 2.1.4-3: T_{MIN-RX} Interval

2088 Note that the above picture can be misleading if not interpreted carefully, as it is not exactly drawn to scale.
 2089 The minimum T_{LPX} value for LP transmitters is 50ns[4], so twice this value would be 100ns. The minimum
 2090 T_{MIN-RX} value is specified to be 20ns[2], whereas in the example picture shown in the spec, the example
 2091 T_{MIN-RX} pulse appears more on the order of $1.0*T_{LPX}$, not $0.4*T_{LPX}$. In any case, a conformant LP-RX
 2092 should be able to detect LP states with durations as short as 20ns[2].

2093 In this test, the DUT's LP-RX will be sent valid LP sequences with states as short as 20ns. The DUT must
 2094 successfully detect states as short as 20ns in order to be considered conformant[2].

2095 Test Setup

2096 See Annex B.2.

2097 Test Procedure

- 2098 • Connect the DUT to the Test System.
- 2099 • Configure the Test System to generate a suitable LP test pattern with voltage levels $V_{OH} = 1.2V$,
 2100 and $V_{OL} = 0V$ on both the V_A , V_B , and V_C Lines, and with $T_{LPX} = 50ns$, on Lane 0.
- 2101 • Transmit the test sequence to the DUT.
- 2102 • Verify via any valid observable that the DUT received the test sequence without errors.
- 2103 • Repeat the previous three steps, slowly decreasing T_{LPX} for the LP states in the test sequence, until
 2104 the DUT indicates errors in the received data.
- 2105 • Record the smallest T_{LPX} value at which the DUT consistently received the test sequence without
 2106 errors.
- 2107 • Repeat the previous steps for all Lanes.

2108 Observable Results

- 2109 • Verify that the smallest T_{LPX} value for which the DUT can consistently receive the test sequence
 2110 without errors is less than or equal to 20ns.

2111 Possible Problems

2112 None.

Test 2.1.5 LP-RX Input Pulse Rejection (e_{SPIKE})

Purpose

To verify that the DUT's LP receiver rejects short-term signal glitches that are smaller than the specified conformance limit.

References

- [1] C-PHY Specification, Section 9.2.2
- [2] Ibid, Table 29
- [3] Ibid, Figure 51

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for e_{SPIKE} , which describes an LP receiver's ability to reject short-term glitches, i.e., narrow pulses with voltage levels outside of the current Logic state, but that should not change the receiver state, as their widths are sufficiently shorter than the nominal T_{LPX} interval.

The specification states[1],

- 1145 The LP receiver shall reject any input signal smaller than e_{SPIKE} . Signal pulses wider than T_{MIN-RX} shall propagate through the LP receiver.
- 1146

Figure 2.1.5-1: e_{SPIKE} Specification Definition

The specification further describes e_{SPIKE} in the following table [2],

Table 29 LP Receiver AC Specifications {copy of D-PHY Table 23}

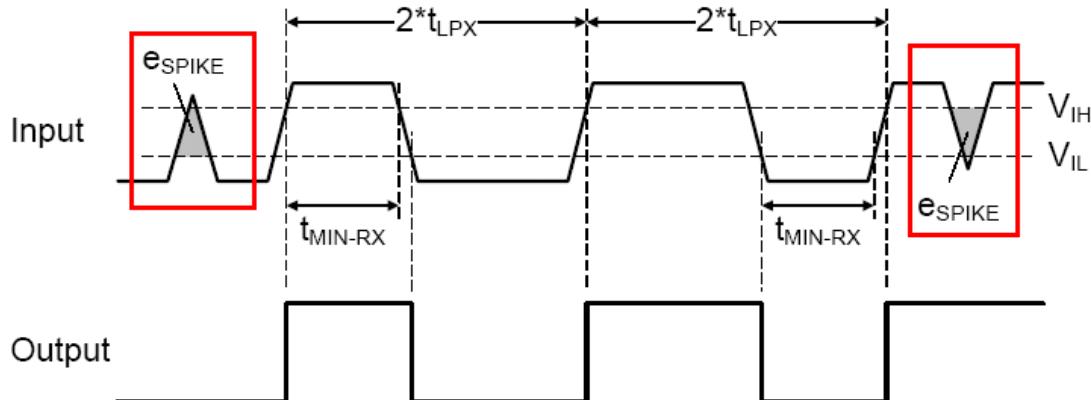
Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V·ps	1, 2, 3
T_{MIN-RX}	Minimum pulse width response	20			ns	4
V_{INT}	Peak interference amplitude			200	mV	
f_{INT}	Interference frequency	450			MHz	

Note:

1. Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state. e_{SPIKE} generation will ensure the spike is crossing both $V_{IL,MAX}$ and $V_{IH,MIN}$ levels.
2. An impulse less than this will not change the receiver state.
3. In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.
4. An input pulse greater than this shall toggle the output.

Figure 2.1.5-2: e_{SPIKE} Specification Requirements

2134 The conformance limit for e_{SPIKE} is defined in units of Volts *times* picoseconds, (V*ps), which allows for
 2135 multiple potential test cases (high voltage/short-duration, vs. low voltage/long duration). Example e_{SPIKE}
 2136 glitches are shown in the figure below[3].



2137 **Figure 51 Input Glitch Rejection of Low-Power Receivers**

Figure 2.1.5-3: Example e_{SPIKE} Glitch

2138 The general methodology for this test is similar to other LP-RX tests (e.g., send valid sequence with
 2139 proper/nominal LP voltage/timing characteristics, then modify sequence to introduce test artifact.) Again
 2140 there are multiple options for stimulus and observable, however it is beneficial to try to identify, when
 2141 possible, a sufficiently low-level mechanism that can be used with the widest variety of DUT types, and
 2142 ideally for all Lanes.

2143 For this test, one such possible mechanism could be the HS-entry sequence, which is common to all Lanes.
 2144 A proper HS entry sequence consists of LP-111, followed by LP-001 (HS-Rqst) for at least T_{LPX} , then HS-
 2145 000 (Bridge) for time $T_{HS-PREPARE}$. One possible option for this test would be to introduce a spike during the
 2146 LP-001 state, in such a way that it would disrupt RX behavior if seen as a valid level/state change by the
 2147 DUT. Note this must be done with care, and with an awareness of the T_{MIN-RX} and T_{LPX} requirements for
 2148 devices, as the three concepts are interrelated to some degree, with respect to the particular choice of
 2149 stimulus sequence for this test.

2150 Generally speaking, the methodology for this test is similar to Test 2.1.4 (LP-RX Minimum Pulse Width
 2151 Response), with some modifications: The nominal minimum T_{LPX} value of 50ns will be used for all LP
 2152 states in the stimulus sequence, and a glitch (of defined duration) will be introduced in the center of all LP
 2153 states. The approach of adding the glitch to all LP states helps to alleviate potential problems that could
 2154 arise by affecting only one state in a sequence, in which case the effects of how logical state machines will
 2155 be affected by the erroneous reception of just one state.

2156 Also, for this test, care must be given to the particular LP voltage levels used for the test. The test will be
 2157 performed using nominal LP levels ($V_{OH} = 1.2V$, and $V_{OL} = 0V$). Note that the width of the glitch in both
 2158 the positive and negative cases is not the same, as the glitch is defined in units of Volts *times* Picoseconds,
 2159 in terms of time spent *below* V_{IH} (when in LP-1), and *above* V_{IL} (when in LP-0). The cases for the different
 2160 polarities are worked out below.

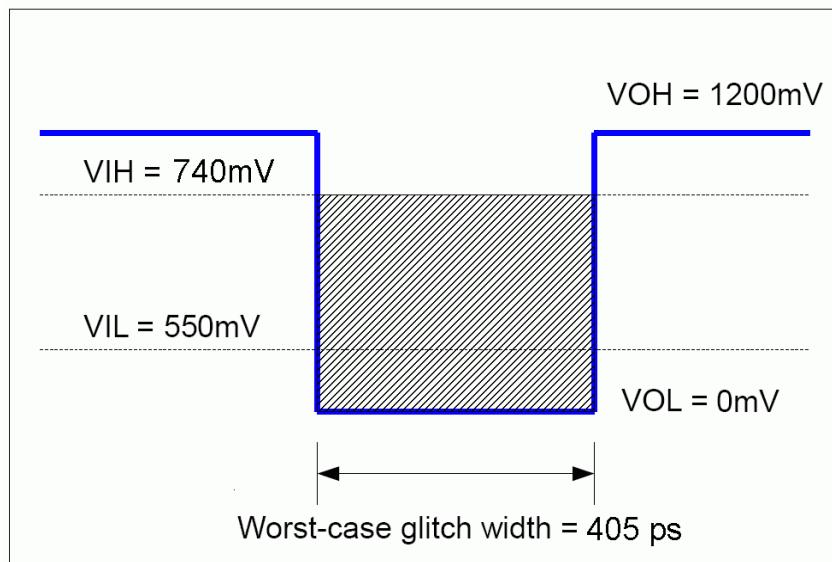
2161 Note for the purposes of this test, V_{IH} will be taken as $V_{IH,MIN} = 740mV$, and $V_{IL,MAX} =$
 2162 $550mV$, and for all test cases the magnitude of all glitches will traverse to the opposite LP voltage level.
 2163 This means a worst-case ‘negative’ glitch while in the LP-1 state would mean dipping below 740mV, down
 2164 to the whatever V_{OL} value the Test System is using. The duration of the worst-case glitch will depend on the
 2165 V_{OL} value selected. For this test, V_{OL} will be 0V.

Also note that the exact duration of the worst-case glitches will vary depending on the test system. The examples shown in the figures below are ‘ideal’ waveforms, in that the rise time is zero, and the edges are perfectly square. In reality, the pulses will have some finite slope and a non-zero rise time. Therefore, the glitch duration values shown below are only *approximate* values, as the actual widths will depend on the shape of the pulses, and the overall system rise time. What is important however, is that the area under the pulse be $300\text{V}\cdot\text{ps}$ (or slightly greater, depending on the resolution of the test system.)

Max Depth / Min Duration Glitches:

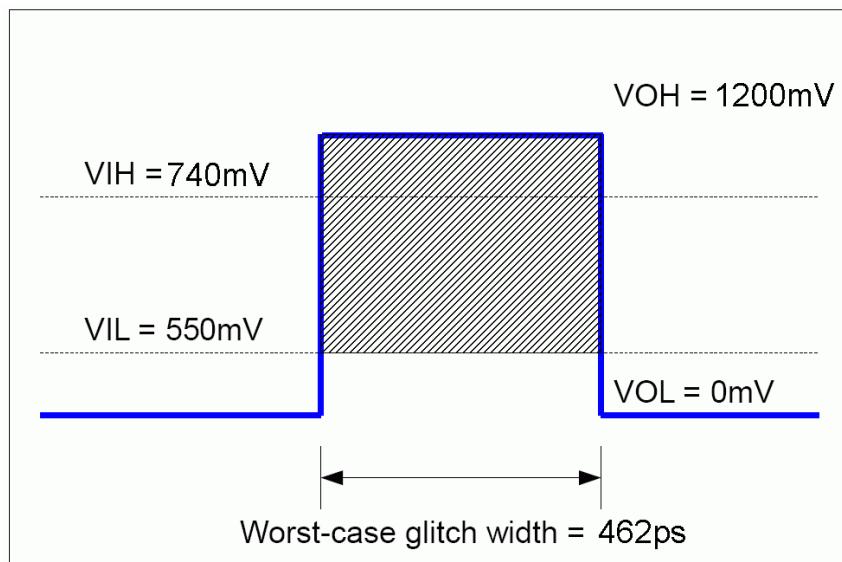
Negative glitch (740 to 0mV): Min duration is *approximately* $300/(740 - 0\text{mV}) = 405 \text{ ps}$

Positive glitch (550 to 1200mV): Min duration is *approximately* $300/(1200-550\text{mV}) = 462 \text{ ps}$



2175

Figure 2.1.5-4: Max Depth/Min Duration Negative Glitch



2176

Figure 2.1.5-5: Max Depth/Min Duration Positive Glitch

2177 **Test Setup**

2178 See Annex B.2.

2179 **Test Procedure**

- 2180 • Connect the DUT to the Test System.
- 2181 • Configure the Test System to generate a suitable test pattern with LP voltage levels $V_{OH} = 1.2V$,
2182 and $V_{OL} = 0V$ on V_A , V_B , and V_C of all Lanes, and with glitch addition disabled in the Test
2183 System.
- 2184 • Transmit the test sequence to the DUT.
- 2185 • Verify via any valid observable that the DUT received the test sequence without errors.
- 2186 • Reconfigure the Test System to enable the addition of $300V \cdot ps$ LP glitches to all LP states of all
2187 Lanes, while still keeping $V_{OH} = 1.2V$, and $V_{OL} = 0V$.
- 2188 • Transmit the test sequence to the DUT.
- 2189 • Verify via any valid observable that the DUT received the test sequence without errors.

2190 **Observable Results**

- 2191 • For all test cases, verify that the DUT receives the LP test sequence without errors.

2192 **Possible Problems**

2193 None.

Group 2 LP-RX Behavioral Requirements

Overview

This group of tests verifies several LP-RX behavioral requirements defined in various Sections of the C-PHY Specification.

Status

The test names, Discussion sections, and Procedures are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on multiple devices. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

Test 2.2.1 LP-RX Initialization period (T_{INIT})**Purpose**

To verify that the Slave DUT's RX Initialization period (T_{INIT}), is greater than the minimum conformant value.

References

[1] C-PHY Specification, Section 6.11

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

The C-PHY Specification includes specifications regarding the initialization behavior of both Master and Slave devices. This includes requirements for how Slave devices are initialized, which is accomplished via the T_{INIT} interval.

The specification states[1],

After power-up, the slave side PHY shall be initialized when the master PHY drives a Stop state (LP-111) for a period longer than t_{INIT} . The first Stop state longer than the specified t_{INIT} is called the initialization period. The master PHY itself shall be initialized by a system or protocol layer input signal (PPI). The master side shall ensure that a Stop state longer than t_{INIT} does not occur on the lines before the master is initialized. The slave side shall ignore all line states during an interval of unspecified length prior to the initialization period. In multi-lane configurations, all lanes shall be initialized simultaneously.

Figure 2.2.1-1: T_{INIT} Specification Requirement

The specification also states[1],

Note that t_{INIT} is considered a protocol-dependent parameter, and thus the exact requirements for $t_{INIT,MASTER}$ and $t_{INIT,SLAVE}$ (transmitter and receiver initialization Stop state lengths, respectively,) are defined by the protocol layer specification and are outside the scope of this document. However, the C-PHY specification does place a minimum bound on the lengths of $t_{INIT,MASTER}$ and $t_{INIT,SLAVE}$, which each shall be no less than 100 μ s. A protocol layer specification using the C-PHY specification may specify any values greater than this limit, for example, $t_{INIT,MASTER} \geq 1$ ms and $t_{INIT,SLAVE} = 500$ to 800 μ s.

Figure 2.2.1-2: T_{INIT} Minimum Conformance Limit

Note that because of the protocol-dependence of this parameter, the proper protocol-specific values must be determined for the DUT, via the respective protocol specifications.

Note also that because T_{INIT} is considered a protocol-dependent parameter by the C-PHY specification, it is possible that the detection and validation of the T_{INIT} interval may be implemented in the protocol layer logic for some DUT types. Therefore, if a DUT is not designed to contain this logic (e.g., for a bare-phy DUT with a PPI or other exposed protocol interface), this test is considered Not Applicable.

For Slave DUTs, a test can be designed in order to verify whether or not the DUT ignores all line states prior to receiving a valid Initialization period. This can be done using a wide variety of sequences, by sending any valid LP or HS sequence to the DUT that causes an observable result. If the sequence is not preceded by a valid T_{INIT} interval, the DUT should ignore the sequence.

2229 For the purposes of this test, all Lanes will be tested simultaneously, by sending T_{INIT} on all Lanes, prior to
2230 the valid sequence.

2231 **Test Setup**

2232 See Annex B.2.

2233 **Test Procedure**

- 2234 • Connect the Slave DUT to the Test Setup, leaving the DUT power off.
2235 • Power on the DUT.
2236 • Without sending a valid Initialization period, send a valid HS or LP test sequence that would
2237 otherwise cause an observable result.
2238 • Verify that the DUT ignores the test sequence.
2239 • Repeat the previous 2 steps multiple times, slowly increasing the duration of the Initialization
2240 period until the DUT is observed to accept the test sequence.
2241 • Record T_{INIT} as the minimum Initialization period that caused the DUT to accept the test sequence.

2242 **Observable Results**

- 2243 • Verify that the value of T_{INIT} is greater than the minimum protocol-specific conformance limit.

2244 **Possible Problems**

2245 None.

Test 2.2.2 ULPS Exit: LP-RX T_{WAKEUP} Timer Value**Purpose**

To verify that the DUT's LP receiver properly exits ULPS when sent a Mark-1 for minimum time (T_{WAKEUP}) followed by a Stop state.

References

[1] C-PHY Specification, Section 6.6.3

[1] Ibid, Table 18

Resource Requirements

See Annex A.2.

Last Technical Modification

June 18, 2014

Discussion

The C-PHY Specification defines a mechanism for bringing Lanes out of the ULPS state[1]. This procedure involves driving a Mark-1 state (LP-100) for a minimum time T_{WAKEUP}, followed by a Stop state (LP-111), which should be detected by the Slave device.

The purpose of this test is to verify that a Slave device properly detects a validly formed ULPS exit sequence that contains a minimum duration T_{WAKEUP} Mark-1 state (1ms)[2]. The Test System will emulate a Master device, which will put the Clock and Data Lanes into the ULPS state. A test sequence will then be sent which begins with the minimum-duration ULPS exit sequence, followed by any valid HS image data sequence that produces an observable result on the DUT. The DUT will then be observed to determine if the image data sequence was properly received (implying that the DUT did successfully exit the ULPS state.)

(Note that the general methodology for this test is similar to the T_{INIT} test of 2.2.1, however rather than sending a valid observable sequence that is preceded by a valid T_{INIT} sequence, the DUT is placed into ULPS mode, and then is sent a valid observable sequence that is preceded by a valid T_{WAKEUP} sequence.)

Test Setup

See Annex B.2.

Test Procedure

- Connect the DUT to the Test System.
- Configure the Test System to send a sequence to the DUT that will put all Lanes into the ULPS state.
- With the DUT in the ULPS state, send the test sequence consisting of a Mark-1 (LP-100) state for 1ms, followed by a valid HS image data sequence.
- Observe whether or not the DUT receives the HS image data sequence (implying that if the image data is received, the DUT must have properly exited ULPS mode.)

Observable Results

- Verify that the DUT exits ULPS mode.

2282 **Possible Problems**

2283 None.

Test 2.2.3 LP-RX Invalid/Aborted Escape Mode Entry

Purpose

To verify that the DUT's LP-RX properly aborts the Escape Mode entry process when it receives an unexpected Stop state prior to completion.

References

[1] C-PHY Specification, Section 6.6.4

[2] Ibid, Figure 28

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

The C-PHY Specification provides a formal definition of the Escape Mode Entry process in state-machine form[1].

The specification also states in text form[2],

681 A lane shall enter escape mode via an escape mode entry procedure (LP-111, LP-100, LP-000, LP-001, LP-
682 000). As soon as the final Bridge state (LP-000) is observed on the lines the lane shall enter escape mode in
683 space state (LP-000). If an LP-111 is detected at any time before the final Bridge state (LP-000), the Escape

Figure 2.2.3-1: Escape Mode Entry Specification Definition

An example of the Escape Mode Entry procedure, reproduced from the specification, is shown below[2].

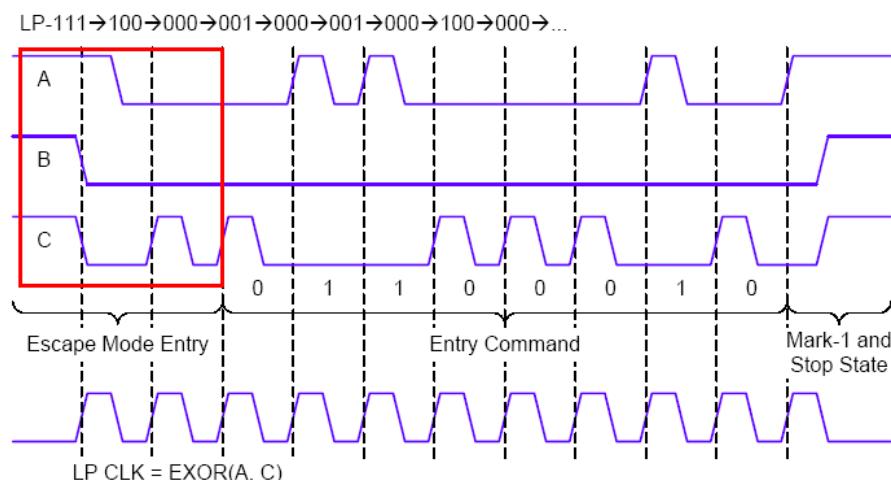


Figure 28 Trigger-Reset Command in Escape Mode

2300

Figure 2.2.3-2: Escape Mode Entry Procedure (with Trigger-Reset Command)

2301 The specification additionally states[2],

683 space state (LP-000). If an LP-111 is detected at any time before the final Bridge state (LP-000), the Escape
2302 684 mode entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

Figure 2.2.3-3: Escape Mode Entry Abort Specification Definition

2303 In this test, the ability of the DUT's LP-RX to properly detect and handle invalid Escape Mode Entry
2304 sequences will be verified. The general methodology for this test requires invalid Escape Mode Entry
2305 sequences to be sent between HS bursts. The DUT will be observed to determine whether the presence of
2306 the invalid sequences causes errors in the received data.

2307 As for which specific test patterns to send for the invalid entry test cases, care must be taken to ensure that
2308 the test cases do not contain other valid LP sequences, which could be misinterpreted by the DUT. Also,
2309 care must be taken to not change the V_A, V_B, and V_C line states simultaneously (e.g., LP-000/111). The
2310 following sequences will be sent, where the state deviations from the valid Escape Mode Entry sequence
2311 are shown in red:

2312 **LP-111, LP-100, LP-000, LP-001, LP-000** (valid Escape Mode Entry sequence)

2313 **Test Case 1) LP-111, LP-100, LP-000, LP-001, LP-111**

2315 **Test Case 2) LP-111, LP-100, LP-111, LP-111, LP-111**

2316 In this test, the 2 above cases of invalid Escape Mode Entry sequences will be sent to the DUT. The
2317 sequences will be inserted between HS bursts in the image data sequence, and should be inserted at the end
2318 of every line of pixel data. In all cases the presence of the invalid Escape Mode Entry sequences shall not
2319 affect the ability of the receiver to properly receive the HS data in order for the DUT to be considered
2320 conformant.

2321 **Test Setup**

2322 See Annex B.2.

2323 **Test Procedure**

- 2324 • Connect the DUT to the Test Setup.
- 2325 • Configure the Test Setup to transmit a valid image or video sequence to the DUT, and verify that
2326 the image data is properly received by the DUT (via any available observable means).
- 2327 • Once proper operation has been verified, modify the sequence by inserting an LP-
2328 111/100/000/001/111 invalid Escape Mode Entry sequence (Test Case #1 above) between HS
2329 bursts (keeping all other necessary video timings intact, as needed), and re-transmit the sequence
2330 to the DUT.
- 2331 • Verify that the DUT is still able to successfully receive the image data without impairment.
- 2332 • Repeat the previous two steps for Test Case #2.

2333 **Observable Results**

- 2334 • In both cases, verify that the integrity of the received data, as well as the overall operation of the
2335 DUT are not negatively affected by the presence of the invalid/aborted Escape Mode Entry
2336 sequences.

2337 **Possible Problems**

2338 None.

Test 2.2.4 LP-RX Invalid/Aborted Escape Mode Command

Purpose

To verify that the DUT's LP-RX properly ignores invalid/aborted Escape commands.

References

[1] C-PHY Specification, Figure 28

[2] Ibid, Section 6.6

[3] Ibid, Table 9 Note 2

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

The previous test (2.2.3) verified a DUT's ability to detect invalidly formed Escape Mode Entry sequences, which were corrupted with LP-111 Stop states at different locations in the Escape Mode Entry sequence. The result of these tests was that the DUT should have effectively ignored the invalid sequence and not have allowed the invalid sequences to negatively impact reception of subsequent valid data.

This test is effectively a continuation of the same idea, extending the LP-111 corruption into the actual command fields. An example showing a validly formed Escape Mode Entry Command (reproduced from the specification) is shown below[1].

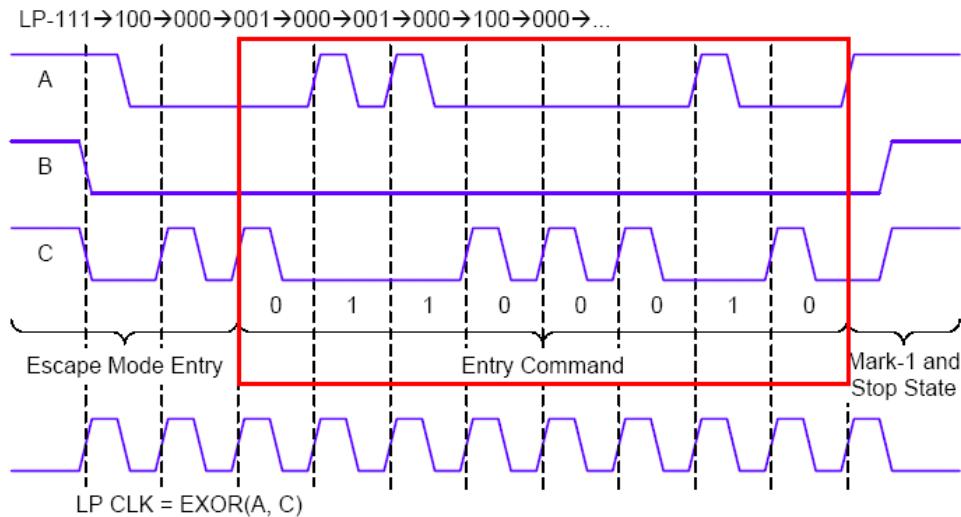


Figure 28 Trigger-Reset Command in Escape Mode

Figure 2.2.4-1: Complete Escape Mode Sequence (Trigger-Reset Command Shown)

2358 The specification states[2],

681 A lane shall enter escape mode via an escape mode entry procedure (LP-111, LP-100, LP-000, LP-001, LP-
682 000). As soon as the final Bridge state (LP-000) is observed on the lines the lane shall enter escape mode in
2359 space state (LP-000). If an LP-111 is detected at any time before the final Bridge state (LP-000), the Escape

Figure 2.2.4-2: Space State Specification Requirement

2360 Also, the specification states[3],

2361 2. *If LP-111 occurs during escape mode the lane returns to Stop state (Control Mode LP-111).*

Figure 2.2.4-3: Escape Mode LP-11 Specification Requirement

2362 Also, the specification states[2],

688 The Stop state shall be used to exit escape mode and cannot occur during escape mode operation because of
689 the spaced-one-hot encoding. The Stop state immediately returns the lane to Control mode. If the entry
690 command doesn't match a supported command, that particular escape mode action shall be ignored and the
2363 receive side waits until the transmit side returns to the Stop state.

Figure 2.2.4-4: Stop State Specification Requirement

2364 In this test, eight test cases of a corrupted Entry Command will be sent to the DUT. They will be inserted
2365 between HS bursts of an otherwise valid image data stream. All of the test sequences will contain valid
2366 Escape Mode Entry sequences, but will abort the Escape Mode command by prematurely returning to LP-
2367 11 before the end of the command. (Note that the command will be aborted only after the Mark-0/1 state,
2368 and not the LP-00 Space state, so as to avoid a transition from LP-00 to LP-11.) A ULPS Entry command
2369 will be used as the basis for the corrupted command sequences. The following corrupted sequence test
2370 cases will be defined:

- 2371 1) [Valid EM Entry] + LP-001/000/001/000/001/000/100/000/100/000/100/000/001/**111** + [Stop]
- 2372 2) [Valid EM Entry] + LP-001/000/001/000/001/000/100/000/100/000/100/**111/111/111** + [Stop]
- 2373 3) [Valid EM Entry] + LP-001/000/001/000/001/000/100/000/100/000/100/**111/111/111/111** + [Stop]
- 2374 4) [Valid EM Entry] + LP-001/000/001/000/001/000/100/000/100/**111/111/111/111/111/111** + [Stop]
- 2375 5) [Valid EM Entry] + LP-001/000/001/000/001/000/100/**111/111/111/111/111/111/111** + [Stop]
- 2376 6) [Valid EM Entry] + LP-001/000/001/000/001/**111/111/111/111/111/111/111/111** + [Stop]
- 2377 7) [Valid EM Entry] + LP-001/000/001/**111/111/111/111/111/111/111/111** + [Stop]
- 2378 8) [Valid EM Entry] + LP-001/111/111/111/111/111/111/111/111/111/111/111/111/111/111/111/111/111 + [Stop]

2379 In all test cases the presence of the aborted ULPS command sequences shall not affect the ability of the
2380 receiver to properly receive the HS image data, in order for the DUT to be considered conformant.

2381 **Test Setup**

2382 See Annex B.2.

2383 **Test Procedure**

- 2384 • Connect the DUT to the Test Setup.
- 2385 • Configure the Test Setup to transmit a valid image or video sequence to the DUT, and verify that
2386 the image data is properly received by the DUT (via any available observable means).
- 2387 • Once proper operation has been verified, modify the sequence by inserting the Test Case #1
2388 (above) aborted ULPS command sequence between HS bursts (keeping all other necessary video
2389 timings intact, as needed), and re-transmit the sequence to the DUT.

- 2390 • Verify that the DUT is still able to successfully receive the image data without impairment.
2391 • Repeat the previous two steps for the 7 additional Test Cases.

2392 **Observable Results**

- 2393 • In all cases, verify that the integrity of the received data, as well as the overall operation of the
2394 DUT are not negatively affected by the presence of the invalid/aborted ULPS command
2395 sequences.

2396 **Possible Problems**

2397 None.

Test 2.2.5 LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits

Purpose

To verify that the DUT's LP-RX ignores any extra bits received following a Trigger Command.

References

- [1] C-PHY Specification, Section 6.6.1
- [2] Ibid, Table 16
- [3] Ibid, Section 5.5

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

The C-PHY specification defines the Escape Mode behavior for C-PHY transmitters and receivers. This includes a requirement for how receivers treat extra bits that are received after an Escape Mode Trigger command.

The specification states[1],

is flagged to the protocol layer at the receive side via the logical PPI. Any bit received after a Trigger Command but before the lines go to the Stop state shall be ignored. Therefore, dummy bytes can be concatenated in order to provide Clock information to the receive side.

Figure 2.2.5-1: Escape Mode Trigger Extra Bits Specification Requirement

In this test, several test cases are constructed that include additional extra bits following the Trigger Command and before the Mark-1/Stop Exit sequence, in an otherwise validly formed Escape Command sequence.

Note that according to the specification wording, this requirement explicitly applies to Escape Mode Trigger commands only, and not the 'Undefined', 'ULPS', or 'LPDT' command types. A list of the assigned Escape Entry Codes is reproduced from the specification in the figure below[2].

Table 16 Escape Entry Codes

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

2420

Figure 2.2.5-2: Assigned Escape Mode Entry Command Codes

2421 Because the receiver behavior upon reception of an Escape Mode Trigger is mostly protocol-defined and
 2422 outside the scope of the C-PHY specification, this test will simply verify that normal operation of the
 2423 receiver is not negatively impacted by the reception of Triggers that have extra post-command bits
 2424 appended after the Command byte.

2425 Note also that this requirement will be verified for all Lanes. While many C-PHY applications may restrict
 2426 most Escape Mode functionality to Lane 0, the C-PHY specification explicitly states[3],

2427 301 All lanes shall include escape mode support for ULPS and Triggers in the forward direction.

Figure 2.2.5-3: Escape Mode ULPS Specification Requirement

2428 The methodology for this test will follow the same general approach as Tests 2.2.3 and 2.2.4, where the
 2429 Escape Mode test case sequence will be inserted between the HS bursts of an otherwise valid data stream.
 2430 However rather than a ULPS Entry command, the Escape Mode sequence for this test will contain a
 2431 Trigger sequence, followed by extra bits. The Escape Mode sequence will be transmitted on all Lanes
 2432 simultaneously. The DUT behavior will be observed to verify that the presence of the extra post-command
 2433 bits does not impact proper image data reception. (Because the Trigger command itself should have no
 2434 impact on normal operation, the default observable in all cases for this test is that the image data should be
 2435 received without error.)

2436 The choice of the extra post-command bits must be defined for this test. This test will concatenate one extra
 2437 byte of data after the Trigger command, and will use the ULPS Entry command as this extra byte. As the
 2438 DUT should ignore this additional byte according the specification, proper DUT behavior should not be
 2439 impacted, as the ULPS command should effectively be ignored by the receiver.

2440 This test will verify that for each of the four Trigger commands (see Figure 2.2.5-2 above), the presence of
 2441 an additional ULPS command byte appended after the Trigger will not affect proper reception of the image
 2442 data stream.

2443 Test Setup

2444 See Annex B.2.

2445 Test Procedure

- 2446 • Connect the DUT to the Test System.
- 2447 • Configure the Test Setup to transmit a valid image or video sequence to the DUT, and verify that
2448 the image data is properly received by the DUT (via any available observable means).
- 2449 • Once proper operation has been verified, modify the sequence by inserting a validly formed
2450 Escape Mode Entry sequence + Reset-Trigger command (01100010) + ULPS command
2451 (00011110) on all Lanes, after each horizontal line of pixel data of the image Data Stream, and re-
2452 transmit the sequence to the DUT.
- 2453 • Verify that the DUT **does** receive the image data stream.
- 2454 • Repeat this process three additional times, using the Unknown-3, Unknown-4, and Unknown-5
2455 Trigger commands in place of the Reset-Trigger, and for each case verify that the DUT **does**
2456 properly receive the image data stream.

2457 Observable Results

- 2458 • Verify that in all test cases the DUT ignores all bits occurring after the last bit of the Trigger
2459 Command, by observing that the DUT properly received the image data stream without error.

2460 Possible Problems

2461 None.

Test 2.2.6 LP-RX Escape Mode Unsupported/Unassigned Commands

Purpose

To verify that the DUT's LP-RX properly ignores unsupported and unassigned Escape Mode commands.

References

[1] C-PHY Specification, Table 16

[2] Ibid, Section 6.6

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

The C-PHY specification defines eight 'assigned' Escape Mode Command codes, which may or may not be supported by a particular DUT. (Note the terms assigned and supported are not equivalent, and have two separate meanings. Devices may or may not support any of the 8 assigned Command codes, however devices should always ignore (i.e., never support) any of the 248 unassigned codes.) The list of assigned codes, reproduced from the specification, is shown below[1].

Table 16 Escape Entry Codes

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

Figure 2.2.6-1: Assigned Escape Mode Entry Command Codes

The specification states[2],

689 the spaced-one-hot encoding. The Stop state immediately returns the lane to Control mode. If the entry
 690 command doesn't match a supported command, that particular escape mode action shall be ignored and the
 691 receive side waits until the transmit side returns to the Stop state.

Figure 2.2.6-2: Escape Mode Unspecified Command Specification Requirement

The methodology for this test will be identical to Tests 2.2.3/4/5, where an Escape Mode sequence will be inserted between HS bursts of an otherwise valid image data stream, on all Data Lanes. The Escape Mode

12-Feb-2016

2482 sequence will contain an unassigned Escape command byte. The DUT's behavior will be observed to verify
2483 that the presence of the unassigned command code does not impact reception of the valid data stream.

2484 In this test, the DUT will be sent all 248 unassigned Command codes, contained in properly formed, valid
2485 Escape sequences. It will also be sent the Undefined-1, Undefined-2, Unknown-3, Unknown-4, and
2486 Unknown-5 Command codes shown above. In all cases, the DUT should ignore the command code.

2487 Note that for the sake of test time, multiple test cases may be combined into a single stimulus sequence,
2488 provided each of the Escape command codes is transmitted in its own LP burst (i.e., it is preceded by its
2489 own Escape Mode Entry sequence and is followed by a return to the Stop state (LP-111) before the next
2490 command code is sent.)

2491 **Test Setup**

2492 See Annex B.2.

2493 **Test Procedure**

- 2494 • Connect the DUT to the Test System.
- 2495 • Configure the Test Setup to transmit a valid image or video sequence to the DUT, and verify that
2496 the image data is properly received by the DUT (via any available observable means).
- 2497 • Once proper operation has been verified, modify the sequence by inserting a validly formed
2498 Escape Mode Entry sequence + the Undefined 1 command code (1001111), on all Lanes,
2499 between the HS bursts of the image Data Stream, and re-transmit the sequence to the DUT.
- 2500 • Verify that the DUT does receive the image data stream.
- 2501 • Repeat this process 4 additional times, using the Undefined-1, Unknown-3, Unknown-4, and
2502 Unknown-5 Trigger commands in place of the Undefined 1 command, and for each case verify
2503 that the DUT does properly receive the image data stream.
- 2504 • Repeat this process 248 additional times, using each of the 248 unassigned command codes, and
2505 for each case verify that the DUT does properly receive the image data stream.

2506 **Observable Results**

- 2507 • For all test cases, verify that the DUT ignores the unsupported/unassigned command, and
2508 successfully receives the image data stream.

2509 **Possible Problems**

2510 None.

Group 3 HS-RX Voltage and Jitter Tolerance Requirements

2511 Overview

2512 This group of tests verifies various High-Speed RX signaling requirements defined in multiple Sections of
2513 the C-PHY Specification (including Sections 9.2.1, 6.x, and 10.2.1).

2514 Status

2515 The test names, Discussion sections, and Procedures are considered to be in release form (i.e., sufficiently
2516 documented to reflect the current state of implementation), and most tests have been successfully
2517 performed on at least one device. Additional modifications to both the test descriptions and
2518 implementations may continue if new opportunities for improvement are identified.

Test 2.3.1 HS-RX Amplitude Tolerance ($V_{CPRX(DC)}$, V_{IHHS} , V_{ILHS})

Purpose

To verify that the DUT's HS receiver can successfully receive signaling with common-mode and differential voltage amplitude levels ($V_{CPRX(DC)}$, V_{IHHS} , V_{ILHS}) within the conformance limits.

References

[1] C-PHY Specification, Section 9.2.1

[2] Ibid, Table 26

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements are specifications for $V_{CPRX(DC)}$, V_{IHHS} , and V_{ILHS} , which together describe the amount of voltage amplitude and offset a receiver should be capable of tolerating, and still be able to operate properly.

The specification states[1],

- 1102 The differential input high and low threshold voltages of the high-speed receiver are denoted by V_{IDTH} and
- 1103 V_{IDTL} , respectively. V_{ILHS} and V_{IHHS} are the single-ended, input low and input high voltages, respectively.
- 1104 $V_{CPRX(DC)}$ is the differential input common-point voltage. The high-speed receiver shall be able to detect
- 1105 differential signals at its A, B and C input signal pins when all three signal voltages, V_A , V_B and V_C , are
- 1106 within the common-point voltage range and if the voltage differences between V_A , V_B and V_C exceed either
- 1107 V_{IDTH} or V_{IDTL} . The high-speed receiver shall receive high-speed data correctly while rejecting common-

Figure 2.3.1-1: $V_{CPRX(DC)}$, V_{IHHS} , V_{ILHS} Specification Definitions

The specification also provides conformance limits for $V_{CPRX(DC)}$, V_{IHHS} , and V_{ILHS} [2].

Table 26 HS Receiver DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$V_{CPRX(DC)}$	Common-Point voltage HS receive mode	95		390	mV	1, 2
V_{IDTH}	Differential input high threshold			40	mV	
V_{IDTL}	Differential input low threshold	-40			mV	
V_{IHHS}	Single-ended input high voltage			535	mV	1
V_{ILHS}	Single-ended input low voltage	-40			mV	1

Figure 2.3.1-2: $V_{CPRX(DC)}$, V_{IHHS} , V_{ILHS} Specification Conformance Requirements

In this test, HS signaling will be sent to the DUT that contains various common-mode and differential levels. Multiple cases will be tested, which verify the lower and upper limits of the conformance ranges. HS data will be sent to the DUT with different common-mode and differential levels, and in all test cases the DUT should be able to receive the data without error. (Note the test pattern can be various HS sequences depending on the DUT type. See Annex F.)

2543 Note that there are actually three different amplitude specifications for C-PHY, each with separate
 2544 conformance ranges. Separate requirements are defined for the HS-RX common-mode levels ($V_{CPRX(DC)}$),
 2545 the HS-RX differential levels (V_{IDTH} and V_{IDTL}), and also a third set of requirements is defined for the
 2546 maximum and minimum allowed single-ended levels of the V_A , V_B , and V_C signals (V_{IHHS} and V_{ILHS}).
 2547 When testing any one of these parameters, it might seem desirable to vary the other two parameters across
 2548 their entire ranges, however this must be done with caution, as there is some interdependence between the
 2549 three specifications, which for some cases is mutually exclusive (e.g., it is not possible to create a signal
 2550 with the maximum RX common-mode level (390mV) and maximum TX differential level (600mVppd)
 2551 simultaneously, as such a signal would have a single-ended $V_A/V_B/V_C$ value of 540mV, which would
 2552 violate the upper V_{IHHS} limit of 535mV.)

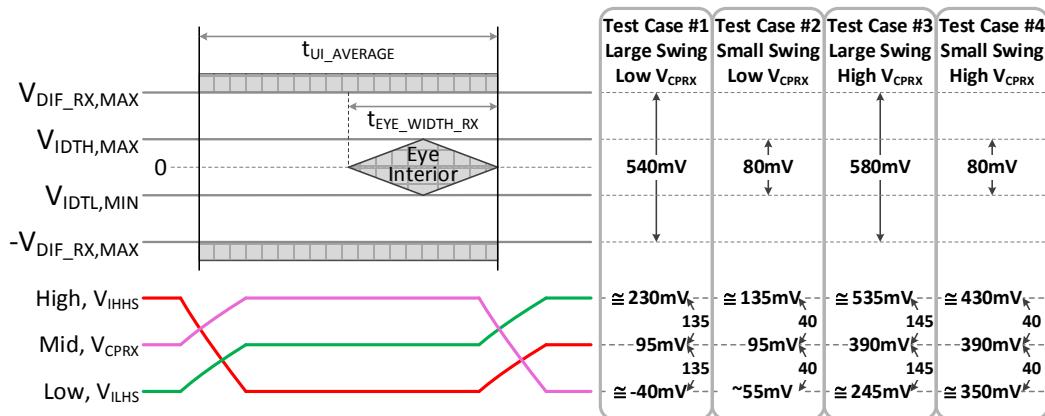
2553 When designing any test with potentially interrelated parameters, it is also important to include control
 2554 cases to help isolate the specific parameter under test. For this test, it has already been mentioned that the
 2555 maximum differential amplitude cannot be used for the maximum common-mode voltage test case,
 2556 however it is possible to select a slightly smaller differential voltage, which does not violate the V_{IHHS}
 2557 single-ended upper limit. A differential voltage of 580mVppd with a common mode level of 390mV will
 2558 produce a maximum single-ended voltage of $390 + (580/4) = 535$ mV. (Where the maximum single-ended
 2559 voltage for either V_A , V_B , or V_C will be equal to the common mode level plus 1/4 the peak-to-peak
 2560 differential level.)

2561 Note that two similar test cases will be defined for verifying the minimum common mode level
 2562 requirements. A summary of all test cases is shown in the table below. For cases 1 and 3, the Pk-Pk
 2563 Differential Voltage corresponds to the difference between the strong one and strong zero levels. For cases
 2564 2 and 4, the Pk-Pk Differential Voltage corresponds to the difference between the weak one and weak zero
 2565 levels.

Table 2.3.1-1: Differential/Common-Mode Amplitude Test Cases

Test Case #	Common-Mode Level (V_{CPRX})	Pk-Pk Differential Voltage (2^*V_{OD})	Approximate Single-Ended V_{IHHS}/V_{ILHS}	Comments
1	95mV	540mVppd	230mV/-40mV	Minimum CM level, but with the largest possible Vdiff* that exactly hits the VILHS lower limit of -40mV, so Vdiff = 540mVppd.
2	95mV	80mVppd	135mV/55mV	Minimum CM level with minimum Vdiff (80mVppd).
3	390mV	580mVppd	535mV/245mV	Maximum CM level, but with the largest possible Vdiff that exactly hits the VIHHS upper limit of 535mV, so Vdiff = 580mVppd
4	390mV	80mVppd	430mV/350mV	Maximum CM level with minimum Vdiff (80mVppd).

2566 * Vdiff = Peak-to-peak value of the differential signal (which equals 2x the V_{OD} value).
 2567 Figure 2.3.1-1 shows how the levels in Table 2.3.1-1 relate to the differential and single-ended waveforms
 2568 for each of the four cases.
 2569



2570

Figure 2.3.1-3 Illustration Showing Differential and Single-Ended Levels**Test Setup**

See Annex B.2.

Procedure for Setting the Signal Levels:

1. Create a nominal C-PHY signal using a PRBS 9 data sequence (or other preferred data sequence that can be verified by the DUT) that has been mapped and encoded per the C-PHY specification. (250mV Single ended Low-Mid-High as 0-125-250mV)
2. Set the amplitude as follows:
 - A. **For Test Cases #1 and #3:** Set the single-ended Mid level produced by the signal generator to the Common-Mode Level (V_{CPRX}) value in Table 2.3.1-1. Adjust the single-ended High and Low levels, V_{IHHS} and V_{ILHS} , keeping them equidistant from V_{CPRX} , to maximize the differential voltage at the receiver input of the DUT without causing mask violations beyond $-V_{DIF_RX,MAX}$ and $V_{DIF_RX,MAX}$, as shown in Figure 2.3.1-1. The difference between $-V_{DIF_RX,MAX}$ and $V_{DIF_RX,MAX}$, is the Pk-Pk Differential Voltage ($2*V_{OD}$) specified in Table 2.3.1-1. It is anticipated that the V_{IHHS} and V_{ILHS} values determined as a result of this procedure will be similar to the corresponding values in Table 2.3.1-1.
 - B. **For Test Cases #2 and #4:** Set the single-ended Mid level produced by the signal generator to the Common-Mode Level (V_{CPRX}) value in Table 2.3.1-1. Adjust the single-ended High and Low levels, V_{IHHS} and V_{ILHS} , keeping them equidistant from V_{CPRX} , to minimize the differential voltage at the receiver input of the DUT without causing mask violations at the eye interior peaks between $V_{IDTL,MIN}$ and $V_{IDTH,MAX}$, as shown in Figure 2.3.1-1. The difference between $V_{IDTL,MIN}$ and $V_{IDTH,MAX}$, is the Pk-Pk Differential Voltage ($2*V_{OD}$) specified in Table 2.3.1-1. It is anticipated that the V_{IHHS} and V_{ILHS} values found as a result of this procedure will be similar to the corresponding values in Table 2.3.1-1.

Test Procedure

- Connect the DUT to the Test System.
- Perform the **Procedure for Setting the Signal Levels** (shown above) to configure the Test System to generate a suitable HS test pattern with the common mode and differential voltage levels specified for Test Case #1 above, for all Lanes.
- Transmit the test sequence to the DUT.
- Verify via any valid observable that the DUT received the test sequence without errors.
- Repeat the previous three steps for Test Cases 2 through 4.

2602 **Observable Results**

- 2603 • Verify that for all test cases the test sequence was received by the DUT without error.

2604 **Possible Problems**

2605 None.

Test 2.3.2 HS-RX Differential Input High/Low Thresholds (V_{IDTH} , V_{IDTL})

Purpose

To verify that the DUT's HS receiver can properly detect V_{OD} voltage levels that are at least as small as the minimum required values (V_{IDTH} , V_{IDTL}).

References

- [1] C-PHY Specification, Section 9.2.1
- [2] Ibid, Table 26

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements are specifications for V_{IDTH} , and V_{IDTL} , which are the HS-RX Differential Input High/Low Threshold Voltages. These are the minimum differential signal levels seen as an HS Strong 1 and HS Strong 0 by the receiver. (It can also be thought of as a receiver 'squench level', below which any activity is not detected by the RX.)

The specification states[1],

- 1102 The differential input high and low threshold voltages of the high-speed receiver are denoted by V_{IDTH} and
 1103 V_{IDTL} , respectively. V_{ILHS} and V_{IHHS} are the single-ended, input low and input high voltages, respectively.
 1104 $V_{CPRX(DC)}$ is the differential input common-point voltage. The high-speed receiver shall be able to detect
 1105 differential signals at its A, B and C input signal pins when all three signal voltages, V_A , V_B and V_C , are
 1106 within the common-point voltage range and if the voltage differences between V_A , V_B and V_C exceed either
 1107 V_{IDTH} or V_{IDTL} . The high-speed receiver shall receive high-speed data correctly while rejecting common-

Figure 2.3.2-1: V_{IDTH} Specification Definition

The specification also defines the conformance limits for V_{IDTH} and V_{IDTL} in a summary table[2].

V_{IDTH}	Differential input high threshold		40	mV	
V_{IDTL}	Differential input low threshold	-40		mV	

Figure 2.3.2-2: V_{IDTH} , V_{IDTL} Conformance Limits

While the specification defines V_{IDTH} and V_{IDTL} as separate parameters, from a practical standpoint it is nearly impossible to verify these values independently, as for any properly-formed HS signal it is not typically possible to vary only the Strong 1 or Strong 0 levels, as they are typically symmetric about the V_{CPTX} level. However it is sufficient for the purposes of conformance to verify both parameters simultaneously.

For this test, an initial verification step will be performed where the high-speed test pattern will be sent to the DUT starting at a nominal differential voltage of $V_{OD} = 150\text{mV}$ (300mV pk-pk differential), to verify proper test setup and DUT operation under 'normal' conditions. (Note also that a nominal V_{CPTX} TX common-mode level of 250mV will be used throughout this entire test. There is no need to test V_{IDTH} at the max/min V_{CPRX} levels, as these cases were already verified in Test 2.3.1). Following this, the procedure will

2636 be repeated, with the differential amplitude slowly decreased for each iteration until the point is reached
2637 where the DUT begins to show errors. V_{IDTH} and V_{IDTL} are recorded as the minimum V_{OD} value where the
2638 DUT was able to consistently receive the test sequence without error.

2639 The V_{IDTH}/V_{IDTL} result must be less than or equal to 40mVpk (80mV pk-pk differential), in order to be
2640 considered conformant[2].

2641 **Test Setup**

2642 See Annex B.2.

2643 **Test Procedure**

- 2644 • Connect the DUT to the Test System.
- 2645 • Configure the Test System to generate a suitable HS test pattern with a nominal common mode
2646 level of 250mV and peak-to-peak differential amplitude of 300mVppd, for all Lanes.
- 2647 • Transmit the test sequence to the DUT.
- 2648 • Verify (via any valid observable) that the DUT received the test sequence without errors.
- 2649 • Repeat the previous three steps, slowly decreasing the peak-to-peak differential voltage across all
2650 Lanes until the point is reached where the DUT begins to indicate errors.
- 2651 • Record the V_{IDTH}/V_{IDTL} result as 0.5 times the smallest peak-to-peak differential amplitude where
2652 the DUT was able to consistently receive the test sequence without errors. (The factor of 0.5 is
2653 required to convert the peak-to-peak differential voltage to V_{OD} , which is defined as the peak value
2654 of the differential signal.)

2655 **Observable Results**

- 2656 • Verify that V_{IDTH}/V_{IDTL} is less than or equal to 40mV.

2657 **Possible Problems**

2658 None.

Test 2.3.3 HS-RX Jitter Tolerance**Purpose**

To verify that the DUT can tolerate signaling with worst-case timing error.

References

[1] C-PHY Specification, Section 10.3

Resource Requirements

See Annex A.2.

Last Technical Modification

October 5, 2015

Discussion

Section 10 of the C-PHY Specification defines the High Speed Timing requirements for C-PHY products. Included in these specifications are requirements for the RX timing specifications an HS receiver must support.

The specification states[1],

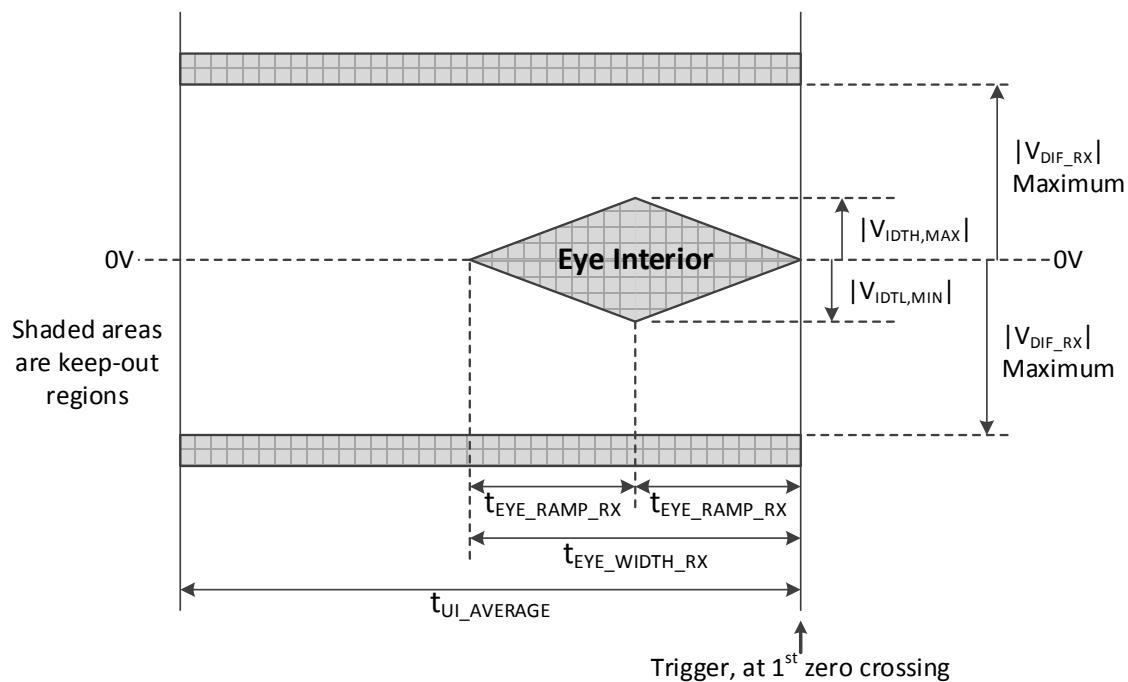
1254 The timing requirements specified in this section shall be met for the signal levels specified in Chapter 9,
1255 with the channel specified in Chapter 8, while transmitting a pseudo-random data pattern having data
1256 transition density similar to the PRBS data patterns described in Chapter 12. The C-PHY Receiver Eye
1257 Diagram shown in Figure 59 defines the receiver eye measurement parameters. The measurement points for
1258 the transmitter and for the receiver are specified in Figure 54.

Figure 2.3.3-1: RX Timing Specification Requirement

The specification also defines the RX timing requirements via an eye diagram. It was agreed that it is more appropriate to test C-PHY v1.0 devices using the Rx Jitter Tolerance test for C-PHY v1.1 devices. The C-PHY v1.0 eye width is only 0.4 UI wide, while the v1.1 eye width is 0.5 UI. Using the 0.4 UI eye width, the test procedure allowed a large amount of duty cycle distortion (DCD) to be used to “close” the eye on the time axis for a worst-case test. Such a large amount of duty cycle distortion was far more than would be experienced in a practical system, and this large amount of DCD caused extreme variations in the UI. By using the 0.5 UI eye width, most of the closure of the eye will be due to Inter-Symbol Interference (ISI), and a smaller amount due to DCD. This is done to ensure that the recovered clock jitter is below 0.4 UI.

The 0.4 UI width of the v1.0 spec is a more stringent specification for the receiver than the 0.5 UI width of the v1.1 spec. Therefore, receivers designed to the v1.0 spec will meet the requirement of the v1.1 spec.

The specification references of the eye diagram and eye diagram parameters shown below are taken from the C-PHY v1.1 draft Specification.



2685

Figure 2.3.3-2: HS-RX Eye Diagram

2686

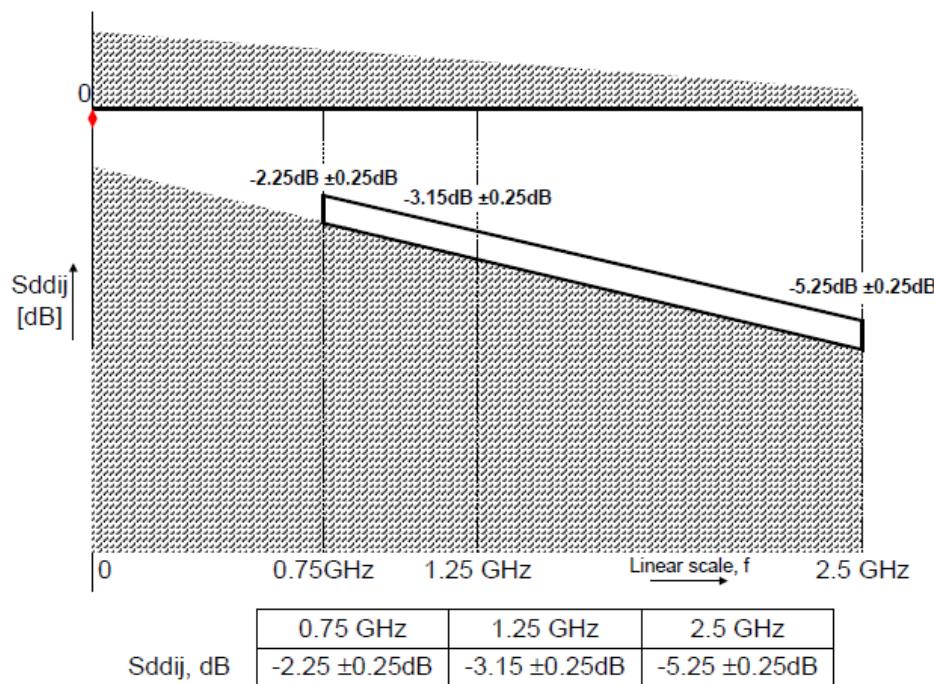
Note that the timing values for the eye diagram are shown in the figure below[2]:

Parameter	Description	Min	Nom	Max	Units	Notes
$t_{EYE_RAMP_RX}$	Eye ramp time at the receiver	0.25			UI	
$t_{EYE_WIDTH_RX}$	Eye width at the receiver	0.5			UI	
$t_{UI_AVERAGE}$	UI average		UI _{INST}			

2687

Figure 2.3.3-3: HS-RX Eye Diagram Timing Values2688
2689
2690

The characteristics of the C-PHY v1.0 channel have been clarified in a later version of the C-PHY specification so that the differential insertion loss does not change with the symbol rate. The insertion loss characteristics of this C-PHY Legacy Channel are repeated below in Figure 2.3.3-4.

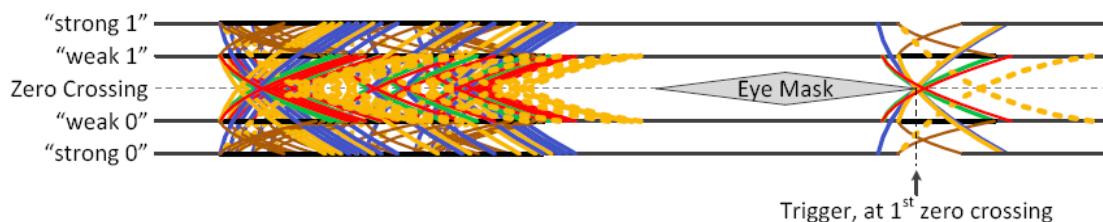


2691

Figure 2.3.3-4: Template for Differential Insertion Losses, C-PHY Legacy Channel

2692 In this test, the timing of a test signal will be modified, and the test signal will be sent to the DUT, to see if
 2693 it can properly receive the signal. The signal will be calibrated using the HS-RX eye diagram as a
 2694 reference.

2695 Note that the methodology to create the eye diagram for C-PHY signaling is slightly different than for
 2696 traditional 2-level signaling. C-PHY uses a ‘triggered eye’, where the trigger point is taken as the first zero
 2697 crossing of any of the three differential waveforms (A minus B, B minus C, and C minus A) that occur at
 2698 each UI boundary. This results in an eye diagram similar to the one shown in the figure below for each of
 2699 the differential waveforms [3]. Additionally the eye mask is allowed to be moved horizontally (optimally)
 2700 to the left (i.e., away from the zero crossing) to a position where there are zero mask hits.



2701

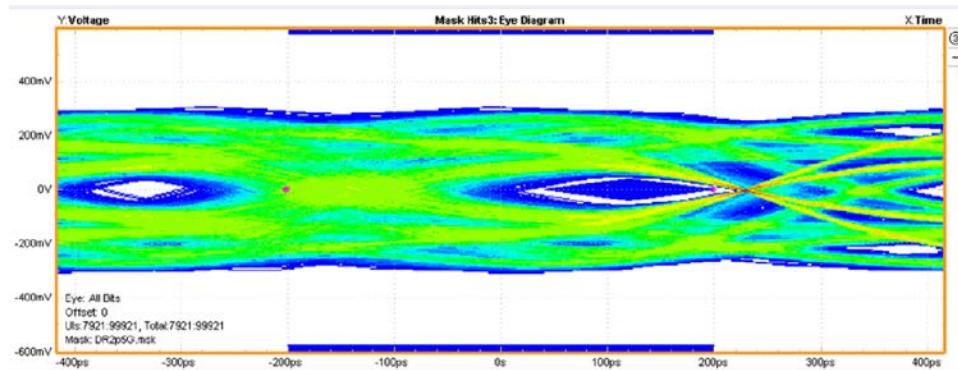
Figure 58 C-PHY Eye Pattern Example, Triggered Eye**Figure 2.3.3-5: HS-RX ‘Triggered Eye’ Diagram**

2702 The eye diagram for the test signal from the signal generator will be calibrated using the following
 2703 procedure: The first step of the procedure is to adjust the resulting HS rise/fall time on the differential (A-
 2704 B, B-C, and C-A signals) on the signal generator output to achieve an eye width of $\leq 0.865\text{UI}$. (Allow a
 2705 range of 0.85UI to 0.88UI.) This will result in a signal that has some amount of ‘switching jitter’, which
 2706 results naturally from the signal transitions.

2707 Add a software-based or hardware-based ISI test channel to the signal having the characteristics of the C-
2708 PHY Legacy Channel described in Figure 2.3.3-4.

2709 To this signal, additional timing impairment will be added, in order to reduce the eye opening to 0.5UI.
2710 While technically a variety of impairments such as SJ or skew between the A, B and C wires can be used to
2711 achieve this eye closure, the most appropriate timing impairment chosen here is Duty Cycle Distortion
2712 (DCD) as defined for single ended NRZ signaling.

2713 Simultaneously increase DCD and reduce the amplitude to be 40mVpk, per the eye diagram. The resulting
2714 signal eye should resemble the figure shown below.



2715

Figure 2.3.3-6: HS-RX Final Calibrated Eye

2716 After the test is run with a nominal DC common-mode level ($V_{CPTX} = 250\text{mV}$), the test will be repeated
2717 with maximum and minimum common-mode levels (175mV and 310mV).

2718 **Details for Creating the Signal:**

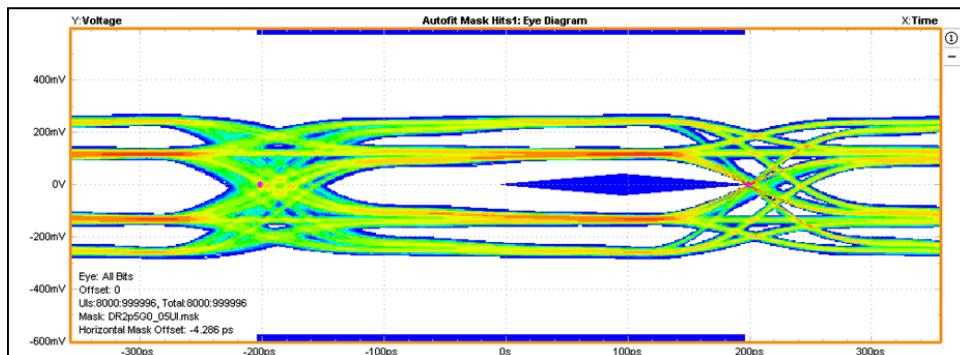
- 2719 1. Create a nominal C-PHY signal using a PRBS 9 data sequence that has been mapped and encoded
2720 per the C-PHY specification. (250mV Single ended Low-Mid-High as (0-125-250mV)
- 2721 2. Slow down the RT/FT to the required amount ~0.135 UI.
- 2722 3. Add the C-PHY Legacy Channel.
- 2723 4. Simultaneously add the DCD until the EYE width is approximately ~ 0.5 UI and adjust the
2724 Amplitude to achieve Eye height: +40mVpk.
- 2725 5. Move the mask horizontally so that it is aligned on the Right side without any hits on the signal.

2726 **Example Results**

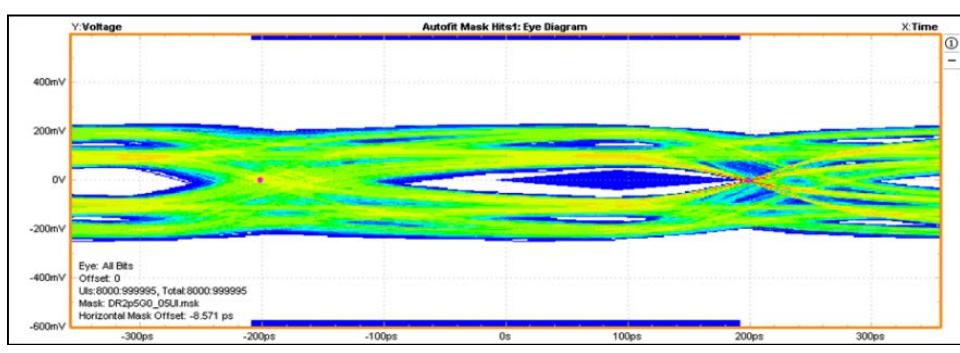
2727 Following are the result after each step of the calibration routine described above for a PRBS9 Test
2728 sequence at symbol rate of 2.5Gbps or at the maximum symbol rate specified by the manufacturer of the
2729 DUT.

12-Feb-2016

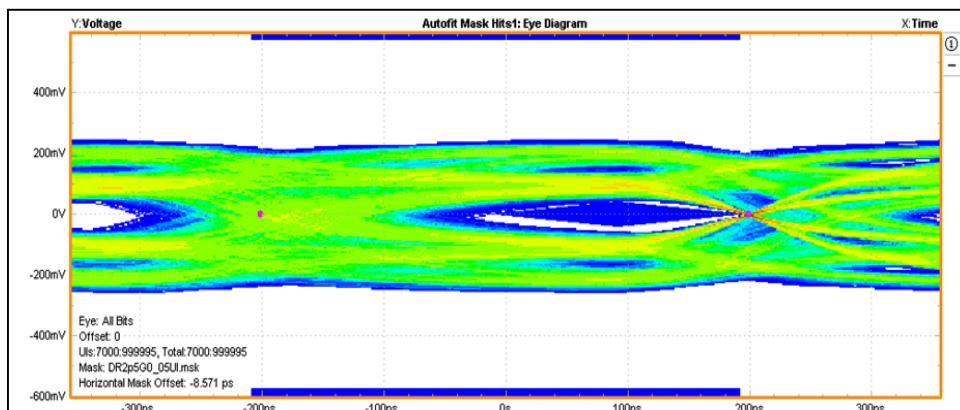
- 2730
2731 1. Differential Eye diagram with Nominal Voltage. Measured a Data jitter of 56psec, and eye width is about 344 psec (0.86UI).



- 2732
2733 2. Slow down the RT/FT and add the Legacy channel. Measured a Data jitter is 131psec, and Eye width is reduced to 269psec (0.67UI)
- 2734

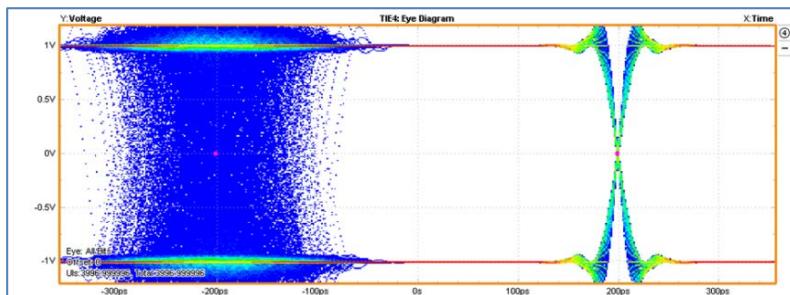


- 2735
2736 3. Add the DCD and adjust amplitude to achieve target eye width and eye height. Data jitter is now increased to 185 psec, and Eye width is reduced to 215 psec (0.53UI).
- 2737



- 2738
2739 For informative purposes only, Clock UI Jitter is noted to be 131psec (0.32 UI) which is less than
2740 the limit of 0.4 UI.

2741



2742 Note that for these tests, a low BER will not be verified. Each test case will be performed using a target
 2743 BER of 1E-10 and a confidence level of 95% (i.e., 3E10 bits). This corresponds to approximately 20
 2744 seconds per test case (assuming a bitrate of 3.35Gbps (1.5Gsp), and a line utilization of 50%, i.e., one
 2745 burst-width of LP between bursts).

2746 The DUT must tolerate all test cases in order to be considered conformant.

2747 **Test Setup**

2748 See Annex B.2.

2749 **Test Procedure**

- 2750 • Connect the DUT to the Test System.
- 2751 • Configure the RX Test Signal Source to transmit signaling to the DUT with parameters according
 2752 to Steps 1 through 4, for all Data Lanes. Set the DC common mode level to 250mV.
- 2753 • Verify (using any valid observable for the given DUT type) that the DUT is able to successfully
 2754 decode the received HS data stream error-free.
- 2755 • Repeat the previous two steps twice, first using a DC common-mode level of 175mV, then using a
 2756 common-mode level of 310mV.

2757 **Observable Results**

- 2758 • For all test cases, verify that the DUT can receive the data without errors.

2759 **Possible Problems**

2760 Note that during any receiver tolerance test, spurious signals from nearby RF sources (e.g., cell phones,
 2761 microwave ovens, etc.) can potentially cause unintended intermittent bursts of errors. Care should be taken
 2762 to minimize the impact of stray RF sources in close proximity to the test setup.

2763 Also, the mask vertex by definition touches the zero crossing point. Hence a ‘Mask Hits’ measurement on
 2764 any analysis tool is expected to show some mask hits (although this is not intended by the specification). To
 2765 remedy this, for the purposes of this test, the entire mask is allowed to be moved horizontally (optimally) to
 2766 the left (i.e., away from the zero crossing) to a position where there are zero mask hits.

Group 4 HS-RX Timer Requirements

Overview

This group of tests verifies various High-Speed RX timer requirements defined in multiple Sections of the C-PHY Specification.

Status

The test names, Discussion sections, and Procedures are considered to be in release form (i.e., sufficiently documented to reflect the current state of implementation), and most tests have been successfully performed on at least one device. Additional modifications to both the test descriptions and implementations may continue if new opportunities for improvement are identified.

Test 2.4.1 HS-RX $t_{3\text{-TERM-EN}}$ Duration

Purpose

To verify that the time required for the DUT's HS-RX to enable its HS line termination ($t_{3\text{-TERM-EN}}$) is within the conformance limits.

References

[1] C-PHY Specification, Table 18

[2] Ibid, Figure 23

Resource Requirements

See Annex A.2.

Last Technical Modification

June 25, 2014

Discussion

As part of the process for switching a Lane out of LP mode, the C-PHY Specification provides a specification for the time required for the Slave to enable its HS line termination before the Master enables the HS differential data signal. (Note this test is only applicable to Slave DUTs).

The specification states[1],

$t_{3\text{-TERM-EN}}$	Time for the slave to enable the HS line termination, starting from the time point when the A, B and C wire cross V_{IL_MAX}	Note 5	38	ns	3
------------------------	---	--------	----	----	---

- 3. Receiver-specific parameter.
- 4. The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.
- 5. As specified in Section 9.2.1, the receiver termination impedances shall not be enabled until the single-ended voltages on all of A, B and C fall below $V_{TERM-EN}$.

Figure 2.4.1-1: $t_{3\text{-TERM-EN}}$ Specification Definition and Conformance Requirements

This interval is shown in the figure below.

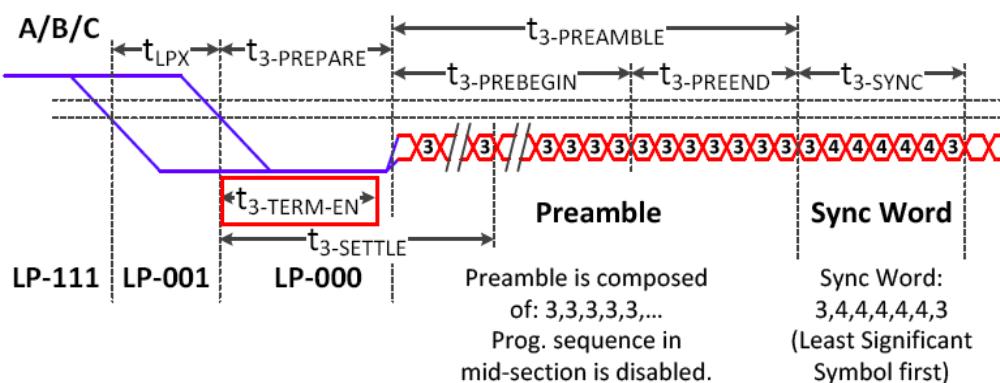


Figure 2.4.1-2: $t_{3\text{-TERM-EN}}$ Interval

2793 In this test, the Test System will emulate a Master device, and initiate an HS Request sequence on the Lane
2794 Under Test. The T₃-TERM-EN interval begins at the point where the LP-00 falling edge (V_C) crosses V_{IL,MAX}
2795 (550mV), and ends at the point when the HS line termination is enabled.

2796 Note that the exact point when the HS line termination is considered “enabled” can be somewhat subjective
2797 in some cases, as the voltage spike that typically occurs on the line when the termination is enabled does
2798 not necessarily have a well-defined shape (and in some cases may not be visible at all). For the purposes of
2799 this test, the measurement point for the termination-enable voltage spike is defined as the maximum voltage
2800 point of the spike (as opposed to the ‘start’ of the spike, which can be even more difficult to clearly
2801 identify.) For devices with sufficient margin in their T₃-TERM-EN timer values, the impact of any potential
2802 measurement uncertainty should be minimal.

2803 The measured duration of T₃-TERM-EN should be greater than the time required for V_C to reach 450mV (i.e.,
2804 V_{TERM-EN}) and less than 38ns[1].

2805 **Test Setup**

2806 This test uses a hybrid test setup. The DUT is connected to the RX Test System in the same manner as the
2807 other HS-RX tests (see Annex B.2), however the DUT behavior is observed by using a DSO to probe the
2808 signaling at the DUT, in a manner similar to the TX test setup shown in Annex B.1.2.

2809 **Test Procedure**

- 2810 • Connect the DUT to the Test System.
2811 • Configure the Test System to emulate a Master device.
2812 • Initiate an HS Request sequence on the DUT’s Lane 0, and capture the exchange using the DSO.
2813 • Measure T₃-TERM-EN, as described above.
2814 • Repeat the previous steps for all other Lanes (if the DUT implements multiple Lanes).

2815 **Observable Results**

- 2816 • For all Lanes, verify that T₃-TERM-EN is greater than the time for V_C to reach 450mV, and less than
2817 38ns.

2818 **Possible Problems**

2819 None.

Test 2.4.2 HS-RX $T_3\text{-PREPARE}$ Tolerance

Purpose

To verify that the DUT's HS-RX can tolerate reception of conformant values for $T_3\text{-PREPARE}$.

References

[1] C-PHY Specification, Figure 23

[2] Ibid, Table 18

[3] Ibid, Section 6.9

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

As part of the process for switching a Lane into HS mode, the C-PHY specification includes requirements for the $T_3\text{-PREPARE}$ interval, which is shown in the figure below[1].

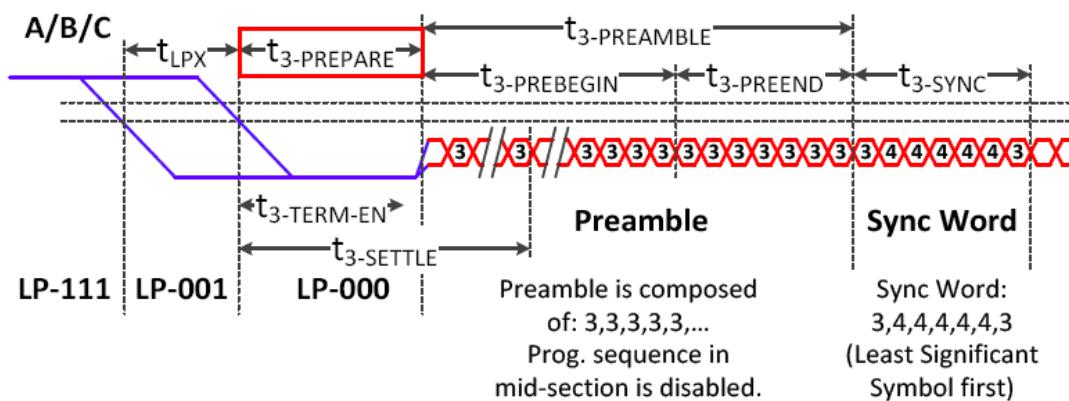


Figure 2.4.2-1: $T_3\text{-PREPARE}$ Interval

The specification also defines the $T_3\text{-PREPARE}$ interval, and provides conformance limits[2].

Table 18 Global Operation Timing Parameters

Parameter	Description	Min	Max	Unit	Notes
$t_{3\text{-PREPARE}}$	Time that the transmitter drives the 3-wire LP-000 line state immediately before the HS_+x line state starting the HS transmission.	38	95	ns	2

Figure 2.4.2-2: $T_3\text{-PREPARE}$ Interval Conformance Requirements

Note that the C-PHY specification defines timing parameters as being either transmitter-specific or receiver-specific[3], and $T_3\text{-PREPARE}$ is defined as a transmitter-specific parameter.

2838 However, the specification also contains a requirement that states[3],

2839 747 Also note that while corresponding receiver tolerances are not defined for every transmitter-specific
 748 parameter, receivers shall also support reception of all allowed conformant values for all transmitter specific
 749 timing parameters in Table 18 for all HS UI values up to, and including, the maximum supported HS symbol
 750 rate specified in the receiver's datasheet.

Figure 2.4.2-3: T₃-PREPARE RX Specification Definition

2840 The TX conformance range for T₃-PREPARE is defined as 38 to 95 ns. In this test, HS bursts containing valid
 2841 image data will be sent to the DUT using different conformant values of T₃-PREPARE.

2842 Test cases will be performed using the maximum and minimum TX values. The test cases are listed in the
 2843 table below.

Table 2.4.2-1: HS Receiver T₃-PREPARE Test Cases

Case #	T3-PREPARE	Notes
1	38ns	Minimum T ₃ -PREPARE
2	95ns	Maximum T ₃ -PREPARE

2844

2845 Also, note that all other timing parameters should be set to nominal values for this test. The recommended
 2846 values are listed in the table below.

Table 2.4.2-2: HS-RX T₃-PREPARE Test Nominal Timer Values

TLPX	T3-PREBEGIN	T3-PROGSEQ	T3-PREEND	T3-SYNC	T3-POST
50ns	448UI	Disabled (0UI)	7UI	7UI	224UI

2847

2848 For all test cases, the DUT must successfully receive the HS data without error in order to be considered
 2849 conformant.

2850 **Test Setup**

2851 See Annex B.2.

2852 **Test Procedure**

- 2853 • Connect the DUT to the Test System.
 2854 • Configure the Test System to transmit an otherwise valid HS image data sequence to the DUT,
 2855 using the T₃-PREPARE Test Case #1 values as described above.
 2856 • Verify that the DUT successfully received the HS image data without error.
 2857 • Repeat the previous two steps for Test Case #2.

2858 **Observable Results**

- 2859 • For all test cases, verify that the DUT successfully received the HS burst data without error.

2860 **Possible Problems**

2861 None.

Test 2.4.3 HS-RX $T_{3-PREBEGIN}$ Tolerance

Purpose

To verify that the DUT's HS-RX can tolerate reception of conformant values for $T_{3-PREBEGIN}$.

References:

[1] C-PHY Specification, Figure 23

[2] Ibid, Section 6.9

Resource Requirements

See Annex A.2.

Last Technical Modification

March 23, 2015

Discussion

As part of the process for switching a Lane into HS mode, the C-PHY specification includes requirements for the $T_{3-PREBEGIN}$ interval, which is shown in the figure below[1].

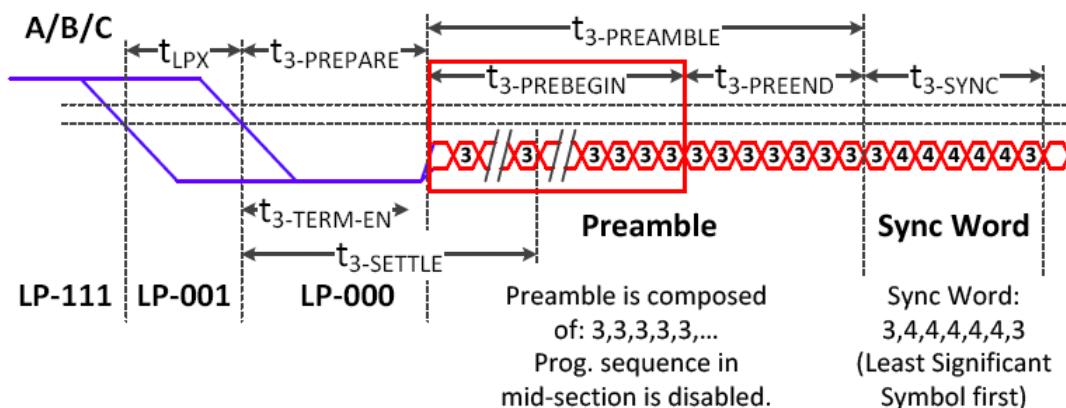


Figure 2.4.3-1: $T_{3-PREBEGIN}$ Interval

The specification also describes the $T_{3-PREBEGIN}$ interval, and provides a recommended length range[2].

755 $t_{3-PREBEGIN}$ should be adjustable from 7 UI minimum to 448 UI maximum in increments of 7 UI.

Figure 2.4.3-2: $T_{3-PREBEGIN}$ Interval Recommended Length Requirements

Note that the specification defines this parameter loosely, and uses a 'should' statement instead of a 'shall'. This is defined from the transmitter's perspective, however. Note that while there is no explicit statement requiring specific receiver requirements for $T_{3-PREBEGIN}$, it is inferred that a receiver must have a detection threshold for $T_{3-PREBEGIN}$ that is between 7 and 448UI, otherwise interoperability problems will occur.

The recommended TX conformance range for $T_{3-PREBEGIN}$ is defined as 7 to 448 UI. In this test, HS bursts containing valid image data will be sent to the DUT using a minimum value of $T_{3-PREBEGIN}$ (7UI). The value of $T_{3-PREBEGIN}$ will be increased in 7UI increments (or a binary search can be used) until the point is found where DUT begins to successfully and consistently receive the bursts. The minimum $T_{3-PREBEGIN}$ value for

2885 which the DUT consistently receives the bursts shall be recorded as the DUT's T_{3-PREBEGIN} detection
 2886 threshold value.

2887 Also, note that all other timing parameters (e.g., T_{3-PREPARE}, T_{3-POST}, etc) should be set to nominal values for
 2888 this test. The recommended values are listed in the table below.

Table 2.4.3-1: HS-RX T_{3-PREBEGIN} Test Nominal Timer Values

TLPX	T3-PREPARE	T3-PROGSEQ	T3-PREEND	T3-SYNC	T3-POST
50ns	70ns	Disabled (0UI)	7UI	7UI	224UI

2889
 2890 The DUT's T_{3-PREBEGIN} detection threshold value must be between 7 and 448UI in order to be considered
 2891 conformant.

2892 **Test Setup**

2893 See Annex B.2.

2894 **Test Procedure**

- 2895 • Connect the DUT to the Test System.
- 2896 • Configure the Test System to transmit an otherwise valid HS image data sequence to the DUT,
 2897 using a T_{3-PREBEGIN} value of 7UI, as described above.
- 2898 • Repeat the previous step, incrementing the T_{3-PREBEGIN} value (or use a binary search) until the DUT
 2899 successfully and consistently receives the HS image data without error.
- 2900 • Record the value as the DUT's T_{3-PREBEGIN} detection threshold.

2901 **Observable Results**

- 2902 • Verify that the DUT's T_{3-PREBEGIN} detection threshold is between 7 and 448UI.

2903 **Possible Problems**

2904 None.

Test 2.4.4 HS-RX T₃-PROGSEQ Tolerance

Purpose

To verify that the DUT's HS-RX can tolerate reception of conformant values for T₃-PROGSEQ.

References

- [1] C-PHY Specification, Figure 23
- [2] Ibid, Section 6.4.4
- [3] Ibid, Section 6.9

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

As part of the process for switching a Lane into HS mode, the C-PHY specification includes requirements for the T₃-PROGSEQ interval, which is shown in the figure below[1].

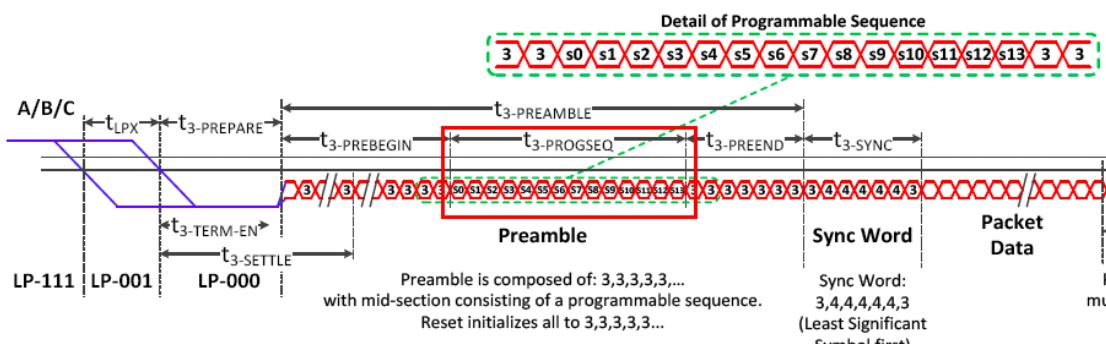


Figure 2.4.4-1: T₃-PROGSEQ Interval

The specification also describes the T₃-PROGSEQ interval[2], and defines its length[3].

- 608 The master may output a programmable sequence during t₃-PROGSEQ of the preamble, if it is enabled using a programmable sequence enable bit such as the MSB of the control register described in section 12.5.3. The symbol values transmitted in the programmable sequence, or whether the programmable sequence is used at all, is a choice of the system designer.

Figure 2.4.4-2: T₃-PROGSEQ Interval Description

$$\begin{aligned}
 & t_{3\text{-SETTLE}} > t_{3\text{-PREPARE}} \\
 & t_{3\text{-SETTLE}} < t_{3\text{-PREPARE}} + t_{3\text{-PREAMBLE}} \\
 & t_{3\text{-PREAMBLE}} = t_{3\text{-PREBEGIN}} + t_{3\text{-PROGSEQ}} + t_{3\text{-PREEND}}
 \end{aligned}
 \quad
 \begin{aligned}
 t_{3\text{-PROGSEQ}} &= 14 \text{ UI or } 0 \text{ UI} \\
 t_{3\text{-PREEND}} &= 7 \text{ UI} \\
 t_{3\text{-SYNC}} &= 7 \text{ UI}
 \end{aligned}$$

Figure 2.4.4-3: T₃-PROGSEQ Length

Note that the specification defines this parameter from the transmitter's perspective. While there is no explicit statement requiring specific receiver requirements for T₃-PROGSEQ, it is inferred as a requirement in this case, as a receiver must be able to tolerate most valid TX values for T₃-PROGSEQ, otherwise interoperability problems will occur. Certain control sequences, such as the Sync Word and Post, should be avoided in T₃-PROGSEQ to prevent unintended operation.

In this test, HS bursts containing valid image data will be sent to the DUT with the T₃-PROGSEQ enabled. The test cases are listed in the table below. Note that the exact value of T₃-PROGSEQ is not defined in the specification, and neither is the expected behavior upon reception, as these specifics are outside the scope of the specification. The purpose of this test will be to verify that inclusion of a default T₃-PROGSEQ value does not adversely impact the DUT's ability to receive valid image data. The sequence for this test may in theory be any valid sequence, but for this test a sequence of "434343434343" will be used, and will be enabled for every burst.

Table 2.4.4-1: HS-RX T₃-PROGSEQ Test Cases

Case #	T3-PROGSEQ	Notes
1	(14UI)	Default T ₃ -PROGSEQ test case

2934

Also, note that all other timing parameters should be set to nominal values for this test. The recommended values are listed in the table below.

Table 2.4.4-2: HS-RX T₃-PROGSEQ Test Nominal Timer Values

TLPX	T3-PREPARE	T3-PREBEGIN	T3-PREEND	T3-SYNC	T3-POST
50ns	70ns	448UI	7UI	7UI	224UI

2937

For all test cases, the DUT must successfully receive the HS data without error in order to be considered conformant.

Test Setup

See Annex B.2.

Test Procedure

- Connect the DUT to the Test System.
- Configure the Test System to transmit an otherwise valid HS image data sequence to the DUT, using the T₃-PROGSEQ Test Case #1 values as described above.
- Verify that the DUT successfully received the HS image data without error.

Observable Results

- For all test cases, verify that the DUT successfully received the HS burst data without error.

Possible Problems

None.

Test 2.4.5 Test 2.4.5 HS-RX $T_{3\text{-POST}}$ Tolerance

Purpose

To verify that the DUT's HS-RX can tolerate reception of conformant values for $T_{3\text{-POST}}$.

References

- [1] C-PHY Specification, Figure 23
- [2] Ibid, Section 6.4.4
- [3] Ibid, Section 6.9

Resource Requirements

See Annex A.2.

Last Technical Modification

October 27, 2014

Discussion

As part of the process for switching a Lane out of HS mode, the C-PHY specification includes requirements for the $T_{3\text{-POST}}$ interval, which is shown in the figure below[1].

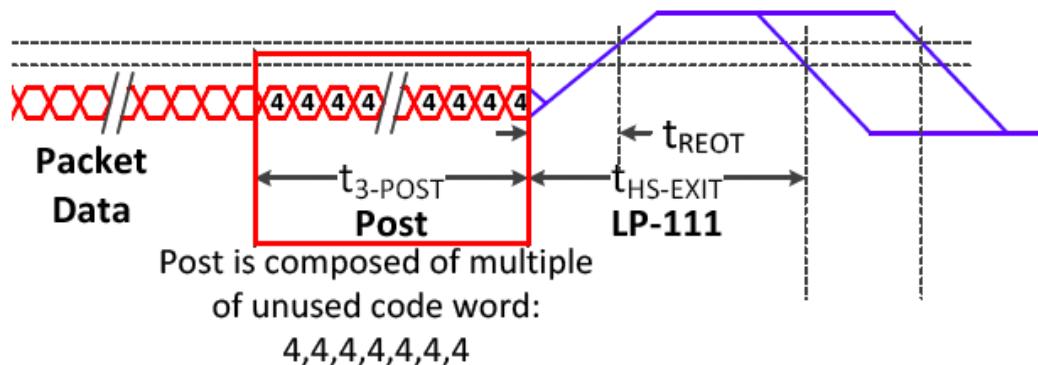


Figure 2.4.5-1: $T_{3\text{-POST}}$ Interval

The specification also describes the $T_{3\text{-POST}}$ interval[2], and provides a recommended length range[3].

618 The end of Packet Data is identified by a unique sequence of "4" symbols in $t_{3\text{-POST}}$. The receiver identifies
 619 the end of Packet Data when it detects a sequence of seven consecutive "4" symbols. The Post field may
 620 often consist of multiple groups of seven "4" symbols to provide a sufficient number of clocks to the upper
 621 layer protocol to clear out any pipeline stages that may contain received data. The length of the Post field is
 622 a programmable value set in the master, for example: the post length field of the register described in section
 623 12.5.4.

Figure 2.4.5-2: $T_{3\text{-POST}}$ Interval Definition

756 example method to specify the length of $t_{3\text{-PREBEGIN}}$ is provided in section 12.5.3. $t_{3\text{-POST}}$ should be
 757 adjustable from 7 UI minimum to 224 UI maximum in increments of 7 UI. An example method to specify
 758 the length of $t_{3\text{-POST}}$ is provided in section 12.5.4.

Figure 2.4.5-3: $T_{3\text{-POST}}$ Interval Length

2968 Note that the specification defines this parameter loosely, and uses a ‘should’ statement instead of a ‘shall’.
 2969 This is defined from the transmitter’s perspective, however. Note that while there is no explicit statement
 2970 requiring specific receiver requirements for T₃-POST, it is inferred that a receiver must have a detection
 2971 threshold for T₃-POST that is between 7 and 224UI, otherwise interoperability problems will occur.

2972 The recommended TX conformance range for T₃-POST is defined as 7 to 224 UI. In this test, HS bursts
 2973 containing valid image data will be sent to the DUT using a minimum value of T₃-POST (7UI). The value of
 2974 T₃-POST will be increased in 7UI increments (or a binary search can be used) until the point is found where
 2975 DUT begins to successfully and consistently receive the bursts. The minimum T₃-POST value for which the
 2976 DUT consistently receives the bursts shall be recorded as the DUT’s T₃-POST detection threshold value.

2977 Also, note that all other timing parameters should be set to nominal values for this test. The recommended
 2978 values are listed in the table below.

Table 2.4.5-1: HS-RX T₃-POST Test Nominal Timer Values

T _L PX	T ₃ -PREPARE	T ₃ -PREBEGIN	T ₃ -PROGSEQ	T ₃ -PREEND	T ₃ -SYNC
50ns	70ns	448UI	Disabled (0UI)	7UI	7UI

2979
 2980 The DUT’s T₃-POST detection threshold value must be between 7 and 224UI in order to be considered
 2981 conformant.

Test Setup

2983 See Annex B.2.

Test Procedure

- 2985 • Connect the DUT to the Test System.
- 2986 • Configure the Test System to transmit an otherwise valid HS image data sequence to the DUT,
 2987 using a T₃-POST value of 7UI, as described above.
- 2988 • Repeat the previous step, incrementing the T₃-POST value (or use a binary search) until the DUT
 2989 successfully and consistently receives the HS image data without error.
- 2990 • Record the value as the DUT’s T₃-POST detection threshold.

Observable Results

- 2992 • Verify that the DUT’s T₃-POST detection threshold is between 7 and 224UI.

Possible Problems

2994 None.

This page intentionally left blank.

Section 3 Interface Impedance and S-Parameters

Overview

This section of tests verifies various S-parameter and low-frequency impedance requirements of C-PHY products, found in Sections 8 and 9 of [\[MIPI01\]](#).

- Group 1 verifies the S-parameter characteristics of the HS-TX interface.
- Group 2 verifies the S-parameter characteristics of the HS-RX interface.
- Group 3 verifies several impedance-related requirements of the LP-TX and LP-RX interfaces.

Comments and questions regarding the documentation and/or implementation of these tests are welcome, and can be sent to test-wg@mipi.org.

Group 1 HS-TX S-Parameters and Impedance

3003 Overview

3004 This group of tests verifies the HS-TX interface S-Parameter and impedance requirements defined in
3005 Section 8.7 of the C-PHY Specification.

3006 Status

3007 The test names, Discussion sections, and Procedures are considered to be in release form (i.e., sufficiently
3008 documented to reflect the current state of implementation), and most tests have been successfully
3009 performed on at least one device. Additional modifications to both the test descriptions and
3010 implementations may continue if new opportunities for improvement are identified.

Test 3.1.1 HS-TX Differential Return Loss (SDD22)

Purpose

To verify that the Differential Return Loss of the DUT's HS transmitters exceeds the minimum conformance limits.

References

- [1] C-PHY Specification, Figure 36
- [2] Ibid, Section 8.7.1
- [3] Ibid, Section 8.3

Resource Requirements

See Annex A.3.

Last Technical Modification

November 10, 2014

Discussion

Section 8 of the C-PHY Specification defines the general interconnect and lane configuration requirements for C-PHY products. Section 8.7 defines the HS Driver and Receiver S-parameter specifications, which includes a specification for TX Differential Return Loss. The specification is defined in terms of a scalable frequency-domain template, reproduced in the figure below[1].

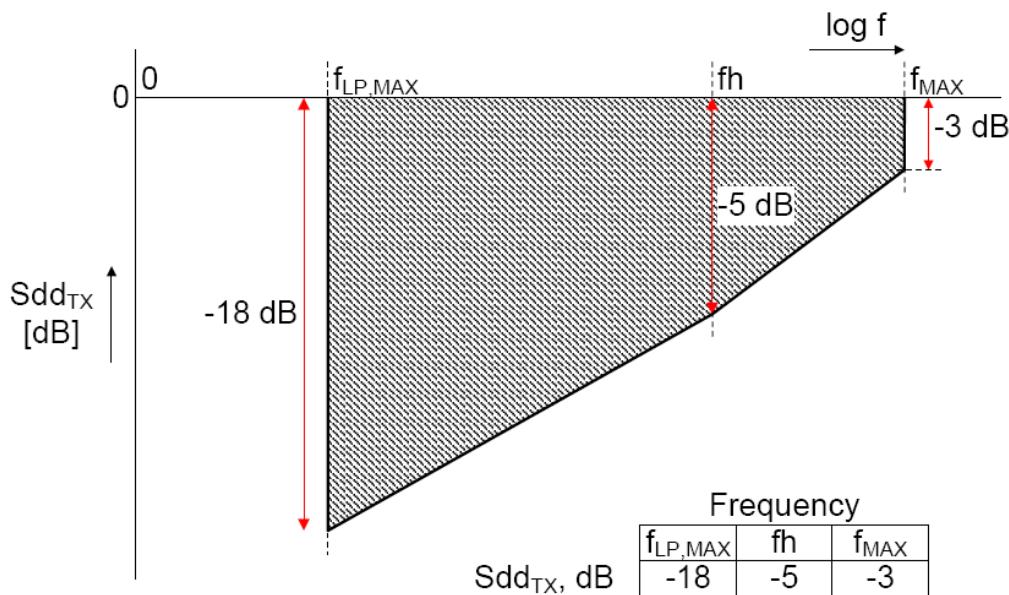


Figure 36 Differential Reflection Template for Lane Module Transmitters

Figure 3.1.1-1: HS-TX Differential Return Loss Conformance Limits

3028 The specification states[2],

967 The differential reflection of a lane module in high-speed TX mode should conform to the limits specified
 968 by the template shown in Figure 36.

Figure 3.1.1-2: Differential Return Loss Specification Requirement

3030 Note that the specification is intentionally defined to be scalable relative to the operating speed of the DUT.
 3031 The parameters f_{MAX} , f_h , and $f_{LP,MAX}$ shown in the figure above are defined below[3].

$$f_{MAX} = \frac{3}{4} \cdot \frac{1}{UI_{INST,MIN}}$$

Figure 3.1.1-3: f_{MAX} Definition

3033 906 The frequency ‘ f_h ’ is the highest fundamental frequency for data transmission and is equal to $1/(2*UI_{INST,MIN})$.

Figure 3.1.1-4: f_h Definition

3034 911 The frequency ‘ $f_{LP,MAX}$ ’ is the maximum toggle frequency for low-power mode.

Figure 3.1.1-5: $f_{LP,MAX}$ Definition

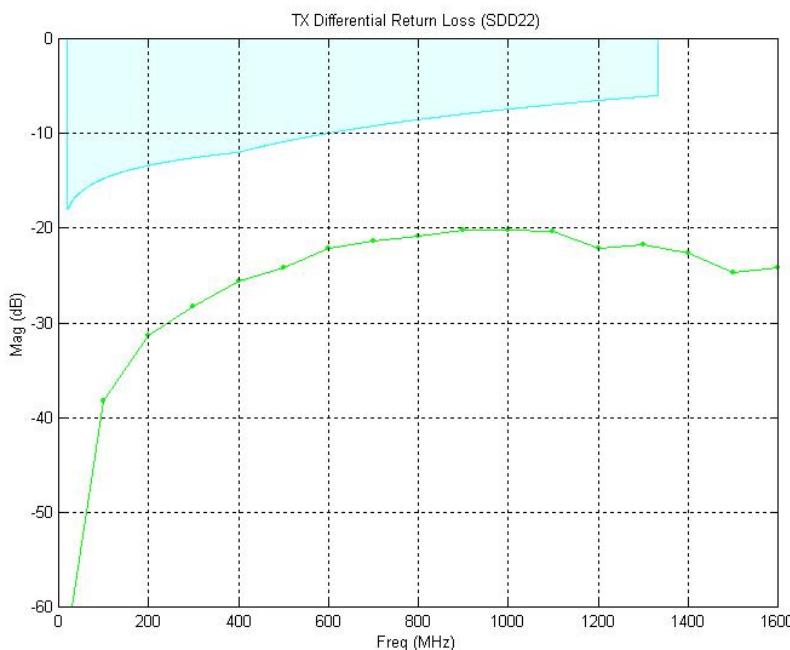
3035 Note that while $f_{LP,MAX}$ is a defined term similar to f_{MAX} , it is not intended as a DUT-specific variable, but
 3036 rather a fixed value, which is 20MHz.

3037 Also, given that this is a transmitter specification, it is necessary to have the DUT in a normal powered-on
 3038 and operational state where it is actively transmitting HS data signaling during the measurement. However,
 3039 care must be taken to ensure that the signaling emitted from the active transmitter does not adversely
 3040 impact the measurement results, and is suitably removed from the measurement. If a Vector Network
 3041 Analyzer (VNA) is used for the measurement, this can be accomplished by setting a sufficiently high
 3042 output power level and narrow IFBW setting on the VNA, and configuring the DUT to transmit a non-
 3043 periodic (i.e., pseudo-random) data pattern, in order to minimize the transmitted energy in any particular
 3044 narrow IF band.

3045 If a Time-Domain Reflectometer (TDR) is used for the measurement, time-domain averaging can be used
 3046 to cancel out the energy being transmitted by the DUT. Because the DUT’s transmitted HS signaling is not
 3047 time-correlated to the incident TDR stimulus pulses (and hence the pulse reflections from the DUT
 3048 interface), the DUT’s signaling will average out over time if averaging is enabled on the TDR. Note that for
 3049 the TDR case, a high-frequency repeating HS pattern is preferred over a pseudo-random pattern, as this
 3050 type of pattern is more easily removed by the averaging operation. For C-PHY, an alternating Strong
 3051 1/Strong 0 pattern is recommended. This can be accomplished by transmitting a +x/-x or +z/-z state
 3052 sequence for the A line, +y/-y or +x/-x for the B line, or +z/-z or +y/-y sequence for the C line. Note this
 3053 will require the use of a test pattern generator within the DUT.

3054 Also note that this Test Suite adopts the S-parameter naming convention such that an HS-RX is always
 3055 described as differential Port 1, and an HS-TX is differential Port 2. (Hence SDD22 for HS-TX Differential
 3056 Return Loss.) The measurement will be performed for all pairs (A-B, B-C, and C-A) of all Lanes.

3057 The HS-TX Differential Return Loss response must fall below the grayed out region shown in the figure
 3058 above in order to be considered conformant (e.g., there must be *at least* 18dB of return loss at $f_{LP,MAX}$, etc).
 3059 An example measurement result showing a conformant Differential Return Loss response is shown in the
 3060 figure below.



3061 **Figure 3.1.1-6: Example Conformant HS-TX Differential Return Loss Result**

3062 **Test Setup**

3063 See Annex B.3.1.

3064 **Test Procedure**

- 3065 • Compute the value of f_{MAX} for the DUT as described above.
3066 • Power on and configure the DUT to force its HS-TX into a fixed HS state, transmitting a
3067 continuous HS pattern on all Lanes.
3068 • Calibrate and configure the Test System for a Differential Return Loss measurement (SDD22)
3069 over the frequency range $f_{LP,MAX}$ (20MHz) to f_{MAX} .
3070 • Connect the DUT's Lane 0 transmitter to the Test System (A-B pair).
3071 • Measure the SDD22 HS-TX Differential Return Loss.
3072 • Repeat the previous two steps for the B-C and C-A pairs.
3073 • Repeat the previous three steps for all other Lanes.

3074 **Observable Results**

- 3075 • For all pair of all Lanes, verify that the SDD22 HS-TX Differential Return Loss meets or exceeds
3076 the limits shown in Figure 3.1.1-1 above.

3077 **Possible Problems**

3078 This measurement requires the DUT to be able to force its HS-TX Lanes into a continuous HS-only mode.
3079 This is considered vendor-specific functionality, and is outside the scope of normal operating behavior.
3080 However, it is necessary in order to make the proper measurements on the HS-TX. If the DUT does not
3081 support this type of functionality, the measurement may not be able to be performed.

Test 3.1.2 HS-TX Common-Mode Return Loss (SCC22)**Purpose**

To verify that the Common-Mode Return Loss of the DUT's HS transmitters exceeds the minimum conformance limits.

References

[1] C-PHY Specification, Section 8.7.2

Resource Requirements

See Annex A.3.

Last Technical Modification

October 27, 2014

Discussion

Section 8 of the C-PHY Specification defines the general interconnect and lane configuration requirements for C-PHY products. Section 8.7 defines the Driver and Receiver S-parameter specifications, which includes a specification for TX Common-Mode Return Loss.

The specification states[1],

970 The common-mode return loss specification is different for a high-speed TX and RX mode, because the RX
971 is not DC terminated to ground. The common mode reflection of a lane module in high-speed TX mode
972 should be less than -3dB from $f_{LP,MAX}$ up to f_{MAX} . The common mode reflection of a lane module in high-
973 speed RX mode should conform to the limits specified by the template shown in Figure 37. Assuming a high

Figure 3.1.2-1: TX Common-Mode Return Loss Specification Requirement

This test verifies the TX requirement.

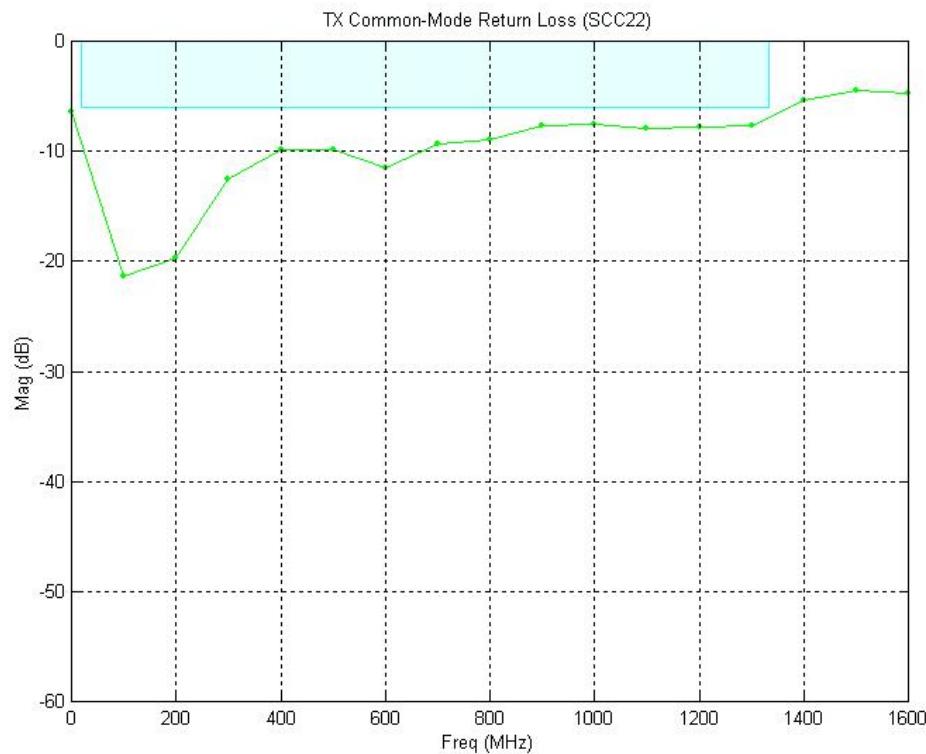
Note that because the TX Common-Mode Return Loss specification is defined simply as a straight limit line across the range ($f_{LP,MAX}$ to f_{MAX}), no template is defined for the TX case. (Note that $f_{LP,MAX}$ is taken to be a fixed value of 20MHz, see Discussion of Test 3.1.1.)

Also, given that this is a transmitter specification, it is necessary to have the DUT in a normal powered-on and operational state where it is actively transmitting data signaling during the measurement. (See comments in Test 3.1.1 Discussion regarding transmitted data patterns.)

Also, this test will be performed for all pairs (A-B, B-C, and C-A) of all Lanes, and will use the same f_{MAX} value for all Lanes, which was computed in the previous test. (See Test 3.1.1 Discussion.)

Also, note that this Test Suite adopts the S-parameter naming convention such that an HS-RX is always described as differential Port 1, and an HS-TX is differential Port 2. (Hence SCC22 for HS-TX Common-Mode Return Loss.)

For all Lanes, the HS-TX Common-Mode Return Loss must be greater than 3dB across the range ($f_{LP,MAX}$ to f_{MAX}) in order to be considered conformant. An example measurement result showing a conformant Common-Mode Return Loss response is shown in the figure below.



3112

Figure 3.1.2-2: Example Conformant HS-TX Common-Mode Return Loss Result**Test Setup**

3114 See Annex B.3.1.

Test Procedure

- 3116 • Obtain the value of f_{MAX} for the DUT that was used in Test 3.1.1.
- 3117 • Power on and configure the DUT to force its HS-TX into a fixed HS state, transmitting a
- 3118 continuous HS pattern on all Lanes.
- 3119 • Calibrate and configure the Test System for a Common-Mode Return Loss measurement (SCC22)
- 3120 over the frequency range ($f_{LP,MAX}$ to f_{MAX}).
- 3121 • Connect the DUT's Lane 0 transmitter to the Test System (A-B pair).
- 3122 • Measure the SCC22 HS-TX Common-Mode Return Loss.
- 3123 • Repeat the previous two steps for the B-C and C-A pairs.
- 3124 • Repeat the previous three steps for all other Lanes.

Observable Results

- 3126 • For all pairs of all Lanes, verify that the SCC22 HS-TX Common-Mode Return Loss is greater
- 3127 than 3dB across the frequency range $f_{LP,MAX}$ to f_{MAX} .

Possible Problems

3129 See Possible Problems comments for Test 3.1.1. The same applies to this test.

Test 3.1.3 HS-TX Mode Conversion Limits (SDC22)**Purpose**

To verify that the Mode Conversion S-parameters of the DUT's HS transmitters exceed the minimum conformance limits.

References

[1] C-PHY Specification, Section 8.7.3

Resource Requirements

See Annex A.3.

Last Technical Modification

October 27, 2014

Discussion

Section 8 of the C-PHY Specification defines the general interconnect and lane configuration requirements for C-PHY products. Section 8.7 defines the Driver and Receiver S-parameter specifications, which includes a specification for TX Mode Conversion Limits.

The specification states[1],

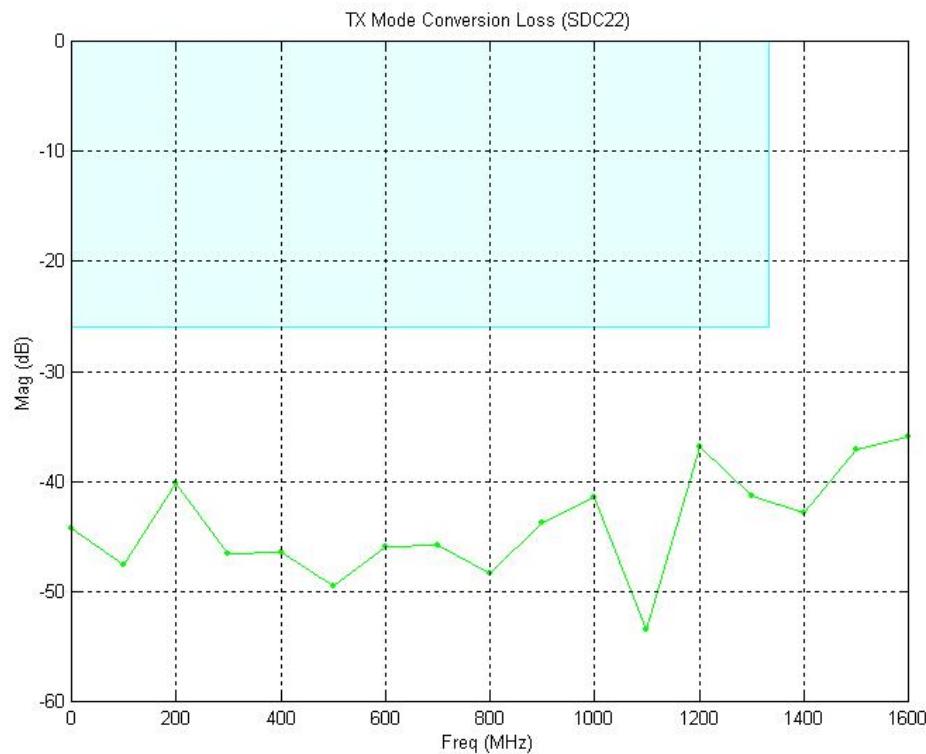
978 The differential to common-mode conversion limits of TX and RX should be -26dB up to f_{MAX} .

Figure 3.1.3-1: Mode Conversion Specification Requirement

Note that mode conversion S-parameters include SDC22 and SCD22 (assuming the TX port of the DUT is considered Differential Port 2, which is the convention used in this test suite, see Test 3.1.1 Discussion.) SDC22 involves launching a common-mode incident stimulus at the DUT interface and measuring the differential reflected energy. SCD22 involves launching a differential incident stimulus at the DUT interface and measuring the common-mode reflected energy. Both measurements offer a measure of the asymmetry or imbalance between the two single-ended trace responses that make up the differential pair (e.g., in the SDC22 case, any imbalance will result in a difference in the reflected energy on each single-ended conductor when stimulated with the same common-mode input). For the purposes of this measurement, SDC22 and SCD22 will yield identical results, hence only SDC22 will be measured.

(The methodology for this test is otherwise identical to Tests 3.1.1 and 3.1.2, except that the SDC22 S-parameter will be measured over the frequency range 0 to f_{MAX} . The measurement will be made for all pairs (A-B, B-C, and C-A) of all Lanes.)

3157 The HS-TX Mode Conversion Loss shall be greater than 26dB over the frequency range 0 to f_{MAX} in order
3158 to be considered conformant. An example measurement result showing a conformant Mode Conversion
3159 Loss response is shown in the figure below.



3160

Figure 3.1.3-2: Example Conformant HS-TX Mode Conversion Loss Result**Test Setup**

3162 See Annex B.1.3.

Test Procedure

- 3164 • Obtain the value of f_{MAX} for the DUT that was used in Test 3.1.1.
- 3165 • Power on and configure the DUT to force its HS-TX into a fixed HS state, transmitting a
- 3166 continuous HS pattern on all Lanes.
- 3167 • Calibrate and configure the Test System for an SDC22 measurement over the frequency range 0 to
- 3168 f_{MAX} .
- 3169 • Connect the DUT's Lane 0 transmitter to the Test System (A-B pair).
- 3170 • Measure the SDC22 HS-TX Mode Conversion Loss.
- 3171 • Repeat the previous two steps for the B-C and C-A pairs.
- 3172 • Repeat the previous three steps for all other Lanes.

Observable Results

- 3174 • For all pairs of all Lanes, verify that the SDC22 HS-TX Mode Conversion Loss is greater than
- 3175 26dB across the frequency range 0 to f_{MAX} .

Possible Problems

3177 See Possible Problems comments for Test 3.1.1. The same applies to this test.

Test 3.1.4 HS-TX Single-Ended Output Impedance (Z_{os})

Purpose

To verify that the Single-Ended Output Impedance (Z_{os}) of the DUT's HS transmitters is within the conformance limits.

References

- [1] C-PHY Specification, Section 9.1.1
- [2] Ibid, Table 22

Resource Requirements

See Annex A.3.

Last Technical Modification

November 10, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for Z_{os} , which is a device's High-Speed Single-Ended Output Impedance.

The specification states[1],

1051 The single-ended output impedance of the transmitter at the A, B and C pins is denoted by Z_{os} .

Figure 3.1.4-1: Z_{os} Specification Definition

The specification also states[1],

1056 The output impedance Z_{os} and the output impedance mismatch ΔZ_{os} shall be compliant with Table 22 for all
1057 six possible high-speed wire states and for all allowed loading conditions. It is recommended that
1058 implementations keep the output impedance during state transitions as close as possible to the steady state
1059 value. The output impedance Z_{os} can be determined by injecting an AC current into the A, B and C pins and
1060 measuring the peak-to-peak voltage amplitude.

Figure 3.1.4-2: Z_{os} Specification Measurement

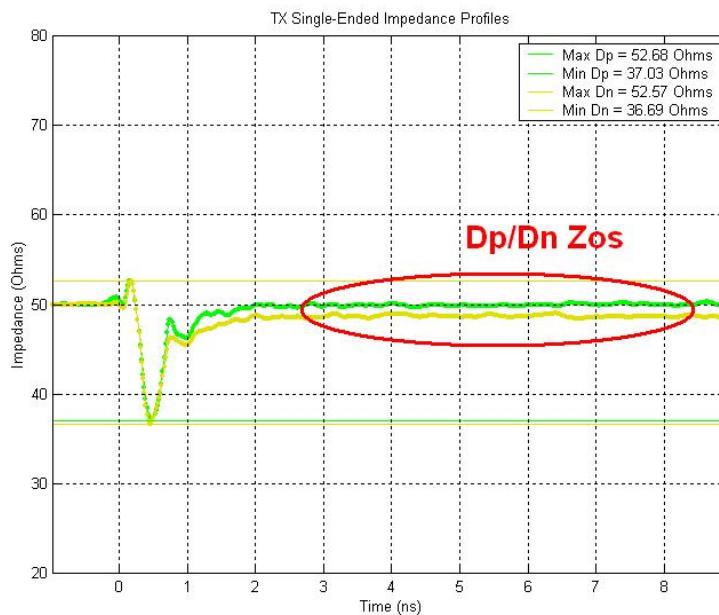
And the specification also defines conformance limits shown below[2].

Z_{os}	Single ended output impedance	40	50	60	Ω	
3197						

Figure 3.1.4-3: Z_{os} Conformance Requirements

While the methodology described above is one possible valid methodology for this measurement, a TDR-based approach is used for the purposes of this test suite. (This approach is chosen primarily because it allows all of the HS-TX and HS-RX S-parameter and impedance tests to be performed using a single setup.)

The TDR-based approach involves measuring the single-ended impedance profiles for the V_A , V_B , and V_C pins of the HS transceiver, and measuring Z_{os} as the final, settled single-ended termination value for each line. An example measurement is shown in the figure below.



3205

Figure 3.1.4-4: Example HS-TX Z_{OS} Measurement

3206 Note that the test pattern used for this test should be an alternating high/low high frequency pattern. (See
 3207 comments in Test 3.1.1 Discussion regarding appropriate test patterns.)

3208 The measured Z_{OS} for the V_A, V_B, and V_C pins for all Lanes shall be within the range of 40 to 60 Ohms in
 3209 order to be considered conformant[2].

3210 **Test Setup**

3211 See Annex B.3.1.

3212 **Test Procedure**

- 3213 • Power on and configure the DUT to force its HS-TX into a fixed HS state, transmitting a
 3214 continuous HS pattern on all Lanes.
- 3215 • Calibrate and configure the Test System for a single-ended impedance profile measurement.
- 3216 • Connect the DUT's Lane 0 transmitter to the Test System.
- 3217 • Measure Z_{OS} for the V_A pin, as described above.
- 3218 • Repeat the previous step for the V_B and V_C pins.
- 3219 • Repeat the previous three steps for all other Lanes.

3220 **Observable Results**

- 3221 • For all Lanes, verify that Z_{OS} is between 40 and 60 Ohms for the V_A, V_B, and V_C pins.

3222 **Possible Problems**

3223 See Possible Problems comments for Test 3.1.1. The same applies to this test.

Test 3.1.5 HS-TX Single-Ended Output Impedance Mismatch (ΔZ_{OS})

Purpose

To verify that the Single-Ended Output Impedance Mismatch (ΔZ_{OS}) of the DUT's HS transmitter is within the conformance limits.

References

- [1] C-PHY Specification, Section 9.1.1
- [2] Ibid, Table 22

Resource Requirements

None.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for ΔZ_{OS} , which is a device's High-Speed Single-Ended Output Impedance Mismatch. A copy of the specification text is reproduced below[1].

1051 The single-ended output impedance of the transmitter at the A, B and C pins is denoted by Z_{OS} . ΔZ_{OS} is the
 1052 mismatch of the single ended output impedances at the A, B and C pins, denoted by Z_{OS_A} , Z_{OS_B} and Z_{OS_C} ,
 1053 respectively. This mismatch is defined as the ratio of the difference between the largest and smallest value of
 1054 Z_{OS_A} , Z_{OS_B} and Z_{OS_C} and the average of those impedances:

$$1055 \quad \Delta Z_{OS} = 3 \cdot \frac{\max(Z_{OS_A}, Z_{OS_B}, Z_{OS_C}) - \min(Z_{OS_A}, Z_{OS_B}, Z_{OS_C})}{Z_{OS_A} + Z_{OS_B} + Z_{OS_C}}$$

1056 The output impedance Z_{OS} and the output impedance mismatch ΔZ_{OS} shall be compliant with Table 22 for all
 1057 six possible high-speed wire states and for all allowed loading conditions. It is recommended that

Figure 3.1.5-1: ΔZ_{OS} Specification

The specification also provides limits for ΔZ_{OS} , shown below[2].

ΔZ_{OS}	Single ended output impedance mismatch			10	%	
-----------------	--	--	--	----	---	--

Figure 3.1.5-2: ΔZ_{OS} Conformance Requirements

The procedure for this test simply involves computing ΔZ_{OS} from the measured Z_{OS} values obtained in Test 3.1.4. The ΔZ_{OS} value will be computed for each Lane.

For all Lanes, the computed ΔZ_{OS} value shall be less than 10% in order to be considered conformant[2].

Test Setup

None.

3246 **Test Procedure**

- 3247 • Obtain the Z_{OS} values for each Lane from Test 3.1.4.
3248 • For each Lane, compute ΔZ_{OS} as described above.

3249 **Observable Results**

- 3250 • For all Lanes, verify that ΔZ_{OS} is less than 10%.

3251 **Possible Problems**

3252 None.

Group 2 HS-RX S-Parameters and Impedance

3253 Overview

3254 This group of tests verifies the HS-RX interface S-Parameter and impedance requirements defined in
3255 Section 8.7 of the C-PHY Specification.

3256 Status

3257 The test names, Discussion sections, and Procedures are considered to be in release form (i.e., sufficiently
3258 documented to reflect the current state of implementation), and most tests have been successfully
3259 performed on at least one device. Additional modifications to both the test descriptions and
3260 implementations may continue if new opportunities for improvement are identified.

Test 3.2.1 HS-RX Differential Return Loss (SDD11)

Purpose

To verify that the Differential Return Loss of the DUT's HS receivers exceeds the minimum conformance limits.

References

[1] C-PHY Specification, Figure 35

Resource Requirements

See Annex A.3.

Last Technical Modification

October 27, 2014

Discussion

Section 8 of the C-PHY Specification defines the general interconnect and lane configuration requirements for C-PHY products. Section 8.7 defines the Driver and Receiver S-parameter specifications, which includes a specification for RX Differential Return Loss. The specification is defined in terms of a scalable frequency-domain template, reproduced in the figure below[1].

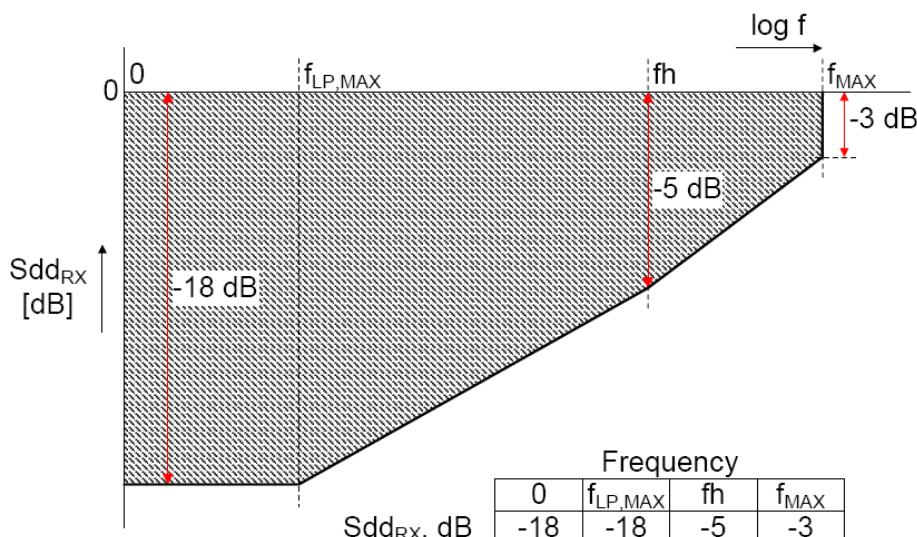


Figure 35 Differential Reflection Template for Lane Module Receivers

Figure 3.2.1-1: HS-RX Differential Return Loss Conformance Limits

The specification states[2],

- 964 The differential reflection of a lane module in high-speed RX mode should conform to the limits specified
965 by the template shown in Figure 35.

Figure 3.2.1-2: HS-RX Differential Return Loss Conformance Requirement

Note that the methodology for this test is essentially the same as the HS transmitter measurement of Test 3.1.1, except the measurement is performed on an HS receiver, and the frequency range is 0 to f_{MAX} , rather than $f_{LP,MAX}$ to f_{MAX} .

Also, rather than requiring the DUT to be forced into a continuous HS transmitting state as was required for the TX measurement, this test requires that the DUT be forced into a state where its HS-RX termination is permanently enabled for the duration of the measurement. This functionality is also considered a vendor-specific feature, and is outside the scope of normal operating behavior, however it is necessary in order for the measurement to be performed.

The Differential Return Loss response must fall below the grayed out region shown in the template in order to be deemed conformant (e.g., there must be *at least* 18dB of return loss at $f_{LP,MAX}$, etc). An example measurement result showing a conformant Differential Return Loss response is shown in the figure below.

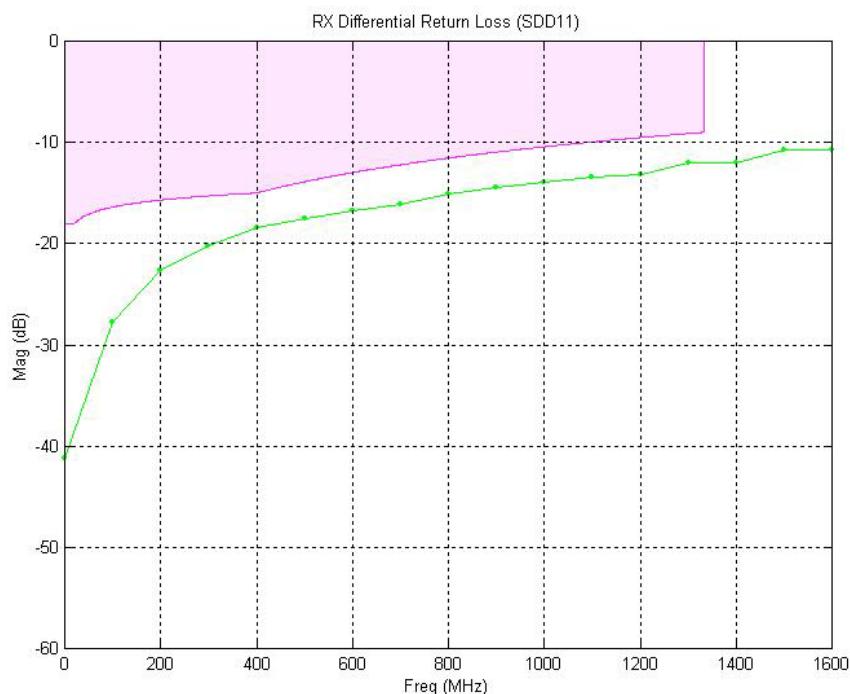


Figure 3.2.1-3: Example Conformant HS-RX Differential Return Loss Result

Test Setup

See Annex B.3.1.

Test Procedure

- Obtain the value of f_{MAX} for the DUT that was used in Test 3.1.1.
- Power on and configure the DUT to force its RX into fixed state where the HS-RX termination is enabled.
- Calibrate and configure the Test System for a Differential Return Loss measurement (SDD11) over the frequency range 0 to f_{MAX} .
- Connect the DUT's Lane 0 receiver to the Test System (A-B pair).
- Measure the SDD11 HS-RX Differential Return Loss.
- Repeat the previous two steps for the B-C and C-A pairs.
- Repeat the previous three steps for all other Lanes.

3302 Observable Results

- 3303 • For all pairs of all Lanes, verify that the SDD11 HS-RX Differential Return Loss meets or exceeds
3304 the limits shown in the figure above.

3305 Possible Problems

3306 As mentioned in the Discussion above, it is mandatory that the DUT's HS-RX termination be forced into a
3307 fixed enabled state in order to properly perform the measurement. Erroneous results may occur if the DUT
3308 is incorrectly configured for any other C-PHY state other than High-Speed (e.g., LP Control or Escape).

Test 3.2.2 HS-RX Common-Mode Return Loss (SCC11)

Purpose

To verify that the Common-Mode Return Loss of the DUT's HS receivers exceeds the minimum conformance limits.

References

- [1] C-PHY Specification, Figure 37
- [2] Ibid, Section 8.7.2
- [3] Ibid, Section 8.3
- [4] Ibid, Table 29

Resource Requirements

See Annex A.3.

Last Technical Modification

October 27, 2014

Discussion

Section 8 of the C-PHY Specification defines the general interconnect and lane configuration requirements for C-PHY products. Section 8.7 defines the Driver and Receiver S-parameter specifications, which includes a specification for RX Common-Mode Return Loss. The specification is defined in terms of a scalable frequency-domain template, reproduced in the figure below[1].

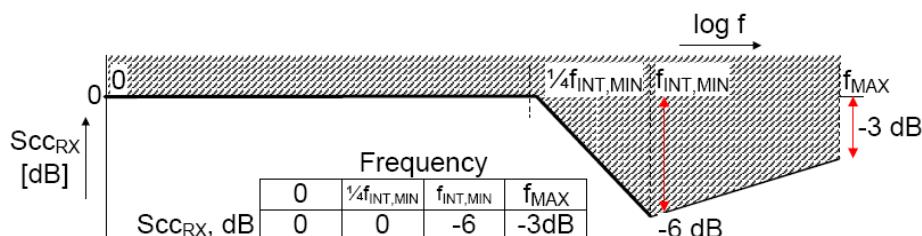


Figure 37 Template for RX Common-Mode Return Loss

Figure 3.2.2-1: Common-Mode Return Loss Conformance Limits

The specification states[2],

- 972 should be less than -3dB from $f_{LP,MAX}$ up to f_{MAX} . The common mode reflection of a lane module in high-speed RX mode should conform to the limits specified by the template shown in Figure 37. Assuming a high
- 973 speed RX mode, the common mode reflection should be less than -3dB from $f_{LP,MAX}$ up to f_{MAX} .

Figure 3.2.2-2: Common-Mode Reflection Specification Requirement

Regarding the definition of f_{INT} , the specification states[3],

- 912 RF interference frequencies are denoted by ' f_{INT} ', where $f_{INT,MIN}$ defines the lower bound for the band of
- 913 relevant RF interferers. The frequency f_{MAX} is defined by

Figure 3.2.2-3: f_{INT} Specification Definition

The value of $f_{INT,MIN}$ is specified in the specification as a fixed value of 450MHz[4].

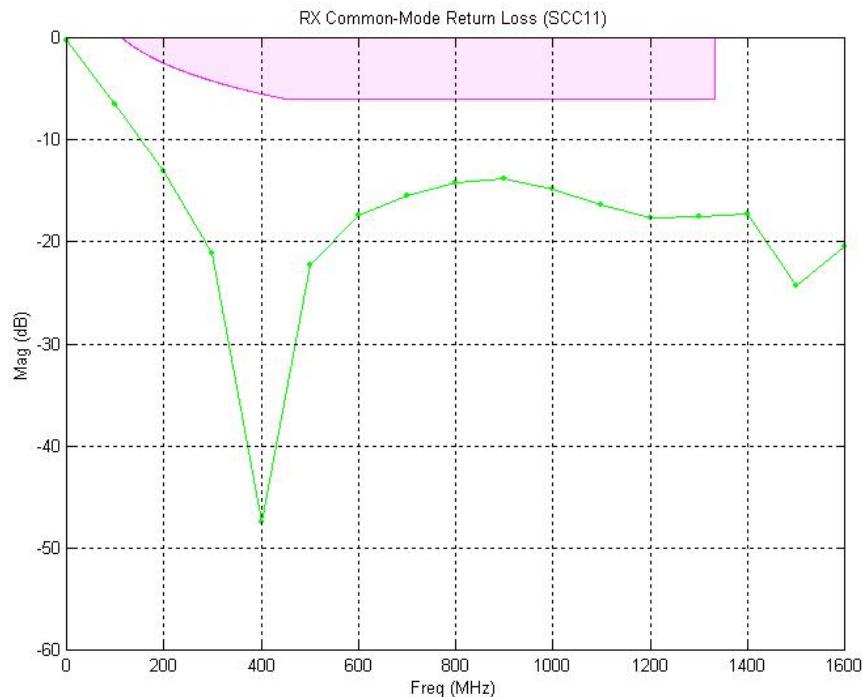
Table 29 LP Receiver AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V·ps	1, 2, 3
T_{MIN-RX}	Minimum pulse width response	20			ns	4
V_{INT}	Peak interference amplitude			200	mV	
f_{INT}	Interference frequency	450			MHz	

Figure 3.2.2-4: f_{INT} Specification Value

The general methodology for this test is otherwise identical to Test 3.2.1, except the SCC11 S-parameter is measured, and different conformance frequencies/limits are applied.

The RX Common-Mode Return Loss response must fall below the grayed out region shown in the template in order to be considered conformant (e.g., there must be *at least* 6dB of return loss at $f_{INT,MIN}$, etc). An example measurement result showing a conformant Common-Mode Return Loss response is shown in the figure below.

**Figure 3.2.2-5: Example Conformant HS-RX Common-Mode Return Loss Result**

Test Setup

See Annex B.3.1.

3342 **Test Procedure**

- 3343 • Obtain the value of f_{MAX} for the DUT that was used in Test 3.1.1.
- 3344 • Power on and configure the DUT to force its RX into fixed state where the HS-RX termination is
3345 enabled.
- 3346 • Calibrate and configure the Test System for a Common-Mode Return Loss measurement (SCC11)
3347 over the frequency range 0 to f_{MAX} .
- 3348 • Connect the DUT's Lane 0 receiver to the Test System (A-B pair).
- 3349 • Measure the SCC11 HS-RX Common-Mode Return Loss.
- 3350 • Repeat the previous two steps for the B-C and C-A pairs.
- 3351 • Repeat the previous two steps for all other Lanes.

3352 **Observable Results**

- 3353 • For all pairs of all Lanes, verify that the SCC11 HS-RX Common-Mode Return Loss meets or
3354 exceeds the limits shown in Figure 3.2.2-1 above.

3355 **Possible Problems**

3356 See Possible Problems comments for Test 3.2.1. The same applies to this test.

Test 3.2.3 HS-RX Mode Conversion Limits (SDC11)**Purpose**

To verify that the Mode Conversion S-parameters of the DUT's HS receivers exceed the minimum conformance limits.

References

[1] C-PHY Specification, Section 8.7.3

Resource Requirements

See Annex A.3.

Last Technical Modification

October 27, 2014

Discussion

Section 8 of the C-PHY Specification defines the general interconnect and lane configuration requirements for C-PHY products. Section 8.7 defines the Driver and Receiver S-parameter specifications, which includes a specification for RX Mode Conversion Limits.

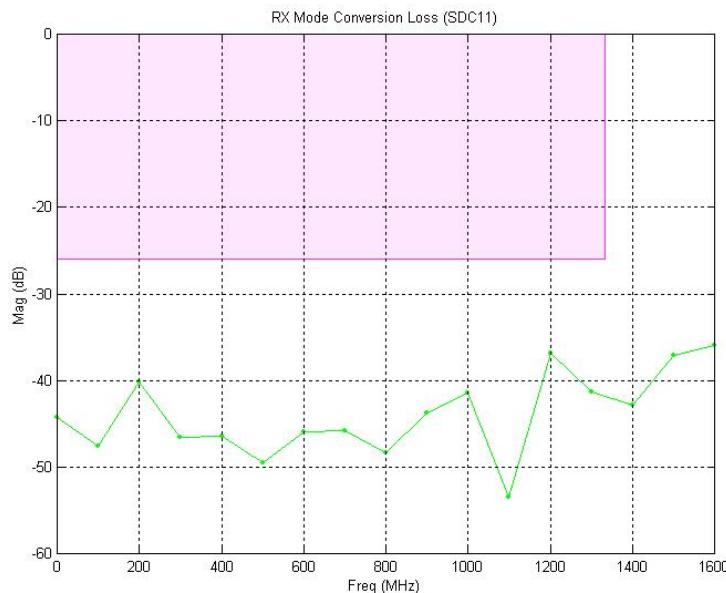
The specification states[1],

978 The differential to common-mode conversion limits of TX and RX should be -26dB up to f_{MAX} .

Figure 3.2.3-1: Mode Conversion Specification Requirement

(The general methodology for this test is otherwise identical to Test 3.2.2, except the SDC11 S-parameter is measured, and different conformance frequencies/limits are applied.)

The HS-RX Mode Conversion Loss must be greater than 26dB over the frequency range 0 to f_{MAX} in order to be considered conformant. An example measurement result showing a conformant Mode Conversion Loss response is shown in the figure below.



3377

Figure 3.2.3-2: Example Conformant HS-RX Mode Conversion Loss Result**3378 Test Setup**

3379 See Annex B.3.1.

3380 Test Procedure

- 3381 • Obtain the value of f_{MAX} for the DUT that was used in Test 3.1.1.
- 3382 • Power on and configure the DUT to force its RX into fixed state where the HS-RX termination is enabled.
- 3383 • Calibrate and configure the Test System for an SDC11 measurement over the frequency range 0 to f_{MAX} .
- 3384 • Connect the DUT's Lane 0 receiver to the Test System (A-B pair).
- 3385 • Measure the SDC11 HS-RX Mode Conversion Loss.
- 3386 • Repeat the previous two steps for the B-C and C-A pairs.
- 3387 • Repeat the previous three steps for all other Lanes.

3390 Observable Results

- 3391 • For all pairs of all Lanes, verify that the SDC11 HS-RX Mode Conversion Loss is greater than 26dB across the frequency range 0 to f_{MAX} .

3393 Possible Problems

3394 See Possible Problems comments for Test 3.2.1. The same applies to this test.

Test 3.2.4 HS-RX Differential Input Impedance (Z_{ID})

Purpose

To verify that Differential Input Impedance (Z_{ID}) of the DUT's HS-RX line termination is within the conformance limits.

References

- [1] C-PHY Specification, Section 9.2.1
- [2] Ibid, Table 26

Resource Requirements

See Annex A.3.

Last Technical Modification

October 27, 2014

Discussion

The C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for Z_{ID} , which is the Differential Input Impedance, and is the impedance of the receiver's HS-RX line termination.

The specification states[1],

- 1121 The differential input impedances Z_{ID} and the differential input impedance mismatch ΔZ_{ID} shall be compliant
 1122 with Table 26 for all six possible high-speed wire states and for all allowed loading conditions. It is

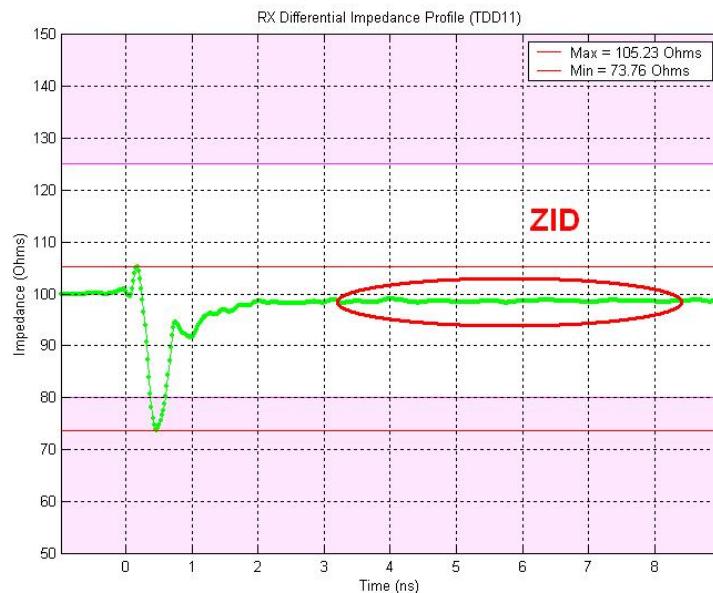
Figure 3.2.4-1: Z_{ID} Specification Definition

The specification also provides conformance limits for Z_{ID} [2],

Z_{ID_AB}	Differential input impedance	80	100	120	Ω	
Z_{ID_BC}						
Z_{ID_CA}						

Figure 3.2.4-2: Z_{ID} Conformance Requirements

In this test, the Z_{ID} value of the DUT's HS receivers will be measured. While multiple valid methods may be used to measure Z_{ID} , this test suite uses a TDR-based approach, where the HS-RX line termination value is determined from the measured TDR impedance profile. The value of Z_{ID} is measured as the final, settled value of the differential impedance profile. An example measurement is shown in the figure below.



3417

Figure 3.2.4-3: Example HS-RX Z_{ID} Measurement

3418 The setup for this test is identical to Tests 3.2.1 - 3.2.3, in that the DUT must be configured such that its
 3419 HS-RX line termination is forced on for the duration of the measurement (see Test 3.2.1 Discussion).

3420 For all pairs (A-B, B-C, and C-A) of all Lanes, the value of Z_{ID} shall be within the range of 80 to 120 Ohms
 3421 in order to be considered conformant[2].

3422 **Test Setup**

3423 See Annex B.3.1.

3424 **Test Procedure**

- 3425 • Power on and configure the DUT to force its RX into fixed state where the HS-RX termination is
 3426 enabled.
- 3427 • Calibrate and configure the Test System for a differential impedance profile measurement.
- 3428 • Connect the DUT's Lane 0 receiver to the Test System (pair A-B).
- 3429 • Measure Z_{ID} , as described above.
- 3430 • Repeat the previous two steps for the B-C and C-A pairs.
- 3431 • Repeat the previous three steps for all other Lanes.
- 3432 • Observable Results
- 3433 • For all Lanes, verify that Z_{ID} is between 80 and 120 Ohms.

3434 **Possible Problems**

3435 See Possible Problems comments for Test 3.2.1. The same applies to this test.

Test 3.2.5 HS-RX Differential Input Impedance Mismatch (ΔZ_{ID})

Purpose

To verify that the Differential Input Impedance Mismatch (ΔZ_{ID}) of the DUT's HS receiver is within the conformance limits.

References

[1] C-PHY Specification, Section 9.2.1

[2] Ibid, Table 26

Resource Requirements

None.

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for ΔZ_{ID} , which is a device's High-Speed Differential Input Impedance Mismatch. A copy of the specification text is reproduced below[1].

1116 The differential input impedances of the receiver for A-B, B-C and C-A pairs are denoted by Z_{ID_AB} , Z_{ID_BC} ,
 1117 and Z_{ID_CA} , respectively. ΔZ_{ID} is the mismatch of the differential input impedances. This mismatch is defined
 1118 as the ratio of the difference between the largest and smallest value of Z_{ID_AB} , Z_{ID_BC} and Z_{ID_CA} , and the
 1119 average of those impedances:

$$1120 \quad \Delta Z_{ID} = 3 \cdot \frac{\max(Z_{ID_AB}, Z_{ID_BC}, Z_{ID_CA}) - \min(Z_{ID_AB}, Z_{ID_BC}, Z_{ID_CA})}{Z_{ID_AB} + Z_{ID_BC} + Z_{ID_CA}}$$

1121 The differential input impedances Z_{ID} and the differential input impedance mismatch ΔZ_{ID} shall be compliant
 1122 with Table 26 for all six possible high-speed wire states and for all allowed loading conditions. It is

Figure 3.2.5-1: ΔZ_{ID} Specification

3451 The specification also provides limits for ΔZ_{ID} , shown below[2].

ΔZ_{ID}	Differential input impedance mismatch			10	%	
-----------------	---------------------------------------	--	--	----	---	--

Figure 3.2.5-2: ΔZ_{ID} Conformance Requirements

3453 The procedure for this test simply involves computing ΔZ_{ID} from the measured Z_{ID} values obtained in Test
 3454 3.2.4. The ΔZ_{ID} value will be computed for each Lane.

3455 For all Lanes, the computed ΔZ_{ID} value shall be less than 10% in order to be considered conformant[2].

Test Setup

None.

3458 **Test Procedure**

- 3459 • Obtain the Z_{ID} values for each Lane from Test 3.2.4.
3460 • For each Lane, compute ΔZ_{ID} as described above.

3461 **Observable Results**

- 3462 • For all Lanes, verify that ΔZ_{ID} is less than 10%.

3463 **Possible Problems**

3464 None.

Group 3 LP-TX/RX Impedance Requirements

3465 Overview

3466 This group of tests verifies several LP-TX and LP-RX low-frequency (DC) impedance requirements
3467 defined in Section 8 of the C-PHY Specification.

3468 Status

3469 The test names, Discussion sections, and Procedures are considered to be in release form (i.e., sufficiently
3470 documented to reflect the current state of implementation), and most tests have been successfully
3471 performed on at least one device. Additional modifications to both the test descriptions and
3472 implementations may continue if new opportunities for improvement are identified.

Test 3.3.1 LP-TX Output Impedance (Z_{OLP})

Purpose

To verify that the Low-Power Output Impedance (Z_{OLP}) of the DUT's LP transmitters are greater than the minimum allowed value.

References

- [1] C-PHY Specification, Section 9.1.2
- [2] Ibid, Table 24
- [3] Ibid, Figure 41
- [4] Ibid, Figure 42
- [5] Ibid, Figure 43

Resource Requirements

See Annex A.3

Last Technical Modification

June 25, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for Z_{OLP} , which is a device's LP Output Impedance. The specification defines the LP Output Impedance as $Z_{OLP} = |(V_{THEVENIN} - V_{PIN}) / I_{OUT}|$. It also defines the circuit below to be used for measuring Z_{OLP} , which is used to create the following I-V curves for the Logic-High and Logic-Low states, also shown below[1].

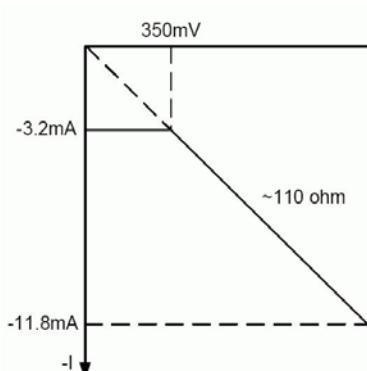


Figure 42 V-I Characteristic for LP Transmitter Driving Logic Low

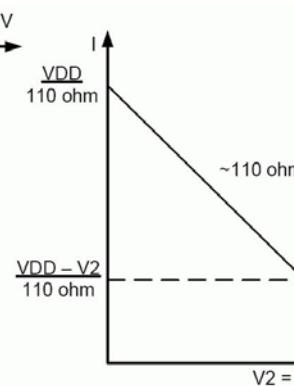


Figure 41 V-I Characteristic for LP Transmitter Driving Logic High

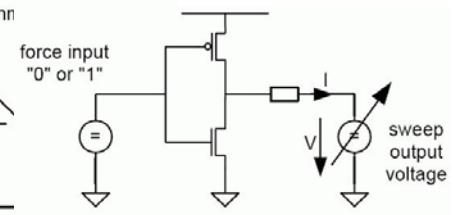


Figure 43 LP Transmitter V-I Characteristic Measurement Setup

Figure 3.3.1-1: VI Characteristic Plots, and Setup for Z_{OLP} Measurement

The specification also provides conformance requirements for Z_{OLP} [2].

Z _O LP	Output impedance of LP transmitter	110			Ω	1, 2
-------------------	------------------------------------	-----	--	--	---	------

Note:

1. See Figure 45 and Figure 46.
2. Though no maximum value for Z_OLP is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

3494

Figure 3.3.1-2: Z_OLP Conformance Requirements

In this test, the DUTs Z_OLP for the V_A, V_B and V_C LP transmitters of each Lane will be measured using a voltage source and a current meter while the DUT is driving a constant LP-000 and LP-111 state.

For the Logic-Low case, the V-I characteristic will be determined by measuring two data points, while the LP-TX is sourcing a continuous LP-000 state. These will be the measured currents I₁ and I₂, for applied voltage values 350mV and 450mV, respectively. These two voltage/current pairs will determine a line on the V-I graph (as shown above), the slope of which will be the Z_OLP Output Impedance, and will be computed as Z_OLP(0) = (450-350) / abs(I₁ - I₂). This measurement will be performed separately for the V_A, V_B and V_C LP transmitters.

For the Logic-High case, a similar procedure will be applied, where the currents I₁ and I₂ for applied voltage levels of 850mV and 550mV will be measured, and used to plot/compute the Z_OLP value for the LP-111 case, where Z_OLP(1) = (850-550) / abs(I₁ - I₂).

For all Lanes, the values of Z_OLP(0) and Z_OLP(1) for V_A, V_B and V_C must be greater than 110 Ohms in order to be considered conformant[2].

Test Setup

See Annex B.3.2

Test Procedure

- Power on the DUT and connect the DUT's Lane 0 to the Test Setup.
- Create a condition that causes the DUT to source a continuous LP-000 state.
- Measure the V-I Characteristic, and compute Z_OLP(0) for the V_A LP-0 state, as described above.
- Measure the V-I Characteristic, and compute Z_OLP(0) for the V_B LP-0 state, as described above.
- Measure the V-I Characteristic, and compute Z_OLP(0) for the V_C LP-0 state, as described above.
- Create a condition that causes the DUT to source a continuous LP-111 state.
- Measure the V-I Characteristic, and compute Z_OLP(1) for the V_A LP-1 state, as described above.
- Measure the V-I Characteristic, and compute Z_OLP(1) for the V_B LP-1 state, as described above.
- Measure the V-I Characteristic, and compute Z_OLP(1) for the V_C LP-1 state, as described above.
- Repeat all of the above steps for all other Lanes.

Observable Results

For all Clock and Data Lanes:

- Verify that Z_OLP(0) for V_A is greater than 110 Ohms.
- Verify that Z_OLP(0) for V_B is greater than 110 Ohms.
- Verify that Z_OLP(0) for V_C is greater than 110 Ohms.
- Verify that Z_OLP(1) for V_A is greater than 110 Ohms.
- Verify that Z_OLP(1) for V_B is greater than 110 Ohms.
- Verify that Z_OLP(1) for V_C is greater than 110 Ohms.

3529

Possible Problems

3530

Note that this test is typically performed on CSI-2 and DSI Master devices only (e.g., camera sensors in the CSI-2 case, and host processors in the DSI case.) It can also be performed on ‘bare-phy’ DUT types. However it is not typically possible to perform this test on Slave devices (e.g., DSI displays), as the Slave’s LP-TX is only active during a Bus Turnaround event, which is not sufficient for test purposes. The measurement could be performed in these cases if a vendor-specific means exists to force a Slave device’s LP-TX into the fixed LP-111 and LP-000 states required for this test.

3531

3532

3533

3534

3535

Test 3.3.2 LP-RX Input Leakage Current (I_{LEAK})

Purpose

To verify that the leakage current of the DUT's LP receiver is within the conformance limits.

References

[1] C-PHY Specification, Section 9.4

[2] Ibid, Figure 53

[3] Ibid, Table 31

Resource Requirements

See Annex A.3

Last Technical Modification

October 27, 2014

Discussion

Section 9 of the C-PHY Specification defines the Electrical Characteristic requirements for C-PHY products. Included in these requirements is a specification for I_{LEAK} , which is a device's LP-RX leakage current.

The specification states[1],

- 1171 than $T_{VPIN(\text{absmax})}$. When the PHY is in the low-power receive mode the pad pin leakage current shall be I_{LEAK}
- 1172 when the pad signal voltage is within the signal voltage range of V_{PIN} . The specification of I_{LEAK} assures

Figure 3.3.2-1: I_{LEAK} Specification Definition

A copy of the specification figure is provided below[2].

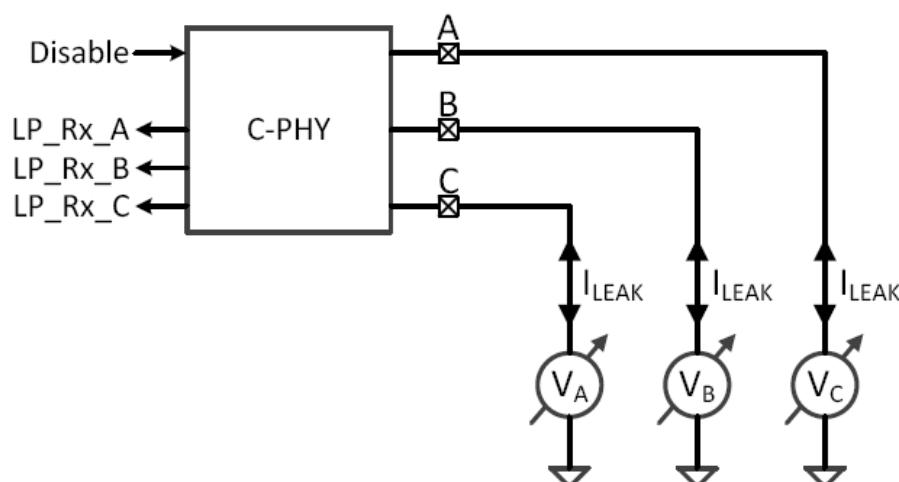


Figure 53 Pin Leakage Measurement Example Circuit

Figure 3.3.2-2: Example I_{LEAK} Measurement Diagram

3554 The specification also states the relevant conformance ranges, and the conditions under which the leakage
 3555 requirements are to be met[3],

Table 31 Pin Characteristic Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{PIN}	Pin signal voltage range	-50		1350	mV	
I_{LEAK}	Pin leakage current	-10		10	μA	1
V_{GNDH}	Ground shift	-50		50	mV	
$V_{PIN}(absmax)$	Transient pin voltage level	-0.15		1.45	V	3
$t_{VPIN(absmax)}$	Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$			20	ns	2

Note:

- 3556 1. When the pad voltage is in the signal voltage range from $V_{GNDH,min}$ to $V_{OH} + V_{GNDH,max}$ and the
 lane module is in LP receive mode.

Figure 3.3.2-3: V_{PIN} , I_{LEAK} Conformance Requirements

3557 Note that Note 1 above corresponds to a range of -50mV to 1350mV.

3558 In this test, the leakage current of the DUT's LP-RX Lanes will be measured using an ammeter with
 3559 picoamp resolution (or smaller), while a voltage is applied at the RX, and varied across the range of -50mV
 3560 to 1350mV.

3561 For all Lanes, the leakage current, I_{LEAK} , should be between -10uA and +10uA for all applied voltage values
 3562 between -50mV and 1350mV (inclusive)[3].

Test Setup

3564 See Annex B.3.3

Test Procedure

- 3566 • Power on the DUT and connect DUT Lane 0 V_A line to the Test Setup.
- 3567 • Set the applied voltage to -50mV.
- 3568 • Observe the leakage current I_{LEAK} .
- 3569 • Slowly increase the applied voltage, in increments no greater than 50mV.
- 3570 • For each incremental applied voltage level, observe the leakage current I_{LEAK} .
- 3571 • Repeat the previous two steps for all applied voltage levels up to and including 1350mV.
- 3572 • Report the maximum observed current (positive or negative), and respective applied voltage level,
 3573 as the final I_{LEAK} result for the given Lane.
- 3574 • Repeat the previous seven steps for the V_B and V_C lines.
- 3575 • Repeat the previous eight steps for all other Lanes.

Observable Results

- 3577 • For all lines of all Lanes, verify that I_{LEAK} is between -10 and +10uA.

Possible Problems

3579 Note that this test is typically performed on CSI-2 and DSI Slave devices only (e.g., host processors in the
 3580 CSI-2 case, and display panels in the DSI case). It can also be performed on 'bare-phy' DUT types.
 3581 However it is not typically possible to perform this test on Master devices (e.g., DSI host processors), as
 3582 the Master's LP-RX is only active during a Bus Turnaround event, which is not sufficient for test purposes.
 3583 The measurement could be performed in these cases if a vendor-specific means exists to force a Master
 3584 DUT's LP-RX into the state required for this test.

Annexes

3585 Overview

3586 A test suite annex is intended to provide additional low-level technical detail pertinent to specific tests
3587 contained in this test suite. An annex often covers topics that are outside of the scope of the Specification
3588 and are specific to the methods used for performing the measurements in this test suite. Annex topics might
3589 also include discussion regarding a specific interpretation of the Specification (for the purposes of this test
3590 suite) for cases where a particular requirement might appear unclear or otherwise open to multiple
3591 interpretations.

3592 Scope of Tests

3593 A test suite annex is considered an informative supplement, and it pertains solely to the test definitions and
3594 procedures contained in this test suite.

This page intentionally left blank.

Annex A Resource Requirements (DUTs and Test Equipment)

3595 **Purpose**

3596 To define the test equipment and DUT requirements necessary for performing the tests in this test suite.

3597 **References**

3598 None.

3599 **Last Technical Modification**

3600 15-Sep-2014

3601 **Discussion**

3602 (Begins on following page)

A.1 LP/HS Transmitter Tests

The LP and HS Transmitter tests of Section 1 are designed and organized to be performed in groups, using several test setups. Currently, different setups are used for the HS versus LP measurements, as more accurate results can be obtained using configurations that are optimized for each case, rather than trying to perform all tests using a single setup. The reasons for this pertain to, 1) the difference in termination requirements for the LP vs. HS signaling cases, and 2) the difference in signal amplitude levels between the LP and HS signals. (More information on this topic appears below.)

Equipment Requirements

In order to perform the LP and HS Clock and Data Lane transmitter tests of Section 1, the following resources are required:

- 1 x DUT, properly mounted on an SMA-based evaluation PCB that meets the Test Vehicle Board (TVB) guidelines. (See *DUT Requirements* section below.)
- 1 x Four-Channel Real-Time Digital Storage Oscilloscope (DSO), Bandwidth should be 5th harmonic or greater for the given C-PHY symbol rate (e.g., 2.5GHz minimum for 1Gsp, 6.0GHz minimum for 2.5Gsp)
- 3 x High-Impedance, Low Capacitive Load Differential Probes (same bandwidth as DSO above)
- 3 x SMA Test Cables
- 1 x MIPI C-PHY Reference Termination Board (RTB) (*See Figure A.1-1 below*)
- 1 x MIPI C-PHY LP Capacitive Load (CLOAD) Fixture
- Post-processing software (DSO-specific).

These components will be used in the various test setup diagrams shown in Annex B of this document.

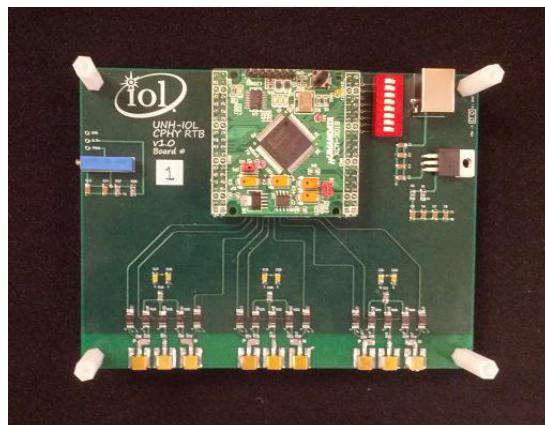


Figure A.1-1: MIPI C-PHY Reference Termination Board (RTB)

DUT Requirements

In addition to test equipment requirements, it is also necessary to specify requirements for the Device Under Test (DUT). These requirements are necessary to ensure accurate and consistent measurements in a proper test environment, and to provide configuration support for all required operating modes needed for performing the various tests.

Test PCB Requirements: In order to measure the DUT characteristics under proper test conditions, and also to interface the DUT to the measurement equipment, there are several requirements for how the DUT is mounted.

The DUT should be mounted on a signal-integrity-grade evaluation board, with all C-PHY signals brought out to individual SMA or SMP connectors. The individual single-ended signals for each Lane should be decoupled and routed to 50-ohm single-ended PCB traces as near to the DUT IC as possible. All high-speed C-PHY signal trace lengths must be matched. Measurement-grade, controlled-impedance connectors should be used.

The UNH IOL has created a freely available PCB design template for MIPI test purposes, known as the Test Vehicle Board, which includes the necessary high-speed SMA and probing point requirements, and may be freely modified by vendors to suit their individual C-PHY-based devices. (Note this is only a generic design template, which vendors must customize and fabricate themselves, prior to submitting products for testing.) The Gerber files for the TVB (along with schematics, design guidelines, and other information) are available on the [MIPI Alliance website](#).

Note that the recommended approach of using a high-quality evaluation PCB which is optimized for signal integrity is intended as a practical and reasonably cost-effective method for performing reasonable conformance measurements across a variety of DUT types. The methods described in this test suite are geared toward demonstrating conformance of CSI-2 and DSI products, and are by no means optimal, but rather seek a balance between measurement accuracy and cost/complexity. It is possible to obtain higher-accuracy results (e.g., for characterization purposes) for many tests through the use of more sophisticated PCB/fixtures designs, termination methods, and probing techniques. Also, de-embedding of test fixturing can also improve measurement accuracy. Use of these techniques is not discouraged if such resources are available.

HS Burst Mode Configurability: Devices desiring HS-TX testing must be capable of being configured to transmit arbitrary CSI or DSI traffic via HS bursts. While there is currently no specific test pattern or test mode defined for TX testing, devices must be able to source a repeated HS burst sequence of approximately 20K-50K HS bits in length, containing a high-transition-density data pattern (i.e., a burst containing many edges, and with a wide distribution of run-lengths). Pseudo-random pixel data is ideal. For best results, frames should not have ‘long’ sequences of all-zero or all-one data, whereby the maximum run length during the packet data should be less than the $T_{HS\text{-}ZERO}$ or $T_{HS\text{-}TRAIL}$ periods for a given DUT. Longer HS bursts are preferable to shorter ones, however the HS-TX must return to the LP-11 Stop state between HS bursts, and the HS bursts should be transmitted as frequently as possible.

LP Escape Mode Configurability: Devices desiring LP-TX testing must be capable of being configured to transmit Escape Mode entry codes for all supported commands (DSI devices). CSI-2 devices must be able to transmit a ULPS Escape Mode sequence on all Data Lanes, as well as the Clock Lane ULPS entry sequence on the Clock Lane, in order for LP-TX measurements to be performed.

A.2 Receiver Tests

Equipment Requirements

In order to perform the HS-RX and LP-RX tests of Section 2, the following resources are required:

- A multichannel, programmable lab-grade signal source, capable of generating appropriate HS and LP signaling. (Note that the HS and LP signaling components can be generated by separate sources, and combined externally using resistive splitters/combiners.)

Also, a receiver test setup additionally requires all of the resources necessary for performing TX measurements (see Annex A.1), which are necessary for measuring and calibrating the output of the signal source used to generate the RX test signals.

DUT Requirements

Furthermore, for receiver testing, DUTs must provide a suitable observation mechanism that allows for verification of the received data that is transmitted to the DUT during a receiver test. Note that the exact observation mechanism will depend on the type of DUT, and may require additional supporting hardware,

3677 depending on the DUT type. A detailed description of RX observation mechanisms for several different
3678 DUT types is presented in Annex F of this document.

A.3 S-Parameter and Impedance Tests

Equipment Requirements

In order to perform the HS and LP TX/RX impedance tests of Section 3, the following resources are required:

- A Time-Domain Reflectometer (TDR) with S-parameter capability.
- A lab-grade variable voltage source
- An ammeter with milliamp resolution
- An ammeter with picoamp resolution

DUT Requirements

The HS S-parameter/return loss tests require measurement of the DUT's HS termination, which is typically only enabled during an HS burst. As this time is not long enough to perform an S-parameter measurement, DUTs must support a vendor-specific mechanism for manually enabling and disabling the HS-RX termination. Also, to measure S-parameters for HS transmitters, the DUT must be placed into a state where it can transmit a continuous HS data pattern. The ideal pattern for this purpose depends on the instrument being used to perform the S-parameter measurements. If a VNA is used, a long, pseudo-random pattern is preferred in order to minimize error in the measurement. If a TDR/TDNA is used, a 'clock pattern' (e.g., repeating 1010 or 1100) will yield the best results. (Also, 'static' test modes that transmit a continuous HS-1 and HS-0 can be used with either a VNA or TDR to isolate the static impedance of the HS-TX, however the recommended methodology for performing S-parameter measurements is to test the interface while in a dynamic transmitting state.)

Also, for the low-frequency LP-TX impedance tests (Z_{OLP}), it must be possible to configure the LP-TX to fixed LP-111 and LP-000 states for the measurements. While this may be done using vendor-specific methods, the LP-111 state can typically be measured during the Stop state during normal operation (if the DUT can be configured to not transmit any other data, i.e., disabling HS burst transmission). Also, the LP-000 state can be measured during the LP-000 Space state following a ULPS entry sequence. (Note that DUTs are required to support the ULPS entry command on all Lanes in order to perform the LP-TX signaling measurements anyway, so this should not be a problem.)

Annex B Test Setups

3705 **Purpose**

3706 To define the basic test setups used for performing the tests in this test suite.

3707 **References**

3708 None.

3709 **Last Modification**

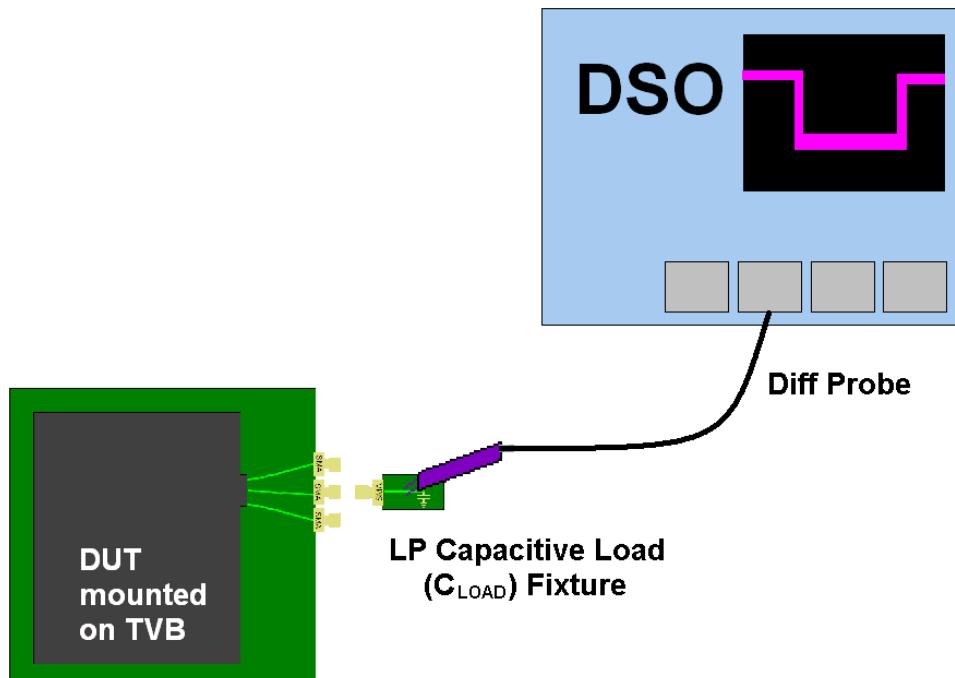
3710 14-Apr-2015

3711 **Discussion**

3712 (Begins on following page)

B.1 Transmitter Tests

B.1.1 LP Transmitter Tests



3713

Figure B-1-1: LP Transmitter Test Setup

3714 Notes on the above setup:

- 3715 • The DUT is connected to the DSO using one high-bandwidth differential probe.
3716 • Differential probe is connected to the test points on the C_{LOAD} Test Fixture, and differential probe
3717 measures the single-ended V_A, V_B, or V_C signal with respect to PCB ground.
3718 • The DUT should be configured to transmit a ULPS entry sequence on all Lanes.
3719 • The DSO vertical gain should be optimized so that the LP signaling spans as much of the vertical
3720 height of the DSO screen as possible.

B.1.2 HS Transmitter Tests

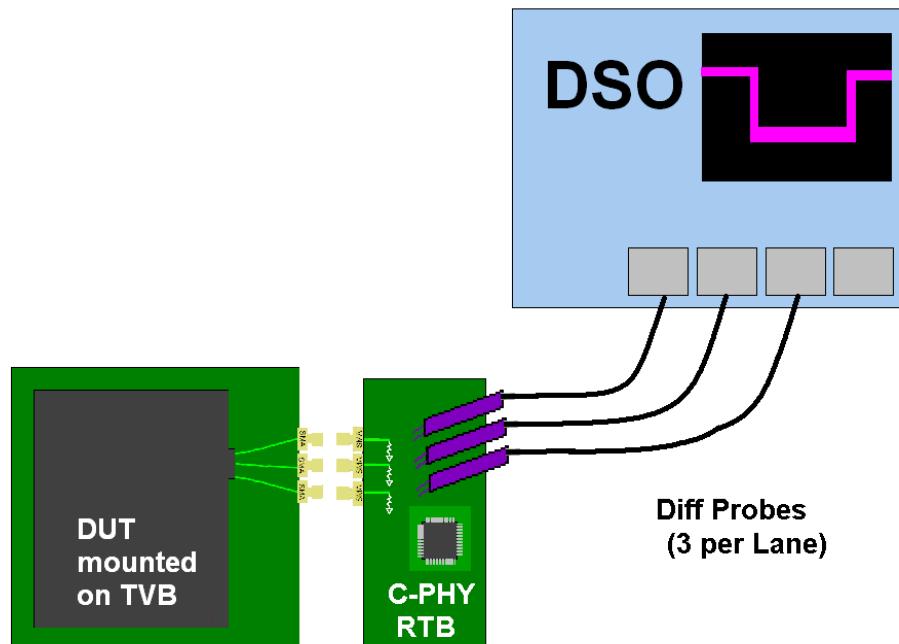
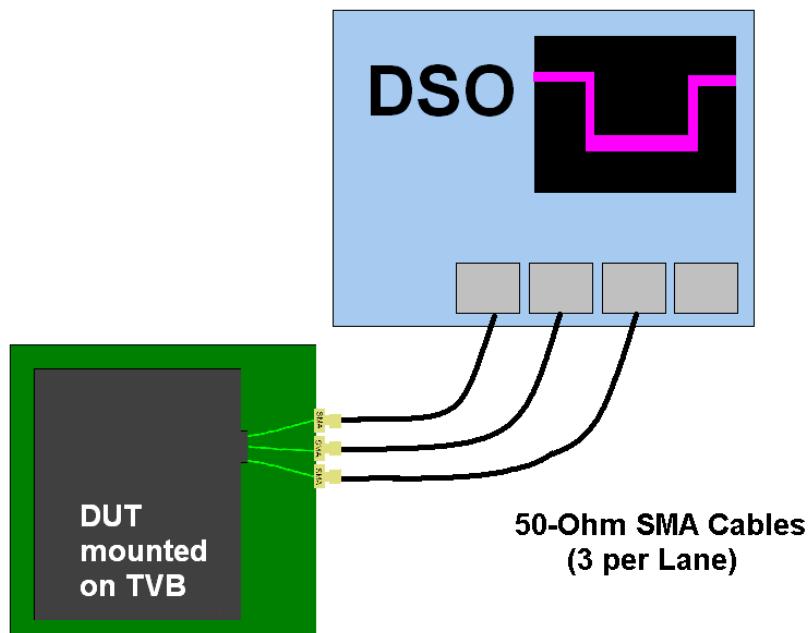


Figure B-1-2a: HS Transmitter Test Setup (Differential Probes, with RTB)

Notes on the above setup:

- The DUT is connected to the DSO using three high-bandwidth, low capacitance differential probes.
- Differential probes are connected to the test points on the Reference Termination Board (RTB), and each differential probe measures the single-ended V_A, V_B, or V_C signal with respect to PCB ground.
- The Reference Termination Board (RTB) provides a reference termination environment, and actively switches in/out a precision HS resistive termination (Z_{ID}), simulating an ‘ideal’ C-PHY receiver.
- The RTB is designed to have a resistive termination (Z_{ID}) value of 50 ohms per line, for all lines.
- The DUT should be configured to transmit a continuous stream of HS bursts.
- The DSO vertical gain should be optimized so that the DUT signaling spans as much of the vertical height of the screen as possible.



3735

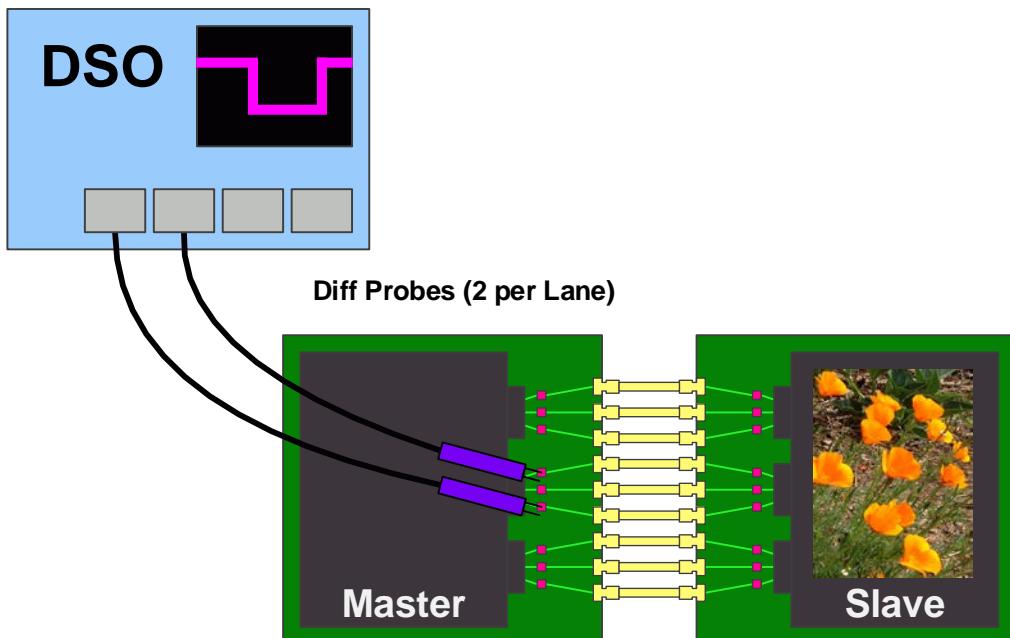
Figure B-1-2b: HS Transmitter Test Setup

(Direct DSO Connection, for HS Rise/Fall Time Tests Only)

3736 Notes on the above setup:

- 3737 • The DUT is connected to the DSO using three high-bandwidth, low loss 50-ohm coaxial cables.
3738 • Each cable measures the single-ended V_A , V_B , or V_C signal with respect to PCB ground.
3739 • The DSO serves as the termination, and is designed to have a resistive termination (Z_{ID}) value of
3740 50 ohms per line, for all lines.
3741 • The DUT should be configured to transmit a continuous stream of HS bursts.
3742 • The DSO vertical gain should be optimized so that the DUT signaling spans as much of the
3743 vertical height of the screen as possible.

B.1.3 Bus Turnaround Tests



3744

Figure B-1-3: Bus Turnaround Test Setup

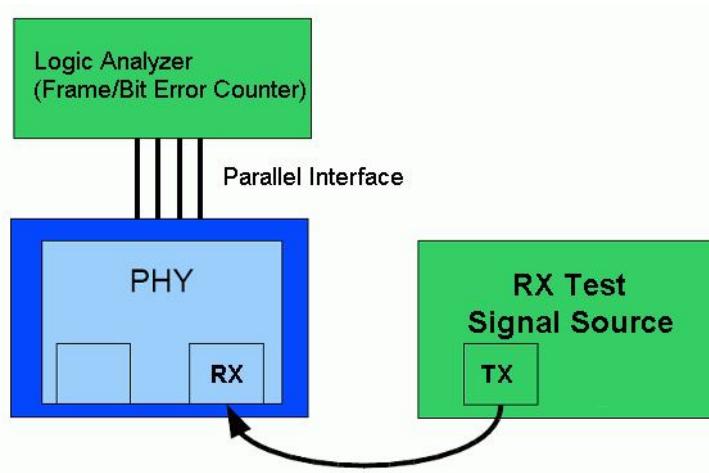
Notes on the above setup:

- Note the figure above is only for reference (see further below).
- The general purpose of this setup is to probe the link between a Master and Slave device in order to observe a Bus Turnaround event. For the BTA tests, it is possible for the DUT be either the Master or the Slave in the above diagram, depending on the DUT type (see further below).
- If the DUT is a MASTER device, the tests are performed using either of the following as the Slave device:
 - 1) An actual Slave device that supports Bus Turnaround, or
 - 2) A piece of test equipment (e.g., signal source, protocol generator) that can implement a Bus Turnaround.
- If the DUT is a SLAVE device, the tests can be performed using either of the following as the Master:
 - 1) An actual Master device that supports Bus Turnaround, or
 - 2) A piece of test equipment (e.g., signal source, protocol generator) that can implement a Bus Turnaround.
- The Data Lane 0 link between Master and Slave is probed using two high-bandwidth, low capacitance differential probes.
- Differential probes may be connected at any point between the Master and Slave, and each differential probe measures the single-ended + or - signal with respect to PCB ground.
- In order to best observe the drive overlap period during the turnaround event, it is recommended that the Master and Slave be configured to use different (but still valid) V_{OL} (LP-0) levels, if possible.

B.2 Receiver Tests

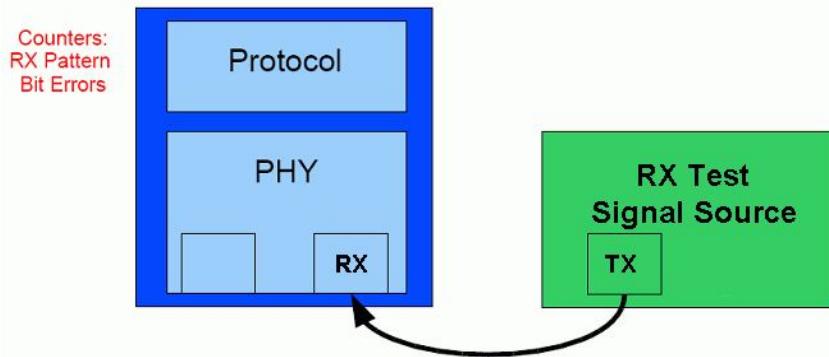
3767
3768

(Note: In addition to the diagrams below, also see Annex F for a more complete discussion regarding the different options for RX test observables for various DUT types.)



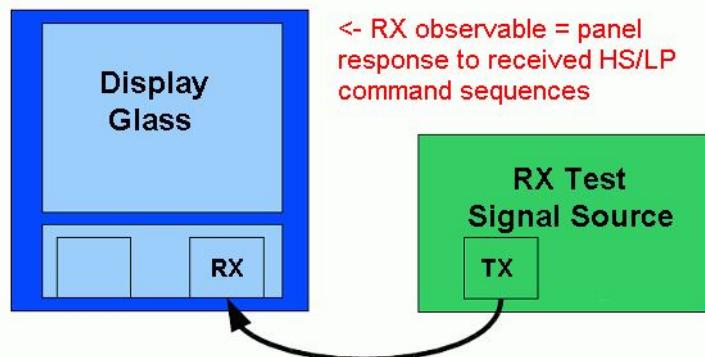
3769

Figure B-2a: LP/HS-RX Test Setup (Bare Phy)



3770

Figure B-2b: LP/HS-RX Test Setup (Combined IC with Phy + Protocol Layers)



3771

Figure B-2c: LP/HS-RX Test Setup (Complete Display Device)

B.3 Other Tests

B.3.1 Impedance and S-Parameter Tests

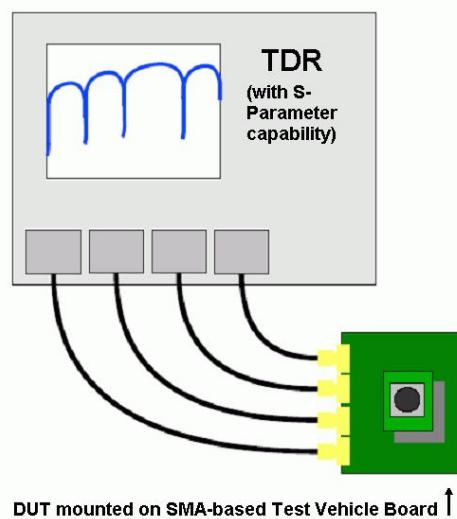


Figure B-3-1: S-Parameter/Return Loss Test Setup

B.3.2 LP-TX Output Impedance

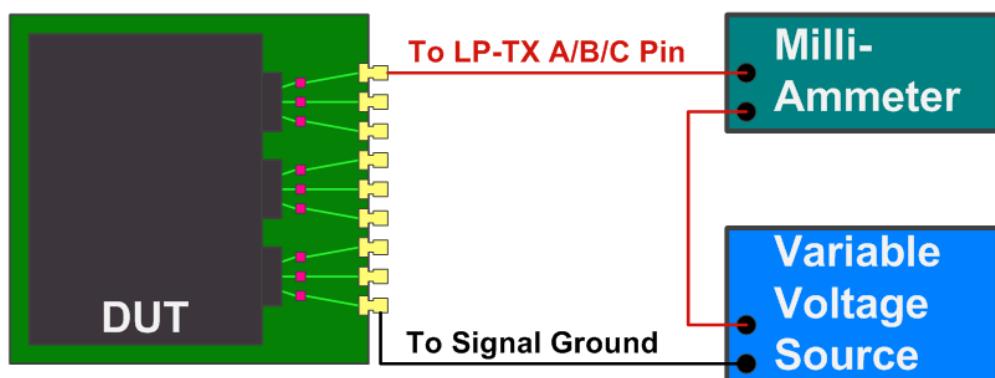
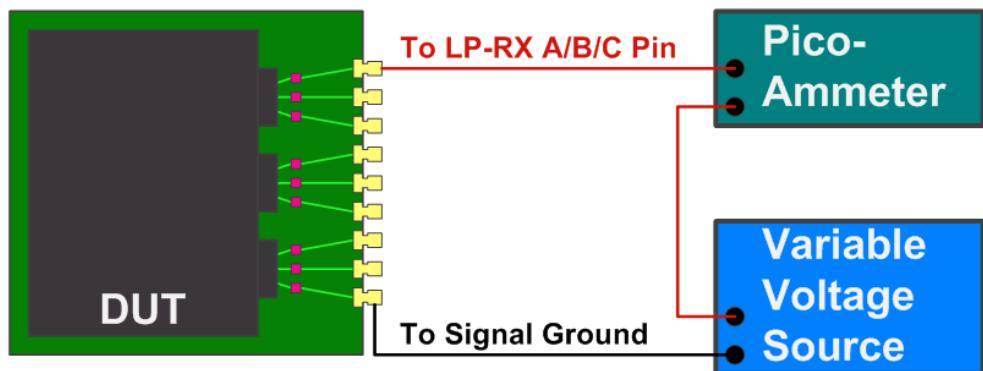


Figure B-3-2: LP-TX Output Impedance (Z_{OLP}) Test Setup

B.3.3 LP-RX Input Leakage Current

3774

Figure B-3-3: LP-RX Input Leakage Current (I_{LEAK}) Test Setup

Annex C Statistical Methodology for Bit Error Rate (BER) Verification

3775 **Purpose**

3776 To develop a procedure for Bit Error Rate (BER) measurement through the application of statistical
3777 methods.

3778 **References**

3779 [1] Miller, Irwin and John E. Freund, Probability and Statistics for Engineers (Second Edition), Prentice-
3780 Hall, 1977, pp. 194-210, 240-245.

3781 **Last Technical Modification**

3782 17-Oct-2008

3783 **Discussion**

3784 (Begins on following page)

C.1 Introduction

One key performance parameters for all digital communication systems is the bit error rate (BER). The bit error rate is the probability that a given bit will be received in error. The BER may also be interpreted as the average number of errors that would occur in a sequence of n bits.

While the bit error rate concept is quite simple, the measurement of this parameter poses some significant challenges. The first challenge is deciding the number of bits, n, that must be sent in order to make a reliable measurement. For example, if 10 bits were sent and no errors were observed, it would be foolish to conclude that the bit error rate is zero. However, common sense tells us that the more bits that are sent without error, the more reasonable this conclusion becomes. In the interest of keeping the test duration as short as possible, we want to send the smallest number of bits that provides us with an acceptable margin of error.

This brings us to the second challenge of BER measurement. Given that we send n bits, what reasonable statements can be made about the bit error rate based on the number of errors observed? Returning to the previous example, if 10 bits are sent and no errors are observed, it is unreasonable to say that the BER is zero. However, it may be more reasonable to say that the BER is 10^{-1} or better. Furthermore, you are absolutely certain that the bit error rate is not 1.

In this Annex, two statistical methods, hypothesis testing and confidence intervals, are applied to help us answer the questions of how many bits we should be sent and what conclusions can be made from the test results.

C.2 Statistical Model

A statistical model for the number of errors that will be observed in a sequence of n bits must be developed before we apply the aforementioned statistical methods. For this model, we will assume that every bit received is an independent Bernoulli trial. A Bernoulli trial is a test for which there are only two possible outcomes (i.e. a coin toss). Let us say that p is the probability that a bit error will occur. This implies that the probability that a bit error will not occur is (1-p).

The property of independence implies that the outcome of one Bernoulli trial has no effect on the outcomes of the other Bernoulli trials. While this assumption is not necessarily true for all digital communications systems, it is still used to simplify the analysis.

The number of successful outcomes, k, in n independent Bernoulli trials is taken from a binomial distribution. The binomial distribution is defined in equation C-1.

$$b(k; n, p) = C_{n,k} p^k (1 - p)^{n-k} \quad (\text{Equation C-1})$$

Note that in this case, a successful outcome is a bit error. The coefficient $C_{n,x}$ is referred to as the binomial coefficient or “n-choose-k”. It is the number of combinations of k successes in n trials. Returning to coin toss analogy, there are 3 ways to get 2 heads from 3 coin tosses: (tails, heads, heads), (heads, tails, heads), and (heads, heads, tails). Therefore, $C_{3,2}$ would be 3. A more precise mathematical definition is given in equation C-2.

$$C_{n,k} = \frac{n!}{k!(n-k)!} \quad (\text{Equation C-2})$$

3818 This model reflects the fact that for a given probability, p, a test in which n bits are sent could yield many
 3819 possible outcomes. However, some outcomes are more likely than others and this likelihood principle
 3820 allows us to make conclusions about the BER for a given test result.

C.3 Hypothesis Test

3821 The statistical method of hypothesis testing will allow us to establish a value of n, the number of bits to be
 3822 sent, for the BER measurement. Naturally, the test begins with a hypothesis. In this case, we will
 3823 hypothesize that the probability of a bit error, p, for the system is less than some target BER, P_0 . This
 3824 hypothesis is stated formally in equation C-3.

$$H_0 : p \leq P_0$$

(Equation C-3)

3825 We now construct a test for this hypothesis. In this case, we will take the obvious approach of sending n
 3826 bits and counting the number errors, k. We will interpret the test results as shown in table C-1.

Table C-1 Acceptance and Rejections Regions for H_0

Test Result	Conclusion
$k = 0$	H_0 is true
$k > 0$	H_0 is false

3827 We now acknowledge the possibility that our conclusion is in error. Statisticians define two different
 3828 categories of error. A type I error is made when the hypothesis is rejected even though it is true. A type II
 3829 error is made when the hypothesis is accepted even though it is false. The probability of a type I and a type
 3830 II error are denoted as α and β respectively. Table C-2 defines type I and type II errors in the context of this
 3831 test.

Table C-2 Definitions of Type I and Type II Errors

Type I Error	$k > 0$ even though $p \leq \text{BER}$
Type II Error	$k = 0$ even though $p > \text{BER}$

3832 A type II error is arguably more serious and we will define n so that the probability of a type II error, β , is
 3833 acceptable. The probability of a type II error is given in equation C-4.

$$\beta = (1 - p)^n < (1 - P_0)^n$$

(Equation C-4)

3834 Equation C-4 illustrates that the upper bound on the probability of a type II error is a function of the target
 3835 bit error rate and n. By solving this equation for n, we can determine the minimum number of bits that need
 3836 to be sent in order to verify that p is less than a given P_0 for a given probability of type II error.

$$n > \frac{\ln(\beta)}{\ln(1 - P_0)}$$

(Equation C-5)

3837 Let us now examine the probability of a type I error. The definition of α is given in equation C-6.

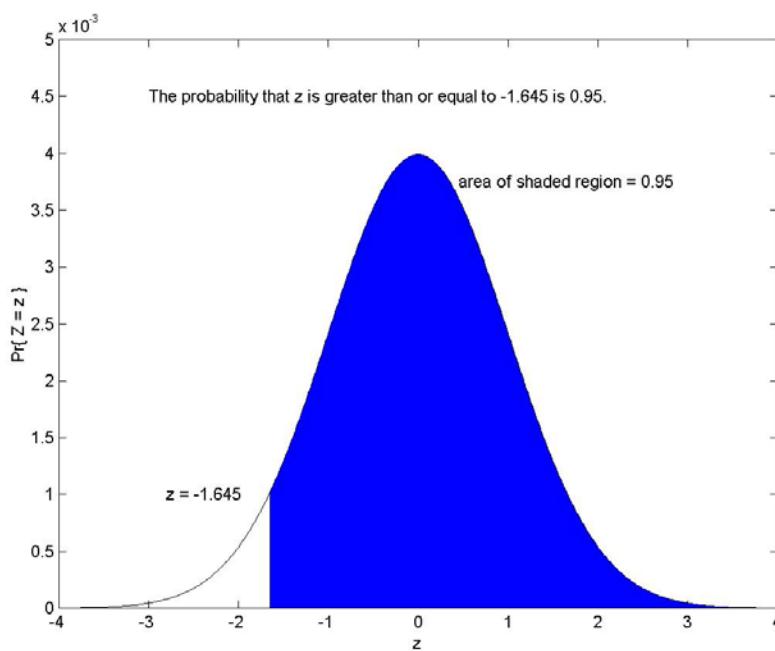
$$\alpha = 1 - (1 - p)^n \leq 1 - (1 - P_0)^n \quad (\text{Equation C-6})$$

3838 Equation C-6 shows that while we increase n to make β small, we simultaneously raise the upper bound on
 3839 α . This makes sense since the likelihood of observing a bit error increases with the number of bits that you
 3840 send, no matter how small bit error rate is. Therefore, while the hypothesis test is very useful in
 3841 determining a reasonable value for n , we must be very careful in interpreting the results. Specifically, if we
 3842 send n bits and observe no errors, we are confident that p is less than our target bit error rate (our level of
 3843 confidence depends on how small we made β). However, if we do observe bit errors, we cannot be quick to
 3844 assume that the system did not meet the BER target since the probability of a type I error is so large. In the
 3845 case of $k > 0$, a confidence interval can be used to help us interpret k.

C.4 Confidence Interval

3846 The statistical method of confidence intervals will be used to establish a lower bound on the bit error rate
 3847 given that $k > 0$. A confidence interval is a range of values that is likely to contain the actual value of some
 3848 parameter of interest. The interval is derived from the measured value of the parameter, referred to as the
 3849 point estimate, and the confidence level, $(1-\alpha)$, the probability that the parameter's actual value lies within
 3850 the interval.

3851 A confidence interval requires a statistical model of the parameter to be bounded. In this case, we use the
 3852 statistical model for k given in equation C-1. If we were to compute the area under the binomial curve for
 3853 some interval, we would be computing the probability that k lies within that interval. This concept is shown
 3854 in figure C-1.



3855

Figure C-1: Computing the Probability that $z \geq -1.645$ (Standard Normal Distribution).

3856 To compute the area under the binomial curve, we need a value for the parameter p . To compute a
 3857 confidence interval for k , you assume that k/n , the point estimate for p , is the actual value of p .

3858 Note that figure C-1 illustrates the computation of the lower tolerance bound for k_l , a special case where the
 3859 confidence interval is $[k_l, +\infty]$. A lower tolerance bound implies that in a percentage of future tests, the
 3860 value of k will be greater than k_l . In other words, actual value of k is greater than k_l with probability equal
 3861 to the confidence level. Therefore, if k_l/n is greater than P_0 , we can say that the system does not meet the
 3862 target bit error rate with probability $(1-\alpha)$. By reducing α , we reduce the probability of making a type I
 3863 error.

3864 To determine the value of k_l , it is useful to assume that the binomial distribution can be approximated by a
 3865 normal (Gaussian) distribution when n is large. The mean and variance of this equivalent distribution are
 3866 the mean and variance of the corresponding binomial distribution (given in equations C-7 and C-8).

$$\mu_K = np$$

(Equation C-7)

$$\sigma_K^2 = np(1-p)$$

(Equation C-8)

3867 Now, let α be the probability that $Z \leq z_\alpha$ where Z is a standard normal random variable. A standard random
 3868 variable is one whose mean is zero and whose variance is one. The random variable K can be standardized
 3869 as shown in equation C-9.

$$Z = \frac{K - \mu_K}{\sigma_K}$$

(Equation C-9)

3870 Note that Z is greater than z_α with probability $(1-\alpha)$, the confidence level. We apply this inequality to
 3871 equation C-9 and solve for K to get equation C-10.

$$\begin{aligned} K &> \mu_K + z_\alpha \sigma_K \\ K &> np + z_\alpha \sqrt{np(1-p)} \end{aligned}$$

(Equation C-10)

3872 As mentioned before, we assume that p is k/n . We can now generate an expression for k_l , the value that K
 3873 will exceed with probability $(1-\alpha)$. This expression is given in equation C-11.

$$k_l = k + z_\alpha n \sqrt{\frac{(k/n)(1-k/n)}{n}}$$

(Equation C-11)

3874 Finally, we argue that if K exceeds k_l , then the actual value of p must exceed k_l/n . Therefore, we can
 3875 generate an expression for p_l , the value that p will exceed with probability $(1-\alpha)$, and compare it to the
 3876 target bit error rate. By applying this comparison (given in equation F-12) the probability of a type I error
 3877 can be greatly reduced. For example, by setting z_α to -1.645 , the probability of a type I error is reduced to
 3878 5%.

$$P_0 \geq p_l = \frac{k_l}{n} = \frac{k}{n} + z_\alpha \sqrt{\frac{(k/n)(1-k/n)}{n}}$$
(Equation C-12)

C.5 Sample Test Construction

We now compress the theory presented in sections C-2 through C-4 into two inequalities that may be used to construct a bit error rate test. First, we take equation F-5 and assume that $\ln(1-P_0)$ is $-P_0$ (valid for P_0 much less than one). The results is equation C-13.

$$n > \frac{-\ln(\beta)}{P_0}$$
(Equation C-13)

Second, we examine equation C-12. Assuming that $(1-k/n)$ is very close to 1 and substituting $-\ln(\beta)/P_0$ for n , we get equation C-14.

$$-\ln(\beta) \geq k + z_\alpha \sqrt{k}$$
(Equation C-14)

The largest value of k that satisfies equation C-14 is k_l . The benefit of these two equations is that a bit error rate test is uniquely defined by β and α and that the test scales with P_0 . Table C-3 defines n and k_l in terms of β and α .

Table C-3 n and k_l as a Function of β and α .

β	$-\ln(\beta)$	n	α	z_α	k_l
0.10	2.30	$2.30/P_0$	0.10	-1.29	5
0.10	2.30	$2.30/P_0$	0.05	-1.65	6
0.05	3.00	$3.00/P_0$	0.05	-1.65	7
0.05	3.00	$3.00/P_0$	0.01	-2.33	10
0.01	4.60	$4.60/P_0$	0.05	-1.65	9
0.01	4.60	$4.60/P_0$	0.01	-2.33	13

As an example, let us construct a test to determine if a given system is operating at a bit error rate of 10^{-12} or better. Given that a 5% chance of a type I error is acceptable, the test would take the form of sending 3×10^{12} bits and counting the number of errors. If no errors are counted, we are confident that the BER was 10^{-12} or better.

Given that a 5% chance of a type II error is acceptable, we find that k_l is 7. If more than 7 errors are counted, we are confident that the bit error rate is greater than 10^{-12} . However, what if between 1 and 7 errors are counted? These cases may be handled several different ways. One option is to make a statement about the bit error rate (whether it is less than or greater than 10^{-12}) at a lower level of confidence. Another option would be to state that the test result is success since we cannot establish with an acceptable probability of error that the BER is greater than 10^{-12} . Such a statement implies that we failed to meet the burden of proof for the conjecture that the BER exceed 10^{-12} . Of course, the burden of proof could be shifted to the device under test which would imply that any outcome other than $k = 0$ would correspond to failure (the device under test failed to prove to us that the BER no more than 10^{-12}). If neither of these

3900 solutions is acceptable, it is always an option to perform a more vigorous bit error rate test in order to
3901 clarify the result.

C.6 Packet Error Rate Measurement

3902 It is often easier to measure packet errors than it is to measure bit errors. In these cases, it is helpful to have
3903 some linkage between the packet error rate and the bit error rate. To make this linkage, we assume that the
3904 bit error rate is low enough and the packet size is small enough so that each packet error contains exactly
3905 one bit error.

3906 To complete the linkage, some care must be taken regarding how many packets to send. A bit error is only
3907 detectable in the region of the packet that is covered by the cyclic redundancy check (CRC). In the context
3908 of MIPI CSI/DSI, this applies to the payload portions of all Long Packet types. There is no guarantee that
3909 errors in the frame headers (for either Short or Long packets), and inter-packet gap will be detected.
3910 Therefore, we must translate n from the number of bits sent to the number of “observable” bits that are
3911 sent. This will increase the test duration since a portion of the time will be spent sending unobservable bits.

3912 For packets of length x bits, at least n/x packets must be sent to perform the equivalent bit error rate test. If
3913 no packet errors are observed, the conclusion is that the bit error rate is less than P_0 . If more than k_1 packet
3914 errors are observed, the conclusion is that the bit error rate is greater than P_0 .

3915 Note that x is the length of the packet after encoding (if line coding is used). In other words, in an 8B/9B
3916 encoding environment, a 64-byte packet is 576 bits in length after encoding. Also note that to reinforce the
3917 assumption that there is only one bit error per packet error, a test should be run with the shortest possible
3918 packets. However, if extremely low bit error rates are to be verified, it may be favorable to use long packets
3919 to increase the percentage of observable bits and reduce the test duration.

This page intentionally left blank.

Annex D Standardized Software Interface for Test Automation

3920 **Purpose**

3921 To define a common software interface that allows DUTs to provide access to error and fault information
3922 for the purposes of test automation, particularly RX tolerance testing.

3923 **References**

3924 None.

3925 **Last Modification**

3926 14-Apr-2015

3927 **Discussion**

3928 (Begins on following page)

D.1 Introduction

For some DUT types, proprietary tools exist, which allow access to checksum error counters, burst counters or other indicators that indicate if a receiver is able to receive data properly. To allow integration of such proprietary tools in an automated test environment the following interface can be implemented which acts as wrapper for such tools (definition given in C#.Net).

D.2 Software Interface Definition

```
3933 public interface IBerReader
3934 {
3935     /// <summary>
3936     /// This method will be called once to connect your BER reader.
3937     /// </summary>
3938     /// <param name="address">The address string can be used by your implementation
3939     /// to configure the connection to the MipiBerReader interface</param>
3940     void Connect(string address);
3941
3942     /// <summary>
3943     /// This method will be called once the connection should be closed
3944     /// </summary>
3945     void Disconnect();
3946
3947     /// <summary>
3948     /// This method will be called prior the individual tests to tell the device
3949     /// what mode is tested. This can be used to load appropriate
3950     /// setups.
3951     /// </summary>
3952     /// <param name="mode">configuration mode in which the DUT will be tested</param>
3953     void Init(string mode);
3954
3955     /// <summary>
3956     /// Will be called at the beginning of the BER measurement and allows to
3957     /// implement a reset for a DUT.
3958     /// </summary>
3959     void ResetDut();
3960
3961     /// <summary>
3962     /// Start the counters. This method MUST reset the counters!
3963     /// </summary>
3964     void Start();
3965
3966     /// <summary>
3967     /// Stop the DUT to read out the counters (see
3968     /// GetReadCounterWithoutStopSupported()).
3969     /// </summary>
3970     void Stop();
```

```
3971     /// <summary>
3972     /// This method should return counters, one counting the bits/frames/lines
3973     /// or bursts and one counting the errors detected by the MipiBerReader.
3974     /// The automation software will compute the BER using the following
3975     /// equation BER=errorCounter/bitCounter. If bitCounter stays at 0 even
3976     /// if the stimmmulus is sending data then this will also interpreted as fail.
3977     /// </summary>
3978     /// <param name="bitCounter">Contains the number of bits which are received
3979     /// by the DUT. If it is not possible to count bits the value can also contain
3980     /// frames, or bursts. It is just a matter of the value defined as target BER.
3981     /// If it is not possible to get the number of bits/frames/bursts then the
3982     /// method can return a value of -1 and the automation software can compute
3983     /// the number of bits by the data rate and the time of running.</param>
3984     /// <param name="errorCounter">Total number of errors since the last start.
3985     /// </param>
3986     void GetCounter(out double bitCounter, out double errorCounter);
3987
3988     /// <summary>
3989     /// This method should return a boolean value depending if the device supports
3990     /// reading the counters while it is running or not. In case of this method
3991     /// returns a false then the device needs to be stopped for reading the counters.
3992     /// In this case the automation software will stop data transmission
3993     /// before calling the GetCounter() function, and starting the system after
3994     /// that again.
3995     /// </summary>
3996     /// <returns>false if device needs to be stopped before reading the counters,
3997     /// and true if the counters can be read on the fly.</returns>
3998     bool GetReadCounterWithoutStopSupported();
3999
4000     /// <summary>
4001     /// This number is used to check if all frames where counted, because from the
4002     /// data rate divided by BitsPerFrame the number of frames can be computed and
4003     /// compared with the number given by the bit counter / frame counter resulted
4004     /// by the GetCounter() function. If this property is one the bit counter
4005     /// is exactly a bit counter and not a frame counter.
4006     /// If this number is -1 then the bits per frame is not defined
4007     /// </summary>
4008     double BitsPerFrame {set; get;}
4009
4010     /// <summary>
4011     /// This number is used to compute the BER out of the bit counter of
4012     /// the GetCounter() function. This number can be smaller then the BitsPerFrame
4013     /// because if i.e. the error counter is resulted from the checksum
4014     /// then only the payload will taken into account.
4015     /// if this property is -1 then the counted bits per frame will be
4016     /// estimated by test automation.
4017     /// </summary>
4018     double CountedBitsPerFrame {set; get;}
4019 }
```

This page intentionally left blank.

Annex E MIPI Product Registry Requirements for C-PHY

Purpose

To define the list of applicable/required tests, for the purpose of the MIPI Product Registry program.

References

None.

Last Modification

12-Feb-2016

Discussion

The MIPI Alliance is pleased to provide MIPI Member companies the opportunity to list their qualifying products in the MIPI Product Registry [*MIPI02*]. This Annex details the MIPI Product Registry qualification requirements for products implementing the C-PHY Specification. For more information on the MIPI Product Registry program, please refer to the governing MIPI Policy document [*MIPI03*].

Important Notice: The MIPI Product Registry is not a certification or compliance program. The MIPI Product Registry lists products that have been evaluated by Members, through either self-testing or a qualified independent test lab. MIPI Alliance does not itself evaluate implementations or confirm assertions of conformance.

A C-PHY product qualifies for the MIPI Product Registry by passing all tests that both (a) are marked as "Mandatory" in the following Table, and (b) are relevant for the particular product. A test is relevant if and only if the product implements the corresponding C-PHY feature. If a given C-PHY feature is not implemented in the product, then all tests associated with that feature are not applicable to MIPI Product Registry qualification and need not be passed.

For C-PHY, the "Mandatory" tests are those that can be observed and performed though the C-PHY interface.

Note: Apart from MIPI Product Registry qualification, the MIPI Alliance encourages its members to exercise as many applicable tests as possible at appropriate product development stages.

Table E-1: MIPI Product Registry Test Applicability

Test	Description	Required for MIPI Product Registry
1.1.1	LP-TX Thevenin Output High Level Voltage (VOH)	Mandatory
1.1.2	LP-TX Thevenin Output Low Level Voltage (VOL)	Mandatory
1.1.3	LP-TX 15%-85% Rise Time (TRLP)	Mandatory
1.1.4	LP-TX 15%-85% Fall Time (TFLP)	Mandatory
1.1.5	LP-TX Slew Rate vs. CLOAD ($\delta V/\delta t_{SR}$)	Mandatory
1.1.6	LP-TX Pulse Width of Exclusive-OR Clock (TLP-PULSE-TX)	Mandatory
1.1.7	LP-TX Period of Exclusive-OR Clock (TLP-PER-TX)	Mandatory
1.2.1	TLPX Duration	Mandatory
1.2.2	T3-PREPARE Duration	Mandatory
1.2.3	T3-PREBEGIN Duration	Mandatory

1.2.4	T3-PROGSEQ Duration	Mandatory
1.2.5	T3-PREEND Duration	Mandatory
1.2.6	T3-SYNC Duration	Mandatory
1.2.7	HS-TX Differential Voltages (VOD-AB, VOD-BC, VOD-CA)	Mandatory
1.2.8	HS-TX Differential Voltage Mismatch (Δ VOD)	Mandatory
1.2.9	HS-TX Single-Ended Output High Voltages	Mandatory
1.2.10	HS-TX Static Common-Point Voltages (VCPTX)	Mandatory
1.2.11	HS-TX Static Common-Point Voltage Mismatch (Δ VCPTX(HS))	Mandatory
1.2.12	HS-TX Dynamic Common-Point Variations Between 50-450MHz (Δ VCPTX(LF))	Mandatory
1.2.13	HS-TX Dynamic Common-Point Variations Above 450MHz (Δ VCPTX(HF))	Mandatory
1.2.14	HS-TX Rise Time (tR)	Mandatory
1.2.15	HS-TX Fall Time (tF)	Mandatory
1.2.16	T3-POST Duration	Mandatory
1.2.17	30%-85% Post-EoT Rise Time (TREOT)	Mandatory
1.2.18	THS-EXIT Value	Mandatory
1.2.19	HS Clock Instantaneous UI (UIINST)	Mandatory
1.2.20	HS Clock Delta UI (Δ UI)	Mandatory
1.3.1	INIT: LP-TX Initialization Period (TINIT,MASTER)	Mandatory
1.3.2	ULPS Exit: Transmitted TWAKEUP Interval	Mandatory
1.3.3	BTA: TX-Side TTA-GO Interval Value	Not Applicable
1.3.4	BTA: RX-Side TTA-SURE Interval Value	Not Applicable
1.3.5	BTA: RX-Side TTA-GET Interval Value	Not Applicable
2.1.1	LP-RX Logic 1 Input Voltage (VIH)	Mandatory
2.1.2	LP-RX Logic 0 Input Voltage, Non-ULP State (VIL)	Mandatory
2.1.3	LP-RX Input Hysteresis (VHYST)	Mandatory
2.1.4	LP-RX Minimum Pulse Width Response (TMIN-RX)	Mandatory
2.1.5	LP-RX Input Pulse Rejection (eSPIKE)	Mandatory
2.2.1	LP-RX Initialization period (TINIT)	Mandatory
2.2.2	ULPS Exit: LP-RX TWAKEUP Timer Value	Mandatory
2.2.3	LP-RX Invalid/Aborted Escape Mode Entry	Mandatory
2.2.4	LP-RX Invalid/Aborted Escape Mode Command	Mandatory
2.2.5	LP-RX Escape Mode, Ignoring of Post-Trigger-Command Extra Bits	Mandatory
2.2.6	LP-RX Escape Mode Unsupported/Unassigned Commands	Mandatory
2.3.1	HS-RX Amplitude Tolerance (VCPRX(DC), VIHHS, VILHS)	Mandatory

2.3.2	HS-RX Differential Input High/Low Thresholds (VIDTH, VIDTL)	Mandatory
2.3.3	HS-RX Jitter Tolerance	Mandatory
2.4.1	HS-RX T3-TERM-EN Duration	Mandatory
2.4.2	HS-RX T3-PREPARE Tolerance	Mandatory
2.4.3	HS-RX T3-PREBEGIN Tolerance	Mandatory
2.4.4	HS-RX T3-PROGSEQ Tolerance	Mandatory
2.4.5	HS-RX T3-POST Tolerance	Mandatory
3.1.1	HS-TX Differential Return Loss (SDD22)	Not Applicable
3.1.2	HS-TX Common-Mode Return Loss (SCC22)	Not Applicable
3.1.3	HS-TX Mode Conversion Limits (SDC22)	Not Applicable
3.1.4	HS-TX Single-Ended Output Impedance (ZOS)	Not Applicable
3.1.5	HS-TX Single-Ended Output Impedance Mismatch (ΔZOS)	Not Applicable
3.2.1	HS-RX Differential Return Loss (SDD11)	Not Applicable
3.2.2	HS-RX Common-Mode Return Loss (SCC11)	Not Applicable
3.2.3	HS-RX Mode Conversion Limits (SDC11)	Not Applicable
3.2.4	HS-RX Differential Input Impedance (ZID)	Not Applicable
3.2.5	HS-RX Differential Input Impedance Mismatch (ΔZID)	Not Applicable
3.3.1	LP-TX Output Impedance (ZOLP)	Not Applicable
3.3.2	LP-RX Input Leakage Current (ILEAK)	Not Applicable

This page intentionally left blank.

Annex F RX Test Observables for DUT Device Types

Purpose

To discuss various options for DUT observable behavior for performing LP/HS-RX testing, for different types and classes of C-PHY-based DUTs.

References

- [1] C-PHY Specification, Section 5.5
- [2] DSI-2 Specification, Section 5.2.3 (C-PHY Command Mode Interfaces)
- [3] C-PHY Specification, Section 12

Last Modification

17-Oct-2008

Discussion

F.1 Introduction

For performing the RX tolerance tests of Section 2, almost all test procedures involve variations of the same basic theme:

- Generate and transmit a controlled test stimulus sequence that is specifically designed to isolate the parameter of interest.
- Verify successful (or unsuccessful) reception of the test stimulus by the DUT.

Note that depending on the test, the stimulus may be a “pure” LP sequence (e.g., Escape Mode Command), or an HS Burst sequence (which inherently contains LP signaling, as the LP-111 Stop state and HS Entry process are valid and defined LP sequences.)

The preferred method to verify the receiver for tests that use an HS Burst sequence is to utilize the C-PHY built-in test functions defined in the C-PHY Specification [3]. This defines the use of specific PRBS functions and defines a set of control and status registers to set up specific test conditions and observe results within the C-PHY without having to probe the interface or make use of any higher-level protocol functions. This is particularly useful for “bare phy” devices that might exist as test chips.

In case the designer chooses not to use the C-PHY built-in test functions defined in the C-PHY Specification [3], RX tests must utilize some aspect of basic device operation as an observable mechanism in order to determine whether or not a particular test stimulus was successfully received. The difficulty of this however, is that there is no single common observable that is guaranteed to be supported by all MIPI product classes (e.g., CSI-2, DSI-2). In addition, because this test suite supports testing of different C-PHY DUT types (e.g., bare phy, phy + protocol test IC’s, finished products, hosts, peripherals, etc.), identification of a suitable observable may depend heavily on the DUT type and implementation. In this Annex, options for several different device types and classes will be discussed. While this Annex is not intended as an exhaustive list, it does describe a set of options that should cover a majority of cases.

F.2 Bare C-PHY

In the case of a “bare phy” (meaning a test IC which does not include a protocol layer, and includes some type of parallel PPI-like interface), a common approach is to probe the HS and LP signals of the parallel interface to verify that the stimulus sent into the C-PHY LP/HS interface is accurately received. However, the recommended approach is to use the built-in test functions described in the C-PHY Specification [3]. This detailed test function description can be used to ensure compatibility between test equipment and the device under test.

4080 Typically, two slightly different configurations are used for performing LP vs. HS tests. Because of the
4081 simpler nature of the LP output of the parallel interface, a DSO may be used to monitor the interface's LP
4082 output, while a repeated LP stimulus is presented at the C-PHY interface. Differential probes may be
4083 connected at the C-PHY and parallel interfaces, and the logical output observed at the parallel interface can
4084 be directly verified against the LP stimulus presented at the C-PHY input, by overlaying the two traces on a
4085 DSO screen. Typically the input parameter can be varied to find the threshold point at which the parallel
4086 interface output no longer matches the C-PHY input. (Note it is also not uncommon for there to be an
4087 'intermittent' region, prior to total failure, where behavior may show sporadic errors, but not totally failing.
4088 It may be of informative use to note these cases, however in most test procedures, the last point at which
4089 'consistent' valid behavior was observed is take to be the measured threshold point.)

4090 For HS tests, it is not practical to verify the parallel data by observation using a DSO. In this case however,
4091 a Logic Analyzer can be used to verify the parallel output stream against a known C-PHY HS input.

4092 The specific HS data pattern used as the test stimulus should be chosen to isolate the parameter under test.
4093 For the purposes of most HS-RX tests (e.g., common mode/differential amplitude tests, etc.), it is advisable
4094 to use a test pattern that lends itself to accurate amplitude measurements (e.g., a repeating 1010, 11001100,
4095 or 11110000 pattern, etc.) versus a 'stressful' worst-case pattern such as the BER test pattern defined in
4096 Annex D. While the worst-case pattern might seem like a better choice, it actually complicates the test
4097 methodology, as it can be more difficult to measure (and thus calibrate an accurate amplitude level for the
4098 RX Test System signal source). Also, it contains frequency-dependent subsections, which may behave
4099 differently as they are affected by the frequency-dependent losses occurring between the point where the
4100 signals are injected into the DUT (e.g., SMA connectors on the test PCB), and the point corresponding to
4101 the C-PHY IC pins. The added factors of decreased calibration accuracy and unknown/uncontrollable
4102 frequency-dependent effects can decrease overall test repeatability and accuracy.

4103 For all HS-RX tests (except the informative RX jitter test), a repeating 11001100 data pattern will be used
4104 for the HS burst payload data. (Note an explicit HS burst length is not specified here, however it is
4105 recommended that the test pattern be roughly as long as a typical Long Packet, i.e., several thousand bits.)

F.3 DSI-2 Display Device (C-PHY + DSI-2 Protocol + Display Driver + Glass, Integrated)

4106 In the case of a finished DSI display product, all of the components are typically integrated into a single
4107 package, and no access to any parallel interface is available. In this case, there are multiple potential
4108 observable mechanisms:

- 4109 • Incorporate the built-in test functions in the display device, or display driver IC, and use the
4110 standard DSI-2 register read/write functions to control and monitor the built-in test functions and
4111 status monitoring circuitry. A detailed test register definition is provided in the C-PHY
4112 Specification [3]. The starting address of this built-in test register space is flexible to
4113 accommodate the needs of each application.
- 4114 • The displayed image (i.e., visual inspection of HS pixel data)
- 4115 • For DCS (i.e., Command Mode) displays, observation of panel behavior in response to LP- or HS-
4116 issued DCS commands (e.g., toggling display backlight, power, color mode, invert mode, etc.)
- 4117 • For non-DCS (Video Mode) displays, observation of panel behavior in response to LP- or HS-
4118 issued DSI commands (e.g., *Color Mode On/Off*, *Turn On Peripheral/Shutdown Peripheral*, etc.)
- 4119 • For Command Mode displays (and optionally Video Mode displays that support bi-directional
4120 communication), acknowledgement of a variety of defined error types can be observed via
4121 presence of an *Acknowledge and Error Report* packet from the display, which can be triggered by
4122 initiating a Bus Turn-Around (BTA) event from the host. If any of the defined error types have
4123 been detected by the display, an *Acknowledge and Error Report* packet will be sent by the display
4124 following a BTA.

- 4125 • Access to vendor-specific internal registers and status indicators through the C-PHY interface (if
4126 the display supports bi-directional communication), which may be queried in order to determine
4127 the result of a previous stimulus.

4128 **Command Mode Displays**

4129 For LP tests, if the DUT supports the DCS command set, the easiest stimulus/observable vehicle is to
4130 transmit the DCS **set_display_on** and **set_display_off** commands to the DUT using LP signaling. This
4131 involves transmitting the following sequence:

4132 **Escape Mode Entry Sequence + Escape Mode LPDT Command + LPDT-encoded DCS Command Packet**

4133 Using this sequence as a test vehicle, all of the LP electrical parameters can be varied, and the on/off
4134 behavior of the display can be used as the observable to determine whether or not the stimulus was received
4135 correctly. Note however that because LP commands are only transmitted on Data Lane 0 for DSI devices,
4136 this technique only allows for exercising the full set of C-PHY LP-RX characteristics for Data Lane 0 of a
4137 DSI display device.

4138 For HS-RX testing of Command Mode displays, it is possible to leverage the fact that Command Mode
4139 displays will always support reverse direction capability. Thus, any series of HS packets can be followed by
4140 a Bus Turn-Around (BTA) assertion, after which a display will respond is required to respond with an
4141 *Acknowledge and Error Report* packet, if any of the defined error types were observed since the last
4142 peripheral-to-host transaction. While many of the error types can be used as observables for various tests,
4143 the *Checksum Error* type (bit 10) is of primary interest, as it provides observability across an arbitrarily
4144 long series of HS bits/packets sent to the DUT. If a checksum error was detected for any HS packet since
4145 the last peripheral-to-host transaction, it will be identified by the peripheral via the transmission of an
4146 *Acknowledge and Error Report* packet. This mechanism allows system and component Bit Error Rate
4147 verification tests to be performed. (See Test 2.3.3, and Annex C of this document for more about BER
4148 tests.)

4149 Also, another option that can be used for nearly all of the HS-RX tests (particularly any measurement that
4150 requires finding the failure point of the DUT, e.g., amplitude or timing thresholds) would be to use the same
4151 methodology described above for the LP tests (e.g., DCS **set_display_on** and **set_display_off** commands
4152 to the DUT), but send them using HS signaling. The success or failure of reception can readily and easily
4153 be determined by visual inspection of the DUT's behavior.

4154 **Video Mode Displays**

4155 To perform LP-RX tests on Video-Mode-only displays, a modified version of the Command Mode
4156 methodology above can be used. While Video Mode displays are not *required* to support all of the defined
4157 DSI commands, it is likely that most Video-Mode-only displays will support the **Shutdown Peripheral** and
4158 **Turn On Peripheral** commands. These commands are similar in nature to the DCS **set_display_on** and
4159 **set_display_off** counterparts, and can be used in the same fashion as a vehicle for performing LP-RX tests
4160 on displays that only support Video Mode. (Though again, the same issue applies to Video Mode displays,
4161 in that these commands are only received on Data Lane 0, leaving the same remaining question of how to
4162 test LP-RX functionality on Data Lanes 1 and 2.)

4163 In the event that a Video-Mode-only display does not support the **Shutdown Peripheral** and **Turn On**
4164 **Peripheral** commands, an alternative supported command will have to be determined (preferably a simple
4165 non-image-data command, which produces a visible behavior on the panel), however the general
4166 methodology will otherwise be the same.

4167 HS-RX testing of Video-Mode-only displays can be performed using the same method described in the
4168 previous paragraph for LP-RX, but by sending the commands using HS signaling. (Again, this applies
4169 primarily to amplitude and timing threshold measurements.)

For BER-style HS-RX tests, the same methodology described above for Command Mode displays can be used, but only if the Video Mode display supports bi-directional communication (which is possible and allowed by the specification, however not likely to be the case for most typical Video Mode displays).

Unfortunately, for Video-Mode-only displays that only support unidirectional communication, the only real observable for performing a BER-type test is the display glass itself. In this case, visual inspection of the displayed image for distortion or other artifacts can be used, however depending on the test time (and the reliability of the human observer), this is more of a qualitative observable, rather than a quantitative one.

F.4 CSI-2 Image Sensor (C-PHY + CSI-2 Protocol + Image Sensor Module)

Although this Annex relates to Rx devices, it is worth noting some useful capabilities that can be incorporated into CSI-2 transmitter devices (Image Sensors) to make interoperability testing easier and to be a more thorough test than could be normally achieved. Again, it is highly recommended to include in the image sensor module the built-in test functions described in the C-PHY Specification [3]. This will allow PHY to PHY interoperability testing to take place without having to involve the protocol layer. The precise definition of the built-in test circuitry ensures that the transmitter and receiver test functions will be compatible.

In case the built-in test functions are not included in the transmitter, similar principles of image transmission and CRC error checking described above for display testing can be applied to CSI-2 devices as well.

F.5 Lane-Dependent Limitations of LP Test Patterns

For most LP-RX tests, it would be desirable to use a test sequence that contained only LP-based signaling (e.g., Escape Mode commands, or DSI/DCS packets sent via LPDT). However, one limitation of this approach is that for CSI and DSI implementations (i.e., non-bare-phy DUT types), LPDT communication is restricted to Data Lane 0 only. This means LPDT test sequences cannot be used on Data Lanes 1 and 2.

Furthermore, Escape Mode behavior is also restricted for the different Lanes. The C-PHY spec states that “*All Lanes shall include Escape mode support for ULPS and Triggers in the Forward direction.*”[1], however the DSI spec states that, “*All Trigger messages shall be communicated across Data Lane 0.*”[2]. This means that for many DUT cases, the available options for LP test patterns for use on Data Lanes 1 and 2 will be severely restricted.

One pattern that may offer some opportunity is the ULPS Escape Mode command, as all Data Lanes are still required to support this command, as Lanes must still be put into ULPS individually via this command. Technically this should offer attractive potential as a test mechanism, however the difficulty comes in terms of observability, as there is no easy way to visually determine if a Lane has entered the ULPS state by visual inspection. Lanes should technically not accept any LP/HS traffic while in ULPS, until they have been brought out of ULPS via a proper ULPS exit sequence. This fact could be used as a test mechanism, (e.g., send test ULPS sequence, then verify acceptance of some other valid command to see if ULPS command was successful).

One other option exists for exercising different Lanes of a DUT, which is referred to as Lane Remapping, and is described below.

F.6 Lane Remapping

For some DUT types, one additional option exists, which can be leveraged to allow testing of various HS- and LP-RX parameters for different Lanes of a multi-Lane DUT. It is somewhat of a trick, and is called Lane Remapping.

Many DUTs, particularly Hosts, support the capability to reprogram their Lane configuration, such that the number and ordering of the Data Lanes can be arbitrarily assigned, in addition to the position of the Clock Lane also being programmable. In this case, any of the DUT ports can be configured to serve as Data Lane 0, thus allowing the full set of LPDT test patterns to be used to test the LP-RX characteristics of that DUT

4213 port. Granted, the Lane will always be tested as a Data Lane 0, however from the perspective of validating
4214 C-PHY LP- and HS-RX physical layer characteristics, this should be irrelevant, as it is the specific silicon
4215 circuitry of each of the DUT ports that is being tested.

4216 While this methodology can typically be applied to Host DUTs, it unfortunately cannot be applied to most
4217 peripherals, as they typically do not support custom remapping of the C-PHY lanes.

This page intentionally left blank.

Contributing Individuals

The list below includes those persons who participated in the Working Group that developed this Conformance Test Suite and who consented to appear on this list.

Ahmed Abouella	Mixel, Inc.
Andy Baldman	MIPI Alliance
Min-Jie Chong	Keysight Technologies, Inc.
Thomas Dippon	Keysight Technologies, Inc.
Keyur Diwan	Tektronix, Inc.
Michael Fleischer-Reumann	Keysight Technologies, Inc.
Mohamed Hafed	Introspect Technology
Tom Kopek	ON Semiconductor
Brent Newman	Qualcomm Incorporated
Parthasarathy Raju	Tektronix, Inc.
P. E. Ramesh	Tektronix, Inc.
Ravindra Rudraraju	Intel Corporation
Tatsuya Sugioka	Sony Corporation
Axel Wankmueller	Keysight Technologies, Inc.
Rick Wietfeldt	Qualcomm Incorporated
George Wiley	Qualcomm Incorporated
Charles Wu	OmniVision Technologies, Inc.