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MIPI D-PHY Interface Test

Jack Lee

Agenda

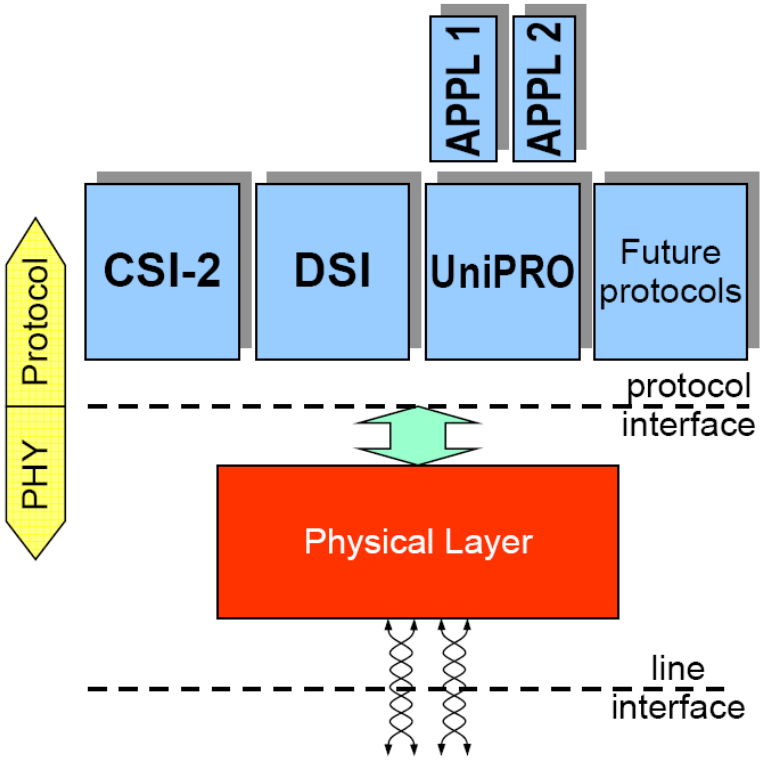
- MIPI D-PHY Overview
- Test Solutions with Standard Digital
  - D-PHY Rx
  - D-PHY Tx
- Improved Testing Capability
  - FPGA Solution on DIB
  - Protocol Aware (PA)
  - Hardware Source-Synchronous

MIPI D-PHY IP Core

Overview

MIPI D-PHY is a High-speed low power serial transceiver interface supporting interconnections of a wide range of low-power high-speed mobile applications such as digital Camera Serial Interface (CSI), graphic Display Serial Interface (DSI), UniPro™ and other MIPI devices using the PHY Protocol Interface (PPI).

- Flexible
- Low cost
- High Speed
- Low power consumption
- Serial interface



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MIPI UniPro

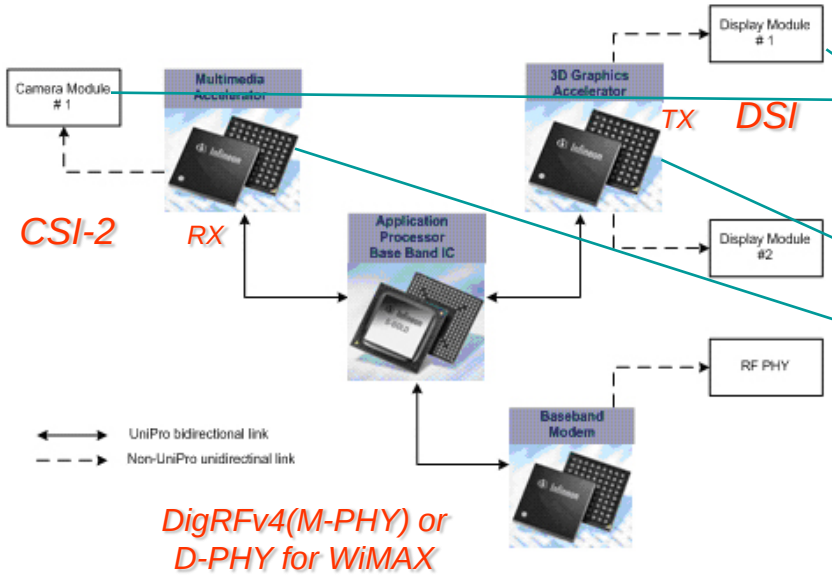
Introduction to the MIPI UniPro Standard

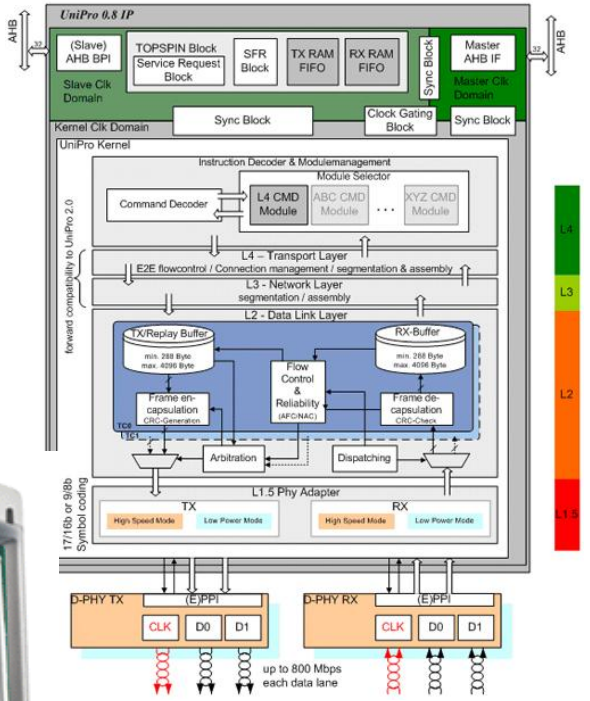
UniPro Unified Protocol IP

MIPI UniPro defines a layered protocol on a high-speed serial interface for interconnecting devices and components within mobile systems such as cellular telephones, handheld computers, digital cameras, and multimedia devices.

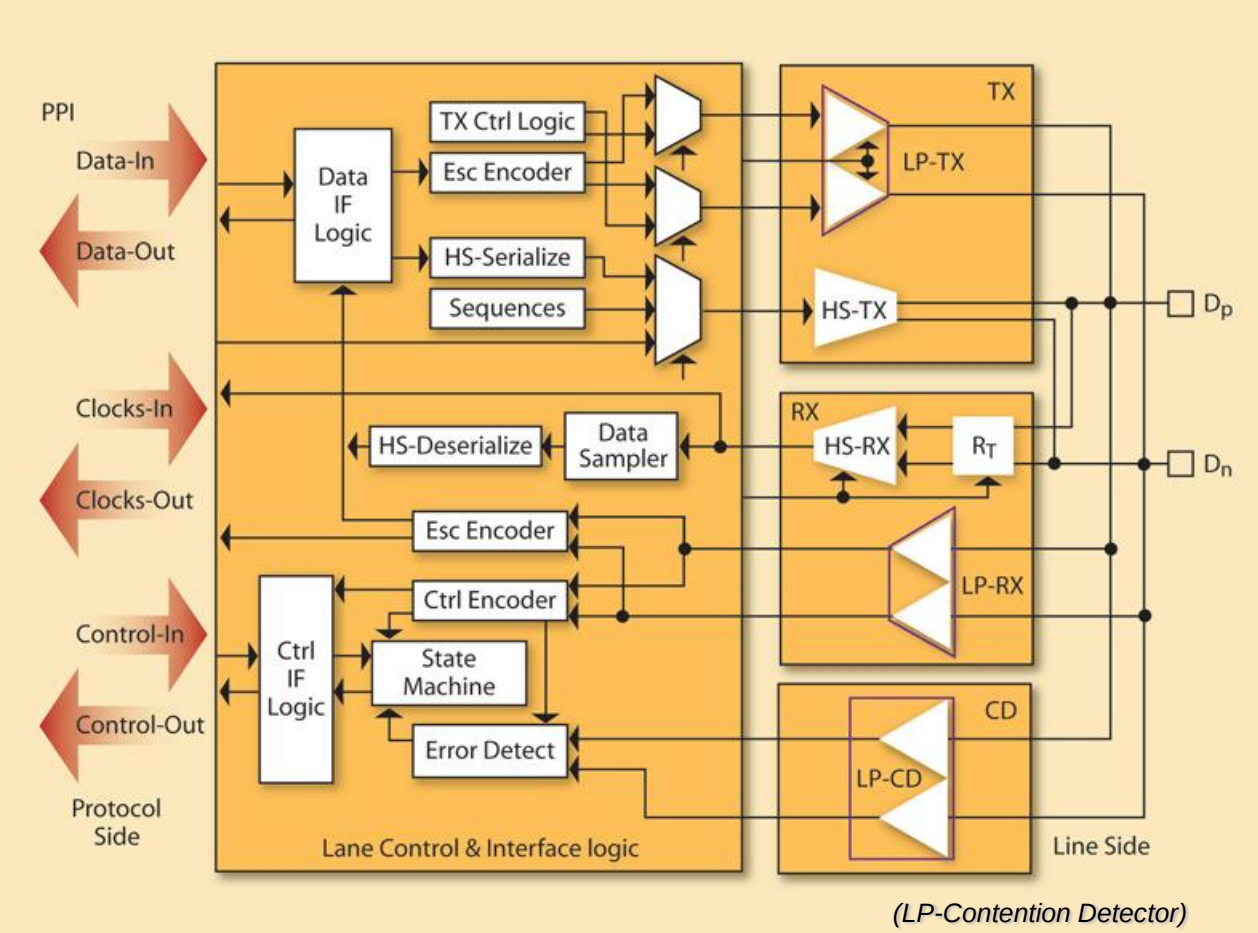
UniPro (Unified Protocol) is a standard developed by the MIPI Alliance (Mobile Industry Processor Interface, www.mipi.org).

Use Cases



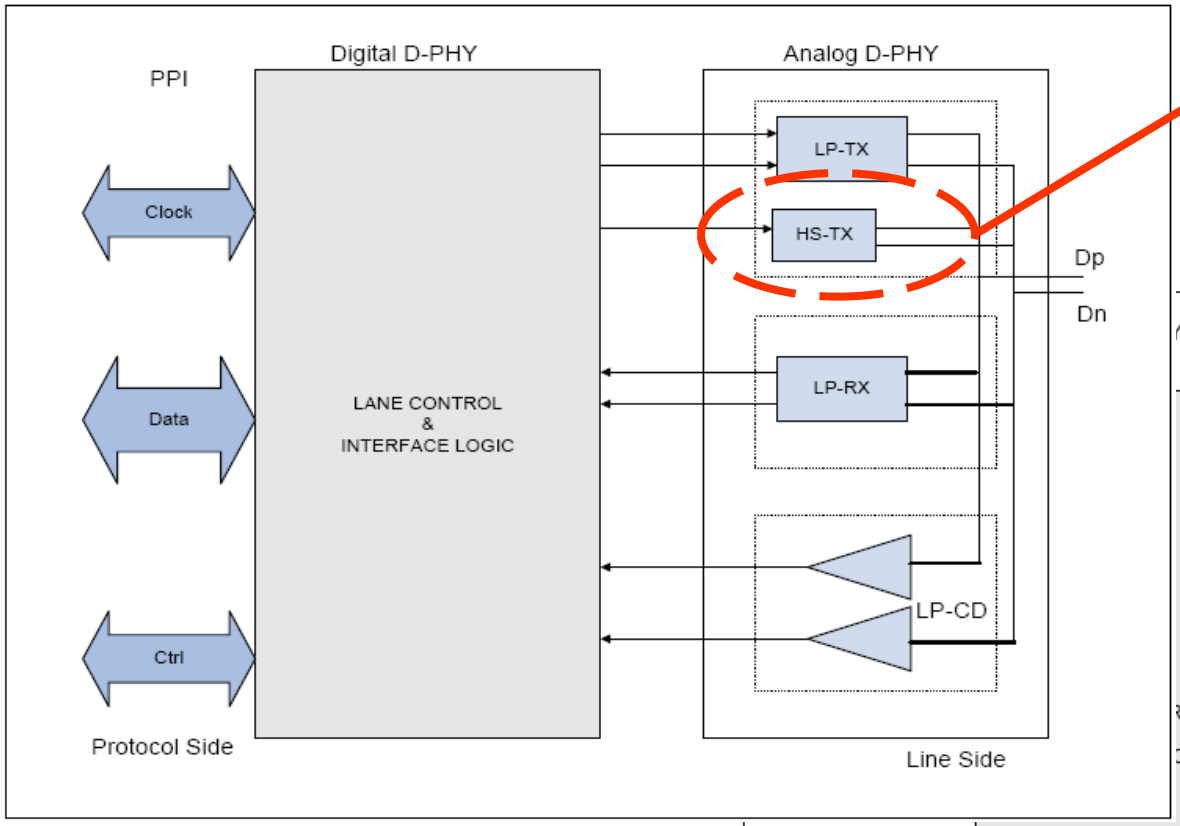


MIPI D-PHY Full Block Diagram



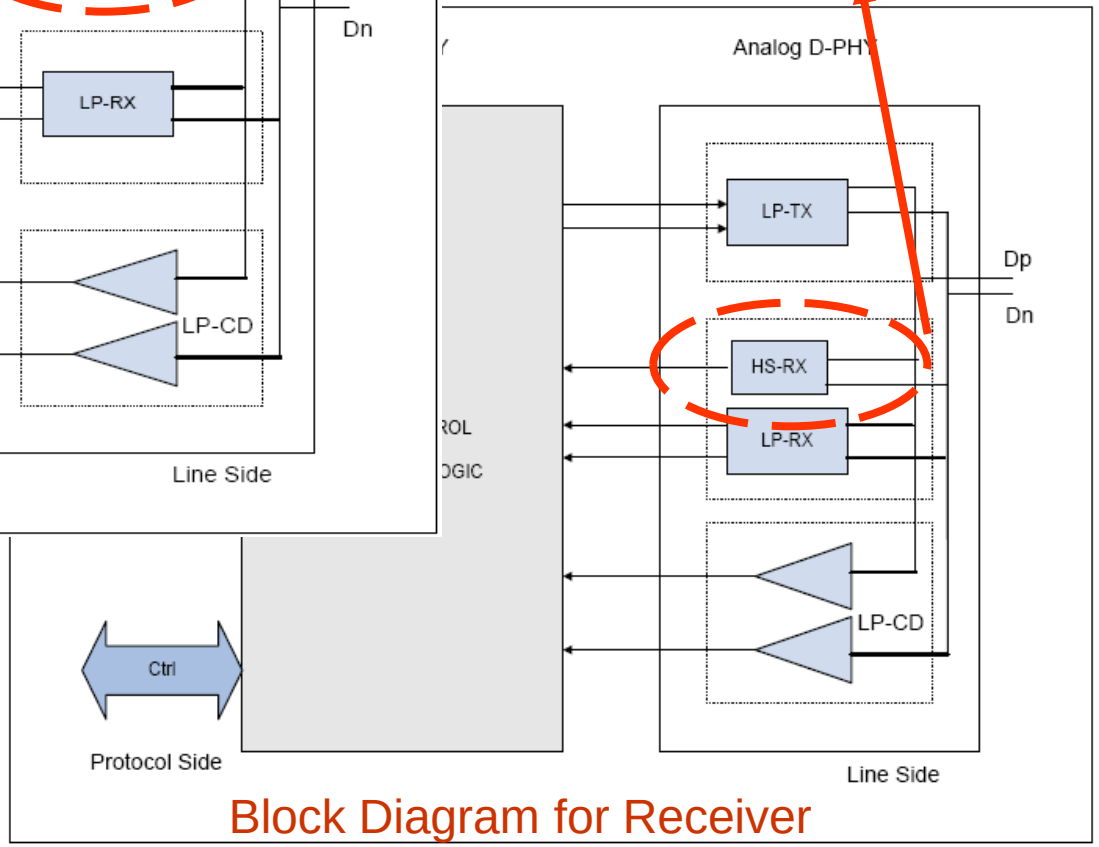
Universal Lane Mode Architecture

MIPI D-PHY Block Diagram for TX and RX



Support DSI

Support CSI

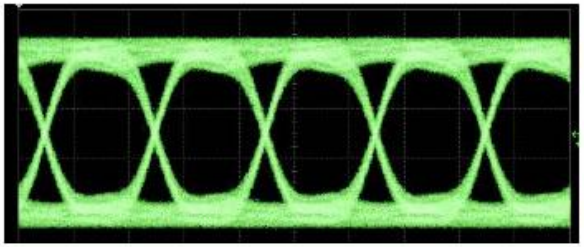


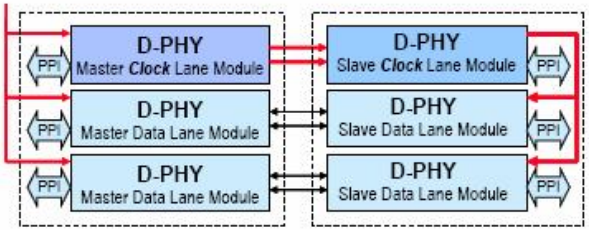
Block Diagram for Transmitter

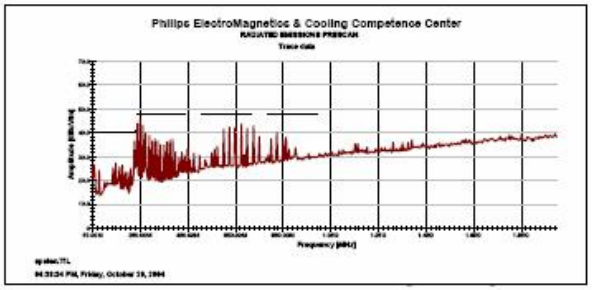
Block Diagram for Receiver

MIPI D-PHY Characteristics

- Data lanes
  - High-Speed Mode
    - Level: 400mVpp, differential for 100 ohm termination
    - Speed: 80Mb/s -1Gb/s
    - Synchronous transfer
  - Low-Power Mode
    - Level: 1.2V CMOS level driver, single-ended
    - Speed: < 10Mbps
    - Lane 0 only has LP signal
    - Asynchronous transfer
  - Bi-directionality (HSx ¼)
- Lane scalability
  - N data lanes + 1 Clock Lane
- Interconnect
  - PCBs, flexfoils, cables, connectors
  - Low pin and wire count
- Power
  - Low operational power (mW-range)
  - Very low stand-by power (uW-range)
- Robustness
  - Low EMI
  - Ease of integration
  - Noisy environment
    - Tolerance ~10mVdiff ~100mVcom







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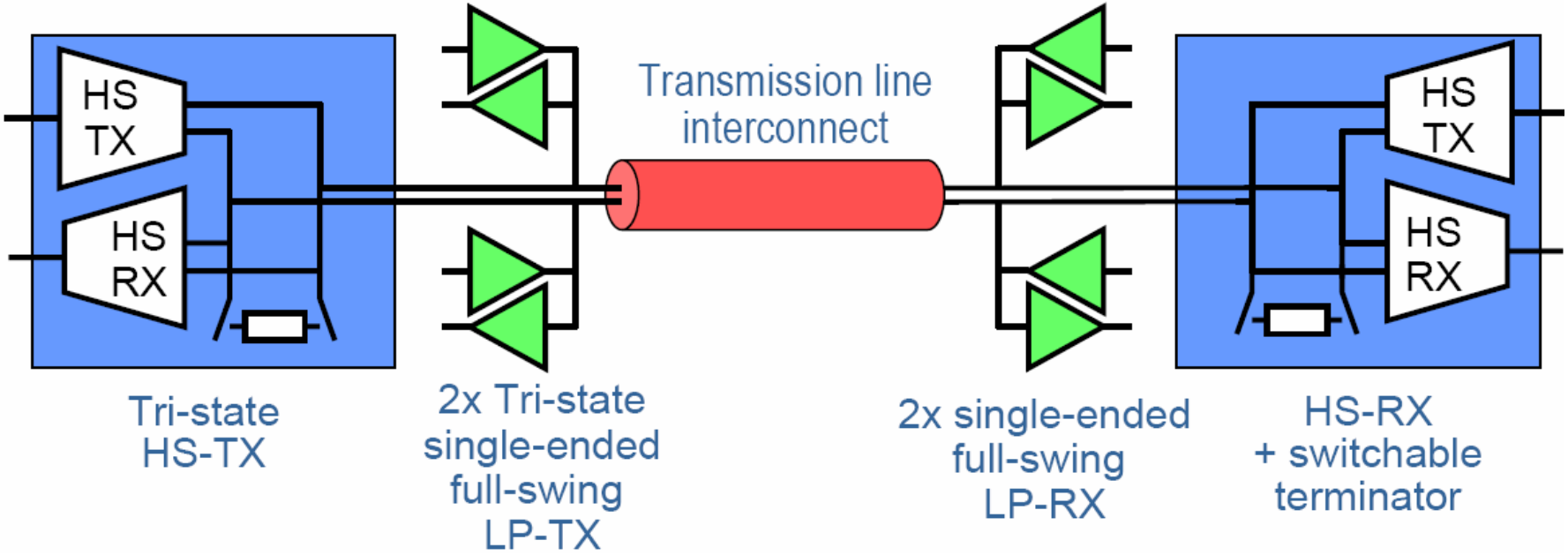
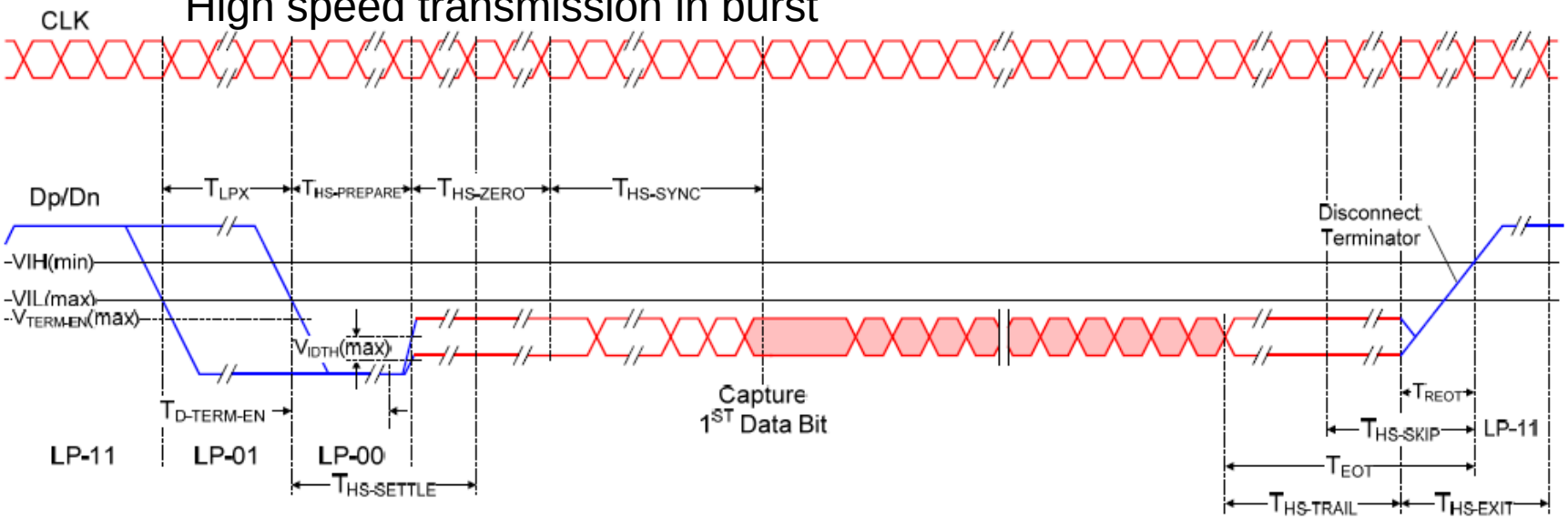
MIPI D-PHY Interface Overview

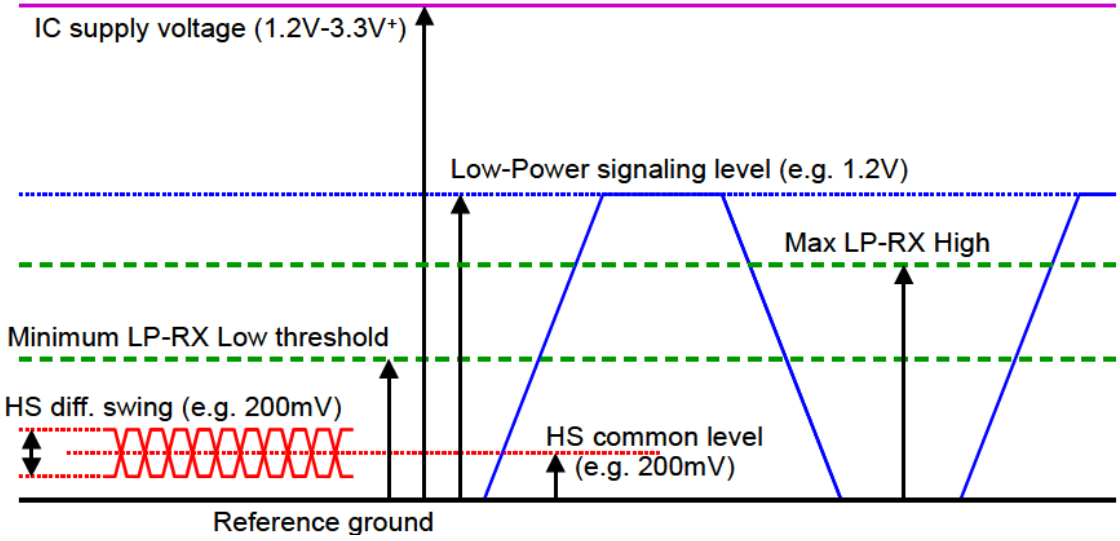
1. Serial High-speed: Fully-terminated differential signaling
   - First generation: Source-Synchronous with/without encoding
2. Low-Power: unterminated 1.2V CMOS-like signaling
   - HF filtering and 1.2V CMOS-like signaling
   - HF filtering and hysteresis for noise immunity
3. Contention detection for Bi-directionality
   - Optional reverse data transfers are Master synchronous



MIPI D-PHY Timing and level Specification

High speed transmission in burst





Line Level

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Signal Directions & Protocol Implementations

	MODE			
Device *(Baseband Processor)*	HS Drv	HS Rcv	LP Drv	LP Rcv
Tester	*HS Rcv*	*HS Drv*	*LP Rcv*	*LP Drv*
	Diff	*Diff*	*SE*	*SE*
	Term	*Term*	*HiZ*	*HiZ*
D-PHY Rx	-	Y	Y	Y
CSI-2	-	Y	Y/N	Y/N
D-PHY Tx	Y	-	Y	Y
DSI	Y	-	Y	Y

Note:
- **LP signaling only used on Lane0**
- **CSI, DSI do not support reverse traffic in the HS/4 rate**

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  - D-PHY Rx
  - D-PHY Tx
- Improved Testing Capability UP1100
  - Protocol Aware (PA)
  - Hardware Source-Synchronous

D-PHY Rx (CSI) Requirements

Device modes:

- Receive HS mode differentially
- Receive LP mode single-ended (unterminated)
- Drive LP mode single-ended

Tester Requirements:

- Drive 3(/4) levels per-line
- Drive Differential & Single-Ended
- 2 compare levels per-line
- Unterminated compare

	Test Conditions	UltraFLEX Options	Test Solution			
	D-PHY Modes (per-Burst)		DIB Components	# chans per DIFF Pair	# of unique levels *(per-line)*	LP Termination
CSI-2 *D-PHY Rx*	•Device receives HS	UP800 HSD1000 UP1100	None	2	3 drive	-
	•Device receives HS •Device receives LP •Device drives LP	UP800 HSD1000 UP1100	None	2	3 drive 2 compare	50Ω to 1.2V
		UP800 HSD1000 UP1100	3 resistors per line	4	4 drive 2 compare	HiZ

***Requires that the LP/HS mode switching is deterministic in both order & time*

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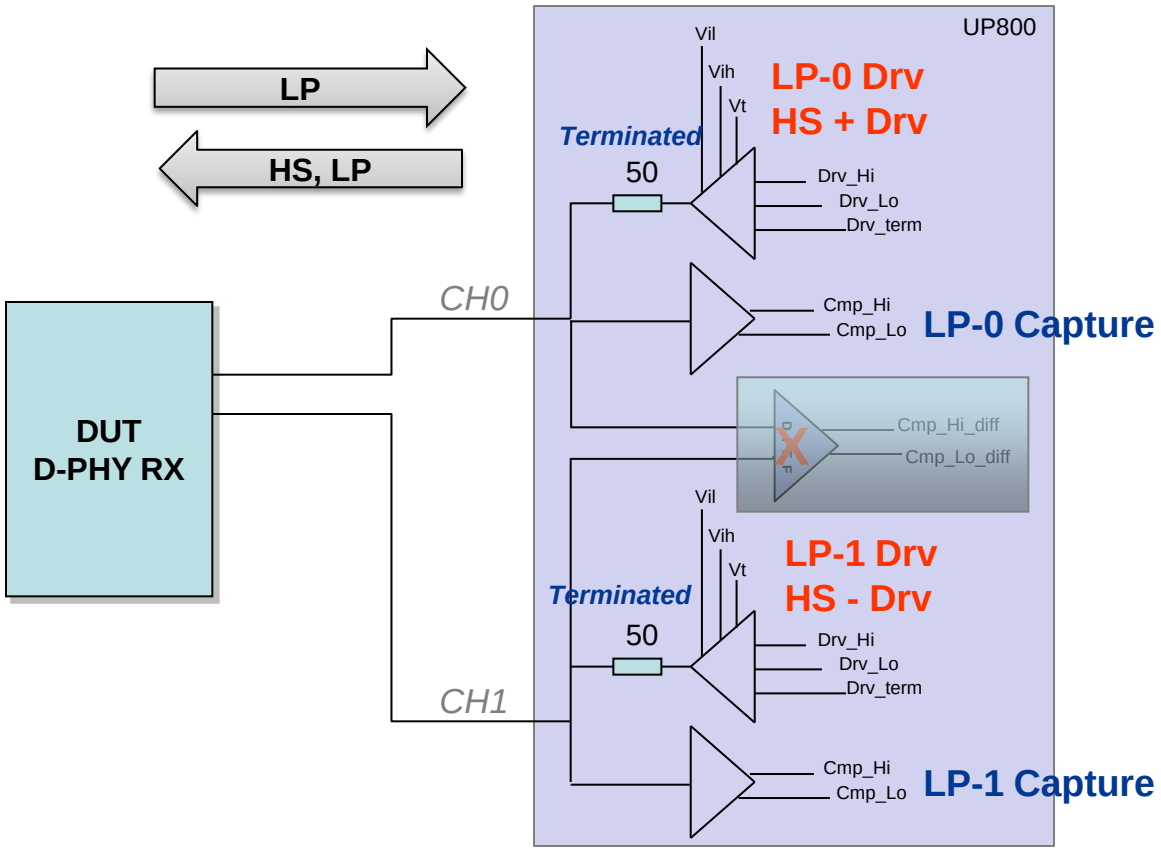
D-PHY Rx
Option #1: 3-Level Drive, Terminated LP

- 2 digital channels per diff pair
- 3 unique levels from tester drive
- Tester receive of LP only in terminated mode
  - *50ohm term to Vt = LP_Vih = 1.2V*
  - *Device must handle driving LP into 50ohms to 1.2V*

	MODE			
Device	HS Drv	HS Rcv	LP Drv	LP Rcv
Tester	*HS Rcv*	*HS Drv*	*LP Rcv*	*LP Drv*
D-PHY Rx	-	Y	Y	Y
CSI-2	-	Y	Y/N	Y/N

Param	Programmed	Use
Vil	0V	HS/LP Vlo
Vih	100mV-300mV	HS Vhi
Vt	1.2V	LP Vhi
PE Mode	*LargeSwing-VT*	-



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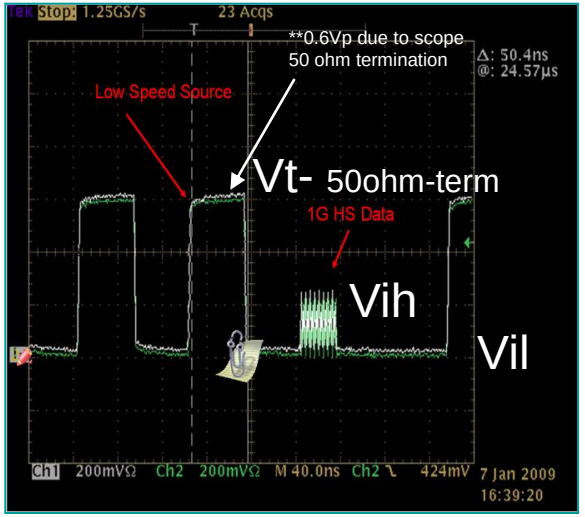

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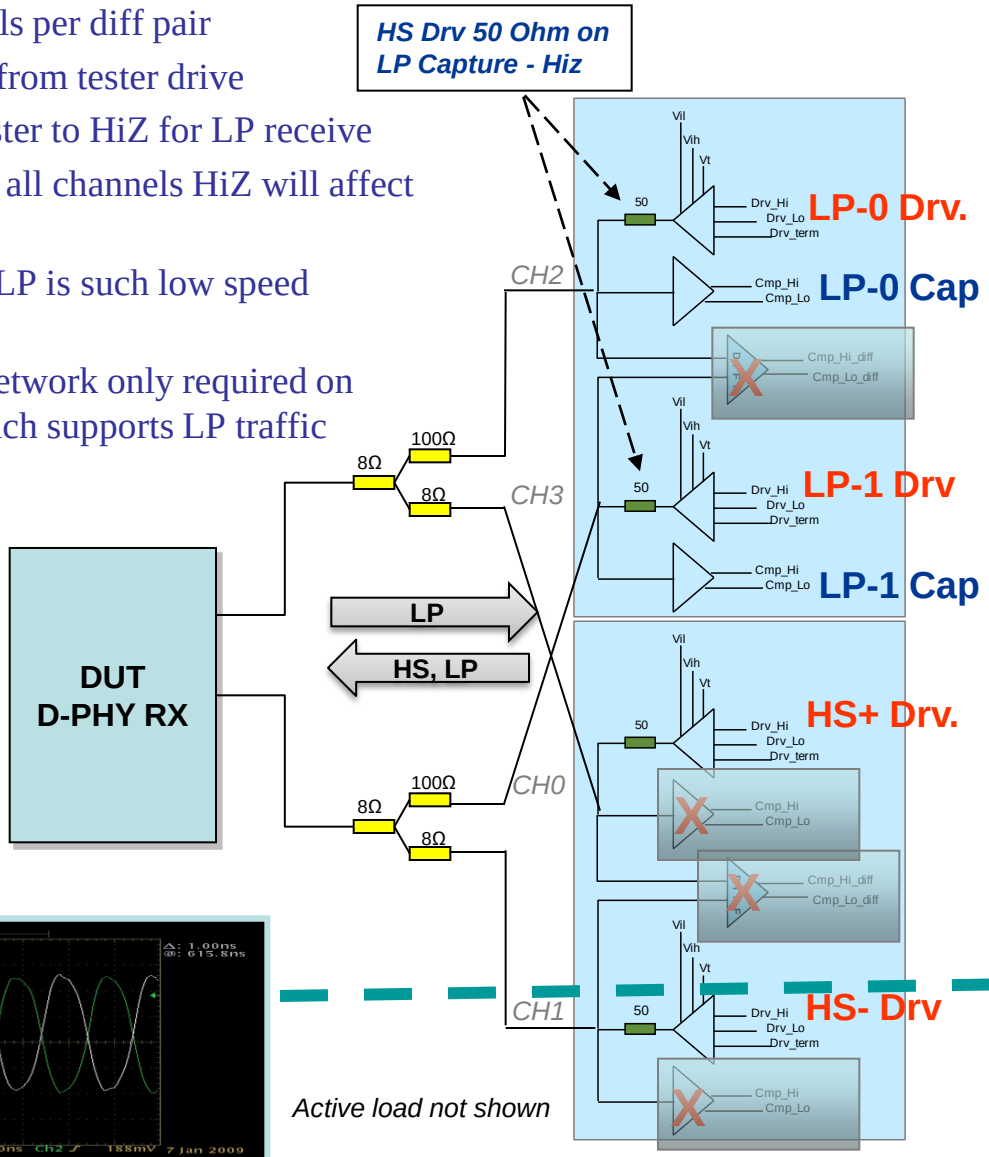
D-PHY Rx
Option #2: 3-Level Drive, Unterminated LP

- 4 digital channels per diff pair
- 3 unique levels from tester drive
  - Allows tester to HiZ for LP receive
- LP receive with all channels HiZ will affect signal integrity
  - OK since LP is such low speed (<10Mhz)
  - Resistor network only required on Lane0 which supports LP traffic

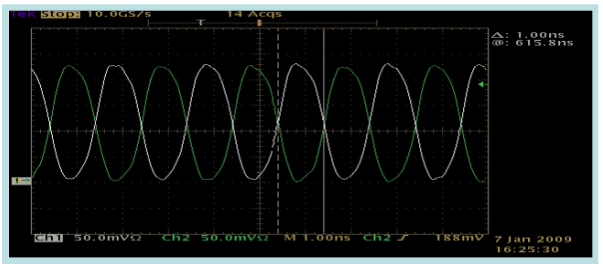


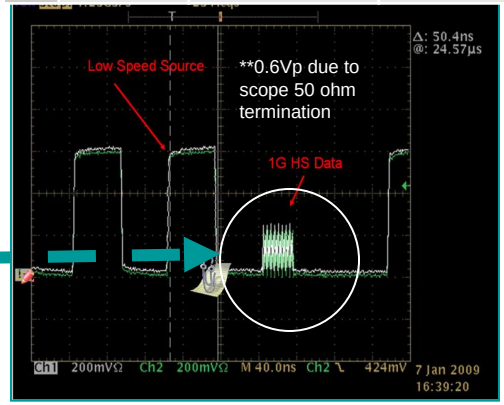
Active load not shown

	MODE			
Device	HS Drv	HS Rcv	LP Drv	LP Rcv
Tester	*HS Rcv*	*HS Drv*	*LP Rcv*	*LP Drv*
D-PHY Rx	-	Y	Y	Y
CSI-2	-	Y	Y/N	Y/N

	Param	Programmed	Use
Chan 0, 1 (HS)	Vil	Vcm - 2*Vdiff/2	HS Vil
	Vih	Vcm + 2*Vdiff/2	HS Vih
	Vt	-	-
	PE Mode	*LargeSwing-HiZ*	-

	Param	Programmed	Use
Chan 2, 3 (LS)	Vil	0V	LP Vil
	Vih	1.2V	LP Vih
	Vt	-	-
	Vol	*550mV*	LP Vol
	Voh	680mV	LP Voh
	PE Mode	*LargeSwing-HiZ*	





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D-PHY Tx (DSI) Requirements

Device modes:

- Drives HS differential
- Drives LP single-ended
- Receive LP single-ended (unterminated)

Tester Requirements *(within a single burst)*:

- Compare differential & single-ended
- Terminated & Unterminated compare
- 4 compare levels (per-line)
- 3 bits of unique compare data (per-pair)
- Drive 2 levels per-line

	Test Conditions	UltraFLEX Options	Test Solution			
	D-PHY Modes (per-Burst)		DIB Components	# chans per DIFF Pair	# of unique levels	LP Termination
DSI *D-PHY Tx*	•Device drives HS	UP800 HSD1000 UP1100	None	2	2 compare per burst	-
	•Device drives HS •Device drives LP •Device receives LP	UP800 HSD1000 UP1100	3 resistors per line	4	4 compare 2 drive	HiZ

***Requires that the LP/HS mode switching is deterministic in both order & time*

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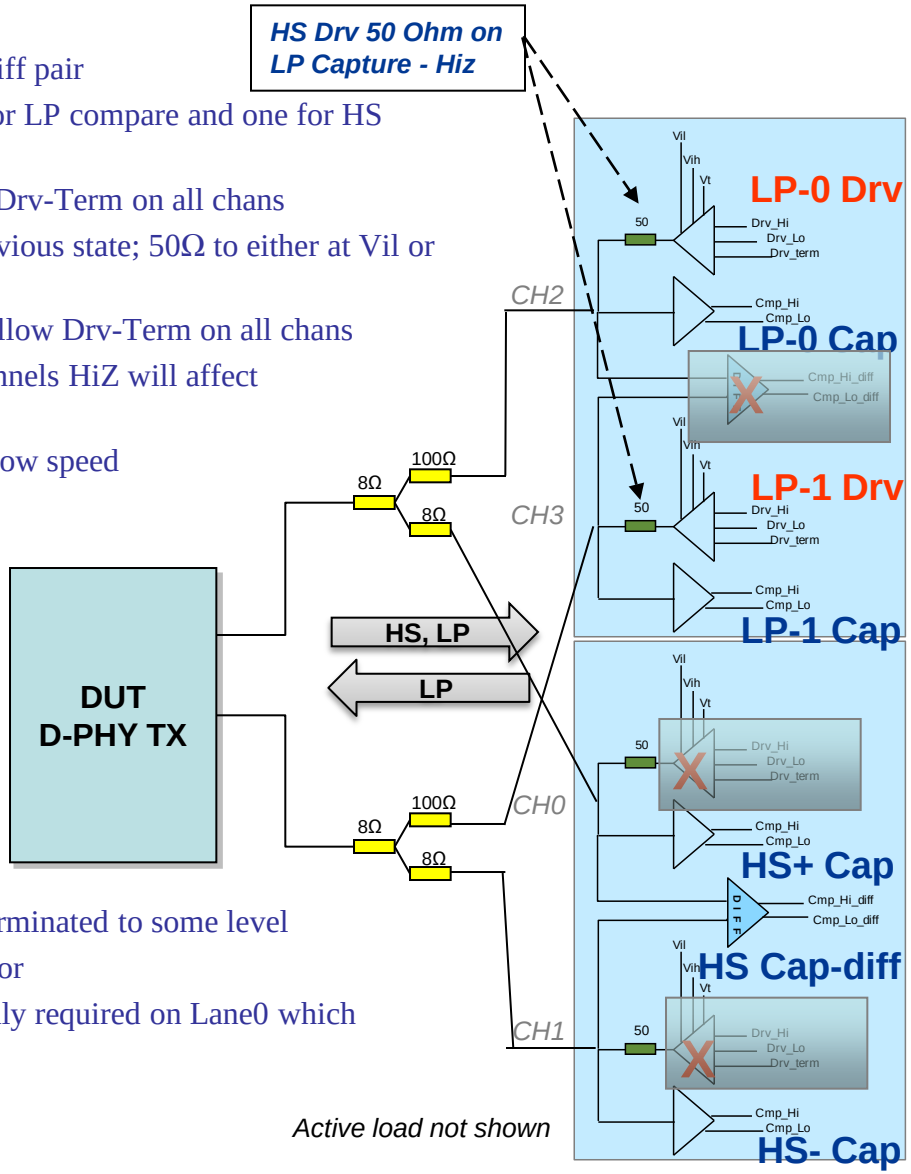
D-PHY Tx

HS modified Vt/Vcomp, LP HiZ

- 4 digital channels per diff pair
- Use 2 Time Sets; one for LP compare and one for HS compare
  - 1. (HS) that allows Drv-Term on all chans
    - PE stays in previous state; 50Ω to either at Vil or Vih
  - 2. (LP) does NOT allow Drv-Term on all chans
- LP receive with all channels HiZ will affect signal integrity
  - Expect ok as LP is low speed
- HS receive is doubly terminated to some level
  - Use DIFF comparator
  - Resistor network only required on Lane0 which supports LP traffic



	MODE			
Device	HS Drv	HS Rcv	LP Drv	LP Rcv
Tester	*HS Rcv*	*HS Drv*	*LP Rcv*	*LP Drv*
D-PHY Tx	Y	-	Y	Y
DSI	Y	-	Y	Y

	Param	Programmed	Use
Chan 0,1 (HS)	Vil		HS Vt
	Vih		HS Vt
	Vt	-	-
	Vol		HS Vol
	Voh		HS Voh
	PE Mode	LargeSwing-HiZ	-
Chan 2,3 (LP)	Vil	0V	LP Vil
	Vih	1.2V	LP Vih
	Vt	-	-
	Vol	550mV	LP Vol
	Voh	880mV	LP Voh
	PE Mode	LargeSwing-HiZ	-

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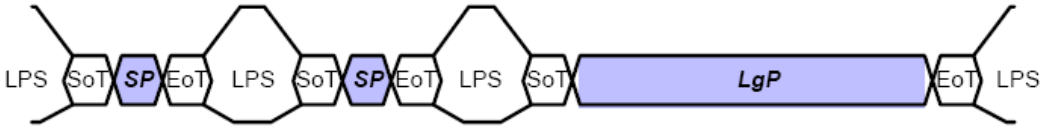
State Transitions & Non-Determinism

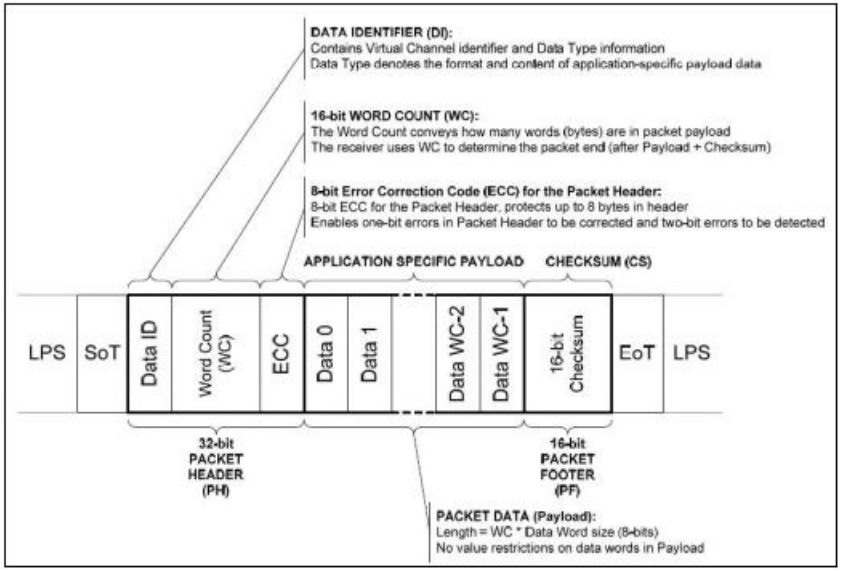


Separate Transmissions

KEY:

LPS	– Low Power State	SP	– Short Packet
SoT	– Start of Transmission	LgP	– Long Packet
EoT	– End of Transmission		

- In "mission-mode"
  - HS packets are separated by LP commands
  - HS packet lengths vary



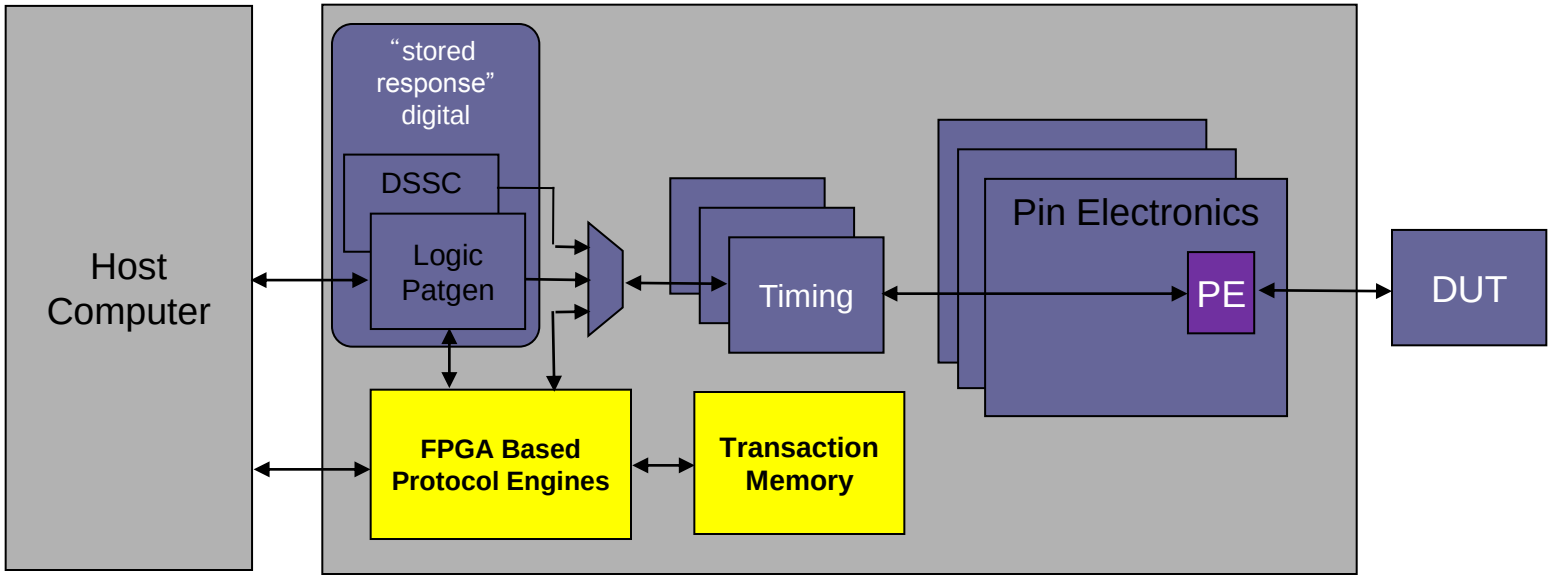
LgP Structure

Standard Digital (no PA)

*Mode switches between HS/LP modes must be deterministic in:
- Order
- Time

*Packet lengths must be deterministic

Handling Non-Determinism
With UP1100PA

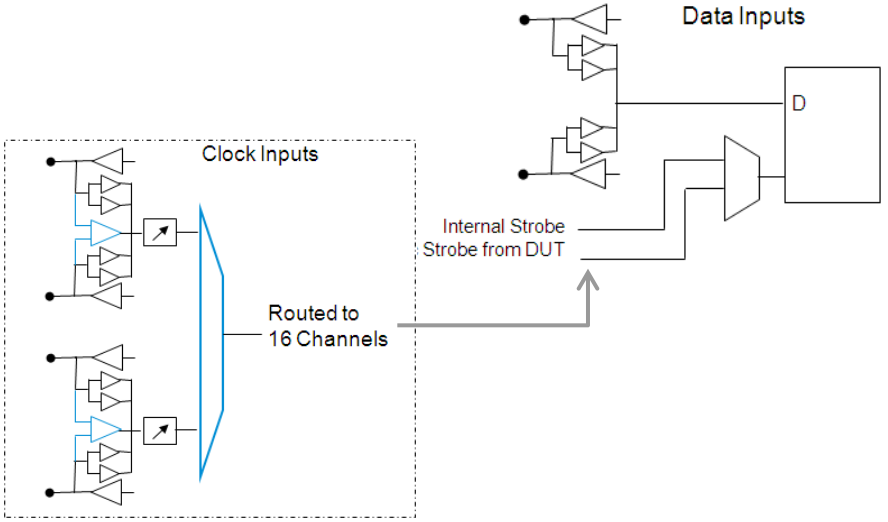


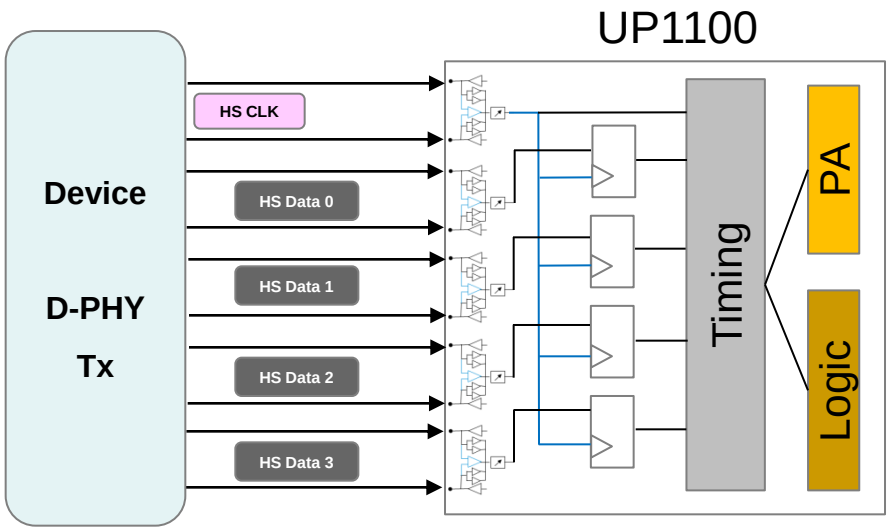
- PA in UP1100 could automatically handle the timing non-determinism
  - The **order** of packets and HS/LP transitions must still be deterministic
  - Less DFT required
  - More coverage testing near mission-mode

Source-Sync Timing Measurement of Device HS Tx With UP1100PA

UP1100 has hardware source-sync capability behind the digital pins

- 4 of Each 16 pin block have source sync capability
- Each Source Sync Input can be SE or Differential
- Each Source Sync Input has local adjust capability for fast edge searches
- Data Channels use internal Strobe or Source Sync Strobe
- Src Sync Clock to Data pin Accuracy +/100ps





** Real-time AC parametric measurements:

→**1 burst for accurate timing measurement compared to many burst iterations for software-based solutions**

** Supports both PA and standard logic testing

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Conclusions

- D-PHY mode switching within a burst creates unique test challenges
  - UltraFLEX digital solutions solve these challenges with flexible timing and pin electronics
- UP1100 Option adds unique capability to improve test coverage
  - More “mission-mode” testing allowed by PA handling non-determinism
  - Hardware Source-Synchronous feature allows real-time AC parametric timing measurements

Appendix A

- LP signal timing parameters-1

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{CLK-MISS}$	Detection time that the clock has stopped toggling			60	ns	1
$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60 ns + 52*UI			ns	
$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8			UI	
$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS clock transmission	38		95	ns	
$T_{CLK-TERM-EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL,MAX}$	Time for Dn to reach $V_{TERM-EN}$		38	ns	
$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			ns	
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock	300			ns	
$T_{D-TERM-EN}$	Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35 ns + 4*UI		
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state			105 ns + n*12*UI		3
$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			ns	

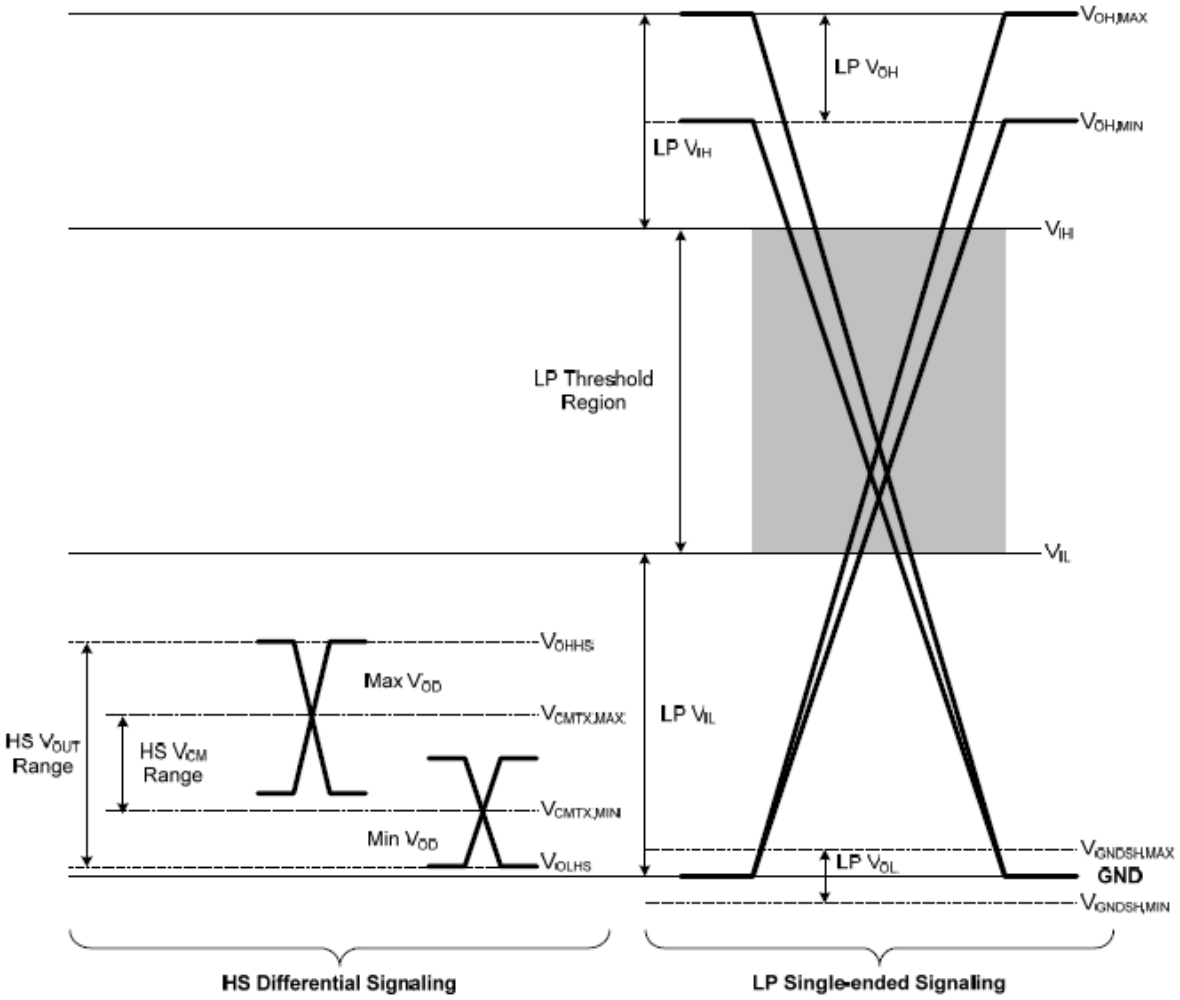
Appendix B

- LP signal timing parameters-2

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns	
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145 ns + 10*UI			ns	
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40		55 ns + 4*UI	ns	
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60 ns + n*4*UI)			ns	2, 3
T_{INIT}	Initialization period (PHY might calibrate)	100			µs	
T_{LPX}	Length of any Low-Power state period	50			ns	4
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2		
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$			ns	
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPX}$			ns	
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}		$2*T_{LPX}$	ns	
T_{WAKEUP}	Recovery time from Ultra-Low Power State	1			ms	

Appendix C

- D-PHY Signal Level



Appendix D

- HS Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{CMTX}	HS transmit static common-mode voltage	150	200	250	mV	1
$\lvert\Delta V_{CMTX(1,0)}\rvert$	V_{CMTX} mismatch when output is Differential-1 or Differential-0			5	mV	2
$\lvert V_{OD}\rvert$	HS transmit differential voltage	140	200	270	mV	1
$\lvert\Delta V_{OD}\rvert$	V_{OD} mismatch when output is Differential-1 or Differential-0			10	mV	2
V_{OHHS}	HS output high voltage			360	mV	1
Z_{OS}	Single ended output impedance	40	50	62.5	Ω	
ΔZ_{OS}	Single ended output impedance mismatch			10	%	

Appendix E

- HS Transmitter AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMTX(HF)}$	Common-level variations above 450MHz			15	mV_{RMS}	
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450MHz			25	mV_{PEAK}	
t_R and t_F	20%-80% rise time and fall time			0.3	UI	1
		150			ps	

Appendix F

- LP Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	
V_{OL}	Thevenin output low level	-50		50	mV	
Z_{OLP}	Output impedance of LP transmitter	110			Ω	1, 2

Appendix G

- LP Transmitter AC Specifications

Parameter	Description		Min	Nom	Max	Units	Notes
T_{RLP}/T_{FLP}	15%-85% rise time and fall time				25	ns	1
T_{REOT}	30%-85% rise time and fall time				35	ns	1, 5, 6
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40			ns	4
		All other pulses	20			ns	4
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock		90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0pF		30		500	mV/ns	1, 2, 3, 7
	Slew rate @ C_{LOAD} = 5pF		30		200	mV/ns	1, 2, 3, 7
	Slew rate @ C_{LOAD} = 20pF		30		150	mV/ns	1, 2, 3, 7
	Slew rate @ C_{LOAD} = 70pF		30		100	mV/ns	1, 2, 3, 7
C_{LOAD}	Load capacitance		0		70	pF	1

Appendix H

- HS Receiver DC Specifications

Parameter	Description	Min	Nom	Max	Units	Note
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70		330	mV	1,2
V_{IDTH}	Differential input high threshold			70	mV	
V_{IDTL}	Differential input low threshold	-70			mV	
V_{IHHS}	Single-ended input high voltage			460	mV	1
V_{ILHS}	Single-ended input low voltage	-40			mV	1
$V_{TERM-EN}$	Single-ended threshold for HS termination enable			450	mV	
Z_{ID}	Differential input impedance	80	100	125	Ω	

Appendix I

- HS Receiver AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450 MHz			100	mV	2
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz – 450MHz	-50		50	mV	1, 4
C_{CM}	Common-mode termination			60	pF	3

Appendix J

- LP Receiver DC and AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IH}	Logic 1 input voltage	880			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
V_{HYST}	Input hysteresis	25			mV	

Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V·ps	1, 2, 3
T_{MIN-RX}	Minimum pulse width response	20			ns	4
V_{INT}	Peak interference amplitude			200	mV	
f_{INT}	Interference frequency	450			MHz	

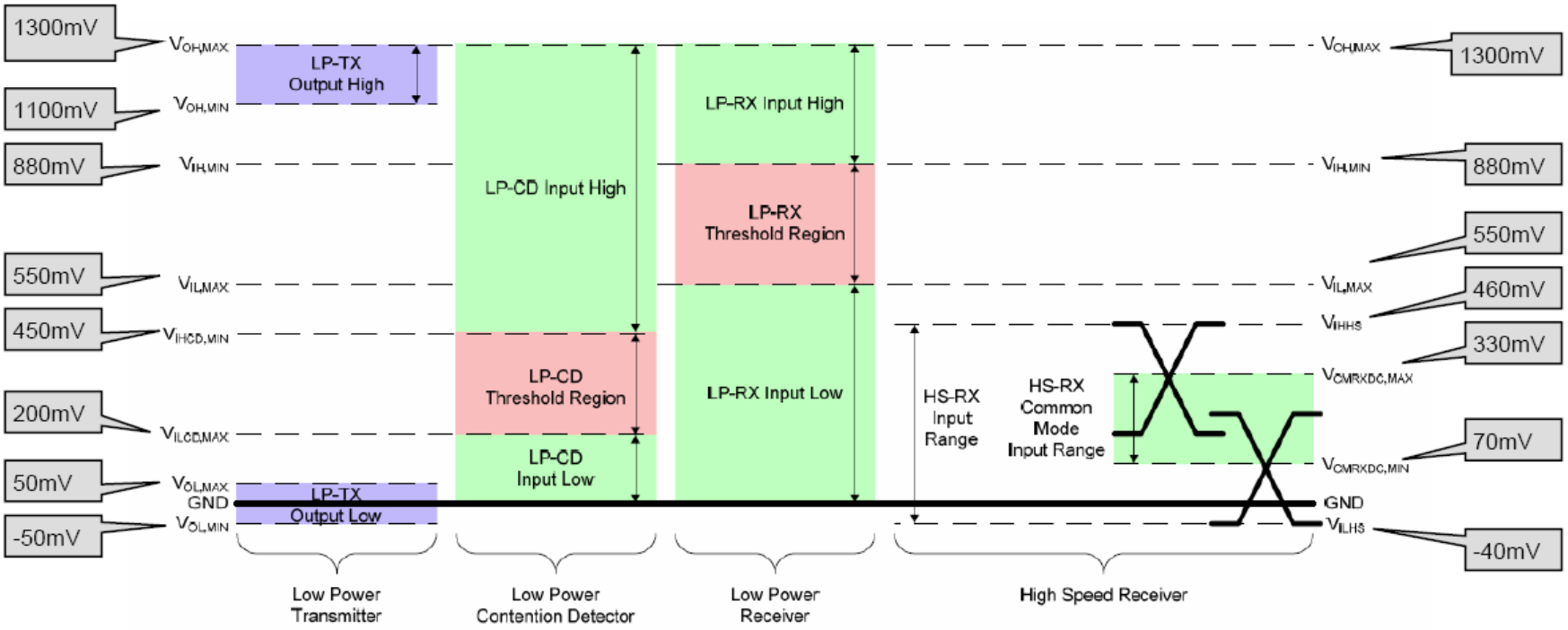
Appendix K

- LP Transmitter AC Specifications

Parameter	Description		Min	Nom	Max	Units	Notes
T_{RLP}/T_{FLP}	15%-85% rise time and fall time				25	ns	1
T_{REOT}	30%-85% rise time and fall time				35	ns	1, 5, 6
$T_{LP-PULSE-TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40			ns	4
		All other pulses	20			ns	4
$T_{LP-PER-TX}$	Period of the LP exclusive-OR clock		90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0pF		30		500	mV/ns	1, 2, 3, 7
	Slew rate @ C_{LOAD} = 5pF		30		200	mV/ns	1, 2, 3, 7
	Slew rate @ C_{LOAD} = 20pF		30		150	mV/ns	1, 2, 3, 7
	Slew rate @ C_{LOAD} = 70pF		30		100	mV/ns	1, 2, 3, 7
C_{LOAD}	Load capacitance		0		70	pF	1

MIPI D-PHY Interface Source and Capture Voltage Levels

Appendix L



max Differential input high threshold V_{IDTH} = 70mV
min Differential input low threshold V_{IDTL}=-70mV

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