MIPI Alliance Specification for M-PHY^{SM}

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Further technical changes to this document are expected as work continues in the PHY Working Group

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Release History

Date	Release	Description
2008-08-29	v0.10.00	• Initial release
2008-09-19	v0.20.00	• First JEDEC release
2008-11-25	v0.30.00	• Second JEDEC release
2009-02-05	v0.70.00	• Third JEDEC release
2009-09-11	v0.71.00	• WG voting release
2009-12-29	v0.80.00 r0.01	• WG voting release
2010-03-29	v0.80.00 r0.02	• Interim release for WG review
2010-04-08	v0.80.00 r0.03	• Release for Second Draft Review
2010-04-12	v0.80.00 r0.04	• Release for Second Draft Review after WG review
2010-04-27	v0.80.00 r0.05	• Release for Second Draft Review after input from Board.
2010-04-28	v0.80.00 r0.08	• Release for Second Draft Review after input from Board and WG.
2010-05-01	v0.80.00 r0.07	• Release for Second Draft Review after input from Board and WG.
2010-08-13	v0.80.00	• Board approved release.

1 Introduction

1 This document describes a serial interface technology with high bandwidth capabilities, which is particularly developed for mobile applications to obtain low pin count combined with very good power efficiency. It is targeted to be suitable for multiple protocols, including UniPro^{SM} and DigRF^{SM} v4, and for a wide range of applications.

2 The M-PHY specification features the following aspects:

- BURST mode operation for improved power efficiency
- Multiple transmission modes with different bit-signaling and clocking schemes intended for different bandwidth ranges to enable better power efficiency over a huge range of data rates
- Multiple transmission speed ranges/rates per BURST mode to further scale bandwidth to application needs and for mitigation of interference problems. Rates for high-speed mode are fixed, for low-speed modes they are flexible within ranges
- Multiple power saving modes, where power consumption can be traded-off against recovery time
- Symbol coding (8b10b) for spectral conditioning, clock recovery, and in-band control options for both PHY and Protocol level.
- Clocking flexibility: designed to be able to operate with independent local reference clocks at each side, but suitable to exploit the benefits of a shared reference clock
- Optical friendly: enables low-complexity electro-optical signal conversion and optical data transport inside the interconnect between MODULEs
- Distance: optimized for short interconnect (<10 cm) but extendable to a meter with good quality interconnect or even further with optical converters and optical waveguides.
- Configurability: differences in supported functionality (to reduce cost) and tune for best performance (implementation) without hampering interoperability

1.1 Scope

12 This document specifies unidirectional LANEs and its individual parts, as building blocks for composition of a dual-simplex LINK by application protocols. An M-PHY implementation allows one or more LANEs in each direction, allows differences in optional funtionality between LANEs, allows different momentary operating modes between LANEs, and allows asymmetry in amount of LANEs and LANE properties for the two directions of the dual-simplex LINK. Protocols applying M-PHY technology may have different LANE constraints and choose different operation control and data striping/merging solutions. Therefore, this document provides the features to enable LINK composition, but does not specify how multiple transmitters and receivers are combined into a PHY-unit for a certain LINK composition. Each LANE has its own interface to the Protocol Layer.

13 MODULEs can disclose their capabilities and do contain several configurable parameters in order to allow differentiation on supported functionality and tune for best performance without hampering interoperability. Therefore, protocols need to support some configuration mechanism to determine and define the operational settings. Most flexible is an auto-discovery negotiation protocol to determine the commonly-supported settings of the Physical Layer which are most desirable for running the application. M-PHY supports this, but does not include the configuration protocol itself. Alternatively, the protocol may directly program the required settings if there is predetermined higher system knowledge about which MODULEs are present at both ends of that LINK.

14 The M-PHY specification shall always be used in combination with a higher layer MIPI specification that references this specification. Any other use of the M-PHY specification is strictly prohibited, unless approved in advance by the MIPI Board of Directors.

1.2 Purpose

Mobile devices face increasing bandwidth demands for each of its functions as well as an increase of the number of functions integrated into the system. This requires wide bandwidth, low-pin count (serial) and highly power-efficient (network) interfaces that provides sufficient flexibility to be attractive for multiple applications, but which can also be covered with one physical layer technology. M-PHY is the successor of D-PHY, requiring less pins and providing more bandwidth per pin (pair) with improved power efficiency.

2 Terminology

16 The MIPI Alliance has adopted Section 13.1 of the IEEE Specifications Style Manual, which dictates use of the words “shall”, “should”, “may”, and “can” in the development of documentation, as follows:

17 The word *shall* is used to indicate mandatory requirements strictly to be followed in order to conform to the Specification and from which no deviation is permitted (*shall* equals *is required to*).

18 The use of the word *must* is deprecated and shall not be used when stating mandatory requirements; *must* is used only to describe unavoidable situations.

19 The use of the word *will* is deprecated and shall not be used when stating mandatory requirements; *will* is only used in statements of fact.

20 The word *should* is used to indicate that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (*should* equals *is recommended that*).

21 The word *may* is used to indicate a course of action permissible within the limits of the Specification (*may* equals *is permitted*).

22 The word *can* is used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

23 All sections are normative, unless they are explicitly indicated to be informative.

2.1 Definitions

24 BURST Sequence of 8b10b encoded data transmission delimited by and including a HEAD-OF-BURST and TAIL-OF-BURST.

25 COMMA Non-data symbol which can not be found at any bit position within any combination of other valid symbols.

26 DIF-N Logical LINE state, driven by the M-TX, corresponding with a negative differential LINE voltage. Voltage levels and signal transition timing specifications for the M-TX as well as detection requirements for the M-RX are defined in Section 5.

27 DIF-P Logical LINE state, driven by the M-TX, corresponding with a positive differential LINE voltage. Voltage levels and signal transition timing specifications for the M-TX as well as detection requirement for the M-RX are defined in Section 5.

28 DIF-Q LINE state when the M-RX can be high-impedance resulting in undriven lines with an undefined LINE state.

29 DIF-X Indication that LINE state can be either DIF-P or DIF-N, but nothing else.

30 DIF-Z Logical LINE state, driven by the M-RX, corresponding with almost zero differential LINE voltage. Voltage levels and signal transition timing specifications for M-TX and M-RX are defined in Section 5.

31 DISABLED MODULE state when the MODULE is powered, but not enabled.

32 FILLER Non-data symbol(s) inserted when no data is provided by the protocol during a BURST.

33 FLAG Control signal that indicates the occurrence of a certain event.

34 FRAME Series of symbols separated by MARKERs.

35 GEAR Speed range (PWM) or fixed RATEs (HS) of communication in LS or HS mode. Each HS GEAR includes two RATEs which differ about 15% for mitigation of EMI.

36 HEAD-OF-BURST
Period between exiting STALL state or SLEEP state until the first MARKER0 in a BURST, indicating start of PAYLOAD data.

37 HIBERN8 Deepest low-power state without loss of configuration information.

38 HS-BURST High speed state including PREPARE, SYNC, MARKERs, and data.

39 HS-GEAR GEAR in HS-MODE.

40 HS-MODE High-Speed operation loop consisting of STALL and HS-BURST.

41 LANE A LANE is a unidirectional point-to-point differential serial connection, consisting of an M-PHY transmit MODULE (M-TX), an M-PHY receive MODULE (M-RX), and a LINE.

42 LINE Differential point-to-point interconnect between the PINs of M-TX and M-RX. The interconnect may include optical media converters and optical waveguide.

43 LINE-CFG LANE state to exchange configuration parameters with Media Converters

44 LINE-INIT LINE-CFG sub-state before transmission of an LCC.

45 LINE-RESET
Reset via the LINE by means of the exceptional signal condition of a long DIF-P.

46 LINK One or more PHY LANEs in each direction plus an additional LANE management layer that provides a bidirectional data transport means, agnostic to the actual LANE composition.

47 LS-BURST Low speed state including PREPARE, MARKERs, and data.

48 LS-MODE Type-I: Combination of SLEEP, PWM-BURST, INIT, and LINE-CFG states.
Type-II: Combination of SLEEP and SYS-BURST states.

49 MARKER Non-data symbol, used for protocol related control purposes.

50 MODE Indicates either HS-MODE or LS-MODE.

51 MODULE Indication for either an M-TX or M-RX.

52 M-PORT Combination of MODULEs at one side of a LINK.

53 PAYLOAD BURST without HOB and TOB. PAYLOAD may consist of multiple FRAMEs.

54 PIN A point of external physical electrical connection for a component. Examples of a “PIN” may include (but are not limited to) a BGA ball, QFP lead, or solder pad.

55 POWERED Any LANE or MODULE state when power supply is available.

56 PREPARE First part of the HOB after exiting STALL or SLEEP up to but not including the SYNC sequence.

57 PWM Bit modulation scheme carrying the data information in the duty-cycle, and explicit clock information in the period.

58 PWM-BURST
Transmission of an LS-BURST in pulse-width modulated bit format and using 8b10b coding.

59 RATE Exact speed of communication in a certain mode in kbps, Mbps, or Gbps.

60 SAVE Set of power saving states STALL, SLEEP, HIBERN8, DISABLED, and UNPOWERED.

SLEEP Power saving state used between LS-BURSTs.

STALL Power saving state between HS-BURSTs with fast recovery time.

SUB-LINK One or more LANES in the same direction as fraction of a LINK.

SYMBOL-INTERVAL
10 UI period for the transmission of one symbol.

SYNC An 8b10b symbol sequence with high edge-density intended for fast phase alignment.

SYS-BURST Transmission of an LS-BURST synchronous at the SysClk rate. Only possible for shared SysClk applications.

TAIL-OF-BURST
End-of-payload MARKER2 plus the period to return and settle to unterminated state.

UNIT-INTERVAL
Nominal length of one bit.

UNPOWERED
MODULE state when the power supply is removed.

2.2 Abbreviations

e.g. For example(Latin: exempli gratia)

i.e. That is (Latin: id est)

2.3 Acronyms

b0, b1 Bit with logical value “0” or “1”, respectively. The signaling format depends on operating MODE. A prefix indicating the MODE is occasionally used for clarification, e.g. PWM-b0.

CFG Configuration

FLR FILLER symbol

FSM Finite State Machine

HOB HEAD-OF-BURST

HS High-Speed

LCC LINE Control Command

LS Low-Speed

LSb Least Significant bit

MC Media Converter

MC-RX Media Converter Receiver

MC-TX Media Converter Transmitter

MIPI Mobile Industry Processor Interface

MK# Short indicator for MARKER symbols

MSb Most Significant bit

M-RX M-PHY electrical Receiver

88	M-TX	M-PHY electrical Transmitter
89	NRZ	Non-Return-to-Zero
90	O-RX	Optical Receiver
91	O-TX	Optical Transmitter
92	PIF	Protocol InterFace
93	PWM	Pulse-Width-Modulation
94	RCT	Re-Configuration Trigger
95	RDS	Running Digital Sum
96	SAP	Service Access Primitive (defining interactions with Protocol Layer)
97	SECDED	Single Error Correction, Double Error Detection
98	SI	Symbol Interval
99	SYS	SYstem-clock Synchronous
100	TOB	TAIL-OF-BURST
101	UI	Unit Interval

3 References

102 [IBM01] Widmer, A. X.; Franaszek, P. A., “A DC-Balanced, Partitioned-Block, 8B/ 10B Transmission Code”, *IBM Journal of Research. Development*, VOL. 27, NO. 5, September 1983

103 [INC01] INCITS/TR-35:2004, *Fibre Channel – Methodologies for Jitter and Signal Quality Specification – MJSQ*, Working Draft, T11.2/ Project 1316-DT/ Rev 14.1, <http://www.t11.org>, InterNational Committee for Information Technology Standards, 5 June 2005

4 Architecture and Operation

104 This section specifies the concept, communication principles, signaling schemes, interface structure and operation of M-PHY interfaces.

4.1 PIN, LINE, LANE, SUB-LINK, LINK, and M-PORT

105 A LANE is a unidirectional, single-signal, physical transmission channel used to transport information from point A to point B. A LANE consists of an M-PHY transmit MODULE (M-TX), an M-PHY receive MODULE (M-RX), and a LINE, which is the point-to-point interconnect between the M-TX and M-RX. An M-TX or M-RX has only one differential electrical output or input LINE interface, respectively, which corresponds with two signaling PINs for each MODULE. The PINs are individually denoted as DP and DN, where DP is defined as the positive node of the differential signal. An optional prefix, TX or RX, can be used to indicate the M-TX or M-RX PINs, respectively. Specifications in this document are defined at the PINs of the M-TX and M-RX, and PINs-to-PINs through the LINE. Figure 1 illustrates the relationship between different parts of an M-PHY LINK.

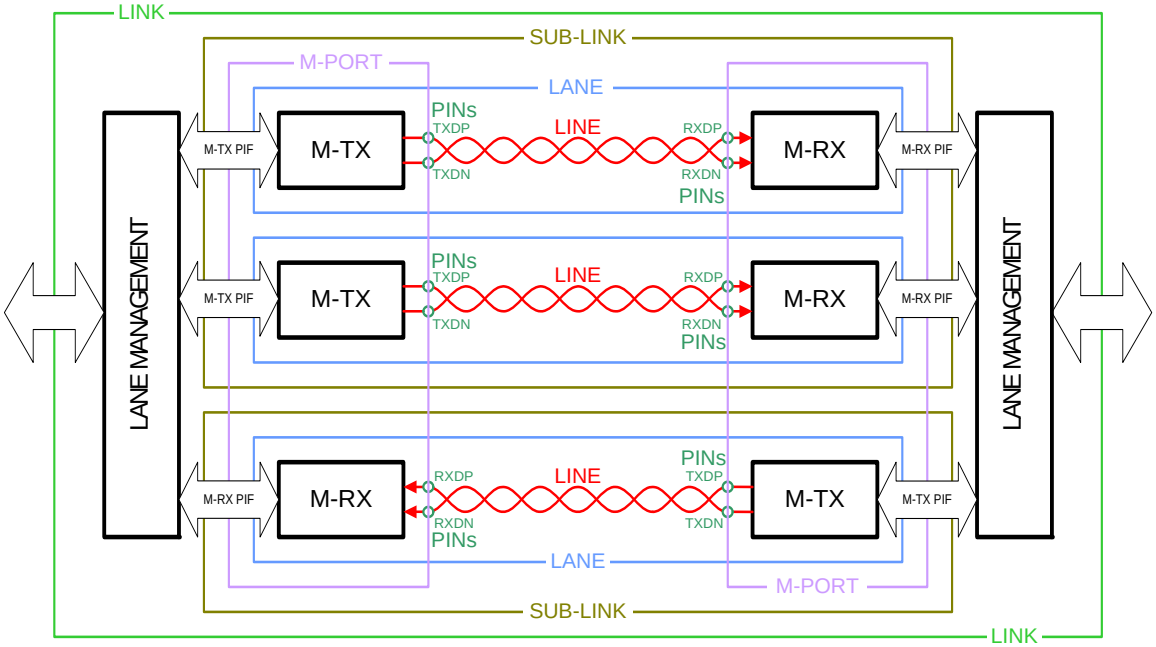


Figure 1 M-PHY Lane Example

106 In the case of a galvanic interconnect, the LINE consists of two differentially-routed wires connecting the LINE interface PINs of the M-TX and M-RX. Typically, these wires are transmission lines. Guidelines for LINE characteristics are described in Section 6. A LINE may contain converters to other transmission media, such as optical fiber. For data transfer purposes, such a LINE might be considered as a black box with end-to-end signal transfer requirements defined at the PINs. Additionally, for advanced configuration functions interaction between MODULEs and Media Converters is supported. Figure 2 shows the setup of a LANE with Media-Converters (MC-TX / MC-RX) in the LINE.

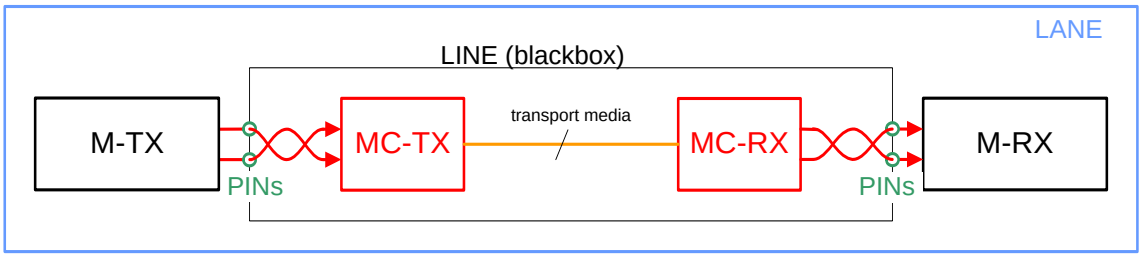


Figure 2 Example LANE Configuration with Media Converter

107 An interface based on M-PHY technology shall contain at least one LANE in each direction. There are no symmetry requirements from an M-PHY perspective for the number of LANEs in each direction.

108 All LANEs in the same direction within a LINK are denoted as a SUB-LINK. Two SUB-LINKs with opposite directions plus additional LANE management, which provides bidirectional data transport functionality agnostic to the actual LANE composition, is called a LINK. A set of M-TXs and M-RXs in a device that compose one interface port is denoted as an M-PORT.

109 This document specifies LANEs and their individual parts including M-TX, M-RX, interconnect, and optionally Media Converters. Furthermore, this specification sets some boundary conditions for M-TX and M-RX inside a single M-PORT, which puts some constraints for the usage of LANEs within SUB-LINKs. This document does not specify the LANE management function in order to allow maximum flexibility of LANE exploitation by protocols. Therefore, the composition of LANEs in the two SUB-LINKs and the specification of LANE management, which completes the LINK, is left to protocols applying M-PHY technology.

4.2 LINE States

110 M-PHY technology exploits only differential signaling. a LINE can show the following states:

111 • A positive differential voltage, driven by the M-TX, which is denoted by LINE state DIF-P

112 • A negative differential voltage, driven by the M-TX, which is denoted by LINE state DIF-N

113 • A weak zero differential voltage, maintained by M-RX, which is denoted by LINE state DIF-Z

114 • An unknown, floating LINE voltage, or no LINE drive, which is denoted by LINE state DIF-Q

115 Table 1 list all possible LINE conditions with the resulting LINE state

Table 1 LINE Conditions and Resulting LINE States

Differential LINE Voltage	M-TX Output Impedance	M-RX Input Impedance	LINE State Set by	LINE State Name
Positive	Low	Any	M-TX	DIF-P
Negative	Low	Any	M-TX	DIF-N
Zero	High	Medium	M-RX	DIF-Z
Unknown or floating	High	High	None	DIF-Q

116 For data transmission, only DIF-P and DIF-N are exploited. DIF-Z can only occur during power-up and power-saving states. DIF-Q can only occur when the M-RX is not powered. DIF-X is used as an alias to denote that the LINE state can be either DIF-P or DIF-N.

117 The transition point between DIF-Z and DIF-N is defined by the squelch threshold level, which is positioned between the DIF-N and DIF-Z electrical LINE levels (Section 5.2.6).The transition point between DIF-P and DIF-N is defined at the zero crossing of the differential signal.

4.2.1 Termination Scheme

118 An M-TX shall terminate both wires in the LINE with a characteristic impedance R_{SE_TX} during any DIF-P or DIF-N state, both differentially as well as common-mode with respect to ground. The M-TX can have a larger resistance during SLEEP and STALL as described in Section 5.1.1.3 as $R_{SE\_PO\_TX}$

119 An M-RX does not always terminate the LINE, but certain options such as HS-MODE require support for terminated operation. Therefore, an M-RX including these options shall include a switchable differential LINE termination.

120 The M-RX termination condition are optionally indicated in the electrical parameter and LINE state name by a subscript RT (Resistively Terminated) or NT (Not Terminated). For example, DIF-P_{RT} is a DIF-P state with receiver termination enabled.

121 Figure 3 shows an example of a LINE termination scheme. The electrical characteristics of LINE states and terminations are specified in Section 5.

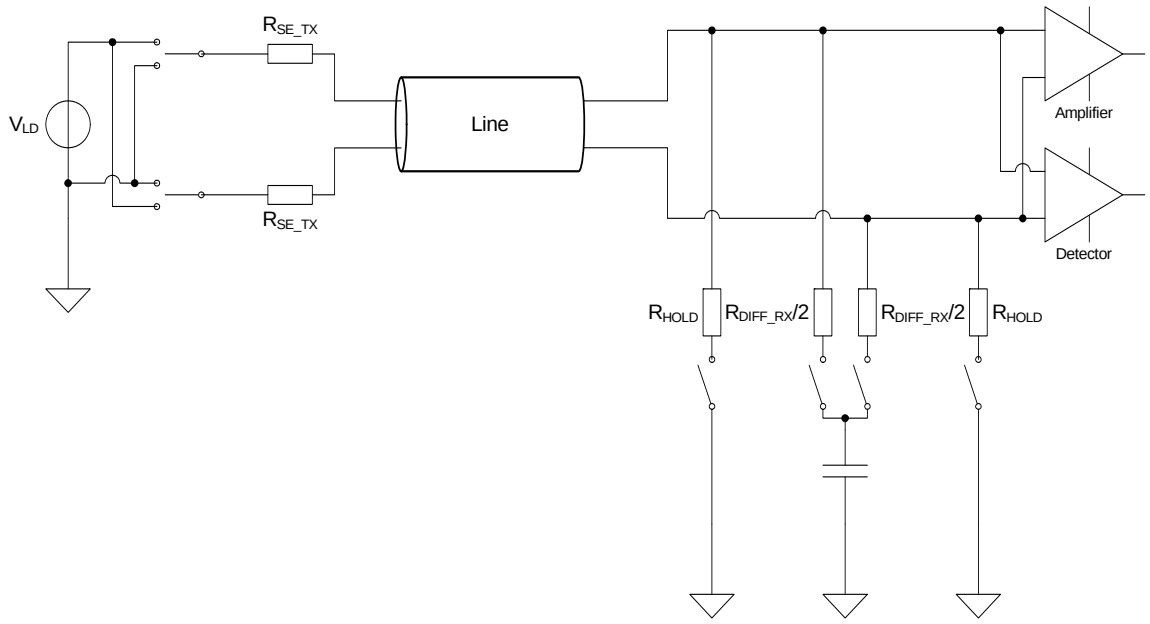


Figure 3 Example I/O Termination

4.2.2 Signal Amplitudes

122 All communication is based on low-swing, DC-coupled, differential signaling. The LINE driver in an M-TX may support two drive strengths, resulting in different signal amplitudes. Large Amplitude (LA) is about 400 mV_{PK_NT} (and roughly 200 mV_{PK_RT}), while the Small Amplitude (SA) is about 240 mV_{PK_NT} (and roughly 120 mV_{PK_RT}). Detailed electrical level specifications are provided in Section 5. Drivers can support either one of these two, or both, amplitudes. If both amplitudes are supported, Large Amplitude shall be the default configuration setting. An M-RX is able to receive both amplitudes if an appropriate interconnect is used according to the guidelines in Section 6. Signal amplitudes are optionally indicated in parameter names by an “LA” or an “SA” subscript.

4.3 Signaling Schemes

123 M-PHY technology exploits two different signaling schemes for transmission of bits, which are conceptually described in the following sections. Detailed parameter value specifications are provided in Section 5.

4.3.1 Non-Return-to-Zero (NRZ)

124 For NRZ, each bit is represented by a period of either DIF-P or DIF-N, corresponding to a binary one or a binary zero, respectively. All bits are directly concatenated and have equal length.

4.3.2 Pulse Width Modulation

125 The Pulse Width Modulation (PWM) scheme has self-clocking properties. Each bit consists of a combination of two sub-phases, a DIF-N followed by a DIF-P. One of the two sub-phases is longer than the other: $T_{PWM\_MAJOR} > T_{PWM\_MINOR}$, depending upon whether a binary one, or binary zero is being sent. The binary information is in the ratio of the duration of the DIF-N and DIF-P states. If the LINE state is DIF-P for the majority of the bit period, the bit is a binary one (PWM-b1). If the LINE state is DIF-N for the majority of the bit period, the bit is a binary zero (PWM-b0).

126 Each bit period contains two edges, where the falling edge is at a fixed position and the rising edge position is modulated. This means that the PWM bit stream explicitly contains a bit clock with period T_{PWM}, which equals the duration of one bit. T_{PWM} may vary from bit to bit during a transmission, except in LINE-CFG. The bit waveforms for this signaling technique are shown in Figure 4.

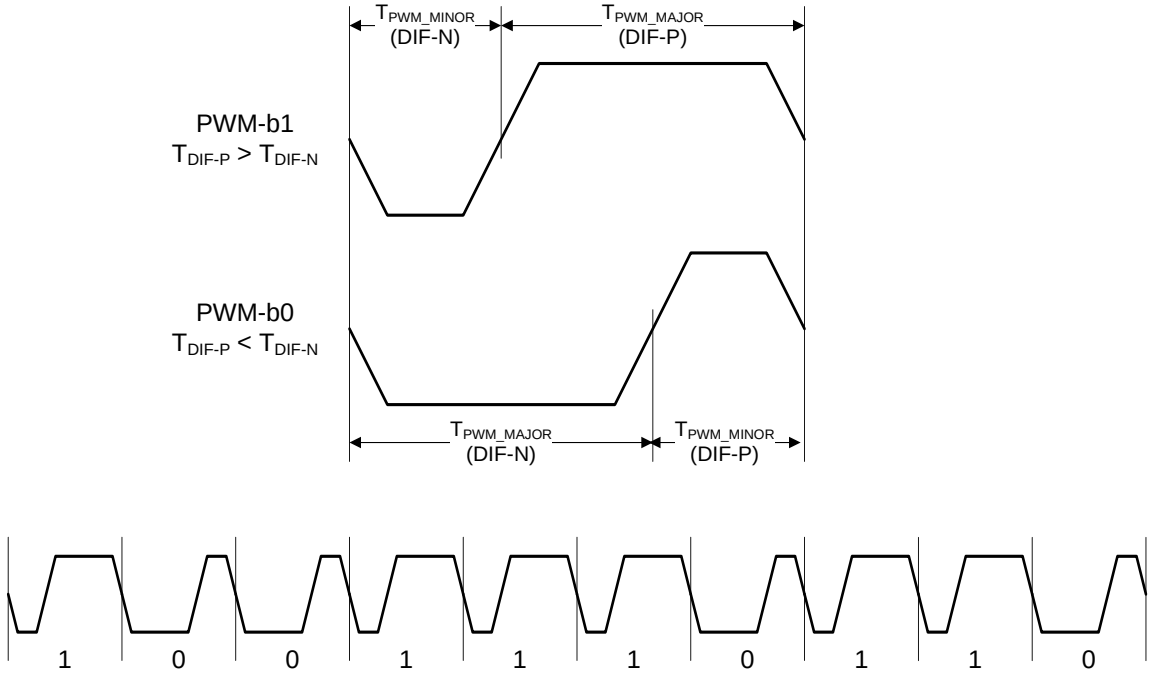


Figure 4 PWM Bit Waveforms and Bit Stream Example

127 M-PHY technology utilizes PWM signaling with FIXED-RATIO and FIXED-MINOR format. For the FIXED-RATIO format, the durations of T_{PWM_MAJOR} and T_{PWM_MINOR} are ideally two-thirds and one-third of the bit period, respectively. For the FIXED-MINOR format, the duration of T_{PWM_MINOR} is specified as an absolute time duration, while T_{PWM_MAJOR} scales with the bit period. The latter format is utilized for very low baud rates (PWM-G0).

4.4 Overview of Concept, Features, and Options

128 This document encompasses the full specification of LANEs, including transmitters (M-TX) and receivers (M-RX), and interconnect (LINE), to support the required set of data transmission, power saving, and control states. Furthermore, this document defines some constraints on options and operation between transmitter and receiver MODULEs within a single M-PORT.

129 A MODULE is specified by the characteristics that can be observed on its PINs. Therefore, M-TX and M-RX operation is fully characterized by the sequence of LINE states. All allowed sequences of LINE states are structured into MODULE states and modes, which are specified by means of state machines in subsequent sections. Detailed electrical characteristics of a MODULE are covered in Section 5.

130 Data transfer occurs in BURSTs, which can be either in High-Speed mode (HS-MODE) or Low-Speed mode (LS-MODE).

131 There are two fundamentally different types of MODULEs, denoted as Type-I and Type-II, depending on the signaling scheme used in LS-MODE. A Type-I MODULE employs PWM signaling, while a Type-II MODULE uses system-clock synchronous, NRZ signaling (denoted by “SYS”). This implies differences in the sequence of LINE states and state machines for an M-TX and an M-RX, as well as in the LINE performance constraints. Therefore, PWM and SYS signaling are mutually exclusive, and only one of the two signaling schemes shall be selected for an application. Note that a Type-II MODULE requires a shared reference clock between the two ends of the LINE. A Type-I MODULE shall be able to operate with independent local clock references on each side of the LINK (plesiochronous operation). Although a Type-I MODULE does not require a shared clock reference, it may exploit the benefits of a shared reference clock if available. A LANE with Type-I MODULEs allows for media converters in the LINE. Note that Type-I and Type-II MODULEs are not interoperable. However, implementations may support both types of MODULEs in order to enable hardware reuse.

132 All MODULEs in an M-PORT shall support LS-MODE, utilizing either the PWM or SYS signaling scheme depending on the M-PORT type. For PWM signaling (Type-I), there are multiple GEARs to cover different speed ranges. The default (mandatory) GEAR for Type-I is PWM-G1, ranging from 3 to 9 Mbps. There are six GEARs with incremental 2x higher speed ranges (PWM-G2 to G7), and one GEAR below the default speed range (PWM-G0).

133 MODULE functionality can be optionally expanded with HS-MODE. HS-MODE includes a default GEAR (HS-G1) and two optional GEARs (HS-G2 and HS-G3) at incremental 2x higher rates. Each GEAR includes two baud rates for EMI mitigation reasons, e.g. HS-G1 supports 1.25 Gbps and 1.45 Gbps. For the two M-PORT types, HS-MODEs are functionally equal, and very similar regarding signal specifications. However, they might need to operate with different reference clock conditions (shared-clock versus plesiochronous).

134 Support for an optional GEAR in either HS-MODE or LS-MODE requires support for all GEARs below it, down to the default GEAR of that mode. PWM-G0 is independently optional for Type-I MODULEs.

135 In the default configuration, M-RX shall terminate the LINE in HS-BURST and in all other states shall leave the LINE unterminated. Optionally, HS-BURST may be operated without termination for selected GEARs, while LS-BURST may be operated with termination for selected GEARs. Capabilities and settings for each GEAR are handled by configuration, which is specified in Section 4.8. During power-saving states the M-RX shall leave the LINE unterminated.

136 An M-TX can have two different drive strengths, which implies a large amplitude or a small amplitude on the PINs. An M-TX shall support at least one of the two possible drive strengths. The drive strength setting holds for all operating states simultaneously, so changing it adapts the signaling levels of all LINE states. An M-TX that supports both drive strengths shall use Large Amplitude as the default setting.

137 The different options are depicted in Figure 5, where the selected set of options of every M-TX and M-RX shall map onto a contingent part of the figure. The different types result in two option diagrams (and two state machines) intended for different applications.

138 The functional options like supported modes, GEARs, and I/O settings shall be available for read-out in a capability registry for configuration purposes. In combination with a configuration protocol of a higher level specification, this enables interoperability between M-PORTs of the same type, while allowing operation up to the highest commonly supported GEAR and the most optimal commonly supported settings. This configuration process is conceptually specified in Section 4.8.1.

139 Besides functional options, there are also a number of programmable parameters. These parameters shall not be mandated or defined at a fixed value by the protocol or application specifications. They are meant only for design and performance optimizations. Examples of this are programmable Slew-Rate-Control for HS-MODE and programmable timer intervals to optimize timing for actual LINE length, Media Converters, and PHY hardware capabilities. The complete list of options and programmable parameters can be found in Section 8.2.

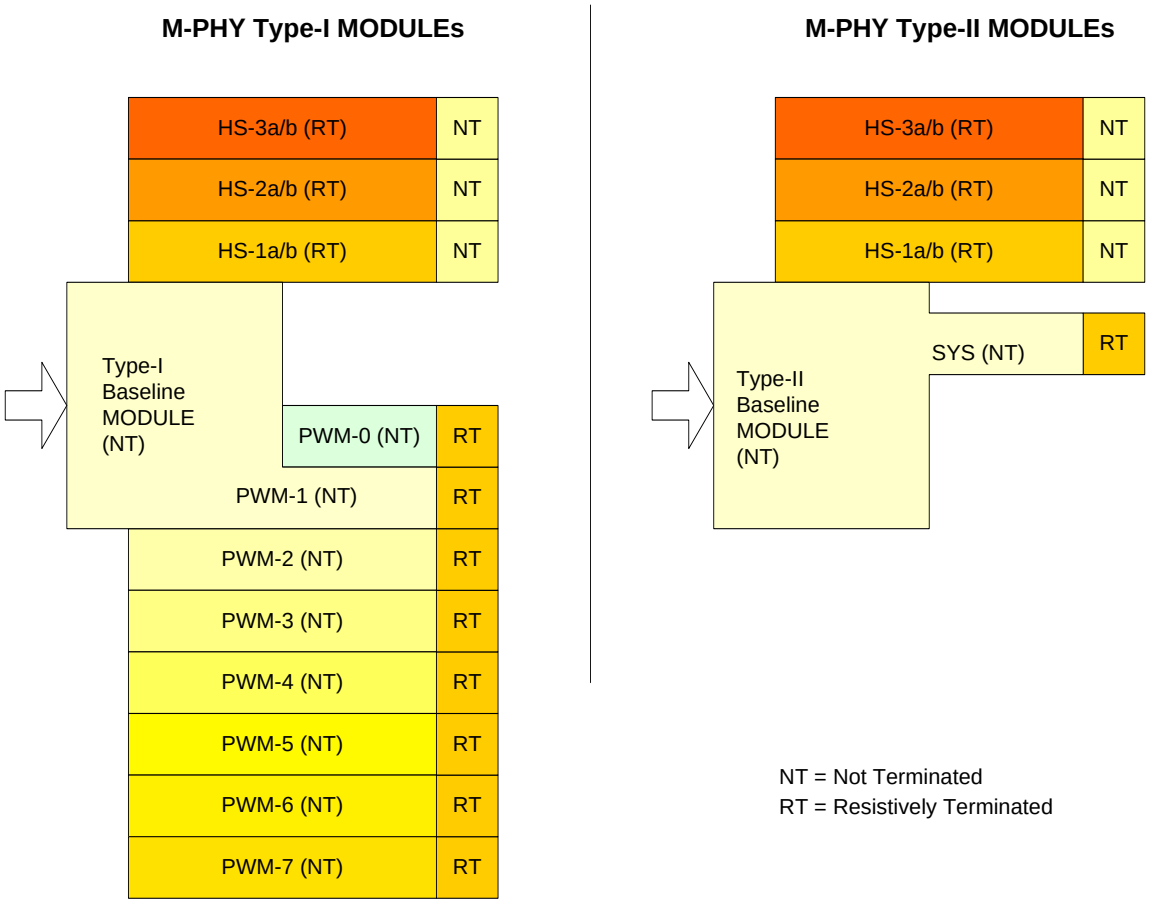


Figure 5 Functional Options for MODULEs in Type-I and Type-II M-PORTs

4.5 Line Coding

140 All information communicated inside BURST states shall be 8b10b encoded according to the data and control symbols assignments prescribed in this section.

4.5.1 Data Symbols

141 The coding of each byte consist of a 5b6b and a 3b4b sub-block encoding. The bits in a data byte are indicated by the capital letters HGFEDCBA. The five data bits “EDCBA” shall encode into a 6-bit sub-block “abcdei”, according to Table 2. The three data bits “HGF” shall encode into the 4-bit sub-block “fghj”, according to Table 3. Several 5b and 3b sub-blocks have two complimentary encoded representations with opposite disparity. The representation with the disparity sign opposite to the running disparity shall be applied for DC balance. For more information on disparity control, see Section 4.5.3.1.

Table 2 5b6b Sub-Block Data Encoding

Input Data		RD = -1	RD = +1	Input Data		RD = -1	RD = +1
Symbol	EDCBA	abcdei		Symbol	EDCBA	abcdei	
D.00	00000	100111	011000	D.16	10000	011011	100100
D.01	00001	011101	100010	D.17	10001	100011	
D.02	00010	101101	010010	D.18	10010	010011	
D.03	00011	110001		D.19	10011	110010	
D.04	00100	110101	001010	D.20	10100	001011	
D.05	00101	101001		D.21	10101	101010	
D.06	00110	011001		D.22	10110	011010	
D.07	00111	111000	000111	D/K.23	10111	111010	000101
D.08	01000	111001	000110	D.24	11000	110011	001100
D.09	01001	100101		D.25	11001	100110	
D.10	01010	010101		D.26	11010	010110	
D.11	01011	110100		D/K.27	11011	110110	001001
D.12	01100	001101		D.28	11100	001110	
D.13	01101	101100		K.28	11100	001111	110000
D.14	01110	011100		D/K.29	11101	101110	010001
D.15	01111	010111	101000	D/K.30	11110	011110	100001
				D.31	11111	101011	010100

Table 3 3b4b Sub-Block Data Encoding

Input		RD^3 = -1	RD^3 = +1	Input		RD^3 = -1	RD^3 = +1
Symbol	HGF	$fghj^3$		Symbol	HGF	fghj	
D.x.0	000	1011	0100	K.x.0	000	1011	0100
D.x.1	001	1001		K.x.1[2]	001	0110	1001

Table 3 3b4b Sub-Block Data Encoding (continued)

Input		$RD^3 = -1$	$RD^3 = +1$	Input		$RD^3 = -1$	$RD^3 = +1$
Symbol	**HGF**	**fghj**[3]		**Symbol**	**HGF**	**fghj**	
D.x.2	010	0101		K.x.2[2]	010	1010	0101
D.x.3	011	1100	0011	K.x.3	011	1100	0011
D.x.4	100	1101	0010	K.x.4	100	1101	0010
D.x.5	101	1010		K.x.5[2]	101	0101	1010
D.x.6	110	0110		K.x.6[2]	110	1001	0110
D.x.P7[1]	111	1110	0001				
D.x.A7[1]	111	0111	1000	K.x.7[1,2]	111	0111	1000

1. *For D.x.7 there is a Primary (D.x.P7) and an Alternate (D.x.A7) coding. The Alternate encoding shall be selected if the Primary coding combined with the preceding 5b/6b code results in five or more consecutive zeroes or ones. Sequences of five identical bits are only used in comma codes for synchronization issues. This implies that D.x.A7 shall only be used for x=17, x=18, and x=20 when RD=-1 and for x=11, x=13, and x=14 when RD=+1. With x=23, x=27, x=29, and x=30, the Alternate code represents the control codes K.x.7. Any other x.A7 code can't be used as it would result in chances for misaligned comma sequences.*
2. *The alternate encoding for the K.x.y codes with disparity 0 allow for K.28.1, K.28.5, and K.28.7 to be "comma" codes that contain a bit sequence that can't be found elsewhere in the data stream.*
3. *For selection of the correct 3b4b sub-block representation, the RD shall be evaluated including the preceding 5b6b sub-block, which is part of the same symbol*

4.5.2 Control Symbols

142 Control symbols are special symbols that do not occur in the data symbol set, that can be used for embedded control features during BURSTs. Table 4 lists all control codes of the 8b10b code set. M-PHY technology exploits four control codes, namely K28.1, K28.3, K28.5, and K28.6. Their functions are briefly mentioned in the table. Symbol K28.5 has comma properties, and shall be detected anywhere in the bitstream for symbol alignment. Details on usage of the codes can be found in Section 4.7. The remaining eight control codes are reserved and shall not be used in M-PORTs

Table 4 Control Symbols

Input		RD = -1	RD = +1	Name	Function
Symbol	**HGF EDCBA**	**abcdei fghj**	**abcdei fghj**		
K.28.0	000 11100	001111 0100	110000 1011	Reserved	
K.28.1[1]	001 11100	001111 1001	110000 0110	FILLER	NOP
K.28.2	010 11100	001111 0101	110000 1010	Reserved	
K.28.3	011 11100	001111 0011	110000 1100	MARKER1	Protocol Separator
K.28.4	100 11100	001111 0010	110000 1101	Reserved	

Table 4 Control Symbols (continued)

Input		RD = -1	RD = +1	Name	Function
Symbol	**HGF EDCBA**	**abcdei fghj**	**abcdei fghj**		
K.28.5[1]	101 11100	001111 1010	110000 0101	MARKER0	HEAD-OF-BURST; Start-of-FRAME
K.28.6	110 11100	001111 0110	110000 1001	MARKER2	TAIL-OF-BURST
K.28.7[2]	111 11100	001111 1000	110000 0111	Reserved	
K.23.7	111 10111	111010 1000	000101 0111	Reserved	
K.27.7	111 11011	110110 1000	001001 0111	Reserved	
K.29.7	111 11101	101110 1000	010001 0111	Reserved	
K.30.7	111 11110	011110 1000	100001 0111	Reserved	

1. *Within the control symbols, K.28.1, K.28.5 are comma symbols. Comma symbols are used for synchronization (finding the alignment of the 8b and 10b codes within a bit-stream). K28.7 has also comma properties, but sets constraints on the symbols around it. Because K.28.7 is not used, the unique comma sequences 0011111 or 1100000 cannot be found at any bit position within any combination of normal codes.*
2. *See note 2 for Table 3.*

4.5.3 Running Disparity

143 The applied 8b10b transmission coding is a DC-balanced coding scheme. The Running-Disparity (RD) is the disparity between the number of ones and zeroes in the proceeding part of the BURST, where each one is counted as +1 and each zero is counted as -1. RD tracking is necessary for correct encoding in the M-TX and error checking in the M-RX.

4.5.3.1 RD Characteristics and M-TX Coding Rules

144 In the absence of transmission errors, the RD stays within -3 and +3, while it always equals -1 or +1 at any of the 6b and 4b sub-block boundaries. All sub-blocks have a disparity of 0, -2, or +2. Sub-blocks with non-zero disparity have complementary representations with positive and negative disparity. In these cases, the representation with the disparity polarity opposite to the RD shall be used such that RD changes from -1 to +1 or vice versa at sub-block boundaries, and accumulation of disparity cannot occur. The starting value of the RD may be +1 or -1 for any BURST, but the M-TX shall follow the RD rules from the first SYNC symbol up to and including TAIL-OF-BURST (MARKER2).

4.5.3.2 M-RX Disparity Handling

145 Although decoding 8b10b does not require RD information, it is useful for error checking purposes. Therefore, the M-RX shall track the RD and flag per symbol to the protocol if an |RD|>1 is observed at any sub-block boundary. An erroneous RD shall be clipped immediately to +1 or -1, which in most cases corresponds to the correct value, such that the RD tracking is immediately capable of detecting further RD errors in subsequent symbols (see Figure 6).

146 The RD shall be correctly set at any MARKER0 inside a BURST. Detected RD errors during the HEAD-OF-BURST shall not be reported to the protocol, as it is normal that bit errors occur during bit synchronization, and the M-RX is not symbol synchronized until the first MARKER0.

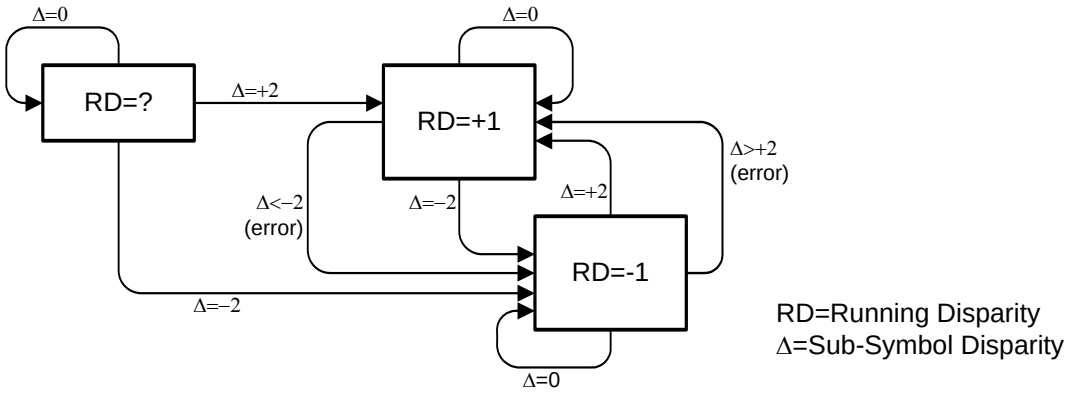


Figure 6 Running Disparity (RD) State Diagram

4.5.4 Bit Order and Binary Value

147 Throughout this document, the chronology for serial binary sequences and timing diagrams is from left (first in time) to right (last in time). Therefore, the notation for 8b10b symbols is “abcdeifghj”, where the “a” bit is transmitted first.

148 The notation of binary data values is MSb to LSb when reading from left to right. Data bytes are therefore indicated by “HGFEDCBA” where “H” is the MSb and A the LSb. This notation is used for payload data bytes as well as for configuration parameter values.

4.6 State Machines

149 The two types of MODULEs result in two alternate state machines intended for different applications with different application boundary conditions. M-PORTs of different type are not interoperable.

150 Both state machines allow for LS-MODE and HS-MODE operation, each including a BURST data transmission and power saving state. Performance scalability can be achieved by use of these modes combined with GEARs within modes.

151 The main differences between the two state machines are the following:

152 • Signaling scheme for LS-BURST (PWM versus SYS)
153 • Support for Media Converters (MC) in the LINE
154 • Assumptions about availability of auxiliary signals (e.g. reference clock, reset)

155 High level commonalities between the two state-machines are the following:

156 • LS-MODE for transmission in the Mbps speed range
157 • HS-MODE for transmission at Gbps rates
158 • Individual power saving states SLEEP and STALL in LS-MODE and HS-MODE, respectively
159 • Ultra-low power state HIBERN8
160 • LINE controlled state switching between BURSTs and its power saving state
161 • Protocol assisted configuration mechanism

162 Despite the high-level commonalities these aspects are not identical for the two MODULE types, and sometimes not even similar, e.g. LS-MODE with PWM (Type-I) versus SYS (Type-II) signaling.

163 The state-machines in a LANE are similar for M-TX and M-RX, however the state transition conditions are different from both perspectives. Therefore, separate state machines are provided for M-TX and M-RX.

4.6.1 State Machine for Type-I MODULEs

164 Specific features of Type-I MODULEs are the following:

165 • PWM self-clocked LS signaling

166 • Operation with independent local reference clocks; may benefit from shared reference clock if available

167 • Fully embedded control within the LANE (additional auxiliary signals are not required)

168 • Support for Media Converters in the LINE

169 State machines for Type-I M-TX and M-RX are shown in Figure 7 and Figure 8, respectively, and explained in the sections that follow.

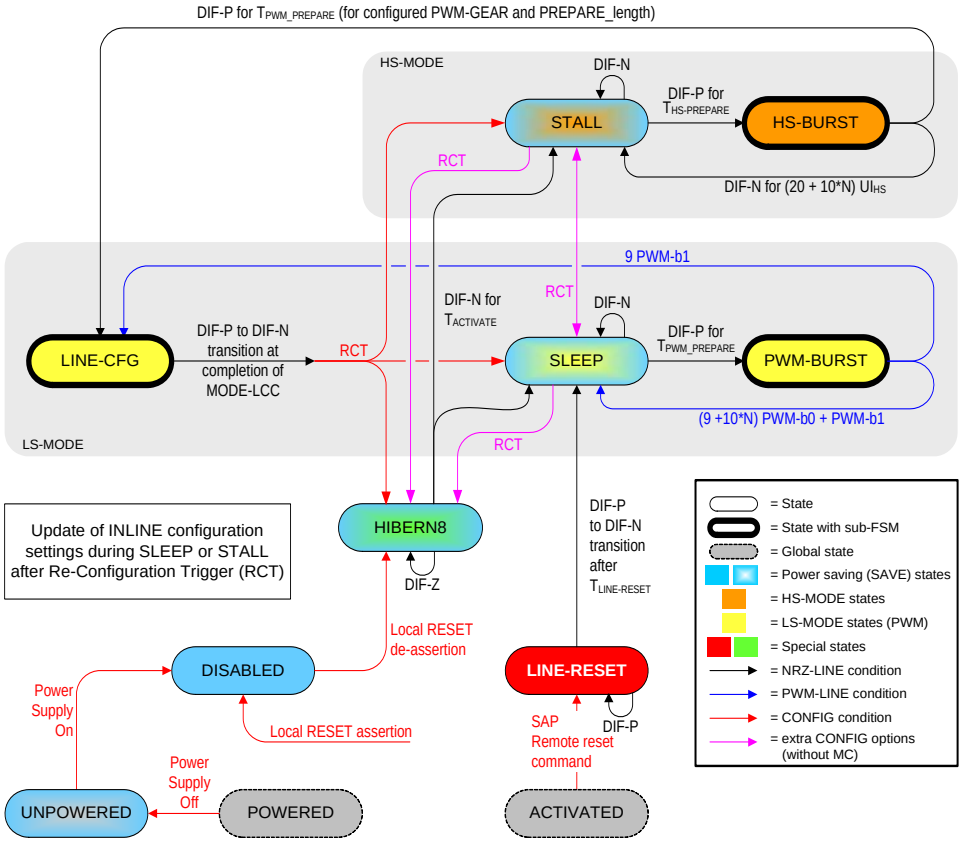


Figure 7 State Diagram for Type-I M-TX

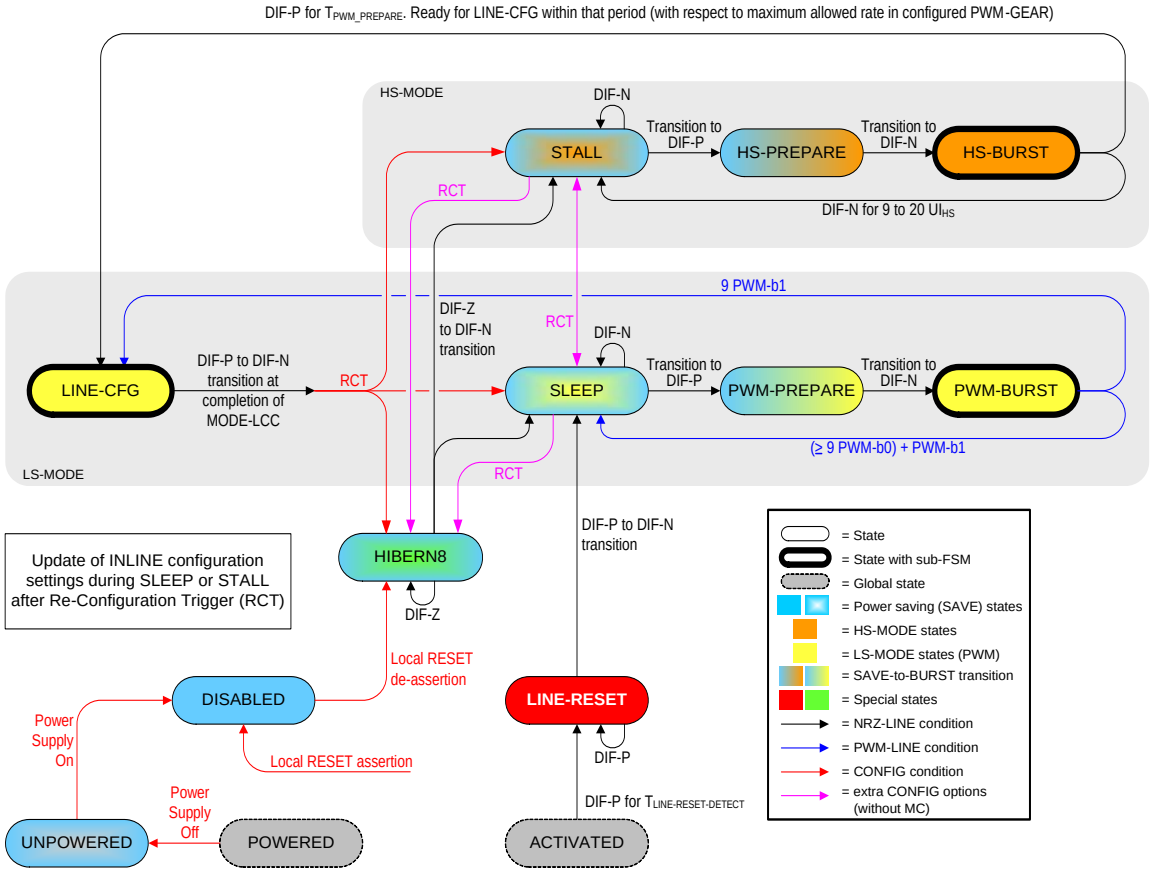


Figure 8 State Diagram for Type-I M-RX

4.6.2 State Machine for Type-II MODULEs

170 Specific features of Type-II MODULEs are the following:

171 • System-Clock-Synchronous LS signaling (SYS)

172 • Requires availability of a shared reference clock

173 • Partially embedded control within the LANE (some state transitions require additional auxiliary control signals)

174 State machines for Type-II M-TX and M-RX are shown in Figure 9 and Figure 10, respectively, and explained in the sections that follow.

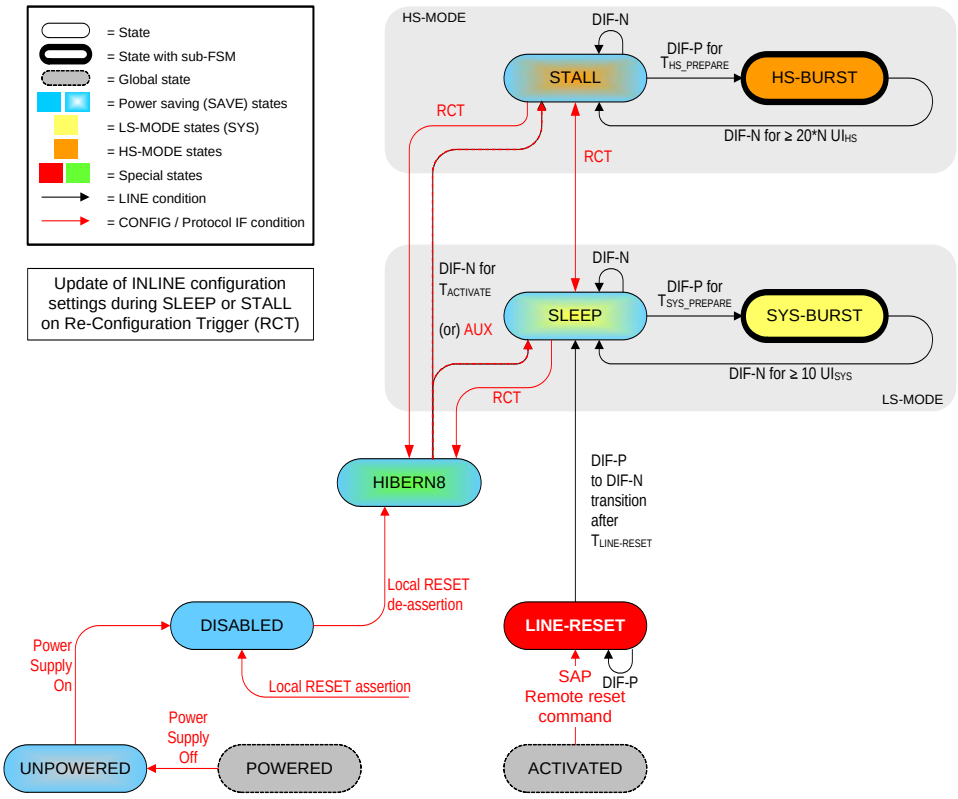


Figure 9 State Diagram for Type-II M-TX

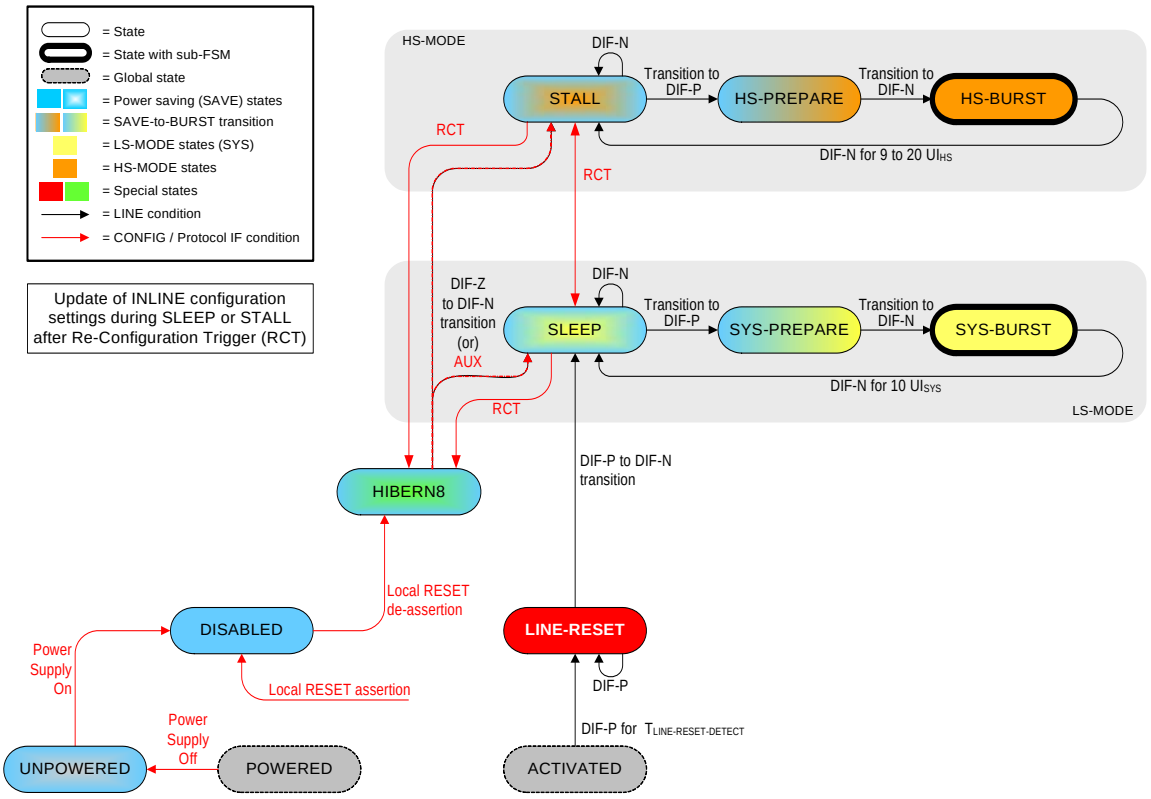


Figure 10 State Diagram for Type-II M-RX

4.6.3 State Machine Structure and State Categories

175 Each state machine encompasses two operating modes, HS-MODE and LS-MODE, that include a data transmission (BURST) state and a MODE-specific power saving (SAVE) state.

176 STALL is the SAVE state of HS-MODE, and SLEEP of LS-MODE. The BURST state of LS-MODE is denoted as PWM-BURST for Type-I and SYS-BURST for Type-II MODULEs, in alignment with the signaling scheme. LINE-CFG is an LS-MODE state for Type-I MODULEs only. Each mode has the following states:

177 • HS-MODE: STALL, HS-BURST

178 • LS-MODE (Type-I MODULEs): SLEEP, PWM-BURST, LINE-CFG

179 • LS-MODE (Type-II MODULEs): SLEEP, SYS-BURST

180 Therefore, each state machine includes only two BURST states. MODULEs may support LS-MODE only. The BURST states for each MODULE type is as follows:

181 • PWM-BURST (Type-I MODULEs only)

182 • SYS-BURST (Type-II MODULEs only)

183 • HS-BURST (Type-I and Type-II MODULEs, optional)

184 BURST states and LINE-CFG contain sub-FSMs, which are specified in Section 4.7.2 and Section 4.7.4.2, respectively.

185 Each state machine contains five SAVE states with a stationary LINE state. There is a specific SAVE state for each operating MODE, an ultra-low power state (HIBERN8), and two system-controlled power saving states for which the interface is no longer functional.

186 • STALL (HS-MODE)
187 • SLEEP (LS-MODE)
188 • HIBERN8 (Ultra-low power state while the LANE remains FUNCTIONAL)
189 • DISABLED (POWERED but not enabled due to a persistent local-reset)
190 • UNPOWERED (No power supply)

191 Furthermore, the following states are special purposes BREAK states:

192 • LINE-RESET (Embedded remote reset via the LINE)
193 • LINE-CFG (Configuration for Media Converters; Type-I MODULEs only)

194 Finally, there are some global state names that are not additional unique states, but are aliases for a subset of the states according to common characteristics.

195 The following names are global state names:

196 • POWERED (any state in the state machine, except UNPOWERED)
197 • SQUELCHED (POWERED states with LINE state DIF-Z, i.e. DISABLED and HIBERN8)
198 • FUNCTIONAL (any POWERED state except DISABLED)
199 • ACTIVATED (all states within HS-MODE or LS-MODE taken together)

200 ACTIVATED states are a subset of the FUNCTIONAL states, which are a subset of the POWERED states. This concept is illustrated in Figure 11.

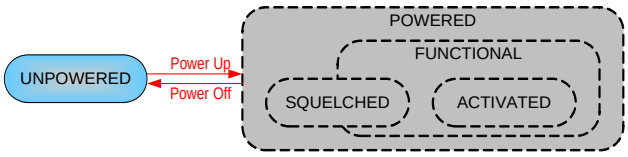


Figure 11 Relationship between Global States

201 An M-RX state transition is triggered by either a LINE or Protocol Interface (PIF) event. A LINE event is either a LINE state transition, LINE state sequence or a bit sequence in the applied signaling format. Some trigger events are also conditional on configuration settings.

4.7 FSM State Descriptions

202 This section specifies the purpose and operation for each of the SAVE, BURST, and BREAK states.

4.7.1 SAVE States

203 This section specifies the five power-saving states, STALL, SLEEP, HIBERN8, DISABLED, and UNPOWERED.

4.7.1.1 STALL

204 STALL is the power saving state in HS-MODE. STALL is mandatory for all MODULEs that support HS-MODE. In this state the M-RX shall be unterminated, while the M-TX shall drive DIF-N. This ACTIVATED state is intended for power savings without a severe penalty on HS-BURST start-up time, in order to enable fast and efficient BURST cycles. This state is exited to HS-BURST by a LINE transition to DIF-P. Entering

STALL can occur from HIBERN8, LINE-CFG, or SLEEP. The latter can only occur with an RCT in the absence of Media Converters. See Section 4.7.1.3, Section 4.7.4.2, and Section 4.7.1.2, respectively. A MODULE shall disclose, via a capability attribute, the minimum time it requires in STALL prior to starting a new BURST. See Section 8.4.

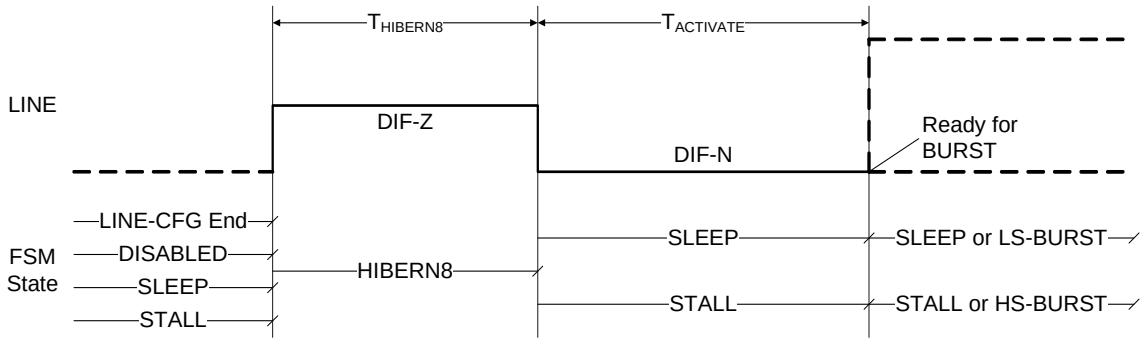
4.7.1.2 SLEEP

205 SLEEP is the power saving state of LS-MODE. SLEEP is mandatory for all MODULEs. The M-RX shall be unterminated, and the M-TX shall drive DIF-N. This state allows the lowest power consumption of all ACTIVATED states. This state is exited to LS-BURST by a LINE transition to DIF-P. Entering SLEEP can occur from HIBERN8, LINE-CFG, LINE-RESET, or STALL. The latter can only occur with an RCT in the absence of Media Converters. See Section 4.7.1.3, Section 4.7.4.2, Section 4.7.4.1, and Section 4.7.1.1, respectively. A MODULE shall disclose to the protocol, via a capability attribute, the minimum time it requires in SLEEP prior to starting a new BURST. See Section 8.4.

4.7.1.3 HIBERN8

206 This FUNCTIONAL state enables ultra-low power consumption, while maintaining the configuration settings. HIBERN8 shall be supported by all MODULEs. The M-TX shall be high-impedance in HIBERN8, while the M-RX shall hold the LINE at DIF-Z.

207 In order to exit HIBERN8, the M-TX shall drive DIF-N for a period $T_{ACTIVATE}$. For embedded HIBERN8 exit control, the M-RX shall include (squelch) detection for a LINE transition to DIF-N. Alternatively, exit of HIBERN8 can be indicated by auxiliary control signals. For Type-I MODULEs, embedded exit control by squelch detection is mandatory, for Type-II MODULEs this is optional. Note that squelch detection is only utilized in HIBERN8, so this function can be disabled for all other states. LANE MODULEs become ACTIVATED on exit of HIBERN8 and shall return to the power saving state of the configured operating mode and be ready for a BURST within $T_{ACTIVATE}$.



Entry to HIBERN8 from SLEEP or STALL only with RCT for Type-II, or Type-I in absence of a Media Converter

Figure 12 Entry and Exit of HIBERN8

208 Entering HIBERN8 can occur from LINE-CFG, STALL, SLEEP, and DISABLED states. Entry of HIBERN8 from LINE-CFG, STALL or SLEEP state is controlled via configuration (see Table 46). The mechanism is specified in Section 4.7.4.2.4. Note that when requesting HIBERN8 from LINE-CFG, the LINE signal first switches from DIF-P to DIF-N, which ends LINE-CFG and causes a Re-Configuration Trigger (RCT). An RCT is an internally driven event that occurs after the end of LINE-CFG and initiates a transition to HIBERN8 causing the LINE signal to switch from DIF-N to DIF-Z. Therefore, HIBERN8 is always entered from a DIF-N LINE state. Entering HIBERN8 from DISABLED does not typically happen simultaneously for the M-TX and the M-RX in a LANE because it depends on independent timings of local RESET signals

on each side of the LANE. Signals and states before, during, and after HIBERN8 state are illustrated in Figure 12.

4.7.1.4 DISABLED

209 DISABLED is a POWERED state, while MODULE operation is disabled by a local RESET signal. When DISABLED, an M-TX shall be high impedance, and an M-RX shall keep the LINE at DIF-Z. All configuration settings shall be reset to default values. LANE operation cannot be (re-)established via LINE signaling. Entry and exit of DISABLED state are controlled by asserting or de-asserting a local RESET at the Protocol InterFace.

4.7.1.5 UNPOWERED

210 UNPOWERED is the state of a MODULE when the power supply is withdrawn. Both M-TX and M-RX shall be high-impedance while UNPOWERED. During UNPOWERED state the LINE level is undefined, except that the LINE voltages shall not exceed the safe operation voltage window V_{PIN}. All configuration settings are lost. During powering-up, a MODULE shall exit into DISABLED state on the assertion of the local RESET. This is typically triggered by a Power-on-Reset signal.

4.7.1.5.1 Power-Up Cycle

211 When the power supply comes up on a MODULE, a local RESET signal shall drive the MODULE into DISABLED. This local RESET is typically derived from the system Power-On-Reset (POR). During power-up until shortly after the assertion of RESET, an M-TX may temporarily expose a lower impedance. However, a Type-I M-TX shall not cause a differential exceeding the squelch threshold throughout the complete power-up cycle until the successful entry of HIBERN8 for both M-TX and M-RX on a LANE.

212 The LINE state becomes defined when the M-RX is POWERED and enters DISABLED state. In DISABLED state the M-TX is high-impedance, while the M-RX pulls the LINE state to DIF-Z. If after the power-up cycle the local RESET is de-asserted, the MODULE shall enter HIBERN8. MODULEs remain DISABLED by keeping the local RESET asserted. Note that the local RESET shall not be de-asserted before the complementary LANE MODULE at the other side of the LINE has been DISABLED.

4.7.2 BURST States General

213 Data transmission occurs in BURSTs with power saving states in-between. BURSTs can be transferred in HS-MODE or LS-MODE, HS-BURST in HS-MODE, and LS-BURST in LS-MODE. There are two variants of LS-BURSTs depending on the applied signaling scheme, PWM-BURST for Type-I MODULEs, and SYS-BURST for Type-II MODULEs. This section specifies the sequence of events during BURST states.

214 Each BURST starts from the SAVE state for that operating mode, with a transition from DIF-N to DIF-P. After a period of DIF-P called PREPARE, a sequence of 8b10b encoded symbols follows as specified in Section 4.7.2.1. After the last 8b10b symbol (MK2) of the BURST either a series of b0s or a series of b1s is transmitted. These series of equal bits violate the 8b10b code characteristics, and indicates whether the LANE shall return to the SAVE state of the current operating mode or shall enter LINE-CFG. In case of PWM signaling the last bit of the sequence is inverted to indicate the end of LINE activity.

215 Each BURST state contains a sub-state machine which specifies the sequence of events during a BURST, which is shown in Figure 13. There is much similarity between individual BURST states, but there are also distinct differences due to the exploited signaling schemes, which are explained in the following sections.

216 The following sections specify the details of the BURST sub-state machine.

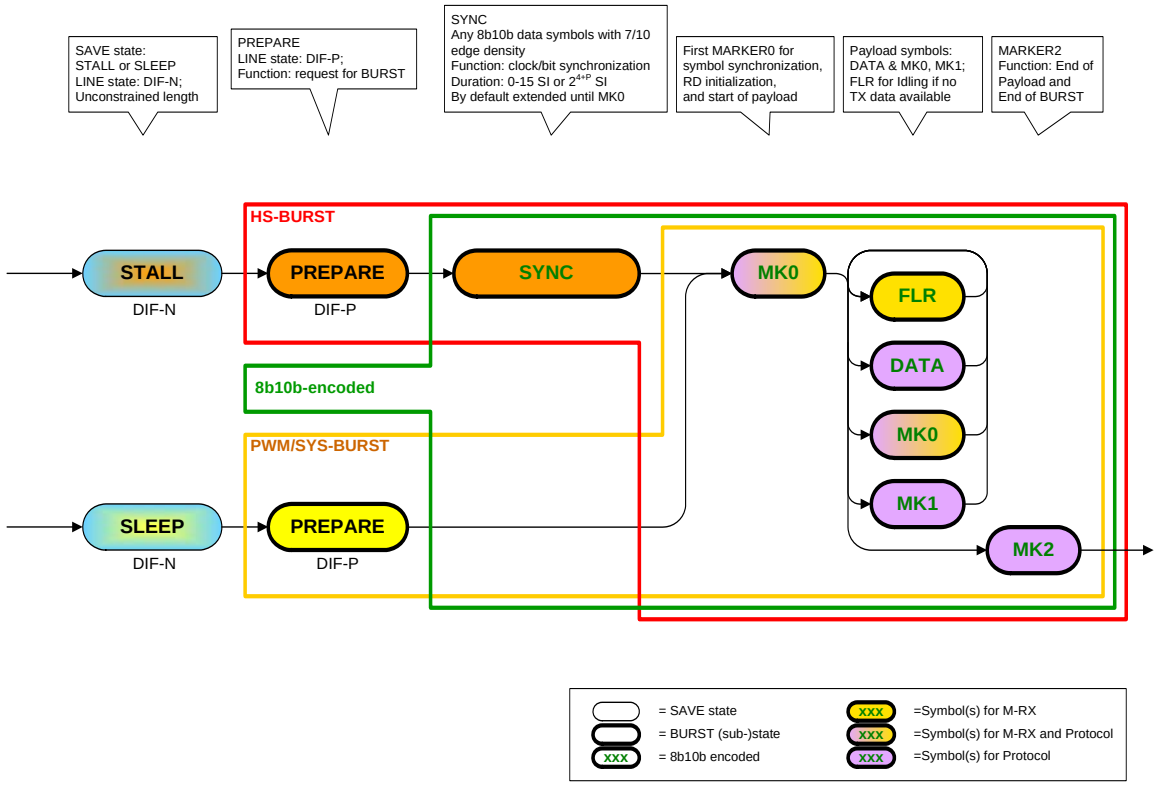


Figure 13 BURST-SAVE: Detailed Sub-FSM

4.7.2.1 PREPARE for BURST

217 PREPARE is the DIF-P period when entering BURST states to allow settling of LINE levels and transceiver settings before the bitstream gets started. If the M-RX is configured to terminate the LINE during the BURST, the termination shall be enabled during the PREPARE period. Signal integrity shall be maintained during any change of termination status. At the end of the PREPARE period the LINE signals shall be settled. The length of PREPARE is configurable and specified in Table 6.

4.7.2.2 SYNC

218 For HS-MODE, the PREPARE period shall be followed by a SYNC sequence. The SYNC sequence is intended for bit synchronization of the M-RX to the embedded clock data stream. The SYNC sequence shall be a serialized subset of 8b10b data symbols with a high edge density for fast synchronization. Therefore, only symbols with at least seven transitions inside the symbol (out of nine possible transitions) may be used for the SYNC sequence. Data symbols fulfilling this condition are listed in Table 5.

219 The SYNC sequence shall, by default, be generated by the M-TX, but can be optionally configured to be provided by the protocol. The default SYNC sequence shall be an alternating D10.5 and D26.5 pattern that may start with either of the two symbols. A SYNC pattern provided by the protocol shall only contain data symbols listed in Table 5. The SYNC sequence may start with RD of +1 or -1. However, for DC-balance, the SYNC sequence shall be encoded according to Running Disparity rules.

Table 5 Valid Data Symbols for SYNC Sequence

Symbol Name	HGFEDCBA	RD = +1	RD = -1	Number of Transitions
		abcdeifghj	abcdeifghj	
D10.2	01001010	0101010101	0101010101	9
D21.5	10110101	1010101010	1010101010	9
D2.2	01000010	0100100101	1011010101	8
D4.2	01000100	0010100101	1101010101	8
D21.0	00010101	1010100100	1010101011	8
D21.4	10010101	1010100010	1010101101	8
D31.2	01011111	0101000101	1010110101	8
D5.2	01000101	1010010101	1010010101	8
D9.2	01001001	1001010101	1001010101	8
D10.5	10101010	0101011010	0101011010	8
D10.6	11001010	0101010110	0101010110	8
D21.1	00110101	1010101001	1010101001	8
D21.2	01010101	1010100101	1010100101	8
D22.5	10110110	0110101010	0110101010	8
D26.5	10111010	0101101010	0101101010	8
D1.2	01000001	1000100101	0111010101	7
D2.5	10100010	0100101010	1011011010	7
D2.6	11000010	0100100110	1011010110	7
D4.5	10100100	0010101010	1101011010	7
D4.6	11000100	0010100110	1101010110	7
D10.0	00001010	0101010100	0101011011	7
D10.4	10001010	0101010010	0101011101	7
D15.2	01001111	1010000101	0101110101	7
D16.2	01010000	1001000101	0110110101	7
D21.7	11110101	1010100001	1010101110	7
D22.0	00010110	0110100100	0110101011	7
D22.4	10010110	0110100010	0110101101	7
D23.5	10110111	0001011010	1110101010	7
D26.0	00011010	0101100100	0101101011	7

Table 5 Valid Data Symbols for SYNC Sequence (continued)

Symbol Name	HGFEDCBA	RD = +1	RD = -1	Number of Transitions
		abcdeifghj	abcdeifghj	
D26.4	10011010	0101100010	0101101101	7
D27.5	10111011	0010011010	1101101010	7
D29.5	10111101	0100011010	1011101010	7
D31.5	10111111	0101001010	1010111010	7
D31.6	11011111	0101000110	1010110110	7
D2.0	00000010	0100101011	1011010100	7
D2.4	10000010	0100101101	1011010010	7
D4.0	00000100	0010101011	1101010100	7
D4.4	10000100	0010101101	1101010010	7
D5.5	10100101	1010011010	1010011010	7
D5.6	11000101	1010010110	1010010110	7
D6.2	01000110	0110010101	0110010101	7
D9.5	10101001	1001011010	1001011010	7
D9.6	11001001	1001010110	1001010110	7
D10.1	00101010	0101011001	0101011001	7
D11.5	10101011	1101001010	1101001010	7
D12.2	01001100	0011010101	0011010101	7
D13.5	10101101	1011001010	1011001010	7
D18.2	01010010	0100110101	0100110101	7
D19.5	10110011	1100101010	1100101010	7
D20.2	01010100	0010110101	0010110101	7
D21.3	01110101	1010100011	1010101100	7
D21.6	11010101	1010100110	1010100110	7
D22.1	00110110	0110101001	0110101001	7
D22.2	01010110	0110100101	0110100101	7
D25.5	10111001	1001101010	1001101010	7
D26.1	00111010	0101101001	0101101001	7
D26.2	01011010	0101100101	0101100101	7
D31.0	00011111	0101001011	1010110100	7
D31.4	10011111	0101001101	1010110010	7

220 The SYNC sequence has a minimum duration, T_{SYNC}, that is configurable in order to accommodate different application conditions as shown in Table 6. The SYNC sequence is followed by payload that shall start with a MARKER0 (MK0). Transmission of MARKER0 is on protocol request. If MARKER0 is not requested before the configured SYNC length expires, the SYNC sequence shall be extended until the protocol requests transmission of MARKER0. PWM-BURST and SYS-BURST do not include SYNC because transmission in LS-MODE is either reference clock-synchronous (SYS) or self-clocked (PWM) depending on the LS signaling scheme.

Table 6 PREPARE and SYNC Attribute and Dependent Parameter Values

Name of Attribute/Parameter	Value	Unit
HS_PREPARE_length	0 to 15	n/a
$T_{HS\_PREPARE}$	HS_PREPARE_length*$2^{(GEAR - 1)}$	SI
LS_PREPARE_length	0 to 15	
$T_{PWM\_PREPARE}$	maximum($2^{LS\_PREPARE\_length + GEAR - 7}$,1)	SI
$T_{SYS\_PREPARE}$	LS_PREPARE_length	SI
SYNC_length	0 to 15	n/a
SYNC_range	0 to 1	n/a
T_{SYNC}	IF SYNC_range=0 SYNC_length ELSE (IF SYNC_range=1) 2^{SYNC_length} END	SI

4.7.2.3 PAYLOAD of BURST

221 After SYNC or PREPARE period, PAYLOAD shall be transferred on request of the protocol. PAYLOAD shall start with a MARKER0 (HEAD-OF-BURST) and shall end with a MARKER2 (TAIL-OF-BURST). Between the HEAD and TAIL symbols, any number of DATA0 to DATA255, MARKER0 or MARKER1 symbols can be transported in any order under protocol control via the PIF. Note that the MARKER0 symbol has comma properties. This shall be utilized in the M-RX, to acquire, check and regain symbol alignment on any occurrence of MARKER0. If during a BURST at any time after the first MARKER0 the protocol does not provide the next symbol request on time, the M-TX will insert FILLER symbols (FLR) in order to prevent failure and corruption of the serial stream. The FILLER symbols are removed by the M-RX, but occurrence is indicated to the protocol via the PIF. The protocol layer may periodically provide MARKER0 for the purposes of self-healing or re-synchronization.

4.7.2.4 Closure of BURST

222 With the transmission of MARKER2 the PAYLOAD ends and the LANE shall either return to the mode's SAVE state or enter LINE-CFG state depending on the polarity of constant bit sequence after MARKER2; this constant bit sequence violates the 8b10b coding rules. The M-RX shall exit BURST mode on detection of the constant bit sequence, not on detection of MK2 itself.

4.7.2.4.1 Closure and Return to SAVE

223 If after MARKER2 a series of b0s is transmitted, the LANE returns to the SAVE state of the operating mode. The amount and format of bits differ for different BURST states depending on the signaling scheme. The conditions are summarized in Table 7. If the M-RX is configured to terminate during BURST, it shall disconnect its termination at return to SAVE state.

4.7.2.4.2 Closure and Return to LINE-CFG

224 After MARKER2 a series of b1s shall be transmitted for a period $T_{PWM\_PREPARE}$, after which the LANE shall return to LINE-CFG state in LS-MODE. The amount and format of bits differ for different BURST states depending on the signaling scheme. The conditions are summarized in Table 7. This state transition does not exist in the Type-II state machine.

Table 7 Summary of BURST Closure Conditions

MODE	MODULE	Return to SAVE		Return to LINE-CFG LINE Condition
		LINE Condition[1]	State	
HS	M-TX	DIF-N for (20 +10*N) UI_{HS}	STALL	DIF-P for $T_{PWM\_PREPARE}$
HS	M-RX	DIF-N for 9 to 20 UI_{HS}	STALL	DIF-P for $T_{PWM\_PREPARE}$
PWM	M-TX	(9 + 10*N) PWM-b0 + PWM-b1	SLEEP	9 PWM-b1
PWM	M-RX	(>= 9 PWM-b0) + PWM-b1	SLEEP	9 PWM-b1
SYS	M-TX	DIF-N for >= 10 UI_{SYS}	SLEEP	N/A
SYS	M-RX	DIF-N for 10 UI_{SYS}	SLEEP	N/A

1. *N is an integer number of symbols. The duration of the BURST closure condition is dynamically controlled by TX_BURST_Closure_Extension.*

4.7.2.5 Example of an HS-BURST

225 A time domain illustration of HS-BURST operation is shown in Figure 14. In this example the M-RX is (default) configured to provide LINE termination during HS-BURST, which can be noticed by the signal level changes during PREPARE and (exit-to-)STALL.

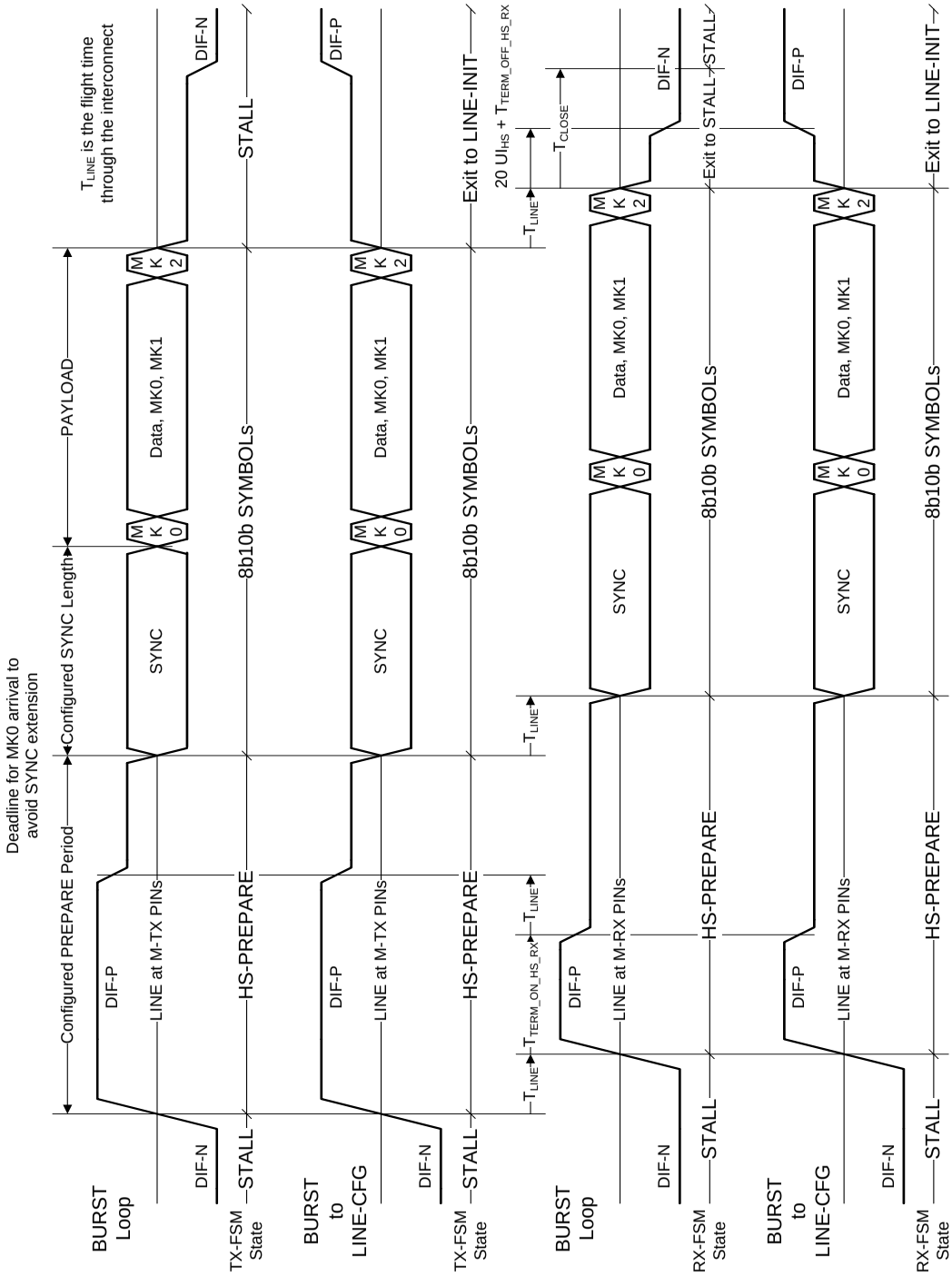


Figure 14 HS-BURST Operation

4.7.3 BURST States Individual

4.7.3.1 HS-BURST

226 HS-BURST is the data transmission state of HS-MODE. HS-BURST starts from STALL on a transition to DIF-P. Data shall be 8b10b encoded in this mode and transmitted using NRZ signaling. After the last symbol of the BURST, a MODULE enters STALL state, or in the case of a Type-I MODULE, enters LINE-CFG state, depending on the exit condition on the LINE.

4.7.3.1.1 HS-GEARs

227 A MODULE in HS-BURST shall only operate at specified fixed rates. There are two RATE series, A and B, where each step in the series scales by a factor of two, while the speed rate difference between the two RATE series is about 15%, as listed in Table 8. If the rates of the two RATE series are pair-wise coupled for closest rates (~15%), these individual couples are denoted as GEARs. A MODULE that includes HS-MODE shall support both RATEs of a GEAR. A MODULE supporting HS-MODE shall support HS-G1. If a higher GEAR is supported all lower GEARs shall be supported as well.

Table 8 HS-BURST: RATE Series and GEARs

RATE A-series (Mbps)	RATE B-series (Mbps)	High-Speed GEARs
1248	1457.6[1]	HS-G1 (A/B)
2496	2915.2[1]	HS-G2 (A/B)
4992	5830.4[1]	HS-G3 (A/B)

1. *The B-series RATEs shown are not integer multiples of common reference frequencies 19.20 MHz or 26.00 MHz, but are within the tolerance range of 2000 ppm.*

4.7.3.2 PWM-BURST

228 PWM-BURST is the data transmission state of LS-MODE of Type-I LINKs. PWM-BURST starts from SLEEP on the transition to DIF-P. Data shall be 8b10b encoded in this mode and transmitted using PWM signaling. After the last symbol of the BURST, a series of at least ten equal PWM-bits is added, which creates an 8b10b run-length violation on the LINE. For a sequence of ten PWM-b0, the LANE shall return to SLEEP state. For a sequence of ten PWM-b1, the LANE shall go to LINE-INIT state.

4.7.3.2.1 PWM-GEARs

229 PWM-BURST has multiple GEARs, each with a limited speed range. Table 9 lists all the PWM-GEARs. PWM-G1 is the default GEAR at start-up and after reset. Only PWM-G1 is mandatory. Except for PWM-G0, each GEAR spans a speed range of a factor of three, while subsequent PWM-GEARs scale with factors of two. This allows a continuum of possible rates. If a higher PWM-GEAR is supported all lower GEARs down to default GEAR shall be supported as well. PWM-G0 is optional independently. For PWM-G1 and all higher PWM-GEARs, FIXED-RATIO signaling shall be applied. The FIXED-MINOR signaling format shall be used for PWM-G0.

Table 9 PWM-BURST GEARs

PWM-GEARs	Min. (Mb/s)	Max. (Mb/s)
PWM-G0	0.01	3

Table 9 PWM-BURST GEARs (continued)

PWM-GEARs	Min. (Mb/s)	Max. (Mb/s)
PWM-G1	3	9
PWM-G2	6	18
PWM-G3	12	36
PWM-G4	24	72
PWM-G5	48	144
PWM-G6	96	288
PWM-G7	192	576

4.7.3.3 System-clock Synchronous BURST (SYS-BURST)

230 SYS-BURST is the data transmission state of LS-MODE of Type-II LINKs. SYS-BURST starts from SLEEP on the transition to DIF-P. Data shall be 8b10b encoded in this mode and transmitted using reference-clock synchronous NRZ signaling. After the last symbol of the BURST, the LINE is driven to DIF-N state. The long DIF-N creates an 8b10b run-length violation which ends SYS-BURST and moves the LANE to SLEEP state.

231 In this mode, MODULEs depend on a shared reference clock for transmission. The transmission rate in this mode shall be an integer division of the shared reference clock frequency, f_{SYS_REF}. The reference clock may originate from an independent system clock or from one of the two devices in the LINK. An example of the latter case is shown in Figure 15, where the device providing the clock is located on the left hand side of the figure.

232 This document only partially specifies this mode, as it also relies on the specifications of the reference clock, the timing relationship between the clock pin on the devices and the reference clock input of the MODULEs (PIF), and the timing between reference clock input of the MODULEs and the LINE signals. Section 5 contains an informative guideline for timing between reference clock and LINE signals. The overall timing specifications for this signaling scheme shall be covered by the protocol specification utilizing this mode.

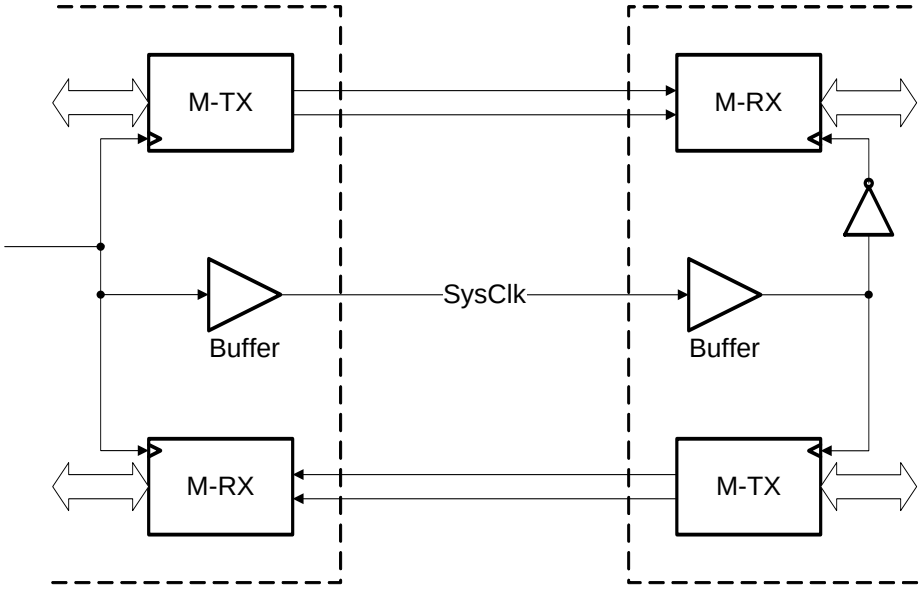


Figure 15 Bidirectional SYS-BURST Clocking Example

4.7.4 BREAK States

233 BREAK states are FUNCTIONAL states with special functions, which are entered by exceptional LINE sequences that do not occur during normal operating modes.

4.7.4.1 LINE-RESET

234 This is the lowest level reset mechanism in order to reset the M-RX via the LINE during operation in case of malfunction. The LINE-RESET condition is a long DIF-P period, which can never occur during normal operation. LINE-RESET shall be functional on all ACTIVATED states. Just before LINE-RESET the M-TX shall drive DIF-N for at least $T_{ACTIVATE}$ so that an M-RX, which may be in HIBERN8, is ACTIVATED before the LINE-RESET condition is driven. For LINE-RESET, the M-TX shall drive DIF-P for $T_{LINE-RESET}$. The M-RX shall be reset when DIF-P is observed on the LINE for $T_{LINE-RESET-DETECT}$. The LINE-RESET timer shall not rely on correct protocol operation. LINE-RESET exits to SLEEP on a transition to DIF-N. LINE-RESET shall reset all configuration settings to their default values.

235

Table 10 LINE-RESET and HIBERN8 Timer Values

Parameter	Min.	Max.	Unit	Descriptions and Notes
$T_{LINE-RESET}$	3.1		ms	
$T_{LINE-RESET-DETECT}$	1	3	ms	
$T_{ACTIVATE}$	10		ms	
$T_{HIBERN8}$	10		ms	

4.7.4.2 LINE-CFG (for Type-I MODULEs Only)

236 LINE-CFG state enables low-level configuration features. This functionality shall be supported by MODULEs used for a LANE that may contain a Media Converter, as a Media Converter is configured by this mechanism. LINE-CFG enables a MODULE to write and read configuration attributes to and from a Media Converter. A Media Converter typically contains only a subset of the physical layer functionality and no protocol stack and therefore cannot be directly accessed by the protocol.

237 The sub-state machines of the LINE-CFG state are shown in Figure 16 and Figure 17 for the M-TX and M-RX, respectively. These state machines consists of LINE Control Commands (LCC) with their corresponding parameter field, interleaved by LINE-INIT states. LINE-INIT state means nine or more b1 bits in a row, generated in case of M-TX or received in case of M-RX. This exception condition does not occur during any other state. The M-TX state machine shall sequence the enabled commands in a specified order, starting with WRITE, followed by READA, then READB, and ending with MODE. The LCC-MODE command exits into SLEEP state. Note that during LINE-INIT states, only commands that are enabled shall be transmitted, not enabled commands shall be skipped. The enabled commands are controlled by protocols via the SAP. The M-RX shall not be sensitive to the order of LCCs, except that the LCC-MODE command is always the last one. However, the M-RX will logically receive commands in the order as specified for the M-TX. Detailed specifications of these states are provided in the following sections. TX_LCC_Sequencer (see Table 46) shall automatically be reset after LCC operation.

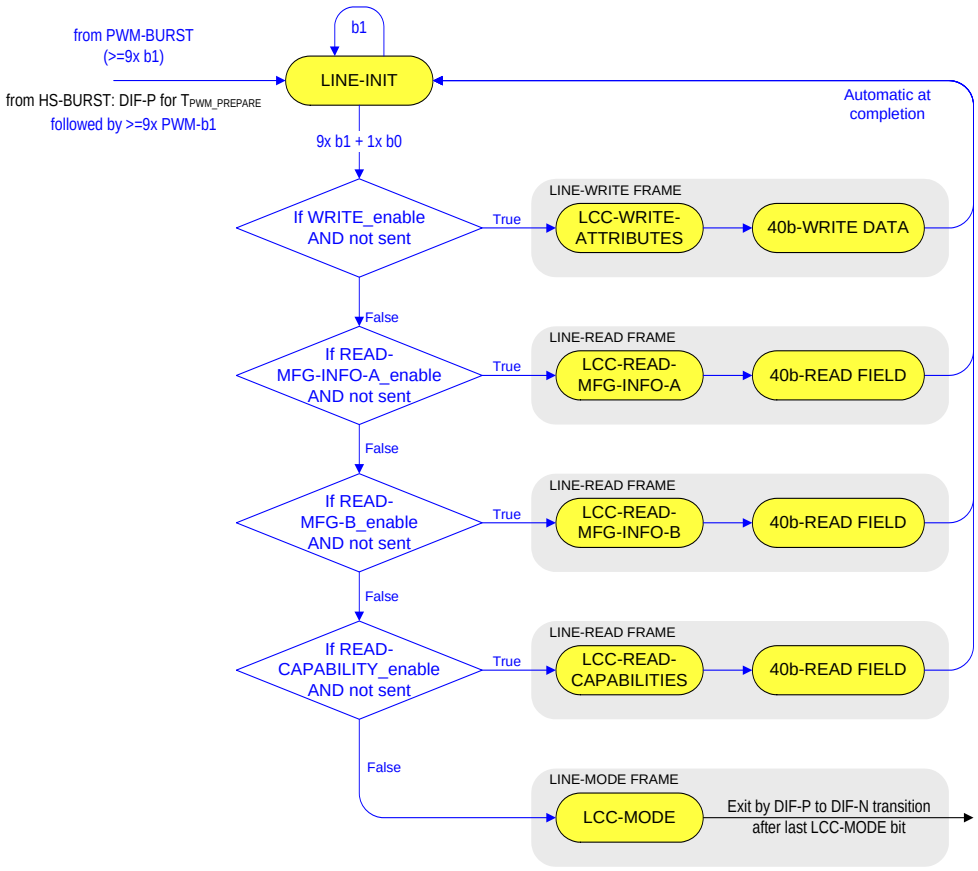


Figure 16 Sub-state Machine of M-TX for LINE-CFG

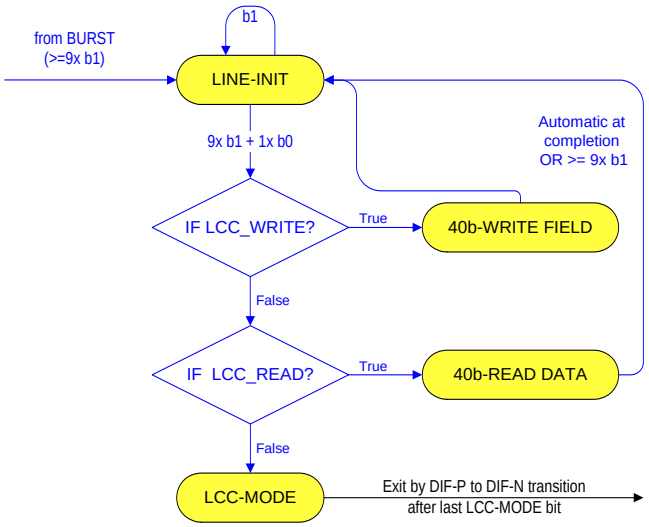


Figure 17 Sub-state Machine of the M-RX for LINE-CFG

4.7.4.2.1 LINE-INIT

238 LINE-CFG is entered in LINE-INIT. This can occur either from HS-BURST with a period $T_{PWM\_PREPARE}$ of DIF-P (which shall be followed by >= 9 PWM-b1s), or from PWM-BURST by a sequence >= 9 PWM-b1s. The LANE stays in LINE-INIT as long as PWM-b1 are transferred, which is under protocol control and may last indefinitely. LINE-INIT ends with a PWM-b0, immediately followed by a 10-bit LINE-Control-Command (LCC) which contains the requested action. LINE-INIT state between two commands shall be exactly ten bits long, consisting of nine b1 bits and one b0 bit. Possible b1 bits belonging to the preceding command shall not be counted, so precisely ten bits are inserted.

4.7.4.2.2 LINE Control Command (LCC)

239 LCCs are 10-bit long and are always preceded by a PWM-b0, being part of, and completing, LINE-INIT. LCCs are not 8b10b encoded. Table 11 lists the functions of the bits in the LCCs, which can be divided into four categories. MODE-LCCs (24), WRITE-LCCs (1), READ-LCCs (2), and RESERVED-LCCs for future usage. MODE-LCCs have no additional data field and are therefore just ten bits long and exit into DIF-N LINE state. The resulting Re-Configuration Trigger will move the state to STALL, SLEEP, or HIBERN8. See Section 4.7.4.2.4 for more details. LCCs shall only be issued starting from LINE-INIT state.

240 LCCs contain five information bits (d[4:0]) which encode the requested action and are transmitted first. The remaining five bits are used to increase robustness. LCCs are protected against bit-errors by a SECDED Hamming code scheme with five parity bits (p1 to p5 = d5 to d9).

Table 11 LCC Definition[1]

d0	d1	LCC-Category	d2	d3	d4	Command	d5	d6	d7	d8	d9
							p1	p2	p3	p4	p5
0	0	MISC	0	0	0	RESERVED	1	1	1	1	1
			0	0	1	RESERVED	0	1	1	0	0
			0	1	0	RESERVED	0	0	0	1	1
			0	1	1	HIBERN8-SLEEP	1	0	0	0	0
			1	0	0	RESERVED	1	0	0	1	0
			1	0	1	RESERVED	0	0	0	0	1
			1	1	0	RESERVED	0	1	1	1	0
			1	1	1	HIBERN8-STALL	1	1	1	0	1
0	1	READ/ WRITE	0	0	0	READ-CAPABILITY	0	1	0	1	0
			0	0	1	RESERVED	1	1	0	0	1
			0	1	0	RESERVED	1	0	1	1	0
			0	1	1	READ-MFG-INFO-A	0	0	1	0	1
			1	0	0	READ-MFG-INFO-B	0	0	1	1	1
			1	0	1	WRITE-ATTRIBUTE	1	0	1	0	0
			1	1	0	RESERVED	1	1	0	1	1
			1	1	1	RESERVED	0	1	0	0	0
1	0	PWM-MODE	0	0	0	PWM-0	0	0	1	1	0
			0	0	1	PWM-1	1	0	1	0	1
			0	1	0	PWM-2	1	1	0	1	0
			0	1	1	PWM-3	0	1	0	0	1
			1	0	0	PWM-4	0	1	0	1	1
			1	0	1	PWM-5	1	1	0	0	0
			1	1	0	PWM-6	1	0	1	1	1
			1	1	1	PWM-7	0	0	1	0	0

Table 11 LCC Definition[1] (continued)

d0	d1	LCC-Category	d2	d3	d4	Command	d5	d6	d7	d8	d9
							p1	p2	p3	p4	p5
1	1	HS-MODE	0	0	0	HS-1A	1	0	0	1	1
			0	0	1	HS-2A	0	0	0	0	0
			0	1	0	HS-3A	0	1	1	1	1
			0	1	1	RESERVED	1	1	1	0	0
			1	0	0	HS-1B	1	1	1	1	0
			1	0	1	HS-2B	0	1	1	0	1
			1	1	0	HS-3B	0	0	0	1	0
			1	1	1	RESERVED	1	0	0	0	1

1. *Columns for LCC data bits in this table are not intended to convey any information on bit-order transmission. Transmission of a 10-bit LCC should always begin with b0.*

4.7.4.2.3 LINE-READ and LINE-WRITE Frames

241 LINE-READ and LINE-WRITE frames contain four byte data/fields (thirty-two bits) after the LCC. These four bytes are transmitted in a 4x10-bit format across the LINE. Each 10-bit block contains one byte of information in the center, which is sandwiched between two b0s. The data bits d[7:0] of each byte shall therefore be located in the second bit through the second-to-last bit of each ten bit block as illustrated in Figure 18. The first and last bit of each 10-bit block shall be b0.

242 The transmitted bytes of a LINE-READ frames shall be all b1 (0xFF), while the payload bytes of a LINE-READ at the M-RX side contain the information, which is read from the Media Converter. There are two READ commands, READA and READB, with the same format, enabling more bits to read if necessary. The M-RX shall store the READ bytes as Media Converter attributes in the configuration registry. The WRITE bytes consists of a selection of bits, which are derived from attributes in the M-TX configuration registry.

243 The exact contents and meaning of the WRITE and READ bytes are specified in Section 8 and Section 7.

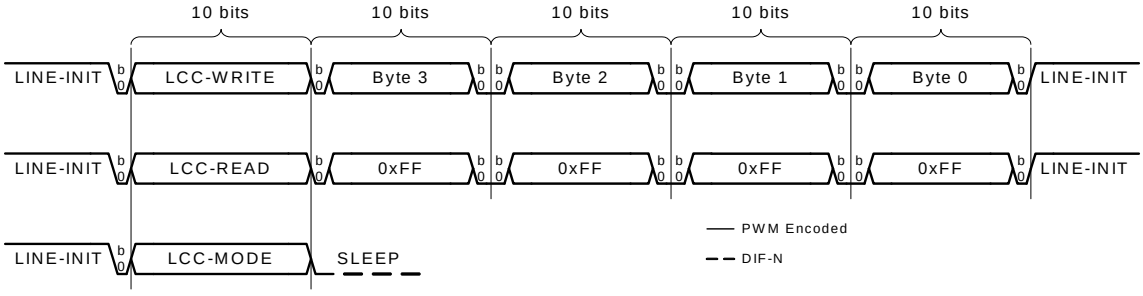


Figure 18 Format of Different LCC Frames on the LINE

4.7.4.2.4 Re-Configuration Trigger (RCT)

244 Several transitions in the state machines are conditional on a Re-Configuration Trigger (RCT). This is to prevent failure of operation due to a temporary, inconsistent set of configured attribute values. The RCT is an indication that re-configuration has been completed, and the set of newly configured attribute values is

consistent. Configuration changes shall not impact functional behavior prior to the RCT. See also Section 4.8 regarding INLINE and OFFLINE attributes. RCT is also the trigger to change operational status (INLINE attributes) according to the new configuration settings. A MODULE shall do that as soon as a it enters (if it was not already in) SAVE state. The protocol shall provide sufficient time to the LANE to complete re-configuration before requesting a new BURST. The minimum required duration of SAVE states is a MODULE capability. See Section 8.4.

245 An RCT is not a signal provided by the protocol, but a logical function of protocol interface signals, MODULE status, and use case. An RCT is generated when the following conditions are fulfilled:

246 1. A CFG-READY indication via the Protocol InterFace

247 2. Entering or being in SAVE state

248 3. Completion of LINE-CFG (Only applies for Type-I MODULEs when a Media Converter is allowed)

249 The first two conditions always apply. This covers Type-II operation and Type-I operation in absence of Media Converters. The third condition is specific for Type-I MODULEs.

250 If the LANE includes a Media Converter, there needs to be provision to configure it. Therefore, some configuration attributes need to be exchanged between Media Converter and LANE MODULEs. This is accomplished by LINE-CFG; see Section 4.7.4.2. The protocol shall configure the M-TX to exit to LINE-INIT from the BURST that contains the CFG-READY message (invisible to MODULEs). The M-TX stays in LINE-INIT, until reception of an M-CTRL-CFGREADY.request primitive from the Protocol Interface, which initiates the execution of the LINE-CFG sequence. LINE-CFG ends with an LCC-MODE command that includes the (newly) requested mode of operation. Note that the MODULEs are in LS-MODE during LINE-CFG. The requested mode can be either LS-MODE, HS-MODE, or HIBERN8, implying that the next state after completion of LINE-CFG can be either SLEEP, STALL, or HIBERN8. The transition from DIF-P to DIF-N after the last bit of the LCC-MODE command is the final trigger to update the operational configuration data for M-TX, M-RX, and Media Converters. Note that the M-RX does not get its configuration information from the LINE-CFG, but via the Protocol Interface. Nevertheless, the configuration settings for M-TX, M-RX, and Media Converters become first effectuated on this DIF-P to DIF-N transition, that ends LINE-CFG.

251 Note that when requesting HIBERN8 from LINE-CFG, the LINE signal first switches from DIF-P to DIF-N which ends LINE-CFG and causes a Re-Configuration Trigger (RCT). This RCT effectuates the request to go to HIBERN8, which causes the LINE signal to switch from DIF-N to DIF-Z.

252 This sequence of events for this special case is illustrated in Figure 19.

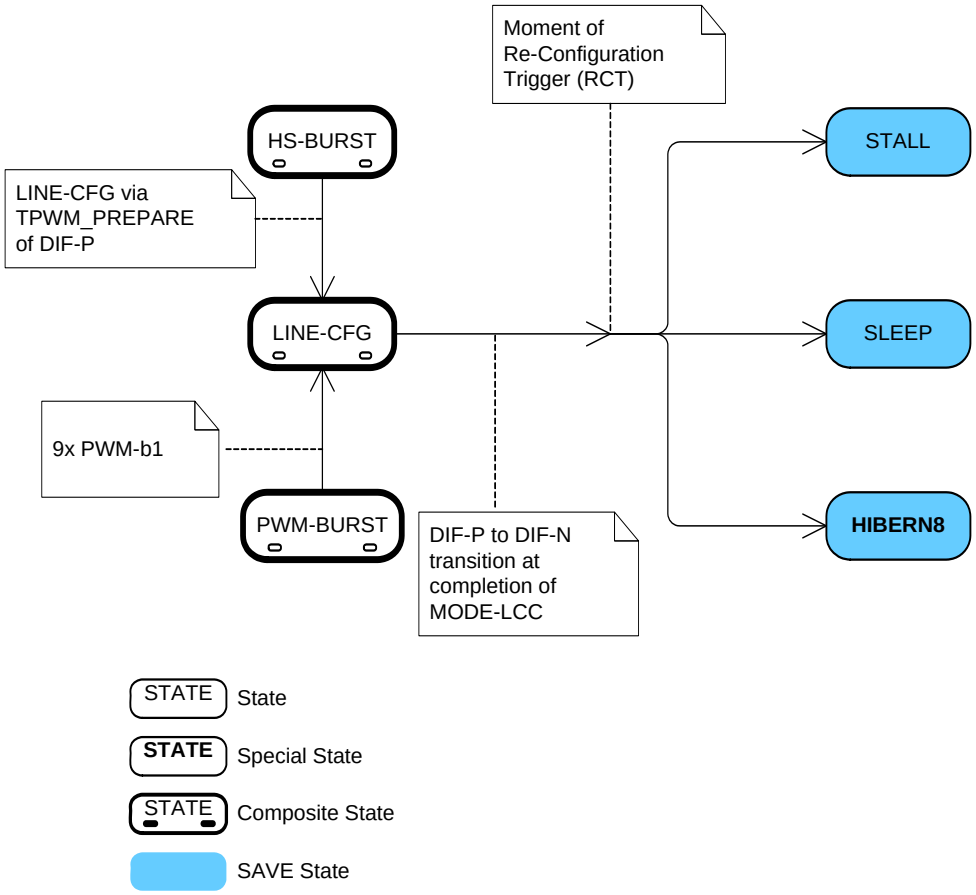


Figure 19 Re-Configuration Trigger after LINE-CFG

4.8 Configuration

253 MODULEs contain several optional modes, optional signaling features, and configurable parameter values. This provides much flexibility to this PHY technology. However, this requires a configuration mechanism to avoid interoperability problems. Minimum required functionality together with default configuration settings ensure that MODULEs of the same type shall always be able to communicate, implying a minimum level of interoperability. MODULEs can disclose their actual capabilities to the protocol. In combination with the dual-simplex minimum LINK constellation this enables negotiation between devices at each side of the LINK to discover commonly supported functionality and the most optimal configuration settings. This allows auto-discovery and configuration without accurate interface prescience at a higher level in the system, but requires a capability discovery, negotiation and selection mechanism in the protocol. This document assumes at least support from the protocol to select correct configuration settings, while the Physical Layer also supports auto-discovery and negotiation. Configuration information is interfaced with the protocol via a CONFIG interface that is part of the PIF.

4.8.1 Conceptual Configuration Process

254 MODULEs operate initially with default settings after OFF or LINE-RESET states. The protocol negotiates, determines and sets new configuration settings. This process consists of the following steps:

255 • Checking MODULE capabilities (optional)

- Determine desired, commonly supported configuration settings
- Change or request to change the PHY configuration settings

For reliably managing operation and its configuration settings, the following four types of registry are required:

- CAPABILITY registry (ROM)
  contains the capabilities of the MODULE. This is fixed information for a certain implementation.
- STATUS registry (alias INLINE-SET)
  contains current operational status and settings that immediately impact actual signaling. Not directly adaptable by the protocol, but is changed by the Physical Layer on request of the protocol via the INLINE-CR registry.
- INLINE-CR registry
  Logs change requests for configuration settings of INLINE parameters, that is, settings that immediately impact actual signaling.
- OFFLINE-SET registry
  Contains configuration settings which do not directly impact actual signaling

Because all MODULEs are specified independently in this document, this registry is ultimately required for every individual MODULE of a LINK. This might be simplified by protocol constraints on LANE composition and operating conditions. Note that which configuration settings are INLINE and OFFLINE depends on the actual state and mode of operation.

The configuration process is illustrated in Figure 20.

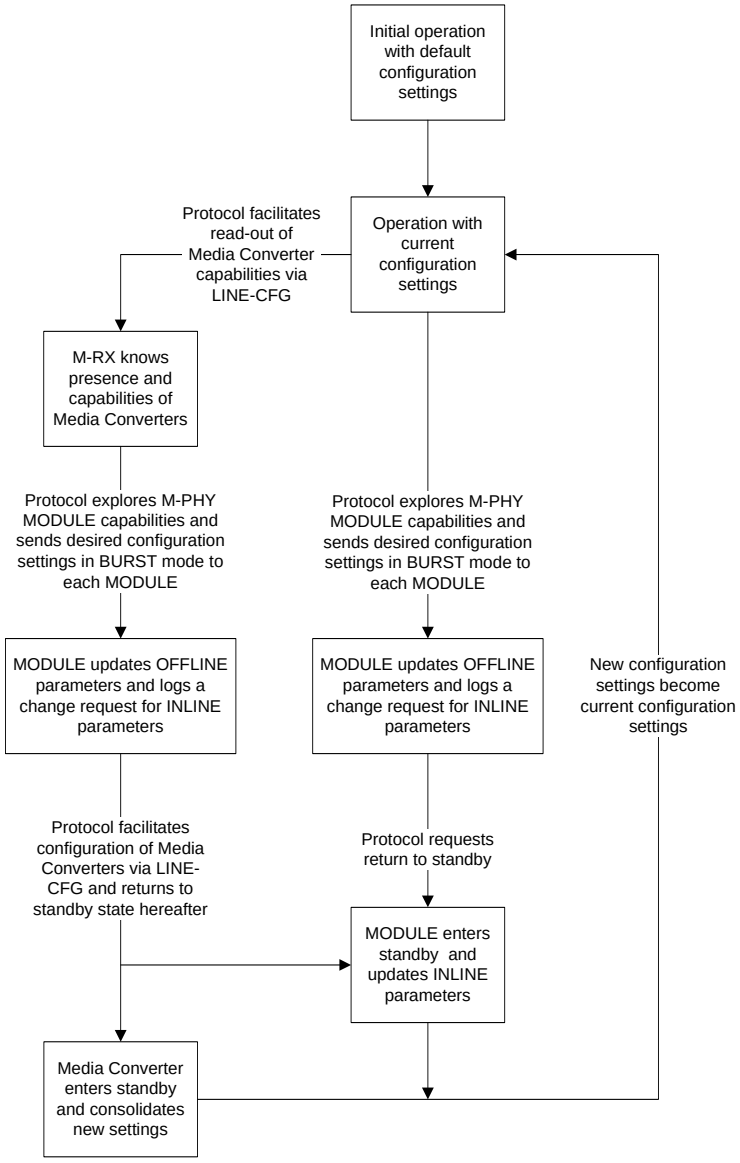


Figure 20 Configuration Flow Diagram

265 A supplementary low-level configuration mechanism based on LCCs can optionally be supported by the Physical Layer for configuration of Media Converters, which lack a Protocol Layer. This supplementary mechanism is intended to enhance to main configuration mechanism, not as a replacement. MODULEs are not re-configured via LINE-CONFIG.

4.8.1.1 Configuration without Media Converters

266 Figure 21 illustrates the steps of the configuration process for a LANE which does not include Media Converters (there may be invisible, non-constraining Media Converters, but these are, in this case, not part of the configuration process).

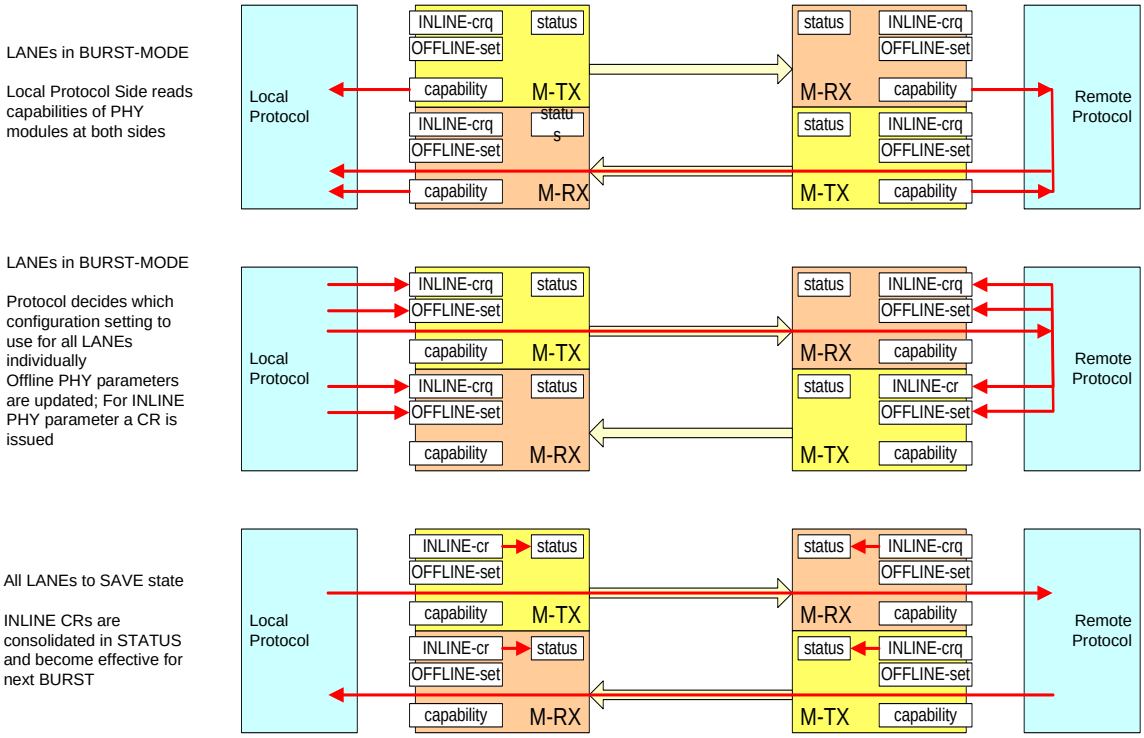


Figure 21 Configuration Steps for LANE

4.8.1.2 Configuration with Media Converters in the LINE

267 Figure 22 illustrates the steps of the configuration process for a LANE which includes configurable Media Converters in the LINE.

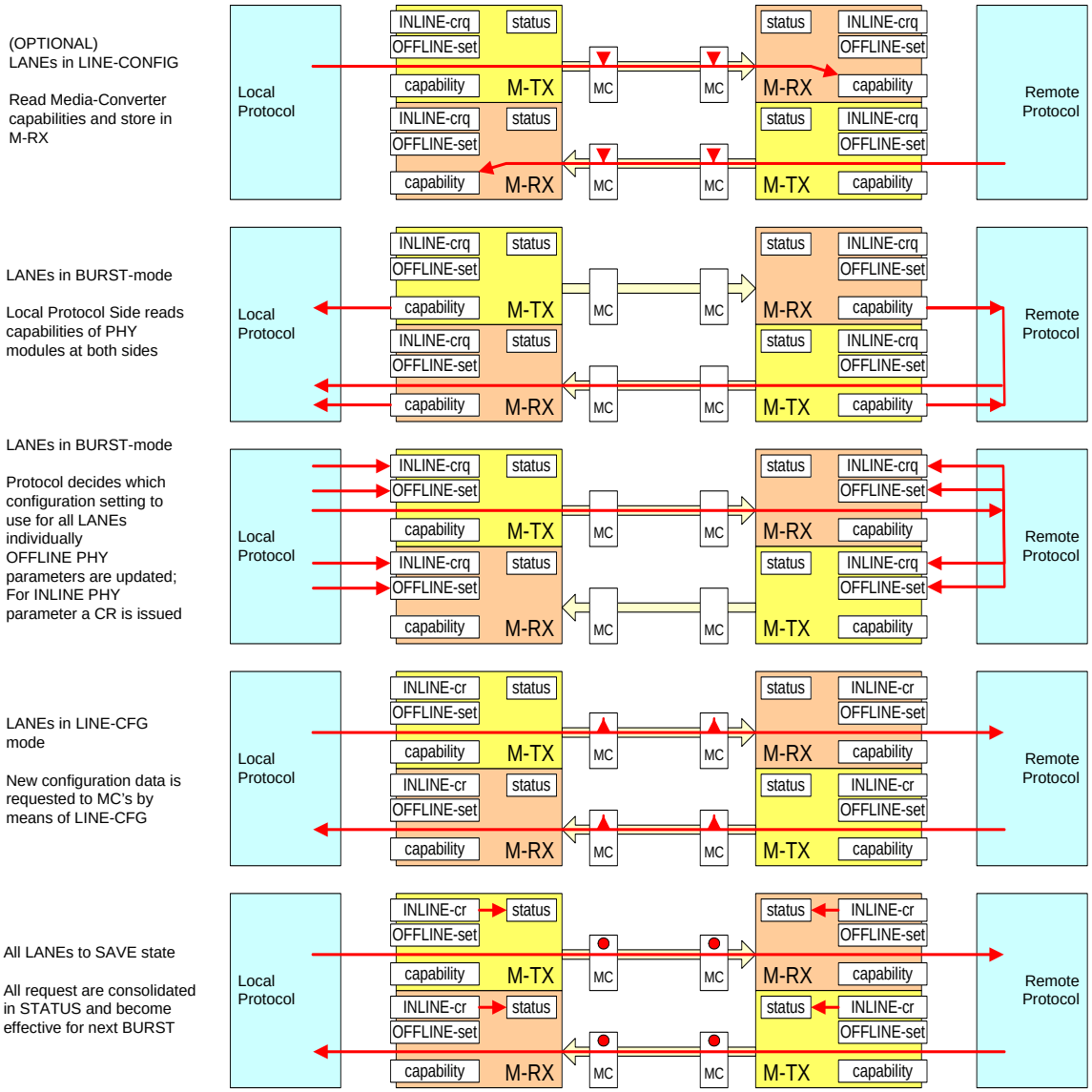


Figure 22 Configuration Steps for LANE including Media Converters

4.8.2 Configuration Parameters

268 Configuration attributes for MODULEs are listed in Section 8.4.

4.9 Multiple LANE Provisions

269 This document governs individual LANEs for a LINK. However, the LANE composition of a LINK is not specified by this document. This section specifies the provisions and constraints for multi-LANE SUB-LINK operation. This enables a multitude of possible LANE compositions for LINKs. The fine selection of allowed LANE combinations is left to the protocols on top of the Physical Layer.

270 There shall be no (tight) PHY-level requirements on timing alignment between SUB-LINKs.

271 Multiple LANEs within a SUB-LINK may be operated simultaneously with the same setting, or can be exploited independently in different states, depending on protocol usage of LANEs. There shall be no (tight) PHY-level requirements on timing alignment between LANEs of a SUB-LINKs that are operating under different conditions. When ACTIVATED, LANEs in a SUB-LINK in the same MODE shall be at the same rate. SUB-LINKs may be in different MODEs. In HS-MODE, both SUB-LINKs shall use the same HS rate series (A or B). SUB-LINKs may be operated in different GEARs. For example, one SUB-LINK may also operate in LS-MODE.

272 This document does not require functional symmetry of M-TXs and M-RXs for the SUB-LINKs of a LINK. However, for test purposes, protocols should exploit symmetric LINK composition.

273 The allocation of PAYLOAD data over multiple LANEs is left to the protocol specifications.

4.10 Test Modes

274 Test modes are special modes of operation which shall not happen during normal operation of a MODULE, which are intended to facilitate electrical, functional and protocol related tests. However, most tests can and should be executed using the normal operating modes. This document intends to cover test mode details in a separate section in the future. This section specifies specific architectural tweaks for special test modes, which cannot be accomplished within the normal operating modes.

4.10.1 LOOPBACK Mode

275 LOOPBACK mode provides a transparent bit-by-bit path from an M-RX input to an M-TX output. This can be done only for commonly supported MODE and GEAR settings for the involved M-RX and M-TX. If multiple M-RXs or M-TXs are present in a complete LINK, the mapping of which M-RX is looped via which M-TX is either specified by the applicable protocol specification or is otherwise left to the implementor. The Physical Layer is set into LOOPBACK mode via configuration.

276 LOOPBACK retransmits via the M-TX the encoded LINE data as recovered by the M-RX without decoding (and re-encoding) the 8b10b symbols. The configured setup in the mode is illustrated in Figure 23. Bypassing the coders avoids bit error multiplication. For any mandatory test condition, the input data provided to the M-RX shall be 8b10b encoded. Furthermore, an implementation should use symbol streams with characteristics similar to what happens in the real application. LOOPBACK mode can for example be used for BER testing.

277 Although this mode allows a test setup to inject a non-8b10b encoded bit stream for experimental purposes, there shall not be mandatory requirements on the functionality or performance of the Physical Layer in this case. Because HS-MODE utilizes embedded-clock data recovery, it is essential that any input bit stream in HS-LOOPBACK contains sufficient edge density.

278 For LOOPBACK the RATEs of M-RX and M-TX shall be identical, even though the MODULEs might be able to operate plesiochronously during normal operation. Note that this test mode is suitable to monitor the internal recovered bitstream of the M-RX on the outside via the M-TX, but not to characterize the M-TX performance.

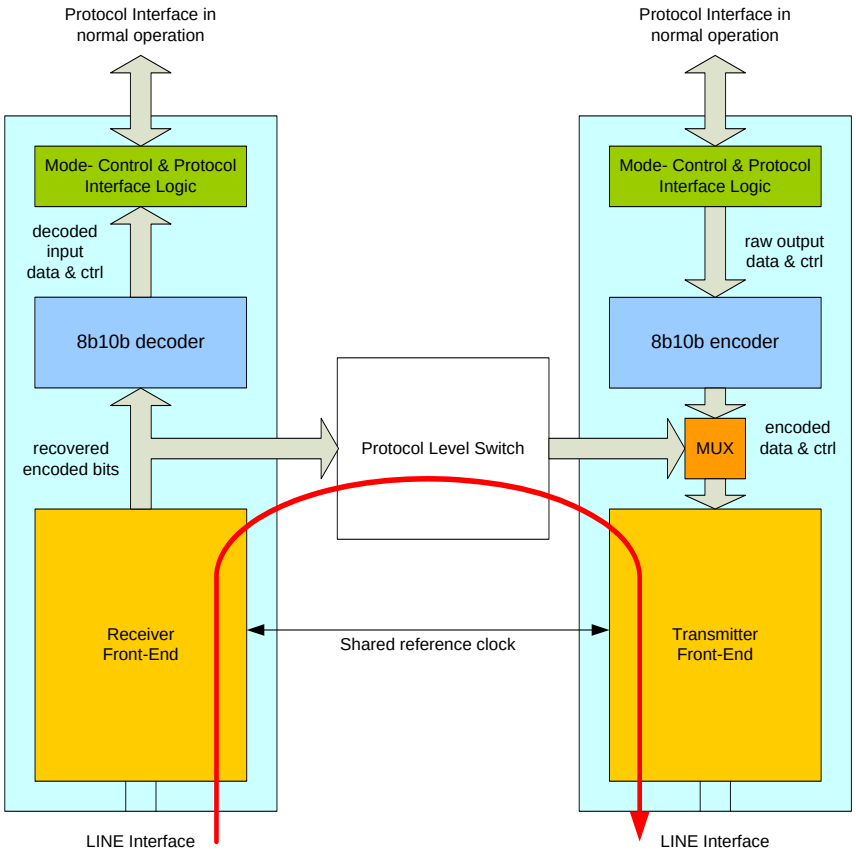


Figure 23 LOOPBACK Configuration

5 Electrical Characteristics

279 This section defines the electrical and low-level timing characteristics of M-TX and M-RX MODULEs. The definitions of the common MODULE characteristics are followed by specific characteristics for HS-MODE, PWM-MODE, and SYS-MODE operation. Finally, this section specifies the general PIN characteristics for MODULEs.

280 The definitions within this section refer to MODULEs in certain MODEs, which are referred to as FUNCTIONs. They are listed with their abbreviations in Table 12.

Table 12 FUNCTIONs and their Abbreviations

Abbreviation	FUNCTION
HS-TX	M-TX in HS-MODE
PWM-TX	M-TX in PWM-MODE
SYS-TX	M-TX in SYS-MODE
HS-RX	M-RX in HS-MODE
PWM-RX	M-RX in PWM-MODE
SYS-RX	M-RX in SYS-MODE
SQ-RX	M-RX in SQUELCH

281 The names of the FUNCTIONs correspond with the operational states of the M-TX and M-RX MODULEs as specified in Section 4.6.3. A MODULE does not need to support all FUNCTIONs, only those required for the intended application. FUNCTIONs required for an M-TX or an M-RX implementation are defined in Section 4.4, Section 4.6, Section 4.7 and higher level protocol standards. Also, the high level timing of the FUNCTIONs and their operation are defined in Section 4.

282 The electrical and timing characteristics of the M-TX and the M-RX MODULEs are defined at the PINs of an IC. Only MODULE characteristics that are observable at the PINs are subject to specification. These characteristics shall meet their specifications for any supported FUNCTION.

283 This specification is intended to be implementation agnostic. The section structure, which is based on FUNCTIONs, does not preclude integrated driver or receiver implementations. Although some figures in this section may suggest a certain driver or receiver implementation, they are used only for illustration purposes.

5.1 M-TX Characteristics

284 This document distinguishes three different operating modes and corresponding FUNCTIONs. Following the definition of the common M-TX electrical and timing characteristics, additional characteristics specific to HS-TX, PWM-TX, and SYS-TX are defined in this section.

5.1.1 Common M-TX Characteristics

285 The common electrical and timing characteristics of an M-TX are defined in this section, which also contains the PIN and signal definitions. The common M-TX characteristics apply to the HS-TX, PWM-TX, and SYS-TX FUNCTIONs.

5.1.1.1 PIN, Signal, and Reference Characteristic Definitions

286 An M-TX drives a low-voltage differential output signal at the PINs TXDP and TXDN either into a terminated, or an unterminated, load. TXDP and TXDN are defined as the positive and negative output PINs, respectively.

287 $V_{TXDP}(t)$ and $V_{TXDN}(t)$ are defined as the signal voltages at TXDP and TXDN with respect to ground. V_{TXDP} and V_{TXDN} are defined as the voltage amplitudes of the $V_{TXDP}(t)$ and $V_{TXDN}(t)$ signals, respectively.

288 $I_{TXDP}(t)$ and $I_{TXDN}(t)$ are defined as the output currents flowing out of TXDP and TXDN, respectively. I_{TXDP} and I_{TXDN} are defined as the current amplitudes of the $I_{TXDP}(t)$ and $I_{TXDN}(t)$ signals, respectively.

289 The PIN voltages and currents, as well as the reference loads R_{REF} and Z_{REF} are shown in Figure 24, where Z_{REF} is the reference load impedance looking into the reference load. R_{REF_RT} and R_{REF_NT} are the reference loads for the terminated and unterminated states, respectively.

290 Z_{REF} is the AC reference load limit which is bounded by the return loss SRL_{REF}. The reference load impedance Z_{REF} is defined having a minimum return loss SRL_{REF} for frequencies up to f_{HS_MAX}. SRL_{REF} is only defined for the terminated state, and can be calculated from the following equation:

$$SRL_{REF} = 20\log\left|\frac{Z_{REF} + Z_0}{Z_{REF} - Z_0}\right| \qquad \text{(Equation 1)}$$

291 where Z_0 is a defined characteristic impedance. C_{PAR} illustrates parasitic capacitance that contributes to Z_{REF}. C_{PAR} is not specified.

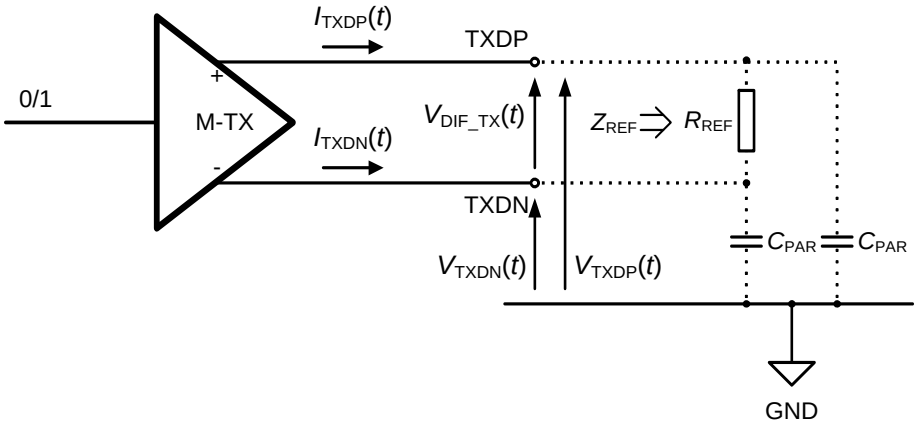


Figure 24 M-TX PIN Voltages, PIN Currents, and Reference Loads

292 An M-TX drives a differential low-swing signal with either Large Amplitude or Small Amplitude. The amplitude of the differential output signal is doubled when the M-TX drives an unterminated load compared to when it drives a terminated load. Differential output signals with large and small amplitudes for the terminated and unterminated states are shown in Figure 25. All single-ended voltage levels are relative to the ground voltage at the M-TX side.

293 The jitter of an HS-TX is specified by means of a bandpass filter with lower and upper cutoff frequencies f_{L_TX} and f_{U_TX}, respectively. An additional lower cutoff frequency $f_{L\_STJ\_TX}$ is defined for the short term jitter of an HS-TX.

294 The jitter is defined for the confidence limit, *CL*, of the distribution function of zero crossings of the differential M-TX output signal. The mean (μ) of the distribution function is located at 0.

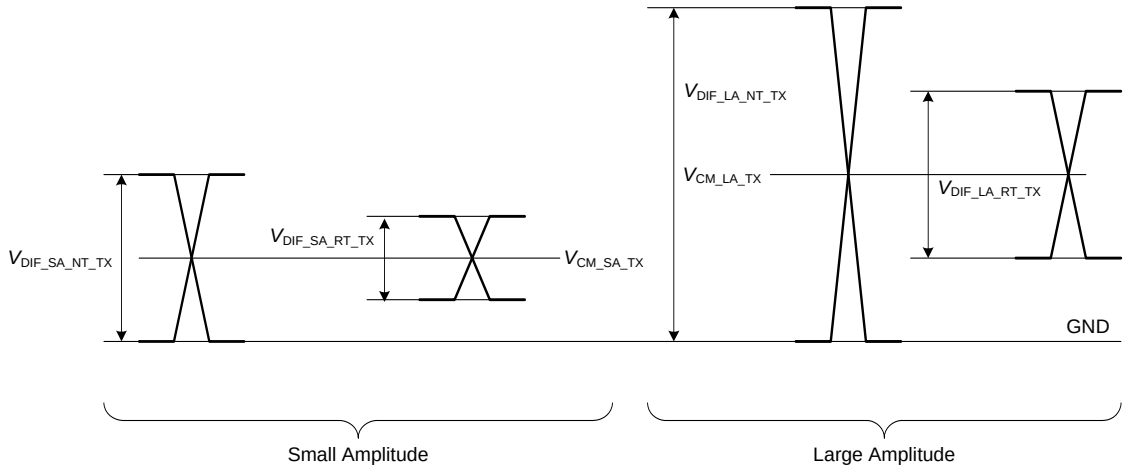


Figure 25 M-TX Signal Levels

295 The reference parameters for the M-TX are summarized in Table 13.

Table 13 M-TX Reference Parameters

Symbol	Values			Unit	Description
	Min.	Nom.	Max.		
Reference Load					
R_{REF_RT}		100		Ω	Reference load for terminated state.
R_{REF_NT}	10			kΩ	Reference load for unterminated state.
Z_0		100		Ω	Characteristic impedance.
Reference Return Loss					
SRL_{REF}	20			dB	Reference return loss for the terminated state. Defined for a characteristic impedance Z_0. Limit for AC reference load for frequencies up to f_{HS_MAX}.
Cutoff Frequency					
f_{L_TX}		1.0		MHz	Lower cutoff frequency of jitter bandpass filter.
$f_{L\_STJ\_TX}$		$\frac{1}{30UI_{HS}}$		Hz	Lower cutoff frequency of jitter bandpass filter for short term jitter.
f_{U_TX}		$\frac{1}{2UI_{HS}}$		Hz	Upper cutoff frequency of jitter bandpass filter.
Limit for BER					
CL	-6.36 σ		6.36 σ		Confidence limit.

5.1.1.2 Differential and Common-mode Voltage

296 An M-TX drives a differential signal on the TXDP and TXDN PINs. The differential output voltage signal $V_{DIF\_TX}(t)$ is defined as the difference of the voltage signals $V_{TXDP}(t)$ and $V_{TXDN}(t)$. V_{DIF_TX} is defined as the amplitude of $V_{DIF\_TX}(t)$. $V_{DIF\_TX}(t)$ can be calculated from the following equation:

$$V_{DIF\_TX}(t) = V_{TXDP}(t) - V_{TXDN}(t) \quad \text{(Equation 2)}$$

297 Separate AC and DC parameters are defined for V_{DIF_TX}. The DC parameter $V_{DIF\_DC\_TX}$ is defined for an M-TX which drives a steady DIF-N or a steady DIF-P LINE state into a reference load R_{REF}. An M-TX shall drive a differential DC output voltage amplitude which meets the specified limits of $V_{DIF\_DC\_TX}$.

298 The AC parameter $V_{DIF\_AC\_TX}$ is defined for an M-TX which drives a test pattern into a reference load R_{REF}, where the lower limit of $V_{DIF\_AC\_TX}$ is defined over the eye opening T_{EYE_TX} as defined in Section 5.1.2.8. The upper limit of $V_{DIF\_AC\_TX}$ is defined as the maximum differential output voltage, when the M-TX drives a test pattern into a reference load R_{REF}. An M-TX shall drive a differential AC output voltage signal which meets the specified limits of $V_{DIF\_AC\_TX}$.

299 The common-mode output voltage signal $V_{CM\_TX}(t)$ is defined as the arithmetic mean value of the signal voltages $V_{TXDP}(t)$ and $V_{TXDN}(t)$ when the M-TX drives a test pattern into a reference load R_{REF}. V_{CM_TX} is defined as the amplitude of $V_{CM\_TX}(t)$. $V_{CM\_TX}(t)$ can be calculated from the following equation:

$$V_{CM\_TX}(t) = \frac{V_{TXDP}(t) + V_{TXDN}(t)}{2} \quad \text{(Equation 3)}$$

300 An M-TX shall drive a common-mode output voltage signal which meets the specified limits of V_{CM_TX}.

301 $V_{DIF\_TX}(t)$ and $V_{CM\_TX}(t)$ for ideal single-ended output signals $V_{TXDP}(t)$ and $V_{TXDN}(t)$ are shown in Figure 26.

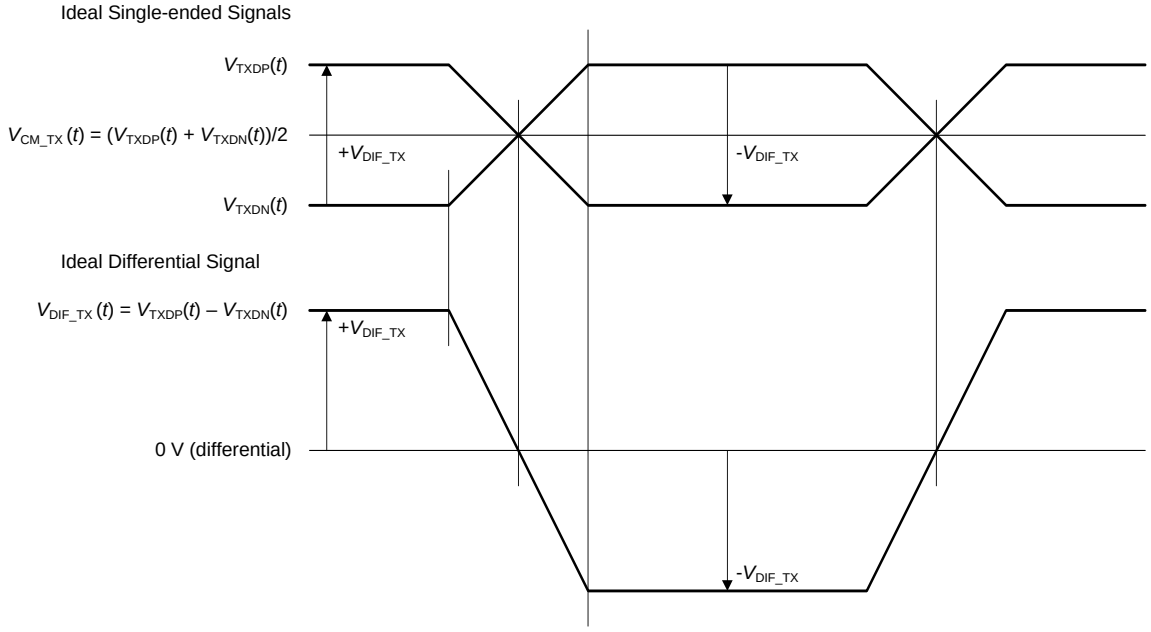


Figure 26 Ideal Single-ended and Differential Signals

5.1.1.3 Single-ended Output Resistance

302 The resistance R_{SE_TX} is defined as the single-ended output resistance of an M-TX at both its TXDP and TXDN PINs. R_{SE_TX} is defined for the case of a terminated M-TX that drives either a DIF-P or DIF-N LINE state with a reference load R_{REF} and a current source I connected between TXDP and TXDN as shown in Figure 27. A change of the current I results in a change of the PIN signal voltages V_{TXDP} and V_{TXDN}.

303 I_{REF} is defined as the value of the current source I that causes a variation of V_{TXDP} and V_{TXDN} by ±25 mV. ΔV_{TXDP} and ΔV_{TXDN} are defined as the peak-to-peak voltages of the signals at TXDP and TXDN, respectively, when the current source is swept between -I_{REF} and I_{REF}. ΔV_{CM_TX} is defined as the peak-to-peak voltage of the V_{CM_TX} signal shown in Figure 27, when the current source is swept between -I_{REF} and I_{REF}.

304 The single-ended output resistance shall conform with the specification limits of R_{SE_TX} for both the DIF-N and DIF-P state. An implementation should keep the output resistance during state transitions close to the steady state output resistance.

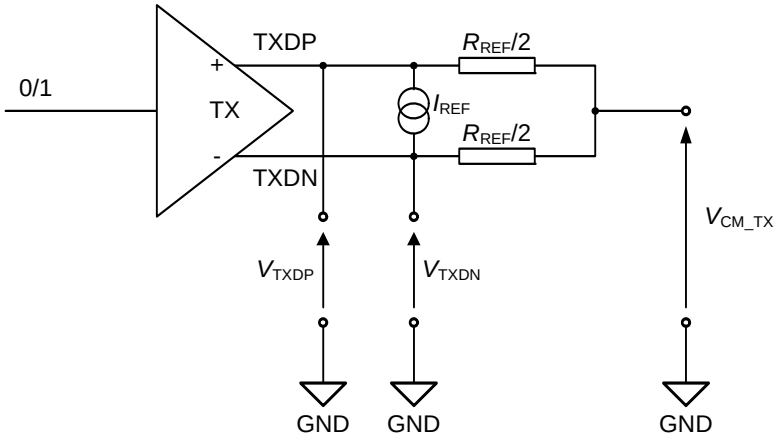


Figure 27 Measurement Setup for Single-ended Output Resistance

305 The single-ended output resistance R_{SE_TX} at TXDP can be calculated using the following equation:

$$R_{SE\_TX}(TXDP) = \frac{|\Delta V_{TXDP}|}{2I_{REF} - \frac{|\Delta V_{TXDP}| - |\Delta V_{CM\_TX}|}{R_{REF}/2}} \quad \text{(Equation 4)}$$

306 Similarly, the single-ended output resistance R_{SE_TX} at TXDN can be calculated using the following equation:

$$R_{SE\_TX}(TXDN) = \frac{|\Delta V_{TXDN}|}{2I_{REF} - \frac{|\Delta V_{TXDN}| - |\Delta V_{CM\_TX}|}{R_{REF}/2}} \quad \text{(Equation 5)}$$

307 $R_{SE\_PO\_TX}$ is defined as the single-ended output resistance of an M-TX in a STALL or SLEEP state at both the TXDP and TXDN PINs. $R_{SE\_PO\_TX}$ is defined for an M-TX, which drives either a DIF-N or a DIF-P LINE state, when a reference load R_{REF} is connected between TXDP and TXDN. The single-ended output resistance of an M-TX in the STALL or SLEEP states shall conform with the specified limit of $R_{SE\_PO\_TX}$.

308 V_{CM_TX} and V_{DIF_TX} shall stay in their specified limits during switching between R_{SE_TX} and $R_{SE\_PO\_TX}$. $R_{SE\_PO\_TX}$ is an optional feature of an M-TX, which is defined to allow for power optimization in the STALL and SLEEP states. If $R_{SE\_PO\_TX}$ is utilized, the single-ended output resistance shall conform with R_{SE_TX} at the exit of the STALL and SLEEP states.

309 $R_{SE\_PO\_TX}$ is defined according to R_{SE_TX}. Using the parameters of the R_{SE_TX} definition, the single-ended output resistance $R_{SE\_PO\_TX}$ at TXDP can be calculated using the following equation:

$$R_{SE\_PO\_TX}(\mathrm{TXDP}) = \frac{|\Delta V_{TXDP}|}{2I_{REF} - \frac{|\Delta V_{TXDP}| - |\Delta V_{CM\_TX}|}{R_{REF}/2}} \quad \text{(Equation 6)}$$

310 Similarly, the single-ended output resistance $R_{SE\_PO\_TX}$ at TXDN can be calculated from the following equation:

$$R_{SE\_PO\_TX}(\mathrm{TXDN}) = \frac{|\Delta V_{TXDN}|}{2I_{REF} - \frac{|\Delta V_{TXDN}| - |\Delta V_{CM\_TX}|}{R_{REF}/2}} \quad \text{(Equation 7)}$$

5.1.1.4 Return Loss

311 The return loss parameters are based on the S-parameter definition in Section 6.2. The common-mode transmitter return loss SCC_{TX} and the differential transmitter return loss SDD_{TX} are defined for an M-TX transmitting a repetitive test pattern consisting of a D.24.3+ followed by a D.24.3- symbol into a reference load R_{REF_RT}. When an M-TX supports Large Amplitude and Small Amplitude its SCC_{TX} and SDD_{TX} have to conform with the specification limits for both amplitudes. SCC_{TX} and SDD_{TX} are defined at the PINs such that they include contributions from the on-chip circuitry as well as from the package.

312 The SDD_{TX} template is shown in Figure 28 along with the return loss at corner frequencies f_{SYS_MAX}, f_{HS}, and f_{HS_MAX}. SCC_{TX} is defined for frequencies up to f_{HS_MAX}. An M-TX shall fulfill both the common-mode transmitter return loss SCC_{TX} and the differential transmitter return loss SDD_{TX} specification limits.

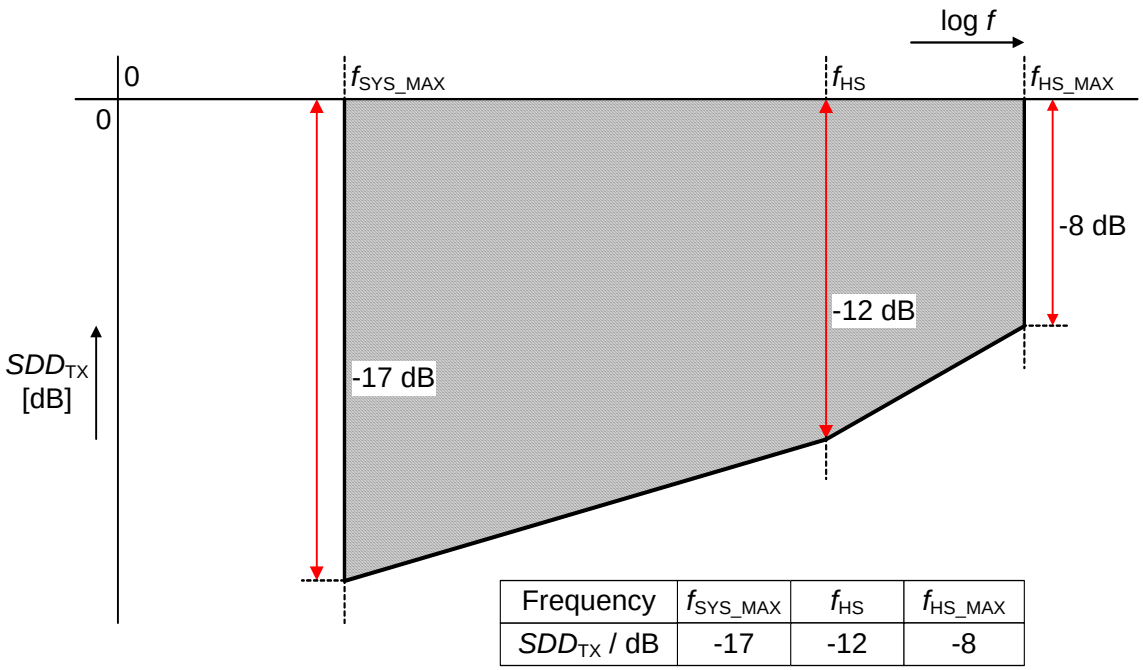


Figure 28 Template for Differential Transmitter Return Loss SDD_{TX}

5.1.1.5 LINE Disturbance during M-TX Power-up

313 An M-TX in a Type-I LINK shall not cause a LINE condition upon the transition from the UNPOWERED to a POWERED state which can be detected as a non-squelch state by the SQ-RX of the LANE. The allowed LINE disturbance upon such a transition of an M-TX is hence restricted by the squelch pulse rejection as defined in Section 5.2.6.

314 Squelch detection is not used in a Type-II LINK. Hence, there is no restriction of the LINE disturbance caused by an M-TX upon the transition from the UNPOWERED state to a POWERED state in such a LINK.

5.1.1.6 Common M-TX Parameters

315 The common electrical and timing parameters of an M-TX are listed in Table 14.

Table 14 Common M-TX Parameters

Symbol	Values		Unit	Description
	Min.	Max.		
M-TX Electrical				
$V_{DIF\_DC\_LA\_RT\_TX}$	160	240	mV	Large Amplitude differential TX DC voltage in a terminated state. Defined for R_{REF_RT}[1] and test pattern[2]. See Section 5.1.1.2.
$V_{DIF\_AC\_LA\_RT\_TX}$	140	250	mV	Large Amplitude differential TX AC voltage in a terminated state. Defined for R_{REF_RT}[1] and test pattern[3]. See Section 5.1.1.2.

Table 14 Common M-TX Parameters (continued)

Symbol	Values		Unit	Description
	Min.	Max.		
$V_{DIF\_DC\_LA\_NT\_TX}$	320	480	mV	Large Amplitude differential TX DC voltage in an unterminated state. Defined for R_{REF_NT}[4] and test pattern[2]. See Section 5.1.1.2.
$V_{DIF\_AC\_LA\_NT\_TX}$	280	500	mV	Large Amplitude differential TX AC voltage in an unterminated state. Defined for R_{REF_NT}[4] and test pattern[3]. See Section 5.1.1.2.
$V_{DIF\_DC\_SA\_RT\_TX}$	100	130	mV	Small Amplitude differential TX DC voltage in a terminated state. Defined for R_{REF_RT}[1] and test pattern[2]. See Section 5.1.1.2.
$V_{DIF\_AC\_SA\_RT\_TX}$	80	140	mV	Small Amplitude differential TX AC voltage in a terminated state. Defined for R_{REF_RT}[1] and test pattern[3]. See Section 5.1.1.2.
$V_{DIF\_DC\_SA\_NT\_TX}$	200	260	mV	Small Amplitude differential TX DC voltage in an unterminated state. Defined for R_{REF_NT}[4] and test pattern[2]. See Section 5.1.1.2.
$V_{DIF\_AC\_SA\_NT\_TX}$	160	280	mV	Small Amplitude differential TX AC voltage in an unterminated state. Defined for R_{REF_NT}[4] and test pattern[3]. See Section 5.1.1.2.
$V_{CM\_LA\_TX}$	160	260	mV	Large Amplitude common-mode TX voltage. Defined for R_{REF_RT}[1] and test pattern[2]. See Section 5.1.1.2.
$V_{CM\_SA\_TX}$	80	190	mV	Small Amplitude common-mode TX voltage. Defined for R_{REF_RT}[1] and test pattern[2]. See Section 5.1.1.2.
M-TX Resistance				
R_{SE_TX}	40	60	Ω	Single-ended output resistance. Defined for R_{REF_RT}[1] and test pattern[2]. See Section 5.1.1.3.
$R_{SE\_PO\_TX}$		500	Ω	Single-ended output resistance in STALL or SLEEP states. Defined for R_{REF_RT}[1] and test pattern[2]. See Section 5.1.1.3.
M-TX Return Loss				
SCC_{TX}		-6.0	dB	Common-mode transmitter return loss. Defined for R_{REF_RT}[1] up to f_{HS_MAX} and test pattern[5]. See Section 5.1.1.4.

1. *External reference load R_{REF_RT} and a reference impedance Z_{REF} which conforms to SRL_{REF}*
2. *Defined when driving both a DIF-N and a DIF-P LINE state.*

3. *Measurement based on accumulative eye diagram. Measurements are accomplished using the Compliant Random Pattern (CRPAT) and the Compliant Jitter Tolerance Pattern (CJTPAT). CRPAT and CJTPAT are defined in [INC01]. To obtain a specific measurement value, mean values of a series of measurements are calculated to fulfill a certain standard deviation of a given probability density function. For all measurements a certain settling time has to be taken into account. The differential voltage amplitude shall be measured as peak value utilizing representative data patterns. DC balanced patterns shall be used to avoid mean offsets.*
4. *External reference load R_{REF_NT} and capacitances at TXDP and at TXDN within the limit of C_{PIN}.*
5. *Defined for a repetitive test pattern of a D.24.3+ symbol followed by a D.24.3- symbol.*

5.1.2 HS-TX Characteristics

316 This section contains the electrical and timing characteristics specific to an HS-TX which are not covered by the common M-TX parameters in Section 5.1.1.

5.1.2.1 Rise and Fall Times

317 The HS-TX rise and fall times $T_{R\_HS\_TX}$ and $T_{F\_HS\_TX}$, respectively, are defined as transition times between the 20% and 80% signal levels of the differential HS-TX output signal, whose amplitude is defined by $V_{DIF\_DC\_TX}$, when driving a repetitive D.30.3 symbol sequence into a reference load R_{REF}. The minimum limits of $T_{R\_HS\_TX}$ and $T_{F\_HS\_TX}$ shall be met by an HS-TX when operated in HS-GEAR1. The maximum transition times are bounded by the HS-TX eye diagram specification.

5.1.2.2 Slew Rate

318 The slew rate SR_{DIF_TX} is defined as the ratio $\Delta V/\Delta T$, where ΔV is the absolute value of the voltage difference of the differential HS-TX output signal voltage measured at the 20% and 80% levels of $V_{DIF\_DC\_SA\_RT\_TX}$ and ΔT is the corresponding time difference when the HS-TX drives a reference load R_{REF} with Small Amplitude. The specification limits of SR_{DIF_TX} shall be met by an HS-TX that supports slew rate control and which is operated in HS-G1.

319 The slew rate of the HS-TX should be controllable to allow for N different slew rate states. $SR_{DIF\_TX}[1]$ and $SR_{DIF\_TX}[N]$ denominate the slew rate for the fastest and for the slowest slew rate states, respectively. The number N is implementation-specific and is out of scope for this document. The slew rate states should cover a range defined by the maximum slew rate SR_{DIF_TX}[MAX] and the minimum slew rate SR_{DIF_TX}[MIN]. For at least one state the slew rate should be larger than SR_{DIF_TX}[MAX]. For at least one state it should be smaller than SR_{DIF_TX}[MIN].

320 The slew rate shall be monotonically decreasing when stepping from faster to slower slew rate states, i.e., $SR_{DIF\_TX}[i]$ is larger than $SR_{DIF\_TX}[i+1]$, where i is in the range of 1 to N-1. It shall be monotonically increasing when stepping from slower to faster slew rate states. The tolerance of a slew rate state is not defined. Different slew rate states may overlap, but shall not violate the monotonicity requirement.

321 The resolution of the slew rate states ΔSR_{DIF_TX} is defined as the difference of the slew rates of two adjacent slew rate states divided by the slew rate of the slower state.

322 ΔSR_{DIF_TX} can be calculated using the following equation:

$$\Delta SR_{DIF\_TX} = \frac{SR_{DIF\_TX}[i] - SR_{DIF\_TX}[i+1]}{SR_{DIF\_TX}[i+1]} \quad \text{(Equation 8)}$$

323 where $SR_{DIF\_TX}[i+1]$ is the slew rate of the slower slew rate state and $SR_{DIF\_TX}[i]$ is the slew rate of the adjacent faster slew rate state. ΔSR_{DIF_TX} shall be met between $SR_{DIF\_TX}[1]$ and $SR_{DIF\_TX}[N]$.

5.1.2.3 Intra-differential Output Skew

324 The intra-differential transmitter output skew T_{SKEW_TX} is defined as the time between the intersections of the single-ended output signals $V_{TXDP}(t)$ and $V_{TXDN}(t)$ with the averaged common-mode voltage V_{CM_TX}, when the HS-TX drives a test pattern into a reference load R_{REF}. The intra-differential transmitter output skew shall be in the specification limits of T_{SKEW_TX}. A skew of the single-ended output signals results in a common-mode voltage ripple as illustrated in Figure 29.

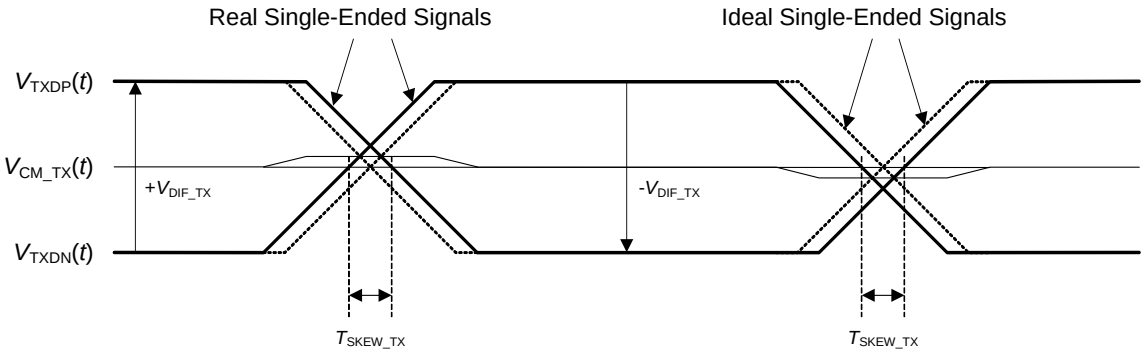


Figure 29 Impact of Signal Skew on Common-mode

5.1.2.4 LANE-to-LANE Skew

325 The HS-TX LANE-to-LANE skew $T_{L2L\_HS\_TX}$ is defined as the time between the zero crossings of the differential output signals $V_{DIF\_TX}(t)$ of any two HS-TXs in one SUB-LINK, when both HS-TX drive a test pattern into identical reference loads R_{REF}. The value of $T_{L2L\_HS\_TX}$ is outside the scope of this document. If required, it shall be defined in the protocol specification.

5.1.2.5 Output Resistance Mismatch

326 The HS-TX output resistance mismatch ΔR_{SE_TX} is defined as the difference of the single-ended output resistances R_{SE_TX} at the TXDP and TXDN PINs, when the HS-TX drives either a steady DIF-N or DIF-P LINE state into a reference load R_{REF}. R_{SE_TX} is defined in Section 5.1.1.3.

327 ΔR_{SE_TX} can be calculated from the following equation:

$$\Delta R_{SE\_TX} = R_{SE\_TX}(\mathrm{TXDP}) - R_{SE\_TX}(\mathrm{TXDN}) \qquad \text{(Equation 9)}$$

328 where R_{SE_TX}(TXDP) is the output resistance driving either a DIF-N or a DIF-P and R_{SE_TX}(TXDN) is the output resistance driving either a DIF-N or a DIF-P such that Equation 9 has to be evaluated for four cases. The HS-TX output resistance mismatch shall be in the limits of ΔR_{SE_TX} for all four cases.

329 Transmitter output signal mismatch, as well as the transmitter output gain mismatch, originates from ΔR_{SE_TX}. The transmitter output gain mismatch definition is out of scope for this document. A transmitter output signal mismatch results in different signal transition times as well as in different differential DC output voltages $V_{DIF\_DC\_TX}$ when driving a DIF-P or a DIF-N LINE state. Both effects cause a ripple of V_{CM_TX}. An example of a V_{CM_TX} ripple is illustrated in Figure 30.

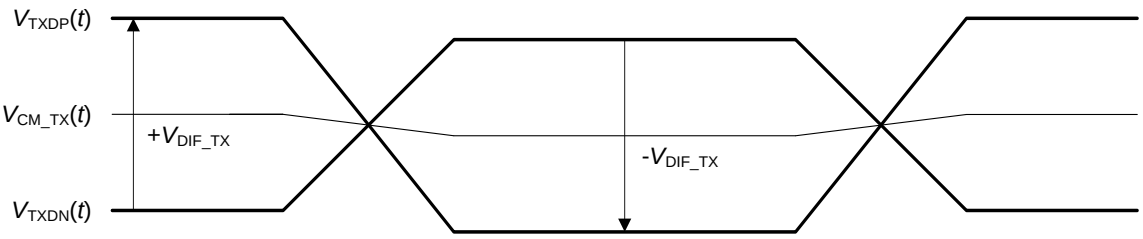


Figure 30 Impact of Output Signal Mismatch on Common-mode Voltage

5.1.2.6 Transmitter Pulse Width

330 The transmitter pulse width T_{PULSE_TX} of an HS-TX differential output signal is defined as the time between the zero crossings of a single bit of the differential output signal $V_{DIF\_TX}(t)$ when driving a test pattern into a reference load R_{REF}. The transmitter pulse width of an HS-TX output signal shall conform with the lower limit of T_{PULSE_TX}.

5.1.2.7 Transmitter Jitter

331 To ensure interoperability among the components that comprise an end-to-end LANE, the jitter budget must be adhered to by the M-TX, the M-RX, and possibly a reference clock. The tolerance for the LINE is indirectly defined by the jitter specifications, the voltage margins, the eye opening at the M-TX output, and by the receiver tolerance.

332 The transmitter total jitter TJ_{TX} is a convolution of the deterministic jitter DJ_{TX} and the random jitter RJ_{TX} of the differential output signal $V_{DIF\_TX}(t)$ of the HS-TX. TJ_{TX} is the sum of the arithmetic sum of the deterministic jitter contributions $DJ_{TX}[j]$, where $DJ_{TX}[j]$ are peak-to-peak values, and the square root of the sum of squared random jitter contributions $RJ_{TX}[i]$ multiplied by two times the Q-factor Q_{BER}, which is a constant depending on the BER. For instance, a BER of 10^{-10} relates to a Q-factor $Q_{BER} = \pm 6.36$.

333 TJ_{TX} can be calculated using following equation:

$$TJ_{TX} = \sum_{j} DJ_{TX}[j] + 2Q_{BER}\sqrt{\sum_{i} RJ_{TX}[i]^2} \qquad \text{(Equation 10)}$$

334 Using the dual-Dirac model, TJ_{TX} can be expressed by the following equation:

$$TJ_{TX} = DJ_{TX}(\delta\delta) + 2Q_{BER}\sigma \qquad \text{(Equation 11)}$$

335 where $DJ_{TX}(\delta\delta)$ is the time between two Dirac pulses and σ is the standard deviation of the Gaussian random jitter of the HS-TX. $DJ_{TX}(\delta\delta)$ is the dual-Dirac model for the deterministic jitter of the HS-TX and σ is the model for the random jitter of the HS-TX. Further details of the dual-Dirac jitter model are described in [INC01].

336 This specification defines the TJ_{TX} and the $DJ_{TX}(\delta\delta)$. In addition the short term total jitter $STTJ_{TX}$ and the short term deterministic jitter $STDJ_{TX}(\delta\delta)$, which limit the jitter within a $30UI_{HS}$ signal sequence, are specified due to the BURST type of HS-MODE transmissions.

337 Raw jitter can contain low or high frequency jitter, which is irrelevant for the HS-TX operation. Hence, the raw jitter has to be processed by a step bandpass filter function $H_{TX}(f)$ with a a lower and upper cutoff frequency f_{L_TX} and f_{U_TX}, respectively, as shown in the following equation:

$$H_{TX}(f) = \begin{cases} 1 & f_{L\_TX} \le f \le f_{U\_TX} \\ < 10^{-3} & \text{else} \end{cases} \quad \text{(Equation 12)}$$

338 A similar step bandpass filter function $H_{STJ\_TX}(f)$ is defined for the short term jitter with a different lower cutoff frequency $f_{L\_STJ\_TX}$. $H_{STJ\_TX}(f)$ is shown in the following equation:

$$H_{STJ\_TX}(f) = \begin{cases} 1 & f_{L\_STJ\_TX} \le f \le f_{U\_TX} \\ < 10^{-3} & \text{else} \end{cases} \quad \text{(Equation 13)}$$

339 The transmitter total jitter TJ_{TX} is defined for the differential output signal $V_{DIF\_TX}(t)$ at the zero crossings when the HS-TX is driving a CJTPAT test pattern into a reference load R_{REF}. The transmitter total jitter of an HS-TX when filtered using the $H_{TX}(f)$ bandpass function shall conform with the limits of TJ_{TX}.

340 In case of a short LINE, the LINE contributes less jitter within the LANE. Hence, the jitter requirement of the HS-TX is relaxed in this case. A transmitter short LINE total jitter TJ_{SL_TX} is defined similar to TJ_{TX}. In case of a short LANE the transmitter short LINE total jitter of an HS-TX shall conform with the limits of TJ_{SL_TX}.

341 The transmitter deterministic jitter $DJ_{TX}(\delta\delta)$ is defined for the differential output signal $V_{DIF\_TX}(t)$ at the zero crossings when the HS-TX is driving a CJTPAT test pattern into a reference load R_{REF}. The transmitter deterministic jitter of an HS-TX when filtered using the $H_{STJ\_TX}(f)$ bandpass function shall conform with the limits of $DJ_{TX}(\delta\delta)$.

342 The transmitter short term total jitter $STTJ_{TX}$ is defined for the differential output signal $V_{DIF\_TX}(t)$ at the zero crossings when the HS-TX is driving a CJTPAT test pattern into a reference load R_{REF}. The transmitter short term total jitter of an HS-TX shall conform with the limits of $STTJ_{TX}$.

343 The transmitter short term deterministic jitter $STDJ_{TX}(\delta\delta)$ is defined for the differential output signal $V_{DIF\_TX}(t)$ at the zero crossings when the HS-TX is driving a CJTPAT test pattern into a reference load R_{REF}. The transmitter short term total jitter of an HS-TX shall conform with the limits of $STDJ_{TX}(\delta\delta)$.

5.1.2.8 Transmitter Eye Opening

344 The transmitter eye opening T_{EYE_TX} is defined as the duration in an eye diagram over which the absolute value of the differential HS-TX output signal is larger than the lower limit of $V_{DIF\_AC\_TX}$ when the HS-TX transmits a test pattern into a reference load R_{REF}. This situation is shown in Figure 31. The absolute value of the HS-TX differential output voltage signal shall be larger than the lower limit of $V_{DIF\_AC\_TX}$ over the transmitter eye opening T_{EYE_TX}. The position of T_{EYE_TX} within the eye is not specified.

345 The parameters shown in Figure 31 are based on the accumulated eye for the required confidence limit, where the total transmit jitter TJ_{TX} is defined around the mean of the zero crossings of the differential HS-TX output voltage signal.

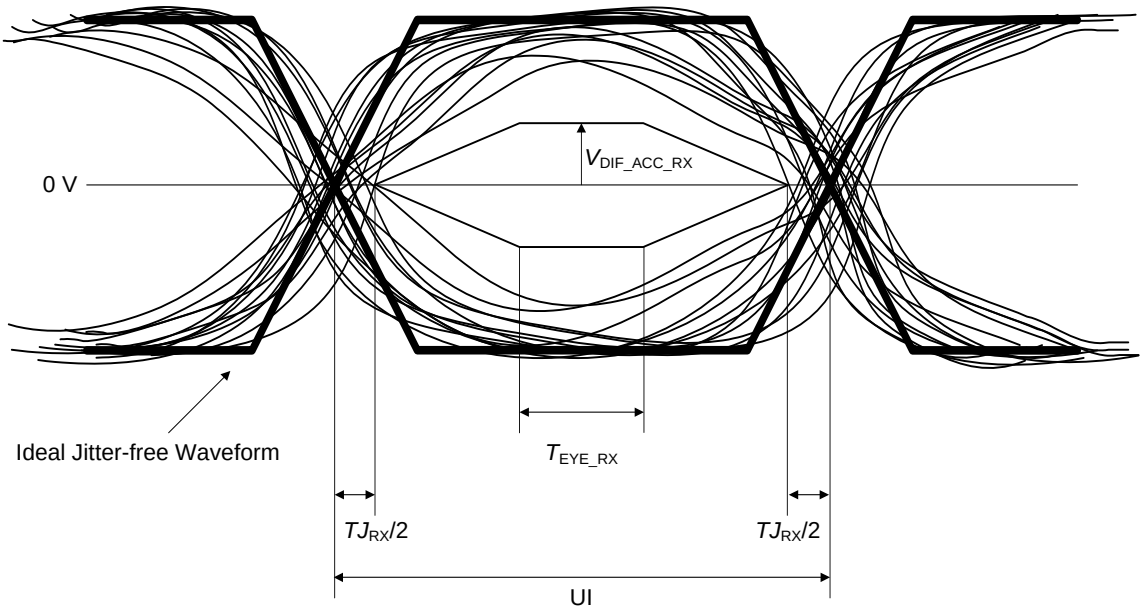


Figure 31 Differential Transmit Eye Diagram

5.1.2.9 Power Spectral Magnitude Limit

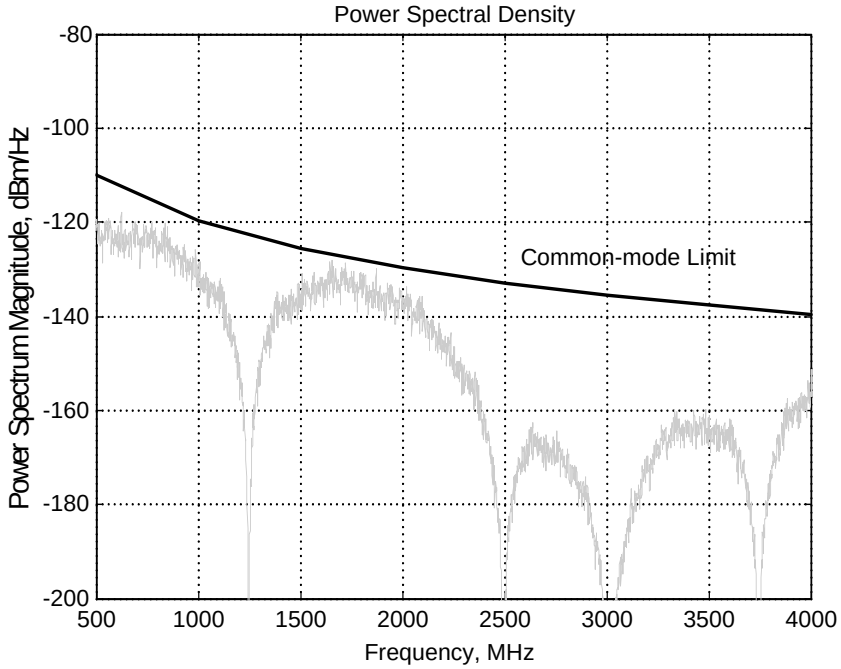
346 A power spectral magnitude limit is defined for the common-mode interference spectrum. A method of acquiring the common-mode interference spectrum of an HS-TX is also defined.

5.1.2.9.1 Common-mode Power Spectral Magnitude Limit

347 Slew rate control is an effective means of limiting electromagnetic interference (EMI) of an HS-TX at its output PINs. Its power spectral density, and thus the level of interference, can be controlled by the slew rate of the HS-TX signal waveform. Smaller slew rates result in a significant suppression of high frequency content of the HS-TX output power spectral density. The slew rate limit is application-specific and interconnect-dependent.

348 The common-mode interference spectrum of the HS-TX is impacted by the intra-differential timing skew of the single-ended output signals at TXDP and TXDN as well as by gain mismatches of the HS-TX.

349 A common-mode power spectral magnitude limit is defined along with a method of generating the spectra of an HS-TX. In order for an HS-TX to meet the common-mode power spectral magnitude limit, a slew rate control might be necessary. The common-mode power spectral magnitude limit is given in the table, and illustrated by the solid curve, in Figure 32. The common-mode interference spectrum shall be below this limit. This limit can be achieved by proper slew rate setting as well as by proper restrictions on intra-differential timing skew and output resistance mismatch. For illustration purposes the common-mode power-spectral density of an 8b10b coded common-mode interference signal (gray curve) is also shown in Figure 32. This curve does not show the spurs at the fundamental frequency nor at the harmonics of the data signal. The suppression of these spurs is not restricted by the common-mode limit.



Common-Mode Limit

F, MHz	Limit, dBm/Hz
500	-109.9
1000	-119.8
1500	-125.6
2000	-129.7
2500	-132.9
3000	-135.5
3500	-137.7
≥4000	-139.6

Figure 32 Common-mode Power Spectral Magnitude Limit

5.1.2.9.2 Spectrum Generation Method

350 The method of acquiring the common-mode interference spectrum of an HS-TX can be applied both in simulation and measurement. The method is described in the following list:

351 • The operating condition of the HS-TX shall be chosen such that it results in the maximum amplitude for the selected amplitude setting in a terminated state with a reference load R_{REF}. In case the HS-TX is operated with Small Amplitude, the temperature, supply voltage, and process shall be selected to result in a maximum HS-TX amplitude. This does not imply that the investigation has to be performed with Large Amplitude instead of Small Amplitude.

352 • The simulation test pattern shall be a PRBS9 sequence, which is not 8b10b coded, with at least seven repetitions. The PRBS9 pattern is defined by $1 + X^5 + X^9$. When the method is applied in a measurement setup, no specific test pattern is defined. Regular signal sequences should be used.

353 • The HS-TX common-mode signal $V_{CM\_TX}(t)$ is calculated from the $V_{TXDP}(t)$ and $V_{TXDN}(t)$ signals.

354 • FFT of the common-mode signal with a Hamming window results in the interference spectrum, which has to be adjusted for the relevant bandwidth.

355 • Slew rate shall be adjusted such that the common-mode interference spectrum complies with the power spectral magnitude limit, for the data rate the HS-TX is operated. With this setting the HS-TX shall also fulfill the transmit jitter and the transmit eye specification.

5.1.2.10 Transmitter Frequency Offset

356 The transmitter frequency offset f_{OFFSET_TX} is defined as the difference of the actual HS-TX frequency from the nominal HS-TX frequency f_{HS}. f_{OFFSET_TX} is defined at the zero crossings of the differential HS-TX output signal when driving a test pattern into a reference load R_{REF}. The transmitter frequency offset of an HS-TX shall conform with the limits of f_{OFFSET_TX}.

5.1.2.11 HS-TX Parameters

357 The electrical and timing parameters specific to an HS-TX are summarized in Table 15.

Table 15 HS-TX Parameters

Symbol	Values		Unit	Description
	Min.	Max.		
HS-TX Timing				
$T_{F\_HS\_TX}$	0.1		UI_{HS}	Fall time. Defined for R_{REF_RT}[1] and R_{REF_NT}[2] and test pattern[3]. See Section 5.1.2.1.
$T_{R\_HS\_TX}$	0.1		UI_{HS}	Rise time. Defined for R_{REF_RT}[1] and R_{REF_NT}[2] and test pattern[3]. See Section 5.1.2.1.
SR_{DIF_TX}[MAX]	0.9		V/ns	Maximum slew rate. Defined in HS-GEAR1 for $V_{DIF\_DC\_SA\_RT\_TX}$[4], R_{REF_RT}[5], and test pattern[6]. See Section 5.1.2.2.
SR_{DIF_TX}[MIN]		0.35	V/ns	Minimum slew rate. Defined in HS-GEAR1 for $V_{DIF\_DC\_SA\_RT\_TX}$[4], R_{REF_RT}[5], and test pattern[6]. See Section 5.1.2.2.
ΔSR_{DIF_TX}	1	30	%	Resolution of slew rate states. Defined in HS-GEAR1 for $V_{DIF\_DC\_SA\_RT\_TX}$[4], R_{REF_RT}[5], and test pattern[6]. See Section 5.1.2.2.
T_{SKEW_TX}	-0.06	0.06	UI_{HS}	Intra-differential skew. Defined for R_{REF_RT}[1] and R_{REF_NT}[2] and test pattern[6]. See Section 5.1.2.3.
T_{PULSE_TX}	0.9		UI_{HS}	Transmitter pulse width. Defined for R_{REF_RT}[1] and R_{REF_NT}[2] and test pattern[6]. See Section 5.1.2.6.
HS-TX Resistance				
ΔR_{SE_TX}	-6	6	Ω	Output resistance mismatch. Defined for R_{REF_RT}[1] and R_{REF_NT}[2] when driving DIF-N and DIF-P. See Section 5.1.2.5.
HS-TX Jitter				
T_{EYE_TX}	0.2		UI_{HS}	Transmitter eye opening[7]. Defined for R_{REF_RT}[1] and R_{REF_NT}[2] and test pattern[6] over a statistical confident record set[8]. See Section 5.1.2.8.
$DJ_{TX}(\delta\delta)$		0.15	UI_{HS}	Transmitter deterministic jitter[9]. Defined for R_{REF_RT}[1] and R_{REF_NT}[2] and test pattern[6] for a statistical confident record set[8,10]. See Section 5.1.2.7.

Table 15 HS-TX Parameters (continued)

Symbol	Values		Unit	Description
	Min.	Max.		
TJ_{TX}		0.32	UI_{HS}	Transmitter total jitter[9]. Defined for R_{REF_RT}[1] and R_{REF_NT}[2] and test pattern[6] for a statistical confident record set[8,10]. See Section 5.1.2.7.
TJ_{SL_TX}		0.40	UI_{HS}	Transmitter short LINE total jitter[9]. Defined for R_{REF_RT}[1] and R_{REF_NT}[2] and test pattern[6] for a statistical confident record set[8,10]. See Section 5.1.2.7.
$STDJ_{TX}(\delta\delta)$		0.10	UI_{HS}	Transmitter short term deterministic jitter[9]. Defined for R_{REF_RT}[1] and R_{REF_NT}[2] and test pattern[6] for a statistical confident record set[10,11]. See Section 5.1.2.7.
$STTJ_{TX}$		0.20	UI_{HS}	Transmitter short term total jitter[9]. Defined for R_{REF_RT}[1] and R_{REF_NT}[2] and test pattern[6] for a statistical confident record set[10,11]. See Section 5.1.2.7.
f_{OFFSET_TX}	-2000	2000	ppm	Transmitter frequency offset. Defined for R_{REF_RT}[1] and R_{REF_NT}[2] and test pattern[6]. See Section 5.1.2.10.

1. *External reference load R_{REF_RT} and a reference impedance Z_{REF} which conforms to SRL_{REF}.*
2. *External reference load R_{REF_NT} and capacitances at TXDP and at TXDN within the limit of C_{PIN}.*
3. *Repetitive sequence of D.30.3 symbols to be used for test. Such a sequence is part of CJTPAT.*
4. *Values are specified for Small Amplitude. For Large Amplitude the slew rate is a factor of 1.85 larger.*
5. *External reference load R_{REF_RT} and a reference impedance Z_{REF} which conforms to SRL_{REF}. The slew rate is only specified for the terminated state. In unterminated state slew rate control is not strictly required due to smaller LINE power. However, slew rate control may also be used in the unterminated state, but it is not specified how this performs in this case.*
6. *CRPAT and CJTPAT to be used for test.*
7. *For slower slew rate settings the transmitter eye mask may be violated.*
8. *Filtered using a reference tracking function equivalent to a bandpass from f_{L_TX} up to f_{U_TX}.*
9. *Accumulated jitter as defined by the dual-Dirac model.*
10. *Measured over a confidence interval, CL, of the distribution function of zero crossings of the differential output signal.*
11. *Filtered using a reference tracking function equivalent to a bandpass from $f_{L\_STJ\_TX}$ up to f_{U_TX}.*

5.1.3 PWM-TX Characteristics

358 This section contains timing characteristics specific to a PWM-TX which are not covered by the common M-TX characteristics in Section 5.1.1. The PWM signaling scheme is defined in Section 4.3.2.

5.1.3.1 PWM Bit Duration, Bit Duration Tolerance, and Ratio

359 A PWM bit consists out of a DIF-N LINE state followed by a DIF-P LINE state, which are either signaled for the minor duration $T_{PWM\_MINOR\_TX}$ or for the major duration $T_{PWM\_MAJOR\_TX}$. The durations $T_{PWM\_MINOR\_TX}$ and $T_{PWM\_MAJOR\_TX}$ are defined as the time between the zero crossings of the differential output signal.

360 The PWM transmit bit duration T_{PWM_TX} is defined as the duration between zero crossings of two consecutive falling edges of a differential signal at the PWM-TX output. $T_{PWM\_MINOR\_TX}$, $T_{PWM\_MAJOR\_TX}$, and T_{PWM_TX} are shown in Figure 33. The PWM transmit bit duration T_{PWM_TX} is for all PWM GEARs the sum of its durations $T_{PWM\_MINOR\_TX}$ and $T_{PWM\_MAJOR\_TX}$, as shown in the following equation:

$$T_{PWM\_TX} = T_{PWM\_MINOR\_TX} + T_{PWM\_MAJOR\_TX} \quad \text{(Equation 14)}$$

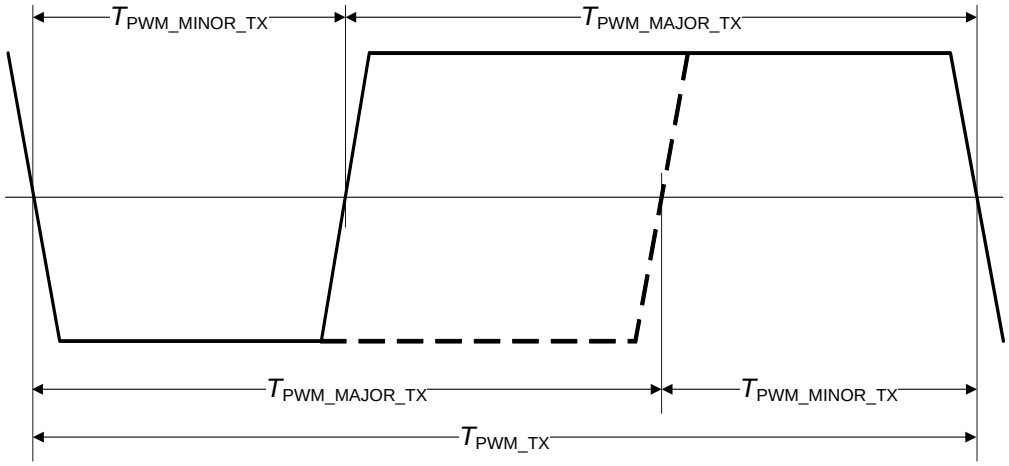


Figure 33 TX Minor and Major Duration in a PWM Signal

361 $T_{PWM\_MINOR\_TX}$ and $T_{PWM\_MAJOR\_TX}$ are determined by T_{PWM_TX} and the PWM transmit ratio k_{PWM_TX} for PWM-G1 and higher PWM GEARs. k_{PWM_TX} is defined as the ratio of $T_{PWM\_MAJOR\_TX}$ and $T_{PWM\_MINOR\_TX}$ of one PWM bit, as shown in the following equation:

$$k_{PWM\_TX} = \frac{T_{PWM\_MAJOR\_TX}}{T_{PWM\_MINOR\_TX}} \quad \text{(Equation 15)}$$

362 For PWM-G0 the minor duration $T_{PWM\_G0\_MINOR\_TX}$ is directly specified. The range of $T_{PWM\_G0\_MINOR\_TX}$ is defined based on the minor duration in PWM-G1.

363 The PWM transmit bit duration tolerance $TOL_{PWM\_G1\_TX}$ is the allowed tolerance of an instantaneous PWM bit duration $T_{PWM\_TX}(i)$ during a LINE-READ state. $TOL_{PWM\_G1\_TX}$ is defined as the ratio of $T_{PWM\_TX}(i)$ and the average of N PWM transmit bit durations during LINE-READ, as shown in the following equation:

$$TOL_{PWM\_G1\_TX} = \frac{T_{PWM\_TX}(i)}{\frac{1}{N}\sum_{i=1}^{N} T_{PWM\_TX}(i)} \quad \text{(Equation 16)}$$

364 where N is a defined number of PWM bits, and i is in the range of 1 to N.

365 While the T_{PWM_TX} range is wide for a PWM GEAR, $TOL_{PWM\_G1\_TX}$ limits the variation of an instantaneous PWM transmit bit duration $T_{PWM\_TX}(i)$ during a LINE-READ state. $TOL_{PWM\_G1\_TX}$ is not defined for other states during a PWM-BURST than LINE-READ.

366 A PWM-TX shall output a PWM signal whose PWM transmit bit duration T_{PWM_TX} is in the specified range of the operational PWM-GEAR during a PWM-BURST. For PWM-G1 and higher GEARs the PWM transmit ratio k_{PWM_TX} shall be in the specified range for each PWM bit. For PWM-G0 the minor duration $T_{PWM\_MINOR\_G0\_TX}$ shall be in the specified range for each PWM bit.

367 A PWM-TX shall output a PWM signal whose PWM transmit bit duration tolerance is in the limits of $TOL_{PWM\_G1\_TX}$ during LINE-READ in PWM-G1.

5.1.3.2 Rise and Fall Time

368 The PWM-TX rise and fall times $T_{R\_PWM\_TX}$ and $T_{F\_PWM\_TX}$, respectively, are defined as transition times between the 20% and 80% signal levels of the differential SYS-TX output signal, whose amplitude is defined by V_{DIF_TX}, when driving a reference load R_{REF}. The rise and fall times of a PWM-TX shall comply with the limits of $T_{R\_PWM\_TX}$ and $T_{F\_PWM\_TX}$.

5.1.3.3 LANE-to-LANE Skew

369 The PWM-TX LANE-to-LANE skew $T_{L2L\_PWM\_TX}$ is defined as the time between the zero crossings of the falling edges of the differential output signals $V_{DIF\_TX}(t)$ of any two PWM-TXs in one SUB-LINK, when both PWM-TX drive a test pattern into identical reference loads R_{REF}. The value of $T_{L2L\_PWM\_TX}$ is outside the scope of this document. If required, it shall be defined in the protocol specification.

5.1.3.4 PWM-TX Parameters

370 The timing parameters specific to a PWM-TX are summarized in Table 16.

Table 16 PWM-TX Parameters

Symbol	Values		Unit	Description
	Min.	Max.		
$T_{PWM\_G0\_TX}$	1 / 3	1 / 0.01	µs	PWM transmit bit duration in PWM-G0. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.3.1.
$T_{PWM\_G1\_TX}$	1 / 9	1 / 3	µs	PWM transmit bit duration in PWM-G1. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.3.1.
$T_{PWM\_G2\_TX}$	1 / 18	1 / 6	µs	PWM transmit bit duration in PWM-G2. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.3.1.
$T_{PWM\_G3\_TX}$	1 / 36	1 / 12	µs	PWM transmit bit duration in PWM-G3. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.3.1.
$T_{PWM\_G4\_TX}$	1 / 72	1 / 24	µs	PWM transmit bit duration in PWM-G4. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.3.1.

Table 16 PWM-TX Parameters (continued)

Symbol	Values		Unit	Description
	Min.	Max.		
$T_{PWM\_G5\_TX}$	1 / 144	1 / 48	µs	PWM transmit bit duration in PWM-G5. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.3.1.
$T_{PWM\_G6\_TX}$	1 / 288	1 / 96	µs	PWM transmit bit duration in PWM-G6. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.3.1.
$T_{PWM\_G7\_TX}$	1 / 576	1 / 192	µs	PWM transmit bit duration in PWM-G7. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.3.1.
$TOL_{PWM\_G1\_TX}$	0.90	1.10		PWM transmit bit duration tolerance in PWM-G1. Defined for R_{REF_NT}[1] and test pattern[2] during LINE-READ. See Section 5.1.3.1.
N	50			Number of PWM bits. Defined for R_{REF_NT}[1] and test pattern[2] during LINE-READ. See Section 5.1.3.1.
$T_{PWM\_G0\_MINOR\_TX}$	1 / 27	1 / 9	µs	PWM transmit minor duration in PWM-G0. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.3.1.
k_{PWM_TX}	0.63 / 0.37	0.72 / 0.28		PWM transmit ratio for PWM-G1 and higher PWM GEARs. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.3.1.
$T_{R\_PWM\_TX}$		0.070	T_{PWM_TX}	Rise time. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.3.2.
$T_{F\_PWM\_TX}$		0.070	T_{PWM_TX}	Fall time. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.3.2.

1. *External reference load R_{REF_NT} and capacitances at TXDP and at TXDN within the limit of C_{PIN}. If terminated state is supported external reference load R_{REF_RT} and a reference impedance Z_{REF} which conforms to SRL_{REF} has to be verified additionally.*
2. *Test pattern CJTPAT.*

5.1.4 SYS-TX Characteristics

371 This section contains timing characteristics specific to a SYS-TX which are not covered by the common M-TX characteristics in Section 5.1.1.

5.1.4.1 Rise and Fall Times

372 The SYS-TX rise and fall times $T_{R\_SYS\_TX}$ and $T_{F\_SYS\_TX}$, respectively, are defined as transition times between the 20% and 80% signal levels of the differential SYS-TX output signal, whose amplitude is defined by V_{DIF_TX}, when driving a repetitive D.30.3 symbol sequence into reference load R_{REF}. The rise and fall times of a SYS-TX shall comply with the limits of $T_{R\_SYS\_TX}$ and $T_{F\_SYS\_TX}$.

5.1.4.2 LANE-to-LANE Skew

373 The SYS-TX LANE-to-LANE skew $T_{L2L\_SYS\_TX}$ is defined as the time between the zero crossings of the differential output signals $V_{DIF\_TX}(t)$ of any two SYS-TXs in one SUB-LINK, when both SYS-TX drive a test pattern into identical reference loads R_{REF}. The value of $T_{L2L\_SYS\_TX}$ is outside the scope of this document. If required, it shall be defined in the protocol specification.

5.1.4.3 Data-to-Clock Skew

374 A system synchronous clocking scheme is used in the SYS-BURST mode, an example of which is shown in Figure 14. Since the reference clock is not considered to be a part of an M-PORT, definition of the clock characteristics is outside the scope of this specification. Parameters like the reference clock frequency, the duty cycle distortion of the reference clock signal, or the rise and fall times of the reference clock signal have to be covered in the protocol specification utilizing the M-Phy technology.

375 The data-to-clock skew between the data signals of a SYS-TX and the reference clock signal has also to be defined in the protocol specification, such that no unnecessary limitations for the clocking scheme or system timing are put forth by this specification. This leaves maximum flexibility to the protocol specification, which only has to adhere to the zero crossing of the SYS-TX output signal, when it is driving a reference load R_{REF}, as reference timing point for such a definition. The data-to-clock skew has to be defined for both SUB-LINKs. Interoperability in SYS-BURST mode thus has partly to be ensured by the protocol specification.

376 There might be applications for which a data-to-clock skew cannot be defined, e.g. in case of an external reference clock signal. In such a case, the propagation delay between the external reference clock signal and the SYS-TX data signals has to be defined in the protocol specification.

377

5.1.4.4 SYS-TX Parameters

378 The timing parameters specific to a SYS-TX are summarized in Table 17.

Table 17 SYS-TX Parameters

Symbol	Values		Unit	Description
	Min.	Max.		
$T_{R\_SYS\_TX}$		0.20	UI_{SYS}	Rise time. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.4.1.
$T_{F\_SYS\_TX}$		0.20	UI_{SYS}	Fall time. Defined for R_{REF_NT}[1] and test pattern[2]. See Section 5.1.4.1.

1. *External reference load R_{REF_NT} and capacitances at TXDP and at TXDN within the limit of C_{PIN}. If terminated state is supported external reference load R_{REF_RT} and a reference impedance Z_{REF} which conforms to SRL_{REF} has to be verified additionally.*
2. *Repetitive sequence of D.30.3 symbols to be used for test. Such a sequence is part of CJTPAT.*

5.2 M-RX Characteristics

379 This document distinguishes three different operating modes and corresponding FUNCTIONs. Following the definition of the common M-RX electrical and timing characteristics, which apply to HS-RX, PWM-RX, and SYS-RX, additional characteristics, which are specific to each receive FUNCTION, are defined in this section. The SQ-RX, which is an optional FUNCTION of an M-RX, is defined at the end of this section.

5.2.1 Common M-RX Characteristics

380 The common electrical and timing characteristics of an M-RX are defined in this section, which also contains the PIN and signal definitions. The common M-RX characteristics apply to the HS-RX, PWM-RX, and SYS-RX FUNCTIONs.

5.2.1.1 PIN, Signal, and Reference Characteristic Definitions

381 RXDP and RXDN are the input PINs of the M-RX MODULE. RXDP is defined as the positive input PIN and RXDN as the negative input PIN.

382 $V_{RXDP}(t)$ and $V_{RXDN}(t)$ are defined as the voltage signals at these PINs with respect to ground. V_{RXDP} and V_{RXDN} are defined as the voltage amplitudes of the $V_{RXDP}(t)$ and $V_{RXDN}(t)$ signals, respectively.

383 $I_{RXDP}(t)$ and $I_{RXDN}(t)$ are defined as the input currents flowing into RXDP and RXDN, respectively. I_{RXDP} and I_{RXDN} are defined as the current amplitudes of the $I_{RXDP}(t)$ and $I_{RXDN}(t)$ signals, respectively.

384 $I_{RXPN}(t)$ is defined as the current, which flows from RXDP to RXDN, in case the termination resistor is enabled. I_{RXPN} is defined as the current amplitude of $I_{RXPN}(t)$.

385 The PIN voltages and currents are shown in Figure 34.

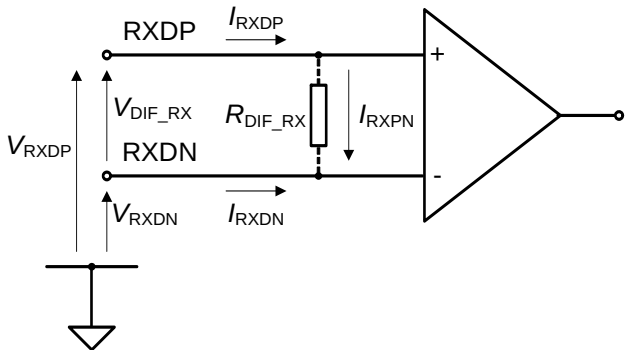


Figure 34 PIN Voltages and PIN Currents of an M-RX

386 The M-RX contains a differential line receiver which supports the detection of M-TX signals having Large Amplitude as well as Small Amplitude. An M-RX has only to support FUNCTIONs required for the targeted application. An M-RX may contain a switchable differential termination resistor R_{DIF_RX} between its input PINs RXDP and RXDN for improving the signal integrity. It is defined in Section 4.7.2, when R_{DIF_RX} shall be enabled or disabled. When R_{DIF_RX} is enabled the M-RX is operated in the terminated state, otherwise it is operated in the unterminated state.

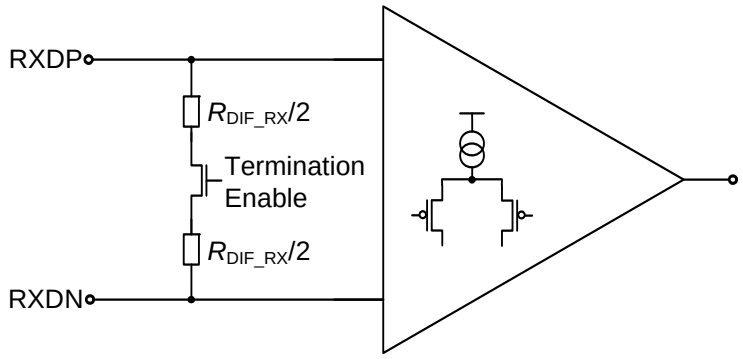


Figure 35 M-RX Implementation Example

387 A simplified diagram of an example implementation using a PMOS input stage is shown in Figure 35. The common-mode voltage of the LINE has to remain in the common-mode voltage limits upon switching of the termination resistor. This is achievable through an AC ground at the center tap of the termination resistor, for example, by use of a capacitor.

388 The jitter tolerance of an M-RX is specified for a frequency range limited by the lower and upper frequencies f_{L_RX} and f_{U_RX}, respectively. An additional lower frequency $f_{L\_STJ\_TX}$ is defined for the short term jitter of an M-RX.

389 Discrete test frequencies f_{SJ1_RX}, f_{SJ2_RX}, f_{SJ3_RX}, f_{SJ4_RX}, and f_{SJ5_RX} are defined for the sinusoidal jitter tolerance. f_{SJ3_RX} is the system clock frequency of the chip, which in case of a Type-II M-Port may be different than f_{SYS_CLK}.

390 The jitter is defined for the confidence limit, *CL*, of the distribution function of zero crossings of a differential test signal at the M-RX input. The mean (μ) of the distribution function is located at 0.

391 The reference parameters for the M-RX are summarized in Table 18.

Table 18 M-RX Reference Parameters

Symbol	Values			Unit	Description
	Min.	Nom.	Max.		
Frequency					
f_{L_RX}		1.0		MHz	Lower frequency for jitter tolerance.
$f_{L\_STJ\_RX}$		$\frac{1}{30UI_{HS}}$		Hz	Lower frequency for short term jitter tolerance.
f_{U_RX}		$\frac{1}{2UI_{HS}}$		Hz	Upper frequency for jitter tolerance.
f_{SJ1_RX}		1.0		MHz	Test frequency for sinusoidal jitter tolerance.
f_{SJ2_RX}		10		MHz	Test frequency for sinusoidal jitter tolerance.

Table 18 M-RX Reference Parameters (continued)

Symbol	Values			Unit	Description
	Min.	Nom.	Max.		
f_{SJ3_RX}		f_{SYSTEM}		Hz	Test frequency for sinusoidal jitter tolerance. Frequency of system clock.
f_{SJ4_RX}		$\frac{1}{30UI_{HS}}$		Hz	Test frequency for sinusoidal jitter tolerance.
f_{SJ5_RX}		$\frac{1}{5UI_{HS}}$		Hz	Test frequency for sinusoidal jitter tolerance.
f_{SJ6_RX}		$\frac{1}{2UI_{HS}}$		Hz	Test frequency for sinusoidal jitter tolerance.
Limit for BER					
CL	-6.36 σ		6.36 σ		Confidence limit.

5.2.1.2 Differential and Common-mode Voltage

392 The differential input voltage signal $V_{DIF\_RX}(t)$ is defined as the difference of the voltage signals $V_{RXDP}(t)$ and $V_{RXDN}(t)$ at the M-RX PINs. V_{DIF_RX} is defined as the amplitude of $V_{DIF\_RX}(t)$. $V_{DIF\_RX}(t)$ can be calculated from the following equation:

$$V_{DIF\_RX}(t) = V_{RXDP}(t) - V_{RXDN}(t) \quad \text{(Equation 17)}$$

393 The minimum value of V_{DIF_RX} defines the minimum differential voltage amplitude of a test pattern an M-RX has to receive while the maximum value of V_{DIF_RX} defines the maximum differential voltage amplitude of a test pattern an M-RX has to receive.

394 The receiver common-mode voltage signal $V_{CM\_RX}(t)$ is defined as the arithmetic mean value of the voltage signals $V_{RXDP}(t)$ and $V_{RXDN}(t)$ when a test pattern is applied at the M-RX input PINs. V_{CM_RX} is defined as the amplitude of $V_{CM\_RX}(t)$. $V_{CM\_RX}(t)$ can be calculated from the following equation:

$$V_{CM\_RX}(t) = \frac{V_{RXDP}(t) + V_{RXDN}(t)}{2} \quad \text{(Equation 18)}$$

395 The V_{CM_RX} parameter values are defined such that they cover DC deviations, which can, e.g., be caused by a ground shift between an M-TX and an M-RX or by an output signal mismatch of the M-TX.

396 An M-RX shall detect a differential input signal at its RXDP and RXDN PINs with a differential voltage amplitude in the range of V_{DIF_RX} and with common-mode voltage in the range of V_{CM_RX}.

5.2.1.3 Termination Resistance

397 An M-RX may contain a switchable differential termination resistor RDIF_RX. RDIF_RX is defined by the ratio of the difference of the PIN voltage amplitudes VRXDP and VRXDN and the current amplitude IRXPN, which flows from RXDP to RXDN, when the differential input voltage amplitude and the receiver common-mode voltage are both in the range of VDIF_RX and VCM_RX, respectively.

398 R_{DIF_RX} can be calculated from the following equation:

$$R_{DIF\_RX} = \frac{V_{RXDP} - V_{RXDN}}{I_{RXPN}} \quad \text{(Equation 19)}$$

399 The termination resistance shall conform with the limits of R_{DIF_RX}.

5.2.1.4 Differential Termination Switching Time

400 If an M-RX contains a differential termination resistor, it detects from the LINE state, when R_{DIF_RX} has to be enabled or disabled, as defined in Section 4.7.2.

401 The differential termination enable time $T_{TERM\_ON\_RX}$ is defined as the time from the zero crossing of the triggering DIF-N to DIF-P transition until the time when the differential input voltage reaches the evaluation level $V_{TERM\_ON\_EVAL}$, where $V_{TERM\_ON\_EVAL}$ is defined as the 20% level of the voltage difference in the unterminated and terminated state as shown by the following equation:

$$V_{TERM\_ON\_EVAL} = 0.2(V_{DIF\_NT\_RX} - V_{DIF\_RT\_RX}) \quad \text{(Equation 20)}$$

402 The differential termination enable time shall conform with the limit of $T_{TERM\_ON\_RX}$.

403 R_{DIF_RX} is disabled through different triggering events for the HS-MODE, the PWM-MODE, and the SYS-MODE. This results in three different definitions of the differential termination disabled time. All termination disable times are defined using an evaluation level $V_{TERM\_OFF\_EVAL}$, which is defined as the 80% level of the voltage difference in the unterminated and terminated state as shown by the following equation:

$$V_{TERM\_OFF\_EVAL} = 0.8(V_{DIF\_NT\_RX} - V_{DIF\_RT\_RX}) \quad \text{(Equation 21)}$$

404 In HS-MODE, the differential termination disable time $T_{TERM\_OFF\_HS\_RX}$ is defined as the time starting after $20UI_{HS}$ following a MARKER2 until the time when the differential input voltage reaches $V_{TERM\_OFF\_EVAL}$. The differential termination disable time shall conform with the limit of $T_{TERM\_OFF\_HS\_RX}$ in HS-MODE.

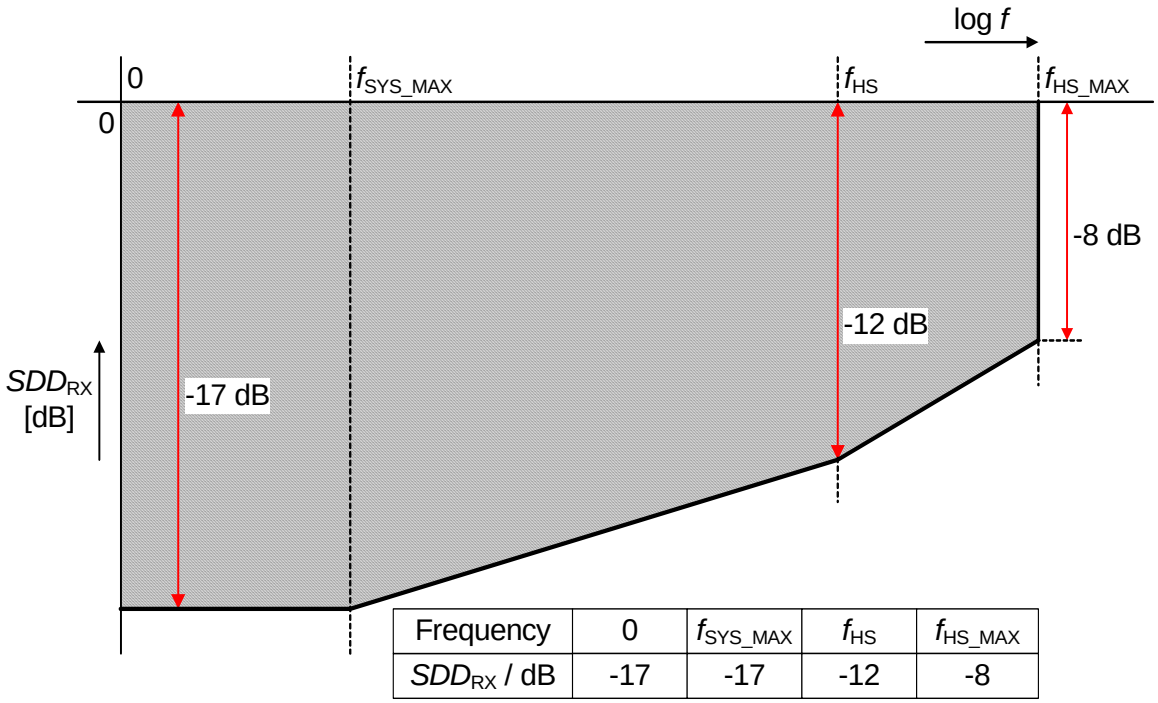
405 In PWM-MODE, the differential termination disable time $T_{TERM\_OFF\_PWM\_RX}$ is defined as the time starting after $9T_{PWM\_RX}$ following a MARKER2 until the time when the differential input voltage reaches $V_{TERM\_OFF\_EVAL}$. The differential termination disable time shall conform with the limit of $T_{TERM\_OFF\_HS\_RX}$ in PWM-MODE.

406 In SYS-MODE, the differential termination disable time $T_{TERM\_OFF\_SYS\_RX}$ is defined as the time starting after $10UI_{SYS}$ following a MARKER2 until the time when the differential input voltage reaches $V_{TERM\_OFF\_EVAL}$. The differential termination disable time shall conform with the limit of $T_{TERM\_OFF\_SYS\_RX}$ in SYS-MODE.

5.2.1.5 Return Loss

407 The receiver return loss parameter is based on the S-parameter definition in <<<TBD section>>>. The differential receiver return loss SDD_{RX} is defined for an M-RX whose termination resistor is enabled. SDD_{RX} is defined at the PINs such that it includes contributions from the on-chip circuitry as well as from the package. In the unterminated state the PIN capacitance should be limited by C_{PIN_RX}.

408 The SDD_{RX} template is shown in Figure 36 along with the return loss values at certain corner frequencies f_{SYS_MAX}, f_{HS}, and f_{HS_MAX}. The differential receiver return loss of an M-RX shall conform with the specification limits of SDD_{RX}.



Frequency	0	f_{SYS_MAX}	f_{HS}	f_{HS_MAX}
SDD_{RX} / dB	-17	-17	-12	-8

Figure 36 Template for Differential Receiver Return Loss SDD_{RX}

5.2.2 Common M-RX Parameters

409 The common electrical and timing parameters of an M-RX are summarized in Table 19.

Table 19 Common M-RX Parameters

Symbol	Values		Unit	Description
	Min.	Max.		
M-RX Electrical				
$V_{DIF\_RT\_RX}$	60	245	mV	Differential RX voltage amplitude in terminated state. Defined for test pattern. Defined for test pattern[1]. See Section 5.2.1.2.
$V_{DIF\_NT\_RX}$	120	490	mV	Differential RX voltage amplitude in unterminated state. Defined for test pattern[1]. See Section 5.2.1.2.
V_{CM_RX}	25	330	mV	RX common-mode voltage[2]. Defined for test pattern[1]. See Section 5.2.1.2.
M-RX Resistance				
R_{DIF_RX}	80	110	Ω	Differential input resistance[3]. Defined over V_{DIF_RX} range. See Section 5.2.1.3.

Table 19 Common M-RX Parameters (continued)

Symbol	Values		Unit	Description
	Min.	Max.		
M-RX Timing				
$T_{TERM\_ON\_RX}$		5.0	ns	Differential termination enable time. See Section 5.2.1.4.
$T_{TERM\_OFF\_HS\_RX}$		5.0	ns	Differential termination disable time in HS-MODE[4]. See Section 5.2.1.4.
$T_{TERM\_OFF\_PWM\_RX}$		15	SI	Differential termination disable time in PWM-MODE[5]. See Section 5.2.1.4.
$T_{TERM\_OFF\_SYS\_RX}$		15	SI	Differential termination disable time in SYS-MODE[6]. See Section 5.2.1.4.

1. *CRPAT and CJTPAT to be used for test.*
2. *The values include a ground shift of ±50 mV between the M-TX and M-RX.*
3. *The tolerance for the minimum and the maximum of R_{DIF_RX} is different when a nominal resistance of 100 Ω is assumed. The reason for the 20 Ω decrease of the minimum is to cope with interconnect resistances below 50 Ω However, for the maximum only an increase of 10 Ω is specified to limit the voltage drop over R_{DIF_RX}.*
4. *$T_{TERM\_OFF\_HS\_RX}$ may be negative when R_{DIF_RX} is disabled during the reception of 20 UI_{HS} of either DIF-P or DIF-N.*
5. *$T_{TERM\_OFF\_PWM\_RX}$ may be negative when R_{DIF_RX} is disabled during the reception of 9*T_{PWM_RX} of either PWM-b1 or PWM-b0.*
6. *$T_{TERM\_OFF\_SYS\_RX}$ may be negative when R_{DIF_RX} is disabled during the reception of 10 UI_{SYS} of DIF-N.*

5.2.3 HS-RX Characteristics

410 This section contains the electrical and timing characteristics specific to an HS-RX which are not covered by the common M-RX characteristics in Section 5.2.1.

5.2.3.1 LANE-to-LANE Skew

411 The HS-RX LANE-to-LANE skew $T_{L2L\_HS\_RX}$ is defined as the time between the zero crossings of the differential input signal $V_{DIF\_RX}(t)$ at any two HS-RXs in one SUB-LINK when test patterns are applied at both HS-RX PINs. The value of $T_{L2L\_HS\_RX}$ is outside the scope of this document. If required, it shall be defined in the protocol specification.

5.2.3.2 Receiver Jitter Tolerance

412 The receiver total jitter tolerance TJ_{RX} is defined similarly to the transmitter total jitter TJ_{TX}. TJ_{RX} is the sum of the receiver sinusoidal jitter tolerance SJ_{RX} and the receiver random jitter tolerance RJ_{RX} of the differential input signal $V_{DIF\_RX}(t)$. The sequence of jitter events of a signal is a sinusoidal jitter when the jitter events vary sinusoidally from edge to next edge, oscillating between two peaks at a significantly smaller frequency than the transmission rate. The sinusoidal jitter is characterized by its oscillation frequency f_{SJ_RX} and its amplitude which value is identical to the receiver sinusoidal jitter tolerance SJ_{RX}. SJ_{RX} is used as a model for the deterministic jitter of an HS-TX. TJ_{RX} is shown by the following equation:

$$TJ_{RX} = SJ_{RX} + RJ_{RX} \quad \text{(Equation 22)}$$

413 The eye opening at the HS-RX input for the required confidence limit *CL* is defined by $1 - TJ_{RX}$, where TJ_{RX} is the total jitter tolerance of an HS-RX.

414 TJ_{RX} and SJ_{RX} are defined over the frequency range from f_{L_RX} to f_{U_RX}. In addition, the receiver short term total jitter tolerance $STTJ_{RX}$ and the receiver short term sinusoidal jitter tolerance $STSJ_{RX}$, which limit the jitter within a $30UI_{HS}$ signal sequence, are specified due to the BURST type of an HS-MODE transmission. $STTJ_{RX}$ and $STSJ_{RX}$ are defined over the frequency range from $f_{L\_STJ\_RX}$ to f_{U_RX}. $STTJ_{RX}$ is shown by the following equation:

$$STTJ_{RX} = STSJ_{RX} + RJ_{RX} \quad \text{(Equation 23)}$$

415 The receiver total jitter tolerance TJ_{RX} is defined for the differential input signal $V_{DIF\_RX}(t)$ at the zero crossings when a CJTPAT test pattern is applied at an HS-RX.

416 The receiver sinusoidal jitter tolerance SJ_{RX} is defined for the differential input signal $V_{DIF\_RX}(t)$ at the zero crossings when a CJTPAT test pattern, having a sinusoidal jitter with an oscillation frequency f_{SJ_RX}, is applied at an HS-RX, where f_{SJ_RX} is either f_{SJ1_RX}, f_{SJ2_RX}, f_{SJ3_RX}, or f_{SJ4_RX}. f_{SJ3_RX} is only part of this list, if it is within the range set by f_{SJ1_RX} and f_{SJ3_RX}.

417 An HS-RX shall tolerate a CJTPAT test pattern with a sinusoidal jitter SJ_{RX} on to which the random noise RJ_{RX} is superpositioned, where the value of RJ_{RX} is indirectly specified through Equation 22.

418 The receiver total short term jitter tolerance $STTJ_{RX}$ is defined for the differential input signal $V_{DIF\_RX}(t)$ at the zero crossings when a CJTPAT test pattern is applied at an HS-RX.

419 The receiver short term sinusoidal jitter tolerance $STSJ_{RX}$ is defined for the differential input signal $V_{DIF\_RX}(t)$ at the zero crossings when a CJTPAT test pattern, having a sinusoidal jitter with an oscillation frequency f_{SJ_RX}, is applied at an HS-RX, where f_{SJ_RX} is either f_{SJ3_RX}, f_{SJ4_RX}, f_{SJ5_RX}, or f_{SJ6_RX}. f_{SJ3_RX} is only part of this list, if it is within the range set by f_{SJ4_RX} and f_{SJ6_RX}.

420 An HS-RX shall tolerate a CJTPAT test pattern with a short term sinusoidal jitter $STSJ_{RX}$ on to which the random noise RJ_{RX} is superpositioned, where the value of RJ_{RX} is indirectly specified through Equation 23. The value of RJ_{RX} for the short term jitter differs from the value of RJ_{RX} for the normal jitter.

5.2.3.3 Receiver Eye Opening and Accumulated Differential Receiver Input Voltage

421 An accumulated differential input voltage amplitude $V_{DIF\_ACC\_RX}$ defines the minimum vertical receiver eye opening. $V_{DIF\_ACC\_RX}$ is shown in Figure 37. $V_{DIF\_ACC\_RX}$ applies to a SYS-RX, to a PWM-RX, and to an HS-RX operated in HS-GEAR1. They shall detect a differential input signal at the RXDP and RXDN PINs, whose accumulated differential input voltage amplitude conforms with the limit of $V_{DIF\_ACC\_RX}$.

422 The receiver eye may be reopened to, e.g. 50 mV, by use of a simple Linear Time Equalizer.

423 An HS-RX operated in HS-GEAR2 or HS-GEAR3 shall detect a differential input signal at the RXDP and RXDN PINs, whose accumulated differential input voltage amplitude conforms with the limit of $V_{DIF\_ACC\_RX\_G2}$ or $V_{DIF\_ACC\_RX\_G3}$, respectively.

424 The minimum value of V_{DIF_RX}, as described in Section 5.2.1.2, defines the minimum instantaneous differential input voltage amplitude at the M-RX PINs. In addition, the accumulated differential receiver input voltage $V_{DIF\_ACC\_RX}$ is defined as the minimum differential voltage amplitude within an accumulated eye diagram generated from a test pattern. $V_{DIF\_ACC\_HS\_G1\_RX}$, $V_{DIF\_ACC\_HS\_G2\_RX}$, and $V_{DIF\_ACC\_HS\_G3\_RX}$ are the accumulated differential receiver input voltages for an HS-RX operated in HS-G1, HS-G2, and HS-G3, respectively. The receiver eye opening T_{EYE_RX} is defined as the duration over which the differential voltage amplitude is larger than $V_{DIF\_ACC\_RX}$ in the accumulated eye diagram generated from a test pattern. The total receiver jitter tolerance TJ_{RX} is defined as the duration between the

earliest and latest zero crossing at one crossing point in the accumulated eye diagram generated from a test pattern. $V_{DIF\_ACC\_RX}$, T_{EYE_RX}, and TJ_{RX} are shown in Figure 37.

425 An HS-RX shall receive an input signal at the RXDP and RXDN PINs which conforms with the limits of $V_{DIF\_ACC\_RX}$, T_{EYE_RX}, and TJ_{RX}. Definitions given in Figure 37 are based on the accumulated eye for the required confidence limit *CL*.

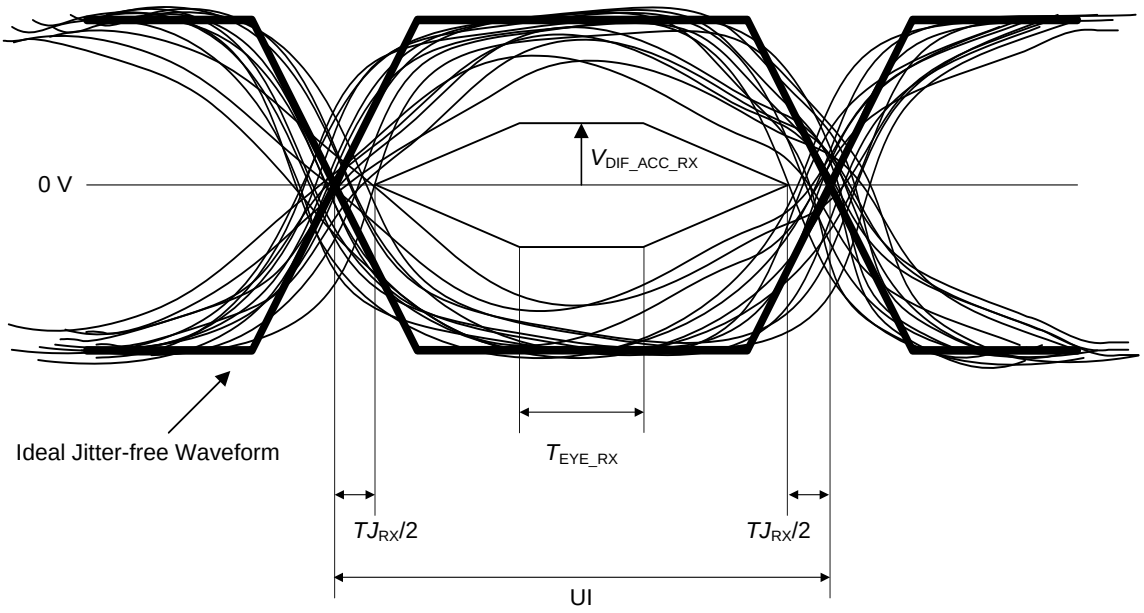


Figure 37 Receiver Eye Diagram

5.2.3.4 Receiver Pulse Width

426 The receiver pulse width T_{PULSE_RX} is defined as the minimum time between the zero crossings of the differential input signal $V_{DIF\_RX}(t)$ when a test pattern is applied at the RXDP and RXDN PINs of an HS-RX. T_{PULSE_RX} is shown in Figure 38 for a DIF-P pulse. Each symbol has to conform with both the receiver eye diagram given in Figure 37 and the receiver pulse width in Figure 38 to ensure reliable reception.

427 An HS-RX shall detect an input signal whose receiver pulse width conforms with the limit of T_{PULSE_RX}.

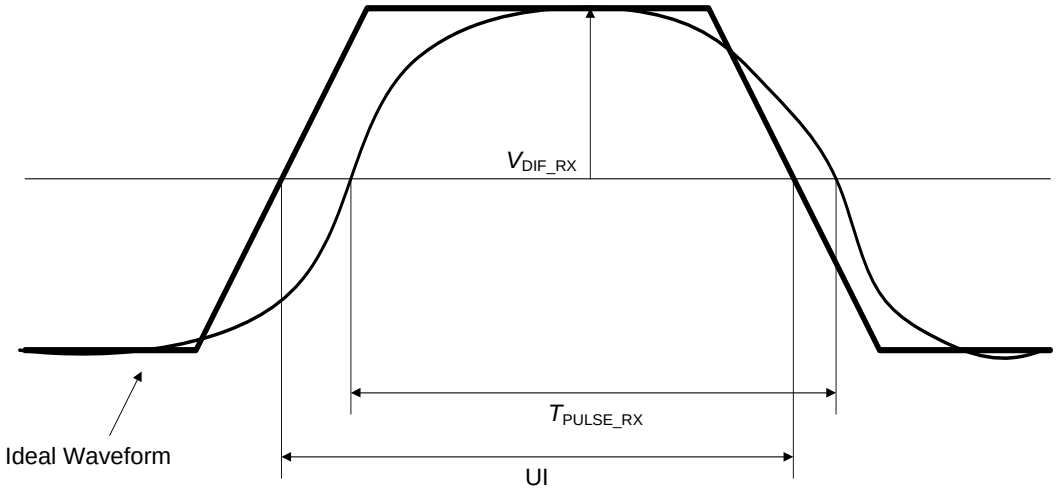


Figure 38 Receiver Pulse Width

5.2.3.5 HS-RX Parameters

428 The electrical and timing parameters of the HS-RX are summarized in Table 20.

Table 20 HS-RX Parameters

Symbol	Values		Unit	Description
	Min.	Max.		
HS-RX Electrical				
$V_{DIF\_ACC\_HS\_G1\_RX}$	40		mV	Accumulated differential receiver input voltage for HS-G1[1]. Defined for test pattern[2,3]. See Section 5.2.3.3.
$V_{DIF\_ACC\_HS\_G2\_RX}$	tbd		mV	Accumulated differential receiver input voltage for HS-G2[1]. Defined for test pattern[2,3]. See Section 5.2.3.3.
$V_{DIF\_ACC\_HS\_G3\_RX}$	tbd		mV	Accumulated differential receiver input voltage for HS-G3[1]. Defined for test pattern[2,3]. See Section 5.2.3.3.
HS-RX Timing				
T_{EYE_RX}	0.20		UI_{HS}	Receiver eye opening. Defined for test pattern[2,3] over a statistical confident record set[6]. See Section 5.2.3.3.
T_{PULSE_RX}	0.80		UI_{HS}	Receiver pulse width. Defined for test pattern[2,3]. See Section 5.2.3.4.

Table 20 HS-RX Parameters (continued)

Symbol	Values		Unit	Description
	Min.	Max.		
HS-RX Jitter				
SJ_{RX}		0.35	UI_{HS}	Receiver sinusoidal jitter tolerance[4]. Defined for test pattern[2] and frequencies f_{SJ1_RX}, f_{SJ2_RX}, f_{SJ3_RX}[5], and f_{SJ4_RX} for a statistical confident record set[3,6,7]. See Section 5.2.3.2.
$STSJ_{RX}$		0.20	UI_{HS}	Receiver short term sinusoidal jitter tolerance[4]. Defined for test pattern[2] and frequencies f_{SJ3_RX}[8], f_{SJ4_RX}, f_{SJ5_RX}, and f_{SJ6_RX} for a statistical confident record set[3,7,9]. See Section 5.2.3.2.
TJ_{RX}		0.52	UI_{HS}	Receiver total jitter tolerance[4]. Defined for test pattern[2] and a statistical confident record set[3,6,7]. See Section 5.2.3.2.
$STTJ_{RX}$		0.30	UI_{HS}	Receiver short term total jitter tolerance[4]. Defined for test pattern[2] and a statistical confident record set[3,7,9]. See Section 5.2.3.2.

1. *Measurement based on accumulative eye diagram.*
2. *CRPAT and CJTPAT to be used for test.*
3. *The test has to be performed at the maximum data rate of the applicable HS-GEAR.*
4. *Accumulated jitter as defined by the jitter model in Section 5.2.3.2.*
5. *f_{SJ3_RX} only applies if following inequation holds: $f_{SJ1\_RX} < f_{SJ3\_RX} < f_{SJ4\_RX}$.*
6. *Filtered using a reference tracking function equivalent to a bandpass from f_{L_RX} up to f_{U_RX}.*
7. *Measured over the confidence interval, CL, of the distribution function of zero crossings of the differential input signal.*
8. *f_{SJ3_RX} only applies if following inequation holds: $f_{SJ4\_RX} < f_{SJ3\_RX} < f_{SJ6\_RX}$.*
9. *Filtered using a reference tracking function equivalent to a bandpass from $f_{L\_STJ\_RX}$ up to f_{U_RX}.*

5.2.4 PWM-RX Characteristics

429 This section contains the timing characteristics specific to a PWM-RX which are not covered by the common M-RX characteristics in Section 5.2.1. The PWM signaling scheme is defined in Section 4.3.2.

5.2.4.1 Accumulated differential Receiver Input Voltage

430 The minimum value of V_{DIF_RX}, as described in Section 5.2.1.2, defines the minimum instantaneous differential input voltage amplitude at the M-RX PINs. In addition, the accumulated differential receiver input voltage $V_{DIF\_ACC\_PWM\_RX}$ is defined as the minimum differential voltage amplitude within an accumulated eye diagram generated from a test pattern, when the PWM-RX is operated in PWM-G5, PWM-G6, or PWM-G7.

431 An PWM-RX operated in PWM-G5, PWM-G6, or PWM-G7 shall detect a differential input signal at the RXDP and RXDN PINs, whose accumulated differential input voltage amplitude conforms with the limit of $V_{DIF\_ACC\_PWM\_RX}$.

5.2.4.2 PWM Bit Duration, Bit Duration Tolerance, and Ratio

432 The PWM receive bit duration T_{PWM_RX} is defined as the duration between zero crossings of two consecutive falling edges of a differential signal at the PWM-RX input. $T_{PWM\_MINOR\_RX}$, $T_{PWM\_MAJOR\_RX}$, and T_{PWM_RX} are shown in Figure 39. The PWM receive bit duration T_{PWM_RX} is, for all PWM GEARs, the sum of its durations $T_{PWM\_MINOR\_RX}$ and $T_{PWM\_MAJOR\_RX}$, as shown in the following equation:

$$T_{PWM\_RX} = T_{PWM\_MINOR\_RX} + T_{PWM\_MAJOR\_RX} \quad \text{(Equation 24)}$$

433 The limits of T_{PWM_RX} are, for all PWM GEARs, identical to the limits of T_{PWM_TX}.

434

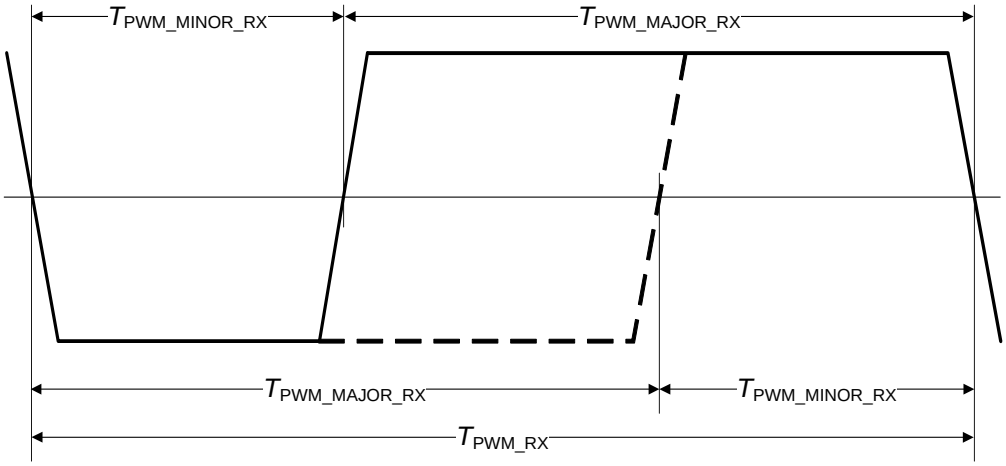


Figure 39 RX Minor and Major Duration in a PWM Signal

435 $T_{PWM\_MINOR\_RX}$ and $T_{PWM\_MAJOR\_RX}$ are determined by T_{PWM_RX} and the PWM receive ratio k_{PWM_RX} for PWM-G1 and higher PWM GEARs. k_{PWM_RX} is defined as the ratio of $T_{PWM\_MAJOR\_RX}$ and $T_{PWM\_MINOR\_RX}$ of one PWM bit, as shown in following equation:

$$k_{PWM\_RX} = \frac{T_{PWM\_MAJOR\_RX}}{T_{PWM\_MINOR\_RX}} \quad \text{(Equation 25)}$$

436 For PWM-G0, the minor duration $T_{PWM\_G0\_MINOR\_RX}$ is directly specified. The range of $T_{PWM\_G0\_MINOR\_RX}$ is defined based on the minor duration in PWM-G1.

437 The PWM receive bit duration tolerance $TOL_{PWM\_G1\_RX}$ is the allowed tolerance of an instantaneous PWM bit duration $T_{PWM\_RX}(i)$ during a LINE-READ state in PWM-G1. $TOL_{PWM\_G1\_RX}$ is defined as the ratio of $T_{PWM\_RX}(i)$ and the average of N PWM receive bit durations during LINE-READ, as shown in the following equation:

$$TOL_{PWM\_G1\_RX} = \frac{T_{PWM\_RX}(i)}{\frac{1}{N}\sum_{i=1}^{N} T_{PWM\_RX}(i)} \quad \text{(Equation 26)}$$

438 where N is a defined number of PWM bits, and i is in the range of 1 to N.

439 While the T_{PWM_RX} range is wide for a PWM GEAR, $TOL_{PWM\_G1\_RX}$ limits the variation of an instantaneous PWM receive bit duration $T_{PWM\_RX}(i)$ during a LINE-READ state. $TOL_{PWM\_G1\_RX}$ is not defined for states other than LINE-READ during a PWM-BURST.

440 A PWM-RX shall detect a PWM input signal whose PWM receive bit duration T_{PWM_RX} is in the specified range of the operational PWM GEAR during a PWM-BURST. For PWM-G1 and higher GEARs, the PWM receive ratio k_{PWM_RX} shall be in the specified range for each PWM bit. For PWM-G0, the minor duration $T_{PWM\_MINOR\_G0\_RX}$ shall be in the specified range for each PWM bit.

441 A PWM-RX shall detect a PWM input signal whose PWM receive bit duration tolerance is in the limits of $TOL_{PWM\_G1\_RX}$ during LINE-READ in PWM-G1.

5.2.4.3 LANE-to-LANE Skew

442 The PWM-RX LANE-to-LANE skew $T_{L2L\_PWM\_RX}$ is defined as the time between the zero crossings of the falling edges of the differential input signal $V_{DIF\_RX}(t)$ at any two PWM-RXs in one SUB-LINK when test patterns are applied at both PWM-RX PINs. The value of $T_{L2L\_PWM\_RX}$ is outside the scope of this document. If required, it shall be defined in the protocol specification.

5.2.4.4 PWM-RX Parameters

443 The timing parameters of the PWM-RX are shown in Table 21.

Table 21 PWM-RX Parameters

Symbol	Values		Unit	Description
	Min.	Max.		
PWM-RX Electrical				
$V_{DIF\_ACC\_PWM\_RX}$	40		mV	Accumulated differential RX voltage amplitude[1]. Defined for test pattern[2] in PWM-G5, PWM-G6, and PWM-G7. See Section 5.2.4.1.
PWM-RX Timing				
$T_{PWM\_G0\_RX}$	1/3	1/0.01	µs	PWM receive bit duration in PWM-G0. Defined for test pattern[2]. See Section 5.2.4.2.
$T_{PWM\_G1\_RX}$	1/9	1/3	µs	PWM receive bit duration in PWM-G1. Defined for test pattern[2]. See Section 5.2.4.2.
$T_{PWM\_G2\_RX}$	1/18	1/6	µs	PWM receive bit duration in PWM-G2. Defined for test pattern[2]. See Section 5.2.4.2.
$T_{PWM\_G3\_RX}$	1/36	1/12	µs	PWM receive bit duration in PWM-G3. Defined for test pattern[2]. See Section 5.2.4.2.
$T_{PWM\_G4\_RX}$	1/72	1/24	µs	PWM receive bit duration in PWM-G4. Defined for test pattern[2]. See Section 5.2.4.2.
$T_{PWM\_G5\_RX}$	1/144	1/48	µs	PWM receive bit duration in PWM-G5. Defined for test pattern[2]. See Section 5.2.4.2.

Table 21 PWM-RX Parameters (continued)

Symbol	Values		Unit	Description
	Min.	Max.		
$T_{PWM\_G6\_RX}$	1/288	1/96	µs	PWM receive bit duration in PWM-G6. Defined for test pattern[2]. See Section 5.2.4.2.
$T_{PWM\_G7\_RX}$	1/576	1/192	µs	PWM receive bit duration in PWM-G7. Defined for test pattern[2]. See Section 5.2.4.2.
$TOL_{PWM\_G1\_RX}$	0.89	1.11		PWM receive bit duration tolerance in PWM-G1. Defined for test pattern[2] during LINE-READ. See Section 5.2.4.2.
N	50			Number of PWM bits. $TOL_{PWM\_G1\_RX}$ has to be met during LINE-READ state over N PWM bits. See Section 5.2.4.2.
$T_{PWM\_G0\_MINOR\_RX}$	1/27	1/9	µs	PWM receive minor duration in PWM-G0. Defined for test pattern[2]. See Section 5.2.4.2.
k_{PWM_RX}	0.60/ 0.40	0.75/ 0.25		PWM receive ratio for PWM-G1 and higher PWM GEARs. Defined for test pattern[2]. See Section 5.2.4.2.

1. *Measurements based on accumulative eye diagram.*
2. *CRPAT and CJTPAT to be used for test.*

5.2.5 SYS-RX Characteristics

444 This section contains the timing characteristics specific to a SYS-RX which are not covered by the common M-RX characteristics in Section 5.2.1.

5.2.5.1 LANE-to-LANE Skew

445 The SYS-RX LANE-to-LANE skew $T_{L2L\_SYS\_RX}$ is defined as the time between the zero crossings of the differential input signal $V_{DIF\_RX}(t)$ at any two SYS-RXs in one SUB-LINK when test patterns are applied at both SYS-RX pins. The value of $T_{L2L\_SYS\_RX}$ is outside the scope of this document. If required, it shall be defined in the protocol specification.

5.2.5.2 Setup and Hold Times

446 Some parameters of the SYS-BURST mode have to be defined by the protocol specification, as described in Section 5.1.4.3. The setup and hold times of the data signal at the SYS-RX input with respect to the reference clock signal belong to the parameters which are defined in the protocol specification. The zero crossing of the differential signal at the SYS-RX input is used as reference timing point for such a definition. Thus, Interoperability in SYS-BURST mode is partly ensured by the protocol specification.

5.2.6 SQ-RX Characteristics

447 This section contains the electrical and timing characteristics specific to a SQ-RX which are not covered by the common M-RX characteristics in Section 5.2.1. The SQ-RX drives a DIF-Z LINE state in certain states. Additionally, the SQ-RX can monitor the LINE state to detect a non-squelch state. The operation of the SQ-RX is described in Section 4.6.

5.2.6.1 Squelch Common-mode Voltage and Squelch Differential Voltage

448 The squelch common-mode voltage signal V_{CM_SQ}(t) is defined as the arithmetic mean value of the voltage signals V_{RXDP}(t) and V_{RXDN}(t) when the SQ-RX drives a DIF-Z at RXDP and RXDN while the LINE is not driven from the M-TX. V_{CM_SQ} is defined as the amplitude of V_{CM_SQ}(t). V_{CM_SQ}(t) can be calculated from following equation:

$$V_{CM\_SQ}(t) = \frac{V_{RXDP}(t) + V_{RXDN}(t)}{2} \quad \text{(Equation 27)}$$

449 A SQ-RX shall keep the squelch common-mode voltage at the M-RX PINs within the limits of V_{CM_SQ}, while driving a DIF-Z and the LINE is not driven from the M-TX.

450 The squelch differential voltage signal $V_{DIF\_SQ}(t)$ is defined as the difference of the signal voltages $V_{RXDP}(t)$ and $V_{RXDN}(t)$ at the M-RX PINs when the SQ-RX drives a DIF-Z at RXDP and RXDN while the LINE is not driven from the M-TX. V_{DIF_SQ} is defined as the amplitude of $V_{DIF\_SQ}(t)$. $V_{DIF\_SQ}(t)$ can be calculated from following equation:

$$V_{DIF\_SQ}(t) = V_{RXDP}(t) - V_{RXDN}(t) \quad \text{(Equation 28)}$$

451 The SQ-RX shall control the signal voltages at the M-RX PINs such that the squelch differential voltage is below the limit of V_{DIF_SQ}, while the SQ-RX drives a DIF-Z and the LINE is not driven from the M-TX.

452 The limits of V_{CM_SQ} and of V_{DIF_SQ} can be achieved by use of a differential resistor or two single-ended resistors, for instance. V_{CM_SQ} and of V_{DIF_SQ} impose limits on the M-RX input resistances at RXDP and RXDN. The lower value of the M-RX input resistances at RXDP and RXDN has to be such that an M-TX with Small Amplitude can drive the LINE from the non-squelch state to the squelch state while the SQ-RX is driving DIF-Z. The upper value of the M-RX input resistances is limited by the PIN leakage currents of the M-TX, the PIN leakage currents of the M-RX, and the mismatch of the M-TX PIN leakage currents. The M-RX input resistances has to be such that the limits of V_{CM_SQ} and of V_{DIF_SQ} are met for the specified M-RX and M-TX PIN leakage currents while the SQ-RX is driving DIF-Z.

5.2.6.2 Squelch Exit Voltage

453 The squelch exit voltage V_{SQ} is the threshold voltage of the SQ-RX, which shall operate when the common-mode voltage is in the V_{CM_SQ} range. When enabled the SQ-RX shall indicate a squelch state of the LINE, as long as the voltage difference of V_{RXDN} and V_{RXDP} is smaller than the minimum squelch exit voltage V_{SQ}, i.e., squelch shall be indicated when the following relation holds:

$$V_{RXDN}(t) - V_{RXDP}(t) < V_{SQ,\,MIN} \quad \text{(Equation 29)}$$

454 When enabled the SQ-RX shall indicate a non-squelch state of the LINE, as long as the voltage difference of V_{RXDN} and V_{RXDP} is larger than the maximum squelch exit voltage V_{SQ}, i.e., non-squelch shall be indicated when the following relation holds:

$$V_{RXDN}(t) - V_{RXDP}(t) > V_{SQ,\,MAX} \quad \text{(Equation 30)}$$

455 The SQ-RX does not need to detect if V_{RXDP} is by more than V_{SQ} larger than V_{RXDN}, because it is only required to detect the transition of the LINE state from DIF-Z to DIF-N.

5.2.6.3 Squelch Exit Time

456 The squelch exit time T_{SQ} is the duration from non-squelch detection until the M-RX enters the SLEEP state. T_{SQ} is defined from the crossing of the differential signal $V_{RXDN} - V_{RXDP}$ with $V_{SQ,MAX}$ until the M-RX

enters the SLEEP state. No value is defined for T_{SQ}, which is an M-RX internal characteristic. However the DIF-N, which is signaled by the M-TX upon exit of the HIBERN8 state for the period $T_{ACTIVATE}$, is an upper bound for T_{SQ}. A lower bound is the pulse width of a DIF-N pulse, which is detected as a non-squelch state by the SQ-RX. This pulse width is not specified, but bounded by the squelch pulse rejection.

5.2.6.4 Squelch Pulse and RF Rejection

457 The squelch noise pulse width T_{PULSE_SQ} is defined as the time the M-RX input signal $V_{RXDN}(t) - V_{RXDP}(t)$ is larger than $V_{SQ,MAX}$. T_{PULSE_SQ} is shown in Figure 40. The SQ-RX shall reject single input noise pulses with an amplitude beyond $V_{SQ,MAX}$ and shorter than the squelch noise pulse width T_{PULSE_SQ}, where the pulse is of a rectangular shape.

458 The noise pulse spacing T_{SPACE_SQ} is defined as the time between the crossings of two adjacent pulse edges of two different, but adjacent, noise pulses with $V_{SQ,MAX}$. Multiple pulses shall be rejected by the SQ-RX when the duration between adjacent pulses is larger than T_{SPACE_SQ}. An example of pulses and a DIF-Z to DIF-N transition, which shall be detected as a non-squelch state by the SQ-RX, is shown in Figure 40.

459 Furthermore, the SQ-RX has to be tolerant to superimposed RF interferences onto the $V_{RXDP}(t)$ and $V_{RXDN}(t)$ signals. This implies an input signal filter. The RF interference is modelled by a sinusoidal signal with a peak interference amplitude V_{INT_SQ} and an interference frequency f_{INT_SQ}. The RF interference is superimposed on the M-RX input signal. The SQ-RX shall meet all specifications in presence of RF interferences with a peak interference amplitude V_{INT_SQ} and frequencies higher than the interference frequency f_{INT_SQ}. The interference shall not cause glitches or incorrect operation during signal transitions.

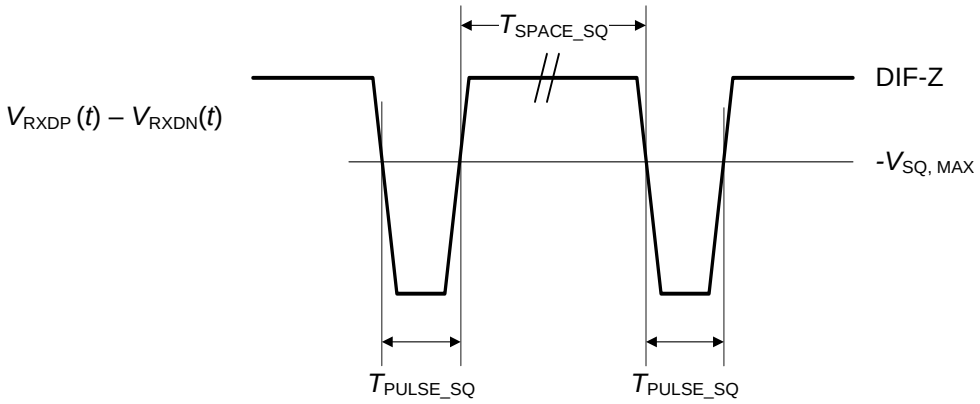


Figure 40 Pulse Rejection and Non-squelch State Detection

5.2.6.5 SQ-RX Parameters

460 The electrical and timing parameters of the SQ-RX are summarized in Table 22.

Table 22 SQ-RX Parameters

Symbol	Values		Unit	Description
	Min.	Max.		
SQ-RX Electrical				
V_{SQ}	50	140	mV	Squelch exit voltage. Defined for test pattern. See Section 5.2.6.2.

Table 22 SQ-RX Parameters (continued)

Symbol	Values		Unit	Description
	Min.	Max.		
V_{DIF_SQ}		20	mV	Squelch differential voltage. Defined for test pattern. See Section 5.2.6.1.
V_{CM_SQ}	0	330	mV	Squelch common-mode voltage. Defined for test pattern. See Section 5.2.6.1.
V_{INT_SQ}		200	mV	Peak interference amplitude. Defined for test pattern. See Section 5.2.6.4.
f_{INT_SQ}	500		MHz	Interference frequency. Defined for test pattern. See Section 5.2.6.4.
SQ-RX Timing				
T_{PULSE_SQ}		20	ns	Noise pulse width. Defined to test pattern. See Section 5.2.6.4.
T_{SPACE_SQ}	500		ns	Noise pulse spacing. Defined for test pattern. See Section 5.2.6.4.

5.3 PIN Characteristics

461 The PIN characteristics of an M-TX and of an M-RX are defined in this section.

5.3.1 PIN Capacitance

462 The single-ended PIN capacitance C_{PIN_RX} of the M-RX is defined as the capacitance between the RXDP and RXDN PINs to ground. C_{PIN_RX} is the lump sum of all single-ended capacitance at an M-RX PIN. The single-ended PIN capacitance should conform to the limit of C_{PIN_RX}.

463 The PIN capacitance mismatch ΔC_{PIN_RX} of an M-RX is defined as the difference of the PIN capacitances at RXDP and RXDN. The PIN capacitance mismatch shall conform to the limits of ΔC_{PIN_RX}. ΔC_{PIN_RX} limits the timing skew between the single-ended signals.

5.3.2 PIN Signal Voltage Range

464 The PIN signal voltage V_{PIN} is defined as the single-ended signal voltage of an M-RX or M-TX PIN to ground. No structure within an M-RX or M-TX shall be damaged when a DC voltage that is within the limits of V_{PIN} is applied at a PIN for an indefinite period of time. The single-ended output signals of an M-TX shall conform with the limits of V_{PIN}.

5.3.3 PIN Leakage Current

465 The PIN leakage current I_{LEAK} is defined as the PIN current flowing in or out of a MODULE when a single-ended voltage in the PIN signal voltage range V_{PIN} is applied at a MODULE PIN. I_{LEAK} is defined for MODULEs which do not drive the LINE and, in the case of an M-RX, whose termination resistor is disabled. The PIN leakage current of every MODULE PIN shall conform with the limits of I_{LEAK}.

466 The PIN leakage current mismatch ΔI_{LEAK_TX} is defined as the difference of the PIN leakage currents at the TXDP and TXDN PINs of an M-TX, when signal voltages are applied which conform with the V_{CM_SQ} and V_{DIF_SQ} ranges. The PIN leakage current mismatch shall stay in the limits of ΔI_{LEAK_TX}.

5.3.4 Ground Shift

467 The ground shift V_{GNDSH} is defined as the ground potential difference of an M-TX and M-RX within a LANE. The ground shift of MODULEs within a LANE shall conform with the limits of V_{GNDSH}.

468 The ground shift is taken into account in the definition of signal voltage parameters. It does not need to be added on top of any signal parameter.

5.3.5 PIN Parameters

469 The common PIN characteristics of an M-RX and M-TX are summarized in Table 23.

Table 23 PIN Parameters

Symbol	Values		Unit	Description
	Min.	Max.		
C_{PIN}		1.5	pF	PIN capacitance. Effective PIN capacitance to ground at an M-RX PIN[1].
ΔC_{PIN}	-0.15	0.15	pF	Mismatch of PIN capacitance. Mismatch of M-RX PIN capacitances[2].
V_{PIN}	-100	600	mV	PIN signal voltage range. Signal voltage range.
I_{LEAK}	-10	10	µA	PIN leakage current. Measured over PIN signal voltage range.
ΔI_{LEAK}	-5	5	µA	PIN leakage current mismatch. Measured over signal voltage range[3].
V_{GNDSH}	-50	50	mV	Ground shift. Ground shift between M-TX and M-RX.

1. *Includes package capacitance.*
2. *For recommended PIN capacitance only.*
3. *Only specified for M-TX PINs.*

6 Electrical Interconnect

470 This section is mainly only informative except for the return loss specifications for the M-TX and M-RX, which are mandatory. All interconnect content is intended as an implementation guideline. If it is strictly followed a system is expected to function. However, a system may also function even when the interconnect recommendations are not fully met, but this depends on the characteristics of the M-TX and M-RX.

471 The LINE is the interconnect between M-TX and an M-RX which conducts the interface signals between two physical layers. This includes differential signalling for both high speed and low speed data transfer. Thus, the LINE should be implemented by means of balanced, differential, point-to-point transmission lines referenced to ground. The LINE may consist of several cascaded transmission lines, such as printed circuit boards, flex-foils, or cable connections that may also include vias and connectors.

472 A LANE is a unidirectional connection of an M-TX and an M-RX via a LINE. The overall LANE performance is therefore determined by the combination of these three elements. This section defines the characteristics of the LINE. For example, tightly coupled lines may be chosen to provide greater confinement of the propagating interface signal fields and thus, to improve isolation parameters for a given application.

473 The tolerances for characteristic impedances of the LINE and the tolerance on LINE termination impedances for M-TX and M-RX are specified by means of S-parameter templates over the whole operating frequency range.

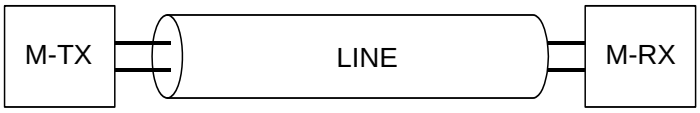


Figure 41 Point-to-Point Interconnect

6.1 Definitions

474 The frequency f_{HS} is defined by the frequency of the current data rate for high-speed data transmission and can be expressed by the following equation:

$$f_{HS} = \frac{1}{(2UI_{HS})} \quad \text{(Equation 31)}$$

475 The frequency f_{HS_MAX} is defined by the following equation:

$$f_{HS\_MAX} = \frac{3}{4} f_{HS\_MAX\_BAUD} \quad \text{(Equation 32)}$$

476 where $f_{HS\_MAX\_BAUD}$ is the frequency of the highest data rate. The frequency f_{HS_MIN} is defined by the following equation:

$$f_{HS\_MIN} = \frac{1}{10} f_{HS\_MIN\_BAUD} \quad \text{(Equation 33)}$$

477 where $f_{HS\_MIN\_BAUD}$ is the frequency of the smallest data rate for high-speed data transmission. The frequency f_{MAX} indicates the maximum frequency of a system implementation.

478 The frequency f_{PWM_MAX} is defined by the following equation:

$$f_{PWM\_MAX} = \frac{2}{3} f_{PWM\_MAX\_BAUD} \quad \text{(Equation 34)}$$

479 where $f_{PWM\_MAX\_BAUD}$ is the frequency of the highest data rate in PWM mode. The frequency f_{SYS_MAX} is defined as the maximum of the reference clock f_{SYS}.

480 The LINE delay T_{LINE} is the time during which a signal is transmitted from the M-TX port of a LINE to its M-RX port. It is measured between zero crossings of the differential signal at both ports.

481 The LANE-to-LANE skew is the skew between different LANEs within a multi-LANE SUB-LINK due to LINE mismatches. M-TX as well as M-RX mismatches do not contribute to the LANE-to-LANE skew. The LANE-to-LANE skew is measured between zero crossings of the differential signals at the M-RX ports within a multi-LANE SUB-LINK. It should be met at the M-RX ports within a multi-LANE SUB-LINK, when signals at the M-TX ports do not have a skew. The value of the LANE-to-LANE skew is outside the scope of this document. If required, it shall be defined in the protocol specification.

482 The LINE reference impedance is denominated by Z_0. The S-parameters are defined based on Z_0.

6.1.1 Interconnect Parameters

483 The electrical and timing parameters of the interconnect are summarized in Table 24.

Table 24 Interconnect Parameters

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
LINE delay	T_{LINE}		7	ns	Measured between zero crossings at test points[1] with conformance test signal source[2] and pattern[3].
LINE reference impedance	Z_0	49.5	50.5	Ω	Nominal reference impedance for definition of S-parameters[4].

1. *Measured between LINE input port and LINE output port, which is terminated by a 100 Ω reference resistor R_{REF} and 1.5 pF reference capacitors C_{REF} at both pins.*
2. *External signal source connected to LINE input port.*
3. *Test pattern at maximum data rate shall be used for test.*
4. *Tolerance defined for measurement setup. Nominal resistance for calculations is 50 Ω*

6.2 S-parameter Specifications

484 The characteristics of the LINE are specified by S-parameters for the M-TX, the LINE, and the M-RX. The LINE is defined by mixed-mode 4-port S-parameters while M-RX and M-TX are specified by mixed-mode reflection parameters. The S-parameter limits are defined by means of templates.

485 The LANE characteristics depend on the targeted bit rates. Most S-parameters are specified on a normalized frequency axis. Only parameters that are important for the suppression of external RF interference are specified on an absolute frequency scale. This scale extends up to f_{MAX}.

486 Only the overall characteristics of the LINE and the maximum reflection of M-RX and M-TX are specified. This fully specifies the signal behavior at the M-RX and the M-TX PINs.

6.3 Characterization Conditions

487 All S-parameter definitions are based on a reference impedance Z_0. The characterization can be done with a measurement system the scheme of which is shown in Figure 42. $V_{C[PORT]}$ denotes the common-mode voltage at a specific port whereas $V_{D[PORT]}$ denotes the differential voltage at a specific port.

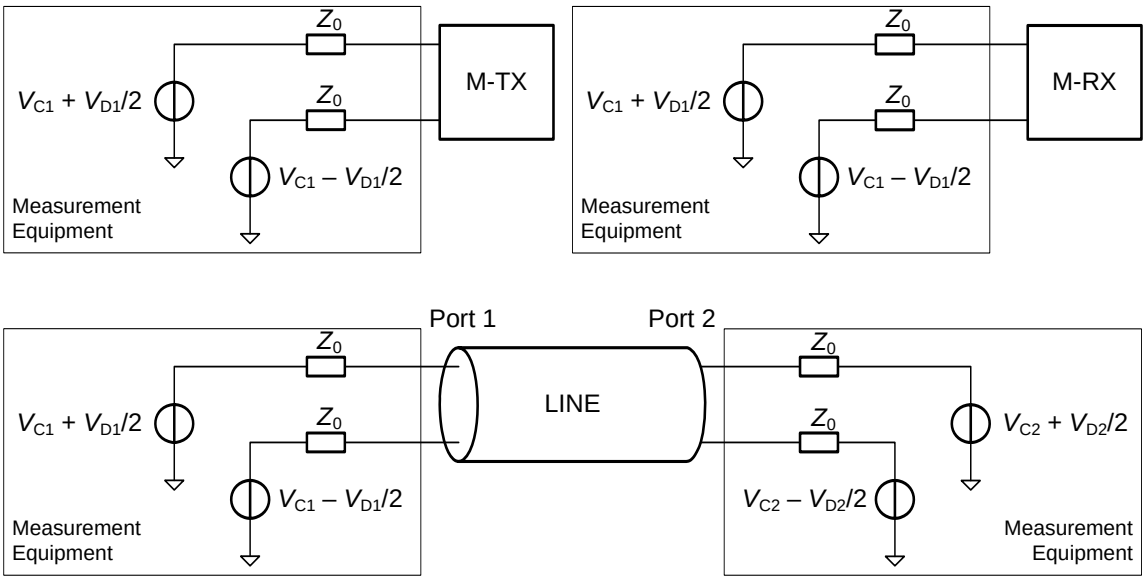


Figure 42 Setup for S-parameter Characterization of M-RX, M-TX, and LINE

488 The syntax of S-parameters is S[measured-mode][driven-mode][measured-port][driven-port], where measured-mode and driven-mode can be either “c” or “d” to indicate common-mode or differential mode, respectively, and measured-port and driven-port can be either “1” or “2”. For example, Sdd21 of the LINE is the reflected differential signal at port 2 due to a differential signal driven at port 1, and Sdc22 is the measured differential reflected signal at port 2 due to a common-mode signal driven at port 2.

6.4 Interconnect Specifications

489 The LINE is specified by means of mixed-mode 4-port S-parameter templates. This includes the differential and common-mode, insertion and return losses, and mode-conversion limits.

490 The set of S-parameters is a limit for long links (< 30 cm) where the large swing Transmitter voltage is utilized.

6.4.1 Differential Characteristics

6.4.1.1 Insertion Loss

491 The differential transfer behavior (insertion loss) of the LINE is specified by the Sdd21 and Sdd12 template shown in Figure 43 for HS-GEAR1 and PWM GEARs.

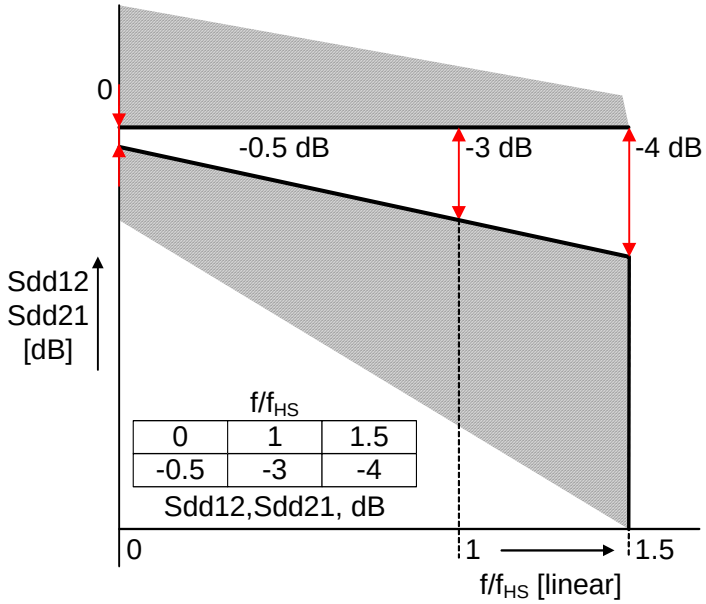


Figure 43 Template for Differential Insertion Loss for HS-GEAR1 and PWM GEARs

6.4.2 Common-mode Characteristics

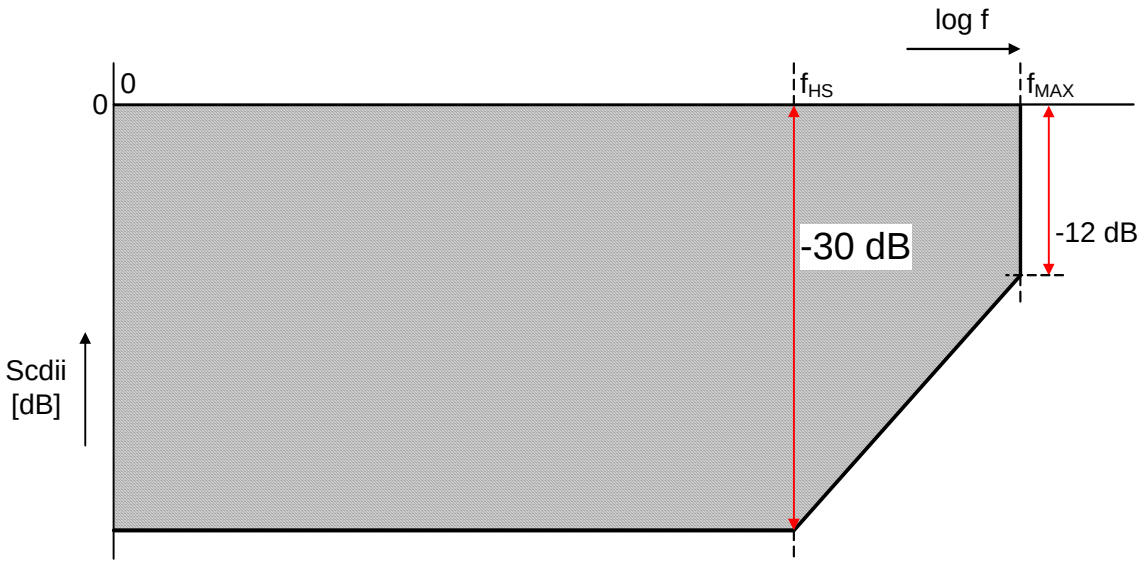
492 The common-mode reflection coefficients Scc11 and Scc22 (common-mode return loss) should both be below -6 dB at frequencies up to f_{HS_MAX}.

6.4.3 Mode-Conversion Limits

493 All mixed-mode, 4-port S-parameters for differential to common-mode conversion, and vice-versa, should be below -26 dB for frequencies up to f_{MAX}. This includes Sdc12, Scd21, Scd12, Sdc21, Sdc11, and Sdc22.

6.4.4 Inter-Line Cross Coupling

494 The common-mode to differential inter-LINE cross coupling between differential LINEs should meet the requirements shown in Figure 44.



Scdii, dB	0	f_{HS}	f_{MAX}
	-30	-30	-12

Figure 44 Inter-Line Common-mode Cross-Coupling Template

6.5 Jitter Influence on LINE Characterization

495 For proper LINE characterization the jitter influence should be considered by applying the following procedure:

496 1. S-parameter measurement of the LINE (see Figure 42 for the measurement setup.)

497 2. LINE simulation utilizing the measured S-parameters and a behavioral M-TX model along with a reference load.

498 3. Worst case simulations of M-TX and LINE into a reference load. Jitter measurement at the reference load. Reference clock jitter and M-TX jitter not covered in simulation have to be added.

499 4. Comparison of the resulting eye margins with the M-RX and M-TX eye specifications given in Table 20 and Table 15 to determine whether or not the LINE meets the specification.

6.5.1 LINE Simulation Setup

500 The statistical simulation setup to generate the eye diagrams for single-LINK LINE characterization is depicted in Figure 45. Test patterns are fed into the behavioral M-TX model with a parasitic impedance Z_{TX_P}, its output into the LINE characterized by the S-parameters, and then into an implementation-specific parasitic load Z_{RX_P} and the reference load R_{REF} for a terminated or unterminated setup.

501 The behavioral M-TX model should be an ideal source and should consider all transmitter specification parameters listed in Table 15 to accommodate for worst case simulations over the whole parameter range, and thus obtain the worst case eye margins for a particular LINE. Furthermore, when generating test patterns the 8b10b coding rules have to be followed. Either fixed patterns for all LINE types or LINE specific patterns may be used as test patterns for simulation.

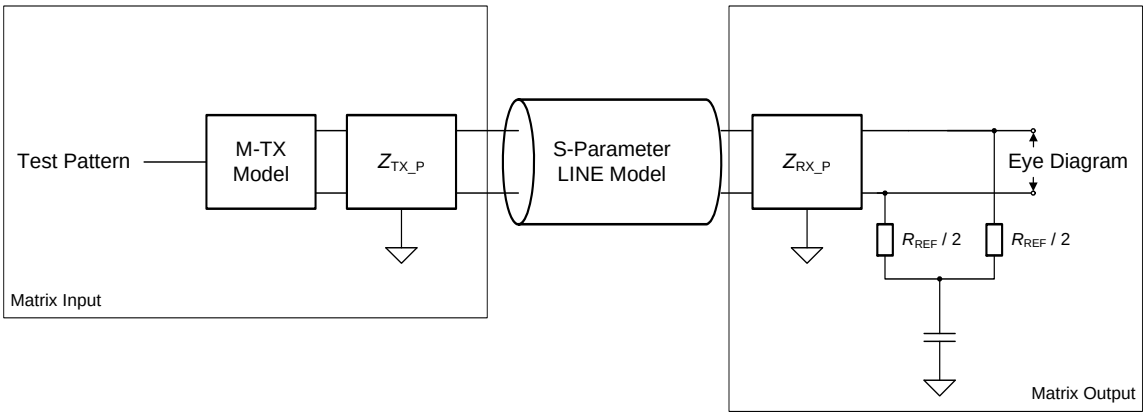


Figure 45 Simulation Environment for Characterizing LINE

502 An R-L-C model for both parasitic impedances Z_{TX_P} and Z_{RX_P} as well as a time delay shall be defined.

6.5.2 LINE Characterization

503 For LINE simulation, low frequency jitter components of reference clock and M-TX are not taken into account. However, the worst case low frequency jitter components of the reference clock and the M-TX must be considered in the overall jitter budget. The design margin is the difference of the resulting eye parameters and the M-RX eye parameters defined in Section 5.2.

504 LINE simulations are carried out only considering high frequency M-TX jitter including duty-cycle distortion phase jitter. High frequency M-TX jitter compresses pulses to minimum width and thus, reduces the eye opening. In the following procedure, proper post-processing has to be applied.

505 1. Take into account the effect of non-simulated jitter, i.e., the jitter not originating from the LINE itself, which cannot be tracked by the CDR. Thus, M-TX jitter and Reference Clock jitter, i.e., random jitter (RJ) and deterministic jitter (DJ) greater than the CDR bandwidth are considered.

506 2. Estimation of voltage and time margins from the eye center.

507 Figure 46 illustrates an example of a typical eye diagram obtained from LINE simulations. First, M-TX and LINE are simulated taking into account the duty-cycle distortion phase jitter. Subsequently, the influence of the non-simulated jitter components, i.e., RJ components of the reference clock and RJ and DJ components of the M-TX, is considered. Thus, the deterministic jitter from the M-TX has to be added to the simulation results and subsequently, the root-mean-square of the random jitter terms from the M-TX and the reference clock has to be calculated and added to the total jitter using the dual-Dirac model. Adding the non-simulated jitter components to the simulated jitter results into a slewing of the eye. Finally, voltage and time margins are obtained from the eye diagram and compared with the specification parameters listed in Table 20.

508 When simulating M-TX jitter, the maximum amount of duty-cycle distortion, for which 0.1 UI may be assumed, should be accounted for. The deterministic jitter from the M-TX has to be added to the simulation results.

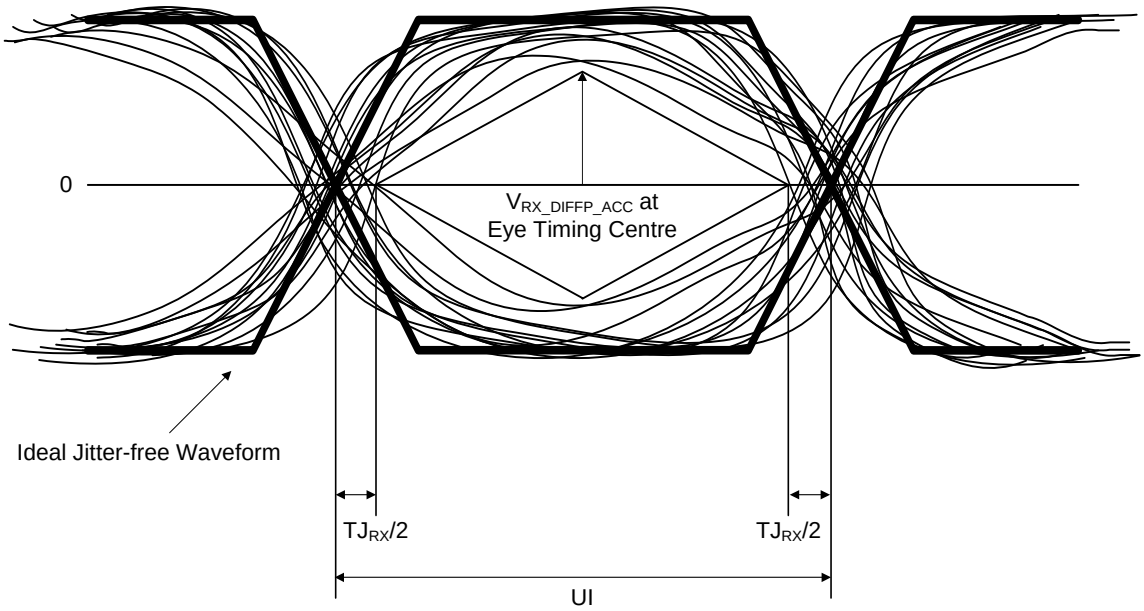


Figure 46 Eye Margins from LINE Simulation Results

7 Optical Media Converter (OMC)

509 An Optical Media Converter (OMC), illustrated in Figure 47, converts electrical signals from an M-TX into optical signals (light waves), transports the signals across a medium such as a Plastic Optical Fiber (POF), and converts the optical signals back into electrical signals that an M-RX can receive.

510 An OMC is considered an inseparable unit, consisting of an optical transmitter (O-TX), an optical receiver (O-RX), each with appropriate photonics, and an optical wave guide. An auxiliary interconnection parallel with the optical interconnect as shown in the figure may be implemented between the O-TX and O-RX. The mechanical and optical interconnect solution and optical interface between the O-TX and O-RX are not within the scope of this specification.

511 A LINE shall contain only one OMC.

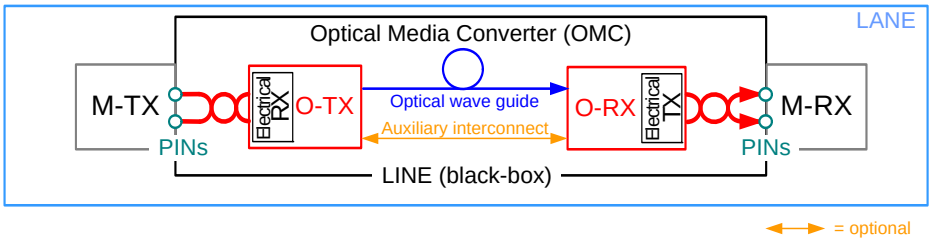


Figure 47 LANE with an OMC

7.1 Application Benefits of the OMC

512 An OMC can replace a galvanic interconnect for improving signal integrity over longer distances, improving EMI characteristics, as well as offering assembly and reliability benefits provided by optical mediums such as flexible Plastic Optical Fiber.

7.2 Types of OMCs

513 This specification defines two type of OMCs: Basic and Advanced. A Basic OMC supports defined minimal functionality including LCC-WRITE, and can operate within a LANE under the condition that the protocol has knowledge that an OMC has been applied and its capabilities known. An Advanced OMC supports LCC-READ and LCC-WRITE and therefore can communicate its presence and capabilities to the protocol. Read and write functions are provided for OMC configuration. Definitions and operation of these functions are in Section 4.7.4.2 and Section 4.8.1.2. OMC-specific details can be found in Section 7.6.

7.3 Internal and External OMCs

514 An Internal OMC is contained within the mechanical outline of the mobile device and has no externally available end-user connector. An optical interconnect inside a mobile device can be used to interconnect two printed circuit boards (PCB) or a module to a PCB. Some common examples include connections from displays, cameras, or non-cellular RF transceivers to the main PCB.

515 An External OMC is used to connect a mobile device to other devices such as an auxiliary display. Implementation details for External OMCs are beyond the scope of this specification. An OMC used by a mobile manufacturer for test purposes is also not within the scope of this specification.

516 An OMC may be implemented as an internal or external interconnect. From the electrical interface perspective there is no difference between the two options.

7.4 OMC – Architecture and Operations

517 An OMC shall support the state machine illustrated in Figure 48, which is based on the M-RX Type-I state machine defined in Section 4.6.1. Differences from the Type-I state machine include the following:

518 • RCT from STALL to SLEEP and STALL to HIBERN8 are not supported by an OMC and as such these transitions are not shown in Figure 48.

519 • Transition criteria from HS-BURST to LINE-CFG for an OMC shall occur on the transition of DIF-P to DIF-N.

520 • Transition criteria from PWM-BURST to LINE-CFG for an OMC shall occur after nine PWM-b1s

521 • DISABLED is a transitory state where the OMC shall independently move to HIBERN8 after an internal POR condition within t_{POR}

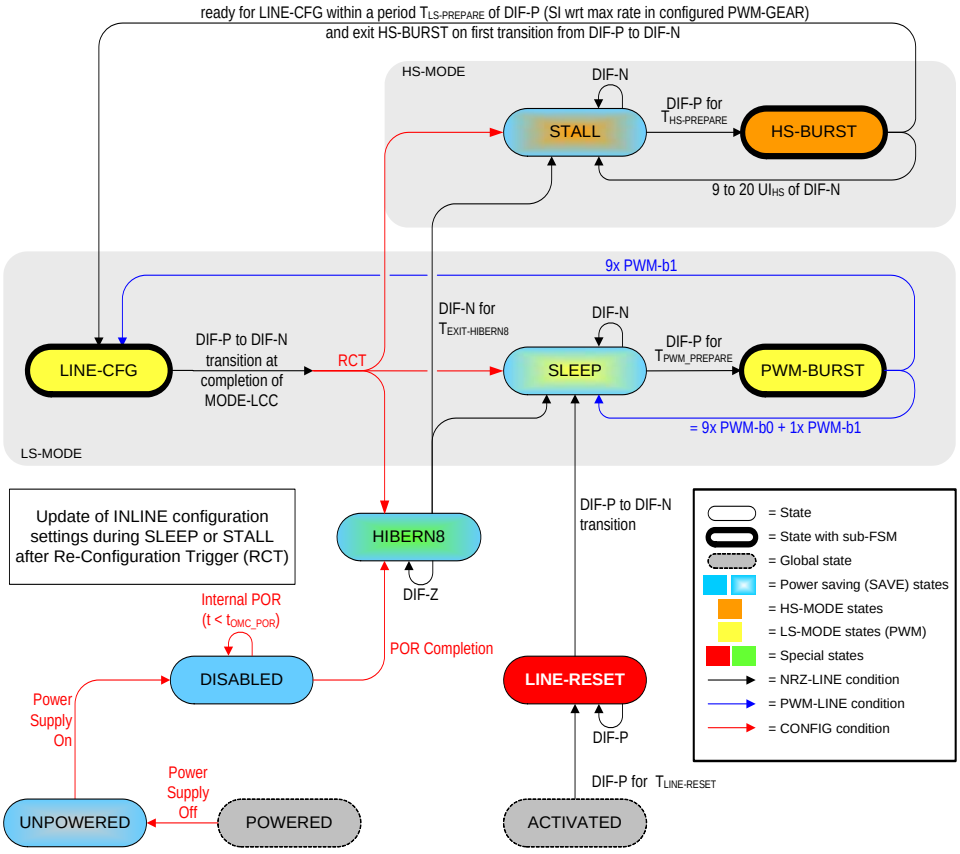


Figure 48 OMC State Diagram (based on Type-I M-RX)

522 The state machine requires that the OMC pass static, DC-unbalanced and DC-balanced signaling. For STALL, SLEEP, HIBERN8, LINE-RESET states and the transition out of these states, a static driven signal is transmitted. The maximum time that a LANE may stay in these power saving states is not defined. For LINE-CFG and the transmission of LCCs, unbalanced signaling is transmitted. The worst case condition occurs in LINE-INIT, which is maintained by the transmission of a continuous PWM-b1. The upper limit for the time duration of LINE-INIT is not specified. DC unbalancing is defined by the PWM signaling characteristics, the FIXED-RATIO scheme is used for gears PWM-G1 and greater, and the FIXED-MINOR scheme for the optional PWM-G0. Finally, during PWM-Burst and HS-Burst 8b10b fully DC-balanced data is transmitted.

523 The following sections add further information to the state machine state definitions given in Section 4.6 with reference to the OMC and OMC state machine. The OMC state machine shall change state based on input

from the protocol through the M-TX using LINE signaling only. No additional signaling for the OMC, outside of the LINE, is provided in this document.

7.4.1 OMC – Data Transmission BURST Modes

524 This document supports three kinds of BURST transmission, including SYS-BURST, HS-BURST and PWM-BURST. An OMC shall support the Type-I PWM-BURST state, and may support the Type-I HS-BURST state.

525 While operating in BURST mode the O-TX input shall conform to the M-RX input specifications defined in Section 5.2.1, and the O-RX output shall conform to the M-TX output specifications defined in Section 5.1.1.

7.4.1.1 OMC – PWM-BURST

526 A SYNC period does not follow the PREPARE period when moving from SLEEP state into PWM-BURST Therefore, the OMC connection to the M-RX shall provide PWM data immediately following the PREPARE period.

7.4.2 OMC – HS-BURST

527 For HS-BURST, an 8b10b-encoded SYNC sequence for a configurable period follows the PREPARE period. Part of this sequence is available for OMC settling as well as the tuning and settling of any clock and data recovery circuits in the M-RX. The OMC settling $T_{OMC\_HS\_START}$ shall be added to any requirement of M-RX circuitry when setting the SYNC length. During the SYNC period the OMC shall hold a PREPARE DIF-P at the output pins until sufficient settling is achieved to transmit valid in-specification data. A small amount of additional pulse width distortion is expected due to de-squelching the O-RX output driver.

7.4.3 OMC – DISABLED

528 The DISABLED state is a transitory state whereby the OMC initiates an independent internal power-on-reset (POR). Upon completion of an internal POR, the OMC shall automatically transition to HIBERN8, which is the lowest power state for the OMC. A POR condition, from entering the DISABLED state to exiting the POR into the HIBERN8 state shall conform to T_{OMC_POR} as specified in Table 25.

Table 25 POR Timing

Parameter	Symbol	Values		Units	Note/Test Condition
		Min.	Max.		
Time taken from entering DISABLED to exiting POR into HIBERN8	T_{OMC_POR}		1	ms	

7.4.3.1 Power Supply Removal

529 The OMC shall enter the DISABLED state from any state with the removal and reapplication of the power supplies. No additional signaling is available to enter the DISABLED state. The OMC should internally handle any additional requirements for POR.

530 The OMC shall exit the DISABLED state with default configuration settings.

7.4.3.2 OMC – HIBERN8

531 HIBERN8 is the lowest power dissipating state for an OMC. During HIBERN8 the OMC shall ensure the LINE is properly terminated. For implementations where the M-TX relies on the O-TX for termination and O-RX relies on the M-RX for termination, the O-TX shall include a weak pull down (DIF-Z), and the O-RX shall maintain a high output impedance as defined in Section 5.2.1 and illustrated for the OMC use-case in Figure 49.

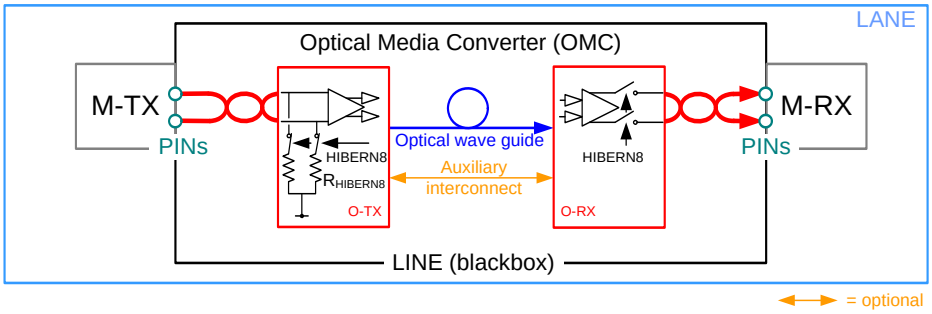


Figure 49 DIF-Z OMC Implementation

7.4.4 OMC – Transitional States

7.4.4.1 OMC – LINE-RESET

532 OMC outputs shall follow M-TX outputs for the LINE-RESET signal and therefore shall comply with the $T_{LINE\text{-}RESET}$ specification in Table 10.

7.5 OMC – Electrical and Interconnect

533 The electrical parameters defined in this section for the OMC use-case is referenced to the test points illustrated in Figure 50. In order to meet an acceptable LINE jitter budget the galvanic connection between the M-TX and O-TX, and the O-RX and M-RX, respectively, should be kept short. These short galvanic connections are defined within this section, but are described for information only. For OMC use-cases the mandatory specification are parameters defined at TP1 and TP4.

534 It is important to note that the OMC input (TP2) electrical characteristics are specified as per the M-RX and the OMC output (TP3) electrical characteristics are specified as per the M-TX as defined in Section 5.1.1.

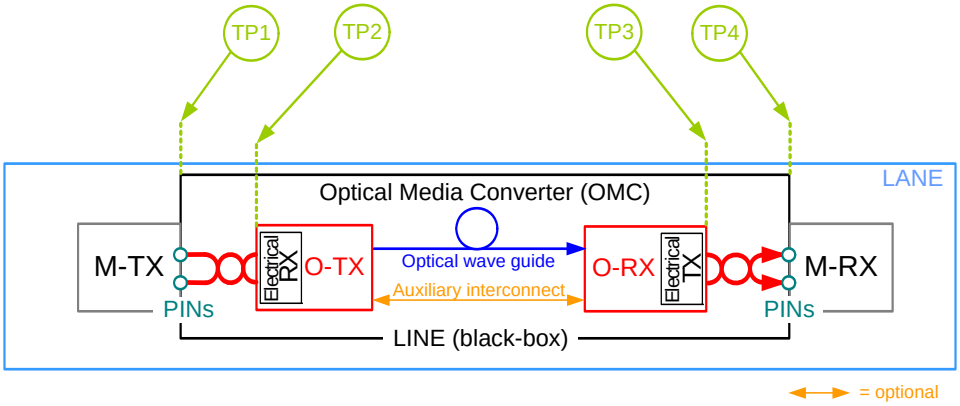


Figure 50 Electrical Specification Test Points

7.5.1 OMC – Galvanic Connection Specification

535 Table 26 defines the electrical characteristics of a short galvanic connection for OMC use-cases. The maximum expected connection length per side of the OMC is $L_{gal\text{-}OMCcase}$. It is important to note that lengths longer than this, if used without care, are likely to result in higher deterministic jitter than specified by $Dj_{gal\text{-}OMCcase}$, imposing tighter restrictions on the O-TX and O-RX.

Table 26 Galvanic Connection Specification (informative)

Parameter	Symbol	Values		Units	Note/Test Condition
		Min	Max.		
Galvanic connection length from OMC and M-TX/M-RX	$L_{gal\text{-}OMCcase}$		3	cm	This is the individual length per side.
Deterministic jitter contribution from a length, $L_{gal\text{-}OMCcase}$ of galvanic connection	$Dj_{gal\text{-}OMCcase}$		0.04	UI	

7.5.2 OMC – Signal Delay

536 LINE delay due to galvanic connections and signal propagation delay due to the use of an OMC (or electrically buffered PWM transmission using OMC auxiliary interconnect) are considered separately.

7.5.2.1 OMC – LINE Delay

537 A LINE delay is specified in Section 6.1.1 for electrical signal integrity. For the OMC use-case it is expected that the short galvanic connection should easily meet this requirement. For some use-cases it is desirable to bypass low speed signals from the input PINs to the output PINs by switching in a direct galvanic connection. For this implementation the LINE is dependant on the termination in the M-RX. The OMC shall meet the accordant LINE delay requirement.

7.5.2.2 OMC – Signal Propagation Delay

538 Some propagation delay is expected through the OMC during optical transmission, and in implementations where bypassing is achieved using some form of buffering across an OMC auxiliary interconnect. This propagation delay is not expected to result in signal integrity issues and shall be handled at a protocol level. An OMC shall create no more than $T_{OMC\text{-}PropDelay}$ during BURST transmission.

539 The parameters for signaling delay through the OMC are defined in Table 27.

Table 27 Signaling Delay

Parameter	Symbol	Values		Units	Note/Test Condition
		Min.	Max.		
Signal propagation delay through optical media converter (for optical or buffered electrical transmission)	$T_{OMC\text{-}PropDelay}$		50	ns	

7.5.3 OMC – HS-BURST Operation

7.5.3.1 OMC – HS-BURST Timing

540 When entering HS-BURST state it is necessary to allow the OMC additional time to settle any internal control loops, e.g., DC restoration or automatic gain control. This is supported by a SYNC period during which a training sequence of configurable length is transmitted. It is important that the M-RX receive only valid M-PHY signals and as such the OMC shall hold the PREPARE state at the outputs to the O-RX from the beginning of the SYNC period until the OMC is fully settled, as defined by $T_{OMC\_HS\_START}$.

541 For an advanced OMC this capability shall be stored in the allocated field, MC_HS_START_TIME, for reporting during an LCC-READ-CAPABILITY, Table 32.

542 It is likely that the first few bits transmitted from the OMC output upon entering HS-BURST will have out-of-specification pulse width distortion while the O-RX output driver recovers from a squelched state. $T_{OMC\_HS\_START}$ shall include any PREPARE time requirements for the OMC. Any pulse width settling shall occur within the specified start-up time $T_{OMC\_HS\_START}$ and therefore shall not reduce any settling time allocated for the M-RX circuitry within the SYNC sequence. An OMC shall meet the specified HS-BURST amplitude requirements during this time.

543 The SYNC period shall be configured for the additive settling of both the OMC and the M-RX circuitry.

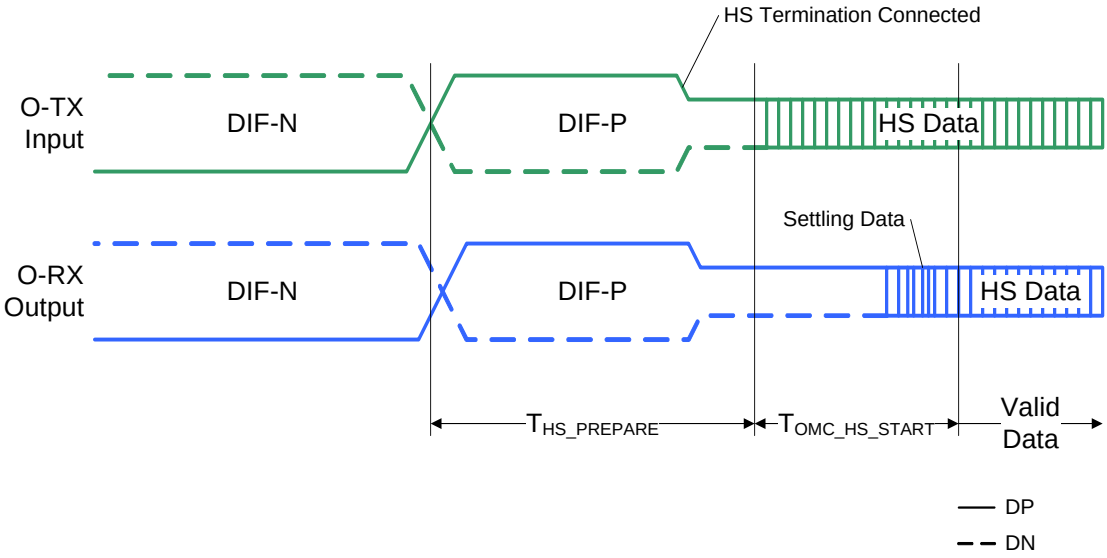


Figure 51 HS-BURST Entry

Table 28 HS-BURST Entry

Parameter	Symbol	Values		Units	Note/Test Condition
		Min.	Max.		
Time required for the OMC to transmit in-specification data	$T_{OMC\_HS\_START}$		10	µS	

7.5.3.2 OMC – HS-BURST Jitter Budget

544 An OMC is intended as a drop-in signal repeater that substitutes the copper interconnects with a medium of inherently higher bandwidth capability, mechanical reliability and lower EMI. While acknowledging these inherent benefits it is also important to note the challenges of designing an optical LINK into a mobile application. When designing to the ultra-low power demands of the mobile application, jitter becomes strongly correlated to power dissipation. For these reasons, the optical jitter budget is kept as high as possible while ensuring no disproportionate impact is made on other inline components. Table 29 specifies a separate jitter budget for the OMC use-case that takes advantage of the shorter galvanic connections at the electrical interfaces.

545 While the galvanic connection is short, jitter is expected to be generated by impedance mismatches from both connection impedance and device termination. In addition to this, capacitive loading and reflections are also seen as possible contributors to jitter on these connections.

546 The jitter figures provided in Table 29 support a BER of 10^{-10} and their derivation is defined in Section 5.1.2.7 for transmit jitter and Section 5.2.3.2 for receive jitter tolerance. The values given are intended to support up to HS-GEAR2 operation, including both RATE series-A and series-B (jitter budget for HS-GEAR3 will be added at a later date).

Table 29 Optical Media Converter (OMC) Jitter Budget

Parameter	Unit	M-TX Output	Galvanic Connection	OMC Input	OMC	OMC Output	Galvanic Connection	M-RX Input
Reference		1	1 – 2	2	2 – 3	3	3 – 4	4
Random jitter	1 / UI (RMS)	0.014	0.000	0.014	0.015	0.021	0.000	0.021
Data jitter	1 / UI	0.150	0.040	0.190	0.140	0.330	0.040	0.370
Total jitter	1 / UI	0.326	0.040	0.366	0.329	0.595	0.040	0.635

7.6 OMC Configuration

547 An OMC shall support line-control-codes (LCCs) for state transitions out of LINE-CFG. A Basic OMC supporting optional features beyond those specified as mandatory shall also support the required CONFIG-LCCs associated with the supported features as outlined in Table 30. An OMC shall pass all LCCs to the M-RX.

548 An Advanced OMC is defined as additionally supporting the CONFIG-LCC-READ commands, providing a mechanism for the protocol to interrogate the PHY for information on OMC configurable capabilities and settings as well as other proprietary data, e.g., device ID, IC revision etc.

7.6.1 OMC Detection

7.6.1.1 Basic OMC

549 It is expected that for a Basic OMC, system awareness is hard-coded at the implementation stage in some protocol memory. This is then acknowledged by the protocol during system configuration. Further to this any configurable capabilities supported by a Basic OMC shall also be hard-coded if it is to be used by the PHY interface.

7.6.1.2 Advanced OMC

550 An Advanced OMC shall support read capability as defined in Section 7.6.2.2. The presence of an Advanced OMC within a PHY can be determined through interrogation of the read data stored at the M-RX, after an LCC read action. In order to support discovery, one bit is assigned in the OMC capability register (OMC_TYPE_Attribute in Table 32). In the case of an Advanced OMC this attribute shall be set to “0”.

551 If a read operation is attempted on a PHY without an Advanced OMC, i.e. where LCC-READ-CAPABILTIY is not supported, the four PWM-b1 bytes transmitted by the M-TX during a read, see Figure 53, shall be received by the M-RX and stored in the OMC capability register. Therefore, for implementations using a basic OMC, or a direct galvanic connection, the OMC_TYPE_Attribute shall be set by default to “1”.

552 The OMC_TYPE_Attribute does not differentiate between a basic OMC and a direct galvanic connection; it only indicates the presence of an Advanced OMC.

7.6.2 OMC – Configuration LCCs

553 Table 30 shows the bit order for setting parameters in an OMC. The capabilities of an OMC should be known by the protocol, outlined for Basic and Advanced use-cases in Section 7.6.1, before configuration is attempted in order to prevent selection of unsupported options.

Table 30 OMC Line Control Codes[1]

b0	b1	TYPE	b2	b3	b4	PARAM SETTING	b5	b6	b7	b8	b9
0	0	MISC	0	0	0	RESERVED	1	1	1	1	1
			0	0	1	RESERVED	0	1	1	0	0
			0	1	0	RESERVED	0	0	0	1	1
			0	1	1	HIBERN8-SLEEP	1	0	0	0	0
			1	0	0	RESERVED	1	0	0	1	0
			1	0	1	RESERVED	0	0	0	0	1
			1	1	0	RESERVED	0	1	1	1	0
			1	1	1	HIBERN8-STALL	1	1	1	0	1
0	1	READ/ WRITE	0	0	0	READ-CAPABILITY	0	1	0	1	0
			0	0	1	READ-CUSTOM-OTX	1	1	0	0	1
			0	1	0	READ-CUSTOM-ORX	1	0	1	1	0
			0	1	1	READ-MFG-INFO-A	0	0	1	0	1
			1	0	0	READ-MFG-INFO-B	0	0	1	1	1
			1	0	1	WRITE-ATTRIBUTE	1	0	1	0	0
			1	1	0	WRITE-CUSTOM-OTX	1	1	0	1	1
			1	1	1	WRITE-CUSTOM-ORX	0	1	0	0	0
1	0	PWM-MODE	0	0	0	PWM-G0	0	0	1	1	0
			0	0	1	PWM-G1	1	0	1	0	1
			0	1	0	PWM-G2	1	1	0	1	0
			0	1	1	PWM-G3	0	1	0	0	1
			1	0	0	PWM-G4	0	1	0	1	1
			1	0	1	PWM-G5	1	1	0	0	0
			1	1	0	PWM-G6	1	0	1	1	1
			1	1	1	PWM-G7	0	0	1	0	0

Table 30 OMC Line Control Codes[1] (continued)

b0	b1	TYPE	b2	b3	b4	PARAM SETTING	b5	b6	b7	b8	b9
1	1	HS-MODE	0	0	0	HS-1A	1	0	0	1	1
			0	0	1	HS-2A	0	0	0	0	0
			0	1	0	HS-3A	0	1	1	1	1
			0	1	1	RESERVED	1	1	1	0	0
			1	0	0	HS-1B	1	1	1	1	0
			1	0	1	HS-2B	0	1	1	0	1
			1	1	0	HS-3B	0	0	0	1	0
			1	1	1	RESERVED	1	0	0	0	1

1. *Columns for LCC data bits in this table are not intended to convey any information on bit-order transmission. Transmission of a 10-bit LCC should always begin with b0.*

554 Line-Control-Codes shall be entered from LINE-INIT, a LINE-CFG sub-state, where the LINE-CFG sub-state machine is defined in Section 4.7.4.2. An OMC exits LINE-CFG to one of three states, SLEEP, STALL or HIBERN8, on a Re-Configuration Trigger (RCT) shown in Figure 48. For an OMC, an RCT is an internally driven event that shall occur within $t_{RCT\text{-}STALL}$ moving to STALL and $t_{RCT\text{-}HIBERN8}$ moving to HIBERN8 from the DIF-P to DIF-N transition at the completion of an LCC. Further reference to RCTs is given in Section 4.7.4.2.4.

555 The LCC type in Table 30 indicates the OMC destination state upon complete transmission of the code. A READ/WRITE type LCC shall exit to LINE-INIT ready for additional LCCs. MODE-PWM type LCC commands shall be followed by SLEEP. A MODE-HS-type LCC command shall be followed by STALL, configured and ready for BURST mode transmission. MISC contains a mixed group of LCCs where destination states are considered on an individual basis.

556 The OMC may enter the HIBERN8 state via two codes in order to indicate whether the OMC enters the STALL or SLEEP state upon exiting HIBERN8 state. These codes are implemented to support direct entry into the desired BURST state following HIBERN8.

7.6.2.1 OMC – LCC-WRITE

557 The write function may be used to load data onto the OMC for configuration purposes. Two types of write are defined, WRITE-ATTRIBUTE supporting configuration of operational settings, e.g. termination settings, and WRITE-CUSTOM supporting proprietary configurations required for stand-alone testing purposes.

558 Configurable write attributes within an OMC should be considered as write-only. There is no read function for reading out configured write attribute data from an OMC to the M-RX.

559 Following an LCC-WRITE, the OMC shall expect a configuration field of 10-bit words. The first and last bit of each 10-bit word shall be delimited with a PWM-b0, the remaining eight bits shall contain configuration data.

560 For WRITE-ATTRIBUTE, the OMC shall return to the LINE-INIT sub-state immediately after receiving the four delimited WRITE bytes. For WRITE-CUSTOM, the OMC shall return to the LINE-INIT sub-state upon receiving nine PWM-b1s, as illustrated in Figure 52.

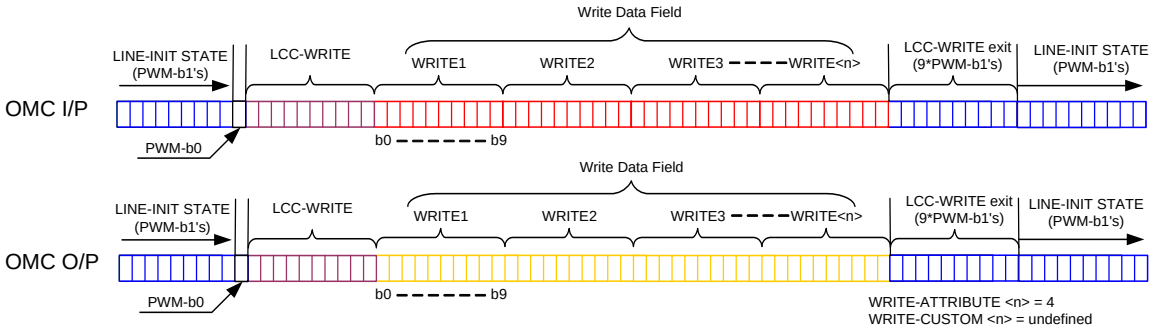


Figure 52 OMC WRITE Function

7.6.2.1.1 OMC – LCC-WRITE-ATTRIBUTE

561 WRITE-ATTRIBUTE is intended for setting configuration parameters required for LANE operation and therefore requires protocol support. Following an LCC-WRITE-ATTRIBUTE the OMC shall expect a four byte field of attribute configuration data as defined in Table 31.

562 Details on the configuration of the settings listed in Table 31 are defined in Table 48.

Table 31 LCC-WRITE-ATTRIBUTE

WRITE	BIT	Configuration Setting
WRITE1	0	DELIMITER (always 0)
	1	M_TX_Amplitude (Provided as info for OMC optimization)
	2	MC_OUTPUT_Amplitude
	3	MC_HS_Unterminated_Enable
	4	MC_LS_Terminated_Enable
	5	MC_HS_Unterminated_LINE_Drive_Enable
	6	MC_LS_Terminated_LINE_Drive_Enable
	7	RESERVED
	8	RESERVED
	9	DELIMITER (always 0)

Table 31 LCC-WRITE-ATTRIBUTE (continued)

WRITE	BIT	Configuration Setting
WRITE2	0	DELIMITER (always 0)
	1	RESERVED
	2	RESERVED
	3	RESERVED
	4	RESERVED
	5	RESERVED
	6	RESERVED
	7	RESERVED
	8	RESERVED
	9	DELIMITER (always 0)
WRITE3	0	DELIMITER (always 0)
	1	RESERVED
	2	RESERVED
	3	RESERVED
	4	RESERVED
	5	RESERVED
	6	RESERVED
	7	RESERVED
	8	RESERVED
	9	DELIMITER (always 0)
WRITE4	0	DELIMITER (always 0)
	1	RESERVED
	2	RESERVED
	3	RESERVED
	4	RESERVED
	5	RESERVED
	6	RESERVED
	7	RESERVED
	8	RESERVED
	9	DELIMITER (always 0)

7.6.2.1.2 OMC – LCC-WRITE-CUSTOM

563 WRITE-CUSTOM is intended for stand-alone test purposes only and therefore does not require protocol support. Provision is made for two WRITE-CUSTOM LCCs addressing the O-RX and O-TX individually. Given the proprietary nature of this feature, and that no interoperability is required, the configuration field length is undefined.

7.6.2.2 OMC – LCC-READ

564 Upon receiving an LCC-READ command the OMC shall transmit a four byte configuration field containing OMC-specific data. This read function provides a mechanism for the PHY to read data from the OMC. Three read commands are available, READ-CAPABILITY, which is used to recover data about the OMC's capabilities and is shown in Table 32, READ-MFG-INFO, which is used to retrieve manufacturing ID and vendor-specific information, and READ-CUSTOM, which provides a configuration field that is left to the implementer's definition.

565 Following an LCC-READ command the M-TX shall transmit four PWM-b1 delimited bytes to complement the configuration field, illustrated in Figure 53. A PWM-b1 delimited byte shall consist of eight PWM-b1s delimited by PWM-b0s. These bytes shall take the common construction of eight PWM-b1s delimited by a PWM-b0 at the beginning and end to make ten PWM bits. The M-TX transmitted PWM-b1 bytes can be used by the OMC to time the READ data onto the O-RX data outputs to the M-RX.

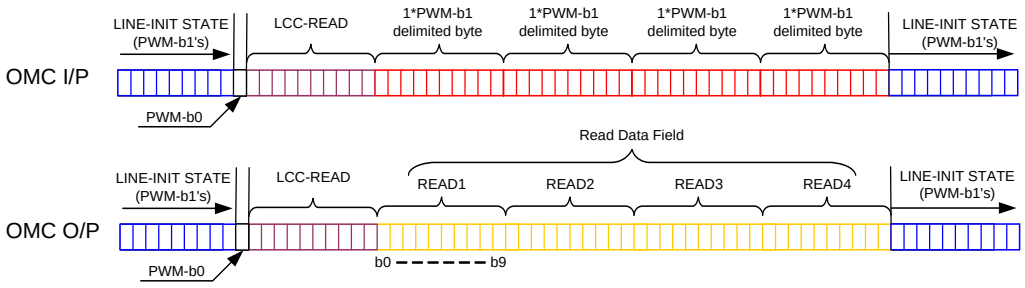


Figure 53 OMC READ Function

7.6.2.2.1 OMC – LCC-READ-CAPABILITY

566 The READ-CAPABILITY function can be used to retrieve an OMC's capabilities for PHY configuration. Following an LCC-READ-CAPABILITY the OMC shall transmit a four byte field of capability data to the M-RX as defined in Table 32.

567 Details on the setting of the attributes listed in Table 32 are defined in Section 8.4.

Table 32 LCC-READ-CAPABILITY Supported Capabilities Bit Definitions

READ	BIT	Capabilities
READ1	0	DELIMITER (always 0)
	1	MC_HSMODE_Capability
	2	MC_HSGEAR_Capability (up to which GEAR) – bit0 (LSB)
	3	MC_HSGEAR_Capability (up to which GEAR) – bit1
	4	MC_HS_START_TIME – Var – bit0 (LSB)
	5	MC_HS_START_TIME – Var – bit1
	6	MC_HS_START_TIME – Var – bit2
	7	MC_HS_START_TIME – Var – bit3
	8	MC_HS_START_TIME – Range – bit0
	9	DELIMITER (always 0)
READ2	0	DELIMITER (always 0)
	1	RESERVED
	2	RESERVED
	3	MC_RX_SA_Capability
	4	MC_RX_LA_Capability
	5	MC_LS_PREPARE_LENGTH – bit0 (LSB)
	6	MC_LS_PREPARE_LENGTH – bit1
	7	MC_LS_PREPARE_LENGTH – bit2
	8	MC_LS_PREPARE_LENGTH – bit3
	9	DELIMITER (always 0)
READ3	0	DELIMITER (always 0)
	1	MC_PWMG0_Capability
	2	MC_PWMGEAR_Capability (up to which GEAR) – bit0 (LSB)
	3	MC_PWMGEAR_Capability (up to which GEAR) – bit1
	4	MC_PWMGEAR_Capability (up to which GEAR) – bit2
	5	MC_HS_Unterminated_Capability
	6	MC_LS_Terminated_Capability
	7	MC_HS_Unterminated_LINE_Drive_Capability
	8	MC_LS_Terminated_LINE_Drive_Capability
	9	DELIMITER (always 0)

Table 32 LCC-READ-CAPABILITY Supported Capabilities Bit Definitions (continued)

READ	BIT	Capabilities
READ4	0	DELIMITER (always 0)
	1	OMC_TYPE_ATTRIBUTE (Advanced = 0)
	2	RESERVED
	3	RESERVED
	4	RESERVED
	5	RESERVED
	6	RESERVED
	7	RESERVED
	8	RESERVED
	9	DELIMITER (always 0)

7.6.2.2.2 OMC – LCC-READ-MFG-INFO-A/B

568 The READ-MFG-INFO function can be used to retrieve the Manufacturing ID and vendor-specific information from an OMC. There are two LCCs assigned for this function which follow the four byte format as defined in Section 7.6.2.2.

569 After receiving an LCC-READ-MFG-INFO-A an OMC shall transmit two delimited bytes containing Manufacturing ID in the fields READ1 and READ2, followed by two delimited bytes containing vendor-specific information in fields READ3 and READ4, defined in Table 33.

570 After receiving an LCC-READ-MFG-INFO-B an OMC shall transmit an additional four delimited bytes containing vendor-specific information as defined in Table 33. This additional vendor-specific information complements the two bytes transmitted during an LCC-READ-MFG-INFO-A triggered read.

571 The content of vendor-specific information is not defined further in this specification to allow full implementation flexibility. For example, the field could be fixed, reporting IC revision data, or programmable, using Non-Volatile Memory, supporting OMC revision data.

572 Further description of the bytes listed in Table 33is defined in Table 52

Table 33 LCC-READ-MFG-INFO-A/B Byte Map

Byte	READ-MFG-INFO-A	READ-MFG-INFO-B
READ1	MC_MFG_ID_Part1	MC_Ext_Vendor_Info_Part1
READ2	MC_MFG_ID_Part2	MC_Ext_Vendor_Info_Part2
READ3	MC_Vendor_Info_Part1	MC_Ext_Vendor_Info_Part3
READ4	MC_Vendor_Info_Part2	MC_Ext_Vendor_Info_Part4

7.6.2.2.3 OMC – LCC-READ-CUSTOM

573 The READ-CUSTOM function is intended for stand-alone test purposes only and therefore does not require protocol support. Provision is made for two READ-CUSTOM LCCs addressing the O-RX and O-TX individually. This read function shall follow the four byte format as defined in Section 7.6.2.2.

7.7 OMC – M-PHY Conformance

574 There are different levels of M-PHY conformance for an OMC as defined in Table 34.

575 An OMC shall support the features in Table 34 labeled “Required”. An OMC may support features labeled “Optional”. An OMC shall not support features labeled as “Not Supported”.

Table 34 OMC M-PHY Conformance

Feature	Support
SLEEP State	Required
PWM-BURST-MODE – GEAR1	Required
PWM-BURST-MODE GEARs other than GEAR1	Optional
HS-BURST-MODE	Optional
STALL State	Required If HS-BURST-MODE is supported
LINE-CFG State	Required
WRITE-ATTRIBUTE Command	Required
WRITE-CUSTOM Command	Optional
READ-CAPABILITY Command	Required for Advanced OMC
READ-CUSTOM Command	Optional
READ-MFG-INFO-A/B	Required for Advanced OMC
LINE-RESET State	Required
HIBERN8 State	Required
SYS-BURST-MODE	Not Supported

7.8 OMC – Test Methodology

576 An OMC shall be tested against the M-PHY-specified electrical characteristics. The OMC shall provide a signal at its outputs that conforms to all M-RX requirements for any valid input signals provided by an M-TX, except as provided for in this section. For conformance testing this requirement is inclusive of the galvanic connection between the OMC and M-TX/M-RX.

577 Parameters requiring special attention for the OMC use-case, i.e. jitter, propagation delay, POR timing etc, have test conditions/notes outlined within Section 7. These conditions can be found alongside the appropriate parameter definition.

8 The Protocol Interface

578 This section defines the Protocol Interface of M-PORTs. This interface connects an M-PORT with the Protocol Layer that utilize M-PHY for the Physical Layer. Protocols applying M-PHY technology include UniPro^{SM} and DigRF^{SM} v4. The M-PORT Protocol Interface is represented in Figure 54.

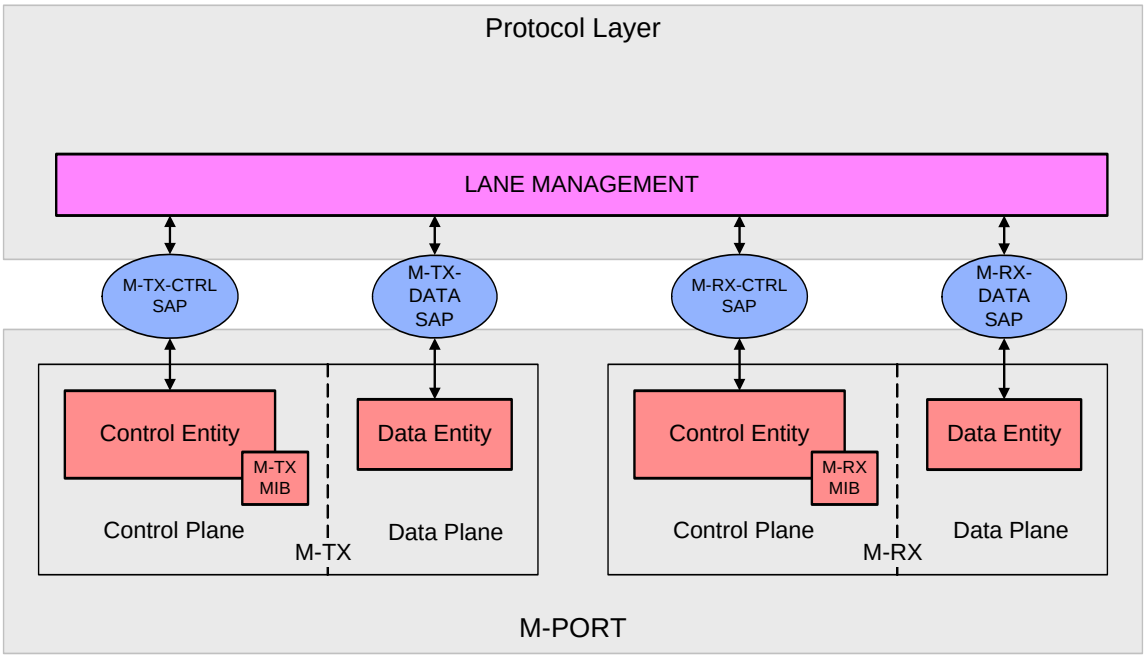


Figure 54 M-PORT Protocol Interface

579 The normative interface specification is based on service access points (SAPs) and service primitives. M-TX-DATA SAP (M-TX Data Service Access Point) and M-RX-DATA SAP (M-RX Data Service Access Point) provide access to the data services of an M-TX and an M-RX, respectively. M-TX-CTRL SAP (M-TX Control Service Access Point) and M-RX-CTRL SAP (M-RX Control Service Access Point) provide access to configuration and reset services of an M-TX and M-RX, respectively.

580 All data transported across LANEs goes through, and is controlled by, the M-TX-DATA and M-RX-DATA SAPs, while the M-TX and M-RX local RESET, LINE-RESET, mode and parameter settings (configuration) are controlled through the M-TX-CTRL and M-RX-CTRL SAPs.

581 An M-PORT may consist of one or more M-TXs and one or more M-RXs. All individual M-TXs and M-RXs in an M-PORT are independent from the Protocol InterFace perspective and each MODULE has its own DATA and CTRL SAP. Constraints on supported MODULE functionality of multi-LANE SUB-LINKS are specified in Section 4.9. LINK composition and usage of LANEs shall be defined by protocols that utilize M-PHY technology for the Physical Layer.

8.1 Service Primitive Naming Convention

582 This document uses an OSI-conforming naming convention for service primitives. Service primitive names are structured as follows:

583 <service-primitive>::= <name-of-service-primitive> ({<parameter>, }*)

584 <name-of-service-primitive> ::= <layer-identifier> - <service-primitive-name> . <primitive>

585 <parameter> ::= <service control information> | <service user data>

586 <layer-identifier> ::= M (or M-LANE or M-CTRL)

587 <service-primitive-name> ::= e.g. SYMBOL | PREPARE | CFGGET | CFGSET | …

588 <primitive> ::= request | indication | response | confirm

589 Services are specified by describing the service primitives and parameters that characterize them. A service may have one or more related primitives that constitute the activity that is related to that particular service. Each service primitive may have zero or more parameters that convey the information required to provide the service.

590 A primitive can be one of four generic types:

591 • Request: The request primitive is passed from the Protocol Layer to a MODULE to request that a service is initiated by the MODULE.

592 • Indication: The indication primitive is passed from a MODULE to the Protocol Layer to indicate an event that is significant to the Protocol Layer. This event may be logically related to a remote service request, or it may be caused by a LANE event.

593 • Response: The response primitive is passed from Protocol Layer to a MODULE to complete a procedure previously invoked by an indication primitive.

594 • Confirm: The confirm primitive is passed from a MODULE to the Protocol Layer to convey the results of one or more associated previous service requests.

8.2 M-TX-DATA and M-RX-DATA SAP

595 The M-TX-DATA SAP and M-RX-DATA SAP contain service primitives for data transfer between the Protocol Layer and the MODULEs of an M-PORT. More specifically, M-TX-DATA SAP provides service primitives for sending data, FILLER symbols, changing the LINE state between BURST-SAVE loop, and sending programmable synchronization pattern during SYNC period of HS-BURST. M-RX-DATA SAP provides service primitives to transfer received data, indicate LINE state change between BURST-SAVE loop and reception of FILLER symbols to the Protocol Layer. Each MODULE (M-TX or M-RX) shall have its own SAP (M-TX-DATA SAP or M-RX-DATA SAP, respectively). Table 35 and Table 36 give an overview of the service primitives provided by the M-TX-DATA SAP and the M-RX-DATA SAP, respectively, and displays the respective section numbers.

Table 35 M-TX-DATA SAP Service Primitives

Name	Request	Indication	Response	Confirm
M-LANE-SYMBOL	8.2.1	n/a	n/a	8.2.3
M-LANE-PREPARE	8.2.4	n/a	n/a	8.2.6
M-LANE-SYNC	8.2.7	n/a	n/a	8.2.8

Table 36 M-RX-DATA SAP Service Primitives

Name	Request	Indication	Response	Confirm
M-LANE-SYMBOL	n/a	8.2.2	n/a	n/a
M-LANE-PREPARE	n/a	8.2.5	n/a	n/a

Table 36 M-RX-DATA SAP Service Primitives (continued)

Name	Request	Indication	Response	Confirm
M-LANE-BurstEnd	n/a	8.2.9	n/a	n/a
M-LANE-HIBERN8Exit	n/a	8.2.10	n/a	n/a

596 There are parameters associated with some of these primitives. Table 37 defines the names, types and valid ranges of these parameters.

Table 37 Parameters of M-TX-DATA SAP and M-RX-DATA Service Primitives

Name	Type	Valid Range	Description
DataN_Ctrl	Boolean	FALSE, TRUE	Data symbol or control symbol selector
DataValue	Integer	0 to 255	Normal payload data
MarkerN_Filler	Boolean	FALSE, TRUE	Marker or FILLER control symbol selection
MarkerNumber	Integer	0 to 2	Type of MARKER symbol selector
3b4b_Error	Boolean	FALSE, TRUE	3b4b Sub-block coding error
5b6b_Error	Boolean	FALSE, TRUE	5b6b Sub-block coding error
Res_Error	Boolean	FALSE, TRUE	Reserved symbol error
RD_Error	Boolean	FALSE, TRUE	Running Digital Sum error

597 The following sections define the meaning of M-TX-DATA SAP and M-RX-DATA SAP service primitives and their associated parameters.

8.2.1 M-LANE-SYMBOL.request

598 This primitive requests the transmission of either a payload data symbol or a control symbol from the Protocol Layer to an M-TX. The control symbol can be either a marker symbol (MK0, MK1, or MK2) or a FILLER symbol. See Section 4.5.2 and Section 4.7.2 for constraints on MARKER usage by the Protocol.

8.2.1.1 Semantics of the Service Primitive

599 The semantics of the M-LANE-SYMBOL.request are as follows:

```
600 M-LANE-SYMBOL.request (
601                         DataN_Ctrl,
602                         DataValue,
603                         MarkerN_Filler,
604                         MarkerNumber
605                         )
```

606 Table 38 specifies the parameters for the M-LANE-SYMBOL request primitive.

Table 38 Parameters for the M-LANE-SYMBOL.request Primitive

Name	Type	Valid Range	Description
DataN_Ctrl	Boolean	FALSE = 0, TRUE = 1	DataN_Ctrl set to “FALSE” selects value associated with the DataValue parameter for transmission; DataN_Ctrl set to “TRUE” chooses either a marker or a FILLER control symbol based on the value of MarkerN_Filler parameter for transmission
DataValue	Integer	0 to 255	Normal payload data. This parameter shall be ignored when DataN_Ctrl set to “TRUE”
MarkerN_Filler	Boolean	FALSE = 0, TRUE = 1	MarkerN_Filler set to “FALSE” selects marker symbol based on the value of MarkerNumber parameter for transmission; MarkerN_Filler set to “TRUE” selects the FILLER symbol for transmission; This parameter shall be ignored when DataN_Ctrl set to “FALSE”
MarkerNumber	Integer	0 to 2	MarkerNumber set to “0” selects MARKER0 (MK0) for transmission; MarkerNumber set to “1” selects MARKER1 (MK1) for transmission; MarkerNumber set to “2” selects MARKER2 (MK2) for transmission; This parameter shall be ignored when DataN_Ctrl set to “FALSE” or MarkerN_Filler set to “TRUE”

8.2.1.2 When Generated

607 This primitive shall be generated by the Protocol Layer in order to transmit a byte of payload data or any marker symbol or a FILLER symbol over the LINE. This primitive with details as M-LANE-SYMBOL.request (FALSE, DataValue, X, X), where DataValue takes valid range as defined in Table 38 and X means ignore that parameter, shall be generated by Protocol Layer in order to transmit a byte of payload data over the LINE.

608 Since MARKER0 symbol is needed to achieve symbol boundary synchronization at M-RX, before actual payload data transmission starts, the Protocol Layer shall generate this primitive with MARKER0 symbol details, i.e., M-LANE-SYMBOL.request (TRUE, X, FALSE, 0), where X means ignore that parameter, at the very beginning of a data transmission BURST. In other words, the Protocol Layer shall generate this primitive with MARKER0 symbol details after issuing an M-LANE-PREPARE.request, but before issuing this primitive with details other than MARKER0 symbol.

609 This primitive with MARKER2 symbol details, i.e., M-LANE-SYMBOL.request (TRUE, X, FALSE, 2), where X means ignore that parameter, shall be issued at the end of a data transmission BURST to allow M-TX to enter into a power saving state.

610 Protocol Layer may request transmission of a FILLER symbol, explicitly, by using this primitive with FILLER symbol details, i.e., M-LANE-SYMBOL.request (TRUE, X, TRUE, X), where X means ignore that parameter. Note that M-TX will insert FILLER symbols autonomously in a BURST state as described in the Section 4.7.2.3.

611 The Protocol Layer shall not exceed the valid range of any parameter. MODULEs shall not verify the validity of any parameter value. Out of range values may lead to malfunction of MODULEs.

8.2.1.3 Effect on Receipt

612 When this primitive is requested with DataN_Ctrl set to “FALSE”, the M-TX shall encode the DataValue byte into an 8b10b Data symbol and then transfer the symbol over the LINE.

613 When this primitive is requested with DataN_Ctrl set to “TRUE” and MarkerN_Filler set to “FALSE” and MarkerNumber set to “0”, “1”, or “2”, the M-TX shall transmit an 8b10b control symbol corresponding to the MARKER0, MARKER1 or MARKER2 symbol, respectively, over the LINE.

614 When this primitive is requested with DataN_Ctrl set to “TRUE” and MarkerN_Filler set to “TRUE”, the M-TX shall transmit 8b10b control symbol corresponding to the FILLER symbol over the LINE.

615 Refer to Section 4.5 for encoding and serialization process.

8.2.2 M-LANE-SYMBOL.indication

616 This primitive reports the reception of a data payload byte or a Marker or a Filler symbol over the LINE.

8.2.2.1 Semantics of the Service Primitive

617 The semantics of the M-LANE-SYMBOL.indication primitive are as follows:

```
618 M-LANE-SYMBOL.indication(
619                         DataN_Ctrl,
620                         DataValue,
621                         MarkerN_Filler,
622                         MarkerNumber,
623                         3b4b_Error,
624                         5b6b_Error,
625                         RD_Error,
626                         Res_Error
627                       )
```

628 Table 39 specifies the parameters for the M-LANE-SYMBOL.indication primitive.

Table 39 Parameters for the M-LANE-SYMBOL.indication Primitive

Name	Type	Valid Range	Description
DataN_Ctrl	Boolean	FALSE = 0, TRUE = 1	When DataN_Ctrl set to “FALSE”, the value associated with the DataValue parameter shall be considered as a received payload byte; When DataN_Ctrl is set to “TRUE”, the value of MarkerN_Filler shall be used in identifying the type of a control symbol received
DataValue	Integer	0 to 255	Indicates normal payload data, one byte in length; this parameter shall be ignored when DataN_Ctrl set to “TRUE”

Table 39 Parameters for the M-LANE-SYMBOL.indication Primitive (continued)

Name	Type	Valid Range	Description
MarkerN_Filler	Boolean	FALSE = 0, TRUE = 1	If the value set to MarkerN_Filler is “FALSE”, then the value associated with a MarkerNumber parameter shall be used in identifying the type of marker symbol received; When MarkerN_Filler is set to “TRUE”, it shall be considered as reception of a FILLER symbol over the LINE; This parameter shall be ignored when DataN_Ctrl set to “FALSE”
MarkerNumber	Integer	0 to 2	This parameter shall be ignored either DataN_Ctrl set to “FALSE” or MarkerN_Filler set to “TRUE”; The value of MarkerNumber = “0” shall be considered as reception of a MARKER0 (MK0) symbol over the LINE; The value of MarkerNumber = “1” shall be considered as reception of a MARKER1 (MK1) symbol over the LINE; The value of MarkerNumber = “2” shall be considered as reception of a MARKER2 (MK2) symbol over the LINE
3b4b_Error	Boolean	FALSE = 0, TRUE = 1	3b4b Sub-block coding error; FALSE: No error detected TRUE: Error detected
5b6b_Error	Boolean	FALSE = 0, TRUE = 1	5b6b Sub-block coding error; FALSE: No error detected TRUE: Error detected
RD_Error	Boolean	FALSE = 0, TRUE = 1	Running Disparity error; FALSE: No error detected TRUE: Error detected
Res_Error	Boolean	FALSE = 0, TRUE = 1	Reserved symbol error; FALSE: No error detected TRUE: Error detected

8.2.2.2 When Generated

629 This primitive shall be generated by the M-RX when an 8b10b data symbol or a control symbol corresponding to MARKER0, MARKER1, MARKER2, or FILLER is received over the LINE.

630 When the received 8b10b symbol is a valid data symbol, DataValue shall carry the decoded payload byte. In this case, 3b4b_Error, 5b6b_Error and Res_Error shall be set to “FALSE”. In this case, DataN_Ctrl value shall be set to “TRUE”, and all other parameter values, except DataValue, shall be ignored

631 If the received 8b10b symbol is a marker symbol, then the M-RX shall set DataN_Ctrl to “TRUE”, MarkerN_Filler to “FALSE”, and the MarkerNumber shall be set to 0, 1, or 2, if the received marker symbol is MARKER0, MARKER1 or MARKER2, respectively. DataValue parameter may be set to “0” and shall be ignored by the Protocol Layer. All the error parameters shall be set to “FALSE”.

632 If the received 8b10b symbol is a FILLER symbol, then the M-RX shall set DataN_Ctrl to “TRUE” and MarkerN_Filler to “TRUE”. The parameters DataValue and MarkerNumber may be set to “0” and shall be ignored by the Protocol Layer. All the error parameters shall be set to “FALSE”.

633 If the received 8b10b symbol is an invalid symbol, DataValue shall carry the re-mapped payload byte, with potentially incorrect bits for the invalid sub-block, but correct bits of the valid sub-block. In this case, 3b4b_Error or 5b6b_Error shall be set to “TRUE”, depending on which of the sub-blocks was in error. Res_Error shall be set to “FALSE”.

634 If the received 8b10b symbol is a valid, but reserved symbol (i.e. not equal to a data symbol, MARKER0, MARKER1, MARKER2 or FILLER), DataValue shall carry the re-mapped payload byte. In this case, 3b4b_Error and 5b6b_Error shall be set to “FALSE” and Res_Error shall be set to “TRUE”.

635 If the Running Disparity (RD) in the M-RX (See Section 4.5.3) computes an RD error for the currently received 8b10b symbol, the RD_Error parameter shall be set to “TRUE”. This setting shall not depend on the other error parameters described above.

8.2.2.3 Effect on Receipt

636 On receipt of the M-LANE-SYMBOL.indication primitive, the Protocol Layer is notified of the availability of inbound data byte or the reception of a MARKER0, MARKER1, MARKER2, or FILLER symbol by the M-RX and generating a corresponding marker number or FILLER indication, and error information at M-RX. The Protocol Layer shall consume the data byte or a marker number along with error information and may carry out appropriate Protocol action.

637 Protocol Layer shall ignore the MarkerN_Filler and MarkerNumber parameters when DataN_Ctrl is set to “TRUE”; shall ignore DataValue parameter when DataN_Ctrl and MarkerN_Filler are set to “FALSE”; shall ignore DataValue and MarkerNumber parameters when DataN_Ctrl is set to “FALSE” and MarkerN_Filler is set to “TRUE”.

8.2.3 M-LANE-SYMBOL.confirm

638 This primitive informs the Protocol Layer that the M-TX has completed the previously issued M-LANE-SYMBOL.request.

8.2.3.1 Semantics of the Service Primitive

639 The semantics of M-LANE-SYMBOL.confirm primitive are as follows

```
640 M-LANE-SYMBOL.confirm(
641                       Status
642                       )
```

643 Table 40 specifies the parameters for the M-LANE-SYMBOL.confirm primitive.

Table 40 Parameters for the M-LANE-SYMBOL.confirm Primitive

Name	Type	Valid Range	Description
Status	Boolean	ACCEPTED = 0, BUSY = 1	Status = ACCEPTED means that M-TX has accepted the previously requested symbol for transmission and ready for new request to be served; Status = BUSY means that M-TX has rejected the previously requested symbol; the Protocol Layer may issue the request again

8.2.3.2 When Generated

644 This primitive shall be generated when the M-TX has either accepted or rejected the previously issued M-LANE-SYMBOL.request primitive. It also confirms that the M-TX may accept another request to transfer a payload byte or a marker or a FILLER symbol from the Protocol Layer.

8.2.3.3 Effect on Receipt

645 Following the issuing of an M-LANE-SYMBOL.request and prior to the reception of an M-LANE-SYMBOL.confirm primitive, the Protocol Layer shall not trigger a new M-LANE-SYMBOL.request primitive. Upon receiving this primitive the Protocol Layer may issue a new data or marker symbol, or configuration request or retry the previously rejected symbol request.

8.2.4 M-LANE-PREPARE.request

646 This primitive requests the M-TX to enter into a BURST state, either HS-BURST, PWM-BURST or SYS-BURST depending upon the mode of operation, from the power saving state. See Section 4 for more details on BURST state, power saving state and operating modes.

8.2.4.1 Semantics of the Service Primitive

647 The semantics of the M-LANE-PREPARE.request primitive are as follows:

```
648 M-LANE-PREPARE.request (
649                     )
```

650 This primitive has no parameter.

8.2.4.2 When Generated

651 The Protocol Layer shall issue this primitive to request the M-TX to enter from power saving state to BURST state corresponding to the M-TX mode of operation. This primitive shall only be issued when the M-TX is in power saving state.

8.2.4.3 Effect on Receipt

652 The M-TX shall enter into the BURST state following the sequence of operation as described in Section 4.7.2.

8.2.5 M-LANE-PREPARE.indication

653 This primitive informs the Protocol Layer that the M-RX is coming out of power saving state and entering into a BURST state, either HS-BURST, PWM-BURST or SYS-BURST depending on the M-RX mode of operation. See Section 4 for more details on BURST state, power saving state and operating modes.

8.2.5.1 Semantics of the Service Primitive

654 The semantics of the M-LANE-PREPARE.indication primitive are as follows:

```
655 M-LANE-PREPARE.indication (
656                     )
```

657 This primitive has no parameter.

8.2.5.2 When Generated

658 The M-RX shall issue this primitive to the Protocol Layer when M-RX detects PREPARE period (a period of DIF-P LINE state) while it is in power saving state.

8.2.5.3 Effect on Receipt

659 The Protocol Layer shall accept M-RX entering to the BURST state corresponding to the M-RX mode of operation and shall be prepared to receive data.

8.2.6 M-LANE-PREPARE.confirm

660 This primitive informs the Protocol Layer that the M-TX has started entering into BURST state following the reception of M-LANE-PREPARE.request.

8.2.6.1 Semantics of the Service Primitive

661 The semantics of M-LANE-PREPARE.confirm primitive are as follows

```
662 M-LANE-PREPARE.confirm(
663                       )
```

664 This primitive has no parameter.

8.2.6.2 When Generated

665 This primitive shall be generated by the M-TX when it enters into a PREPARE period upon the reception of an M-LANE-PREPARE.request primitive.

8.2.6.3 Effect on Receipt

666 Upon receiving this primitive the Protocol Layer may issue a programmable synchronization sequence through M-LANE-SYNC.request primitive when the M-TX is configured to receive external synchronization pattern from the protocol. Otherwise, the Protocol Layer may issue MARKER0 symbol request at any time during the SYNC period.

8.2.7 M-LANE-SYNC.request

667 This primitive requests the transmission of a programmable sync pattern byte wise over the LINE. For more details on SYNC sequences see Section 4.7.2.2.

8.2.7.1 Semantics of the Service Primitive

668 The semantics of the M-LANE-SYNC.request primitive are as follows:

```
669 M-LANE-SYNC.request (
670                       SyncData
671                       )
```

672 Table 41 specifies the parameters for the M-LANE-SYNC.request primitive

Table 41 Parameters for M-LANE-SYNC.request Primitive

Name	Type	Valid Range	Description
SyncData	Integer	0 to 255	A byte of data from the programmable sync sequence

8.2.7.2 When Generated

673 This primitive shall be generated by the Protocol Layer to request the transmission of a synchronization pattern to be provided by the protocol. This primitive only has effect if the M-TX is configured to send a

programmable synchronization sequence. The synchronization sequence shall be issued to the M-TX one byte at a time using this primitive. The Protocol Layer shall wait for the M-LANE-SYNC.confirm primitive before issuing this primitive again. The first issue of this primitive shall only take place after the Protocol Layer receives M-LANE-PREPARE.confirm primitive from the M-TX to the previously issued M-LANE-PREPARE.request primitive and before SYNC period starts.

8.2.7.3 Effect on Receipt

674 The M-TX shall encode SyncData byte as an 8b10b symbol and then transfer the symbol over the LINE. Upon transmission of SyncData byte the M-TX shall issue an M-LANE-SYNC.confirm primitive to the Protocol Layer.

8.2.8 M-LANE-SYNC.confirm

675 This primitive informs the Protocol Layer that the M-TX has completed the previously issued service request M-LANE-SYNC.request.

8.2.8.1 Semantics of the Service Primitive

676 The semantics of M-LANE-SYNC.confirm primitive are as follows

```
677 M-LANE-SYNC.confirm(
678                     )
```

679 This primitive has no parameter.

8.2.8.2 When Generated

680 This primitive shall be generated when the M-TX has completed serving the previously issued M-LANE-SYNC.request primitive and is ready to accept another synchronization sequence symbol from the Protocol Layer to transfer.

8.2.8.3 Effect on Receipt

681 The Protocol Layer may issue a new synchronization symbol or marker symbol request upon receiving this primitive. The Protocol Layer shall not issue a new M-LANE-SYNC.request until a previously issued M-LANE-SYNC.request has been responded with this primitive.

8.2.9 M-LANE-BurstEnd.indication

682 This primitive reports the reception of a BURST CLOSURE condition to the Protocol as described in Section 4.7.2.4.

8.2.9.1 Semantics of the Service Primitive

683 The semantics of the M-LANE-BurstEnd.indication primitive are as follows:

```
684 M-LANE-BurstEnd.indication(
685                           )
```

686 This primitive has no parameter.

8.2.9.2 When Generated

687 This primitive shall be generated by the M-RX to the Protocol Layer when M-RX detects a sequence of b0 or b1 on LINE over the period defined in Section 4.7.2.4 while it is in BURST state.

8.2.9.3 Effect on Receipt

688 Protocol Layer shall accept end of BURST state and shall consider that the M-RX is entering either into LINE-CFG state when sequence of b1 received over a period as described in Section 4.7.2.4.2 or SAVE state when sequence of b0 received over a period as described in Section 4.7.2.4.1.

8.2.10 M-LANE-HIBERN8Exit.indication

689 This primitive reports the exit of HIBERN8 state to the Protocol as described in Section 4.7.1.3.

8.2.10.1 Semantics of the Service Primitive

690 The semantics of the M-LANE-HIBERN8Exit.indication primitive are as follows:

691
```
M-LANE-HIBERN8Exit.indication(
692                           )
```

693 This primitive has no parameter.

8.2.10.2 When Generated

694 This primitive shall be generated by the M-RX to the Protocol Layer when M-RX detects exit of HIBERN8 state as defined in Section 4.7.1.3 while M-RX is in HIBERN8 state.

8.2.10.3 Effect on Receipt

695 Protocol Layer shall accept exit of HIBERN8 state and shall consider that the M-RX is entering either to SLEEP or to STALL state based on the value of RX_MODE attribute. The Protocol Layer may use this primitive to get out of hibernation.

8.2.11 Sequence of Service Primitives

696 The possible relationships among primitives at M-TX-DATA SAP and M-RX-DATA SAP are illustrated by the given time sequence diagrams shown in Figure 55. They also indicate a possible logical relationship in terms of time. Primitives that occur earlier in time and connected by dotted lines are logical predecessors of subsequent primitives.

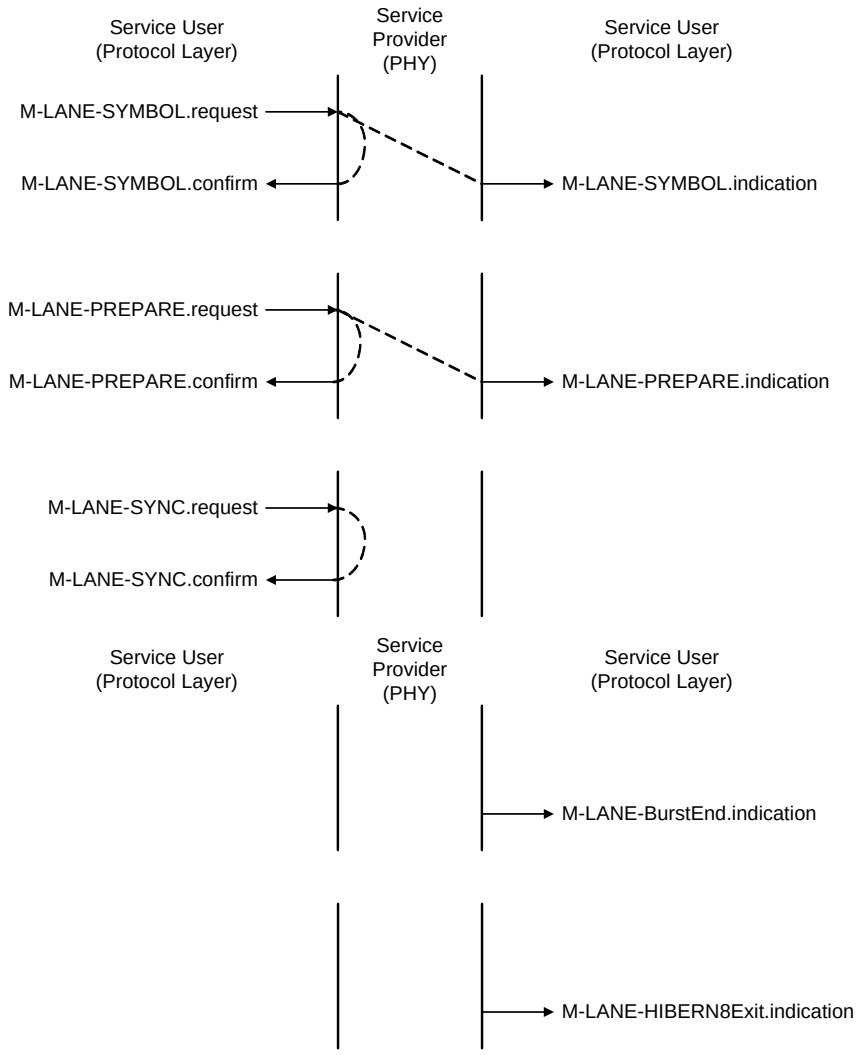


Figure 55 Sequence of Primitives at M-TX-DATA SAP and M-RX-DATA SAP

8.3 M-TX-CTRL SAP and M-RX-CTRL SAP

697 M-TX-CTRL SAP and M-RX-CTRL SAP contain service primitives for configuring M-TX and M-RX, respectively, and obtaining capability and status information from these MODULEs. Table 42 and Table 43 give an overview of the service primitives provided by M-TX-CTRL SAP and M-RX-CTRL SAP, respectively, and display the respective section numbers. There are parameters associated with these primitives. Section 8.4 defines the name, type and valid range of these parameters.

Table 42 M-TX-CTRL SAP Service Primitives

Name	Request	Indication	Response	Confirm
M-CTRL-CFGGET	8.3.1	n/a	n/a	8.3.2
M-CTRL-CFGSET	8.3.3	n/a	n/a	8.3.4

Table 42 M-TX-CTRL SAP Service Primitives (continued)

Name	Request	Indication	Response	Confirm
M-CTRL-CFGREADY	8.3.5	n/a	n/a	8.3.6
M-CTRL-RESET	8.3.7	n/a	n/a	8.3.8
M-CTRL-LINERESET	8.3.9	n/a	n/a	8.3.11

Table 43 M-RX-CTRL SAP Service Primitives

Name	Request	Indication	Response	Confirm
M-CTRL-CFGGET	8.3.1	n/a	n/a	8.3.2
M-CTRL-CFGSET	8.3.3	n/a	n/a	8.3.4
M-CTRL-CFGREADY	8.3.5	n/a	n/a	8.3.6
M-CTRL-RESET	8.3.7	n/a	n/a	8.3.8
M-CTRL-LINERESET	n/a	8.3.10	n/a	n/a
M-CTRL-LCCReadStatus	n/a	8.3.12	n/a	n/a

698 The parameters associated with these primitives are defined in Table 44 with the name, type and valid range.

Table 44 Parameters of M-TX-CTRL SAP and M-RX-CTRL SAP Service Primitives

Name	Type	Valid Range	Description
MIBattribute	Attribute name	Any attribute ID as defined in Section 8.4	The name of the MIB attribute
MIBvalue	Depends on attribute	Depends on the attribute as defined in Section 8.4	The value of the MIB attribute

699 The following sections define the meaning of M-TX-CTRL SAP and M-RX-CTRL SAP service primitives and their associated parameters.

8.3.1 M-CTRL-CFGGET.request

700 This primitive requests information about a MIB attribute, which are defined in Section 8.4.

8.3.1.1 Semantics of the Service Primitive

701 The semantics of the M-CTRL-CFGGET.request primitive are as follows:

```
702 M-CTRL-CFGGET.request(
703                     MIBattribute
704                     )
```

705 The primitive parameter is defined in Table 44.

8.3.1.2 When Generated

706 This primitive is generated by the Protocol Layer to obtain information of an MIBattribute from a MODULE's MIB. The Protocol Layer shall ensure that the requested MIBattribute exists. The MODULE may not check the validity of an MIBattribute. Undefined attribute names may result in malfunctioning of a MODULE. After issuing an M-CTRL-CFGGET.request primitive, the Protocol Layer shall wait for the M-CTRL-CFGGET.confirm primitive reception before issuing a new configuration service request.

8.3.1.3 Effect on Receipt

707 The MODULE retrieves value of the requested attribute from its MIB and responds with M-CTRL-CFGGET.confirm that gives the result.

8.3.2 M-CTRL-CFGGET.confirm

708 This primitive reports the result of a service request on MIBattribute.

8.3.2.1 Semantics of the Service Primitive

709 The semantics of the M-CTRL-CFGGET.confirm primitive are as follows:

```
710 M-CTRL-CFGGET.confirm(
711                     MIBvalue
712                     )
```

713 The primitive parameters are defined in Table 44.

8.3.2.2 When Generated

714 This primitive shall be generated by a MODULE in response to the most recent M-CTRL-CFGGET.request by the Protocol Layer. The MIBvalue parameter shall contain the value of the requested MIBattribute.

8.3.2.3 Effect on Receipt

715 The Protocol Layer shall accept this primitive in order to receive the value of the requested MIBattribute. The MIBvalue parameter will carry this value.

8.3.3 M-CTRL-CFGSET.request

716 This primitive requests to set an MIB attribute indicated by the parameter MIBattribute to the value hold by the parameter MIBvalue.

8.3.3.1 Semantics of the Service Primitive

717 The semantics of the M-CTRL-CFGSET.request primitive are as follows:

```
718 M-CTRL-CFGSET.request(
719                     MIBattribute,
720                     MIBvalue
721                     )
```

722 The primitive parameters are defined in Table 44.

8.3.3.2 When Generated

723 The Protocol Layer shall generate this primitive to set an MIB attribute indicated by MIBattribute parameter with the value of MIBvalue parameter. The Protocol Layer shall ensure that the requested MIBattribute exists and the MIBvalue is in valid range of the requested MIBattribute. A MODULE may not check the validity of

MIBattribute and MIBvalue. Undefined attribute names or out of range attribute values may result in malfunctioning of the MODULE. After issuing an M-CTRL-CFGSET.request primitive, the Protocol Layer shall wait for the M-CTRL-CFGSET.confirm primitive reception before issuing a new configuration service request.

8.3.3.3 Effect on Receipt

724 The MODULE shall set the specified MIBattribute with the value carried by MIBvalue in its MIB registry. If setting the value of an MIBattribute implies a specific action, then this action shall not be performed until the M-CTRL-CFGREADY.request primitive is received. The MODULE shall respond with M-CTRL-CFGSET.confirm after registering the MIBvalue for the requested attribute.

8.3.4 M-CTRL-CFGSET.confirm

725 This primitive confirms registering the attribute value based on the last issued request to set the value of an attribute in the MIB.

8.3.4.1 Semantics of the Service Primitive

726 The semantics of the M-CTRL-CFGSET.confirm primitive are as follows:

```
727 M-CTRL-CFGSET.confirm(
728                       )
```

729 This primitive has no parameter.

8.3.4.2 When Generated

730 This primitive shall be generated by a MODULE in response to the most recent M-CTRL-CFGSET.request by the Protocol Layer after setting the value of the requested MIBattribute.

8.3.4.3 Effect on Receipt

731 The Protocol Layer is informed about serving the M-CTRL-CFGSET.request issued previously. The Protocol Layer may issue another service request upon receiving this primitive.

8.3.5 M-CTRL-CFGREADY.request

732 This primitive requests a MODULE to update the operation settings of MIB attribute(s) with the corresponding MIB values that are issued through previous M-CTRL-CFGSET.request.

8.3.5.1 Semantics of the Service Primitive

733 The semantics of the M-CTRL-CFGREADY.request primitive are as follows:

```
734 M-CTRL-CFGREADY.request(
735                         )
```

736 This primitive has no parameter.

8.3.5.2 When Generated

737 The Protocol Layer shall issue this primitive after sending all setting requests to MIB attributes that compose a consistent new configuration parameter set. Issuing this primitive enables the MODULE to perform specific actions based on the MIB attributes set and the values assigned to these attributes. If a MODULE is in BURST state when this primitive is issued, then the Protocol Layer shall bring the MODULE into power saving state before specific actions can be taken and the new setting become effective.

8.3.5.3 Effect on Receipt

738 The MODULE shall perform specific actions, if any, required upon receiving this primitive, based on the configuration set requests received before. These actions shall be performed, if needed, when the MODULE is entering into or in power saving state.

8.3.6 M-CTRL-CFGREADY.confirm

739 This primitive reports the reception of M-CTRL-CFGREADY.request to update the operation settings to the configured MIB attribute(s).

8.3.6.1 Semantics of the Service Primitive

740 The semantics of the M-CTRL-CFGREADY.confirm primitive are as follows:

741 `M-CTRL-CFGREADY.confirm(`
742 `)`

743 This primitive has no parameter.

8.3.6.2 When Generated

744 This primitive shall be generated by the MODULE in response to the reception of M-CTRL-CFGREADY.request by the Protocol Layer.

8.3.6.3 Effect on Receipt

745 The Protocol Layer is informed about registering the M-CTRL-CFGREADY.request issued previously. Upon receiving this primitive, if the MODULE is in BURST state, then the Protocol Layer shall request the MODULE enter into power saving state.

8.3.7 M-CTRL-RESET.request

746 This primitive requests the MODULE reset to its Power-On Reset state. All previous configuration settings are lost.

8.3.7.1 Semantics of the Service Primitive

747 The semantics of the M-CTRL-RESET.request primitive are as follows:

748 `M-CTRL-RESET.request(`
749 `)`

750 This primitive has no parameter.

8.3.7.2 When Generated

751 The Protocol Layer issues this request when it is desired to reset the MODULE to its default state and settings.

8.3.7.3 Effect on Receipt

752 When the Protocol Layer issues this request, the MODULE shall enter into DISABLED state specified in Section 4.7.1.4.

8.3.8 M-CTRL-RESET.confirm

753 This primitive shall only be utilized for modeling purposes of Protocol Layer.

754 This primitive informs the Protocol Layer that the MODULE has completed previously requested RESET action and ready to service any request.

8.3.8.1 Semantics of the Service Primitive

755 The semantics of the M-CTRL-RESET.confirm primitive are as follows

```
756 M-CTRL-RESET.confirm(
757                              )
```

758 This primitive has no parameter.

8.3.8.2 When Generated

759 After a request from the Protocol Layer to reset the MODULE, the MODULE shall generate this primitive upon completion of initialization and ready to receive a service request.

8.3.8.3 Effect on Receipt

760 Upon receiving this primitive the Protocol Layer should aware that the MODULE has completed initialization, reset all configuration settings to default values and entered HIBERN8 state.

8.3.9 M-CTRL-LINERESET.request

761 This primitive requests an M-TX to perform a LINE-RESET action. All configuration (rates, amplitudes, etc.) settings are lost and reset to default values. The M-TX also asserts a signal on the LINE so that the remote M-RX recognizes the LINE-RESET state and acts accordingly.

8.3.9.1 Semantics of the Service Primitive

762 The semantics of the M-CTRL-LINERESET.request primitive are as follows:

```
763 M-CTRL-LINERESET.request(
764                              )
```

765 This primitive has no parameter.

8.3.9.2 When Generated

766 The Protocol Layer shall issue this request when it is desired to reset a LANE to the default state.

8.3.9.3 Effect on Receipt

767 Upon receiving this request, the M-TX shall perform LINE-RESET as described in Section 4.7.4.1.

8.3.10 M-CTRL-LINERESET.indication

768 This primitive reports to the Protocol Layer that the M-RX has been reset by a LINE-RESET

8.3.10.1 Semantics of the Service Primitive

769 The semantics of the M-CTRL-LINERESET.indication primitive are as follows:

```
770 M-CTRL-LINERESET.indication(
771                                )
```

772 This primitive has no parameter.

8.3.10.2 When Generated

773 When M-RX detects LINE-RESET as described in Section 4.7.4.1, it shall indicate the same to the Protocol Layer using this primitive.

8.3.10.3 Effect on Receipt

774 When the Protocol Layer receives this primitive, it should be aware that the LANE is reset by a LINE-RESET and both M-TX and M-RX on this LANE will be in default state with default attribute values.

8.3.11 M-CTRL-LINERESET.confirm

775 This primitive informs the Protocol Layer that the MODULE has completed a previously requested LINE-RESET action.

8.3.11.1 Semantics of the Service Primitive

776 The semantics of the M-CTRL-LINERESET.confirm primitive are as follows

```
777 M-CTRL-LINERESET.confirm(
778                           )
```

779 This primitive has no parameter.

8.3.11.2 When Generated

780 After a request from the Protocol Layer to an M-TX to reset the LANE by a LINE-RESET, the M-TX shall issue this primitive upon completion of the LINE-RESET operation as described in Section 4.7.4.1.

8.3.11.3 Effect on Receipt

781 Upon receiving this primitive the Protocol Layer should aware that the M-TX has completed LINE-RESET activity and reset all configuration settings to default values while entering into SLEEP state.

8.3.12 M-CTRL-LCCReadStatus.indication

782 This primitive informs the Protocol Layer that M-RX is received result of LCC-READ command, which is initiated at M-TX and the received result is set in the corresponding OMC Status attributes.

8.3.12.1 Semantics of the Service Primitive

783 The semantics of the M-CTRL-LCCReadStatus.indication primitive are as follows

```
784 M-CTRL-LCCReadStatus.indication(
785                                 )
```

786 This primitive has no parameter.

8.3.12.2 When Generated

787 M-RX shall generate this primitive when it detects a write operation to any of the OMC Status attributes that are listed in $$$.

8.3.12.3 Effect on Receipt

788 This primitive indicates to the Protocol Layer that an LCC-READ operation has been initiated at M-TX and the corresponding LCC-READ result is available through OMC Status attributes. Protocol Layer may read the value of OMC Status attributes using M-CTRL-CFGGET.request primitive before they are overwritten.

789 Whenever any member of a group is read via LCC-READ, all the members of the group are updated. Since a group of attributes are read at the same time, the OMC status attributes output might change after recieving another M-CNTRL-CFGGET.request primitive for that group.

8.3.13 Sequence of Service Primitives

790 The possible relationships among primitives at M-TX-CTRL SAP and M-RX-CTRL SAP are illustrated by the given time sequence diagrams shown in Figure 56. They also indicate a possible logical relationship in terms of time. Primitives that occur earlier in time and connected by dotted lines are logical predecessors of subsequent primitives.

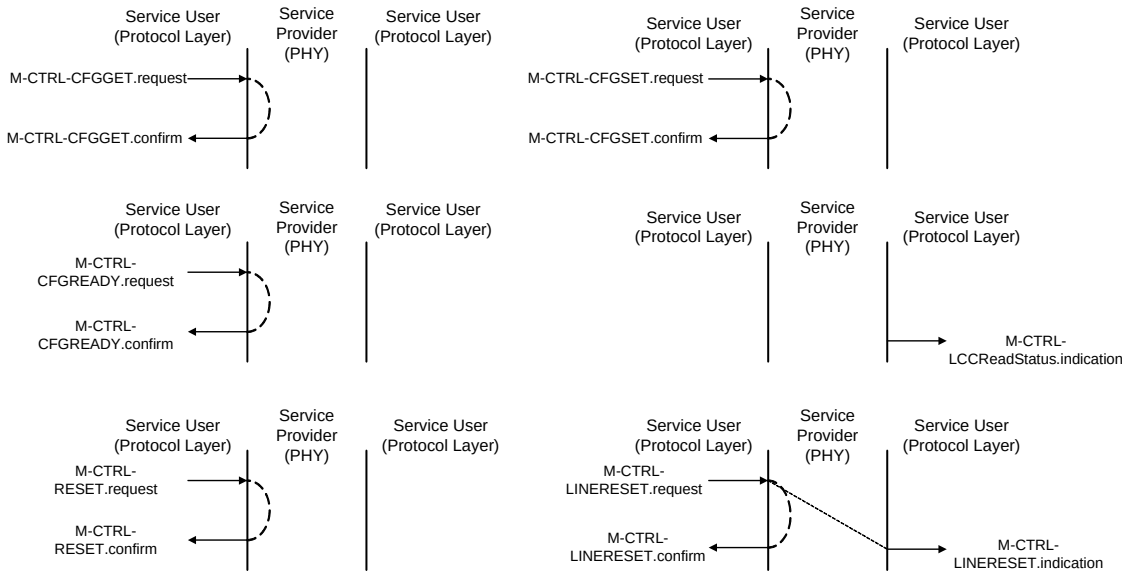


Figure 56 Sequence of Service Primitives at M-TX-CTRL SAP and M-RX-CTRL SAP

8.4 M-TX and M-RX Attributes

791 Capability, configuration and status attributes for an M-TX are listed in Table 45, Table 46, and Table 47, respectively, and for an M-RX these attributes are listed in Table 49, Table 50, and Table 51, respectively. Write-only and status attributes relevant to OMC are listed in Table 48, and Table 52, respectively. Capability attributes describe the capabilities of an implementation and shall be read-only. Currently, only one status attribute is defined for a MODULE to provide the current operating state of the MODULE. In case of an OMC, status attributes that are accessible at M-RX provide the result of an LCC-READ operation initiated at M-TX. No request, such as M-CTRL-CFGSET.request, shall be made by Protocol to write any value to any capability or status attribute. Any write request, such as M-CTRL-CFGSET.request, to a capability or status attribute shall be ignored and shall not be responded by a MODULE.

792 Configuration attributes are used for configuring a MODULE based on applicable capabilities, if there are any, to control its behavior. Configuration attributes shall be readable and writable. A write request, such as M-CTRL-CFGSET, to a configuration attribute shall hold a valid AttributeID and attribute value corresponding to that AttributeID. The attribute value shall not violate range of values of applicable capabilities, if any, for that attribute. Validity check of AttributeID and its corresponding value for a write request may not be performed in a MODULE. A read request, such as M-CTRL-CFGGET, to a configuration or capability attribute shall hold a valid AttributeID. Validity check of AttributeID for a read request may not be performed in a MODULE.

793 Write-only attributes of an OMC are used for configuring the OMC; there is no read function for reading configured write attribute data from an OMC to the M-RX. No request, such as M-CTRL-CFGGET.request, shall be made by the Protocol Layer to read a value from a write-only attribute. Any read request, such as M-CTRL-CFGGET.request, to a write-only attribute shall be ignored and shall not be responded by a MODULE.

794 The “Attribute Name” column in the tables specifies a symbolic name in a human readable form for an attribute.

795 The “AttributeID” column contains a hexadecimal code for an attribute which shall be used in read or write request made to an attribute. The parameter MIBattribute of M-CTRL-CFGGET.request and M-CTRL-CFGSET.request service primitives shall contain AttributeID of an attribute.

796 The “Description” column of an attribute provides a brief description of the attribute and four optional fields.

797 • The “*Existence depends on*” field of an attribute contains capability attributes that are applicable for its existence. An attribute becomes an Existence-dependant attribute if the “Description” contains an “Existence Depends on” field. An Existence-dependent attribute exists if all attributes listed in its “Existence Depends on” field are “TRUE”. Before making any read or write access to an existence dependant attribute, the Protocol shall ensure that all the applicable attributes for its existence are realizable to logical “TRUE” condition. If any of the attributes listed in the “Existence Depends on” field of an Existence-dependant attribute results in a logical “FALSE” condition then no access shall be made to that Existence-dependant attribute. For example, before accessing TX_HSGEAR_Capability attribute, TX_HSMODE_Capability attribute’s value is verified because the latter attribute is listed in the former attribute’s “Existence Depends on” field (see Table 45). The TX_HSGEAR_Capability attribute is accessed if and only if TX_HSMODE_Capability attribute’s value is “TRUE”.

798 • The “*Value depends on*” field of an attribute contains capability attributes that are applicable for defining its value. While writing to an attribute that has a “Value Depends on” field, the value being written to the attribute shall not exceed the worst case value limits defined for those capability attributes that are listed in its “Value Depends on” field. For example, to set TX_PWM_G1_SPINUP_TIME attribute’s value, TX_PWM_G1_SPINUP_TIME_Capability attribute’s value must be read as the latter attribute is listed in former attribute’s “Value Depends on” field. For example, if the value of TX_PWM_G1_SPINUP_TIME_Capability attribute is 14, then the value of TX_PWM_G1_SPINUP_TIME attribute must not be below 14 (worst case value limit).

799 • The “*Req’d Values*” field is applicable only to configuration attributes. If a configuration attribute is supported by a MODULE, then the MODULE shall support all values or range of values specified in the The “*Req’d Values*” field of that configuration attribute.

800 • The “*Reset Value*” field is applicable to configuration attributes only and specifies the default value of an attribute. A configuration attribute shall hold this default value after exiting the DISABLED state.

801 The “FSM” column of an attribute contains those FSM types that this attribute shall be applicable. So, this column specifies the validity of an attribute to be used in either TYPE-I or TYPE-II or both (TYPE-I and TYPE-II).

802 The “Type” column of an attribute specifies the type of data (as used in most common programming languages) it holds.

803 The “Bits” column of an attribute either recommends or mandates which bits to use for representing the possible values listed inside an attribute’s value range.

804 The “Range” column of an attribute specifies permissible limits of range of values that an attribute can take. Supported value range for an attribute shall not exceed the range of values specified in the “Range” column of that attribute.

Table 45 M-TX Capability Attributes

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
TX_HSMODE_Capability	0x01	Specifies support for HS-MODE.	Both	Bool	B[0][1]	FALSE = 0, TRUE = 1
TX_HSGEAR_Capability	0x02	Specifies supported HS-GEARs. *Existence depends on:* TX_HSMODE_Capability	Both	Enum	B[1:0][1]	HS_G1_ONLY = 1, HS_G1_TO_G2 = 2, HS_G1_TO_G3 = 3
TX_PWMG0_Capability	0x03	Specifies support for PWM-G0.	TYPE-I	Bool	B[0][1]	NO = 0, YES = 1
TX_PWMGEAR_Capability	0x04	Specifies support for PWM-GEARs other than PWM-G0.	TYPE-I	Enum	B[2:0][1]	PWM_G1_ONLY = 1, PWM_G1_TO_G2 = 2, PWM_G1_TO_G3 = 3, PWM_G1_TO_G4 = 4, PWM_G1_TO_G5 = 5, PWM_G1_TO_G6 = 6, PWM_G1_TO_G7 = 7
TX_Amplitude_Capability	0x05	Specifies supported signal amplitude levels.	Both	Enum	B[1:0][1]	SMALL_AMPLITUDE_ONLY = 1, LARGE_AMPLITUDE_ONLY = 2, LARGE_AND_SMALL_AMPLITUDE = 3
TX_ExternalSYNC_Capability	0x06	Specifies support for external SYNC pattern. *Existence depends on:* TX_HSMODE_Capability	Both	Bool	B[0]	FALSE = 0, TRUE = 1

Table 45 M-TX Capability Attributes (continued)

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
TX_HS_Unterminated_LINE_Drive_Capability	0x07	Specifies whether M-TX supports driving an unterminated LINE in HS-MODE or not. *Existence depends on:* TX_HSMODE_Capability	Both	Bool	B[0][1]	NO = 0, YES = 1
TX_LS_Terminated_LINE_Drive_Capability	0x08	Specifies whether M-TX supports driving a terminated LINE in LS-MODE or not.	Both	Bool	B[0][1]	NO = 0, YES = 1
TX_Min_SLEEP_NoConfig_Time_Capability	0x09	Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed.	Both	Int	B[3:0][1]	0 to 15
TX_Min_STALL_NoConfig_Time_Capability	0x0A	Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed.	Both	Int	B[3:0][1]	0 to 15
TX_Min_SAVE_Config_Time_Capability	0x0B	Specifies minimum reconfiguration time (in 40 ns steps). This applies only to SLEEP and STALL states.	Both	Int	B[7:0]	0 to 250 (10000 ns)
TX_REF_CLOCK_SHARED_Capability	0x0C	Specifies support for a shared reference Clock.	TYPE-I	Bool	B[0][1]	NO = 0, YES = 1

1. *Recommended bit assignment.*

Table 46 M-TX Configuration Attributes

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
TX_MODE	0x21	M-TX operating mode. *Existence depends on:* TX_HSMODE_Capability *Req'd Value:* LS_MODE *Reset Value:* LS_MODE	Both	Enum	B[1:0][1]	LS_MODE = 1, HS_MODE = 2
TX_HSRATE_Series	0x22	HS mode RATE series value of M-TX. *Existence depends on:* TX_HSMODE_Capability *Req'd Value:* A and B *Reset Value:* A	Both	Enum	B[1:0][1]	A = 1, B = 2
TX_HSGEAR	0x23	HS-GEAR value of M-TX. *Existence depends on:* TX_HSMODE_Capability *Value depends on:* TX_HSGEAR_Capability *Req'd Value:* HS_G1 *Reset Value:* HS_G1	Both	Enum	B[1:0][1]	HS_G1 = 1, HS_G2 = 2, HS_G3 = 3
TX_PWMGEAR	0x24	PWM-GEAR value of M-TX. *Value depends on:* TX_PWMGEAR_Capability, TX_PWMG0_Capability *Req'd Value:* PWM_G1 *Reset Value:* PWM_G1	TYPE-I	Enum	B[2:0][1]	PWM_G0 = 0, PWM_G1 = 1, PWM_G2 = 2, PWM_G3 = 3, PWM_G4 = 4, PWM_G5 = 5, PWM_G6 = 6, PWM_G7 = 7

Table 46 M-TX Configuration Attributes (continued)

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
TX_Amplitude	0x25	Type of drive strength on PINs at M-TX. *Value depends on:* TX_Amplitude_Capability *Reset Value:* LARGE_AMPLITUDE	Both	Enum	B[1:0][1]	SMALL_AMPLITUDE = 1, LARGE_AMPLITUDE = 2
TX_HS_SlewRate	0x26	Slew Rate control of M-TX output driver. *Existence depends on:* TX_HSMODE_Capability *Reset Value:* see [2]	Both	Enum	B[7:0][3]	0 to 255[4]
TX_SYNC_Source	0x27	Source of synchronization pattern at M-TX. *Existence depends on:* TX_HSMODE_Capability, TX_ExternalSync_Capability *Req'd Value:* INTERNAL_SYNC *Reset Value:* INTERNAL_SYNC	Both	Enum	B[0][1]	INTERNAL_SYNC = 0, EXTERNAL_SYNC = 1
TX_HS_SYNC_LENGTH	0x28	High Speed Synchronization pattern length of M-TX in SI. *Existence depends on:* TX_HSMODE_Capability *Req'd Values:* FINE, COARSE, 0 to 15[5] *Reset Values:* COARSE, 15	Both	Int	B[7:6]	FINE = 0, COARSE = 1
					B[5:0]	0 to 15[5]

Table 46 M-TX Configuration Attributes (continued)

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
TX_HS_PREPARE_LENGTH	0x29	HS prepare length in SI. *Existence depends on:* TX_HSMODE_Capability *Req'd Values:* 0 to 15[6] *Reset Value:* 15[6]	Both	Int	B[3:0][1]	0 to 15[6]
TX_LS_PREPARE_LENGTH	0x2A	PWM prepare time in SI. *Req'd Values:* 0 to 15[7] *Reset Value:* 15[7]	TYPE-I	Int	B[3:0][1]	0 to 15[7]
TX_HIBERNATE_Control	0x2B	M-TX HIBERN8 state control. *Req'd Values:* ENTER, EXIT *Reset Value:*EXIT	TYPE-I	Bool	B[0][1]	EXIT = 0, ENTER = 1
TX_LCC_Enable	0x2C	LCCs support by the M-TX. *Req'd Values:* YES, NO *Reset Value:* YES	TYPE-I	Bool	B[0][1]	NO = 0, YES = 1
TX_BURST_Closure_Extension	0x2D	BURST CLOSURE sequence is extended as long as the value of this attribute is TRUE. *Req'd Values:* FALSE, TRUE *Reset Value:* FALSE	TYPE-I	Bool	B[0][1]	FALSE = 0, TRUE = 1
TX_BYPASS_8B10B_Enable	0x2E	Enable/disable 8b10b encoding operation at M-TX. *Req'd Value:* FALSE *Reset Value:* FALSE	Both	Bool	B[0][1]	FALSE = 0, TRUE = 1

Table 46 M-TX Configuration Attributes (continued)

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
TX_DRIVER_POLARITY	0x2F	M-TX output driver polarity. *Req'd Values:* NORMAL, INVERTED *Reset Value:* NORMAL	Both	Enum	B[0][1]	NORMAL = 0, INVERTED = 1
TX_HS_Unterminated_LINE_Drive_Enable	0x30	Enable M-TX to drive unterminated LINE in HS-MODE. *Existence depends on:* TX_HSMODE_Capability, TX_HS_Unterminated_LINE_Drive_Capability *Req'd Values:* NO, YES *Reset Value:* NO	Both	Bool	B[0][1]	NO = 0, YES = 1
TX_LS_Terminated_LINE_Drive_Enable	0x31	Enable M-TX to drive terminated LINE in LS-MODE. *Existence depends on:* TX_LS_Terminated_LINE_Drive_Capability *Req'd Values:* NO, YES *Reset Value:* NO	Both		B[0][1]	NO = 0, YES = 1

Table 46 M-TX Configuration Attributes (continued)

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
TX_LCC_Sequencer	0x32	To set bits for carrying out multiple LCC-READ or LCC-WRITE operations. To perform an LCC operation the corresponding bit for this attribute shall be set. *Req'd Values:* READ-CAPABILITY, READ-MFG-INFO-A, READ-MFG-INFO-B, WRITE-ATTRIBUTE *Reset Values:* 0 (no LCC operation requested)	TYPE-I	Enum	B[7:0]	B[0] = 1: LCC READ-CAPABILITY requested, B[0] = 0: LCC READ-CAPABILITY not requested; B[1] = 1: LCC READ-MFG-INFO-A requested, B[1] = 0: LCC READ-MFG-INFO-A not requested; B[2] = 1: LCC READ-MFG-INFO-B requested, B[2] = 0: LCC READ-MFG-INFO-B not requested B[6:3]: Reserved and shall be set to 0b0000, B[7] = 1: LCC WRITE-ATTRIBUTE requested, B[7] = 0: LCC WRITE-ATTRIBUTE not requested

1. *Recommended bit assignment.*
2. *Implementation should ensure that the TX_HS_SlewRate value does not violate other parameter specifications*
3. *256 steps monotonically decreasing*
4. *"0" represents the fastest slew rate value and "255" represents the slowest slew rate value. Maximum number of possible steps are 256 (0 to 255). An implementation may support less than 256 steps but be able to interpret the 8-bit range.*
5. *Actual value is calculated as If (Bit[7:6] == COARSE); then $2^{(0b00101+Bit[5:0])}$-1; else Bit[5:0]).*
6. *Actual HS prepare length is calculated using the formula for $T_{HS\_PREPARE}$ in Table 6 with TX_HSGEAR*
7. *Actual PWM prepare length is calculated using the formula for $T_{PWM\_PREPARE}$ in Table 6 with TX_PWMGEAR*

Table 47 M-TX Status Attributes

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
TX_FSM_State	0x41	To read out the current state of M-TX	Both	Enum	B[3:0][1]	HIBERN8 = 0, SLEEP = 1, STALL = 2, LS-BURST = 3, HS-BURST = 4, LINE-CFG = 5

1. *Recommended bit assignment*

Table 48 OMC Write-only Attributes

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
MC_Output_Amplitude	0x61	Type of drive strength on PINs at OMC output. *Value depends on:* MC_RX_LA_Capability, MC_RX_SA_Capability *Reset Value:* LARGE_AMPLITUDE	TYPE-I	Enum	B[0][1]	SMALL_AMPLITUDE = 0, LARGE_AMPLITUDE = 1
MC_HS_Unterminated_Enable	0x62	Enable disconnection of resistive termination of O-TX in HS-MODE. *Existence depends on:* MC_HSMODE_Capability, MC_HS_Unterminated_Capability *Req'd Value:* OFF *Reset Value:* OFF	TYPE-I	Bool	B[0]	OFF = 0, ON = 1

Table 48 OMC Write-only Attributes (continued)

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
MC_LS_Terminated_Enable	0x63	Enable O-TX resistive termination in LS-MODE. *Existence depends on:* MC_LS_Terminated_Capability *Req'd Value:* OFF *Reset Value:* OFF	TYPE-I	Bool	B[0][1]	OFF = 0, ON = 1
MC_HS_Unterminated_LINE_Drive_Enable	0x64	Enable O-RX to drive unterminated LINE in HS-MODE. *Existence depends on:* MC_HSMODE_Capability, MC_HS_Unterminated_LINE_Drive_Capability *Req'd Value:* OFF *Reset Value:* OFF	TYPE-I	Bool	B[0][1]	OFF = 0, ON = 1
MC_LS_Terminated_LINE_Drive_Enable	0x65	Enable O-RX to drive terminated LINE in LS-MODE. *Existence depends on:* MC_LS_Terminated_LINE_Drive_Capability *Req'd Value:* OFF *Reset Value:* OFF	TYPE-I	Bool	B[0][1]	OFF = 0, ON = 1

1. *Recommended bit assignment.*

Table 49 M-RX Capability Attributes

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
RX_HSMODE_Capability	0x81	Specifies support for HS-MODE.	Both	Bool	B[0][1]	FALSE = 0, TRUE = 1

Table 49 M-RX Capability Attributes (continued)

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
RX_HSGEAR_Capability	0x82	Specifies supported HS-GEARs. *Existence depends on:* RX_HSMODE_Capability	Both	Enum	B[1:0][1]	HS_G1_ONLY = 1, HS_G1_TO_G2 = 2, HS_G1_TO_G3 = 3
RX_PWMG0_Capability	0x83	Specifies support for PWM-G0.	TYPE-I	Bool	B[0][1]	NO = 0, YES = 1
RX_PWMGEAR_Capability	0x84	Specifies supported PWM-GEARs other than PWM-G0.	TYPE-I	Enum	B[2:0][1]	PWM_G1_ONLY = 1, PWM_G1_TO_G2 = 2, PWM_G1_TO_G3 = 3, PWM_G1_TO_G4 = 4, PWM_G1_TO_G5 = 5, PWM_G1_TO_G6 = 6, PWM_G1_TO_G7 = 7
RX_HS_Unterminated_Capability	0x85	Specifies support for disconnection of resistive termination in HS-MODE. *Existence depends on:* RX_HSMODE_Capability	Both	Bool	B[0][1]	NO = 0, YES = 1
RX_LS_Terminated_Capability	0x86	Specifies support for enabling resistive termination in LS-MODE.	TYPE-I	Bool	B[0][1]	NO = 0, YES = 1
RX_Min_SLEEP_NoConfig_Time_Capability	0x87	Specifies minimum time (in SI) in SLEEP state needed when inline configuration was not performed.	Both	Int	B[3:0][1]	0 to 15
RX_Min_STALL_NoConfig_Time_Capability	0x88	Specifies minimum time (in SI) in STALL state needed when inline configuration was not performed.	Both	Int	B[3:0][1]	0 to 15
RX_Min_SAVE_Config_Time_Capability	0x89	Specifies minimum reconfiguration time (in 40 ns steps). This applies only to SLEEP and STALL states.	Both	Int	B[7:0]	0 to 250 (10000 ns)
RX_REF_CLOCK_SHARED_Capability	0x8A	Specifies support for a shared reference Clock.	TYPE-I	Bool	B[0][1]	NO = 0, YES = 1

Table 49 M-RX Capability Attributes (continued)

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
RX_HS_SYNC_LENGTH	0x8B	High Speed Synchronization pattern length in SI. *Existence depends on:* RX_HSMODE_Capability *Req'd Values:* None *Reset Value:* None	Both	Int	B[7:6]	FINE = 0, COARSE = 1
					B[5:0]	0 to 15[2]
RX_HS_PREPARE_LENGTH	0x8C	HS prepare length in SI. *Existence depends on:* RX_HSMODE_Capability *Req'd Values:* 0 to 15[3] *Reset Value:* 0 to 15[3]	Both	Int	B[3:0][1]	0 to 15[3]
RX_LS_PREPARE_LENGTH	0x8D	PWM prepare time in SI. *Req'd Values:* 0 to 15[4] *Reset Value:* 15[4]	TYPE-I	Int	B[3:0][1]	0 to 15[4]

1. *Recommended bit assignment.*
2. *Actual value shall be calculated as If (Bit[7:6] == COARSE); then $2^{(0b00101+Bit[5:0])}$-1; else Bit[5:0])*
3. *Actual HS prepare length is calculated using the formula for $T_{HS\_PREPARE}$ in Table 6 with RX_HSGEAR*
4. *Actual PWM prepare length is calculated using the formula for $T_{PWM\_PREPARE}$ in Table 6 with RX_PWMGEAR*

Table 50 M-RX Configuration Attributes

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
RX_MODE	0xA1	Operating mode. *Existence depends on:* RX_HSMODE_Capability *Req'd Value:* LS_MODE *Reset Value:* LS_MODE	Both	Enum	B[1:0][1]	LS_MODE = 1, HS_MODE = 2

Table 50 M-RX Configuration Attributes (continued)

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
RX_HSRATE_Series	0XA2	HS mode RATE series value. *Existence depends on:* RX_HSMODE_Capability *Req'd Values:* A and B *Reset Value:* A	Both	Enum	B[1:0][1]	A = 1, B = 2
RX_HSGEAR	0xA3	Current HS-GEAR. *Existence depends on:* RX_HSMODE_Capability *Value depends on:* RX_HSGEAR_Capability *Req'd Value:* HS_G1 *Reset Value:* HS_G1	Both	Enum	B[1:0][1]	HS_G1 = 1, HS_G2 = 2, HS_G3 = 3
RX_PWMGEAR	0xA4	Current PWM-GEAR. *Req'd Value:* PWM_G1 *Reset Value:* PWM_G1	TYPE-I	Enum	B[2:0][1]	PWM_G0 = 0, PWM_G1 = 1, PWM_G2 = 2, PWM_G3 = 3, PWM_G4 = 4, PWM_G5 = 5, PWM_G6 = 6, PWM_G7 = 7
RX_LS_Terminated_Enable	0xA5	Enable resistive termination of M-RX in LS-MODE. *Existence depends on:* RX_LS_Terminated_Capability *Req'd Value:* OFF *Reset Value:* OFF	TYPE-I	Bool	B[0][1]	OFF = 0, ON = 1

Table 50 M-RX Configuration Attributes (continued)

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
RX_HS_Unterminated_Enable	0xA6	Enable disconnection of resistive termination of M-RX in HS-MODE. *Existence depends on:* RX_HSMODE_Capability, RX_HS_Unterminated_Capability *Req'd Value:* OFF *Reset Value:* OFF	Both	Bool	B[0][1]	OFF = 0, ON = 1
RX_Enter_HIBERNATE	0xA7	M-RX entry to HIBERN8 state control. *Req'd Values:* YES, NO *Reset Value:* YES for Local-RESET, NO for LINE-RESET	TYPE-I	Bool	B[0][1]	NO = 0: Protocol Layer shall not set the value of this attribute to "NO". When the M-RX is in HIBERN8 state, upon squelch detection the M-RX exits HIBERN8 state (to SLEEP or STALL state) and resets this attribute value to NO, YES = 1: Can be set by the Protocol. The M-RX enters from SLEEP or STALL state to HIBERN8 state, if it is not already in HIBERN8 state.
RX_BYPASS_8B10B_Enable	0xA8	8b10b Decoding Enable. *Req'd Value:* FALSE *Reset Value:* FALSE	Both	Bool	B[0][1]	FALSE = 0, TRUE = 1

1. *Recommended bit assignment.*

Table 51 M-RX Status Attributes

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
RX_FSM_State	0xC1	To read out the current state of M-RX	Both	Enum	B[3:0][1]	HIBERN8 = 0, SLEEP = 1, STALL = 2, LS-BURST = 3, HS-BURST = 4, LINE-CFG = 5

1. *Recommended bit assignment*

Table 52 OMC Status Attributes

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
OMC_TYPE_Capability	0xD1	Specifies the type of OMC present.	TYPE-I	Enum	B[0][1]	ADVANCED = 0, BASIC = 1
MC_HSMODE_Capability	0xD2	Specifies whether or not OMC supports HS-MODE.	TYPE-I	Bool	B[0][1]	FALSE = 0, TRUE = 1
MC_HSBURST_Capability	0XD3	Specifies which HS-GEARs that OMC supports. *Existence depends on:* MC_HSMODE_Capability	TYPE-I	Enum	B[1:0][1]	HS_G1_ONLY = 1, HS_G1_TO_G2 = 2, HS_G1_TO_G3 = 3
MC_HS_START_TIME_Var_Capability	0xD4	Specifies High Speed start up time of OMC. *Existence depends on:* MC_HSMODE_Capability	TYPE-I	Int	B[3:0][1]	0 to 15

Table 52 OMC Status Attributes (continued)

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
MC_HS_START_TIME_Range_Capability	0xD5	Specifies the granularity that High Speed start up time OMC takes. *Existence depends on:* MC_HSMODE_Capability	TYPE-I	Bool	B[0][1]	FINE = 0, COARSE = 1
MC_RX_SA_Capability	0xD6	Specifies whether or not OMC supports Small Amplitude	TYPE-I	Bool	B[0][1]	FALSE = 0, TRUE = 1
MC_RX_LA_Capability	0xD7	Specifies whether or not OMC supports Large Amplitude	TYPE-I	Bool	B[0][1]	FALSE = 0, TRUE = 1
MC_LS_PREPARE_LENGTH	0xD8	Specifies OMC PREPARE length for PWM-BURST	TYPE-I	Bool	B[3:0]	0 to 15
MC_PWMG0_Capability	0xD9	Specifies whether or not OMC supports PWM-G0.	TYPE-I	Bool	B[0][1]	NO = 0, YES = 1
MC_PWMGEAR_Capability	0xDA	Specifies which PWM-GEARs other than PWM-G0 are supported by OMC	TYPE-I	Enum	B[2:0][1]	PWM_G1_ONLY = 1, PWM_G1_TO_G2 = 2, PWM_G1_TO_G3 = 3, PWM_G1_TO_G4 = 4, PWM_G1_TO_G5 = 5, PWM_G1_TO_G6 = 6, PWM_G1_TO_G7 = 7
MC_LS_Terminated_Capability	0xDB	Specifies whether or not O-TX supports enabling of resistive termination in PWM-MODE	TYPE-I	Bool	B[0][1]	NO = 0, YES = 1
MC_HS_Unterminated_Capability	0xDC	Specifies support for disconnection of resistive termination in HS-MODE by O-TX. *Existence depends on:* MC_HSMODE_Capability	TYPE-I	Bool	B[0][1]	NO = 0, YES = 1

Table 52 OMC Status Attributes (continued)

Attribute Name	AttributeID	Description	FSM	Type	Bits	Range
MC_LS_Terminated_LINE_Drive_Capability	0xDD	Specifies whether or not O-RX supports driving a terminated LINE in PWM-MODE.	TYPE-I	Bool	B[0][1]	NO = 0, YES = 1
MC_HS_Unterminated_LINE_Drive_Capability	0xDE	Specifies whether or not O-RX supports driving a unterminated LINE in HS-MODE. *Existence depends on:* MC_HSMODE_Capability	TYPE-I	Bool	B[0][1]	NO = 0, YES = 1
MC_MFG_ID_Part1	0xDF	Manufacturer identification least significant byte	TYPE-I	Int	B[7:0]	0 to 255
MC_MFG_ID_Part2	0xE0	Manufacturer identification most significant byte	TYPE-I	Int	B[7:0]	0 to 255
MC_Vendor_Info_Part1	0xE1	Vendor specific information least significant byte	TYPE-I	Int	B[7:0]	0 to 255
MC_Vendor_Info_Part2	0xE2	Vendor specific information most significant byte	TYPE-I	Int	B[7:0]	0 to 255
MC_Ext_Vendor_Info_Part1	0xE3	Extended vendor specific information least significant byte	TYPE-I	Int	B[7:0]	0 to 255
MC_Ext_Vendor_Info_Part2	0xE4	Extended vendor specific information second least significant byte	TYPE-I	Int	B[7:0]	0 to 255
MC_Ext_Vendor_Info_Part3	0xE5	Extended vendor specific information third least significant byte	TYPE-I	Int	B[7:0]	0 to 255
MC_Ext_Vendor_Info_Part4	0xE6	Extended vendor specific information most significant byte	TYPE-I	Int	B[7:0]	0 to 255

1. *Recommended bit assignment.*

Annex A Signaling Interface Description (normative)

805 The signaling interfaces described in this annex are optional. However, if a MODULE includes these interfaces it shall implement them as described in this annex.

806 The signaling interface for a MODULE (M-TX or M-RX) consists of two independent interfaces for control service primitives (M-TX-CTRL SAP and M-RX-CTRL SAP) and for data transfer service primitives (M-TX-DATA SAP and M-RX-DATA SAP). An M-PORT with multiple M-TXs or M-RXs uses a set of signals defined for M-TX or M-RX for each MODULE. To keep the same structure used for SAP definitions, the signaling interface of a MODULE is divided into DATA and CTRL signaling interfaces.

807 A shadow memory bank inside the MODULE implements the OFFLINE-SET and INLINE-CR registries as defined in Section 4.8.1, and a separate effective configuration bank implements the INLINE-SET registry. Both the shadow memory and the effective configuration banks are written sequentially. However the entire contents of the shadow memory bank can be uploaded to the effective configuration bank in a single Protocol Layer-requested step. For maximum implementation versatility, the effective configuration bank can be accessed directly by the Protocol Layer as well. However, the Protocol Layer shall ensure that direct updates to this bank, through either direct access or shadow memory upload, take place only in STALL, SLEEP or HIBERN8 states.

808 Due to the high data rates supported in M-PHY implementations, the width of the data buses conveying data to and from the Physical Layer can be increased, and different parallelization options are provided.

809 Finally, testability extensions to the CTRL signal interface are also included in this specification. However, the definition of the internal M-RX and M-TX structures controlled by these extensions is out of scope for this document.

810 Section A.2 and Section A.3 define the signals used in the signaling interface of an M-TX, and M-RX, respectively. While the CTRL signaling interfaces for M-TXs and M-RXs cannot be identical, this annex provides a common signal definition for M-TX-CTRL SAP and M-RX-CTRL SAP to the furthest extent possible. M-TX-DATA SAP and M-RX-DATA SAP signaling interfaces are, by their nature, substantially different.

A.1 One-Hot Coding of Control Symbols

811 Table 53 defines the One-Hot coding of control symbols.

Table 53 One-Hot Coding of Control Symbols

One-Hot Code	Type of Control Symbol at TX	Type of Control Symbol at RX
0000 0000	Reserved	Reserved Symbol Error
0000 0001	MARKER0	MARKER0
0000 0010	MARKER1	MARKER1
0000 0100	MARKER2	MARKER2
0000 1000	Reserved	Reserved
0001 0000	Reserved	Reserved
0010 0000	Reserved	Reserved
0100 0000	Reserved	Reserved
1000 0000	FILLER	FILLER

A.2 The M-RX Signaling Interface

812 A schematic overview of the M-RX signaling interface is shown in Figure 57.

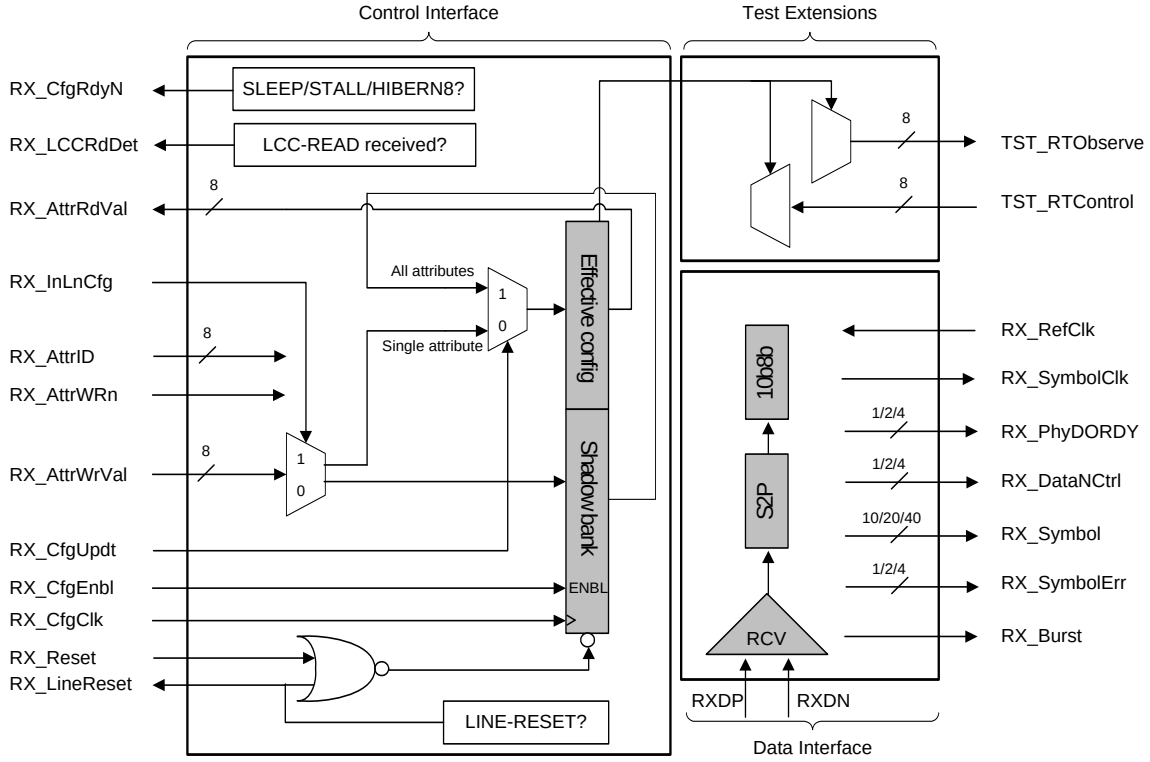


Figure 57 M-RX Signal Interfaces Diagram

A.2.1 M-RX Signal Description

813 In Table 54 through Table 56, entries in the “Direction” column specifies the direction of each signal from the perspective of the M-RX. An input signal (abbreviated as “I”) is driven by the Protocol Layer. An output signal (abbreviated as “O”) is driven by the M-RX.

814 The “Detection Type” column indicates the relevant condition for a given signal. A Detection Type of “Level” means the relevant information is either a high or low level on the signal. A Detection Type of “Transition” means a change from high-to-low or low-to-high causes the described action. A Detection Type of “Clock” indicates the signal is used to synchronize other signals on the interface. A Detection Type of “Asynch” means the signal changes state asynchronously to the relevant clock signal.

Table 54 M-RX-CTRL Interface Signals

Signal Name	Direction	Detection Type	Width	Signal Description
RX_CfgClk	I	Clock	1	Control Interface Clock. All M-RX-CTRL interface signals, with the exception of RX_Reset, are synchronous with this signal. The exact frequency of RX_CfgClk is implementation specific, but shall not be lower than 400 KHz to allow for squelch detection, adequate measurement of $T_{LINE-RESET}$, and LCC-READ event signaling. RX_CfgClk should have a minimum frequency of 10 MHz to prevent very high interface access latencies. RX_CfgClk shall be available in all M-RX power states except DISABLED and UNPOWERED.
RX_Reset	I	Asynch	1	RX_Reset is the active-high asynchronous reset for all logic inside the M-RX. RX_Reset implements the Local RESET function as defined in Section 4.7. The Protocol Layer, or other source, shall set RX_Reset to “1” for at least 100 ns.
RX_LineReset	O	Transi-tion	1	RX_LineReset indicates the status of the LINE-RESET process in the M-RX. M-RX shall set RX_LineReset to “1” when LINE-RESET is detected. M-RX shall set RX_LineReset to “0” once it has transitioned to the LINE-RESET exit state (see Section 4.7.4.1).
RX_AttrID	I	Level	8	RX_AttrID carries the Attribute ID of M-RX Configuration attributes for read or write operations, or M-RX Capability attribute or OMCS Status Attributes for read operation.
RX_AttrRdVal	O	Level	8	RX_AttrRdVal carries the attribute value read from an M-RX-MIB attribute specified by RX_AttrID. The M-RX-MIB attribute value should be held on this bus until a subsequent read command is issued by the protocol. The M-RX shall provide the specified attribute value within one-half of the RX_CfgClk period.
RX_AttrWrVal	I	Level	8	RX_AttrWrVal carries the attribute value to write to an M-RX-MIB attribute specified by RX_AttrID.
RX_AttrWRn	I	Level	1	RX_AttrWRn specifies the operation, read or write, to perform on an M-RX-MIB attribute. The Protocol Layer shall set RX_AttrWRn to “0” to indicate a read operation. The Protocol Layer shall set RX_AttrWRn to “1” to indicate a write operation.

Table 54 M-RX-CTRL Interface Signals (continued)

Signal Name	Direction	Detection Type	Width	Signal Description
RX_CfgEnbl	I	Level	1	Config Enable The Protocol Layer shall set RX_CfgEnbl to “1” for a single RX_CfgClk cycle to perform an attribute read, or write, operation. The Protocol Layer shall set RX_CfgEnbl, RX_AttrID, RX_AttrWRn, RX_InLnCfg and RX_AttrWrVal in the same RX_CfgClk cycle.
RX_InLnCfg	I	Level	1	RX_InLnCfg is used in conjunction with RX_AttrWRn and RX_CfgEnbl to direct an M-RX-MIB write operation to the M-RX's shadow memory bank or to the M-RX's effective configuration bank. The Protocol Layer shall set RX_InLnCfg to “0” to write to the M-RX shadow memory bank. The Protocol Layer shall set RX_InLnCfg to “1” to read, or write, the M-RX effective configuration bank. An attribute write operation to the M-RX effective configuration bank should only take effect when the M-RX is in SLEEP, STALL, or HIBERN8 states. The M-RX may ignore such an operation if it is performed during any other state. ***Note:*** *The Protocol Layer can only read from the M-RX's effective configuration bank, not from the shadow memory.*
RX_CfgUpdt	I	Transi-tion	1	RX_CfgUpdt transfers the contents of the shadow memory to the effective configuration bank. The Protocol Layer shall set RX_CfgUpdt to “1” for a single RX_CfgClk cycle to trigger the upload of the entire M-RX shadow memory contents to the effective configuration bank. While RX_InLnCfg allows for single attributes to be written directly to the M-RX effective configuration bank, e.g. dithering control between HS-BURSTs, RX_CfgUpdt allows the Protocol Layer to make configuration changes to the M-RX's shadow memory sequentially, then make the changes effective atomically.

Table 54 M-RX-CTRL Interface Signals (continued)

Signal Name	Direction	Detection Type	Width	Signal Description
RX_CfgRdyN	O	Level	1	RX_CfgRdyN indicates the M-RX cannot process a register write command to its effective configuration bank. The M-RX shall set this signal to “1” in the same RX_CfgClk cycle that triggers its internal FSM exit from the SLEEP, STALL, or HIBERN8 state to any other state. The M-RX may also set this signal to “1” while it is processing a Protocol-issued change to its effective configuration bank. The M-RX shall only set this signal to “0” when its internal FSM is in SLEEP, STALL, or HIBERN8 state and the MODULE is ready to accept a register write command to any register of its effective configuration bank. For a RX_Reset (Local Reset) command, the M-RX shall set RX_CfgRdyN to “1” asynchronously. The Protocol Layer shall not issue write commands to the M-RX effective configuration bank (including RX_CfgUpdt) until the M-RX sets RX_CfgRdyN to “0”. The M-RX shall respond to read commands from the Protocol Layer regardless of the value of RX_CfgRdyN. The M-RX shall process register write commands to its shadow memory bank regardless of the value of RX_CfgRdyN.
RX_LCCRdDet	O	Transi-tion	1	RX_LCCRdDet indicates the M-RX received an LCC-READ sequence, which results in the update of corresponding attributes in the M-RX. The M-RX shall set RX_LCCRdDet to “1” for a single RX_CfgClk cycle for each LCC-READ sequence detected. Cascaded LCC-READ sequences result in the M-RX asserting and deasserting RX_LCCRdDet as many times as the number of sequences received.

Table 55 M-RX-DATA Interface Signals

Signal Name	Direction	Detection Type	Width	Signal Description
RX_RefClk	I	Clock	1	Reference Clock. RX_RefClk may not be accessible in the M-RX-DATA interface for an M-PHY implementation that comprises an integrated clock multiplier. RX_RefClk shall have no specific phase relationship requirement to any signal in the M-RX-DATA interface.
RX_SymbolClk	O	Clock	1	Symbol Clock All M-RX-DATA interface signals are synchronous with this signal. The M-RX may disable RX_SymbolClk generation when the M-RX is not in LINE-CFG, PWM-BURST, SYS-BURST, or HS-BURST states. The M-RX shall provide the minimum number of cycles to transfer all M-RX data to the Protocol Layer. RX_SymbolClk shall have a period of 10 UI for a 10-bit RX_Symbol bus, 20 UI for a 20-bit RX_Symbol bus, or 40 UI for a 40-bit RX_Symbol bus. The behavior of RX_SymbolClk must be glitch-free even when this signal is being enabled or disabled. The M-RX shall not provide a RX_SymbolClk “1” or “0” pulse with a duration less than one-quarter of the nominal RX_SymbolClk period.
RX_Symbol	O	Level	10, 20, or 40	RX_Symbol is used for BURST data transfer to the Protocol Layer. The contents of this bus depend on the interface width (10, 20 or 40 bits, corresponding to 1, 2 and 4 parallel symbols, respectively), and also on whether or not the 10b8b decoding function is bypassed. When the 10b8b decoding function is disabled, RX_Symbol carries the raw data as received on the LINEs, parallelized according to the implemented width. The LSb of RX_Symbol shall correspond to the earliest received bit. When the 10b8b decoding function is enabled, only the 8, 16, or 32 LSbs of RX_Symbol are used to carry the decoded DATA or control symbol. The M-RX shall set the remaining MSbs to “0”. Control symbols shall be decoded as listed in Table 53.

Table 55 M-RX-DATA Interface Signals (continued)

Signal Name	Direction	Detection Type	Width	Signal Description
RX_PhyDORDY	O	Level	1, 2 or 4	PHY Data Output Ready RX_PhyDORDY indicates data is available in the corresponding RX_Symbol bus range. The width of RX_PhyDORDY is one, two or four bits depending on the RX_Symbol bus width of 10, 20, or 40 bits, respectively. Each bit in RX_PhyDORDY corresponds to a 10b8b symbol in RX_Symbol bus. RX_PhyDORDY bit — RX_Symbol bits (10b8b enabled) 0 — bits[9:0] (bits[7:0]) 1 — bits[19:10] (bits[15:8]) 2 — bits[29:20] (bits[23:16]) 3 — bits[39:30] (bits[32:24]) The M-RX shall set each bit of RX_PhyDORDY to “1” for every RX_SymbolClk cycle that the corresponding RX_Symbol bus range contains new data. The M-RX shall set each bit of RX_PhyDORDY bit to “0” for every RX_SymbolClk cycle that the corresponding RX_Symbol bus range does not contain new data. The Protocol Layer shall always be ready to consume the data from the M-RX.
RX_DataNCtrl	O	Level	1, 2 or 4	RX_DataNCtrl indicates the type of symbol on the indicated range of RX_Symbol. The width of RX_DataNCtrl is one, two or four bits depending on the RX_Symbol bus width of 10, 20, or 40 bits, respectively. RX_DataNCtrl are mapped the same as RX_PhyDORDY. The M-RX shall set the corresponding bit of RX_DataNCtrl to “0” when the related RX_Symbol bus range carries a data symbol. The M-RX shall set the corresponding bit of RX_DataNCtrl to “1” when the related RX_Symbol bus range carries a control symbol or a reserved symbol which was erroneously received (see RX_SymbolErr definition). The M-RX shall set all bits of RX_DataNCtrl to “0” when 10b8b decoding is bypassed.

Table 55 M-RX-DATA Interface Signals (continued)

Signal Name	Direction	Detection Type	Width	Signal Description
RX_SymbolErr	O	Level	1, 2 or 4	The width of RX_SymbolErr is one, two or four bits depending on the RX_Symbol bus width of 10, 20, or 40 bits, respectively. The M-RX shall set each bit of RX_SymbolErr to “1” for one RX_SymbolClk cycle when any of the following conditions on the corresponding RX_Symbol bus range are “TRUE”: • The 3b4b sub-block is in error while decoding the related 8b10b symbol received over the LINE • The 5b6b sub-block is in error while decoding the related 8b10b symbol received over the LINE • The Running Digital Sum algorithm computes an RDS error for the related 8b10b symbol received over the LINE • The related 8b10b symbol received over the LINE is a reserved symbol The M-RX shall set all bits of RX_SymbolErr to “0” for all other conditions. RX_Symbol shall carry, in the corresponding bus range, the re-mapped payload byte except for the case of a Reserved Symbol error. In this case, the corresponding range of RX_Symbol shall be set to 0x00 while the corresponding RX_DataN_Ctrl bit is set to “1” for one RX_SymbolClk cycle. The M-RX shall set all bits of RX_SymbolErr to “0” when 10b8b decoding is bypassed.
RX_Burst	O	Transi-tion	1	RX_Burst provides a framing window to the Protocol Layer for received BURSTs. The M-RX shall set RX_Burst to “1” when it detects the start of a PREPARE period. The M-RX shall set RX_Burst to “0” when it detects any of the BURST exit conditions (see Section 4.7.2) and all 8b10b payload data has been sent to the Protocol Layer via RX_Symbol.

Table 56 M-RX Test Extensions

Signal Name	Direction	Detection Type	Width	Signal Description
TST_RTObserve	O	Asynch	8	TST_RTObserve makes internal M-RX real-time signals observable, e.g. through DMA, by the Protocol Layer, or external test equipment. These signals are asynchronous to any clock on the M-RX-DATA or M-RX-CTRL interfaces. Signals are selected by programming implementation-specific M-RX registers using the M-RX-CTRL interface. The M-RX implementation shall not require TST_RTObserve for normal operation.
TST_RTControl	I	Asynch	8	TST_RTControl carries real-time signals to control implementation-specific signals, e.g. test features, inside the M-RX. These signals are asynchronous to any clock on the M-RX-DATA or M-RX-CTRL interfaces. Internal multiplexers with signals on this bus are selected by programming implementation-specific M-RX registers using the M-RX-CTRL interface. The M-RX implementation shall not require any specific behavior or value on TST_RTControl for normal operation.

A.3 The M-TX Signaling Interface

815 A schematic overview of the M-TX signaling interface is shown in Figure 58.

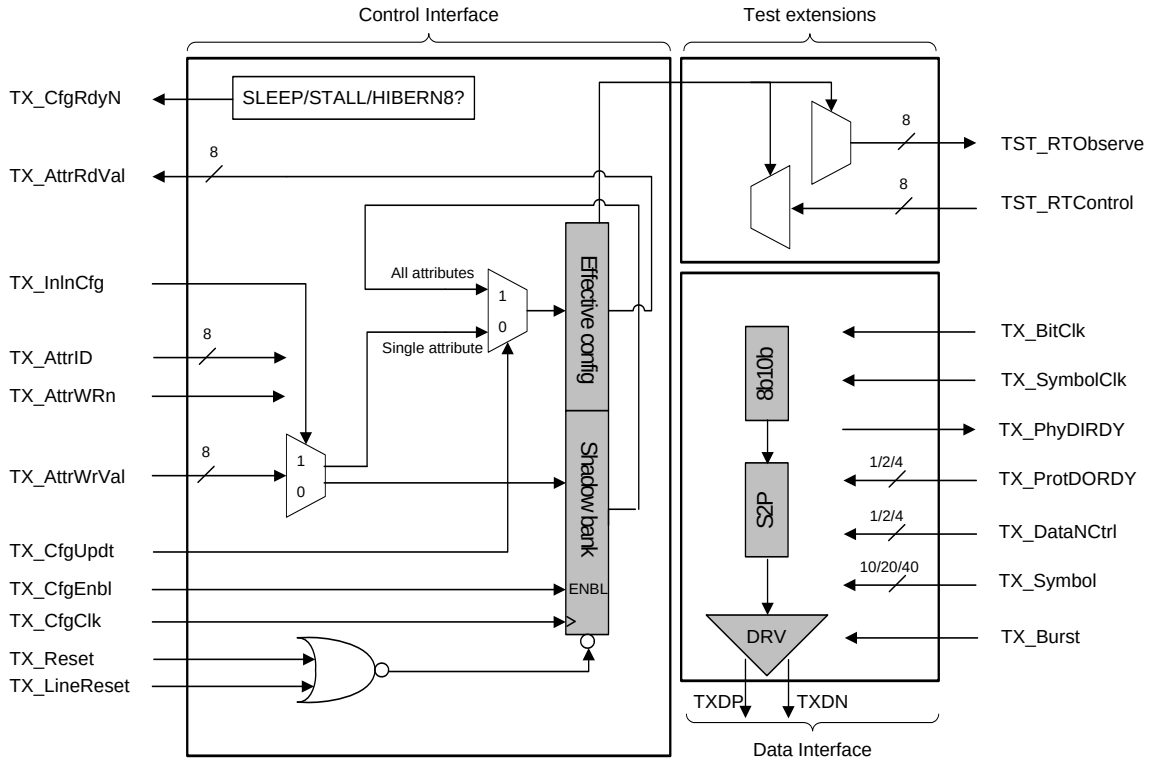


Figure 58 M-TX Signal Interfaces Diagram

A.3.1 M-TX Signaling Interface

816 In Table 57 through Table 59, entries in the “Direction” column specifies the direction of each signal from the perspective of the M-TX. An input signal (abbreviated as “I”) is driven by the Protocol Layer. An output signal (abbreviated as “O”) is driven by the M-TX.

817 The “Detection Type” column indicates the relevant condition for a given signal. A Detection Type of “Level” means the relevant information is either a high or low level on the signal. A Detection Type of “Transition” means a change from high-to-low or low-to-high causes the described action. A Detection Type of “Clock” indicates the signal is used to synchronize other signals on the interface. A Detection Type of “Asynch” means the signal changes state asynchronously to the relevant clock signal.

Table 57 M-TX-CTRL Interface Signals

Signal Name	Direction	Detection Type	Width	Signal Description
TX_CfgClk	I	Clock	1	Identical behavior as RX_CfgClk
TX_Reset	I	Asynch	1	Identical behavior as RX_Reset
TX_AttrID	I	Level	8	Identical behavior as RX_AttrID
TX_AttrRdVal	O	Level	8	Identical behavior as RX_AttrRdVal
TX_AttrWrVal	I	Level	8	Identical behavior as RX_AttrWrVal

Table 57 M-TX-CTRL Interface Signals (continued)

Signal Name	Direction	Detection Type	Width	Signal Description
TX_AttrWRn	I	Level	1	Identical behavior as RX_AttrWRn
TX_CfgEnbl	I	Level	1	Identical behavior as RX_CfgEnbl
TX_InLnCfg	I	Level	1	Identical behavior as RX_InLnCfg
TX_CfgUpdt	I	Transition	1	Identical behavior as RX_CfgUpdt
TX_CfgRdyN	O	Level	1	Identical behavior as RX_CfgRdyN
TX_LineReset	I	Transition	1	TX_LineReset triggers the M-TX to issue a LINE-RESET sequence. The M-TX shall issue a LINE-RESET sequence when the Protocol Layer sets TX_LineReset to “1” for one TX_CfgClk cycle.

Table 58 M-TX-DATA Interface Signals

Signal Name	Direction	Detection Type	Width	Signal Description
TX_BitClk	I	Clock	1	Bit Clock TX_BitClk is used to transmit data bits over the LINEs. TX_BitClk may not be accessible in the M-TX-DATA interface for M-PHY implementations that comprise an integrated clock multiplier. TX_BitClk shall have no specific phase relationship requirement to any signal in the M-TX-DATA interface.

Table 58 M-TX-DATA Interface Signals (continued)

Signal Name	Direction	Detection Type	Width	Signal Description
TX_SymbolClk	I	Clock	1	Symbol Clock All M-TX-DATA interface signals are synchronous with this signal. The Protocol Layer may disable TX_SymbolClk generation when the M-TX is not in LINE-CFG, PWM-BURST, SYS-BURST, or HS-BURST states. For this purpose, the Protocol Layer shall read the M-TX FSM state attribute. TX_SymbolClk shall have a period of 10 UI for a 10-bit TX_Symbol bus, 20 UI for a 20-bit RX_Symbol bus, or 40 UI for a 40-bit RX_Symbol bus. The behavior of TX_SymbolClk must be glitch-free even when this signal is being enabled or disabled. The Protocol Layer shall not provide a TX_SymbolClk “1” or “0” pulse with a duration less than one-quarter of the nominal TX_SymbolClk period.
TX_PhyDIRDY	O	Level	1	PHY Data Input Ready TX_PhyDIRDY indicates the M-TX is ready to accept new data on the TX_Symbol bus. The M-TX shall set TX_PhyDIRDY to “1” when the M-TX is ready to consume data. The M-TX shall set TX_PhyDIRDY to “0” when the M-TX is busy. The Protocol Layer should not update TX_Symbol while TX_PhyDIRDY is “0”.
TX_Symbol	I	Level	10, 20 or 40	TX_Symbol is used for BURST data transfer to the M-TX. The contents of this bus depend on the interface width (10, 20 or 40 bits, corresponding to 1, 2 and 4 parallel symbols, respectively), and also on whether the 8b10b encoding function in the M-TX is bypassed. When the M-TX 8b10b encoding function is bypassed, TX_Symbol carries the raw data to send on the LINEs, parallelized according to the implemented width. The LSb of TX_Symbol shall correspond to the earliest transmitted bit. When the M-TX 8b10b encoding function is enabled, only the 8, 16, or 32 LSbs of TX_Symbol are used to carry the unencoded DATA or control symbol. The M-TX shall ignore the unused MSbs of TX_Symbol. The Protocol Layer should set the unused MSbs to “0”. Control symbols shall be encoded as listed in Table 53.

Table 58 M-TX-DATA Interface Signals (continued)

Signal Name	Direction	Detection Type	Width	Signal Description
TX_ProtDORDY	I	Level	1, 2 or 4	PHY Data Output Ready TX_ProtDORDY indicates data is available in the corresponding TX_Symbol bus range. The width of the TX_ProtDORDY is one, two or four bits depending on the TX_Symbol bus width of 10, 20, or 40 bits, respectively. Each bit in TX_ProtDORDY corresponds to the 8b10b symbol in TX_Symbol bus. TX_ProtDORDY bit — TX_Symbol bits (8b10b enabled) 0 — bits[9:0] (bits[7:0]) 1 — bits[19:10] (bits[15:8]) 2 — bits[29:20] (bits[23:16]) 3 — bits[39:30] (bits[32:24]) The Protocol Layer shall set each bit of TX_ProtDORDY to “1” for every TX_SymbolClk cycle when the corresponding TX_Symbol bus range contains new data. The Protocol Layer shall set each bit of TX_ProtDORDY bit to “0” for every TX_SymbolClk cycle when the corresponding TX_Symbol bus range does not contain new data.
TX_DataNCtrl	I	Level	1, 2 or 4	TX_DataNCtrl indicates the type of symbol on the indicated range of TX_Symbol. The width of the TX_DataNCtrl is one, two or four bits depending on the TX_Symbol bus width of 10, 20, or 40 bits, respectively. The bits of TX_DataNCtrl are mapped the same as the bits of TX_ProtDORDY. The Protocol Layer shall set the corresponding bit of TX_DataNCtrl to “0” when the related TX_Symbol bus range carries a data symbol. The Protocol Layer shall set the corresponding bit of TX_DataNCtrl to “1” when the related TX_Symbol bus range carries a control symbol. The Protocol Layer should set all bits of TX_DataNCtrl to “0” when 8b10b encoding is bypassed. The M-TX shall ignore all bits of TX_DataNCtrl when 10b8b decoding is bypassed.

Table 58 M-TX-DATA Interface Signals (continued)

Signal Name	Direction	Detection Type	Width	Signal Description
TX_Burst	I	Transi-tion	1	TX_Burst initiates a BURST. The Protocol Layer shall set TX_Burst to “1” to initiate a BURST, and hold the value for the duration of the BURST. Once TX_Burst is set to “1”, the M-TX shall send the PREPARE sequence (and SYNC sequence in the case of a HS-BURST), followed by data or FILLER symbols. If any bit of TX_ProtDORDY is set to “1”, the M-TX shall send the data present on the corresponding TX_Symbol bus range. If any bit of TX_ProtDORDY is set to “0”, the M-TX shall send one FILLER for each TX_ProtDORDY bit set to 0. Once TX_Burst is set to “0”, the M-TX shall send the TAIL-OF-BURST sequence (see Section 4.7.2.3).

Table 59 M-TX Test Extensions

Signal Name	Direction	Detection Type	Width	Signal Description
TST_RTObserve	O	Asynch	8	Identical behavior as in M-RX interface
TST_RTControl	I	Asynch	8	Identical behavior as in M-RX interface

A.4 Interface Usage Examples

818 To aid in the design of a conformant implementation, the following use-cases are provided depicting the required interface behavior.

A.4.1 Attribute Read from Shadow Memory and Effective Configuration

819 Figure 59 shows an example of an attribute read from the M-RX. The example shows the M-RX effective configuration bank being read regardless of RX_CfgRdyN value.

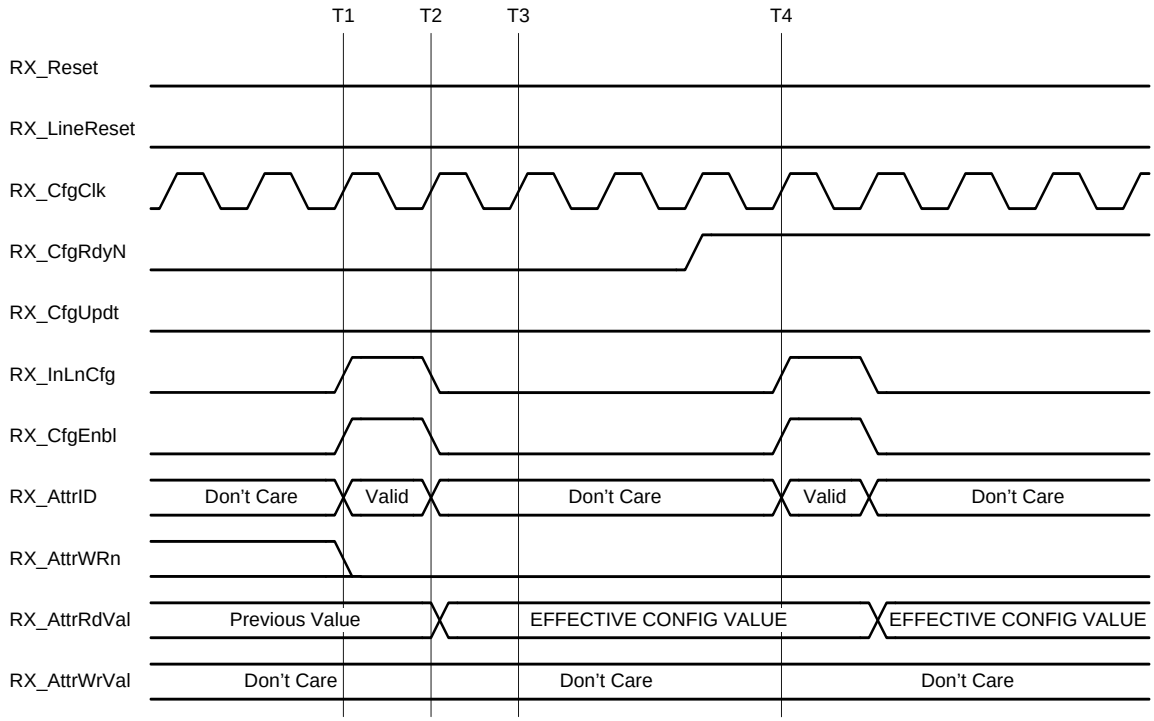


Figure 59 Interface Behavior for Attribute Read Operations

820 At T1, on the rising edge of RX_CfgClk, the Protocol Layer sets RX_CfgEnbl to "1", sets RX_AttrWRn to and RX_InLnCfg to "0", and sets the value of RX_AttrID to the attribute identifier.

821 At T2, on the rising edge of RX_CfgClk, the M-RX captures the command. In response, the M-RX updates RX_AttrRdVal with the effective configuration bank attribute value. Also at T2, the Protocol Layer sets RX_CfgEnbl and RX_InLnCfg to "0" on the rising edge of RX_CfgClk.

822 At T3, the Protocol Layer can capture RX_AttrRdVal. The M-RX holds the value on RX_AttrRdVal until a subsequent read operation, or Local Reset.

823 At T4, on the rising edge of RX_CfgClk, the Protocol Layer initiates a second read operation. In this instance, the M-RX has set RX_CfgRdyN set to "1" indicating it cannot process a write operation. Note that the read operation is unaffected by the RX_CfgRdyN signal.

A.4.2 Attribute Write to Shadow Memory and Effective Configuration

824 Figure 60 shows two attribute writes to the M-RX. In this use-case, an attribute in the shadow memory bank is updated independently of RX_CfgRdyN, then an effective configuration bank attribute is updated only when RX_CfgRdyN is "0".

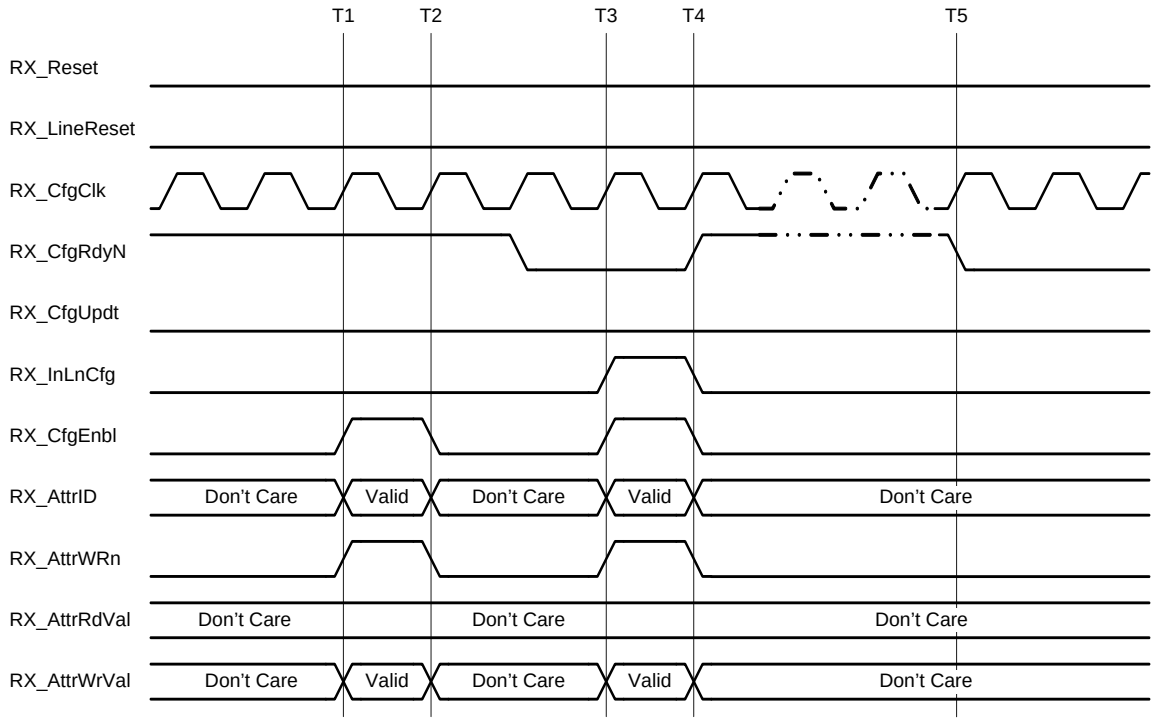


Figure 60 Interface Behavior for Attribute Write Operations

825 At T1, on the rising edge of RX_CfgClk, the Protocol Layer sets RX_CfgEnbl and RX_AttrWRn to "1", and sets the value of RX_AttrID and RX_AttrWrVal. The Protocol Layer holds RX_InLnCfg at "0".

826 At T2, the M-RX samples these signals on the rising edge of RX_CfgClk and performs the requested operation, in this case updating its shadow memory bank. Since the effective configuration bank is not changed, the M-RX performs the requested operation even though RX_CfgRdyN is "1" at this time. The Protocol Layer, on the rising edge of RX_CfgClk at T2, sets RX_CfgEnbl and RX_AttrWRn to "0", and optionally sets to "0" RX_AttrID and RX_AttrWrVal.

827 At T3, another write operation is performed in the same manner as the first, but the Protocol Layer sets RX_InLnCfg to "1" to cause the M-RX to write to the effective configuration bank instead of writing to the shadow memory bank. Consequently, this operation is only performed by the M-RX if RX_CfgRdyN is "0" as illustrated in this use-case.

828 As a result of the operation, the M-RX optionally sets RX_CfgRdyN to "1" at T4, when the write operation is processed. The M-RX optionally holds RX_CfgRdyN at "1" until the change in the configuration is complete. The M-RX then sets RX_CfgRdyN to "0" synchronously with RX_CfgClk at T5. The M-RX is then ready to perform any subsequent write operation.

A.4.3 Effective Configuration Single-step Update and Local Reset

829 Figure 61 shows a single-step (atomic) update of the effective configuration bank followed by a Local Reset.

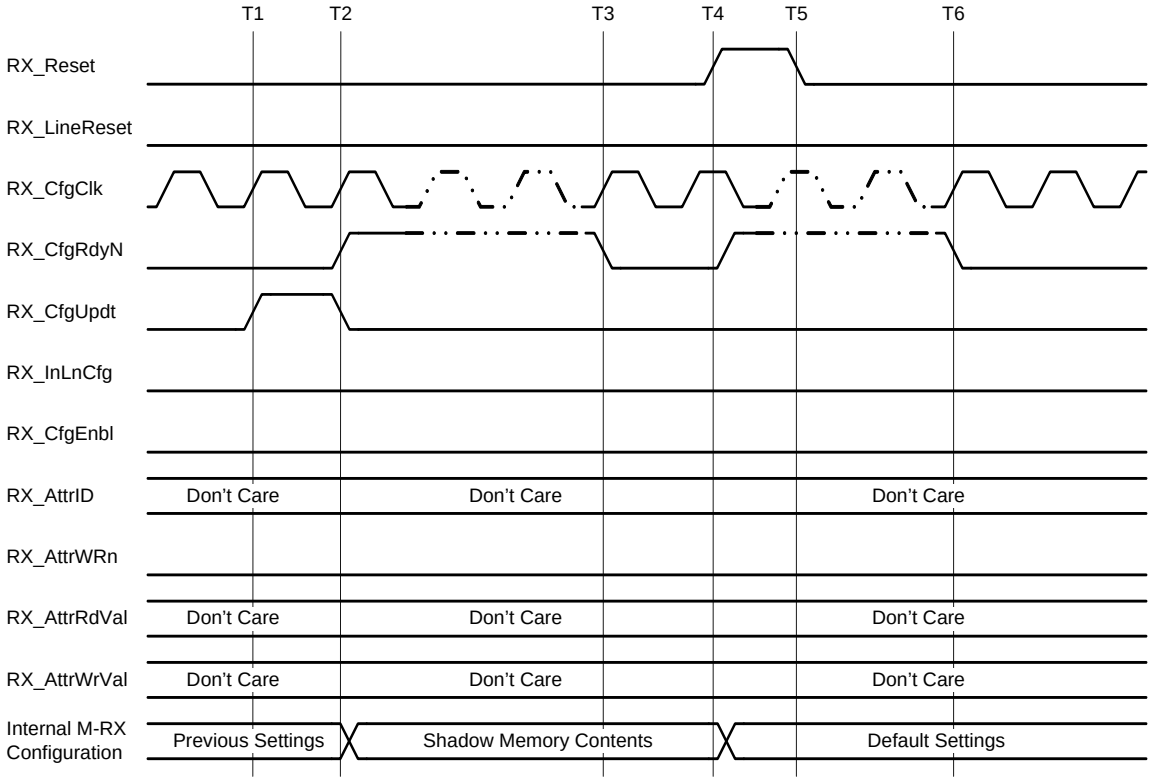


Figure 61 Interface Behavior for RX_CfgUpdt and RX_Reset

830 At T1, the Protocol Layer sets RX_CfgUpdt to "1" for one cycle of RX_CfgClk to upload the entire shadow memory bank into the effective configuration bank in one step. The Protocol Layer holds RX_InLnCfg and RX_CfgEnbl at "0" for this operation. RX_AttrID, RX_AttrWRn, and RX_AttrWrVal are ignored by the M-RX. The M-RX performs this operation only when RX_CfgRdyN is set to "0".

831 The M-RX processes the command on the rising edge of RX_CfgClk at T2, when the entire shadow memory is uploaded into the effective configuration bank. The M-RX then sets RX_CfgRdyN to "1" and holds the value until the change in the M-RX configuration is complete and the M-RX is ready to perform subsequent write operations.

832 At T3, the M-RX sets RX_CfgRdyN to "0"on the rising edge of RX_CfgClk.

833 At T4, the Protocol Layer sets RX_Reset to "1", asynchronous to RX_CfgClk, causing a Local Reset. The M-RX asynchronously sets RX_CfgRdyN to "1" in response, and holds the value until the Protocol Layer sets RX_Reset to "0", which occurs at T5, and it finishes processing the Local Reset. Once the M-RX is ready to perform subsequent write operations, it sets RX_CfgRdyN to "0", which occurs synchronously at T6.

A.4.4 Received LCC and LINE-RESET

834 Figure 62 shows a Type-I M-RX receiving an LCC after an HS-BURST or PWM-BURST followed by a LINE-RESET.

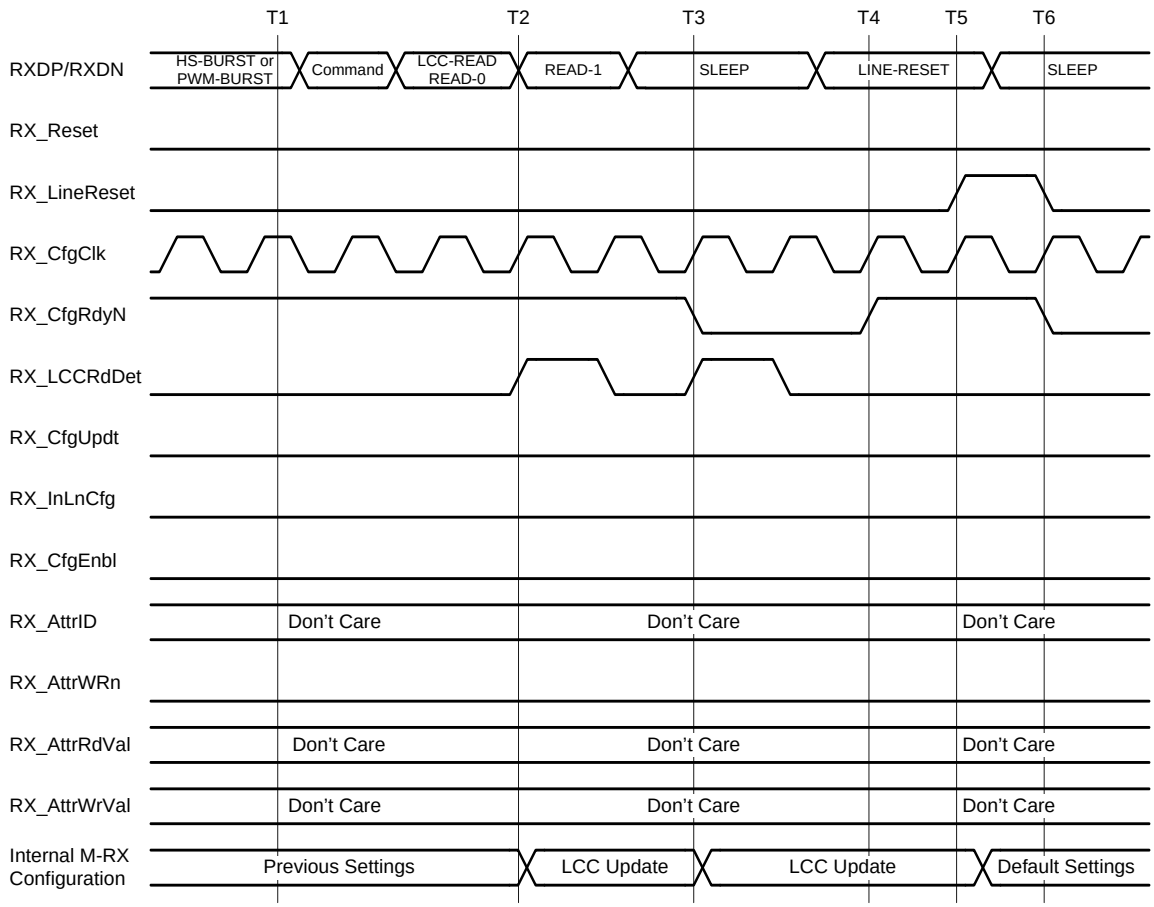


Figure 62 Interface Behavior for LCC Command and LINE-RESET

835 Following an HS-BURST or PWM-BURST, a Type 1 M-RX receives an LCC starting at T1. As shown in the figure, the LCC is asynchronous to RX_CfgClk. Since the LCC follows from HS-BURST or PWM-BURST without passing through STALL, SLEEP or HIBERN8 states, the M-RX holds RX_CfgRdyN at "1".

836 At T2, the M-RX begins processing the LCC, where it sets RX_LCCRdDet to "1" for one cycle of RX_CfgClk to indicate that an LCC-READ command is being processed.

837 At T3, on the rising edge of RX_CfgClk, the M-RX sets RX_LCCRdDet to "1" for one cycle of RX_CfgClk to indicate that a second, cascaded LCC-READ command is being processed. The LINE has already moved to SLEEP state following the second LCC-READ. Therefore, the M-RX also sets RX_CfgRdyN to "0" at T3.

838 At T4, on the rising edge of RX_CfgClk, the M-RX sets RX_CfgRdyN to "1" indicating the LINE is no longer in SLEEP, STALL or HIBERN8 state.

839 At T5, on the rising edge of RX_CfgClk, the M-RX sets RX_LineReset to "1" indicating it has detected the LINE-RESET command. Both RX_CfgRdyN and RX_LineReset are held at "1" for the duration of the LINE-RESET process.

840 At T6, on the rising edge of RX_CfgClk, the M-RX sets RX_CfgRdyN and RX_LineReset to "0" indicating the LINE is in SLEEP state and the LINE-RESET process is complete.

841 Note:

842 *RX_CfgRdyN and RX_LineReset behaviors are independent. In the use-case shown in Figure 62, the M-RX may hold RX_CfgRdyN at "1" at T6 until it is ready to accept subsequent write commands.*

A.4.5 HS Data Reception with 20-bit RX_Symbol Bus

843 Figure 63 shows the interface behavior for an M-RX with a 20-bit interface during HS data reception. 10b8b decoding is enabled in this use-case.

844 In this use-case, the M-RX receives a data transmission from the attached M-TX. An RDS error occurs near the end of the transmission.

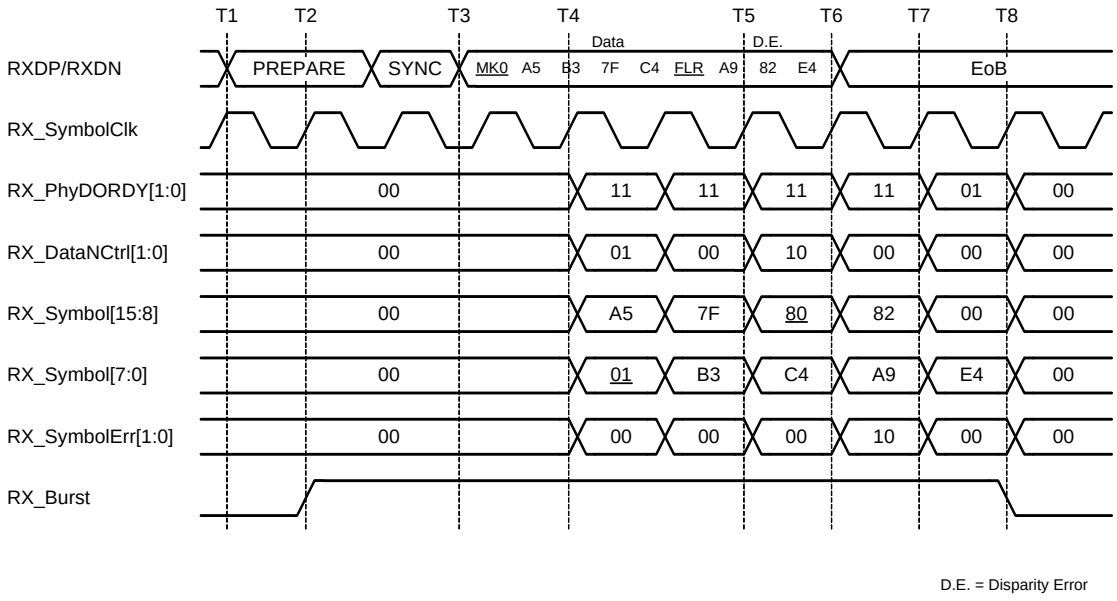


Figure 63 Example 20-bit Interface Behavior for HS Data Reception

845 At T1, the M-RX detects the PREPARE sequence and sets RX_Burst to "1" on the rising edge of RX_SymbolClk at T2.

846 At T3, the SYNC sequence ends. The M-RX receives the first two symbols, a MARKER0 (MK0) and A5 (data).

847 At T4, on the rising edge of RX_SymbolClk, the M-RX sets RX_Symbol[7:0] to "01" (MARKER0) and RX_Symbol[15:8] to "A5". The M-RX also sets RX_DataNCtrl[0] to "0" indicating a control symbol is on RX_Symbol[7:0], and sets RX_DataNCtrl[1] to "1" indicating data is on RX_Symbol[15:8]. RX_SymbolErr[1:0] is held at "00" indicating no errors on RX_Symbol. Finally, the M-RX sets RX_PhyDORDY[1:] to "11" indicating data is available on RX_Symbol. On the next rising edge of RX_SymbolClk, the M-RX sets RX_Symbol[7:0] and RX_Symbol[15:8] to the next two symbols received, "B3" and "7F", respectively. The M-RX sets RX_DataNCtrl[1:0] to "00" indicating both symbols are data. The M-RX sets the remaining signals the same as at T4.

848 At T5, the M-RX sets RX_DataNCtrl[1:0] to "10" indicating it received another control symbol. The M-RX also sets RX_Symbol[7:0] to "C4" (data) and RX_Symbol[15:8] to "80" (FILLER). The M-RX sets the remaining signals the same as at T4.

849 Note:

850 *By itself, the FILLER symbol does not cause the M-RX to set RX_PhyDORDY[1] to "0". However, a mid-stream deassertion of RX_PhyDORDY is possible in plesiochronous Type-I systems due to, e.g. internal FIFO refills in an M-RX implementation.*

851 The M-RX receives the next two symbols, "A9" and "82", in the same manner as the first six symbols. However, as shown in Figure 63, the "82" symbol has an RDS error.

852 At T6, on the rising edge of RX_SymbolClk, the M-RX sets RX_Symbol[7:0] to "A9", RX_Symbol[15:8] to "82", and RX_SymbolErr[1:0] to "10" indicating an error in the data on RX_Symbol[15:8]. The M-RX also sets RX_DataNCtrl[1:0] to "11" indicating both "A9" and "82" are control symbols. Finally, the M-RX sets RX_PhyDORDY[1:0] to "11" indicating data is available on RX_Symbol.

853 At T7, the M-RX detects the end of the BURST and determines it has received an odd number of symbols. It sets RX_Symbol[7:0] to "E4", RX_Symbol[15:8] to "00", and RX_PhyDORDY[1:0] to "01" indicating RX_Symbol[15:8] does not contain data. The M-RX also sets RX_DataNCtrl[1:0] to "00" indicating RX_Symbol does not contain any control symbols. Finally, the M-RX sets RX_SymbolErr[1:0] to "00" indicating there are no errors.

854 At T8, on the rising edge of RX_SymbolClk, the M-RX sets RX_Burst to "0" indicating the end of the Burst.

A.4.6 TX_LineReset Behavior

855 Figure 64 shows a LINE-RESET use-case. In this use-case, the Protocol Layer sends a LINE-RESET to initialize the M-TX and M-RX attached to the LINE.

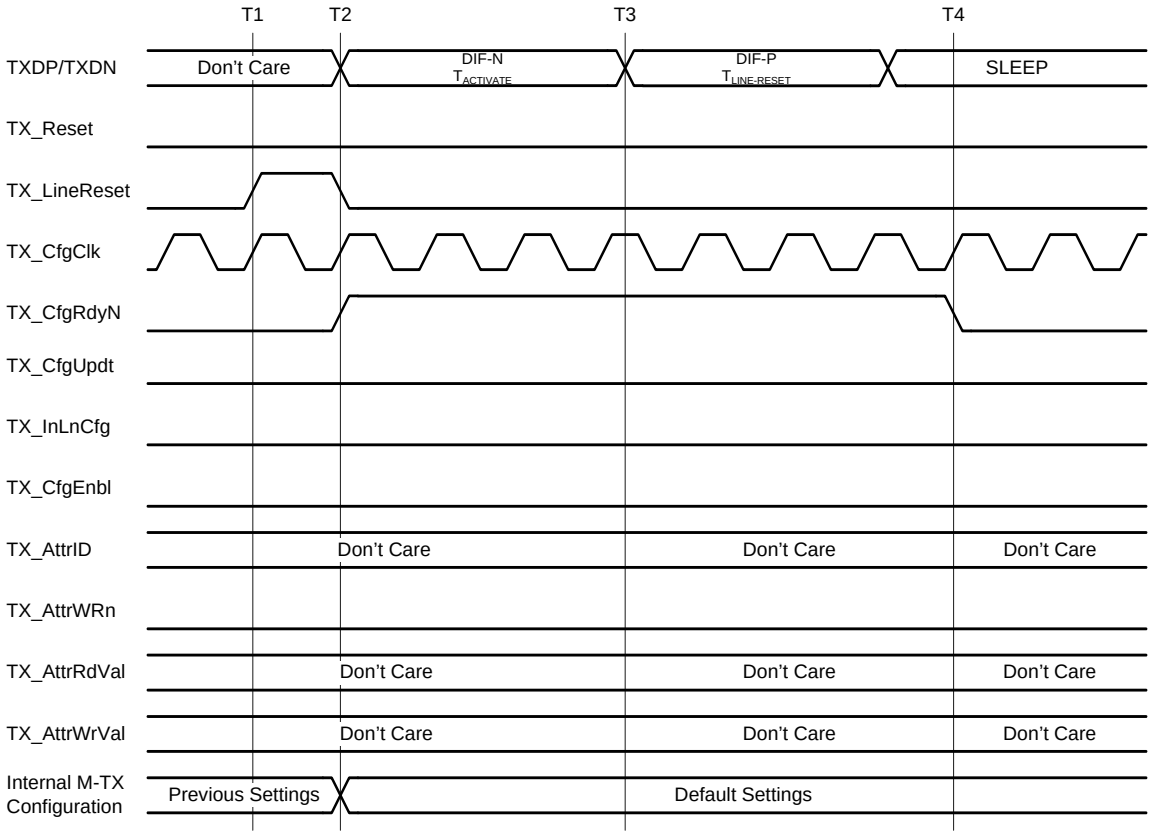


Figure 64 Interface Behavior for a TX_LineReset Command

856 At T1, the Protocol Layer sets TX_LineReset to “1” on the rising edge of TX_CfgClk, and optionally sets it to “0” one TX_CfgClk cycle later at T2.

857 At T2, the M-TX sets TX_CfgRdyN to “1”, updates its internal configuration registers to their default values, and starts issuing the LINE-RESET sequence over the LINE.

858 The M-TX holds TX_CfgRdyN at “1” while it is processing the LINE-RESET.

859 At T4, on the rising edge of TX_CfgClk, the M-TX sets TX_CfgRdyN to “0” to signal its internal FSM exit to SLEEP state. At this time, the M-TX is ready for any subsequent write command or TX_LineReset pulse.

860 Note:

861 *The M-TX only monitors the 0-to-1 transition on TX_LineReset to interpret the command. Consequently, the M-TX does not detect whether the Protocol Layer leaves TX_LineReset at “1” or sets it to “0” at T2.*

A.4.7 HS Transmission on 20-bit TX_Symbol Bus with Data Throttled by Protocol Layer

862 Figure 65 shows an HS transmission with the Protocol Layer controlling the data throughput. 8b10b encoding is enabled in this use-case.

863 In this use-case, the Protocol Layer cannot supply transmission requests as fast as the M-TX transmissions on the LINE. The Protocol Layer throttles the data throughput by changing the value on TX_ProtDORDY. The M-TX continues to transmit, but inserts FILLER symbols whenever the Protocol Layer does not have new data to send.

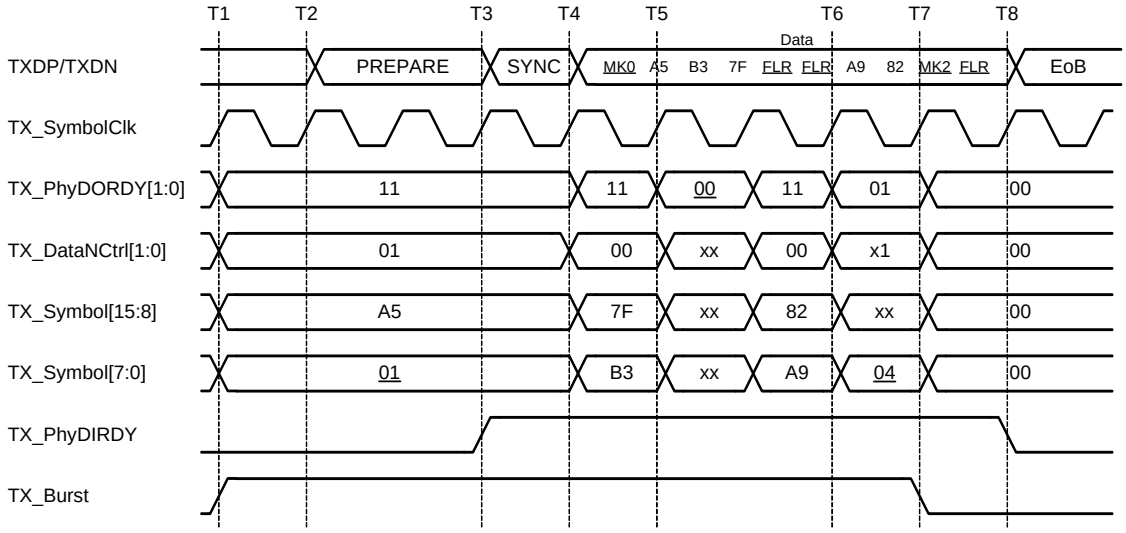


Figure 65 Interface Behavior for HS Transmission with Protocol Layer Throttling Data

864 At T1, on the rising edge of TX_SymbolClk, the Protocol Layer sets TX_ProtDORDY[1:0] to “11”, indicating both TX_Symbol[7:0] and TX_Symbol[15:8] contain data; TX_DataNCtrl[1:0] to “01”, indicating the value on TX_Symbol[7:0] (01) is a control symbol (MARKER0), and the value on TX_Symbol[15:8] (A5) is a data symbol. Finally, the Protocol Layer initiates the HS transmission by setting TX_Burst to “1”.

865 At T2, on the rising edge of TX_SymbolClk, the M-TX reads the Protocol Layer request and issues PREPARE and SYNC sequences.

866 At T3, on the rising edge of TX_SymbolClk, the M-TX sets TX_PhyDIRDY to “1”, far enough in advance of the start of data transmission for the Protocol Layer to read TX_PhyDIRDY at T4.

867 At T4, on the rising edge of TX_SymbolClk, the Protocol Layer holds TX_ProtDORDY[1:0] at “11”, indicating new data is available, and sets TX_DataNCtrl[1:0] to “00”, indicating the values on TX_Symbol[7:0] (B3) and TX_Symbol[15:8] (7F) are data symbols.

868 At T5, on the rising edge of TX_SymbolClk, the Protocol Layer sets TX_ProtDORDY to “00” indicating it does not have new data to send. The M-TX ignores the values on TX_DataNCtrl[1:0] and TX_Symbol[15:0], and inserts two FILLER symbols on the LINE.

869 At T6, on the rising edge of TX_SymbolClk, the Protocol Layer sets TX_ProtDORDY[1:0] to “01”, indicating only TX_Symbol[7:0] has available data, and sets TX_DataNCtrl[1:0] to “01”, indicating the value on TX_Symbol[7:0] (04) is a control symbol (MARKER2).

870 At T7, on the rising edge of TX_SymbolClk, the Protocol Layer sets TX_Burst to “0” indicating the end of the HS-BURST. Meanwhile, the M-TX inserts a FILLER symbol after the MARKER2 symbol since the Protocol Layer submitted an odd number of symbols to transmit.

871 At T8, on the rising edge of TX_SymbolClk, the M-TX reads the TX_Burst signal as “0” and begins transmitting the End-of-Burst sequence on the LINE. The M-TX sets TX_PhyDIRDY to “0”, indicating it is no longer prepared to accept new data to transmit.

A.4.8 HS Transmission on 20-bit TX_Symbol Bus with Data Throttled by M-TX

872 Figure 66 shows an HS transmission with the M-TX controlling the data throughput. 8b10b encoding is enabled in this use-case.

873 In this use-case, the M-TX transmissions on the LINE lag the Protocol Layer requests so the M-TX needs to slow down the transfer from the Protocol Layer. The M-TX throttles the data throughput by changing the value on TX_PhyDIRDY.

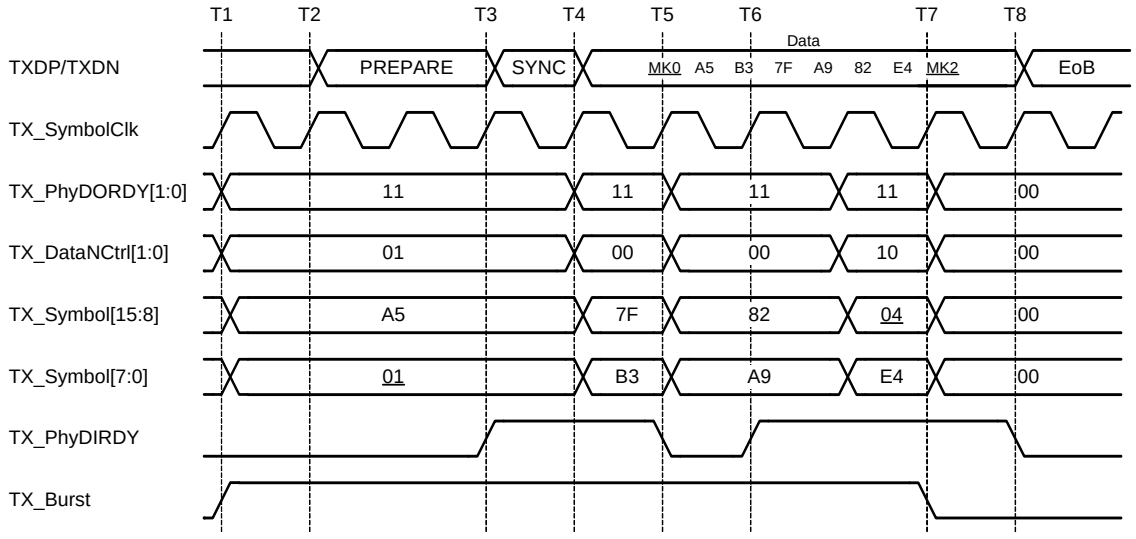


Figure 66 Interface Behavior for HS Transmission with M-TX Throttling Data

874 At T1, on the rising edge of TX_SymbolClk, the Protocol Layer sets TX_ProtDORDY[1:0] to “11”, indicating both TX_Symbol[7:0] and TX_Symbol[15:8] contain data; TX_DataNCtrl[1:0] to “01”,

indicating the value on TX_Symbol[7:0] (01) is a control symbol (MARKER0), and the value on TX_Symbol[15:8] (A5) is a data symbol. Finally, the Protocol Layer initiates the HS transmission by setting TX_Burst to “1”.

875 At T2, on the rising edge of TX_SymbolClk, the M-TX reads the Protocol Layer request and issues PREPARE and SYNC sequences.

876 At T3, on the rising edge of TX_SymbolClk, the M-TX sets TX_PhyDIRDY to “1”, far enough in advance of the start of data transmission for the Protocol Layer to read TX_PhyDIRDY.

877 At T4, on the rising edge of TX_SymbolClk, the Protocol Layer sets TX_ProtDORDY[1:0] to “11”, indicating new data is available, and sets TX_DataNCtrl[1:0] to “00”, indicating the values on TX_Symbol[7:0] (B3) and TX_Symbol[15:8] (7F) are data symbols.

878 At T5, on the rising edge of TX_SymbolClk, the M-TX sets TX_PhyDIRDY to “0”, indicating the M-TX is busy. The Protocol Layer holds TX_ProtDORDY at “11” indicating it has new data to send.

879 At T6, on the rising edge of TX_SymbolClk, the M-TX sets TX_PhyDIRDY to “1” indicating it is again available to accept new data. However, the Protocol Layer reads TX_PhyDIRDY as “0”, and consequently holds the values on TX_ProtDORDY[1:0], TX_DataNCtrl[1:0], and TX_Symbol[15:0].

880 On the next rising edge of TX_SymbolClk the Protocol Layer sets TX_ProtDORDY[1:0] to “11”, and sets TX_DataNCtrl[1:0] to “10”, indicating the value on TX_Symbol[7:0] (E4) is a data symbol and the value on TX_Symbol[15:8] (04) is a control symbol (MARKER2).

881 At T7, on the rising edge of TX_SymbolClk, the Protocol Layer sets TX_Burst to “0” indicating the end of the HS-BURST.

882 At T8, the M-TX reads the TX_Burst signal as “0” on the rising edge of TX_SymbolClk, and begins transmitting the End-of-Burst sequence on the LINE. The M-TX sets TX_PhyDIRDY to “0”, indicating it is no longer prepared to accept new data to transmit.

Annex B Recommended Test Functionality (informative)

883 The purpose of this annex is to provide guidelines for testability features for M-PHY applications. Because explicit test modes are not defined within the Physical Layer, most test functionality is left to higher layers to implement. However, this must be done in a manner that produces the necessary behavior at the Physical Layer interface that is needed for performing physical layer measurements with standard laboratory equipment.

884 This annex describes the functional behavior that should be provided at the Physical Layer interface in order for various classes of measurements to be performed. The behavior is described in an abstract manner, without reference to specific protocols or applications. Because multiple applications of M-PHY technology exist, options for different architectures are discussed. Applications that use M-PHY technology should ensure that sufficient functionality is designed into the higher layer specifications to allow the necessary test functionality to be supported at the Physical Layer interface. Note that this functionality may be supported within the normal operating capabilities of the protocol, or may be implemented via specialized test modes if necessary.

885 This annex is divided into two main sections, test pattern generation and test pattern verification. Test pattern generation is primarily applicable to transmitter measurements, and test pattern verification is applicable to receiver tolerance measurements. A brief section on interoperability testing is also discussed.

B.1 Test Pattern Generation

B.1.1 General Transmitter Test Approach

886 In order to perform transmitter signaling measurements such as amplitude (swing), rise/fall times, skew, jitter, etc, it is necessary for the M-PHY Device Under Test (DUT) to transmit known test patterns into a reference termination load. The signals observed at this reference load are captured using an oscilloscope, and measured for conformance.

887 The reference termination may consist of an external fixture that contains a precision reference termination structure, which is then probed using high-bandwidth active probes. Or in some cases the oscilloscope itself may be used as the reference termination (in cases where a 100 Ω differential termination is required), in which case the signal is sent directly into the instrument, using coaxial cables.

888 In the case of M-PHY technology, where signals must also be measured into an open (unterminated) termination, active probing must be used, as it is the only way to observe signals under these conditions. Active probing is also preferable for terminated measurements, as it allows the signal to be observed as close to the TX PINs as possible, and with minimal capacitive loading.

889 An example transmitter test setup is shown in Figure 67, where the DUT is mounted on an SMA-based Test Vehicle Board (TVB), and is connected to a Reference Termination Board (RTB). Each signaling Lane is probed using two active differential probes.

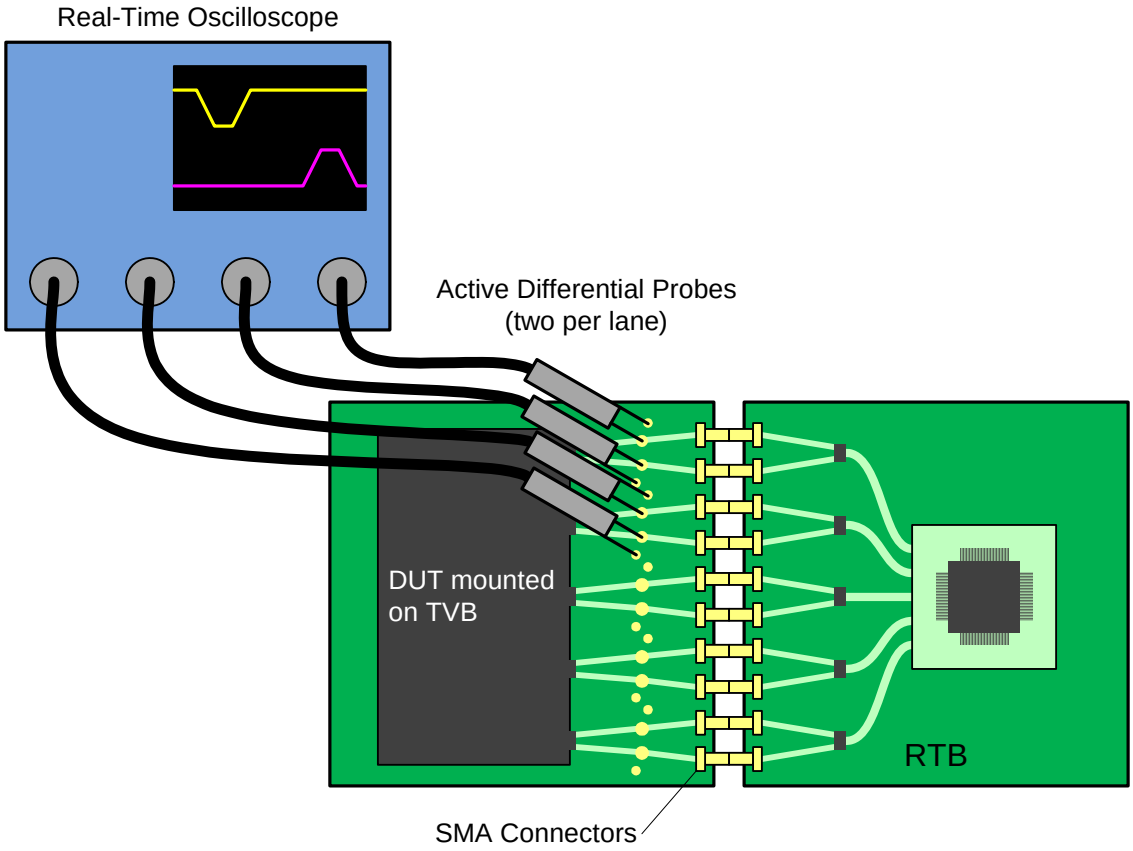


Figure 67 Transmitter Test Setup

B.1.2 Test Patterns

890 Some transmitter measurements, e.g., rise/fall time are typically performed on short repeating patterns consisting of a single repeated 10-bit code word, e.g., D30.7, D10.2, etc. Other measurement such as transmitter jitter are required to be performed on longer repeating patterns such as CJTPAT and CRPAT. (For formal definitions of these patterns, see [INC01].)

891 As a result, it is desirable for M-PHY devices to support a mode that allows a user-specified test pattern to be defined (which can be up to 2320 bits in length for CJTPAT, and 1960 bits for CRPAT.) For maximum flexibility, this mode should allow arbitrary sequences of validly encoded 8b10b 10-bit codewords to be defined, up to several thousand bits in length.

B.1.3 Signaling Type and Speed

892 Two types of signaling are used for an M-PHY implementation, NRZ and PWM. A Type-I MODULE uses NRZ signaling for HS transmission and uses PWM signaling for LS transmission. A Type-II MODULE can use NRZ signaling for LS and HS transmission, while PWM signaling can be used only for LS transmission. In addition, different speed ranges (GEARs) are defined for both HS and LS transmission.

893 DUTs should provide a mechanism that allows both the signaling type and GEAR to be controlled for test purposes.

B.1.4 Continuous vs. Burst Modes

894 Under normal operation, data transmission occurs in bursts, with power-saving states occurring between bursts.

895 Most transmitter measurements can be performed on burst-mode signaling using a real-time oscilloscope. These instruments can capture individual burst waveforms, which can then be post-processed to extract the required measurements.

896 Note that a second class of oscilloscope exists, known as a sampling oscilloscope, which requires a continuous, repeating pattern in order to observe and measure a signal. These instruments sample multiple instances of the same repeating waveform at different time offsets in order to build a picture of the transmitted signal. These types of instruments are typically capable of higher bandwidths and greater vertical precision than real-time oscilloscopes, however they require a continuous, repeating pattern, and cannot measure burst-mode signaling.

897 In order to support the widest range of test instruments and greatest measurement flexibility, M-PHY devices should support both burst-based and continuous transmission modes for test pattern generation.

B.1.5 Disconnect

898 Mechanisms may exist within the protocol to allow configuration of desired test modes and capabilities through the Physical Layer interface. However in these instances, capability must be provided that allows the DUT to remain in the configured test mode once the test mode has been entered, such that it may be disconnected from a protocol-aware LINK partner (that may have been used to perform all or part of the configuration), and reconnected to the test setup. This implies that the DUT maintains the configured transmitter test mode even when no signaling is present at the DUT's receiver. This functionality is often informally referred to as 'disconnect' in the test community, in that if a DUT supports “disconnect”, it will maintain its test modes after being disconnected from a LINK partner.

899 M-PHY devices should support disconnect for all test modes.

B.1.6 Configuration

900 One method for implementing such a feature would be to define a special protocol mechanism, which would allow a special frame/command containing the desired pattern to be sent to the DUT via the Physical Layer interface. Upon reception of this packet, the DUT would transmit the provided pattern continuously, using the desired signaling type, gear, and any other desired settings (which could also be specified along with the pattern.) The test pattern could be transmitted continuously until a separate reset packet is received, or the DUT is power cycled.

B.2 Test Pattern Verification

B.2.1 General Receiver Test Approach

901 The general approach used for verifying receiver conformance involves using a laboratory-grade signal generator to generate signaling that contains controlled amounts of degradation, of various types, per the specification requirements. The signal generator is calibrated by measuring the specified characteristics into a reference termination (which is the same reference termination used for the transmitter conformance measurements). Once the required amount of degradation is calibrated, the signal is removed from the reference termination and applied to the DUT's receiver.

902 At this point, some observable mechanism must be used to determine whether or not the DUT can successfully decode the received signaling without error. There are several ways that this can be achieved.

B.2.2 Loopback Mode

903 Loopback mode is one of the most common mechanisms used for receiver testing. In this mode, data that is received at the RX is retransmitted out the TX. The TX signal can then be observed to verify whether or not any bits were received in error (as the error would be propagated to the TX). Note however that different types of loopback modes exist, and the subtleties of these differences can impact their ability to be used with different types of test instruments. The important differences are discussed below:

904 **Synchronous vs. Plesiochronous**

905 One of the most important characteristics of a loopback mode pertains to how the clocking architecture is defined with respect to the receiver and transmitter. For a synchronous loopback, the recovered clock from the RX is used to retransmit the signal on the TX. This means there is a bit-for-bit relationship between receiver and transmitter, and the exact bit sequence that was sent into the receiver will appear at the transmitter.

906 Typically, this type of loopback mode is implemented outside the scope of normal operation, where the standard protocol operation is no longer applicable, and the DUT will simply forward any data received to the transmitter. The received data is typically not 8b10b decoded and re-encoded in the loopback path, which ensures that a single error at the receiver translates to a single error at the transmitter. This behavior allows traditional Bit Error Rate Tester (BERT) instruments to be used to test the receiver (as these instruments typically require a bit-for-bit correlation between the transmitted and received data patterns.)

907 This document actually specifies this exact type of loopback. The LOOPBACK feature defined in Section 4.10.1 is intended for symmetric architectures that support the same MODE and GEAR settings for the M-RX and M-TX. If this feature is supported, it can actually be used for both receiver and transmitter verification, as most transmitter measurements can be performed on the TX output while the desired test pattern is transmitted into the RX. Note however that this case is not ideal for all transmitter tests, particularly jitter, as measured jitter and frequency while in LOOPBACK are not necessarily the same as during normal operation, as the clock reference is not the same.

908 Other types of loopback include a plesiochronous loopback (sometimes referred to as a “far-end retimed loopback”), which is similar to the synchronous loopback, except the transmitter and receiver run on separate clock domains, i.e., have separate clock references. This means that the RX and TX are operating at almost the same rate, but are not exactly matched. This is still considered a test mode that operates outside the scope of normal protocol operation, where data must be inserted or deleted from the data being looped back in order to account for the rate difference between RX and TX. This is typically accomplished by inserting or deleting specifically defined control codewords that are not considered part of the CRC-checked frame data stream.

909 In this scenario, a BERT or other signal source may be used to generate the test signal that is sent into the receiver, however the signal that is retransmitted by the DUT must be checked using a Frame Error Counter, which is a device that can receive the framed data patterns, and compute/check the CRC (which is included as part of the defined pattern.)

B.2.3 Receiver Pattern Checking

910 Note that the loopback described above can only be used for symmetric architectures, and requires the same MODEs and GEARs to be supported by both the M-RX and M-TX. For M-PHY applications and architectures that are not bidirectional and symmetric, a different approach must be used to verify received data for the purposes of conformance testing.

911 One option consists of a dedicated RX test mode, whereby a predefined test pattern can be transmitted into the M-RX, and the checking operation is actually performed by the receiver itself. This can be done on a bit-for-bit level (if the expected pattern is known by the receiver). However, an easier approach is to use the CRC functionality that already exists in most devices.

912 Such a dedicated RX test mode must be simple enough that a majority of the protocol is bypassed. The DUT must be placed into a mode where simple, framed patterns containing valid CRC's can be sent into the receiver, using a non-protocol-aware signal generator. Note that most current lab signal sources contain some degree of sequencing capability that can be used to send startup/configuration information prior to a repeating test sequence. The only limitation to these instruments however is that they cannot be “interactive” in that they cannot detect and react to transmissions coming from the DUT, if timing-sensitive handshaking is required as part of the protocol. In some cases where the timings are known and repeatable, it may be possible to create sequences that can mimic an interactive protocol exchange, however these typically must be created on a per-DUT basis, and require knowledge of the exact timings required.

913 If a mode exists where a receiver is able to verify CRC-checked frame data, a mechanism must be provided that allows for observation of the results of the checking operation. While this may be achieved though internal vendor-specific registers and counters, it is also possible (and preferable) to allow this to be performed through the Physical Layer interface.

914 Several options exist to enable this, which are all based on acknowledgement mechanisms, provided the DUT contains a low-speed TX, which may be used to communicate information about the received data.

915 If sufficient bandwidth exists, the DUT could transmit some form of defined positive acknowledgement for each successfully received frame, and a negative acknowledgement for each frame received in error. If sufficient bandwidth does not exist, the positive acknowledgements can be omitted, and only the negative acknowledgements sent in the error cases (which are assumed to be few). The acknowledgements may be as simple as a single codeword or short pattern, or any other sequence that can be detected and counted using non-protocol-specific laboratory instruments (or possibly a simple FPGA).

916 In the extreme case, the DUT technically only needs to indicate if any errors were observed over a given period in order for a test to be designed that can verify conformance. If a known amount of data is transmitted to the DUT over a given interval, and the DUT indicates provides a single acknowledgement that no errors were observed, this is a sufficient observable to determine conformance. While knowing an exact error count may certainly be useful for debugging and troubleshooting purposes, such level of detail is not necessary for determining conformance.

917 Applications that do not or cannot implement LOOPBACK should implement some form of dedicated pattern-checking mode, which is capable of verifying a CRC-checked, framed pattern, and which can provide some form of acknowledgement-based observation mechanism.

B.2.4 Receiver Configuration – Termination

918 Note that for the dedicated RX pattern checking test mode (and also potentially loopback modes as well), some level of configuration of the receiver must occur. This includes the MODE and GEAR operation of the receiver, as well as the termination mode (terminated or unterminated).

919 Configuration of the termination mode is another important mechanism. The receiver HS termination is either disabled during normal operation, or enabled such that it is only active during the reception of an HS burst. However, another mode is needed for test purposes, in which the termination can be manually forced into an enabled state.

920 This mode is necessary in order to perform S-parameter measurements of the receiver termination. Because the measurement cannot be made during reception of an HS burst, the receiver must be placed into a mode where the termination is permanently enabled for the duration of the measurement.

921 Applications should provide a mechanism that allows manual enabling and disabling of the receiver HS termination.

B.3 Interoperability Testing

922 Note that the mentioned transmitter and receiver test mechanisms all have been discussed in the context of conformance testing. However, it is important to note that the same mechanisms, e.g., dedicated pattern generation and checking modes, loopback, etc., can also be used to perform physical layer interoperability verification as well.

923 This is performed in the same manner as conformance testing, however instead of using a lab signal generator to generate the test signals, another M-PHY device is used, which is placed into pattern generation mode. This allows vendor-to-vendor physical layer interoperability testing to be performed using the same methodologies that are used for conformance testing. (Note that this only verifies interoperability of the physical layer, however isolation and verification of just the physical layer functionality is an important component of any interoperability test strategy.)

Annex C SI Dithering (informative)

924 When constructing systems using the high speed interface to connect a baseband IC (BBIC) with a radio frequency IC (RFIC) noise coupling between the high speed interface and sensitive LNA inputs of the RFIC is a concern. Interface bit rates are at frequencies that may cause EMI near some of the air interface frequencies. The least destructive EMI would occur if the interface data appeared as a random UI rate bit stream with no repeating sub-UI rate patterns. However, the encoding of the interface data into 8b10b symbols causes repetitive 10 UI patterns in an HS-BURST. Analysis has shown that these repeating SI rate patterns can cause spectral peaking in the EMI that exacerbates the noise coupling problem.

925 SI rate symbol timing can not be changed during a BURST. Symbol boundaries are established at the start of each BURST and must remain on the same 10 UI boundary for the remainder of the BURST. However, 10 UI symbol boundaries may be changed from HS-BURST to HS-BURST. Analysis shows that dithering of the SI starting locations, BURST to BURST, by some fraction of an SI, spreads SI rate EMI enough to offer some EMI benefit.

C.1 Dither Method

926 Delaying the start of each HS-BURST with reference to the last BURST, some random number of UI, accomplishes the desired dithering. This happens naturally in many implementations, but forced dithering ensures a good distribution of starting locations in any system.

927 Within the physical interface there is a UI rate divide by ten counter to produce the SI rate symbol boundaries. If this counter is left running during STALL states, then all HS-BURSTs have the same SI boundaries. That is, the SI clock will be coherent from BURST to BURST, producing maximum EMI. In order to accomplish dithering, this counter should be stopped and restarted from BURST to BURST. Stopping the counter during STALL may be a good practice for power efficiency as well. However, even when the counter is restarted for each HS-BURST, it is possible that the “frames to send”, or “start” signal to the physical interface is generated in a way that produces a poor distribution of symbol boundaries from BURST to BURST, the worst case being the same symbol boundary every BURST. To guarantee a good distribution of BURST to BURST SI starting locations, the “start” signal may be delayed a random number of UI intervals before starting the divide by ten counter to establish the new symbol boundary.

928 In order to adequately randomize the dither delay value, some type of pseudo-random value is needed from BURST to BURST. For example, an 8-bit PRBS might be used to provide the random dither locations. This can be done by ensuring that the PRBS is clocked at least once per HS-BURST. The recommended method is to clock it once at the EOT symbol of each BURST.

929 Figure 68 is an example of a circuit that accomplishes this BURST to BURST starting location dither.

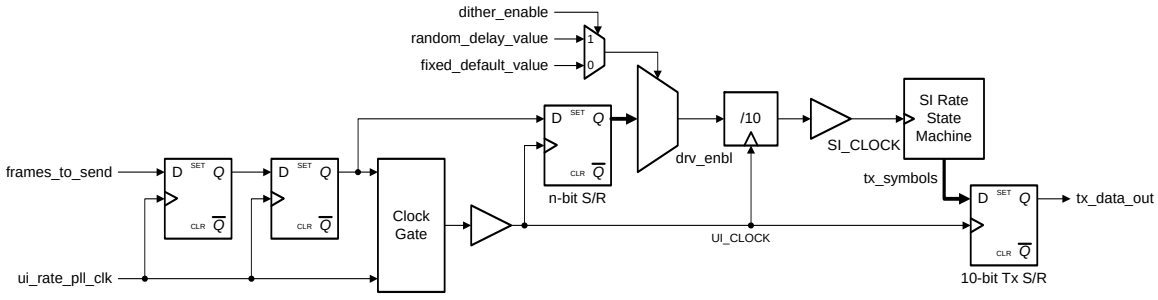


Figure 68 Dithering Circuit Example

C.1.1 Dither Magnitude

930 Since the SI rate patterns repeat every 10 UI, the maximum useful dithering spreads starting locations over a 10 UI range. The minimum dither possible is two locations. Spreading the starting locations over just two locations showed significant benefit in simulations. Table 60 shows all of the possible useful dithering ranges. Because of the reduced complexity required to produce a flat dithering distribution when using a power-of-2 (2^X) number of starting locations, dithering control is limited to four settings; one location (no dithering), two, four and eight locations. In this case, one, two or three bits of the eight bit PRBS generator can be used directly, with no division of the random number by the dither amount necessary.

Table 60 Dithering Ranges

Number of Random Start Positions	Starting UI Delay Range	Range from Default Delay	Divide Required?
1 (no dither)	4 (default)	[0]	No
2	4-5	[0] [+1]	No
3	3-4-5	[-1] [0] [+1]	Yes
4	3-4-5-6	[-1] [0] [+1] [+2]	No
5	2-3-4-5-6	[-2] [-1] [0] [+1] [+2]	Yes
6	2-3-4-5-6-7	[-2] [-1] [0] [+1] [+2] [+3]	Yes
7	1-2-3-4-5-6-7	[-3] [-2] [-1] [0] [+1] [+2] [+3]	Yes
8	1-2-3-4-5-6-7-8	[-3] [-2] [-1] [0] [+1] [+2] [+3] [+4]	No
9	0-1-2-3-4-5-6-7-8	[-4] [-3] [-2] [-1] [0] [+1] [+2] [+3] [+4]	Yes
10	0-1-2-3-4-5-6-7-8-9	[-4] [-3] [-2] [-1] [0] [+1] [+2] [+3] [+4] [+5]	Yes

931 In case a HS-BURST is started to issue a real time critical message over the interface, then the random delay inserted between the “start” signal to the physical interface and the actual start of the BURST adds uncertainty to the delivery time of the message. In order to produce the least uncertainty for this message, a default start delay of half of the maximum dither range should be used when dither is disabled. The range of dither delays is then spread equally around this default delay to produce an uncertainty of approximately plus or minus one half of the maximum dither range.