Specification for

C-PHY SM

Version 1.0 – 05 August 2014

MIPI Board Adopted 07 October 2014

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Further technical changes to this document are expected as work continues in the C-PHY Subgroup of the PHY Working Group.

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Release History

Date	Version	Description
2014-Oct-07	V1.0	Initial Board Approved Release.

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1 Introduction

This document describes a high-speed serial interface called C-PHY, which provides high throughput performance over bandwidth limited channels for connecting to peripherals, including displays and cameras. (This includes display Chip-on-Glass receiver channels and image sensor transmitters that exhibit bandwidth limitations.)

The C-PHY is based on 3-Phase symbol encoding technology delivering 2.28 bits per symbol over three-wire trios, and is targeting 2.5Gsymbols/s. C-PHY has many characteristics in-common with D-PHY [MIPI01]; many parts of C-PHY were adapted from D-PHY. C-PHY was designed to be able to coexist on the same IC pins as D-PHY so that dual-mode devices can be developed.

1.1 Scope

The scope of this document is to describe the lowest layers of the high-speed interfaces to be applied by MIPI Alliance application or protocol level specifications. This includes the physical interface, electrical interface, low-level timing and the PHY-level protocol. The goal has been to define a C-PHY high-speed interface that can coexist on the same pins as the MIPI D-PHY interface. These functional areas taken together are known as C-PHY.

The C-PHY specification shall always be used in combination with a higher layer MIPI specification that references this specification. Any other use of the C-PHY specification is strictly prohibited, unless approved in advance by the MIPI Board of Directors.

The following topics are outside the scope of this document:

- **Explicit specification of signals of the clock generator unit.** The C-PHY specification does implicitly require a minimum performance of the internal clock signals in order to meet the defined specifications of the external signals. Intentionally, only the behavior on the interface pins is constrained. Therefore, the clock generation unit is excluded from this specification, and will be a separate functional unit that provides the required clock signals to the C-PHY in order to meet the specification. This allows many implementation trade-offs as long as these do not violate this specification.
- **Procedure to resolve contention situations.** The C-PHY contains several mechanisms to detect Link contention. However, certain contention situations can only be detected at higher levels and are therefore not included in this specification.
- **Ensure proper operation of a connection between different Lane Module types.** There are several different Lane Module types to optimally support the different functional requirements of several applications. This means that next to some base-functionality there are optional features which can be included or excluded. This specification only ensures correct operation for a connection between matched Lane Modules types, which means: Modules that support the same features and have complementary functionality. In case the two sides of the Lane are not the same type, and these are supposed to work correctly, it shall be ensured by the manufacturer(s) of the Lane Module(s) that the provided additional functionality does not corrupt operation. This can be most easily accomplished if the additional functionality can be disabled by other means independent of the MIPI C-PHY interface, such that the Lane Modules behave as if they were the same type.
- **ESD protection level of the IO.** The required level of ESD protection will depend on a particular application environment and product type.
- **Exact symbol error rate value.** The actual value of the achieved symbol error rate depends on the total system integration and the hostility of the environment. Therefore, it is impossible to specify a symbol error rate for individual parts of the Link. This specification allows for implementations with a symbol error rate less than 10^{-12}.

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- **Specification of the PHY-Protocol Interface.** The C-PHY specification includes a PHY-Protocol Interface (PPI) annex that provides one possible solution for this interface. This annex is limited to the essential signals for normal operation in order to clarify the kind of signals needed at this interface. For power reasons this interface will be internal for most applications. Practical implementations may be different without being inconsistent with the C-PHY specification.
- **Implementations.** This specification is intended to restrict the implementation as little as possible. Various sections of this specification use block diagrams or example circuits to illustrate the concept and are not in any way claimed to be the preferred or required implementation. Only the behavior on the C-PHY interface pins is normative. Regulatory compliance methods are not within the scope of this document. It is the responsibility of product manufacturers to ensure that their designs comply with all applicable regulatory requirements.

Items that are outside of the scope of this document are generally the same as those described in the D-PHY specification, except for a detailed description of built-in test circuitry and test patterns. The built-in test circuit description is included as an informative chapter to be followed at the option of the system or device implementer. This document deviates from the norm and defines the behaviors of the test circuitry because the general functionality of C-PHY is different from most other PHY implementations. It is useful to provide a common test circuit description that can be followed by device implementers and test equipment providers so there will be compatibility between devices implementing C-PHY and test equipment.

Coexistence with D-PHY on the same IC pins is possible, and likely in many applications; the means of doing so is beyond the scope of this standard.

Regulatory compliance methods are not within the scope of this document. It is the responsibility of product manufacturers to ensure that their designs comply with all applicable regulatory requirements.

1.2 Purpose

The C-PHY specification is used by manufacturers to design products that adhere to MIPI Alliance interface specifications for mobile devices such as, but not limited to, camera, display and unified protocol interfaces.

Implementing this specification reduces the time-to-market and design cost of mobile devices by standardizing the interface between products from different manufacturers. In addition, richer feature sets requiring high data rates can be realized by implementing this specification. Finally, adding new features to mobile devices is simplified due to the extensible nature of the MIPI Alliance Specifications.

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2 Terminology

2.1 Use of Special Terms

The MIPI Alliance has adopted Section 13.1 of the *IEEE Standards Style Manual*, which dictates use of the words “shall”, “should”, “may”, and “can” in the development of documentation, as follows:

> The word *shall* is used to indicate mandatory requirements strictly to be followed in order to conform to the Specification and from which no deviation is permitted (*shall* equals *is required to*).
>
> The use of the word *must* is deprecated and shall not be used when stating mandatory requirements; *must* is used only to describe unavoidable situations.
>
> The use of the word *will* is deprecated and shall not be used when stating mandatory requirements; *will* is only used in statements of fact.
>
> The word *should* is used to indicate that among several possibilities one is recommended as particularly suitable, without mentioning or excluding others; or that a certain course of action is preferred but not necessarily required; or that (in the negative form) a certain course of action is deprecated but not prohibited (*should* equals *is recommended that*).
>
> The word *may* is used to indicate a course of action permissible within the limits of the Specification (*may* equals *is permitted to*).
>
> The word *can* is used for statements of possibility and capability, whether material, physical, or causal (*can* equals *is able to*).

All sections are normative, unless they are explicitly indicated to be informative.

2.2 Definitions

Bi-directional: A single Lane that supports communication in both the forward and reverse directions.

C-PHY: The PHY defined in this document. C-PHYs may be used in channel-limited applications, hence the use of the character “C.”

Escape Mode: An optional mode of operation for lanes that allows low bit-rate commands and data to be transferred at very low power.

Forward Direction: The signal direction is defined relative to the direction of the high-speed data. The main direction of data communication, from source to sink, is denoted as the forward direction.

Lane: Consists of two complementary lane modules communicating via three-line, point-to-point lane Interconnects. The term “lane” is often used to denote interconnect only.

Lane Interconnect: Three-line, point-to-point interconnect used for both differential high-speed signaling and low-power, single-ended signaling.

Lane Module: Module at each side of the lane for driving and/or receiving signals on the lane.

Line: An interconnect wire used to connect a driver to a receiver. Three lines are required to create a lane interconnect.

Link: A connection between two devices containing at least one lane. A link consists of at least two PHYs and one lane interconnect.

Master: The master side of a link is defined as the side that transmits the high-speed data. The master side transmits data in the forward direction.

PHY: A functional block that implements the features necessary to communicate over the lane interconnect. A PHY consists of one or more lane modules and a PHY adapter layer.

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PHY Adapter: A protocol layer that converts symbols from an APPI to the signals used by a specific PHY PPI.

PHY Configuration: A set of lanes that represent a possible link. A PHY configuration consists of a one or more lanes.

Reverse Direction: Reverse direction is the opposite of the forward direction. See the description for forward direction.

Slave: The slave side of a link is defined as the side that receives high-speed data from the master. The slave side may transmit data in low-power mode in the reverse direction.

Turnaround: Reversing the direction of communication on a lane.

Unidirectional: A single lane that supports communication in the forward direction only.

Wire State: the combination of signal levels driven on the three lines of a lane.

2.3 Abbreviations

e.g.	For example (Latin: exempli gratia)
i.e.	That is (Latin: id est)

2.4 Acronyms

APPI	Abstracted PHY-Protocol Interface
BER	Bit Error Rate
CIL	Control and Interface Logic
DDR	Double Data Rate
EMI	Electro Magnetic Interference
EoT	End of Transmission
HS	High-Speed; identifier for operation mode
HS-RX	High-Speed Receiver (Low-Swing Differential)
HS-TX	High-Speed Transmitter (Low-Swing Differential)
IEEE	Institute of Electrical and Electronics Engineers
IO	Input-Output
ISTO	Industry Standards and Technology Organization
LP	Low-Power: identifier for operation mode
LP-CD	Low-Power Contention Detector
LPDT	Low-Power Data Transmission
LP-RX	Low-Power Receiver (Large-Swing Single-Ended)
LP-TX	Low-Power Transmitter (Large-Swing Single-Ended)
LPS	Low-Power State(s)
LSB	Least Significant Bit
Mbps	Megabits per second
MSB	Most Significant Bit

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PHY	Physical Layer
PICS	Protocol Implementation Conformance Statement
PLL	Phase-Locked Loop
PPI	PHY-Protocol Interface
PWB	Printed Wiring Board
PRBS	Pseudorandom Binary Sequence
RF	Radio Frequency
RX	Receiver
SE	Single-Ended
SoT	Start of Transmission
TLIS	Transmission-Line Interconnect Structure: physical interconnect realization between Master and Slave
TX	Transmitter
UI	Unit Interval, equal to the duration of any HS state
ULPS	Ultra-Low Power State

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3 References

[MIPI01] *MIPI Alliance Specification for D-PHY*, version 1.2, MIPI Alliance, Inc., 10 September 2014.

[PET01] Peterson, W. Wesley; Weldon, E. J. Jr., *Error-Correcting Codes*, Second Edition, Massachusetts Institute of Technology, 1972.

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4 C-PHY Overview

C-PHY describes a high-speed, rate-efficient PHY, especially suited for mobile applications where channel rate limitations are a factor. The needs of rate limited channels are accomplished through the use of 3-Phase symbol encoding technology delivering approximately 2.28 bits per symbol over a three-wire group of conductors. This C-PHY specification has been written primarily for the connection of cameras and displays to a host processor. Nevertheless, it can be applied to many other applications.

C-PHY has re-used many parts of the D-PHY standard. C-PHY was designed to coexist on the same IC pins as D-PHY so that dual-mode devices can be developed. C-PHY high-speed data coding differs substantially from the D-PHY clock-forwarding system, although the high-speed signal levels and terminations bear some similarity. The low-power mode of D-PHY is reused almost completely, and the transitions to and from the high-speed and low-power modes is very similar to the D-PHY standard.

Key characteristics of C-PHY coding are:

- Uses a group of three conductors rather than conventional pairs. The group of three wires is called a lane, and the individual lines of the lane are called: A, B and C. C-PHY does not have a separate clock lane.
- Within a three-wire lane, two of the three wires are driven to opposite levels; the third wire is terminated to a mid-level (at either one end or both ends), and the voltages at which the wires are driven changes at every symbol.
- Multiple bits are encoded into each symbol epoch, the data rate is ~2.28x the symbol rate. There is no additional overhead for line coding, such as 8b10b, which is not needed.
- Clock timing is encoded into each symbol. This is accomplished by requiring that the combination of voltages driven onto the wires must change at every symbol boundary. This simplifies clock recovery.
- The signal is received using a group of three differential receivers.
- The C-PHY interface can co-exist on the same pins/pads as the D-PHY interface signals.

4.1 Summary of PHY Functionality

The C-PHY provides a synchronous connection between master and slave. A practical PHY configuration consists of one or more three-wire lanes. The link includes a high-speed signaling mode for fast-data traffic and a low-power signaling mode for control purposes. Optionally, a low-power escape mode can be used for low speed asynchronous data communication. High-speed data communication appears in bursts with an arbitrary number of payload data bytes. The low-power mode and escape mode remain the same as defined in the D-PHY specification.

The PHY uses three wires per lane, so three wires are required for the minimum PHY configuration. In high-speed mode each lane is terminated on both sides and driven by a low-swing, 3-Phase signal. In low-power mode all wires are operated single-ended and non-terminated. To minimize EMI, the drivers for this mode shall be slew-rate controlled and current limited.

The maximum achievable bit rate in high-speed mode is determined by the performance of transmitter, receiver and interconnect implementations. This specification is primarily intended to define a solution for a symbol rate range of 80 to 2500 Msps per lane, which is the equivalent of about 182.8 to 5714 Mbps per lane. Although PHY configurations are not limited to this range, practical constraints make it the most suitable range for the intended applications. For a fixed clock frequency, the available data capacity of a PHY configuration can be increased by using more lanes. Effective data throughput can be reduced by employing burst mode communication. The maximum data rate in low-power mode is 10 Mbps.

4.1.1 Summary of Lane Signaling States

Figure 1 shows the current flow through the lane for all six wire states. The circuit examples below are simplified for the data encoding example; they are intended to illustrate the basic signaling states on the three-

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wire link. Figure 1 shows the positive-polarity wire states on the left and negative-polarity wire states on the right. The three rotation states (x, y and z) are shown from top to bottom. The six driven states (called wire states) on a C-PHY lane are called: +x, -x, +y, -y, +z, and -z. The positive polarity wire states have the same wires driven as the corresponding negative polarity states, but the polarity is opposite on the driven pair of wires. For example: the +x wire state is defined as A being driven high and B driven low, while the -x wire state is B driven high and A driven low. The "undriven" conductor can be undriven when operating at lower symbol rates, or is actually driven by a termination at a voltage half way between the highest and lowest driven levels if operating at higher symbol rates.

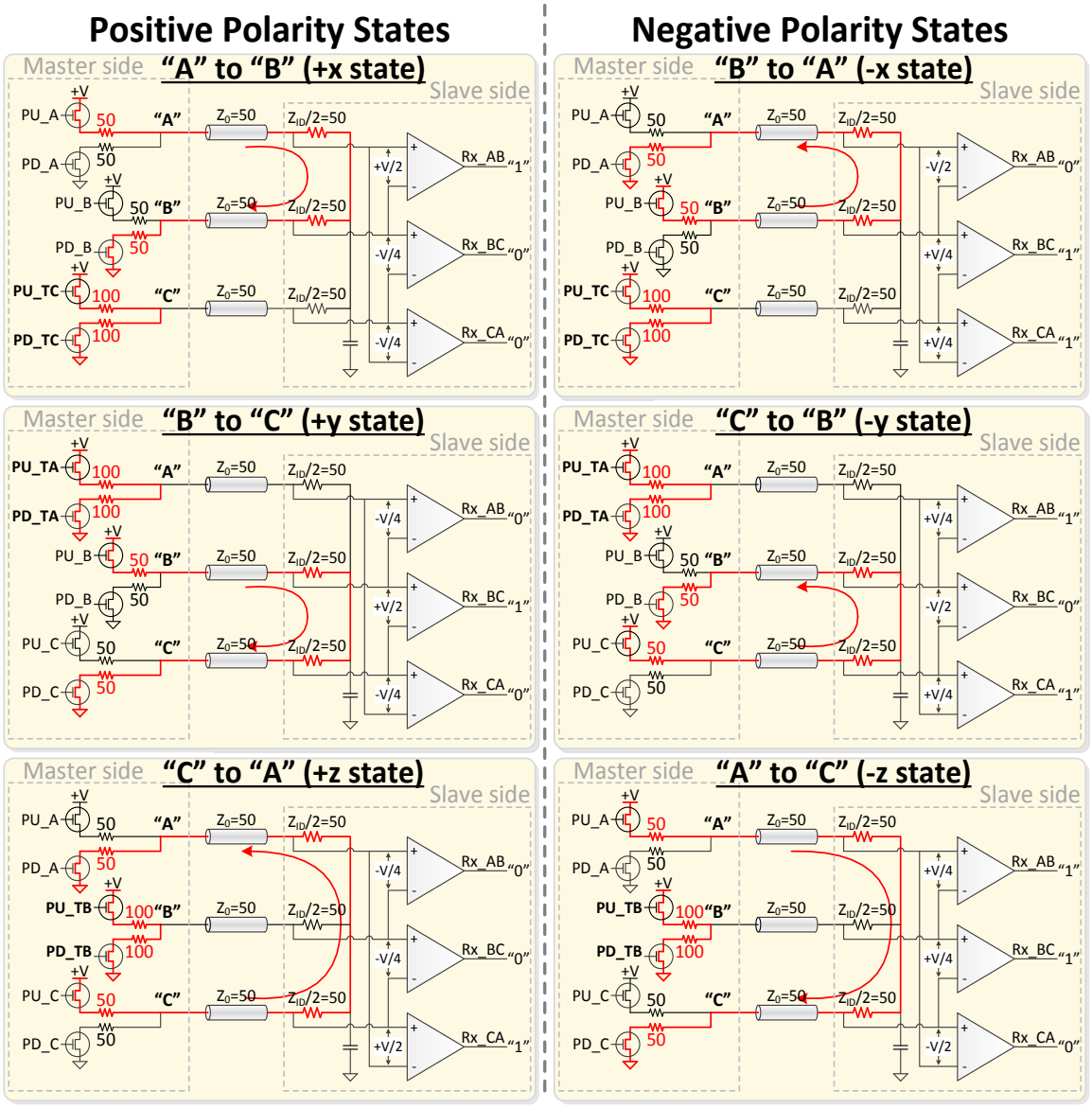

Figure 1 Six Physical Layer Wire States of C-PHY Encoding, Nominal Values Shown

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Table 1 Signal Voltage and Differential Voltage for the Six C-PHY Wire States

Wire State	Wire Amplitude			Receiver diff input voltage			Receiver digital output		
	A	B	C	A – B	B – C	C – A	Rx_AB	Rx_BC	Rx_CA
+x	¾ V	¼ V	½ V	+½ V	-¼ V	-¼ V	1	0	0
-x	¼ V	¾ V	½ V	-½ V	+¼ V	+¼ V	0	1	1
+y	½ V	¾ V	¼ V	-¼ V	+½ V	-¼ V	0	1	0
-y	½ V	¼ V	¾ V	+¼ V	-½ V	+¼ V	1	0	1
+z	¼ V	½ V	¾ V	-¼ V	-¼ V	+½ V	0	0	1
-z	¾ V	½ V	¼ V	+¼ V	+¼ V	-½ V	1	1	0

4.1.2 Representation of Symbols in High-Speed Mode

One of the symbol to wire state encoding rules is that a state-transition exists at every symbol boundary. The reason for this rule is that it encodes the clock timing within the symbol, which has a number of advantages.

With six possible wire states (as shown in Figure 1 and Table 1) there are always 5 possible transitions to the next wire state from any present wire state. The possible state transitions are illustrated in the state diagram in Figure 2. The symbol value is defined by the change in wire state values from one unit interval to the next. Note that more than two bits of information (actually $\log_2(5) = 2.3219$ bits) can be encoded into each symbol. Seven consecutive symbols are used to transmit 16 bits of information. (Note that $5^7 = 78{,}125$ permutations in seven consecutive symbols, with five possible wire state transitions that define each symbol. The information encoded in seven symbols is more than sufficient to represent a 16-bit binary value, $2^{16} = 65{,}536$.)

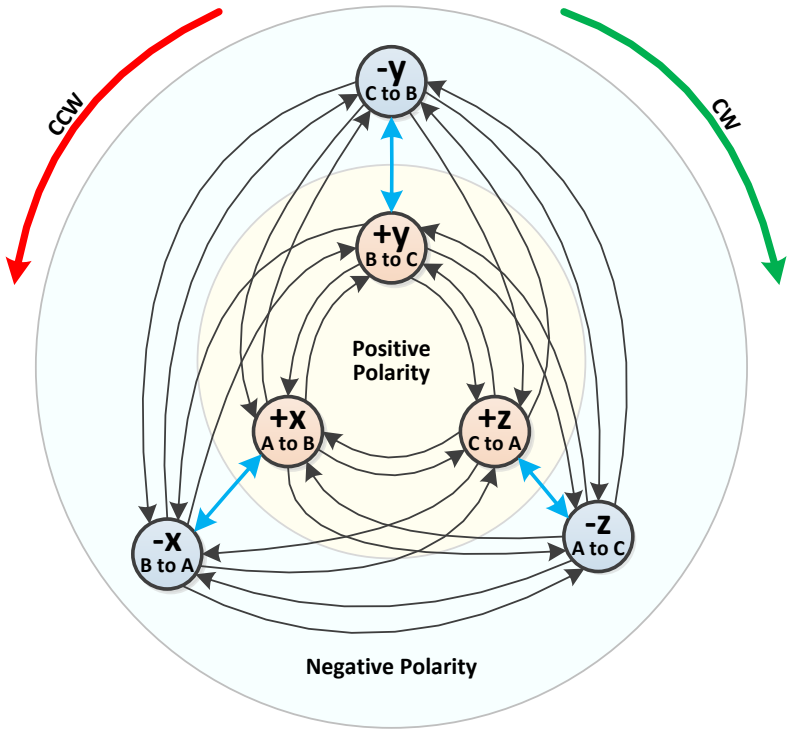

Figure 2 State Diagram Showing All Six Wire States, and All Possible Transitions

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4.1.3 Representation of High-Speed Signaling States

Figure 3 shows all processes involved in the transmission of 16-bit data from the transmitter in the master to the reception of 16-bit words in the receiver at the slave device. 16-bit words at the transmitter are converted to seven channel symbols by a Mapper. Then the seven symbols are serialized and sent one symbol at a time to a Symbol Encoder and 3-wire driver which drives the three signals of the lane (A, B and C lines) at the transmitting end. At the receiving end, there are three differential receivers that receive A minus B, B minus C, and C minus A. The digital outputs of the differential receivers connect to a Symbol Decoder and clock recovery circuit. The output of the Symbol Decoder is fed to a serial-to-parallel converter, and every group of 7 symbols output by the Symbol Decoder is presented to the De-Mapper where they are converted back to a 16-bit word. The functional details of the Mapper, Symbol Encoder, Symbol Decoder and De-Mapper are described in section 6.1.3.

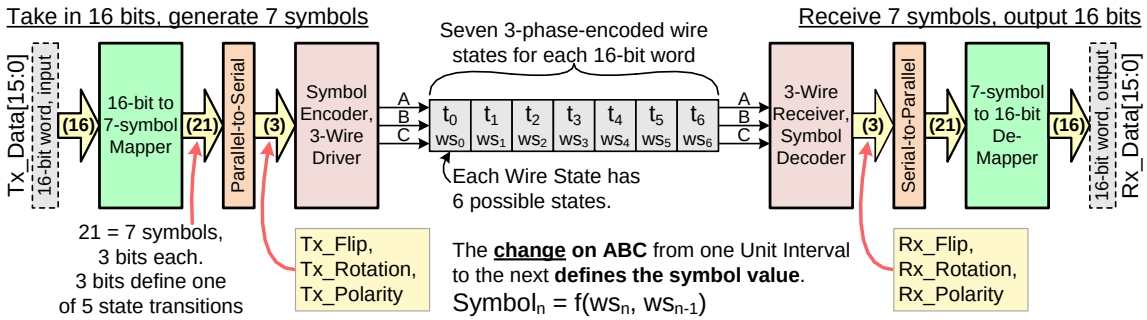

Figure 3 End-to-End Transmission of Data, 16-bit Word Conversion to Channel States

4.2 Mandatory Functionality

All functionality that is specified in this document shall be implemented for all C-PHY configurations, unless it is specifically stated as informative or specified as optional in Section 5.5.

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5 Architecture

This section describes the internal structure of the PHY including its functions at the behavioral level. Furthermore, several possible PHY configurations are given. Each configuration can be considered as a suitable combination from a set of basic modules.

5.1 Lane Modules

A PHY configuration consists of one or more lane modules. Each of these PHY lane modules communicates via three lines to a complementary part at the other side of the lane interconnect.

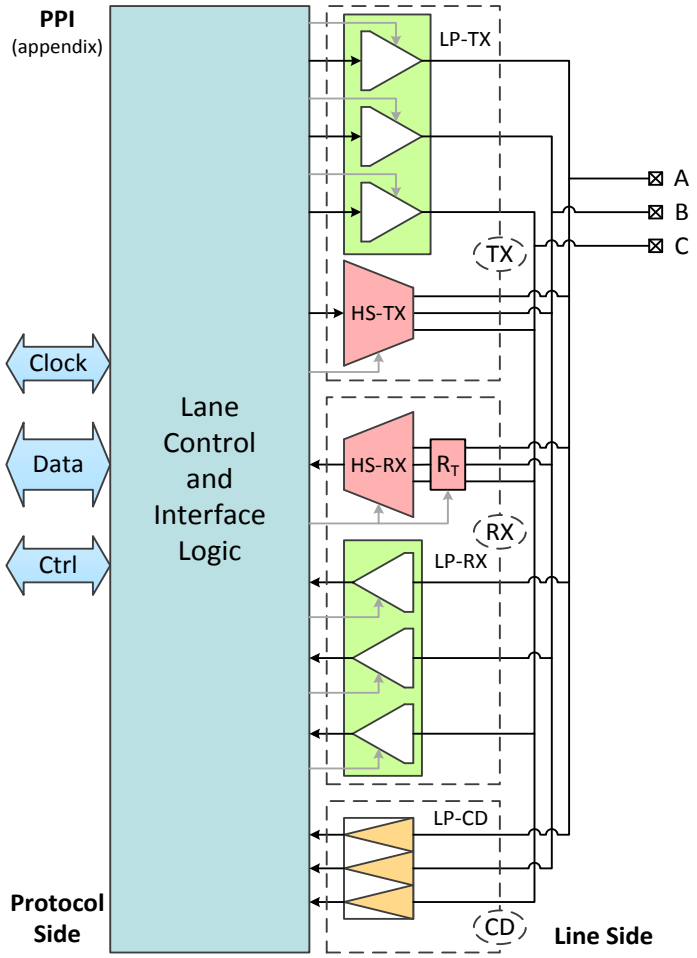

Figure 4 Universal Lane Module Functions

Each lane module consists of one or more high-speed functions utilizing three interconnect wires simultaneously, one or more single-ended low-power functions operating on each of the interconnect wires individually, and control & interface logic. An overview of all functions is shown in Figure 4. High-speed signals have a low voltage swing, e.g. 250 mV, while low-power signals have a large swing, e.g. 1.2V. High-speed functions are used for high-speed data transmission. The low-power functions are mainly used for control, but have other, optional, use cases. The I/O functions are controlled by a Lane Control and Interface Logic block. This block interfaces with the higher layer protocol unit and determines the global operation of the lane module.

High-speed functions include a differential transmitter (HS-TX) and a differential receiver (HS-RX).

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A lane module may contain either a HS-TX or a HS-RX, but not both. An enabled high-speed function shall terminate the lane on its side of the lane interconnect as defined in Section 9.1.1 and Section 9.2.1. If a high-speed function in the lane module is not enabled then the function shall be put into a high impedance state.

Low-power functions include single-ended transmitters (LP-TX), receivers (LP-RX) and low-power Contention-Detectors (LP-CD). Low-power functions are always associated with a lane as these are single-ended functions operating on all three of the interconnect wires individually.

Presence of high-speed and low-power functions is correlated. That is, if a lane module contains a HS-TX it shall also contain a LP-TX. A similar constraint holds for HS-RX and LP-RX.

If a lane module containing a LP-RX is powered, that LP-RX shall always be active and continuously monitor line levels. A LP-TX shall be enabled only when driving low-power states. The LP-CD function is required only for bi-directional operation. If present, the LP-CD function is enabled to detect contention situations while the LP-TX is driving low-power states. The LP-CD checks for contention before driving a new state on the line except in ULPS.

The activities of LP-TX, HS-TX, and HS-RX in a single lane module are mutually exclusive, except for some short crossover periods. For detailed specification of the line-side signals, and the HS-TX, HS-RX, LP-TX, LP-RX and LP-CD functions, refer to Chapter 9 and Chapter 10.

For proper operation, the set of functions in the lane modules on both sides of the lane interconnect has to be matched. This means for each HS and LP transmit or receive function on one side of the lane interconnect, a complementary HS or LP receive or transmit function must be present on the other side. In addition, a contention detector is needed in any lane module that combines TX and RX functions.

5.2 Master and Slave

Each link has a master and a slave side. The master provides the high-speed data signals to each lane and is the main data source. The slave receives the data signals at the lanes and is the main data sink. The main direction of data communication, from source to sink, is denoted as the forward direction. Data communication in the opposite direction is called reverse transmission. Only bi-directional lanes can transmit in LP mode in the reverse direction. High speed reverse data is not supported in any configuration.

5.3 High Frequency Clock Generation

In many cases a PLL Clock Multiplier is needed for the high frequency clock generation at the master side. The C-PHY specification uses an architectural model where a separate Clock Multiplier Unit outside the PHY generates the required high frequency clock signals for the PHY. Whether this Clock Multiplier Unit in practice is integrated inside the PHY is left to the implementer.

5.4 Lanes and the PHY-Protocol Interface

A complete link contains, beside lane modules, a PHY Adapter Layer that ties all lanes, the Clock Multiplier Unit, and the PHY-Protocol Interface together. Figure 5 shows a PHY configuration example for a link with three lanes plus a separate Clock Multiplier Unit. The PHY Adapter Layer, though a component of a PHY, is not within the scope of this specification.

The logical PHY-Protocol interface (PPI) for each individual lane includes a set of signals to cover the functionality of that lane. As shown in Figure 5, Clock signals may be shared for all lanes. The reference clock and control signals for the Clock Multiplier Unit are not within the scope of this specification.

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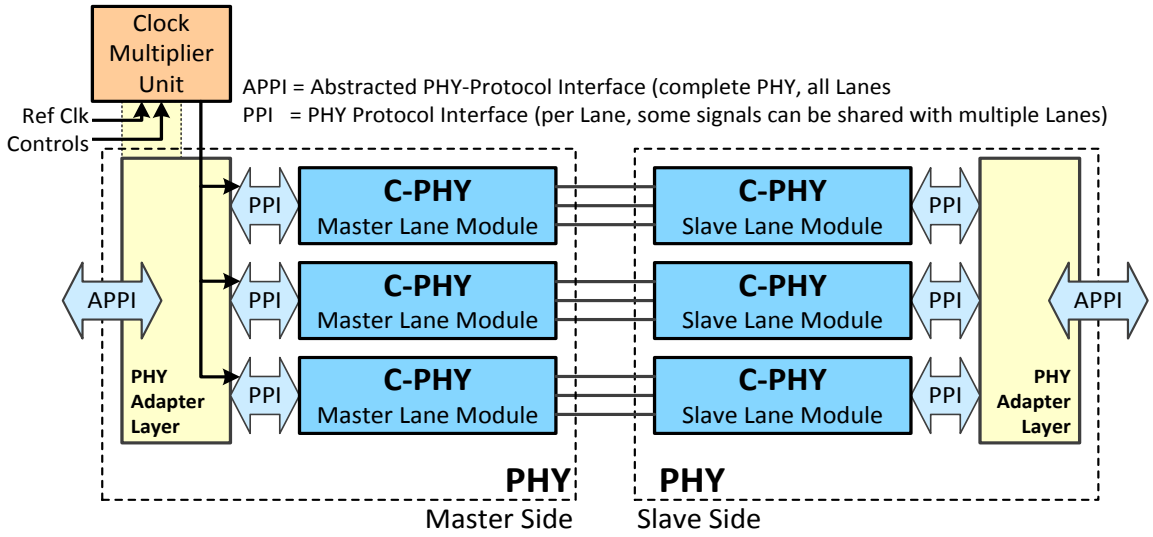

Figure 5 Three Lane PHY Configuration

5.5 Selectable Lane Options

A PHY configuration consists of one or more lanes. All lanes shall support high-speed transmission and escape mode in the forward direction.

There are two main types of lanes:

- Bi-directional (featuring turnaround and some reverse communication functionality)
- Unidirectional (without turnaround or any kind of reverse communication functionality)

Bi-directional lanes shall include the following reverse communication option:

- Low-power reverse escape mode (including or excluding LPDT). Note that high-speed reverse data communication is not supported.

All lanes shall include escape mode support for ULPS and Triggers in the forward direction. Other escape mode functionality is optional; all possible escape mode features are described in Section 6.6. Applications shall define what additional escape mode functionality is required and, for bi-directional lanes, shall select escape mode functionality for each direction individually.

This results in many options for complete PHY configurations. The degrees of freedom are:

- Single or multiple lanes
- Bi-directional and/or unidirectional lane (per lane)
- Supported types of reverse communication (per lane)
- Functionality supported by escape mode (for each direction per lane)

Figure 6 is a flow graph of the option selection process. Practical configuration examples can be found in Section 5.7.

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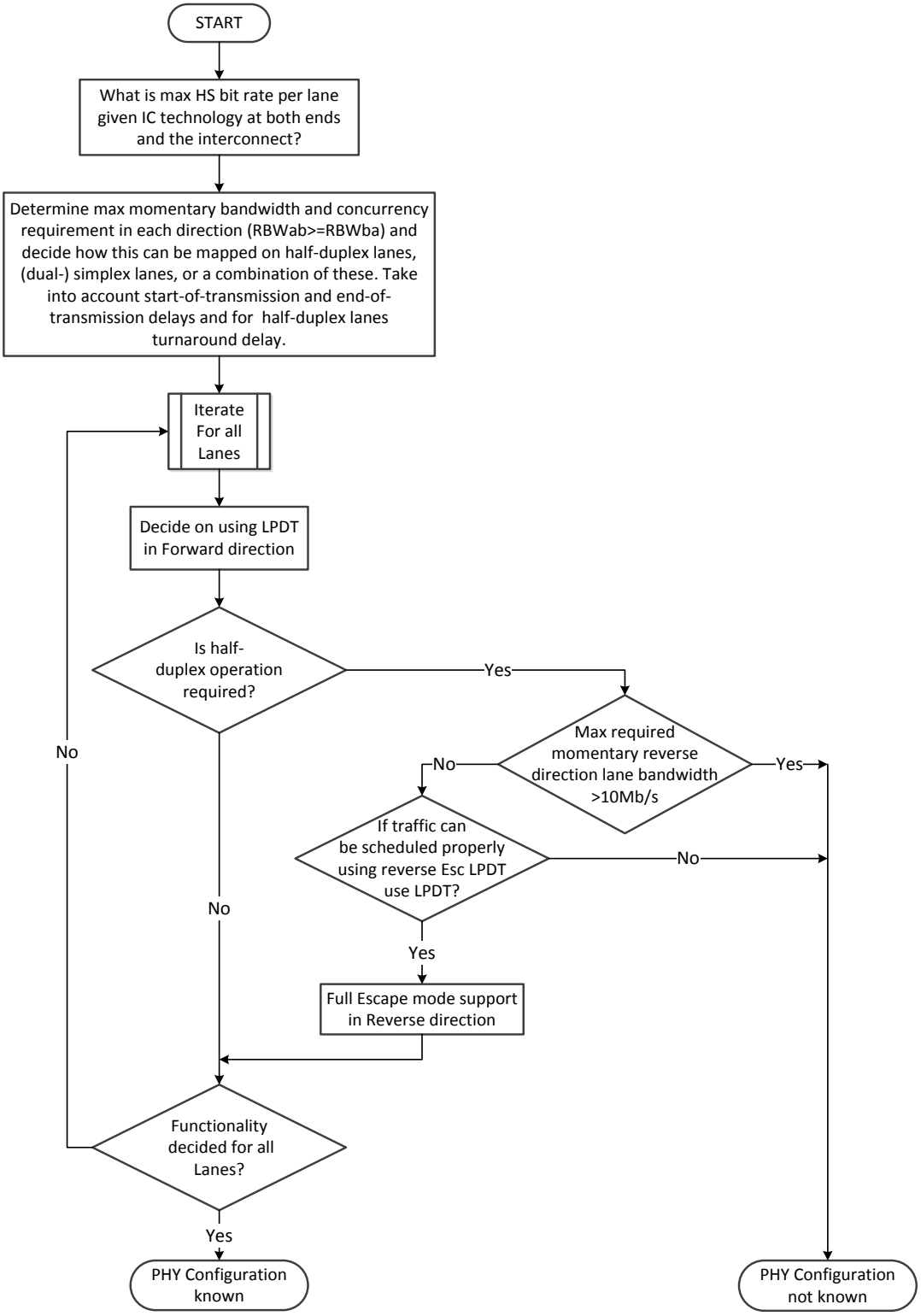

Figure 6 Option Selection Flow Graph

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5.6 Lane Module Types

The required functions in a lane module depend on the lane type and which side of the lane interconnect the lane module is located. There are two main lane types: unidirectional lane and bi-directional lane. Several PHY configurations can be constructed with these lane types. See Figure 6 for more information on selecting lane options. Figure 7 shows a universal lane module diagram with a global overview of internal functionality of the CIL function. This Universal Module can be used for all lane types. The requirements for the 'Control and Interface Logic' (CIL) function depend on the lane type and lane side. Section 6 and Annex A implicitly specify the contents of the CIL function. The actual realization is left to the implementer.

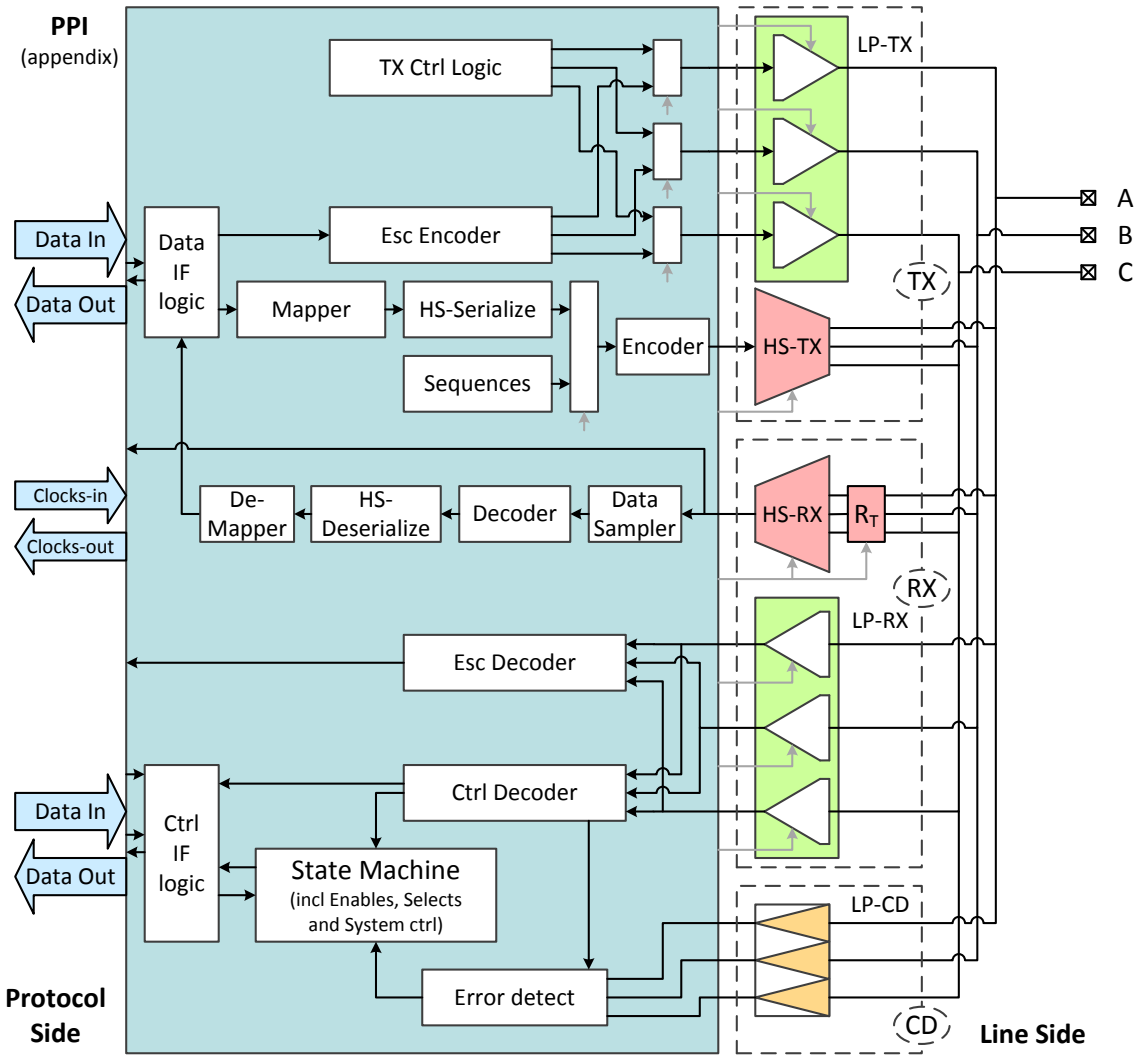

Figure 7 Universal Lane Module Architecture

Of course, stripped-down versions of the universal lane module that just support the required functionality for a particular lane type are possible. These stripped-down versions are identified by the acronyms in Table 2. For simplification reasons, any of the four identification characters can be replaced by an X, which means that this can be any of the available options. For example, a CIL-MFEN is therefore a stripped-down CIL function for the master side of a unidirectional lane with escape mode functionality only in the forward direction. Note that a CIL-XFXN implies a unidirectional link, while either a CIL-XFXE or CIL-XFAA block implies a bidirectional link.

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Table 2 Lane Type Descriptors

Prefix	Lane Interconnect Side	High-Speed Capabilities	Forward Direction Escape Mode Features Supported	Reverse Direction Escape Mode Features Supported
CIL-	M – Master S – Slave X – Don't Care	F – Forward Only	A – All (including LPDT) E – events – Triggers and ULPS Only X – Don't Care	A – All (including LPDT) E – events – Triggers and ULPS Only N – None Y – Any (A, E or A and E) X – Don't Care

Note:

"Any" is any combination of one or more functions.

The recommended PHY-Protocol Interface contains Data-in and Data-out in word format, Input and/or output Clock signals and Control signals. Control signals include requests, handshakes, test settings, and initialization. A proposal for a logical internal interface is described in Annex A. Although not a requirement it may be very useful to use the proposed PPI as a guide. For external use on IC's an implementation may multiplex many signals on the same pins. However, for power efficiency reasons, the PPI is normally within an IC.

5.6.1 Unidirectional Lane

For a unidirectional lane the master module shall contain at least a HS-TX, a LP-TX, and a CIL-MFXN function. The slave side shall contain at least a HS-RX, a LP-RX and a CIL-SFXN.

5.6.2 Bi-directional Lanes

A bi-directional lane Module includes some form of reverse communication; either reverse escape mode, or reverse escape with LPDT. The functions required depend on what methods of reverse communication are included in the lane module.

5.6.2.1 Bi-directional Lane Modes

A bi-directional lane module shall include a low-power reverse escape mode (including or excluding LPDT). The master-side lane module includes a HS-TX, LP-TX, LP-RX, LP-CD, and CIL-MFXY. The slave-side consists of a HS-RX, LP-RX, LP-TX, LP-CD and a CIL-SFXY.

5.7 Configurations

This section outlines several common PHY configurations but should not be considered an exhaustive list of all possible arrangements. Any other configuration that does not violate the requirements of this document is also allowed.

In order to create an abstraction level, the lane modules are represented in this section by lane module Symbols. Figure 8 shows the syntax and meaning of symbols.

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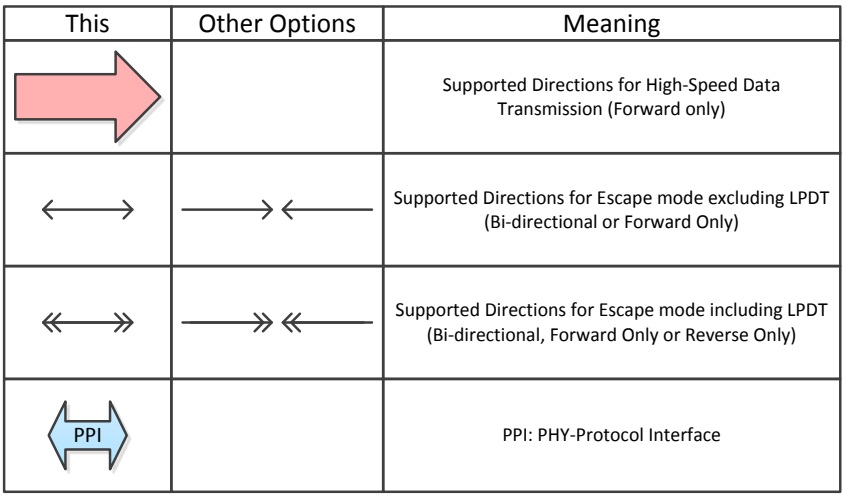

Figure 8 Lane Symbol Macros and Symbols Legend

For multiple lanes a large variety of configurations is possible. Figure 9 shows an overview of symbolic representations for different lane types. The acronyms mentioned for each lane type represent the functionality of each module in a short way. This also sets the requirements for the CIL function inside each Module.

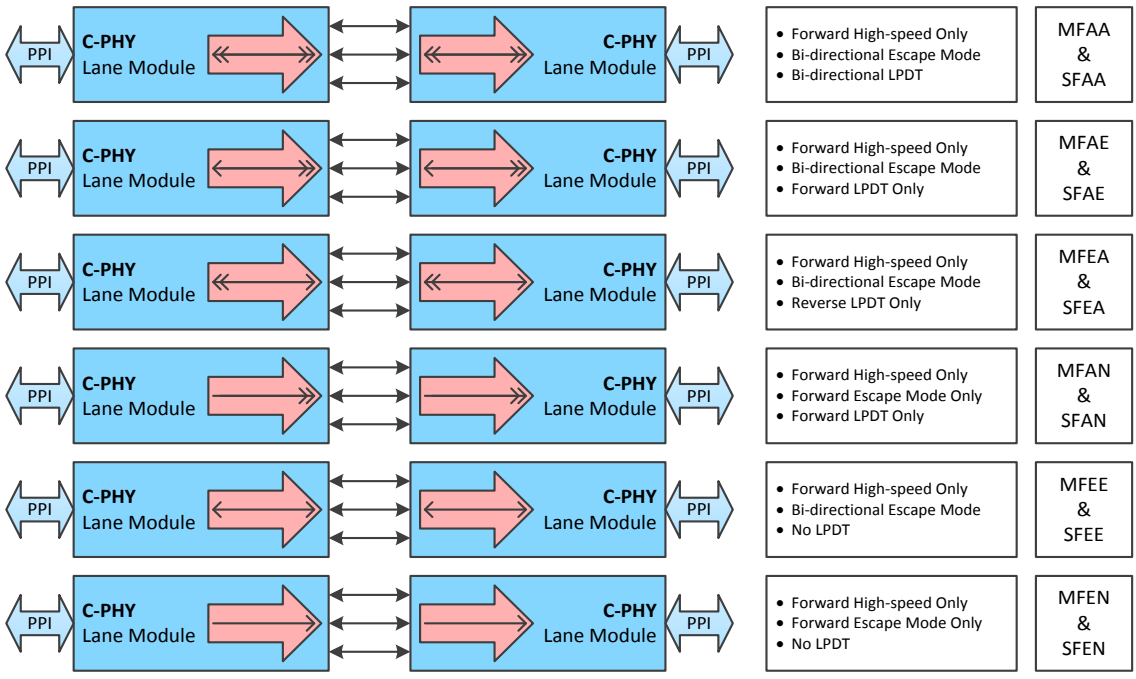

Figure 9 All Possible Lane Types

5.7.1 Unidirectional Configurations

All unidirectional configurations are constructed with one or more unidirectional lanes. Two basic configurations can be distinguished: single-lane and multiple-lanes. For completeness a dual-simplex configuration is also shown. At the PHY level there is no difference between a dual-simplex configuration and two independent unidirectional configurations.

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5.7.1.1 PHY Configuration with a Single Lane

This configuration includes one unidirectional lane from master to slave. Communication is therefore only possible in the forward direction. Figure 10 shows an example configuration without LPDT. This configuration requires three interconnect signal wires.

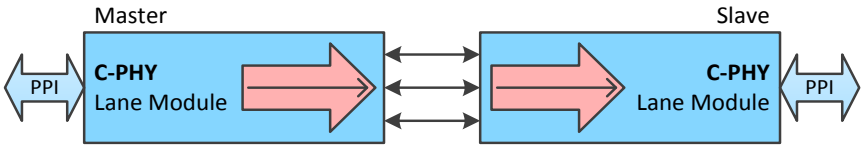

Figure 10 Unidirectional Single Lane Configuration

5.7.1.2 PHY Configuration with Multiple Lanes

This configuration includes multiple unidirectional lanes from master to slave. Bandwidth is extended, but communication is only possible in the forward direction. The PHY specification does not require all lanes to be active simultaneously. In fact, the protocol layer controls all lanes individually. Figure 11 shows an example of this configuration for three lanes. If N is the number of lanes, this configuration requires 3 · N interconnect wires.

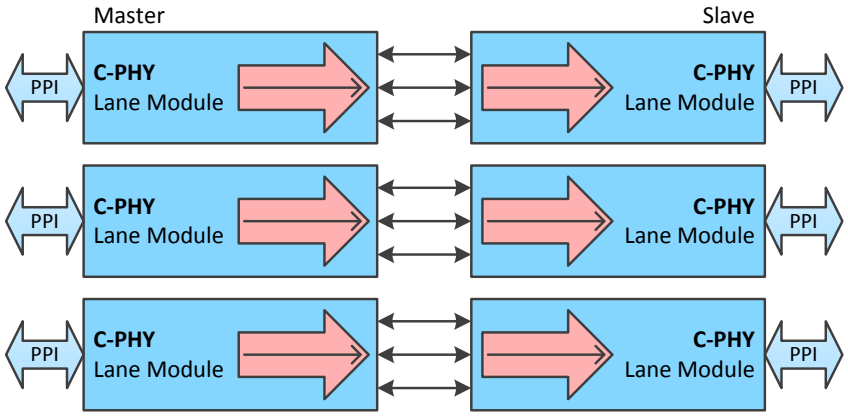

Figure 11 Unidirectional Multiple Lane Configuration without LPDT

5.7.1.3 Dual-Simplex (Two Directions with Unidirectional Lanes)

This case is the same as two independent (dual), unidirectional (simplex) links: one for each direction. Each direction may contain either a single, or multiple, lanes. Please note that the master and slave side for the two different directions are opposite. The PHY configuration for each direction shall comply with the C-PHY specifications. As both directions are conceptually independent, the bit rates for each direction do not have to match. However, for practical implementations, it is attractive to match rates and share some internal signals as long as both links fulfill all specifications externally. Figure 12 shows an example of this dual PHY configuration.

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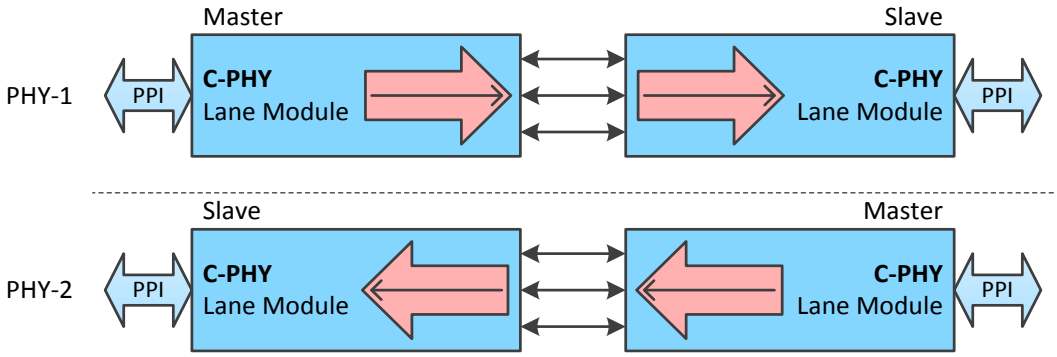

Figure 12 Two Directions Using Two Independent Unidirectional PHYs without LPDT

5.7.2 Bi-Directional Half-Duplex Configurations

Bi-directional configurations consist of one or more bi-directional lanes. Half-duplex operation enables bi-directional traffic across shared interconnect wires. This configuration saves wires compared to the dual-simplex configuration. However, time on the link is shared between forward and reverse traffic and link turnaround. LPDT can have similar rates in the forward and reverse directions. This configuration is especially useful for cases with asymmetrical data traffic.

5.7.2.1 PHY Configurations with a Bi-Directional Single Lane

This configuration includes one of any kind of bi-directional lane. This allows time-multiplexed data traffic in both forward and reverse directions. Figure 13 shows this configuration with a lane that supports both high-speed and escape (without LPDT) communication in both directions. Other possibilities are that only one type of reverse communication is supported or LPDT is also included in one or both directions. All these configurations require three interconnect wires.

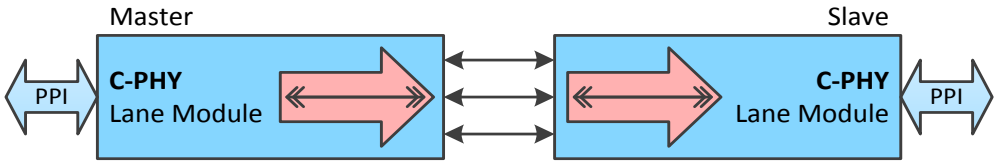

Figure 13 Bidirectional Single Lane Configuration

5.7.2.2 PHY Configurations with Multiple Lanes

This configuration includes multiple bi-directional lanes. Communication is possible in both the forward and reverse direction for each individual lane. The maximum available bandwidth scales with the number of lanes for each direction. The PHY specification does not require all lanes to be active simultaneously or even to be operating in the same direction. In fact, the protocol layer controls all lanes individually. Figure 14 shows an example configuration with two lanes. If N is the number of lanes, this configuration requires 3 · N interconnect wires.

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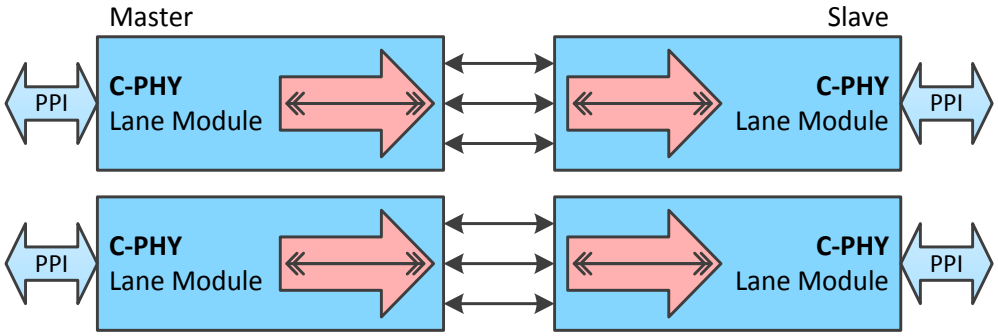

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Figure 14 Bi-directional Multiple Lane Configuration

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6 Global Operation

This section specifies operation of C-PHY including signaling types, communication mechanisms, operating modes and coding schemes. Detailed specifications of the required electrical functions can be found in Section 9.

6.1 Transmission Data Structure

During high-speed, or low-power, transmission, the link transports payload data provided by the protocol layer to the other side of the link. This section specifies the restrictions for the transmitted and received payload data.

6.1.1 Data Units

The minimum payload data unit for the high-speed mode of transmission shall be one 16-bit word. Data provided to a TX and taken from a RX on any lane operating in high-speed mode shall be an integer number of 16-bit words.

The minimum payload data unit for the low-power mode of transmission shall be one byte. Data provided to a TX and taken from a RX on any lane operating in low-power mode shall be an integer number of bytes.

6.1.2 Bit order, Serialization, and De-Serialization

For serial transmission, the data shall be serialized in the transmitting PHY and de-serialized in the receiving PHY. For high-speed data transmission the PHY maps 16-bit words into groups of seven symbols as described in section 6.1.3.3. Symbol s6 is defined as the most significant symbol of the seven symbol group and symbol s0 is defined as the least significant symbol. The group of seven symbols shall be transmitted in the sequence of: s0, s1, s2, s3, s4, s5, s6, where s0 shall be transmitted first. Symbol s1 shall be transmitted in the UI immediately following symbol s0, s2 shall be transmitted in the UI immediately following s1, and so on, and s6 shall be transmitted in the UI immediately following s5. Symbol s0 of the next group of seven symbols shall be transmitted in the UI immediately following s6 of the present group.

6.1.3 Encoding, Decoding, Mapping and De-Mapping

C-PHY shall use two layers of coding with serialization and deserialization in between, as illustrated in Figure 3:

1. **Mapping and De-Mapping** – A Mapper converts a 16-bit data unit to be transmitted into a group of seven transmitted symbols. A De-Mapper converts a group of 7 received symbols into a 16-bit data unit.
2. **Serialization and Deserialization** – A parallel to serial converter accepts a group of 7 symbols from the Mapper and presents one symbol at a time to the Symbol Encoder. A serial to parallel converter accepts one symbol at a time from the Symbol Decoder and presents a group of 7 symbols to the De-Mapper.
3. **Encoding and Decoding** – A Symbol Encoder converts one symbol into a wire state to be sent over the lane based on the present 3-bit symbol value and the wire state that was transmitted in the previous UI. A Symbol Decoder computes a received symbol value based on the wire state received in the present UI and the wire state received in the previous UI.

6.1.3.1 Wire States

One of six possible high-speed wire states shall be driven onto a lane during a high-speed unit interval (UI). Each of the lines of a lane shall be driven to one of three signal levels: low, middle or high. In some implementations the middle signal level can be the result of the transmitter not driving the signal. Each of the three lines in a lane shall be at a different signal level than the other two lines. The six wire states consist of the six possible permutations of driving the three lines of a lane with a different signal level on each line.

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The six wire states shall be called +x, -x, +y, -y, +z and –z are defined as described in Table 3. Examples of the wire states are shown in Figure 1 and Table 1.

The wire states defined as having a positive polarity are: +x, +y and +z. The wire states defined as having a negative polarity are: -x, -y and -z.

Table 3 Definition of Wire States

Wire State Name	High-Speed State Code Name	Line Signal Levels		
		A	B	C
+x	HS_+X	High	Low	Middle
-x	HS_-X	Low	High	Middle
+y	HS_+Y	Middle	High	Low
-y	HS_-Y	Middle	Low	High
+z	HS_+Z	Low	Middle	High
-z	HS_-Z	High	Middle	Low

6.1.3.2 Symbol Encoding and Decoding

Each symbol shall be represented using a 3-bit number having one of five values: 000, 001, 010, 011 and 100. The symbol values are based on the specific transitions between the wire states as shown in Figure 2. These transitions are derived from the 3-bit symbol value where each bit defines a particular wire state change parameter: flip, rotate, and polarity. The flip, rotate and polarity bits affect the wire state as follows:

- The least significant bit of the 3-bit symbol value is Polarity, which indicates whether the polarity changes state from the previous symbol. When Polarity is “one” then the wire state transmitted during symbol interval N has a polarity that is opposite that of the wire state transmitted during symbol interval N-1 (i.e. from positive: +x, +y, +z to negative: -x, -y, -z; or negative to positive); else if Polarity is “zero” then the polarity of the wire state transmitted during symbol interval N remains the same as the wire state transmitted during symbol interval N-1.
- The next least significant bit of the 3-bit value is Rotation, which indicates the direction of rotation from the wire state transmitted during symbol interval N-1 compared to the wire state transmitted during symbol interval N. When Rotation is one, then the direction of rotation is clockwise; else, when Rotation is zero then the direction of rotation is counterclockwise.
- The most significant bit of the 3-bit symbol value is Flip, which indicates there is only a polarity change in the next symbol but the wire state will not rotate to a different phase. A Flip causes a transition between states +x and -x, between +y and -y, or between +z and -z. The flip transitions are represented by the blue arrows in Figure 2. When Flip is one then the phase is the same as the previous symbol but the polarity is opposite of the polarity in the previous symbol. Also, when Flip is one then the values of Rotation and Polarity for the same corresponding symbol are ignored, and are both set to zero.

6.1.3.2.1 Encoding

The symbol encoding shall be performed as described in Table 4, which defines the symbol encoding algorithm. The translation defined in Table 4 converts one 3-bit symbol value into a wire state to be sent over the lane based on the present 3-bit symbol value and the wire state that was transmitted in the previous UI. Every transition in the state diagram of Figure 2 is represented in Table 4. The present wire state is determined by the previous wire state and the symbol input value. For example: if the 3-bit symbol value is 011 (no flip, CW rotation, opposite polarity) and the previous wire state is +y, then the next wire state is -z.

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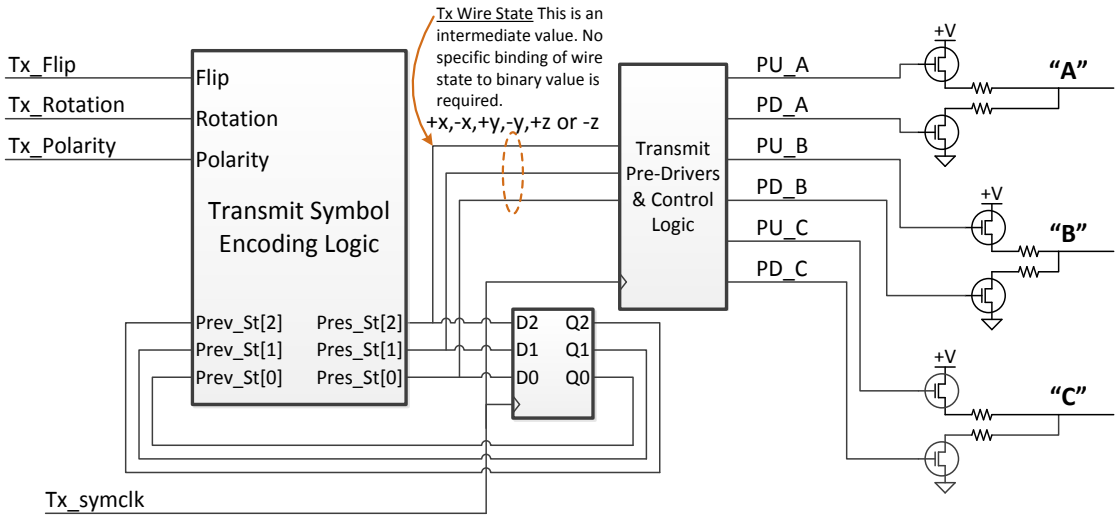
463 **Table 4 Five possible transitions from previous state to present state**

Symbol Input Value	Previous Wire State, interval N-1						What Happens
	+x	-x	+y	-y	+z	-z	
000	+z	-z	+x	-x	+y	-y	Rotate CCW, polarity is Same
001	-z	+z	-x	+x	-y	+y	Rotate CCW, polarity is Opposite
010	+y	-y	+z	-z	+x	-x	Rotate CW, polarity is Same
011	-y	+y	-z	+z	-x	+x	Rotate CW, polarity is Opposite
1xx	-x	+x	-y	+y	-z	+z	Same phase, polarity is Opposite

Note:

1. *Symbol Input value is: [Tx_Flip, Tx_Rotation, Tx_Polarity]*
2. *Values in the table show the Present Wire State transmitted during interval N, as a function of the Previous Wire State transmitted during interval N-1, and 3-bit Symbol Value.*

464 An example Transmit Encoder and driver circuit is shown in Figure 15. The 3-bit binary values that represent
465 the previous and present wire state in Figure 15 exist only to make the example easier to follow. This is to
466 break the process in the example into two steps: Transmit Symbol Encoding Logic and Transmit Pre-driver
467 Control Logic. The wire state binary values are internal to the Symbol Encoder and Transmitter circuit, so
468 the values that describe the wire states within these blocks are an implementation choice. For example: the
469 actual logic circuit could use the decoded 6-bit pre-driver value [PU_A, PD_A, PU_B, PD_B, PU_C, PD_C]
470 to define the present wire state value (using only 6 of the 64 possible values) instead of using the intermediate
471 3-bit wire state value.



472 **Figure 15 Encoder and Transmitter Example**

Table 5 Transmit Pre-Driver Control Logic

Wire State	VA	VB	VC	Driver PU_A	Driver PD_A	Driver PU_B	Driver PD_B	Driver PU_C	Driver PD_C
+x	¾ V	¼ V	½ V	1	0	0	1	0	0
-x	¼ V	¾ V	½ V	0	1	1	0	0	0
+y	½ V	¾ V	¼ V	0	0	1	0	0	1
-y	½ V	¼ V	¾ V	0	0	0	1	1	0
+z	¼ V	½ V	¾ V	0	1	0	0	1	0

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-z	¾ V	½ V	¼ V	1	0	0	0	0	1

Note that the Transmit Pre-Driver Control Logic table is shown only to illustrate the logic function of the translation of wire state to driver control signals. The actual implementation may require carefully designed routing and signal gating to precisely control the skew between the A, B and C wires of the lane.

6.1.3.2.2 Decoding

The symbol decoding function shall be performed as described in Table 6. Every transition in the state diagram of Figure 2 is represented in Table 6. Note that there are no transitions to the same state (because there is always a wire state transition at each symbol boundary) so the table shows "n/a" to indicate that these transitions are not applicable. The symbol value shall be determined based on the transition from the previous wire state (interval N-1) to the present wire state (interval N). For example: if the previous wire state is +y which results in "010" at the output of the receivers (prev_Rx_AB=0, prev_Rx_BC=1, prev_Rx_CA=0) and the present wire state is -z which results in "110" at the output of the receivers (Rx_AB=1, Rx_BC=1, Rx_CA=0), then the symbol value is 011 which represents: no flip, a CW rotation and polarity change. This symbol value of 011 is located in Table 6 where the "+y" column and the "-z state" row intersect. ("y" toward "z" is CW rotation and "+" to "-" is a polarity change.)

Table 6 Receive Transition Mapping

Present Wire State [Rx_AB, Rx_BC, Rx_CA] (received during interval N)	**Previous Wire State [prev_Rx_AB, prev_Rx_BC, prev_Rx_CA] (wire state received during interval N-1)**					
	+x [100]	**-x [011]**	**+y [010]**	**-y [101]**	**+z [001]**	**-z [110]**
+x state [100]	n/a	1xx	000	001	010	011
-x state [011]	1xx	n/a	001	000	011	010
+y state [010]	010	011	n/a	1xx	000	001
-y state [101]	011	010	1xx	n/a	001	000
+z state [001]	000	001	010	011	n/a	1xx
-z state [110]	001	000	011	010	1xx	n/a
	symbol value above = [Rx_Flip, Rx_Rotation, Rx_Polarity]					

An example receiver circuit with symbol decoding is shown below in Figure 16.

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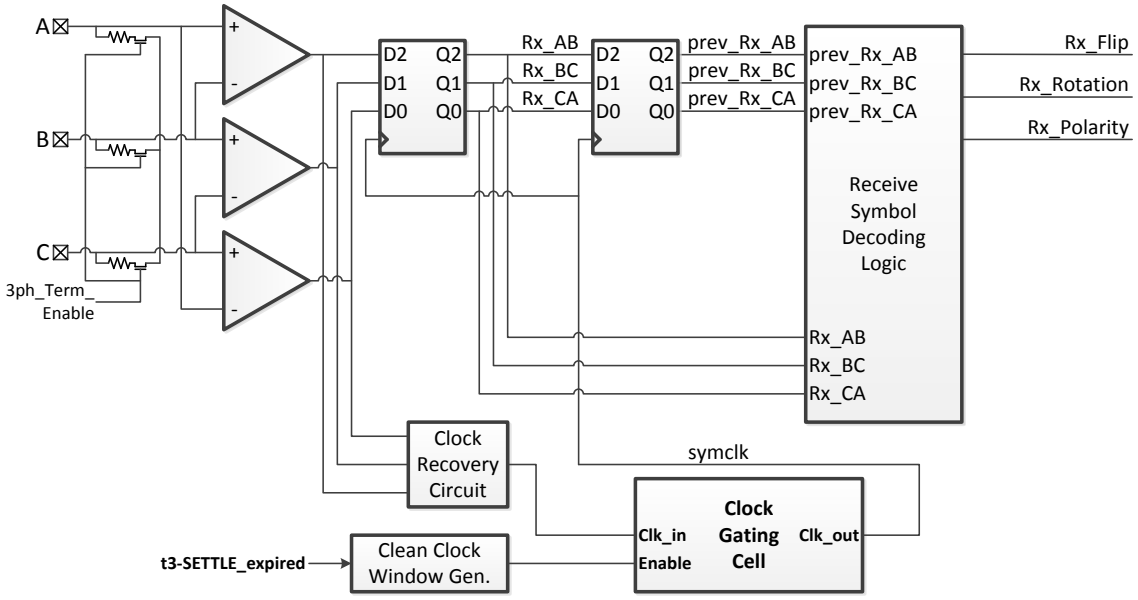

Figure 16 Receiver and Symbol Decoder Example

6.1.3.3 16-to-7 Mapping and 7-to-16 De-Mapping Circuit Implementation

The Mapper and De-Mapper are the outer-most functions in the C-PHY digital coding system. The Mapper is the first function that occurs on the transmit side, and the De-Mapper is the last function performed on the receive side. This order of functions is shown in Figure 3. The Mapper converts a 16-bit word into a group of seven symbols at the transmitting end. At the receiving end, a 7-to-16 De-Mapper converts groups of seven symbols back to 16-bit words. The mapping process is described in 6.1.3.3.1, and the de-mapping process is described in 6.1.3.3.2.

The 16-to-7 Mapper and 7-to-16 De-Mapper perform a mapping and inverse mapping function between 16-bit input/output values and a group of 7 symbols. The Mapper and De-Mapper shall conform to the process defined in Figure 17.

The group of seven symbols is comprised of seven 3-bit symbol values. Each symbol is comprised of a flip, rotate and polarity bit, so for any particular symbol, n, sn = [Flip[n], Rotation[n], Polarity[n]].

A seven-symbol Mapper output value is defined for every possible 16-bit Mapper input value. However, not all possible seven symbol sequences correspond to a 16-bit mapper input value. The output of the De-Mapper is not defined when an invalid group of seven symbols is presented to the input of the De-Mapper. An invalid group of seven symbols is defined as the collection of symbols having a value of “4” (the state of Flip[6:0]) that does not correspond to one of the 28 mapped regions defined in Figure 17. The De-Mapper output is not specified for these invalid groups of seven symbols, so the De-Mapper output should be an implementation choice when an invalid seven symbol group is presented to the De-Mapper.

Since the mapping and inverse mapping functions are completely feed-forward functions, pipeline registers can be inserted between intermediate stages if necessary to lessen timing constraints in systems that operate at a high symbol rate.

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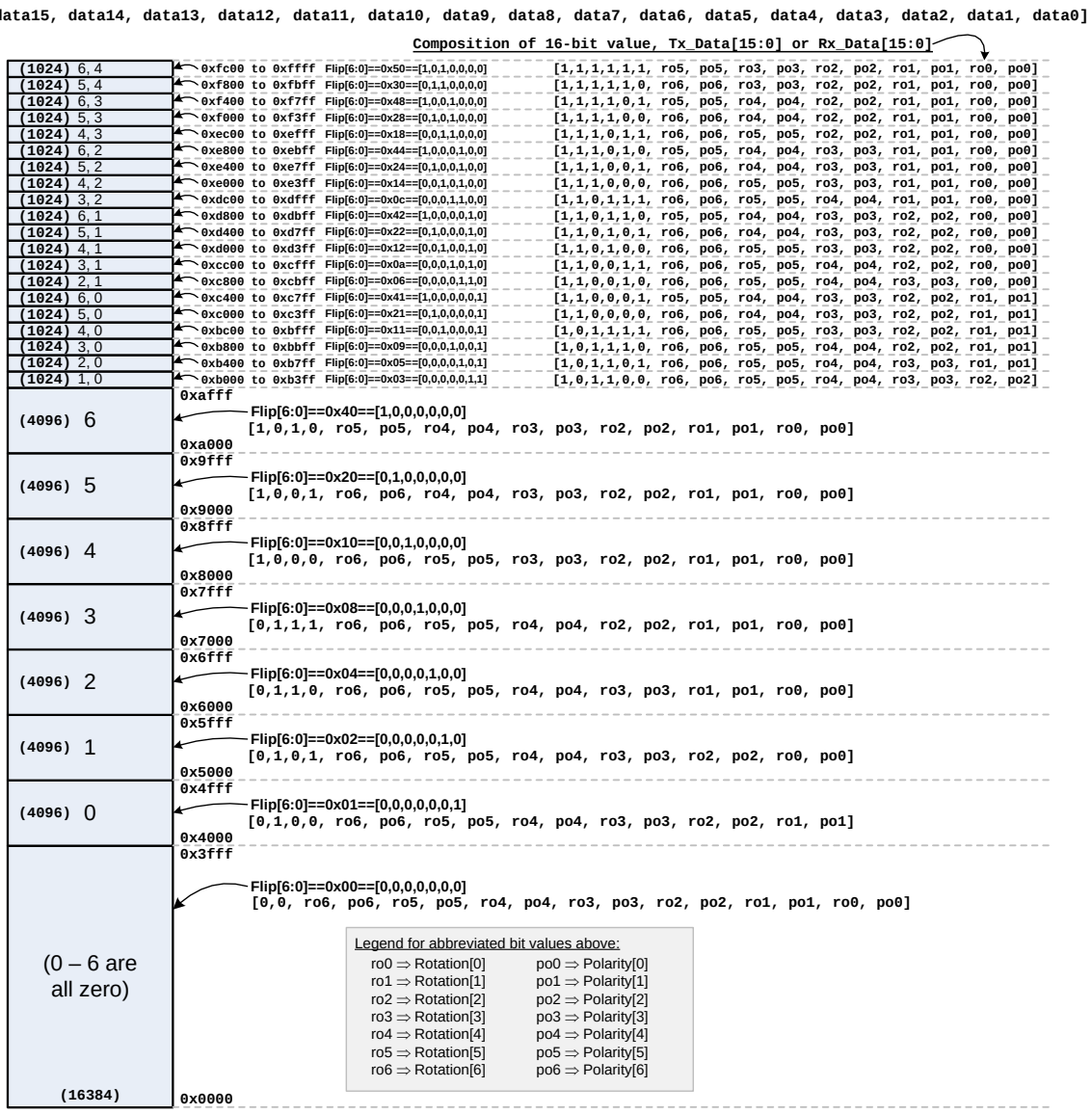

Figure 17 Data Mapping Between Seven Symbols and a 16-Bit Word

Figure 17 specifies the mapping of 16-bit words to groups of seven symbols. The value of the 16-bit word is shown on the left, ranging from 0x0000 at the bottom to 0xffff at the top. The vectors enclosed in square brackets to the right show the correspondence of Rotation and Polarity values to specific bits in the 16-bit word. The seven Flip bits of the seven symbols define one of 28 different regions within the 16-bit range. One region contains 16,384 values, 7 regions contain 4,096 values each, and 20 regions contain 1,024 values each. The use of these varying sized regions simplifies the mapping function.

6.1.3.3.1 Tx 16-bit to 7-symbol Mapper

The Mapper shall perform a translation of a 16-bit value to a seven symbol group per the mapping function defined in Figure 17.

A high-level diagram of an example of a 16-to-7 Mapper is shown in Figure 18, and a low-level implementation of the Mapper example is shown in Figure 19.

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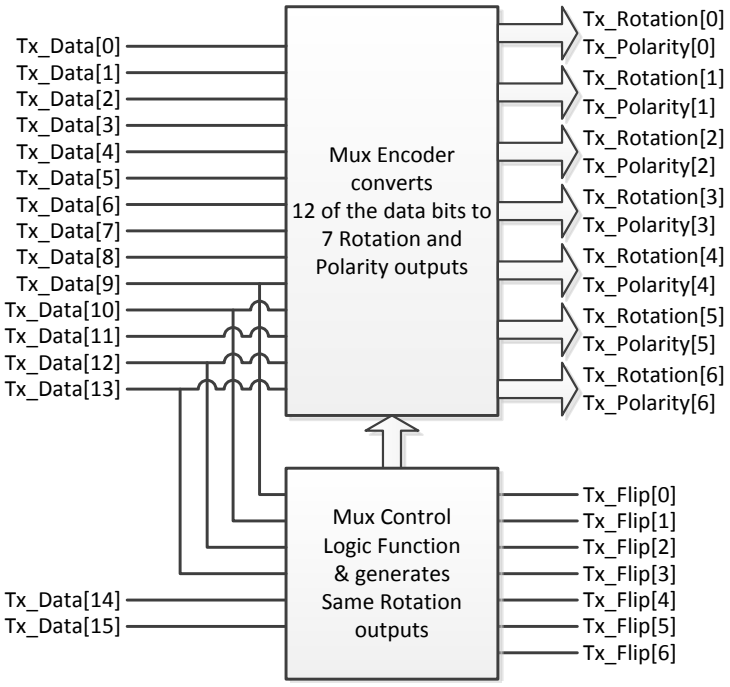

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Figure 18 Example, Mapping Circuit Converts 16-bit Word to Seven Symbols

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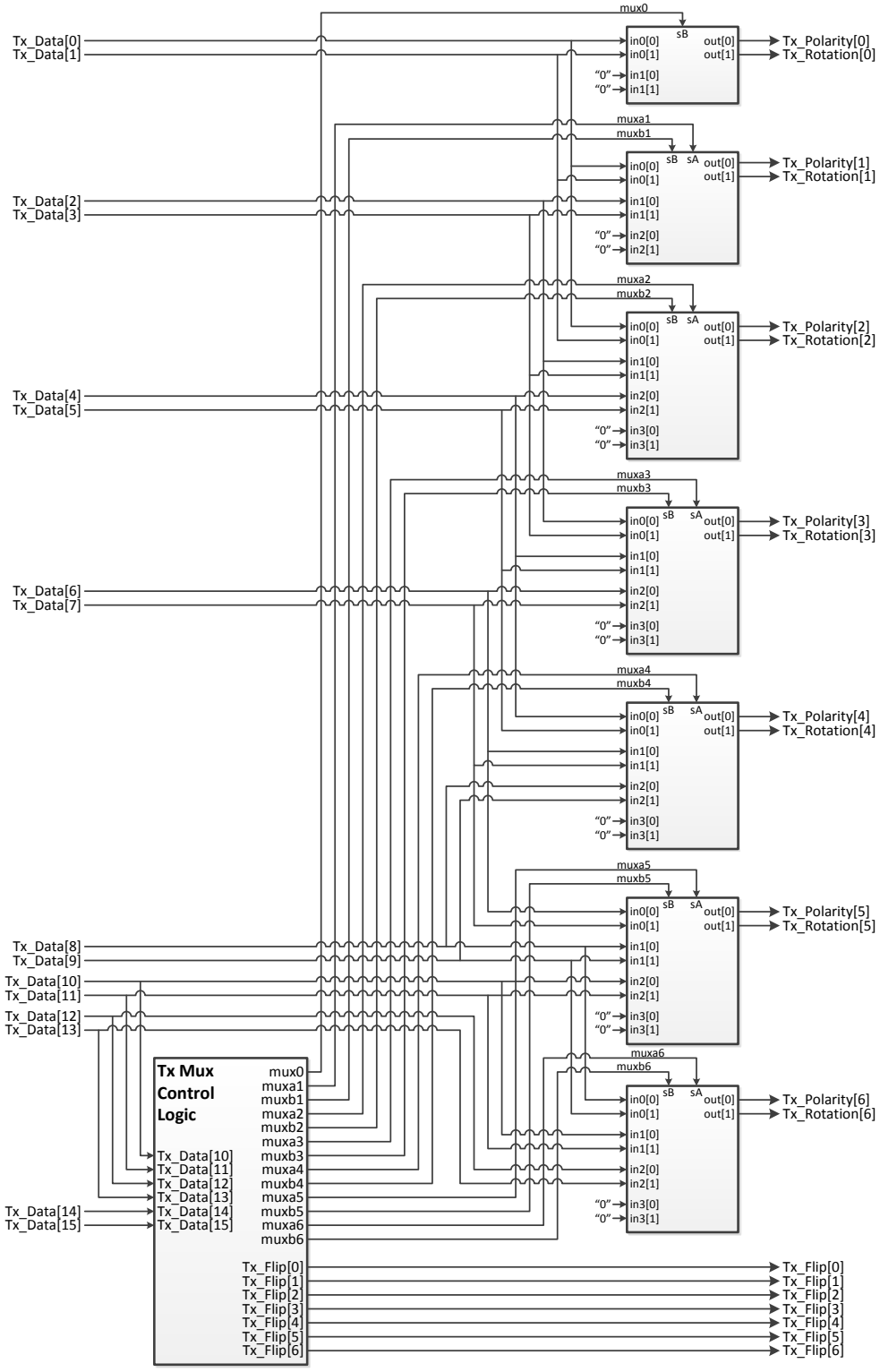

Figure 19 Example, Detailed Logic Diagram of 16-bit word to 7-Symbol Mapping Circuit

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Figure 19 shows the low-level circuit of the 16-to-7 Mapper example in the block diagram of Figure 18 that performs the conversion of a 16-bit data word to be transmitted into seven consecutive symbols. The logic function of the "Tx Mux Control Logic" in the Figure 19 example appears below in Table 7.

Table 7 Truth Table of the "Tx Mux Control Logic" in Figure 19

Tx_Data [15:10]	muxb6	muxa6	muxb5	muxa5	muxb4	muxa4	muxb3	muxa3	muxb2	muxa2	muxb1	muxa1	mux0	Flip[6:0]
0x00 – 0x0f	1	0	1	0	1	0	1	0	1	0	0	1	0	0x00
0x10 – 0x13	0	1	0	1	0	1	0	1	0	1	0	0	1	0x01
0x14 – 0x17	0	1	0	1	0	1	0	1	0	1	1	0	0	0x02
0x18 – 0x1b	0	1	0	1	0	1	0	1	1	1	0	1	0	0x04
0x1c – 0x1f	0	1	0	1	0	1	1	1	1	0	0	1	0	0x08
0x20 – 0x23	0	1	0	1	1	1	1	0	1	0	0	1	0	0x10
0x24 – 0x27	0	1	1	1	1	0	1	0	1	0	0	1	0	0x20
0x28 – 0x2b	1	1	1	0	1	0	1	0	1	0	0	1	0	0x40
0x2c	0	0	0	0	0	0	0	0	0	0	1	0	1	0x03
0x2d	0	0	0	0	0	0	0	0	1	1	0	0	1	0x05
0x2e	0	0	0	0	0	0	1	1	0	1	0	0	1	0x09
0x2f	0	0	0	0	1	1	0	1	0	1	0	0	1	0x11
0x30	0	0	1	1	0	1	0	1	0	1	0	0	1	0x21
0x31	1	1	0	1	0	1	0	1	0	1	0	0	1	0x41
0x32	0	0	0	0	0	0	0	0	1	1	1	0	0	0x06
0x33	0	0	0	0	0	0	1	1	0	1	1	0	0	0x0a
0x34	0	0	0	0	1	1	0	1	0	1	1	0	0	0x12
0x35	0	0	1	1	0	1	0	1	0	1	1	0	0	0x22
0x36	1	1	0	1	0	1	0	1	0	1	1	0	0	0x42
0x37	0	0	0	0	0	0	1	1	1	1	0	1	0	0x0c
0x38	0	0	0	0	1	1	0	1	1	1	0	1	0	0x14
0x39	0	0	1	1	0	1	0	1	1	1	0	1	0	0x24
0x3a	1	1	0	1	0	1	0	1	1	1	0	1	0	0x44
0x3b	0	0	0	0	1	1	1	1	1	0	0	1	0	0x18
0x3c	0	0	1	1	0	1	1	1	1	0	0	1	0	0x28
0x3d	1	1	0	1	0	1	1	1	1	0	0	1	0	0x48
0x3e	0	0	1	1	1	1	1	0	1	0	0	1	0	0x30
0x3f	1	1	0	1	1	1	1	0	1	0	0	1	0	0x50

6.1.3.3.2 Rx 7-symbol to 16-bit De-Mapper

The De-Mapper shall perform a translation of a seven symbol group to a 16-bit value per the mapping function defined in Figure 17.

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A high-level diagram of an example of a 7-to-16 De-Mapping circuit is shown in Figure 20, and a detailed low-level implementation of the De-Mapper example is shown in Figure 21.

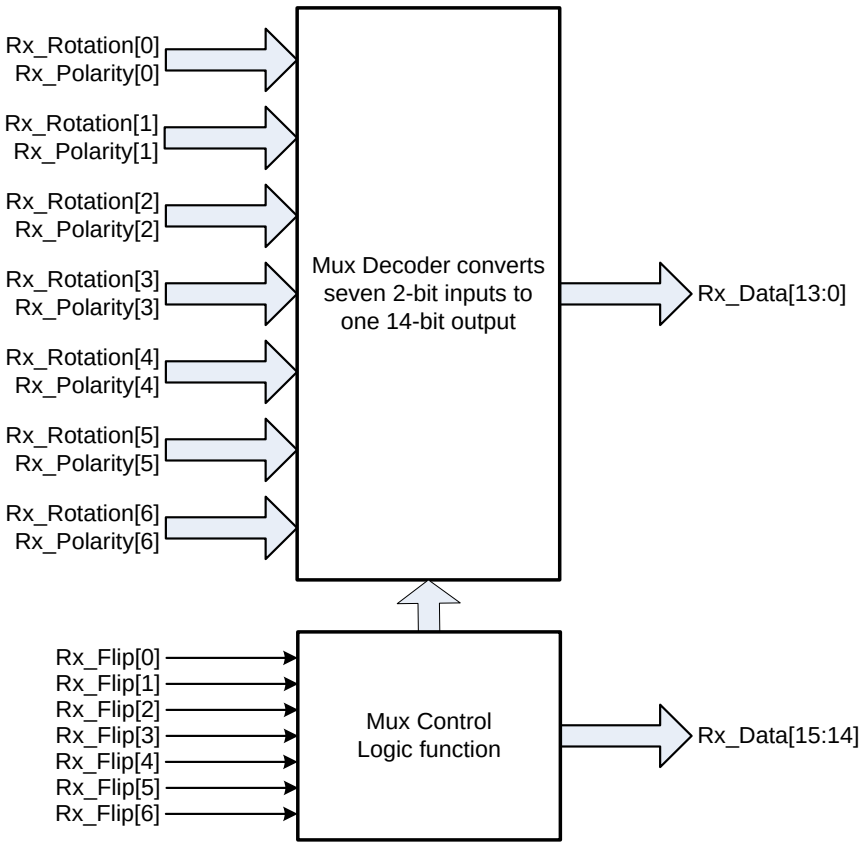

Figure 20 Example, De-Mapping Circuit Converts Seven Symbols to a 16-Bit Word

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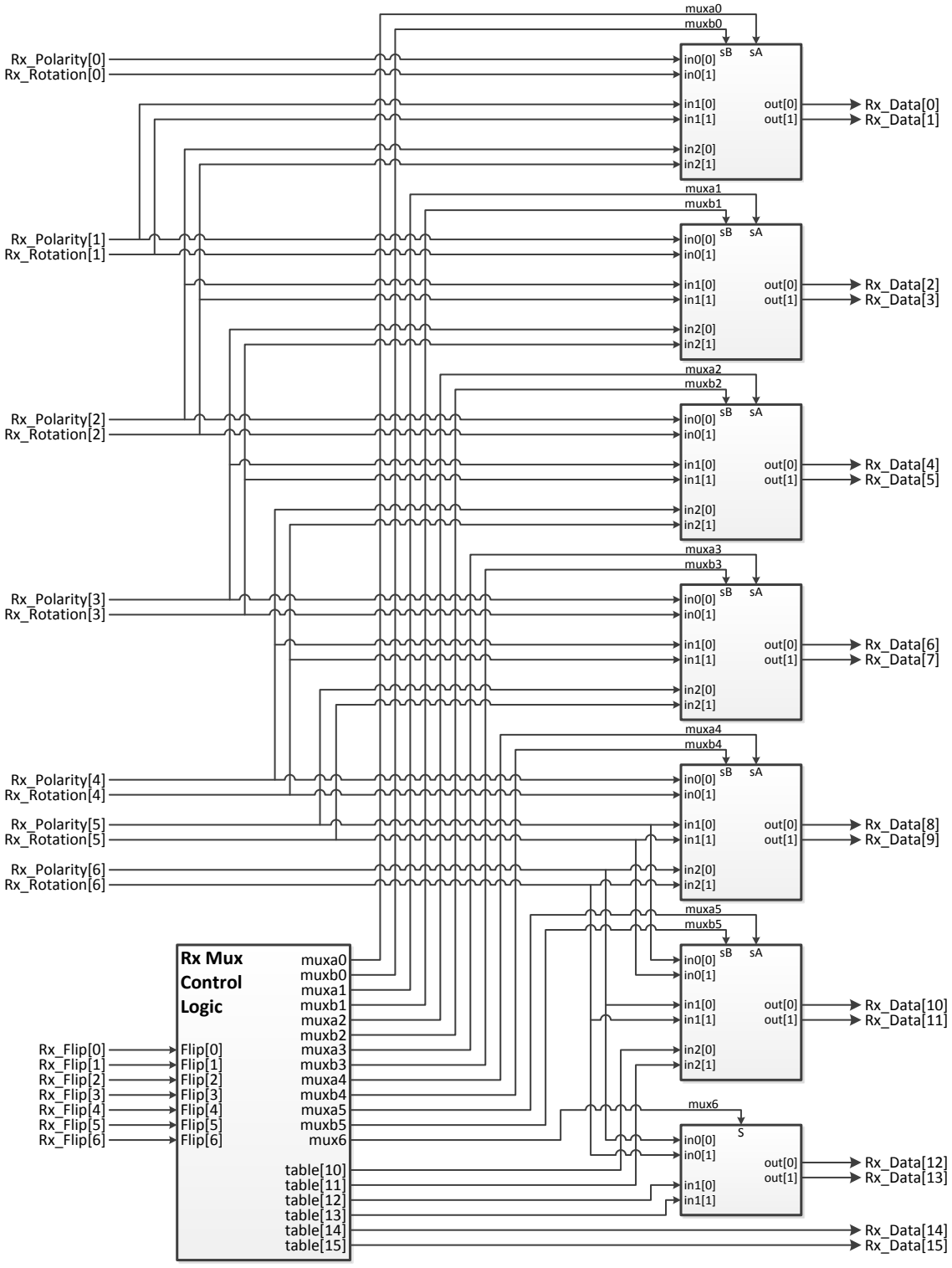

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Figure 21 Detailed Logic Diagram Example of a 7-Symbol to 16-bit Word De-Mapper

533 The logic function of the “Rx Mux Control Logic” in Figure 21 is shown below in Table 8.

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534 **Table 8 Truth Table of the “Rx Mux Control Logic” in Figure 21**

Rx_Flip[6:0]	muxa6	muxb5	muxa5	muxb4	muxa4	muxb3	muxa3	muxb2	muxa2	muxb1	muxa1	muxb0	muxa0	table[15:14]	table[13:12]	table[11:10]
0x00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x
0x01	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	x
0x02	1	0	1	0	1	0	1	0	1	0	1	0	0	1	1	x
0x04	1	0	1	0	1	0	1	0	1	0	0	0	0	1	2	x
0x08	1	0	1	0	1	0	1	0	0	0	0	0	0	1	3	x
0x10	1	0	1	0	1	0	0	0	0	0	0	0	0	2	0	x
0x20	1	0	1	0	0	0	0	0	0	0	0	0	0	2	1	x
0x40	1	0	0	0	0	0	0	0	0	0	0	0	0	2	2	x
0x03	1	1	0	1	0	1	0	1	0	1	0	1	0	2	3	0
0x05	1	1	0	1	0	1	0	1	0	1	0	0	1	2	3	1
0x09	1	1	0	1	0	1	0	1	0	0	1	0	1	2	3	2
0x11	1	1	0	1	0	1	0	0	1	0	1	0	1	2	3	3
0x21	1	1	0	1	0	0	1	0	1	0	1	0	1	3	0	0
0x41	1	1	0	0	1	0	1	0	1	0	1	0	1	3	0	1
0x06	1	1	0	1	0	1	0	1	0	1	0	0	0	3	0	2
0x0a	1	1	0	1	0	1	0	1	0	0	1	0	0	3	0	3
0x12	1	1	0	1	0	1	0	0	1	0	1	0	0	3	1	0
0x22	1	1	0	1	0	0	1	0	1	0	1	0	0	3	1	1
0x42	1	1	0	0	1	0	1	0	1	0	1	0	0	3	1	2
0x0c	1	1	0	1	0	1	0	1	0	0	0	0	0	3	1	3
0x14	1	1	0	1	0	1	0	0	1	0	0	0	0	3	2	0
0x24	1	1	0	1	0	0	1	0	1	0	0	0	0	3	2	1
0x44	1	1	0	0	1	0	1	0	1	0	0	0	0	3	2	2
0x18	1	1	0	1	0	1	0	0	0	0	0	0	0	3	2	3
0x28	1	1	0	1	0	0	1	0	0	0	0	0	0	3	3	0
0x48	1	1	0	0	1	0	1	0	0	0	0	0	0	3	3	1
0x30	1	1	0	1	0	0	0	0	0	0	0	0	0	3	3	2
0x50	1	1	0	0	1	0	0	0	0	0	0	0	0	3	3	3

6.1.4 Data Buffering

535 Data transmission takes place on protocol request. As soon as communication starts, the protocol layer at the
536 transmit side shall provide valid data as long as it does not stop its transmission request. For lanes that use
537 line coding, control symbols can also be inserted into the transmission. The protocol layer on the receive side
538 shall take the data as soon as delivered by the receiving PHY. The signaling concept, and therefore the PHY
539 protocol handshake, does not allow data throttling. Any data buffering for this purpose shall be inside the
540 protocol layer.

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6.2 Lane States and Line Levels

Transmitter functions determine the lane state by driving certain line levels. During normal operation either a HS-TX or a LP-TX is driving a lane. A HS-TX always drives the lane differentially. The three LP-TX's drive the three lines of a lane independently and single-ended. This results in six possible high-speed lane states and four possible low-power lane states: LP-000, LP-001, LP-100 and LP-111. The high-speed lane states are: +x, -x, +y, -y, +z and –z. The interpretation of low-power lane states depends on the mode of operation. The LP-Receivers shall always interpret any of the six high-speed states as LP-000.

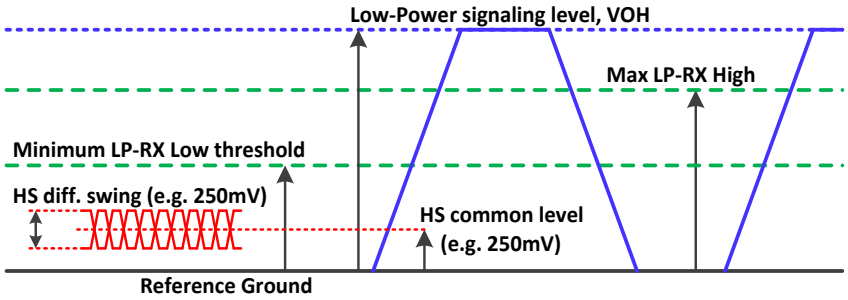

Figure 22 Line Levels

The Stop state has a very exclusive and central function. If the line levels show a Stop state for the minimum required time, the PHY state machine shall return to the Stop state regardless of the previous state. This can be in RX or TX mode depending on the most recent operating direction. Table 9 lists all the states that can appear on a lane during normal operation. Detailed specifications of electrical levels can be found in section 9.

All LP state periods shall be at least t_{LPX} in duration. State transitions shall be smooth and exclude glitch effects. A clock signal can be reconstructed by exclusive-ORing the A and C lines. Ideally, the reconstructed clock duration is at least $2 \cdot t_{LPX}$, but may have a duty cycle other than 50% due to signal slope and trip levels effects.

Table 9 Lane State Descriptions

State Code	Line Voltage Levels			High-Speed	Low-Power	
	A Line	B Line	C Line	Burst Mode	Control Mode	Escape Mode
HS_+X	HS High	HS Low	HS Mid	+x state	N/A, Note 1	N/A, Note 1
HS+-X	HS Low	HS High	HS Mid	-x state	N/A, Note 1	N/A, Note 1
HS_+Y	HS Mid	HS High	HS Low	+y state	N/A, Note 1	N/A, Note 1
HS_-Y	HS Mid	HS Low	HS High	-y state	N/A, Note 1	N/A, Note 1
HS_+Z	HS Low	HS Mid	HS High	+z state	N/A, Note 1	N/A, Note 1
HS_-Z	HS High	HS Mid	HS Low	-z state	N/A, Note 1	N/A, Note 1
LP-000	LP Low	LP Low	LP Low	N/A	Bridge	Space
LP-001	LP Low	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-100	LP High	LP Low	LP Low	N/A	LP-Rqst	Mark-1
LP-111	LP High	LP High	LP High	N/A	Stop	N/A, Note 2

Note:

1. *During high-speed transmission the low-power Receivers observe LP-000 on the lines.*
2. *If LP-111 occurs during escape mode the lane returns to Stop state (Control Mode LP-111).*
3. *Only 4 of the 8 possible low-power states are defined, because the C-PHY low-power states correspond exactly to the D-PHY low-power states so that D-PHY low-power mode can be duplicated.*

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6.3 Operating Modes: Control, High-Speed, and Escape

During normal operation a lane will be either in Control or high-speed mode. High-speed data transmission happens in bursts and starts from and ends at a Stop state (LP-111), which is by definition in Control mode. The lane is only in high-speed mode during data bursts. The sequence to enter High- Speed mode is: LP-111, LP-001, LP-000 at which point the lane remains in high-speed mode until a LP-111 is received. The escape mode can only be entered via a request within Control mode. The lane shall always exit escape mode and return to control mode after detection of a Stop state. If not in high-speed or escape mode the lane shall stay in Control mode. The Stop state serves as a general standby state and may last for any period of time > t_{LPX}. Possible events starting from the Stop state are high-speed data transmission request (LP-111, LP-001, LP-000), escape mode request (LP-111, LP-100, LP-000, LP-001, LP-000) or turnaround request (LP-111, LP-100, LP-000, LP-100, LP-000).

6.4 High-Speed Data Transmission

High-speed data transmission occurs in bursts. To aid receiver synchronization, data bursts shall be extended on the transmitter side with a Preamble and Post sequence. The effects of the high-speed transmitter shall be eliminated on the receiver side by detecting certain events designed to be detected by the receiver so it can ignore the ambiguous operating states during the mode transitions. These Preamble and Post sequences can therefore only be observed on the transmission lines.

Transmission starts from, and ends with, a Stop state. During the intermediate time between bursts a lane shall remain in the Stop state, unless a turnaround or escape request is presented on the lane. During a HS Data Burst the lane shall be in high-speed mode and will be constantly toggling per the encoding rules, thus providing high-speed data timing to the slave side.

6.4.1 Burst Payload Data

The payload data of a burst shall always represent an integer number of payload data words with a minimum length of one word. Note that for short bursts the Start and End overhead consumes much more time than the actual transfer of the payload data. There is no maximum number of words implied by the PHY. However, in the PHY there is no autonomous way of error recovery during a HS data burst. The practical symbol error rate is nearly zero. It is important to consider for every individual protocol what the best choice is for maximum burst length.

6.4.2 Start-of-Transmission

After a Transmit request, a lane leaves the Stop state and prepares for high-speed mode by means of a Start-of-Transmission (SoT) procedure. Table 10 describes the sequence of events on TX and RX side.

Table 10 Start-of-Transmission Sequence

Tx Side	Rx Side
Drives Stop state (LP-111)	Observes Stop state
Drives HS-Rqst state (LP-001) for time t_{LPX}	Observes transition from LP-111 to LP-001 on the lines
Drives Bridge state (LP-000) for time $t_{3\text{-PREPARE}}$	Observes transition from LP-001 to LP-000 on the lines, enables line termination after time $t_{3\text{-TERM-EN}}$
Enables high-speed driver and disables low-power drivers simultaneously.	
Drives Preamble sequence for time $t_{3\text{-PREAMBLE}}$	Enables HS-RX and waits for timer $t_{3\text{-SETTLE}}$ to expire in order to neglect transition effects
	Starts looking for the Sync Word sequence
Inserts the Sync Word Sequence	

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	Synchronizes upon recognition of Sync Word Sequence
Continues to transmit high-speed payload data	
	Receives payload data

6.4.3 End-of-Transmission

At the end of a Data Burst, a lane leaves high-speed Transmission mode and enters the Stop state by means of an End-of-Transmission (EoT) procedure. Table 11 shows a possible sequence of events during the EoT procedure. EoT processing may be performed by the protocol layer or by the C-PHY.

Table 11 End-of-Transmission Sequence

Tx Side	Rx Side
Completes Transmission of payload data	Receives payload data
Transmits the Post Sequence immediately after last payload data bit for time $t_{3\text{-POST}}$	Detect Post Sequence to determine last valid Data word and skip the remainder of the Post sequence
Disables the HS-TX, enables the LP-TX, and drives Stop state (LP-111) for time $t_{HS\text{-EXIT}}$	Detects the lines leaving LP-000 state and entering Stop state (LP-111) and disables Termination

6.4.4 HS Data Transmission Burst

Figure 23 shows the sequence of events during the transmission of a Data Burst. Transmission can be started and ended independently for any lane by the protocol layer. However, for most applications the lanes will start synchronously but may end at different times due to an unequal amount of transmitted bytes per lane. The handshake with the protocol layer is described in Annex A.

Beginning from the Stop state, LP-111, the signals transition to LP-001 and then LP-000 to signal that high-speed data transmission will begin soon. At the end of $t_{3\text{-PREPARE}}$ the low-power drivers are disabled and the high-speed drivers are enabled simultaneously. The TX state machine should transmit the same wire state as the first high-speed wire state at the beginning of $t_{3\text{-PREBEGIN}}$ for each Data Burst in order for the test equipment to measure $t_{3\text{-PREBEGIN}}$ value consistently. This does not correspond to any particular symbol value because there is no previous HS wire state before it. It is likely that the first few wire states of the $t_{3\text{-PREBEGIN}}$ interval will not be seen at the high-speed receiver. This is because there will be some delay for the high-speed drivers to reach their required signal levels at the beginning of $t_{3\text{-PREBEGIN}}$, and also the high-speed receivers will be enabled and at some point start producing outputs toward the end of $t_{3\text{-SETTLE}}$. The receive circuitry shall be enabled toward the end of $t_{3\text{-SETTLE}}$ when it is safe for it to reliably decode the “3” symbols during $t_{3\text{-PRE-BEGIN}}$. It is not guaranteed at exactly which symbol clock generation and symbol decoding will begin at the end of $t_{3\text{-SETTLE}}$. The $t_{3\text{-PREBEGIN}}$ field may often consist of multiple groups of seven “3” symbols to provide a sufficient number of clocks to the upper layer protocol to initialize any pipeline stages prior to receiving data. The length of $t_{3\text{-PREBEGIN}}$ is a programmable value set in the master.

The master may output a programmable sequence during $t_{3\text{-PROGSEQ}}$ of the preamble, if it is enabled using a programmable sequence enable bit such as the MSB of the control register described in section 12.5.3. The symbol values transmitted in the programmable sequence, or whether the programmable sequence is used at all, is a choice of the system designer.

Figure 23 shows examples of the preamble with and without the programmable sequence. Seven symbols of value “3” are sent during $t_{3\text{-PREEND}}$ just prior to sending the Sync Word.

The Sync Word precisely identifies the beginning of the Packet Data and also identifies the timing alignment of word boundaries in the Packet Data. The Sync Word contains a sequence of five “4” symbols which does not occur in any sequence of symbols generated by the Mapper. The Sync Word may also be transmitted later in the burst to mark the beginning of redundant Packet Headers transmitted by the upper layer protocol.

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The end of Packet Data is identified by a unique sequence of “4” symbols in $t_{3\text{-}POST}$. The receiver identifies the end of Packet Data when it detects a sequence of seven consecutive “4” symbols. The Post field may often consist of multiple groups of seven “4” symbols to provide a sufficient number of clocks to the upper layer protocol to clear out any pipeline stages that may contain received data. The length of the Post field is a programmable value set in the master, for example: the post length field of the register described in section 12.5.4.

At the end of $t_{3\text{-}POST}$ the high-speed drivers are disabled and the low-power drivers are enabled simultaneously, and all three signals of the lane are driven high together to LP-111, the Stop state.

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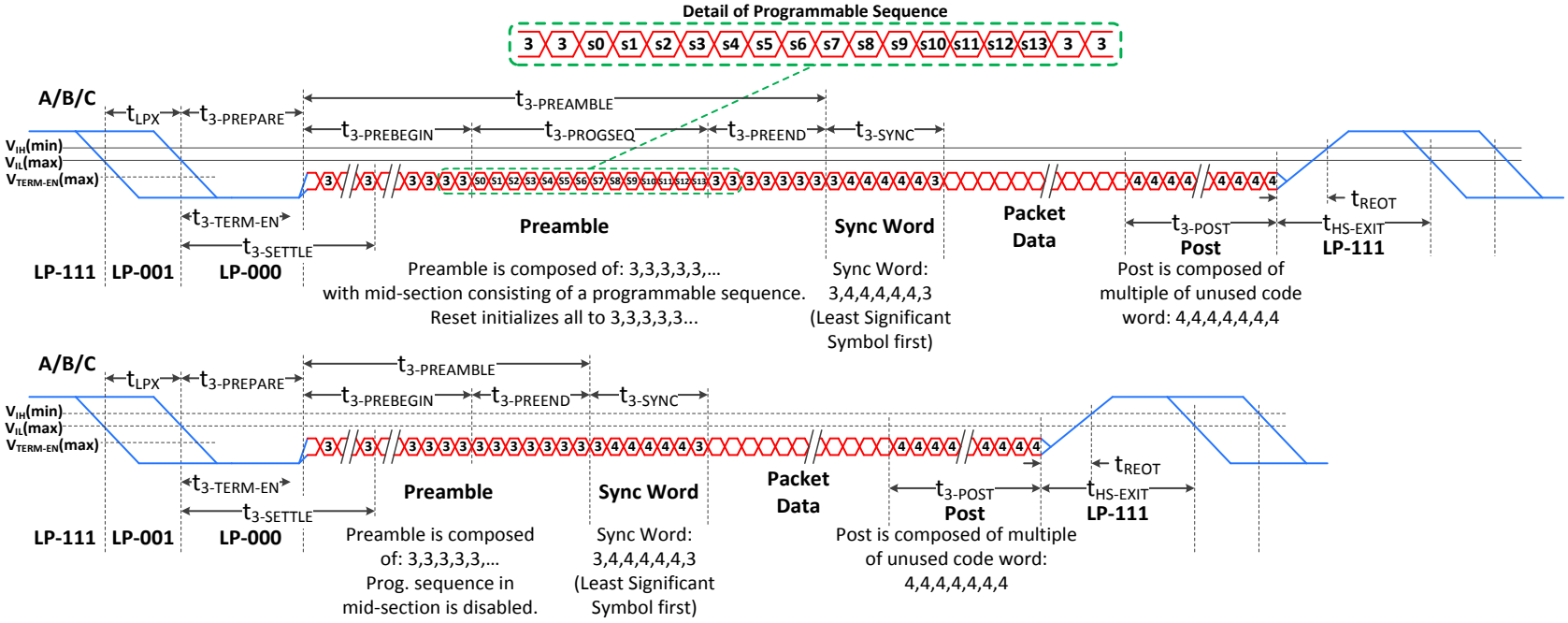

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Figure 23 High-Speed Data Transmission in Burst

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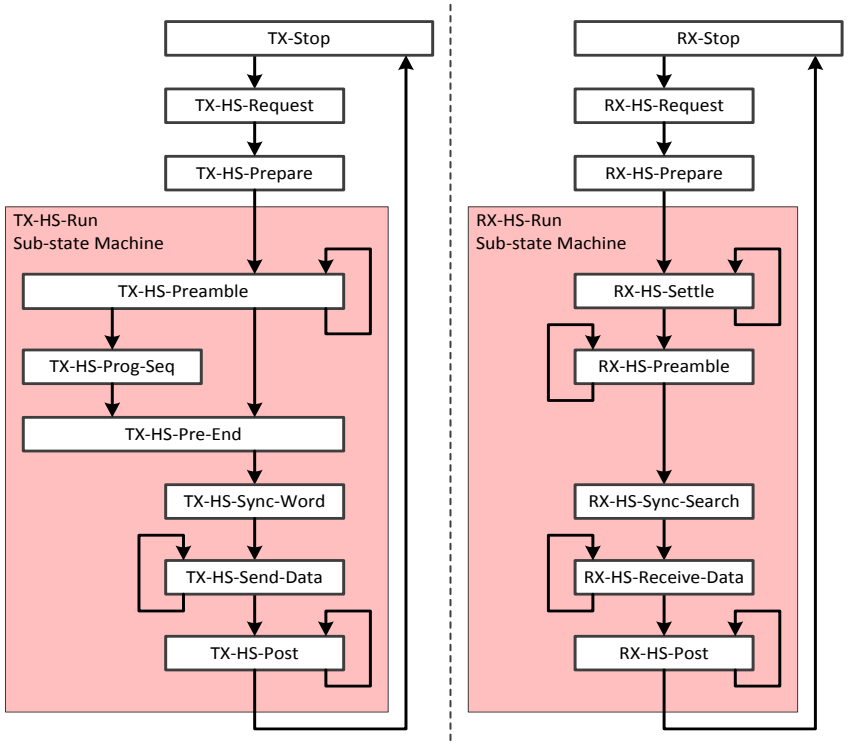

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Figure 24 TX and RX State Machines for High-Speed Data Transmission

628 **Table 12 High-Speed Data Transmission State Machine Description**

State	Line Condition or Line State	Exit State	Exit Conditions
TX-Stop	Transmit LP-111	TX-HS-Request	On request of Protocol for High-Speed Transmission
TX-HS-Request	Transmit LP-001	TX-HS-Prepare	End of timed interval t_{LPX}
TX-HS-Prepare	Transmit LP-000	TX-HS-Preamble	End of interval $t_{3\text{-}PREPARE}$
TX-HS-Preamble	Preamble 3,3,3,3…	TX-HS-Prog-Seq	End of Preamble & Prog-Seq selected
		TX-HS-Pre-End	End of Preamble & Prog-Seq not selected
		TX-HS-Preamble	Preamble words remaining count > 0
TX-HS-Prog-Seq	Prog-Seq	TX-HS-Pre-End	End of Prog-Seq
TX-HS-Pre-End	Pre-End	TX-HS-Sync-Word	End of Pre-End
TX-HS-Sync-Word	Sync Word	TX-HS-Send-Data	End of Sync-Word
TX-HS-Send-Data	Packet Data	TX-HS-Post	End of Packet Data
		TX-HS-Send-Data	Packet Data available to send
TX-HS-Post	Post	TX-Stop	Last word of Post sent

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State	Line Condition or Line State	Exit State	Exit Conditions
	4,4,4,4…	TX-HS-Post	Post words remaining count > 0

Table 13 High-Speed Data Reception State Machine Description

State	Line Condition or Line State	Exit State	Exit Conditions
RX-Stop	LP-111	RX-HS-Request	Line transition to LP-001 detected
RX-HS-Request	LP-001	RX-HS-Prepare	Line transition to LP-000 detected
PX-HS-Prepare	LP-000	RX-HS-Settle	$t_{3\text{-TERM-EN}}$ expired
RX-HS-Settle	LP-000 or Preamble 3,3,3,3…	RX-HS-Prog-Seq	$t_{3\text{-SETTLE}}$ expired & Prog-Seq selected
		RX-HS-Sync-Search	$t_{3\text{-SETTLE}}$ expired & Prog-Seq not selected
		RX-HS-Settle	$t_{3\text{-SETTLE}}$ time not expired
RX-HS-Preamble	Any part of Preamble	RX-HS-Sync-Search	High-speed circuit initialization complete
		RX-HS-Preamble	High-speed circuit initialization not complete
RX-HS-Sync-Search	Preamble or Sync Word	RX-HS-Receive-Data	Sync Word detected
RX-HS-Receive-Data	Packet Data	RX-HS-Post	First word of Post detected
		RX-HS-Receive-Data	Post not yet detected
RX-HS-Post	Post 4,4,4,4…	RX-Stop	Line transition to LP-111 detected
		RX-HS-Post	Receiving Post, waiting for LP-111

6.4.4.1 Sync Word for Packet Header Resynchronization

A given C-PHY wire state link error causes two symbol decoding errors. If the erroneous wire state also matches the wire state immediately preceding and/or following it, then the C-PHY receiver's clock and data recovery circuit will miss one or two symbol clocks, thereby causing loss of 7-symbol word alignment. If left uncorrected, this loss of word alignment will likely cause extensive de-mapping errors in the rest of the received packet payload.

In order to facilitate restoration of the transmitted word alignment, this specification defines an unmapped, 7-symbol Sync Word which may be inserted by the C-PHY transmitter at a point directed by the protocol layer via the PPI. The 7-symbol value of the Sync Word is [3444443], which is the same value used for the Sync Word as described in Section 6.4.4.

The C-PHY transmitter directly encodes the Sync Word into a series of seven wire states, bypassing the symbol mapping block which normally processes 16-bit packet payload words.

The C-PHY receiver recognizes a Sync Word by detecting any sequence of five consecutive {4} symbols immediately followed a {3} symbol at the output of the symbol decoder; i.e. detection of the least significant {3} symbol of the Sync Word is not required. Ignoring the latter symbol actually makes Sync Word detection more robust because a wire state error occurring during the most significant symbol of the 7-symbol payload word immediately preceding the Sync Word also causes corruption of the Sync Word's least significant symbol. See Figure 25 for examples of Sync Word detection.

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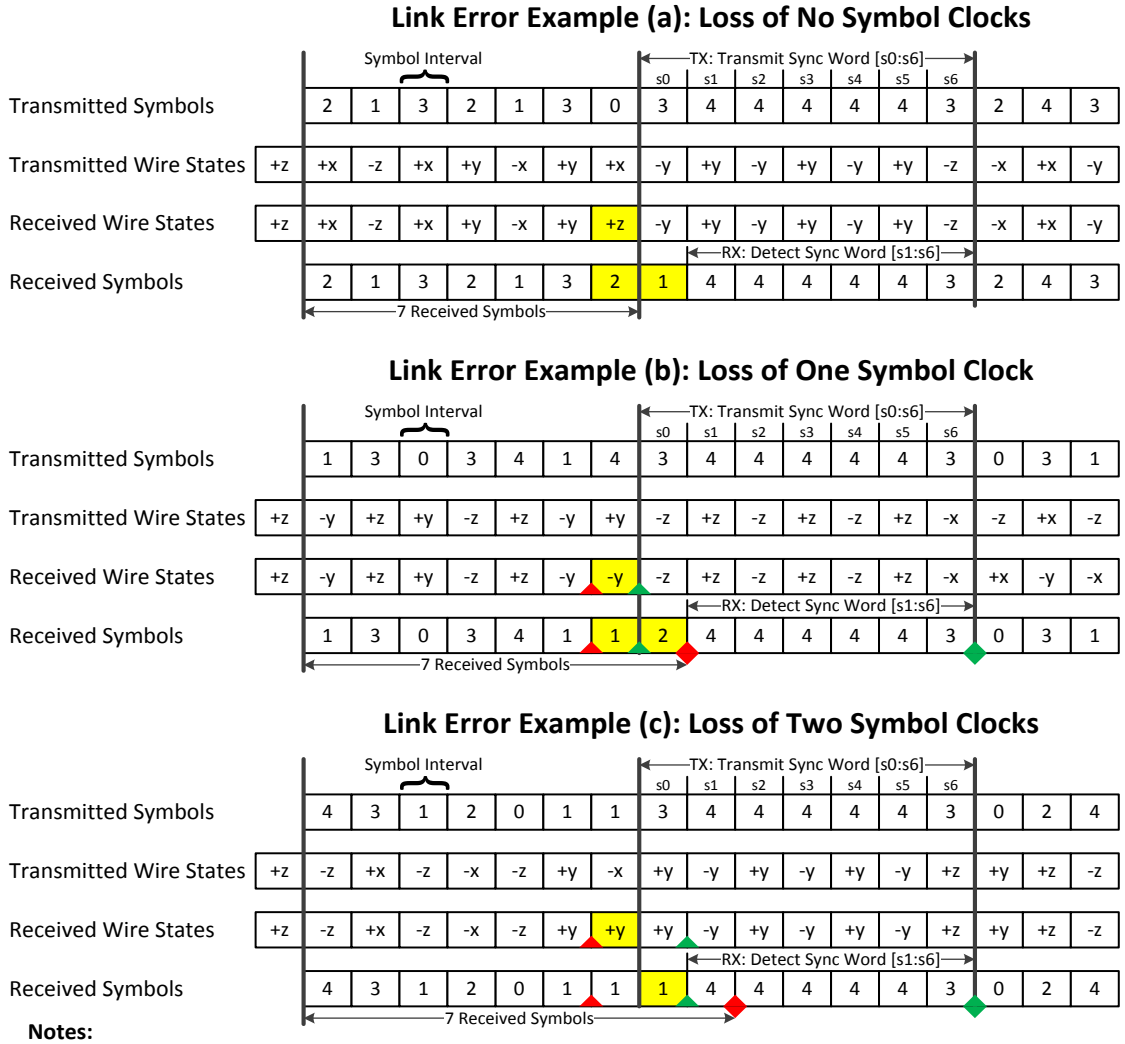
The C-PHY receiver detects the Sync Word directly at the output of the symbol decoder, prior to the symbol de-mapping block. Any 16-bit word generated by the symbol de-mapping block in response to the Sync Word shall be ignored and not passed to the receiver protocol layer.

Upon detecting the Sync Word, the C-PHY receiver resets 7-symbol word alignment to start with the first symbol immediately following Sync Word detection (i.e. the first symbol immediately following the {3} symbol). Word realignment points are shown in the Sync Word detection examples of Figure 25.

All C-PHY receivers shall support Sync Word detection and realignment. While this specification itself does not require a C-PHY transmitter to support Sync Word insertion, it may instead be required by the protocol layer specification used in conjunction with the transmitter.



Notes:

- Symbols are transmitted serially from left to right
- Wire state and symbol errors are highlighted in yellow
- ▲: point at which symbol clock is lost
- ▲: point at which symbol clock is restored
- ◆: point of incorrect word alignment
- ◆: point at which correct word alignment is restored

Figure 25 Link Error and Sync Word Detection Examples

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6.5 Bi-directional Lane Turnaround

The transmission direction of a bi-directional lane can be swapped by means of a link turnaround procedure. This procedure enables information transfer in the opposite direction of the current direction. The procedure is the same for either a change from forward-to-reverse direction or reverse-to-forward direction. Notice that master and slave side shall not be changed by turnaround. Link turnaround shall be handled completely in Control mode. Table 14 lists the sequence of events during turnaround.

Table 14 Link Turnaround Sequence

Initial TX Side = Final RX Side	Initial RX Side = Final TX Side
Drives Stop state (LP-111)	Observes Stop state
Drives LP-Rqst state (LP-100) for time t_{LPX}	Observes transition from LP-111 to LP-100 states
Drives Bridge state (LP-000) for time t_{LPX}	Observes transition from LP-100 to LP-000 states
Drives LP-100 for time t_{LPX}	Observes transition from LP-000 to LP-100 states
Drives Bridge state (LP-000) for time $t_{TA\text{-}GO}$	Observes the transition from LP-100 to Bridge state and waits for time $t_{TA\text{-}SURE}$. After correct completion of this time-out this side knows it is in control.
	Drives Bridge state (LP-000) for a period $t_{TA\text{-}GET}$
Stops driving the lines and observes the line states with its LP-RX in order to see an acknowledgement.	
	Drives LP-100 for a period t_{LPX}
Observes LP-100 on the lines, interprets this as acknowledge that the other side has indeed taken control. Waits for Stop state to complete turnaround procedure.	
	Drives Stop state (LP-111) for a period t_{LPX}
Observes transition to Stop state (LP-111) on the lines, interprets this as turnaround completion acknowledgement, switches to normal LP receive mode and waits for further actions from the other side	

Figure 26 shows the turnaround procedure graphically.

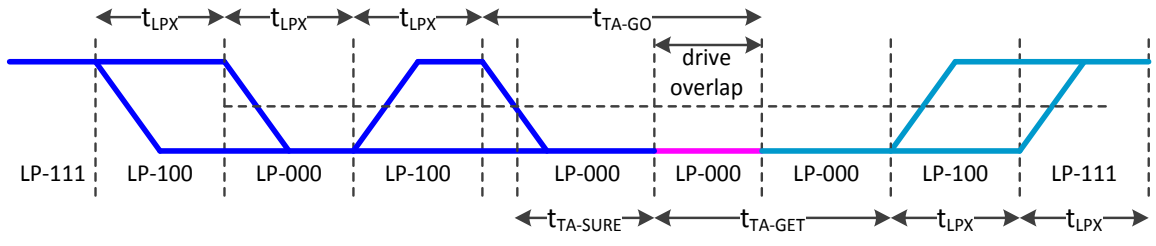

Figure 26 Turnaround Procedure

The low-power clock timing for both sides of the link does not have to be the same, but may differ. However, the ratio between the low-power state periods, t_{LPX}, is constrained to ensure proper turnaround behavior. See Table 18 for the ratio of $t_{LPX(MASTER)}$ to $t_{LPX(SLAVE)}$.

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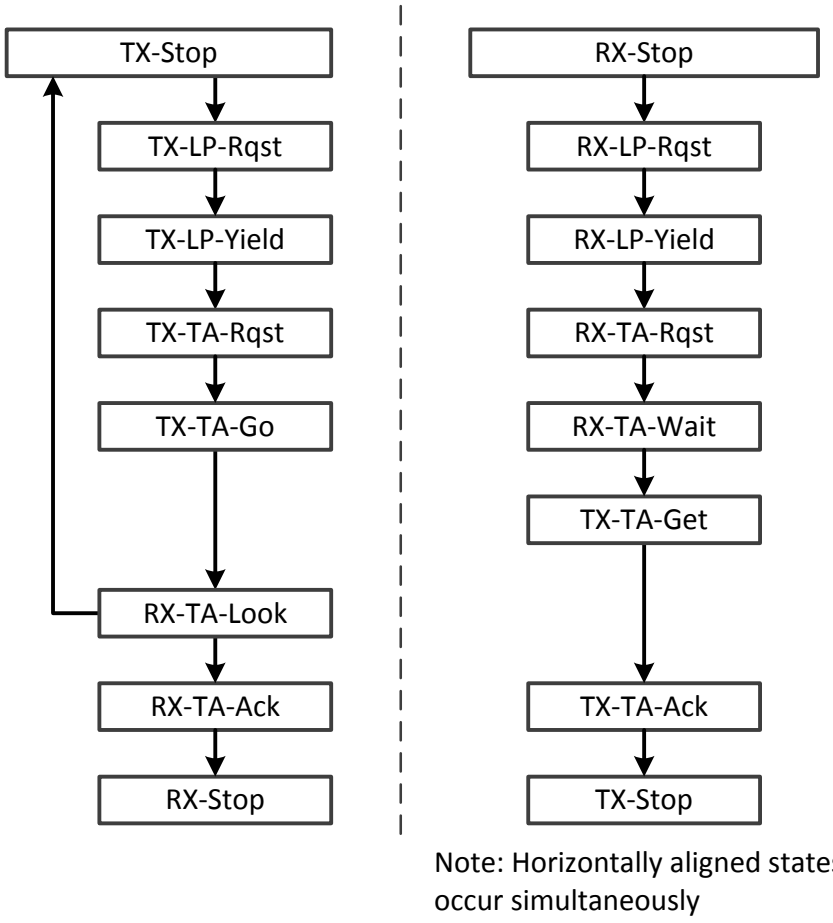
668 The turnaround procedure can be interrupted if the lane is not yet driven into TX-LP-Yield by means of
669 driving a Stop state. Driving the Stop state shall abort the turnaround procedure and return the lane to the
670 Stop state. The PHY shall ensure against interruption of the procedure after the end of TX-TA-Rqst, RX-TA-
671 Rqst, or TX-TA-GO. Once the PHY drives TX-LP-Yield, it shall not abort the turnaround procedure. The
672 protocol layer may take appropriate action if it determines an error has occurred because the turnaround
673 procedure did not complete within a certain time. See Section 7.3.5 for more details. Figure 27 shows the
674 turnaround state machine that is described in Table 15.



675

Figure 27 Turnaround State Machine

676 **Table 15 Turnaround State Machine Description**

State	Line Condition or Line State	Exit State	Exit Conditions
Any Rx state	Any Received	RX-Stop	Observe LP-111 at lines
TX-Stop	Transmit LP-111	TX-LP-Rqst	On request of protocol for turnaround
TX-LP-Rqst	Transmit LP-100	TX-LP-Yield	End of timed interval t_{LPX}
TX-LP-Yield	Transmit LP-000	TX-TA-Rqst	End of timed interval t_{LPX}
TX-TA-Rqst	Transmit LP-100	TX-TA-Go	End of timed interval t_{LPX}
TX-TA-Go	Transmit LP-000	RX-TA-Look	End of timed interval $T_{TA\text{-}GO}$
RX-TA-Look	Receive LP-000	RX-TA-Ack	Line transition to LP-100

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State	Line Condition or Line State	Exit State	Exit Conditions
RX-TA-Ack	Receive LP-100	RX-Stop	Line transition to LP-111
RX-Stop	Receive LP-111	RX-LP-Rqst	Line transition to LP-100
RX-LP-Rqst	Receive LP-100	RX-LP-Yield	Line transition to LP-000
RX-LP-Yield	Receive LP-000	RX-TA-Rqst	Line transition to LP-100
RX-TA-Rqst	Receive LP-100	RX-TA-Wait	Line transition to LP-000
RX-TA-Wait	Receive LP-000	TX-TA-Get	End of timed interval $t_{TA\text{-}SURE}$
TX-TA-Get	Transmit LP-000	TX-TA-Ack	End of timed interval $t_{TA\text{-}GET}$
TX-TA-Ack	Transmit LP-100	TX-Stop	End of timed interval t_{LPX}

Note:

During RX-TA-Look, the protocol layer may cause the PHY to transition to TX-Stop.

During high-speed data transmission, Stop states (TX-Stop, RX-Stop) have multiple valid exit states.

6.6 Escape Mode

Escape mode is a special mode of operation for lanes using Low-Power states. With this mode some additional functionality becomes available. Escape mode operation shall be supported in the forward direction and is optional in the reverse direction. If supported, escape mode does not have to include all available features.

A lane shall enter escape mode via an escape mode entry procedure (LP-111, LP-100, LP-000, LP-001, LP-000). As soon as the final Bridge state (LP-000) is observed on the lines the lane shall enter escape mode in space state (LP-000). If an LP-111 is detected at any time before the final Bridge state (LP-000), the Escape mode entry procedure shall be aborted and the receive side shall wait for, or return to, the Stop state.

Once escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. Table 16 lists all currently available escape mode commands and actions. All unassigned commands are reserved for future expansion.

The Stop state shall be used to exit escape mode and cannot occur during escape mode operation because of the spaced-one-hot encoding. The Stop state immediately returns the lane to Control mode. If the entry command doesn’t match a supported command, that particular escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state.

The PHY in escape mode shall apply spaced-one-hot bit encoding for asynchronous communication. Therefore, operation of a lane in this mode does not depend on a separate clock signal. The complete escape mode action for a Trigger-Reset command is shown in Figure 28.

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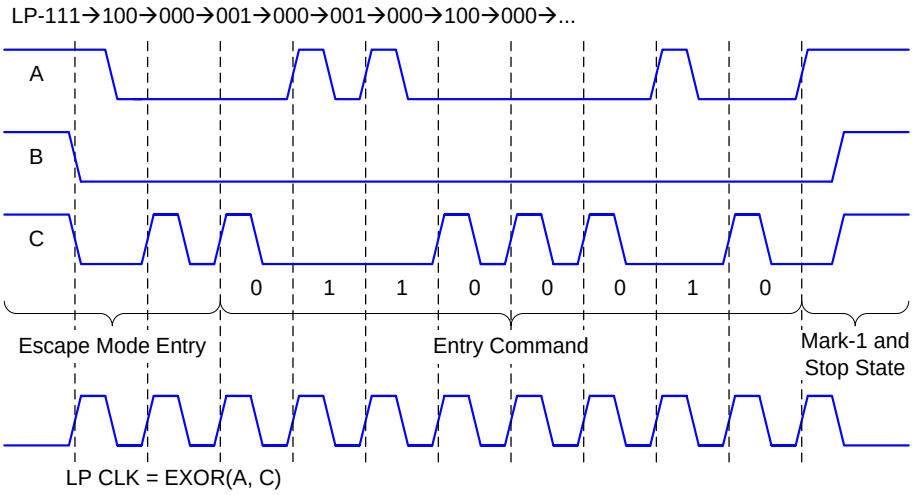

Figure 28 Trigger-Reset Command in Escape Mode

Spaced-one-hot coding means that each mark state is interleaved with a space state. Each symbol consists therefore of two parts: a one-hot phase (Mark-0 or Mark-1) and a space phase. The TX shall send Mark-0 followed by a space to transmit a ‘zero-bit’ and it shall send a Mark-1 followed by a space to transmit a ‘one-bit’. A mark that is not followed by a space does not represent a bit. The last phase before exiting escape mode with a Stop state shall be a Mark-1 state that is not part of the communicated bits, as it is not followed by a space state. The Clock can be derived from the two line signals, A and C, by means of an exclusive-OR function. The length of each individual LP state period shall be at least $t_{LPX,MIN}$.

Table 16 Escape Entry Codes

Escape Mode Action	Command Type	Entry Command Pattern (first bit transmitted to last bit transmitted)
Low-Power Data Transmission	mode	11100001
Ultra-Low Power State	mode	00011110
Undefined-1	mode	10011111
Undefined-2	mode	11011110
Reset-Trigger [Remote Application]	Trigger	01100010
Unknown-3	Trigger	01011101
Unknown-4	Trigger	00100001
Unknown-5	Trigger	10100000

6.6.1 Remote Triggers

Trigger signaling is the mechanism to send a flag to the protocol layer at the receiving side, on request of the protocol layer on the transmitting side. This can be either in the forward or reverse direction depending on the direction of operation and available escape mode functionality. Trigger signaling requires escape mode capability and at least one matching Trigger Escape entry command on both sides of the interface.

Figure 28 shows an example of an escape mode Reset-Trigger action. The lane enters escape mode via the escape mode entry procedure. If the entry command Pattern matches the Reset-Trigger Command a Trigger is flagged to the protocol layer at the receive side via the logical PPI. Any bit received after a Trigger Command but before the lines go to the Stop state shall be ignored. Therefore, dummy bytes can be concatenated in order to provide Clock information to the receive side.

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Note that Trigger signaling including Reset-Trigger is a generic messaging system. The Trigger commands do not impact the behavior of the PHY itself. Therefore, Triggers can be used for any purpose by the protocol layer.

6.6.2 Low-Power Data Transmission

If the escape mode entry procedure is followed-up by the entry command for Low-Power Data Transmission (LPDT), Data can be communicated by the protocol layer at low speed, while the lane remains in low-power mode.

Data shall be encoded on the lines with the same spaced-one-hot code as used for the entry commands. The data is self-clocked by the applied bit encoding and does not rely on a supplemental clock signal. The lane can pause while using LPDT by maintaining a space state on the lines. A Stop state on the lines stops LPDT, exits escape mode, and switches the lane to control mode. The last phase before Stop state shall be a Mark-1 state, which does not represent a data-bit. Figure 29 shows a two-byte transmission with a pause period between the two bytes.

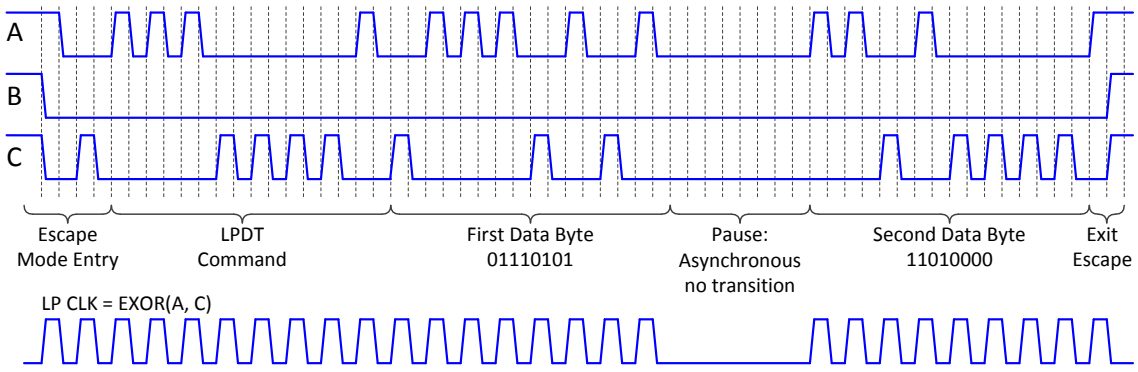

Figure 29 Two Data Byte Low-Power Data Transmission Example

Using LPDT, a low-power (bit) clock signal ($f_{MOMENTARY}$ < 20MHz) provided to the transmit side is used to transmit data. Data reception is self-timed by the bit encoding. Therefore, a variable clock rate can be allowed. At the end of LPDT the lane shall return to the Stop state.

6.6.3 Ultra-Low Power State

If the Ultra-Low Power State entry command is sent after an escape mode entry command, the lane shall enter the Ultra-Low Power State (ULPS). This command shall be flagged to the receive side protocol. During this state, the lines are in the space state (LP-000). Ultra-Low Power State is exited by means of a Mark-1 state with a length t_{WAKEUP} followed by a Stop state. Annex A describes an example of an exit procedure and a procedure to control the length of time spent in the Mark-1 state.

6.6.4 Escape Mode State Machine

The state machine for escape mode operation is shown in Figure 30 and described in Table 17.

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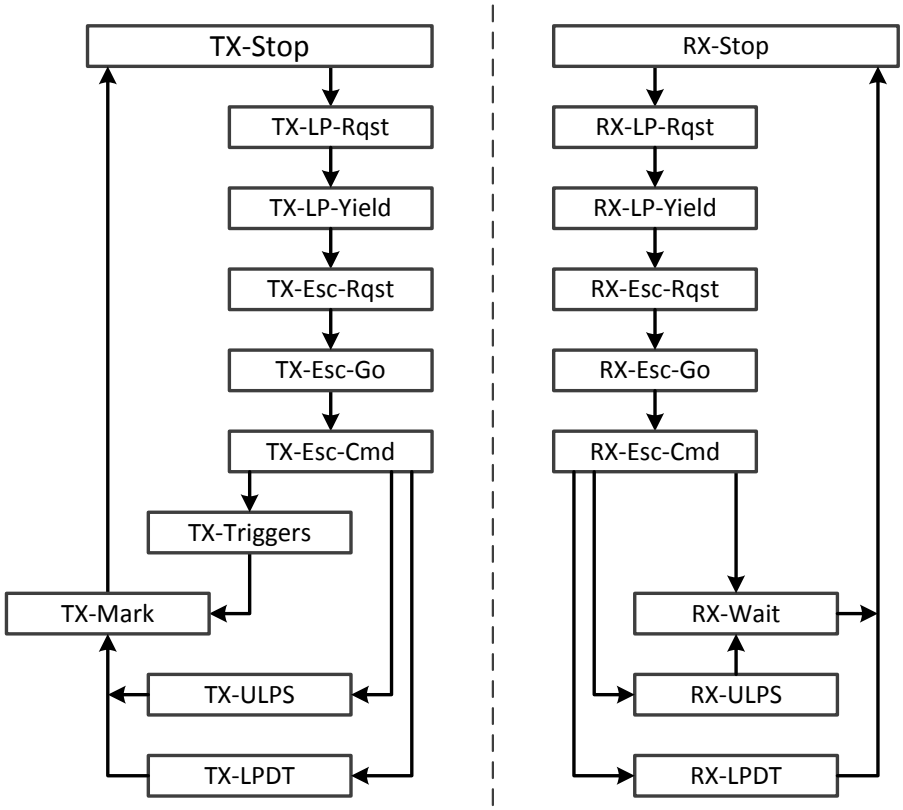

735

Figure 30 Escape Mode State Machine

736 **Table 17 Escape Mode State Machine Description**

State	Line Condition or Line State	Exit State	Exit Conditions
Any RX state	Any Received	RX-Stop	Observe LP-111 at lines
TX-Stop	Transmit LP-111	TX-LP-Rqst	On request of protocol layer for Esc mode (PPI)
TX-LP-Rqst	Transmit LP-100	TX-LP-Yield	After time t_{LPX}
TX-LP-Yield	Transmit LP-000	TX-Esc-Rqst	After time t_{LPX}
TX-Esc-Rqst	Transmit LP-001	TX-Esc-Go	After time t_{LPX}
TX-Esc-Go	Transmit LP-000	TX-Esc-Cmd	After time t_{LPX}
TX-Esc-Cmd	Transmit sequence of 8-bit (16-line-states) spaced-one-hot encoded entry command	TX-Triggers	After a Trigger Command
		TX-ULPS	After Ultra-Low Power Command
		TX-LPDT	After Low-Power Data Transmission Command
TX-Triggers	Space state or optional dummy bytes for the purpose of generating clocks	TX-Mark	Exit of the Trigger State on request of the protocol layer (via the PPI)

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State	Line Condition or Line State	Exit State	Exit Conditions
TX-ULPS	Transmit LP-000	TX-Mark	End of ULP State on request of the protocol layer (via the PPI)
TX-LPDT	Transmit serialized, spaced-one-hot encoded payload data		After last transmitted data bit
TX-Mark	Mark-1	TX-Stop	Next driven state after time t_{LPX}, or t_{WAKEUP} if leaving ULP State
RX-Stop	Receive LP-111	RX-LP-Rqst	Line transition to LP-100
RX-LP-Rqst	Receive LP-100	RX-LP-Yield	Line transition to LP-000
RX-LP-Yield	Receive LP-000	RX-Esc-Rqst	Line transition to LP-001
RX-Esc-Rqst	Receive LP-001	RX-Esc-Go	Line transition to LP-000
RX-Esc-Go	Receive LP-000	RX-Esc-Cmd	Line transition out of LP-000
RX-Esc-Cmd	Receive sequence of 8-bit (16-line-states) spaced-one-hot encoded entry Command	RX-Wait	After Trigger and Unrecognized Commands
		RX-ULPS	After Ultra-Low Power Command
		RX-LPDT	After Low-Power Data Transmission Command
RX-ULPS	Receive LP-000	RX-Wait	Line transition to LP-100
RX-LPDT	Receive serial, Spaced-One-Hot encoded payload data	RX-Stop	Line transition to LP-111 (Last state should be a Mark-1)
RX-Wait	Any, except LP-111	RX-Stop	Line transition to LP-111

Note:

During high-speed data transmission, Stop states (TX-Stop, RX-Stop) have multiple valid exit states.

6.7 (Not Used)

Note:

This section is null for the C-PHY Specification. The section heading has been retained in order to synchronize section numbering with the D-PHY Specification [MIPI01].

6.8 (Not Used)

Note:

This section is null for the C-PHY Specification. The section heading has been retained in order to synchronize section numbering with the D-PHY Specification [MIPI01].

6.9 Global Operation Timing Parameters

Table 18 lists the ranges for all timing parameters used in this section. The values in the table assume a UI variation in the range defined by ΔUI (see Table 32).

Transmitters shall support all transmitter-specific timing parameters defined in Table 18.

Receivers shall support all Receiver-specific timing parameters in defined in Table 18.

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Also note that while corresponding receiver tolerances are not defined for every transmitter-specific parameter, receivers shall also support reception of all allowed conformant values for all transmitter specific timing parameters in Table 18 for all HS UI values up to, and including, the maximum supported HS symbol rate specified in the receiver's datasheet.

Table 18 Global Operation Timing Parameters

Parameter	Description	Min	Max	Unit	Notes
$t_{3\text{-PREPARE}}$	Time that the transmitter drives the 3-wire LP-000 line state immediately before the HS_+x line state starting the HS transmission.	38	95	ns	2
$t_{3\text{-TERM-EN}}$	Time for the slave to enable the HS line termination, starting from the time point when the A, B and C wire cross V_{IL_MAX}	Note 5	38	ns	3
$t_{3\text{-SETTLE}}$	Time interval during which the HS receiver should ignore any HS transitions on the lane, starting from the beginning of $t_{3\text{-PREPARE}}$	95	300	ns	3,4
$t_{3\text{-HS-EXIT}}$	Time that the transmitter drives LP-111 following a HS burst.	100		ns	2
t_{LPX}	Transmitted length of any low-power state period	50		ns	1, 2
t_{INIT}	See Section 6.11.	100		µs	2
Ratio t_{LPX}	Ratio of $t_{LPX(MASTER)}/t_{LPX(SLAVE)}$ between master and slave side	2/3		3/2	
$t_{TA\text{-GET}}$	Time that the new transmitter drives the Bridge state (LP-000) after accepting control during a link turnaround.	$5\cdot t_{LPX}$			2
$t_{TA\text{-GO}}$	Time that the transmitter drives the Bridge state (LP-000) before releasing control during a link turnaround.	$4\cdot t_{LPX}$			2
$t_{TA\text{-SURE}}$	Time that the new transmitter waits after the LP-100 state before transmitting the Bridge state (LP-000) during a link turnaround.	t_{LPX}	$2\cdot t_{LPX}$	ns	2
t_{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1		ms	2

Note:

1. *t_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.*
2. *Transmitter-specific parameter.*
3. *Receiver-specific parameter.*
4. *The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.*
5. *As specified in Section 9.2.1, the receiver termination impedances shall not be enabled until the single-ended voltages on all of A, B and C fall below $V_{TERM\text{-}EN}$.*

$t_{3\text{-SETTLE}} > t_{3\text{-PREPARE}}$ $t_{3\text{-PROGSEQ}}$ = 14 UI or 0 UI

$t_{3\text{-SETTLE}} < t_{3\text{-PREPARE}} + t_{3\text{-PREAMBLE}}$ $t_{3\text{-PREEND}}$ = 7 UI

$t_{3\text{-PREAMBLE}} = t_{3\text{-PREBEGIN}} + t_{3\text{-PROGSEQ}} + t_{3\text{-PREEND}}$ $t_{3\text{-SYNC}}$ = 7 UI

$t_{3\text{-PREBEGIN}}$ should be adjustable from 7 UI minimum to 448 UI maximum in increments of 7 UI. An example method to specify the length of $t_{3\text{-PREBEGIN}}$ is provided in section 12.5.3. $t_{3\text{-POST}}$ should be adjustable from 7 UI minimum to 224 UI maximum in increments of 7 UI. An example method to specify the length of $t_{3\text{-POST}}$ is provided in section 12.5.4.

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6.10 System Power States

Each lane within a PHY configuration, that is powered and enabled, has potentially two different power consumption levels: high-speed transmission mode and Ultra-Low Power State. For details on Ultra-Low Power State see Section 6.6.3. The transition between these modes shall be handled by the PHY.

6.11 Initialization

After power-up, the slave side PHY shall be initialized when the master PHY drives a Stop state (LP-111) for a period longer than t_{INIT}. The first Stop state longer than the specified t_{INIT} is called the initialization period. The master PHY itself shall be initialized by a system or protocol layer input signal (PPI). The master side shall ensure that a Stop state longer than t_{INIT} does not occur on the lines before the master is initialized. The slave side shall ignore all line states during an interval of unspecified length prior to the initialization period. In multi-lane configurations, all lanes shall be initialized simultaneously.

Note that t_{INIT} is considered a protocol-dependent parameter, and thus the exact requirements for $t_{INIT,MASTER}$ and $t_{INIT,SLAVE}$ (transmitter and receiver initialization Stop state lengths, respectively,) are defined by the protocol layer specification and are outside the scope of this document. However, the C-PHY specification does place a minimum bound on the lengths of $t_{INIT,MASTER}$ and $t_{INIT,SLAVE}$, which each shall be no less than 100 µs. A protocol layer specification using the C-PHY specification may specify any values greater than this limit, for example, $t_{INIT,MASTER} \geq 1$ ms and $t_{INIT,SLAVE} = 500$ to 800 µs.

Table 19 Initialization States

State	Entry Conditions	Exit State	Exit Conditions	Line Levels
Master Off	Power-down	Master Initialization	Power-up	Any LP level except Stop states for periods>100µs
Master Init	Power-up or protocol request	TX-stop	A first Stop state for a period longer than $t_{INIT,MASTER}$ as specified by the protocol layer	Any LP signaling sequence that ends with a long initialization Stop state
Slave Off	Power-down	Any LP state	Power-up	Any
Slave Init	Power-up or protocol layer request	RX-Stop	Observe Stop state at the inputs for a period $t_{INIT,SLAVE}$ as specified by the protocol layer	Any LP signaling sequence which ends with the first long initialization stop period

6.12 Calibration

There is no explicit calibration required by the C-PHY specification. Any detail regarding calibration is outside the scope of this specification.

6.13 Global Operation Flow Diagram

All previously described aspects of operation, either including or excluding optional parts, are contained in lane modules. Figure 31 shows the operational flow diagram for a lane module. Within both TX and RX four main processes can be distinguished: High-Speed Transmission, escape mode, turnaround, and initialization.

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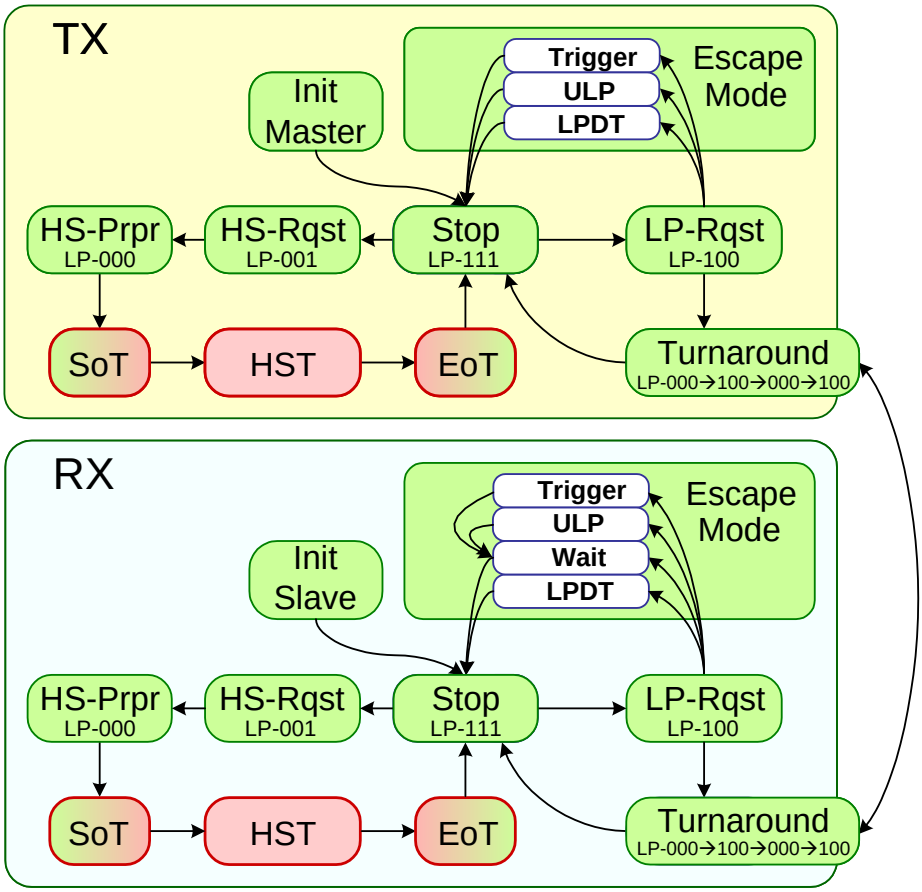

Figure 31 Lane Module State Diagram

6.14 Data Rate Dependent Parameters (informative)

The high-speed data transfer rate of the C-PHY may be programmable to values determined by a particular implementation. Any individual data transfer between SoT and EoT sequences must take place at a given, fixed rate. However, reprogramming the data rate of the C-PHY high-speed transfer is allowed at initialization, before starting the exit from ULP state or in Stop state. The method of data rate reprogramming is out of the scope of this document.

6.14.1 Parameters Containing Only UI Values

Certain parameters are specified as a number of UI intervals. Often this shall be a multiple of 7 UI which simplifies the implementation of both the master and slave because decisions regarding the transmission of fields can take place at a word clock interval. Parameters specified in units of UI are:

- $t_{3\text{-PREBEGIN}}$ – the length of the first part of the Preamble
- $t_{3\text{-PROGSEQ}}$ – the length of the programmable sequence section of the preamble
- $t_{3\text{-PREEND}}$ – the length of the end of the preamble
- $t_{3\text{-PREAMBLE}}$ – the length of the entire preamble including $t_{3\text{-BEGIN}}$, $t_{3\text{-PROGSEQ}}$ and $t_{3\text{-PREEND}}$
- $t_{3\text{-SYNC}}$ – the length of the Sync Word
- $t_{3\text{-POST}}$ – the length of the Post sequence at the end of the burst

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6.14.2 Parameters Containing Time and UI values

There are no parameters specified as the sum of an explicit time and a number of UI.

6.14.3 Parameters Containing Only Time Values

Several parameters are specified only as explicit time values. These explicit time values are typically derived from the time needed to charge and discharge the interconnect and are, therefore, not data rate dependent. It is conceivable to use an analog timer or counter clocked by the UI to ensure the implementation satisfies these parameters. However, if these time values are implemented by counting UI only, then the count value is a function of the data rate and, therefore, must be changed when the data rate is changed.

The following parameters are based on time values alone:

- $t_{3\text{-PREPARE}}$
- $t_{3\text{-TERM-EN}}$
- $t_{3\text{-SETTLE}}$
- $t_{3\text{-HS-EXIT}}$

6.14.4 Parameters Containing Only Time Values That Are Not Data Rate Dependent

The remaining parameters in Table 18 shall be complied with even when the high-speed clock is off. These parameters include low-power and initialization state durations and LP signaling intervals. Though these parameters are not HS data rate dependent, some implementations of D-PHY may need to adjust these values when the data rate is changed.

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7 Fault Detection

There are three different mechanisms to detect malfunctioning of the link. Bus contention and error detection functions are contained within the C-PHY. These functions should detect many typical faults. However, some faults cannot be detected within the C-PHY and require a protocol-level solution. Therefore, the third detection mechanism is a set of application specific watchdog timers.

7.1 Contention Detection

If a bi-directional lane module and a unidirectional module are combined in one lane, only unidirectional functionality is available. Because in this case the additional functionality of one bi-directional PHY Module cannot be reliably controlled from the limited functionality PHY side, the bi-directional features of the bi-directional Module shall be safely disabled. Otherwise in some cases deadlock may occur which can only be resolved with a system power-down and re-initialization procedure.

During normal operation one and only one side of a link shall drive a lane at any given time except for certain transition periods. Due to errors or system malfunction a lane may end up in an undesirable state, where the lane is driven from two sides or not driven at all. This condition eventually results in a state conflict and is called Contention.

All lane modules with LP bi-directionality shall include contention detection functions to detect the following contention conditions:

- Modules on both sides of the same line drive opposite LP levels against each other. In this case, the line voltage will settle to some value between $V_{OL,MIN}$ and $V_{OH,MAX}$. Because V_{IL} is greater than V_{IHCD}, the settled value will always be either higher than V_{IHCD}, lower than V_{IL}, or both. Refer to Section 9.3. This ensures that at least one side of the link, possibly both, will detect the fault condition.
- The Module at one side drives LP-high while the other side drives HS-low on the same line. In this case, the line voltage will settle to a value lower than V_{IL}. The contention shall be detected at the side that is transmitting the LP-high.

The first condition can be detected by the combination of LP-CD and LP-RX functions. The LP-RX function should be able to detect the second contention condition. Details on the LP-CD and LP-RX electrical specifications can be found in Section 9. Except when the previous state was TX-ULPS, contention shall be checked before the transition to a new state. Contention detection in ULPS is not required because the bit period is not defined and a clock might not be available.

After contention has been detected, the protocol layer shall take proper measures to resolve the situation.

7.2 Sequence Error Detection

If for any reason the lane signal is corrupted the receiving PHY may detect signal sequence errors. Errors detected inside the PHY may be communicated to the protocol layer via the PPI. This kind of error detection is optional, but strongly recommended as it enhances reliability. The following sequence errors can be distinguished:

- SoT Error
- SoT Sync Error
- EoT Sync Error
- Escape Entry Command Error
- LP Transmission Sync Error
- False Control Error

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7.2.1 SoT Error

The Sync Word for Start of High-Speed Transmission is fault tolerant of errors in the least significant symbol, as described in Section 6.4.4.1. Therefore, the Sync Word is usable to establish word boundary synchronization and identification of the start of data, but confidence in the payload data is lower. If this situation occurs, an SoT Error is indicated.

7.2.2 SoT Sync Error

If the Sync Word is corrupted in a way that proper synchronization cannot be expected, a SoT Sync Error is indicated.

7.2.3 EoT Sync Error

The EoT Sync Error is not applicable to C-PHY. Redundant Post words follow the packet data, and an error in the misalignment of data words is easily detected by the upper layer protocol.

7.2.4 Escape Mode Entry Command Error

If the receiving lane module does not recognize the received entry command for escape mode an escape mode entry command error is indicated.

7.2.5 LP Transmission Sync Error

At the end of a low-power data transmission procedure, if data is not synchronized to a Byte boundary an Escape Sync Error signal is indicated.

7.2.6 False Control Error

If a LP-Rqst (LP-100) is not followed by the remainder of a valid escape or turnaround sequence, a False Control Error is indicated. This error is also indicated if a HS-Rqst (LP-001) is not correctly followed by a Bridge State (LP-000).

7.3 Protocol Watchdog Timers (informative)

It is not possible for the PHY to detect all fault cases. Therefore, additional protocol-level time-out mechanisms are necessary in order to limit the maximum duration of certain modes and states.

7.3.1 HS RX Timeout

In HS RX mode if no EoT is received within a certain period the protocol layer should time-out. The timeout period can be protocol specific.

7.3.2 HS TX Timeout

The maximum transmission length in HS TX is bounded. The timeout period is protocol specific.

7.3.3 Escape Mode Timeout

A device may timeout during escape mode. The timeout should be greater than the escape mode Silence Limit of the other device. The timeout period is protocol specific.

7.3.4 Escape Mode Silence Timeout

A device may have a bounded length for LP TX-000 during escape mode, after which the other device may timeout. The timeout period is protocol specific. For example, a display module should have an escape mode Silence Limit, after which the host processor can timeout.

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7.3.5 Turnaround Errors

A turnaround procedure always starts from a Stop state. The procedure begins with a sequence of Low- Power States ending with a Bridge State (LP-000) during which drive sides are swapped. The procedure is finalized by the response including a Turn State followed by a Stop state driven from the other side. If the actual sequence of events violates the normal turnaround procedure a "False Control Error" may be flagged to the protocol layer. See Section 7.2.6. The Turn State response serves as an acknowledgement for the correctly completed turnaround procedure. If no acknowledgement is observed within a certain time period the protocol layer should time-out and take appropriate action. This period should be larger than the maximum possible turnaround time for a particular system. There is no time-out for this condition in the PHY.

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8 Interconnect and Lane Configuration

The interconnect between transmitter and receiver carries all signals used in C-PHY communication. This includes both high-speed, low voltage signaling I/O technology and low speed, low power signaling for control functions. For this reason, the physical connection should be implemented by means of point-to-point transmission lines referenced to ground. The total interconnect may consist of several cascaded transmission line segments, such as, printed circuit boards, flex-foils, and cable connections.

Figure 32 Point-to-point Interconnect

8.1 Lane configuration

The complete physical connection of a lane consists of a transmitter (TX), and/or receiver (RX) at each side, with some Transmission-Line-Interconnect-Structure (TLIS) in between. The overall lane performance is therefore determined by the combination of these three elements. The split between these elements is defined to be on the module (IC) pins. This section defines both the required performance of the Transmission-Line-Interconnect-Structure for the signal routing as well as the I/O-cell Reflection properties of TX and RX. This way the correct overall operation of the lane can be ensured.

With respect to physical dimensions, the Transmission-Line-Interconnect-Structure will typically be the largest part. Besides printed circuit board and flex-foil traces, this may also include elements such as vias and connectors.

8.2 Boundary Conditions

The reference characteristic impedance level is 100 Ohm differential, 50 Ohm single-ended per line, and 25 Ohm common-mode for any two lines together. The 50 Ohm impedance level for single-ended operation is also convenient for test and characterization purposes.

This typical impedance level is required for all three parts of the lane: TX, TLIS, and RX. The tolerances for characteristic impedances of the interconnect and the tolerance on line termination impedances for TX and RX are specified by means of S-parameter templates over the whole operating frequency range.

The differential channel is also used for LP single-ended signaling. Therefore, it is strongly recommended to apply only very loosely coupled differential transmission lines.

The flight time for signals across the interconnect should not exceed two nanoseconds.

8.3 Definitions

The frequency ‘fh’ is the highest fundamental frequency for data transmission and is equal to $1/(2*UI_{INST,MIN})$. Implementers should specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a high-speed data transfer for a given implementation.

The frequency ‘fh_{MAX}’ is a device specification and indicates the maximum supported fh for a particular device.

The frequency ‘$f_{LP,MAX}$’ is the maximum toggle frequency for low-power mode.

RF interference frequencies are denoted by ‘f_{INT}’, where $f_{INT,MIN}$ defines the lower bound for the band of relevant RF interferers. The frequency f_{MAX} is defined by

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914 $$f_{MAX} = \frac{3}{4} \cdot \frac{1}{UI_{INST,MIN}}$$

8.4 S-parameter Specifications

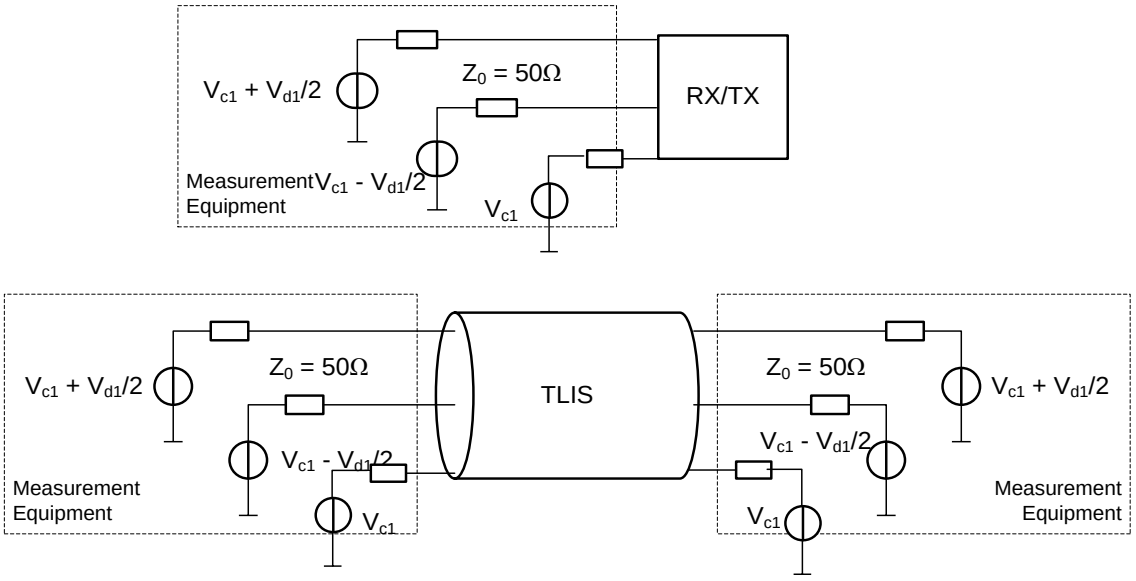
915 The required performance of the physical connection is specified by means of S-parameter requirements for
916 TX, TLIS, and RX, for TLIS by mixed-mode, 4-port parameters, and for RX and TX by mixed-mode,
917 reflection (return loss) parameters. The S-parameter limits are defined over the whole operating frequency
918 range by means of templates.

919 The differential transmission properties are most relevant and therefore this specification uses mixed-mode
920 parameters. As the performance needs depend on the targeted bit rates, most S-parameter requirements are
921 specified on a normalized frequency axis with respect to bit rate. Only the parameters that are important for
922 the suppression of external (RF) interference are specified on an absolute frequency scale. This scale extends
923 up to f_{MAX}. Beyond this frequency the circuitry itself should suppress the high-frequency interference signals
924 sufficiently.

925 Only the overall performance of the TLIS and the maximum reflection of RX and TX are specified. This
926 fully specifies the signal behavior at the RX/TX-module pins. The subdivision of losses, reflections and
927 mode-conversion budget to individual physical fractions of the TLIS is left to the system designer. Annex B
928 includes some rules of thumb for system design and signal routing guidelines.

8.5 Characterization Conditions

929 All S-parameter definitions are based on a 50 Ω impedance reference level. The characterization can be done
930 with a measurement system, as shown in Figure 33.



931

Figure 33 Set-up for S-parameter Characterization of RX, TX and TLIS

8.6 Interconnect Specifications

932 The Transmission-Line Signal-Routing (TLSR) is specified by means of mixed-mode 4-port S-parameter
933 behavior templates over the frequency range. This includes the differential and common-mode, insertion and
934 return losses, and mode-conversion limitations.

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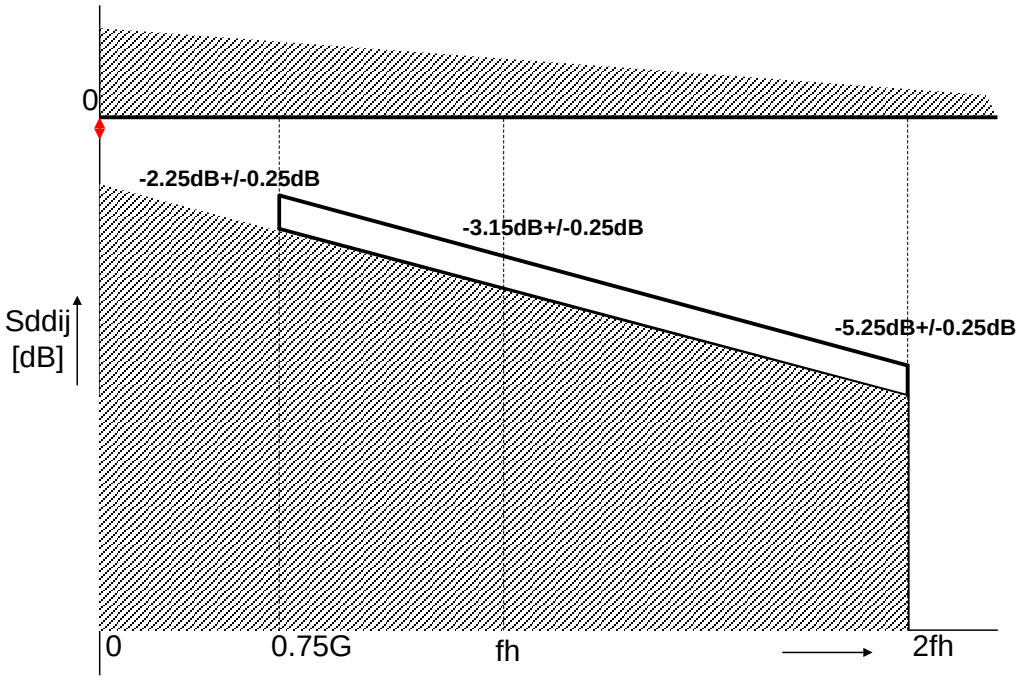
8.6.1 Differential Characteristics

The differential transfer behavior (insertion loss) of the TLIS should meet the Sdd21 and Sdd12 template shown in Figure 34, where i ≠ j. This applies to all the three differential pairs AB, BC & CA.



	0.75G	fh	2fh
Sddij, dB	-2.25 +/-0.25dB	-3.15+/-0.25dB	-5.25 +/-0.25dB

Figure 34 Template for Differential Insertion Losses

The differential reflection for both ports of the TLIS is specified by Sdd11 and Sdd22, and should be less than -12dB from 0 to 2fh. Not meeting the differential reflection coefficients might impact interoperability and operation.

8.6.2 Common-mode Characteristics

The common-mode insertion loss is implicitly specified by means of the differential insertion loss and the intra-lane cross coupling. The requirements for common-mode insertion loss are therefore equal to the differential requirements.

The common-mode reflection coefficients Scc11 and Scc22 should both be below –12 dB at frequencies up to 2fh. Not meeting the common-mode reflection coefficients might impact interoperability and operation.

8.6.3 Intra-Lane Cross-Coupling

The two lines applied as a differential pair during HS transmission are also used individually for single-ended signaling during low-power mode. Therefore, the coupling between the two wires should be restricted in order to limit single-ended cross coupling. The coupling between the two wires is defined as the difference of the S-parameters Scc21 and Sdd21 or Scc12 and Sdd12. In either case, the difference should not exceed –35 dB for frequencies up to 2fh.

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8.6.4 Mode-Conversion Limits

All mixed-mode, 4-port S-parameters for differential to common-mode conversion, and vice-versa, should not exceed –29 dB for frequencies below fh. This includes Sdc12, Scd21, Scd12, Sdc21, Scd11, Sdc11, Scd22, and Sdc22.

8.6.5 Inter-Lane Static Skew

The difference in signal delay between any two Lanes should be less than 160ps for all frequencies up to, and including, fh.

8.7 Driver and Receiver Characteristics

Besides the TLIS the lane consists of two RX-TX modules, one at each side. This paragraph specifies the reflection behavior (return loss) of these RX-TX modules in HS-mode. This applies to all the three differential pairs AB, BC & CA. The signaling characteristics of all possible functional blocks inside the RX-TX modules can be found in Section 9. The low-frequency impedance range for line terminations at Transmitter and Receiver is 80-120Ohm.

The figures in this section apply to the speed ranges:

1. >1.5Gsps and C_{PAD_TX} = 3pF
2. ≤1.5Gsps and C_{PAD}=5pF

8.7.1 Differential Characteristics

The differential reflection of a lane module in high-speed RX mode should conform to the limits specified by the template shown in Figure 35.

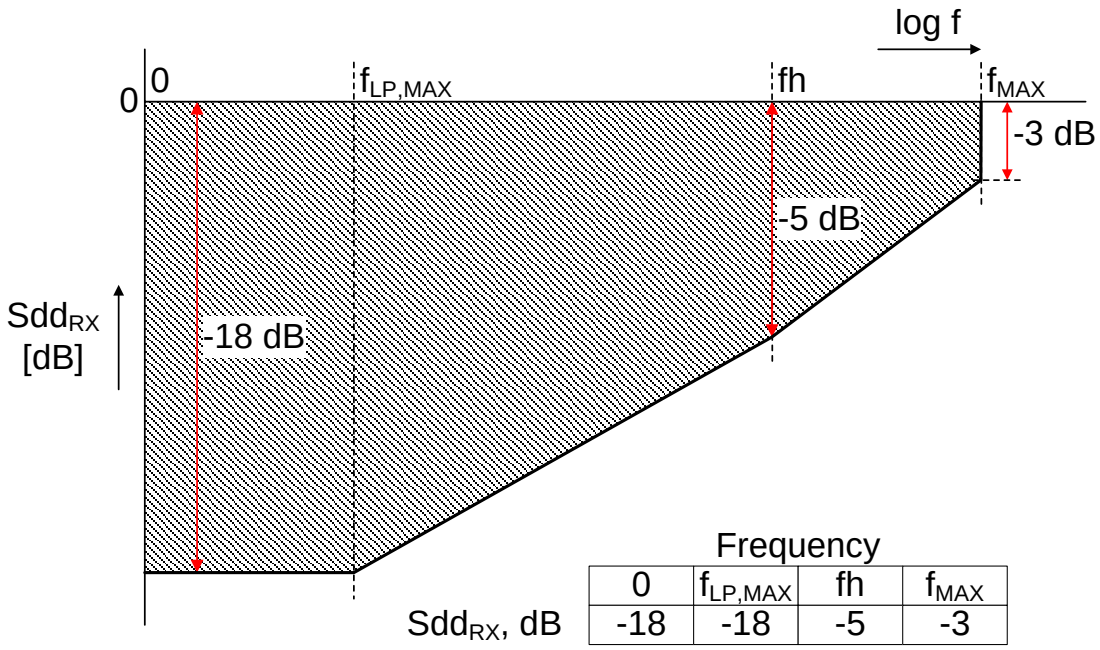

Figure 35 Differential Reflection Template for Lane Module Receivers

The differential reflection of a lane module in high-speed TX mode should conform to the limits specified by the template shown in Figure 36.

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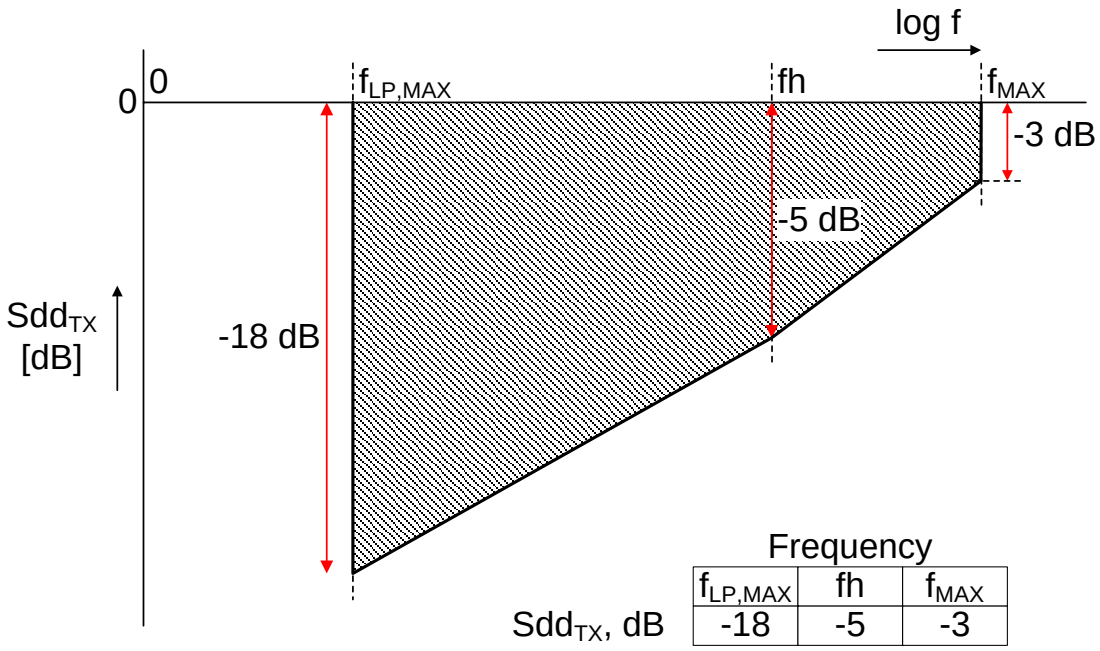

Figure 36 Differential Reflection Template for Lane Module Transmitters

8.7.2 Common-Mode Characteristics

The common-mode return loss specification is different for a high-speed TX and RX mode, because the RX is not DC terminated to ground. The common mode reflection of a lane module in high-speed TX mode should be less than -3dB from $f_{LP,MAX}$ up to f_{MAX}. The common mode reflection of a lane module in high-speed RX mode should conform to the limits specified by the template shown in Figure 37. Assuming a high DC common-mode impedance implies a sufficiently large capacitor at the termination center tap. The minimum value allows integration. While the common-mode termination is especially important for reduced influence of RF interferers the RX requirement limits reflection for the most relevant frequency band.

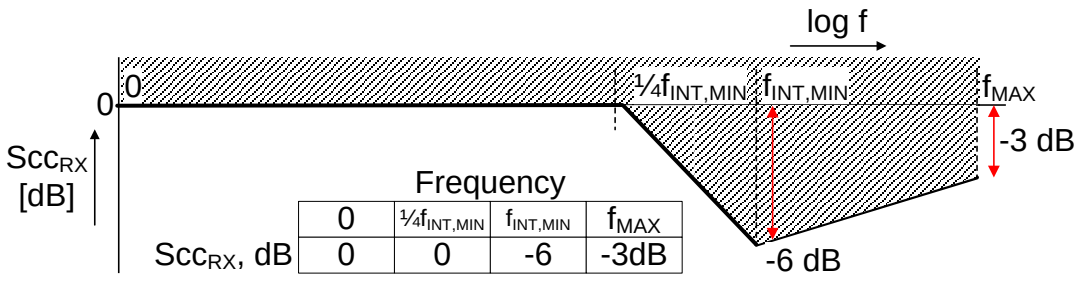

Figure 37 Template for RX Common-Mode Return Loss

8.7.3 Mode-Conversion Limits

The differential to common-mode conversion limits of TX and RX should be -26dB up to f_{MAX}.

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9 Electrical Characteristics

A PHY may contain the following electrical functions: a high-speed Transmitter (HS-TX), a high-speed Receiver (HS-RX), a low-power transmitter (LP-TX), a low-power receiver (LP-RX), and a low-power contention detector (LP-CD). A PHY does not need to contain all electrical functions, only the functions that are required for a particular PHY configuration. The required functions for each configuration are specified in Section 5. All electrical functions included in any PHY shall meet the specifications in this section. Figure 38 shows the complete set of electrical functions required for a fully featured PHY transceiver.

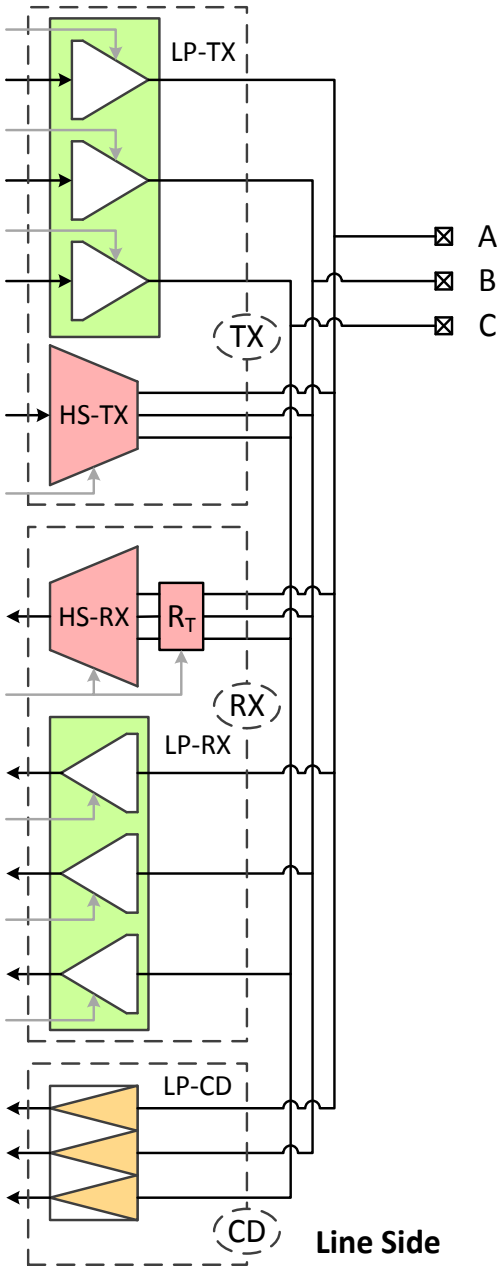

Figure 38 Electrical Functions of a Fully Featured C-PHY Transceiver

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The HS transmitter and HS receiver are used for the transmission of the HS data signals. The HS transmitter and receiver utilize low-voltage C-PHY signaling for signal transmission. The HS receiver contains a switchable star termination.

The LP transmitter and LP receiver serve as a low power signaling mechanism. The LP transmitter is a push-pull driver and the LP receiver is an un-terminated, single-ended receiver.

The signal levels are different for high-speed mode compared to single-ended low-power mode. Figure 39 shows both the high-speed and low-power signal levels on the left and right sides, respectively. The high-speed signaling levels are below the low-power low-level input threshold such that low-power receiver always detects logic low level when high-speed signals are present.

All absolute voltage levels are relative to the ground voltage at the transmit side.

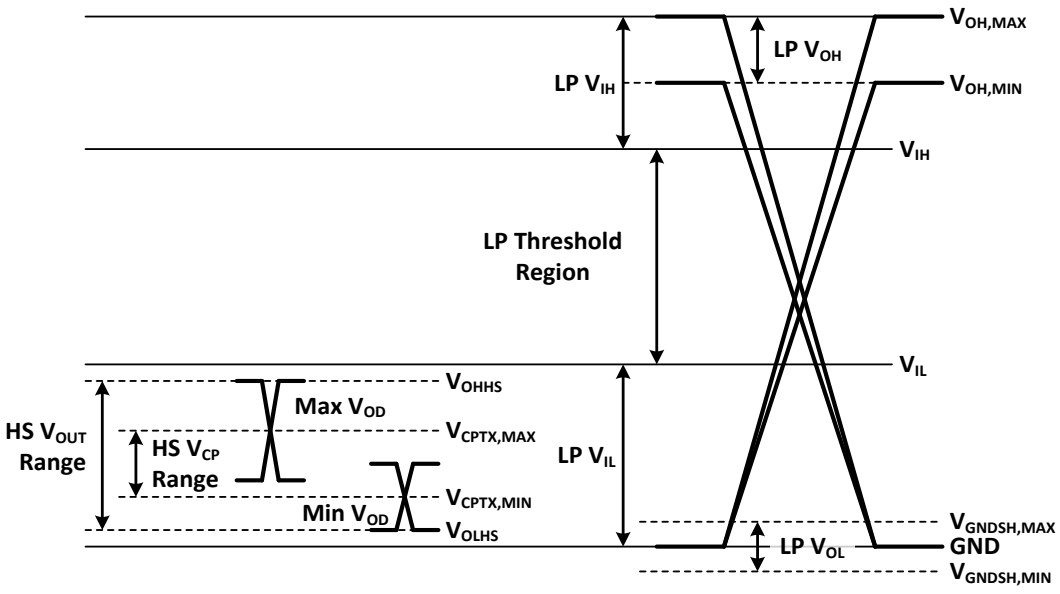

Figure 39 C-PHY Signaling Levels

A lane switches between low-power and high-speed mode during normal operation. Bidirectional lanes can also switch communication direction. The change of operating mode or direction requires enabling and disabling of certain electrical functions. These enable and disable events shall not cause glitches on the lines that would result in a detection of an incorrect signal level. Therefore, all mode and direction changes shall be smooth to always ensure a proper detection of the line signals.

9.1 Driver Characteristics

9.1.1 High-Speed Transmitter

A high-speed C-PHY signal driven on the A, B and C pins is generated by a high-speed output driver. Table 20 is a summary of the six possible high-speed wire states that can be driven on a C-PHY lane. Figure 40 shows two example implementations of a high-speed transmitter. The “T2” Driver Type that presents a valid output impedance at the HS Mid level is the recommended implementation. At slow speeds the “T1” Driver Type may be used if the parametric requirements of Chapter 9 and Chapter 10 can be met.

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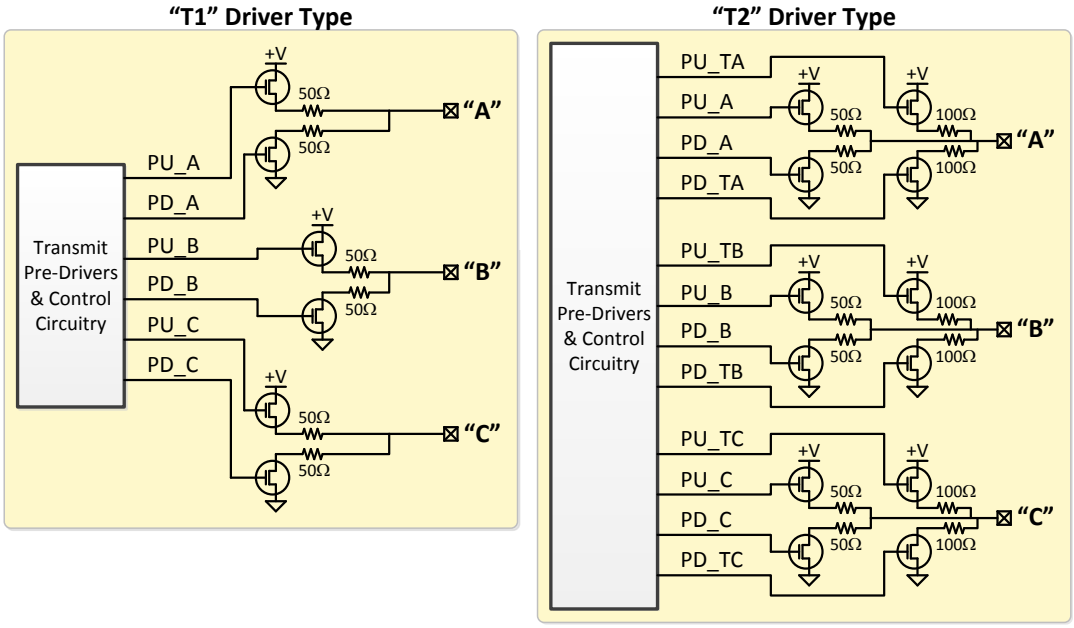
1007 **Table 20 C-PHY High-Speed Wire States**

State Code	Line Voltage Levels		
	A Line	B Line	C Line
HS_+X	HS High	HS Low	HS Mid
HS_-X	HS Low	HS High	HS Mid
HS_+Y	HS Mid	HS High	HS Low
HS_-Y	HS Mid	HS Low	HS High
HS_+Z	HS Low	HS Mid	HS High
HS_-Z	HS High	HS Mid	HS Low



1008 **Figure 40 Example High-Speed Transmitter**

1009 The single-ended output voltages are defined V_A, V_B and V_C at the A, B and C pins, respectively. The
1010 differential output voltages V_{OD_AB}, V_{OD_BC} and V_{OD_CA} are defined as the difference of the voltages: V_A
1011 minus V_B, V_B minus V_C, and V_C minus V_A, respectively.

1012 $$V_{OD\_AB} = V_A - V_B;\ V_{OD\_BC} = V_B - V_C;\ V_{OD\_CA} = V_C - V_A;$$

1013 The output voltages V_A, V_B and V_C at the A, B and C pins shall not exceed the high-speed output high voltage
1014 V_{OHHS}. V_{OLHS} is the high-speed output, low voltage on A, B and C, and is determined by V_{OD_AB}, V_{OD_BC},
1015 V_{OD_CA} and V_{CPTX}. The high-speed V_{OUT} is bounded by the minimum value of V_{OLHS} and the maximum value
1016 of V_{OHHS}.

1017 The common-point voltage V_{CPTX} is defined as the arithmetic mean value of the voltages at the A, B and C
1018 pins:

1019 $$V_{CPTX} = \frac{V_A + V_B + V_C}{3}$$

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V_{OD_AB}, V_{OD_BC} and V_{OD_CA} and V_{CPTX} are shown graphically in Figure 41 for ideal high-speed signals. Figure 42 shows single-ended high-speed signals with the possible kinds of distortion of the differential output and common-point voltages. The strong one and zero levels of V_{OD_AB}, V_{OD_BC} and V_{OD_CA}, and V_{CPTX} may be slightly different for driving any of the six possible wire states on the lane. The strong one and strong zero states for a given wire pair occur only in certain states, and it is the strong levels that are considered to determine ΔV_{OD}. Table 21 shows which high-speed states produce the strong levels for each wire pair.

Table 21 Strong Zero and Strong One State for Each Wire Pair

Wire Pair	Strong Zero State	Strong One State	Weak Zero States	Weak One States
AB	HS_-X	HS_+X	HS_+Y, HS_+Z	HS_-Y, HS_-Z
BC	HS_-Y	HS_+Y	HS_+X, HS_+Z	HS_-X, HS_-Z
CA	HS_-Z	HS_+Z	HS_+X, HS_+Y	HS_-X, HS_-Y

The output differential voltage mismatch, ΔV_{OD}, is defined as the difference of the maximum and minimum of: the absolute values of the differential strong one and strong zero output voltages of the three possible wire pairs. This is expressed by the following equations that consider the V_{OD} for a particular wire pair in a specific state as described in Table 21:

$$V_{OD\_MAX} = max\left(V_{OD\_AB\_+X}, \left|V_{OD\_AB\_-X}\right|, V_{OD\_BC\_+Y}, \left|V_{OD\_BC\_-Y}\right|, V_{OD\_CA\_+Z}, \left|V_{OD\_CA\_-Z}\right|\right)$$

$$V_{OD\_MIN} = min\left(V_{OD\_AB\_+X}, \left|V_{OD\_AB\_-X}\right|, V_{OD\_BC\_+Y}, \left|V_{OD\_BC\_-Y}\right|, V_{OD\_CA\_+Z}, \left|V_{OD\_CA\_-Z}\right|\right)$$

$$\Delta V_{OD} = V_{OD\_MAX} - V_{OD\_MIN}$$

If $V_{CPTX(HS\_+X)}$, $V_{CPTX(HS\_-X)}$, $V_{CPTX(HS\_+Y)}$, $V_{CPTX(HS\_-Y)}$, $V_{CPTX(HS\_+Z)}$, and $V_{CPTX(HS\_-Z)}$ are the common-point voltages for static HS_+X, HS_-X, HS_+Y, HS_-Y, HS_+Z and HS_-Z states, respectively, then the common-point reference voltage is defined as:

$$V_{VCPTX,REF} =$$

$$\frac{V_{VCPTX(HS\_+X)} + V_{VCPTX(HS\_-X)} + V_{VCPTX(HS\_+Y)} + V_{VCPTX(HS\_-Y)} + V_{VCPTX(HS\_+Z)} + V_{VCPTX(HS\_-Z)}}{6}$$

The transient common-point voltage variation is defined by:

$$\Delta V_{CPTX}(t) = V_{CPTX}(t) - V_{CPTX,REF}$$

The static common-point voltage mismatch between the six high-speed states is defined as:

$$V_{MAXCP} = max\left(V_{CPTX(HS\_+X)}, V_{CPTX(HS\_-X)}, V_{CPTX(HS\_+Y)}, V_{CPTX(HS\_-Y)}, V_{CPTX(HS\_+Z)}, V_{CPTX(HS\_-Z)}\right)$$

$$V_{MINCP} = min\left(V_{CPTX(HS\_+X)}, V_{CPTX(HS\_-X)}, V_{CPTX(HS\_+Y)}, V_{CPTX(HS\_-Y)}, V_{CPTX(HS\_+Z)}, V_{CPTX(HS\_-Z)}\right)$$

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1044
$$\Delta V_{CPTX(HS)} = \frac{V_{MAXCP} - V_{MINCP}}{2}$$

1045 The transmitter shall send data such that the high frequency and low frequency common-point voltage
1046 variations do not exceed $\Delta V_{CPTX(HF)}$ and $\Delta V_{CPTX(LF)}$, respectively. An example test circuit for the measurement
1047 of V_{OD} and V_{CPTX} is shown in Figure 43.

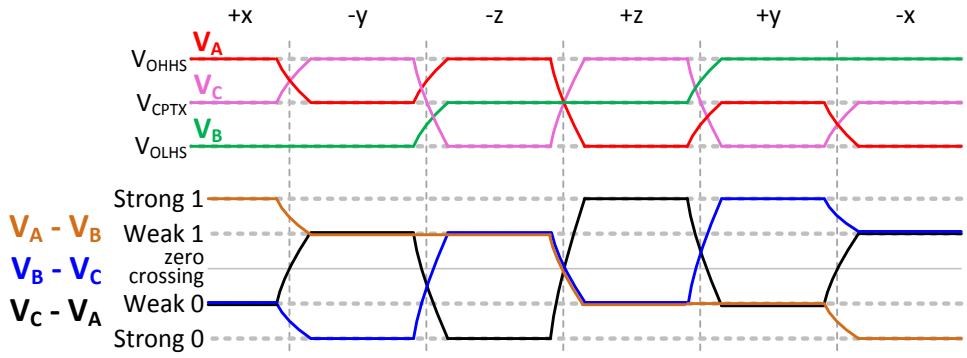

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Figure 41 Ideal Single-ended and Resulting Differential High Speed Signals

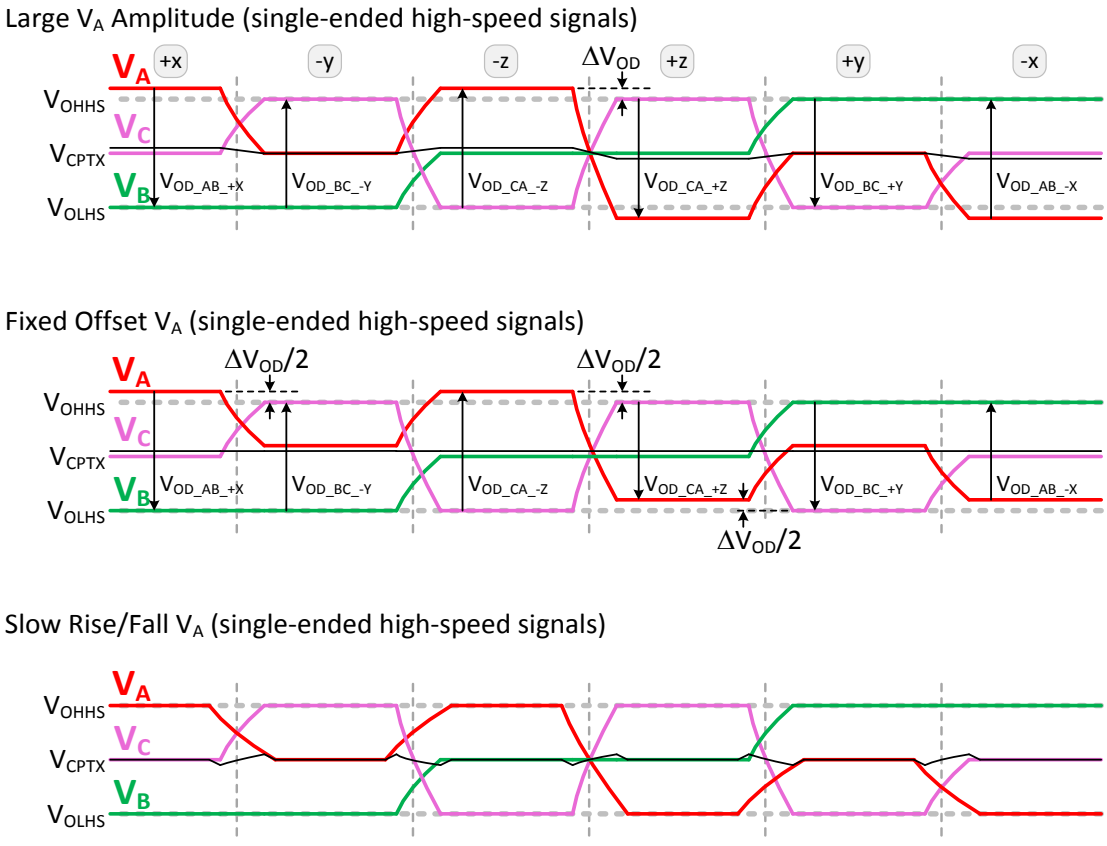

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Figure 42 Possible V_{CPTX} and ΔV_{OD} Distortions of the Single-ended HS Signals

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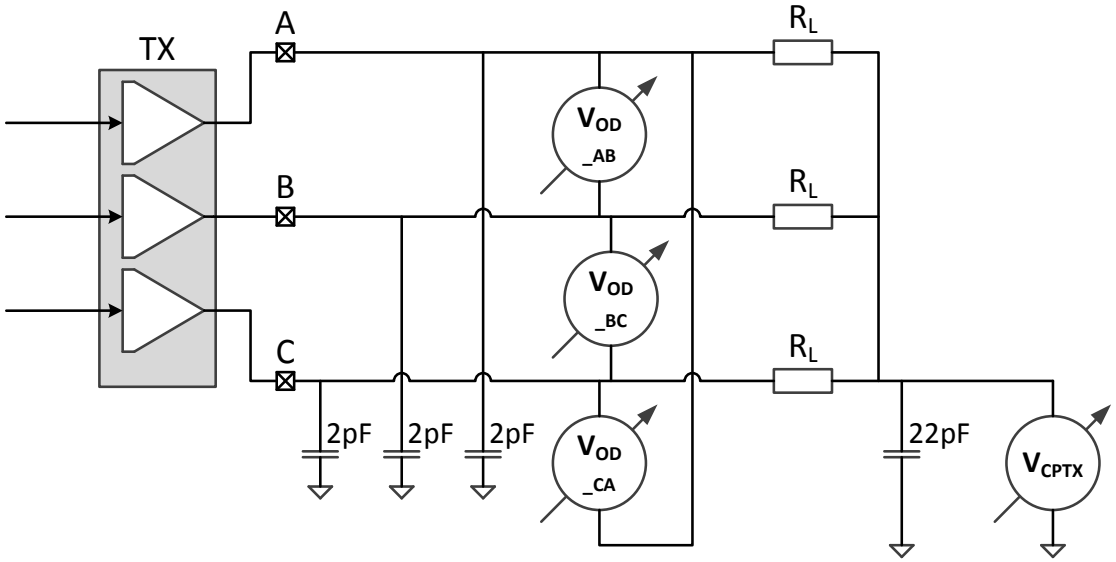

Figure 43 Example Circuit for V_{OD} and V_{CPTX} Measurements

The single-ended output impedance of the transmitter at the A, B and C pins is denoted by Z_{OS}. ΔZ_{OS} is the mismatch of the single ended output impedances at the A, B and C pins, denoted by Z_{OS_A}, Z_{OS_B} and Z_{OS_C}, respectively. This mismatch is defined as the ratio of the difference between the largest and smallest value of Z_{OS_A}, Z_{OS_B} and Z_{OS_C} and the average of those impedances:

$$\Delta Z_{OS} = 3 \cdot \frac{max(Z_{OS\_A}, Z_{OS\_B}, Z_{OS\_C}) - min(Z_{OS\_A}, Z_{OS\_B}, Z_{OS\_C})}{Z_{OS\_A} + Z_{OS\_B} + Z_{OS\_C}}$$

The output impedance Z_{OS} and the output impedance mismatch ΔZ_{OS} shall be compliant with Table 22 for all six possible high-speed wire states and for all allowed loading conditions. It is recommended that implementations keep the output impedance during state transitions as close as possible to the steady state value. The output impedance Z_{OS} can be determined by injecting an AC current into the A, B and C pins and measuring the peak-to-peak voltage amplitude.

The driver shall meet the t_R and t_F specifications as specified in Table 23. The specifications for TX common-mode return loss and the TX differential mode return loss can be found in Section 8.

It is recommended that a high-speed transmitter that is directly terminated at its pins should not generate any overshoot in order to minimize EMI.

Table 22 HS Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{CPTX}	HS transmit static common-point voltage	175	225 to 250	310	mV	1, 3
$\lvert\Delta V_{CPTX(HS)}\rvert$	V_{CPTX} mismatch when output is in any of the six high-speed states			9	mV	2
$\lvert V_{OD}\rvert$ strong	HS transmit differential voltage of the differential strong one and strong zero specified in Table 21.			300	mV	1

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$\|V_{OD}\|$ weak	HS transmit differential voltage of the differential weak one and weak zero specified in Table 21.	97			mV	1
$\|\Delta V_{OD}\|$	V_{OD} mismatch between the absolute values of the differential strong one and strong zero output voltages in any of the six possible high-speed states.			17	mV	2
V_{OHHS}	HS output high voltage			425	mV	1
Z_{OS}	Single ended output impedance	40	50	60	Ω	
ΔZ_{OS}	Single ended output impedance mismatch			10	%	

Note:

1. *Value when driving into load impedance, Z_{ID}, equal to 100 ohms.*
2. *A transmitter should minimize ΔV_{OD} and $\Delta V_{CPTX(HS)}$ in order to minimize radiation, and optimize signal integrity*
3. *Typical value of V_{CPTX} should be in the specified range depending upon the supply voltage used for each implementation.*

1066 **Table 23 HS Transmitter AC Specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CPTX(HF)}$	Common-level variations above 450 MHz			15	mV_{RMS}	
$\Delta V_{CPTX(LF)}$	Common-level variation between 50 MHz and 450 MHz			25	mV_{PEAK}	
t_R and t_F	Rise time and fall time from -58 mV to +58 mV			0.285	UI	1, 2, 3, 5, 6
				0.4 (Note 4)	UI	1, 3, 4, 5, 6
$t_{RISE-FALL-MAX}$	Rise time and fall time limit from -58 mV to +58 mV			360 ps	ps	4, 5

Note:

1. *UI is equal to 1/(2*fh). Refer to Section 8.3 for the definition of fh.*
2. *Applicable for all HS symbol rates > 1.5 Gsps*
3. *To avoid excessive radiation, devices operating at symbol rates ≤ 1.5 Gsps should not use values below 100 ps.*
4. *The maximum absolute time limit of rise and fall times, $t_{RISE-FALL-MAX}$, establishes an upper time limit that is not UI-based. This upper bound that constrains the rise and fall time is useful for implementation of the clock recovery circuit. For rates ≤ 1.5Gsps the rise and fall time shall be ≤ min(0.4 · UI, $t_{RISE-FALL-MAX}$).*
5. *Value when driving into load impedance, Z_{ID}, equal to 100 ohms.*
6. *The rise time measurement applies only to the strong zero to weak one transition, and the fall time measurement applies only to the strong one to weak zero transition.*

9.1.2 Low-Power Transmitter

1067 The low-power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the lines in
1068 all low-power operating modes It is therefore important that the static power consumption of a LP transmitter
1069 be as low as possible. The slew-rate of signal transitions is bounded in order to keep EMI low. An example
1070 of a LP transmitter is shown in Figure 44.

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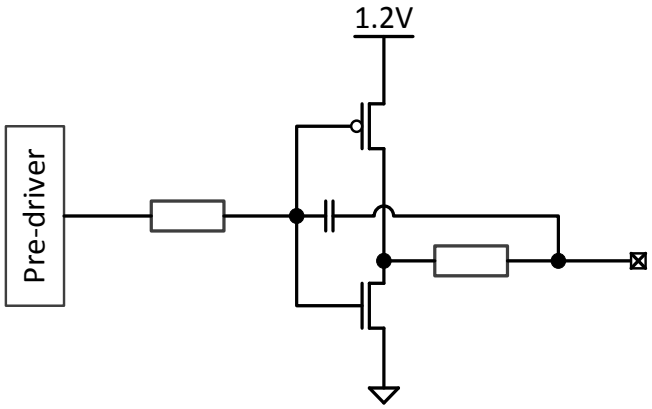

Figure 44 Example LP Transmitter

V_{OL} is the Thevenin output, low-level voltage in the LP transmit mode. This is the voltage at an unloaded pad pin in the low-level state. V_{OH} is the Thevenin output, high-level voltage in the high-level state, when the pad pin is not loaded. The LP transmitter shall not drive the pad pin potential statically beyond the maximum value of V_{OH}. The pull-up and pull-down output impedances of LP transmitters shall be as described in Figure 45 and Figure 46, respectively. The circuit for measuring V_{OL} and V_{OH} is shown in Figure 47.

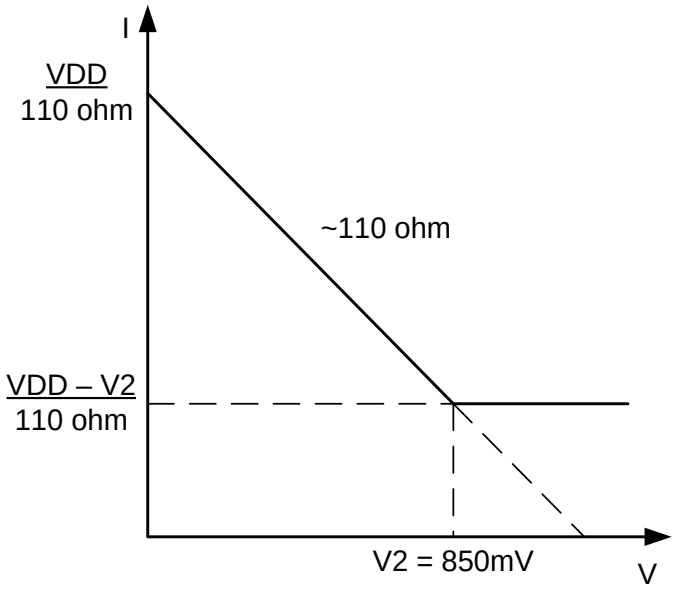

Figure 45 V-I Characteristic for LP Transmitter Driving Logic High

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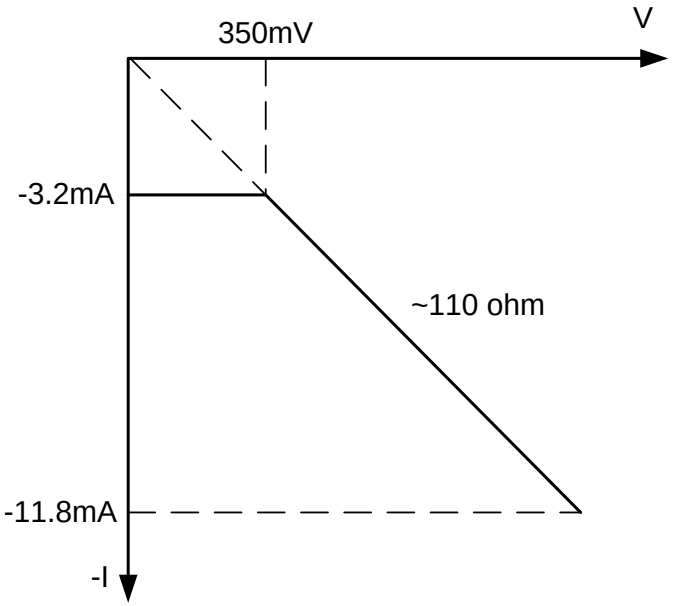

Figure 46 V-I Characteristic for LP Transmitter Driving Logic Low

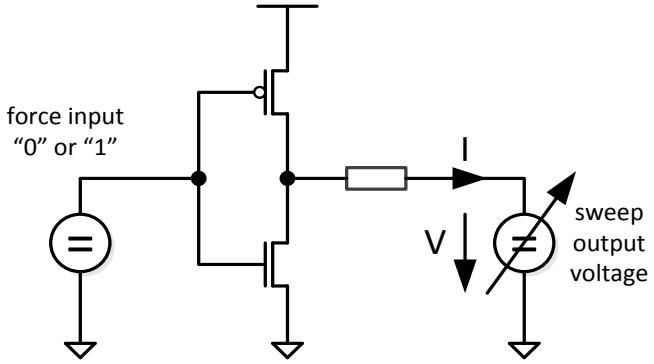

Figure 47 LP Transmitter V-I Characteristic Measurement Setup

The impedance Z_{OLP} is defined by:

$$Z_{OLP} = \left|\frac{V_{THEVENIN} - V_{PIN}}{I_{OUT}}\right|$$

The times t_{RLP} and t_{FLP} are the 15%-85% rise and fall times, respectively, of the output signal voltage, when the LP transmitter is driving a capacitive load C_{LOAD}. The 15%-85% levels are relative to the fully settled V_{OH} and V_{OL} voltages. The slew rate $\delta V/\delta t_{SR}$ is the derivative of the LP transmitter output signal voltage over time. The LP transmitter output signal transitions shall meet the maximum and minimum slew rate specifications as shown in Table 25, Figure 48 and Figure 49. The intention of specifying a maximum slew rate value is to limit EMI.

Table 24 LP Transmitter DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{OH}	Thevenin output high level	0.95		1.3	V	

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V_{OL}	Thevenin output low level	-50		50	mV	
Z_{OLP}	Output impedance of LP transmitter	110			Ω	1, 2

Note:

1. *See Figure 45 and Figure 46.*
2. *Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.*

1089 **Table 25 LP Transmitter AC Specifications**

Parameter	Description		Min	Nom	Max	Units	Notes
t_{RLP}/t_{FLP}	15% - 85% rise time and fall time				25	ns	1
t_{REOT}	30% - 85% rise time and fall time				35	ns	5, 6
$t_{LP\text{-}PULSE\text{-}TX}$	Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after Stop state or last pulse before stop state	40				4
		All other pulses	20				4
$t_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock		90			ns	
$\delta V/\delta t_{SR}$	Slew rate @ C_{LOAD} = 0pF				500	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 5pF				300	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 20pF				250	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 70pF				150	mV/ns	1, 3, 7, 8
	Slew rate @ C_{LOAD} = 0 to 70pF (Falling Edge Only)		25			mV/ns	1, 2, 3
	Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)		25			mV/ns	1, 3, 9
	Slew rate @ C_{LOAD} = 0 to 70pF (Rising Edge Only)		$25 – 0.0625\cdot(V_{O,INST} – 550)$			mV/ns	1, 3, 10, 11
C_{LOAD}	Load capacitance		0		70	pF	1

Note:

1. *C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.*
2. *When the output voltage is between 400 mV and 790 mV.*
3. *Measured as average across any 50 mV segment of the output signal transition.*
4. *This parameter value can be lower than t_{LPX} due to differences in rise vs. fall signal slopes and trip levels and mismatches between A, B and C LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-111) is glitch behavior as described in Section 9.2.2.*
5. *The rise-time of t_{REOT} starts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.*
6. *With an additional load capacitance C_{CP} between 0 and 90 pF on the termination center tap at RX side of the lane*
7. *This value represents a corner point in a piecewise linear curve. See Figure 48 and Figure 49.*
8. *When the output voltage is in the range specified by $V_{PIN(absmax)}$.*

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9. When the output voltage is between 400 mV and 550 mV.
10. Where $V_{O,INST}$ is the instantaneous output voltage, A, B or C, in millivolts.
11. When the output voltage is between 550 mV and 790 mV.

There are minimum requirements on the duration of each LP state. To determine the duration of the LP state, the A, B and C signal lines are each compared to a common trip-level. The result of these comparisons of the A and C signals lines is then exclusive-ORed to produce a single pulse train. The output of this "exclusive-OR clock" can then be used to find the minimum pulse width output of an LP transmitter.

Using a common trip-level in the range [$V_{IL,MAX} + V_{OL,MIN}$, $V_{IH,MIN} + V_{OL,MAX}$], the exclusive-OR clock shall not contain pulses shorter than $t_{LP\text{-}PULSE\text{-}TX}$.

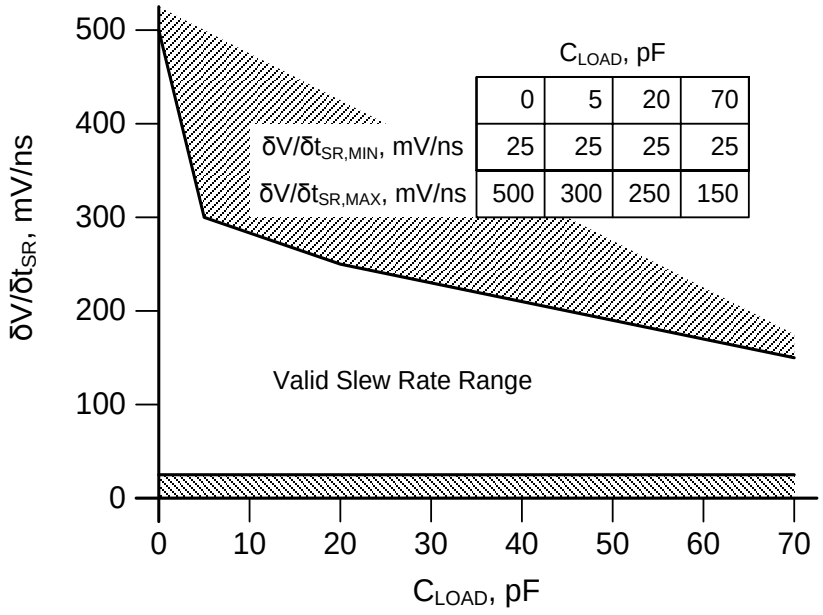

Figure 48 Slew Rate vs. CLOAD (Falling Edge)

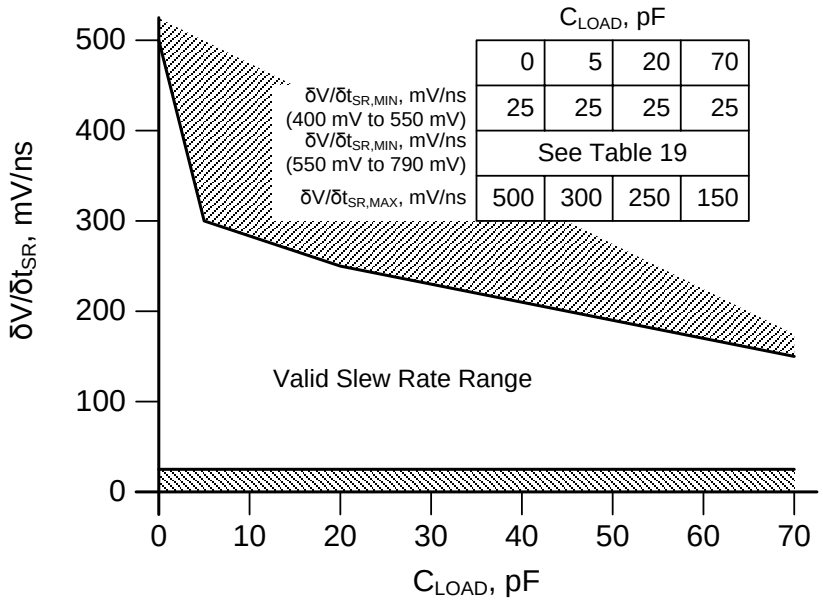

Figure 49 Slew Rate vs. CLOAD (Rising Edge)

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9.2 Receiver Characteristics

9.2.1 High-Speed Receiver

The HS receiver is a group of three differential line receivers. It contains three switchable parallel input terminations, $Z_{ID}/2$ between the three inputs: A, B and C. A simplified diagram of an example implementation is shown in Figure 50.

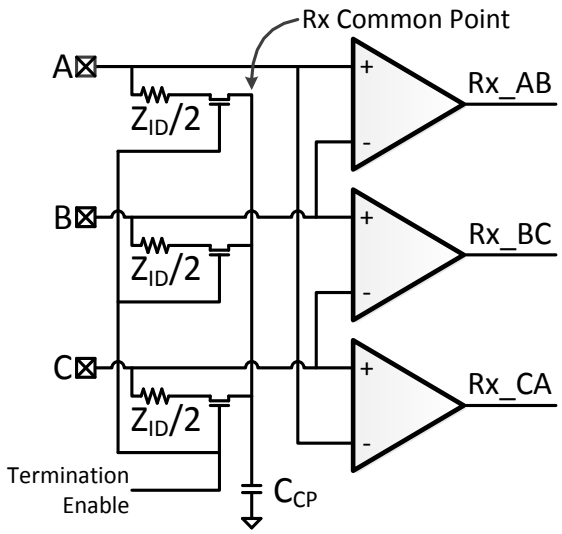

Figure 50 HS Receiver Implementation Example

The differential input high and low threshold voltages of the high-speed receiver are denoted by V_{IDTH} and V_{IDTL}, respectively. V_{ILHS} and V_{IHHS} are the single-ended, input low and input high voltages, respectively. $V_{CPRX(DC)}$ is the differential input common-point voltage. The high-speed receiver shall be able to detect differential signals at its A, B and C input signal pins when all three signal voltages, V_A, V_B and V_C, are within the common-point voltage range and if the voltage differences between V_A, V_B and V_C exceed either V_{IDTH} or V_{IDTL}. The high-speed receiver shall receive high-speed data correctly while rejecting common-point interference $\Delta V_{CPRX(HF)}$ and $\Delta V_{CPRX(LF)}$.

During operation of the high-speed receiver, the three termination impedances $Z_{ID}/2$ are required between the A, B and C pins of the high-speed receiver. The three $Z_{ID}/2$ terminations shall be disabled when the module is not in the high-speed receive mode. When transitioning from low-power mode to high-speed receive mode the termination impedances shall not be enabled until the single-ended input voltages on all of A, B and C fall below $V_{TERM-EN}$. To meet this requirement, a receiver does not need to sense the A, B and C lines to determine when to enable the line termination, rather the LP to HS transition timing can allow the line voltages to fall to the appropriate level before the line termination is enabled.

The differential input impedances of the receiver for A-B, B-C and C-A pairs are denoted by Z_{ID_AB}, Z_{ID_BC}, and Z_{ID_CA}, respectively. ΔZ_{ID} is the mismatch of the differential input impedances. This mismatch is defined as the ratio of the difference between the largest and smallest value of Z_{ID_AB}, Z_{ID_BC} and Z_{ID_CA}, and the average of those impedances:

$$\Delta Z_{ID} = 3 \cdot \frac{max(Z_{ID\_AB}, Z_{ID\_BC}, Z_{ID\_CA}) - min(Z_{ID\_AB}, Z_{ID\_BC}, Z_{ID\_CA})}{Z_{ID\_AB} + Z_{ID\_BC} + Z_{ID\_CA}}$$

The differential input impedances Z_{ID} and the differential input impedance mismatch ΔZ_{ID} shall be compliant with Table 26 for all six possible high-speed wire states and for all allowed loading conditions. It is

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recommended that implementations keep the input impedance during state transitions as close as possible to the steady state value.

The RX common-mode return loss and the RX differential mode return loss are specified in Chapter 8. C_{CP} is the common-mode AC termination, which ensures a proper termination of the receiver at higher frequencies. For higher data rates, C_{CP} is needed at the termination center tap in order to meet the common-mode reflection requirements.

The differential input voltage signal $V_{DIF\_RX}(t)$ is defined as the voltage difference of the receiver inputs for the A-B, B-C and C-A pairs, defined as:

$$V_{DIF\_RX\_AB}(t) = V_A(t) - V_B(t);\ V_{DIF\_RX\_BC}(t) = V_B(t) - V_C(t);\ V_{DIF\_RX\_CA}(t) = V_C(t) - V_A(t);$$

$$V_{DIF\_RX,MAX} = V_{IHHS,MAX} - V_{ILHS,MIN}$$

Table 26 HS Receiver DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$V_{CPRX(DC)}$	Common-Point voltage HS receive mode	95		390	mV	1, 2
V_{IDTH}	Differential input high threshold			40	mV	
V_{IDTL}	Differential input low threshold	-40			mV	
V_{IHHS}	Single-ended input high voltage			535	mV	1
V_{ILHS}	Single-ended input low voltage	-40			mV	1
$V_{TERM-EN}$	Single-ended threshold for HS termination enable			450	mV	
Z_{ID_AB} Z_{ID_BC} Z_{ID_CA}	Differential input impedance	80	100	120	Ω	
ΔZ_{ID}	Differential input impedance mismatch			10	%	

Note:

1. *Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.*
2. *This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-point level tolerance and variations below 450MHz.*

Table 27 HS Receiver AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
$\Delta V_{CPRX(HF)}$	Common-point interference beyond 450 MHz			50	mV	2
$\Delta V_{CPRX(LF)}$	Common-point interference 50MHz – 450MHz	-25		25	mV	1, 4
C_{CP}	Common-point termination			90	pF	3

Note:

1. *Excluding 'static' ground shift of 50mV.*
2. *$\Delta V_{CPRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.*
3. *For higher bit rates, a 22pF capacitor is needed to meet the common-mode return loss specification.*
4. *Voltage difference compared to the DC average common-point potential.*

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9.2.2 Low-Power Receiver

The low-power receiver is an un-terminated, single-ended receiver circuit. The low-power receiver is used to detect the low-power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power.

The input low-level voltage, V_{IL}, is the voltage at which the receiver is required to detect a low state in the input signal. A lower input voltage, $V_{IL-ULPS}$, may be used when the receiver is in the Ultra-Low Power State. V_{IL} is larger than the maximum single-ended line voltage during HS transmission. Therefore, a LP receiver shall detect low during HS signaling.

The input high-level voltage, V_{IH}, is the voltage at which the receiver is required to detect a high state in the input signal. In order to reduce noise sensitivity on the received signal, an LP receiver shall incorporate a hysteresis, The hysteresis voltage is defined as V_{HYST}.

The LP receiver shall reject any input signal smaller than e_{SPIKE}. Signal pulses wider than T_{MIN-RX} shall propagate through the LP receiver.

Furthermore, the LP receivers shall be tolerant of super-positioned RF interference on top of the wanted line signals. This implies an input signal filter. The LP receiver shall meet all specifications for interference with peak amplitude V_{INT} and frequency f_{INT}. The interference shall not cause glitches or incorrect operation during signal transitions.

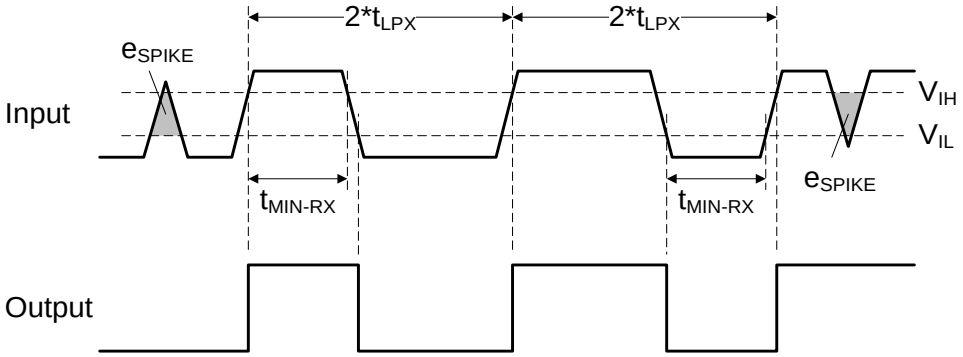

Figure 51 Input Glitch Rejection of Low-Power Receivers

Table 28 LP Receiver DC specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IH}	Logic 1 input voltage	740			mV	
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV	
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV	
V_{HYST}	Input hysteresis	25			mV	

Table 29 LP Receiver AC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
e_{SPIKE}	Input pulse rejection			300	V·ps	1, 2, 3
T_{MIN-RX}	Minimum pulse width response	20			ns	4
V_{INT}	Peak interference amplitude			200	mV	
f_{INT}	Interference frequency	450			MHz	

Note:

1. *Time-voltage integration of a spike above V_{IL} when being in LP-0 state or below V_{IH} when being in LP-1 state. eSpike generation will ensure the spike is crossing both $V_{IL,MAX}$ and $V_{IH,MIN}$ levels.*

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2. *An impulse less than this will not change the receiver state.*
3. *In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.*
4. *An input pulse greater than this shall toggle the output.*

9.3 Line Contention Detection

The low-power receiver and a separate contention detector (LP-CD) shall be used in a bi-directional lane to monitor the line voltage on each low-power signal. This is required to detect line contention as described in Section 7.1. The low-power receiver shall be used to detect an LP high fault when the LP transmitter is driving high and the pin voltage is less than V_{IL}. Refer to Table 28. The LP-CD shall be used to detect an LP low fault when the LP transmitter is driving low and the pin voltage is greater than V_{IHCD}. Refer to Table 30. An LP low fault shall not be detected when the pin voltage is less than V_{ILCD}.

The general operation of a contention detector shall be similar to that of an LP receiver with lower threshold voltages. Although the DC specifications differ, the AC specifications of the LP-CD are defined to match those of the LP receiver and the LP-CD shall meet the specifications listed in Table 29 except for T_{MIN-RX}. The LP-CD shall sufficiently filter the input signal to avoid false triggering on short events.

The LP-CD threshold voltages (V_{ILCD}, V_{IHCD}) are shown along with the normal signaling voltages in Figure 52.

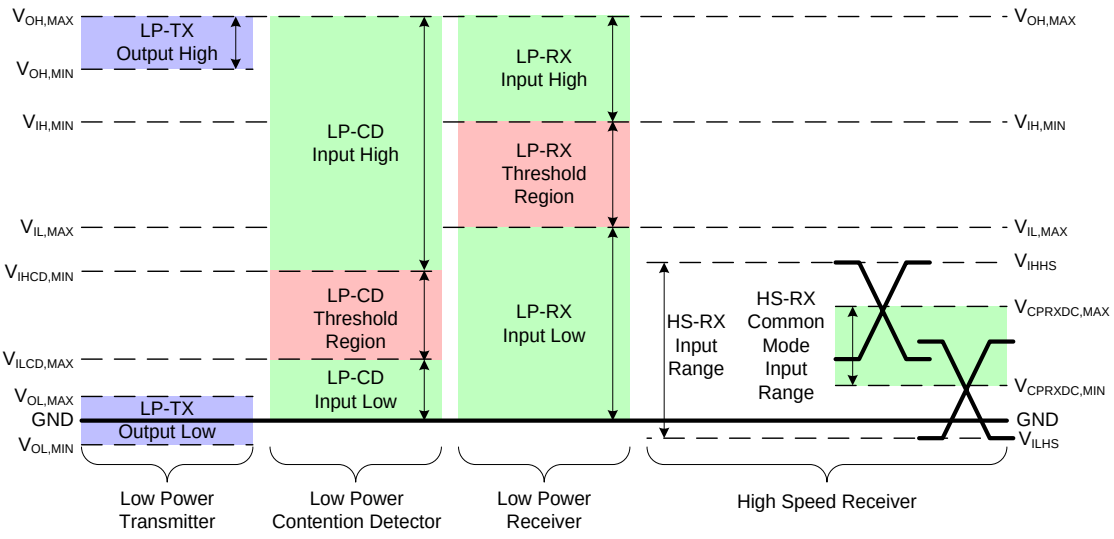

Figure 52 Signaling and Contention Voltage Levels

Table 30 Contention Detector (LP-CD) DC Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
V_{IHCD}	Logic 1 contention threshold	450			mV	
V_{ILCD}	Logic 0 contention threshold			200	mV	

9.4 Input Characteristics

No structure within the PHY may be damaged when a DC signal that is within the signal voltage range V_{PIN} is applied to a pad pin for an indefinite period of time. $V_{PIN(absmax)}$ is the maximum transient output voltage at the transmitter pin. The voltage on the transmitter's output pin shall not exceed $V_{PIN,MAX}$ for a period greater than $T_{VPIN(absmax)}$. When the PHY is in the low-power receive mode the pad pin leakage current shall be I_{LEAK} when the pad signal voltage is within the signal voltage range of V_{PIN}. The specification of I_{LEAK} assures

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1173 interoperability of any PHY in the LP mode by restricting the maximum load current of an LP transmitter.
1174 An example test circuit for leakage current measurement is shown in Figure 53.

1175 The ground supply voltages shifts between a master and a slave shall be less than V_{GNDSH}.

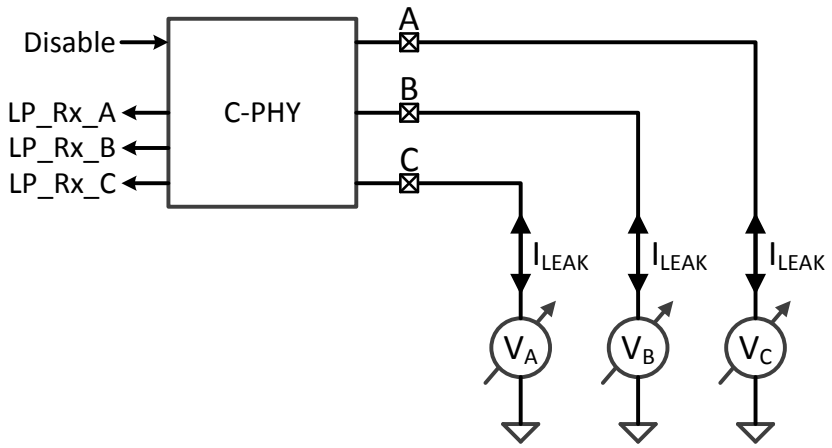

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Figure 53 Pin Leakage Measurement Example Circuit

1177 **Table 31 Pin Characteristic Specifications**

Parameter	Description	Min	Nom	Max	Units	Notes
V_{PIN}	Pin signal voltage range	-50		1350	mV	
I_{LEAK}	Pin leakage current	-10		10	µA	1
V_{GNDSH}	Ground shift	-50		50	mV	
$V_{PIN(absmax)}$	Transient pin voltage level	-0.15		1.45	V	3
$t_{VPIN(absmax)}$	Maximum transient time above $V_{PIN(max)}$ or below $V_{PIN(min)}$			20	ns	2

Note:

1. *When the pad voltage is in the signal voltage range from $V_{GNDSH,MIN}$ to V_{OH} + $V_{GNDSH,MAX}$ and the lane module is in LP receive mode.*
2. *The voltage overshoot and undershoot beyond the V_{PIN} is only allowed during a single 20ns window after any LP-0 to LP-1 transition or vice versa. For all other situations it must stay within the V_{PIN} range.*
3. *This value includes ground shift.*

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10 High-Speed Signal Timing

This section specifies the required timing of the High-speed signaling interface independent of the electrical characteristics of the signal. C-PHY is based on 3-Phase symbol encoding technology where the symbol timing information is encoded in the data sent in each lane. There is at least one transition in the received signal at each UI boundary.

Data transmission may occur at any rate greater than the minimum specified data bit rate.

Figure 54 shows an example PHY configuration including the compliance measurement planes for the specified timing requirements. Note that the effect of signal degradation inside each package due to parasitic effects is included in the timing budget for the transmitter and receiver and is not included in the interconnect degradation budget. See Section 8 for details.

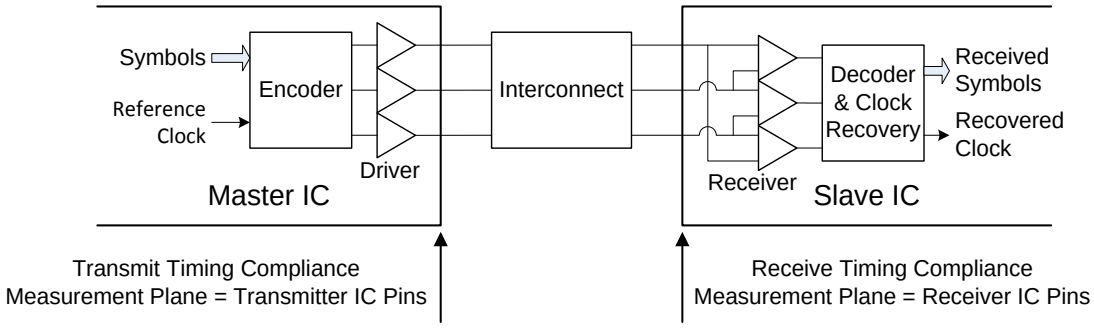

Figure 54 Conceptual C-PHY Lane Timing Compliance Measurement Planes

10.1 High-Speed UI Timing

The master sends high-speed data timing to the slave by encoding the symbol clock timing in the transmitted symbol stream. Symbol encoding to wire states ensures that a transition occurs in the high-speed data at every symbol boundary. The slave recovers the clock for data sampling using these guaranteed transitions in the symbol stream. An example of the single-ended V_A, V_B, and V_C voltages that change at every UI interval, as well as the differential received voltages V_A-V_B, V_B-V_C, and V_C-V_A, is shown in Figure 55.

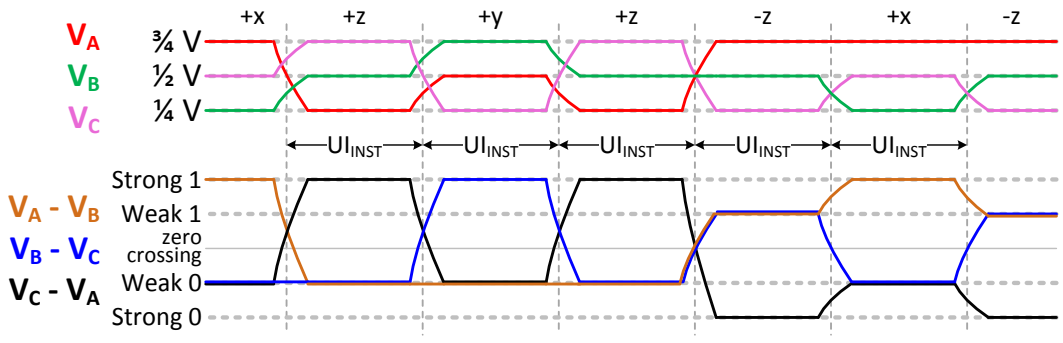

Figure 55 Example of Wire State Transitions at Symbol (UI) Boundaries

Slave circuitry that recovers clock and samples data should respond immediately to transitions in the received data stream. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

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Table 32 Unit Interval (UI) Specification

Parameter	Description	Min	Nom	Max	Units	Notes
UI_{INST}	UI instantaneous			12.5	ns	1, 2
ΔUI	UI variation	-10%		10%	UI	3
		-5%		5%	UI	4

Note:

1. *This value corresponds to a minimum 80 Msps data rate.*
2. *The minimum UI shall not be violated for any single bit period. The allowed instantaneous UI variation can cause instantaneous data rate variations. Therefore, slave devices should be able to accommodate these instantaneous variations of the UI interval .*
3. *When UI ≥ 1ns, within a single burst.*
4. *When UI < 1ns, within a single burst.*

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, it is recommended that devices accommodate these instantaneous variations using some method, such as with elastic storage or by designing the data sink to be tolerant of UI variations.

10.2 High-Speed Data Eye Pattern and Transmission Timing

An eye pattern is a useful tool to specify the C-PHY timing characteristics. The C-PHY eye pattern described below is slightly different than a conventional eye pattern. Differences compared to conventional eye patterns are due to multiple levels seen at the receiving end, and due to specific behaviors of the clock recovery and data capture circuits that are likely to be implemented.

One or more of the differential receiver outputs in the slave will change at each UI boundary due to the symbol encoding rules. When multiple receiver outputs change they are often staggered in time due to slight differences in rise and fall times between the three signals of the lane and due to slight differences in signal propagation times between the combinations of signal pairs received (e.g. A-B, B-C, and C-A). This concept is illustrated in detail in Figure 56, which shows the five types of transitions that can appear in the eye pattern. Figure 56 illustrates the concept that transitions of all three pair combinations can occur at slightly different times near each UI boundary due to the noted characteristics of the C-PHY drivers and receivers; and that there can be one, two or three zero-crossings at each UI boundary. Time $t_{\Delta J}$ in Figure 56, highlights the time difference of the zero-crossings between the first and last signal pair transition.

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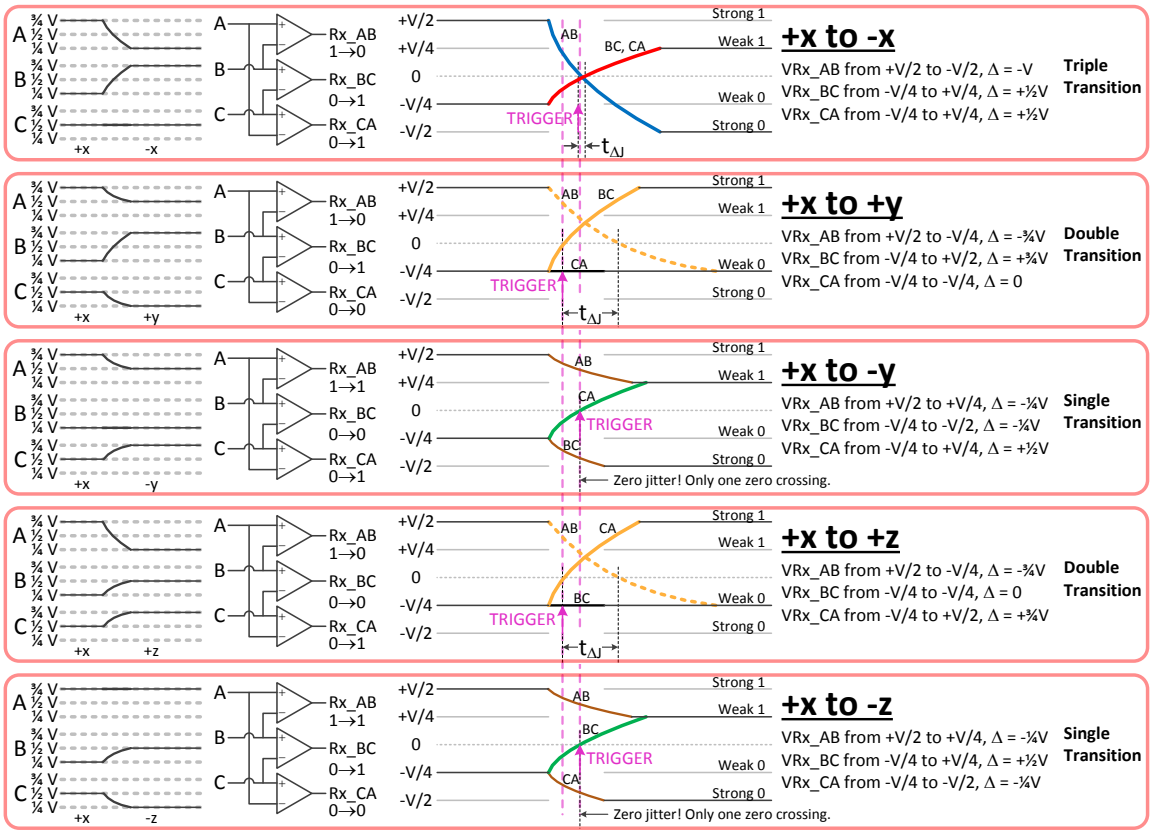

Figure 56 Illustration of all Possible Transitions from the +x State

The eye pattern shown in Figure 57 has four received signal levels that are the result of three transmitted single-ended levels (¼ V, ½ V, ¾ V) of the driver circuit in the C-PHY master. Combinations of the three single-ended levels from the drivers on the three signals of a lane cause a strong and weak 1 and 0 to appear across the three differential receiver inputs in the C-PHY slave (3 ways to receive 2 signals at a time out of a total of 3 signals). Only the center of the eye between the weak 0 and weak 1 are considered by the receivers in the C-PHY slave. The eye pattern shall be drawn by overlapping the three waveforms of all three pairs of signals, which are: A minus B, B minus C, and C minus A. The eye pattern is drawn in this manner because all three pairs of signals are used simultaneously when the clock is recovered and data is captured at the C-PHY slave.

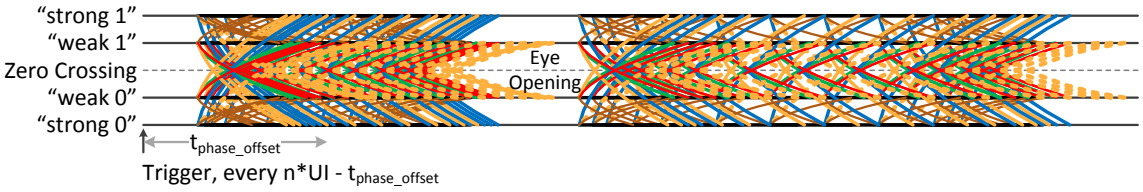

Figure 57 Eye Pattern Example, "Conventional" Trigger

As mentioned previously in section 10.1, the slave recovers the clock for data sampling by using the guaranteed transitions at each UI boundary. Since the receiver can make use of this characteristic, it is important to know the events at the inputs of the differential receivers leading up to the transitions that occur at the UI boundary. Events leading up to the first transition are obscured when the eye is viewed in the conventional manner as shown in Figure 57. The C-PHY eye pattern in Figure 58 is a triggered eye, meaning that the right side of the eye is aligned at a trigger point. The trigger is the first zero crossing of any of the

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three differential waveforms (A minus B, B minus C, and C minus A) that occur at each UI boundary. This trigger point is also shown in the individual waveforms shown in Figure 56 for each of the of the transition types. For UI boundaries that have more than one transition of the differential waveforms, the subsequent transitions in the triggered eye are drawn at their proper position relative to the first transition. (For example: compare the relative position of the solid orange transition with the dashed orange transition in Figure 58, and note how these two transitions are consistent with the same orange transitions in Figure 56.) All of the first zero crossings at each UI boundary are aligned at the trigger point. Similarly, the transitions that occurred during the prior UI boundary are drawn at their proper position relative to the trigger point. The eye mask of the triggered eye diagram represents the worst case that will be observed at a C-PHY receiver that responds to the first zero crossing.

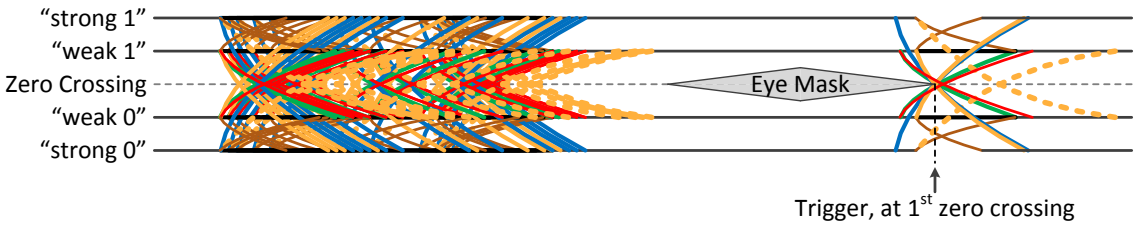

Figure 58 C-PHY Eye Pattern Example, Triggered Eye

The right-most point of the eye mask is aligned with the first zero crossing trigger point so it is consistent with sampling the received data just prior to the trigger point.

As mentioned above, the first zero crossing at each UI boundary (the trigger point) is associated with the sampling of the wire state transmitted prior to that UI boundary. Figure 56 shows that this first transition is caused by the following types of wire state transitions: weak-to-weak, weak-to-strong, and possibly a strong-to-strong (in the triple transition case, +x to -x in Figure 56). The difference of the first transition arrival time at one UI boundary relative to the first transition at the previous UI boundary affects the time period between sampling of two successive wire states (receiver outputs). The peak-to-peak deviation of this zero-crossing time (the trigger point) is illustrated by the two pink dashed lines that span across all five waveforms in Figure 56. Sampling clock jitter is also affected by cycle-to-cycle transmit clock jitter, receiver input offset voltage, and receiver duty-cycle distortion. The jitter caused by the relative difference in zero-crossing time due to the signal slew rate for each transition type is what is illustrated by the pink dashed lines in Figure 56.

10.3 Timing Specifications

The timing requirements specified in this section shall be met for the signal levels specified in Chapter 9, with the channel specified in Chapter 8, while transmitting a pseudo-random data pattern having data transition density similar to the PRBS data patterns described in Chapter 12. The C-PHY Receiver Eye Diagram shown in Figure 59 defines the receiver eye measurement parameters. The measurement points for the transmitter and for the receiver are specified in Figure 54.

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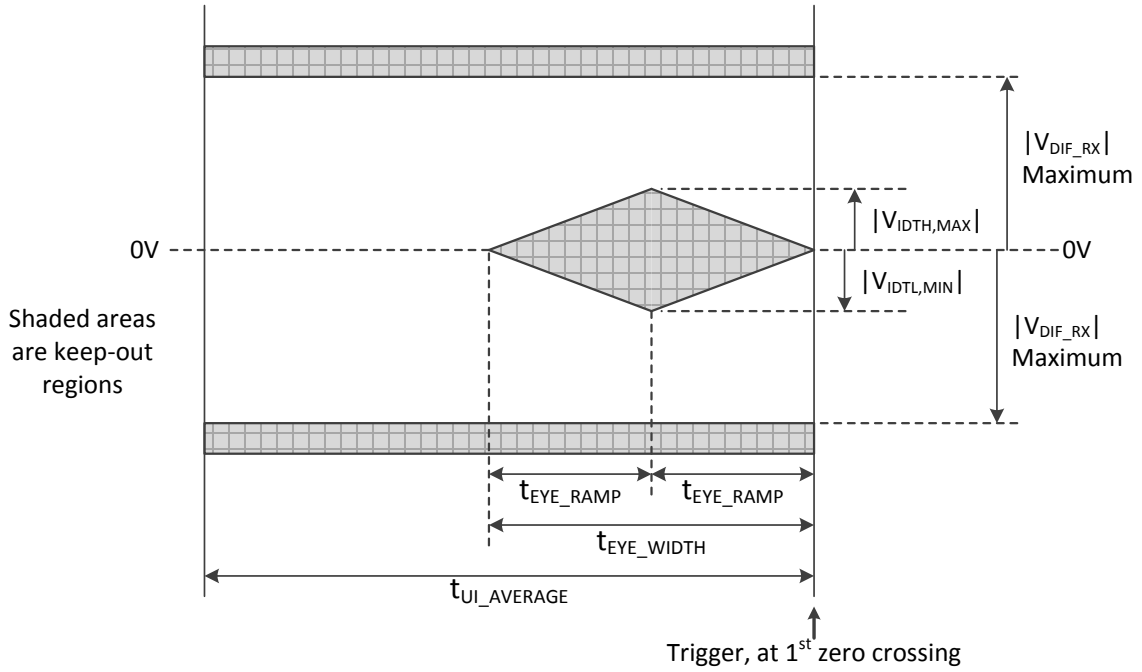

Figure 59 C-PHY Receiver Eye Diagram

$$V_{DIF\_RX} = V_{IHHS,MAX} - V_{ILHS,MIN}$$

The timing specifications are based on allocations of the total unit interval as described in Table 33.

Table 33 Transmit Timing Requirements, TLIS and Receive are Informative

Symbol Rate	TX t_R & t_F	Transmit	C_{PAD_TX}	TLIS	Receive	C_{PAD_RX}
> 1.5Gsps	0.285 UI	0.3 UI	≤ 2pF	0.3 UI	0.4 UI	≤ 2pF
≤ 1.5Gsps	0.4 UI	0.3 UI	≤ 5pF	0.3 UI	0.4 UI	≤ 2pF

10.3.1 Tx Timing Specifications

The transmit signal level requirements and transmit rise and fall time requirements are specified in Section 9.1.1.

The inter-lane skew between lanes that are used together as a group of lanes by a higher layer protocol shall be ±3.5 UI maximum at the output of the transmitter. Inter-lane skew for the interconnect is described in section 8.6.5.

10.3.2 Rx Timing Specifications

The receiver eye diagram requirements are specified below in Table 34, which use Figure 59 as a reference.

Table 34 Receiver Timing Specifications

Parameter	Description	Min	Nom	Max	Units	Notes
t_{EYE_RAMP}	Eye ramp time at the receiver	0.2			UI	
t_{EYE_WIDTH}	Eye width at the receiver	0.4			UI	
$t_{UI\_AVERAGE}$	UI average		UI_{INST}			

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10.4 Reverse High-Speed Data Transmission Timing

High-speed reverse data transmission is not supported.

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11 Regulatory Requirements

1271 All C-PHY based devices should be designed to meet the applicable regulatory requirements.

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12 Built-In Test Circuitry (Informative)

12.1 Introduction

Standardized built-in test circuitry in the C-PHY lane function simplifies production testing, verification, interoperability testing and even self-test of the mobile device that uses the C-PHY. Compatibility of the built-in test circuitry benefits both test equipment and device makers. The test circuit specification defines precise characteristics and behavior of the built-in test circuits, and also includes a register definition for control of the PHY circuit operating and test modes and for observability of important PHY circuit operating conditions.

It is recommended to include the built-in test circuitry and associated control and status registers per the method described in section 12.

12.2 Register Concept

The Lane Configuration and Status Registers can be accessible through any register or memory space that is associated with or related to the C-PHY function. There is no need to use any specific physical interface to gain access to the register or memory space. The only general characteristics to ensure compatibility between test equipment and devices being tested are that each register location be at least 8 bits wide, that the register space be both readable and writeable, and that there are a sufficient number of available address locations to accommodate the product of the per-lane register count times the number of lanes being used plus the number of global registers that are necessary.

12.2.1 Allocation of Register Addresses

Following are specific characteristics of registers that are associated with each C-PHY lane:

3. There is a group of Lane Configuration and Status Registers associated with each C-PHY lane Tx and Rx function.
4. The group of registers for the Tx lane function is separate from a group of registers for the Rx lane function. Each C-PHY master lane is associated with one group of Tx Lane Configuration and Status Registers, and each C-PHY slave lane is associated with one group of Rx Lane Configuration and Status Registers.
5. The individual registers within a group of Lane Configuration and Status Registers that correspond to a specific lane are defined to exist in a contiguous block of addresses starting at a Tx Lane Base Address (Tx_Lane_n_Base) or a Rx Lane Base Address (Rx_Lane_n_Base). The offset of each Lane Configuration and Status Register relative to the Tx Lane Base Address or Rx Lane Base Address is defined for each register definition.
6. The exact physical addresseses of each Tx Lane Base Address and Rx Lane Base Address are flexible. They are defined by the device manufacturer.
7. There can be gaps in the address space between the highest register address within any group of Lane Configuration and Status Registers and Lane Base Address of any other group of Lane Configuration and Status Registers depending on the assignment of physical addresses to base addresses. Device manufacturers may choose to have gaps between Lane Configuration and Status Register groups to be able to fit groups of registers within available addresses in the register address space. (There may be gaps in the address space between each group of Lane Configuration and Status Registers.)
8. Having a unique Tx Lane Base Address or Rx Lane Base Address for each C-PHY lane in a device allows the attributes and status of each lane to be controlled and read individually.

Following are specific characteristics of registers that apply globally across all C-PHY lanes, or to a defined group of C-PHY lanes, in a device:

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9. There is a set of Tx Global Configuration and Status Registers that applies globally to all C-PHY Tx lanes in a device (lanes that have C-PHY master capability) or to a defined group of Tx C-PHY lanes in a device.
10. There is a set of Rx Global Configuration and Status Registers that applies globally to all Rx lanes in a device (lanes that have C-PHY slave capability) or to a defined group of Rx C-PHY lanes in a device.
11. The individual registers within the block of Global Configuration and Status Registers are defined to exist in a contiguous block of addresses beginning from the Tx Global Registers Base Address (Tx_Global_Registers_Base) or Rx Global Registers Base Address (Rx_Global_Registers_Base). The offset of each Global Configuration and Status Register relative to the Tx Global Registers Base Address or Rx Global Registers Base Address is defined for each register definition.
12. The exact physical addresses of the Tx Global Registers Base Address and Rx Global Registers Base Address are flexible. They are defined by the device manufacturer.
13. There can be gaps in the address space between the highest register address within the Tx Global Configuration and Status Registers or Rx Global Configuration and Status Registers and any Tx Lane Base Address or Rx Lane Base Address depending on the assignment of physical addresses to base addresses. Device manufacturers may choose to have gaps between register groups to be able to fit groups of registers within available addresses in the register address space.

A pictorial example of this method is illustrated in Figure 60. This method of register definition enables compatibility between test equipment or test fixtures and devices under test, where only the device-specific base addresses need to be programmed into the testers. Compatibility is ensured by consistent use of the register addressing definition and functional behavior of every bit in the register space defined in this chapter.

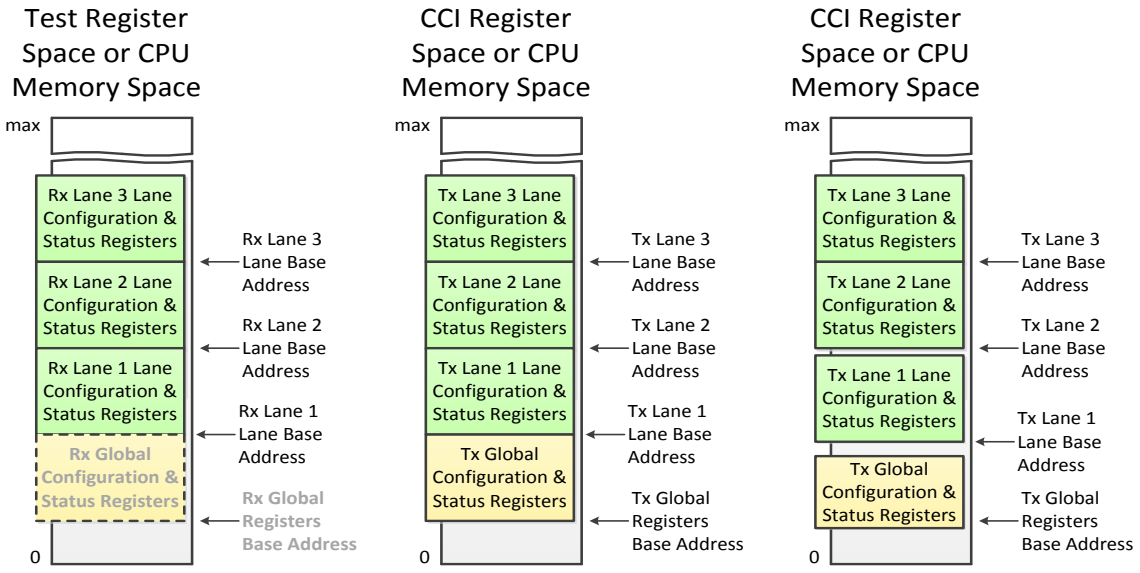

Figure 60 Configuration and Status Register mapping

12.2.2 Example of Register Access via CCI

Examples of suitable interfaces to access the C-PHY register space are: CSI-2 CCI in an image sensor, “flipped” CCI interface or AHB/APB in an application processor, or debug serial bus (JTAG or other) in a display driver IC. The C-PHY Global and Lane Configuration and Status Registers in the image sensor can be accessed easily via the CCI interface. These configuration and status registers in the image sensor can be written and read via CCI without any changes to the intended operating mode of CCI. It is only necessary to allocate space for the registers within the CCI register space. The registers in the application processor may

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be accessed in a number of ways. One method is via a form of CCI, but a special test mode can be enabled where the CCI master in the applications processor is disabled and a CCI slave or even an I2C slave is enabled instead. This CCI slave or I2C slave function is connected to the same SDA and SCL pins as the CCI master, but the slave is only enabled for test mode. The applications processor code will never simultaneously enable both the CCI master and CCI or I2C slave. For normal system operation the CCI master is enabled and the CCI or I2C slave is disabled. For test mode the CCI or I2C slave is enabled and the CCI master is disabled. The recommended locations of CCI master and CCI or I2C slave in each mode, are shown in Figure 61. Other command delivery options such as command bridging through an external device are shown as well.

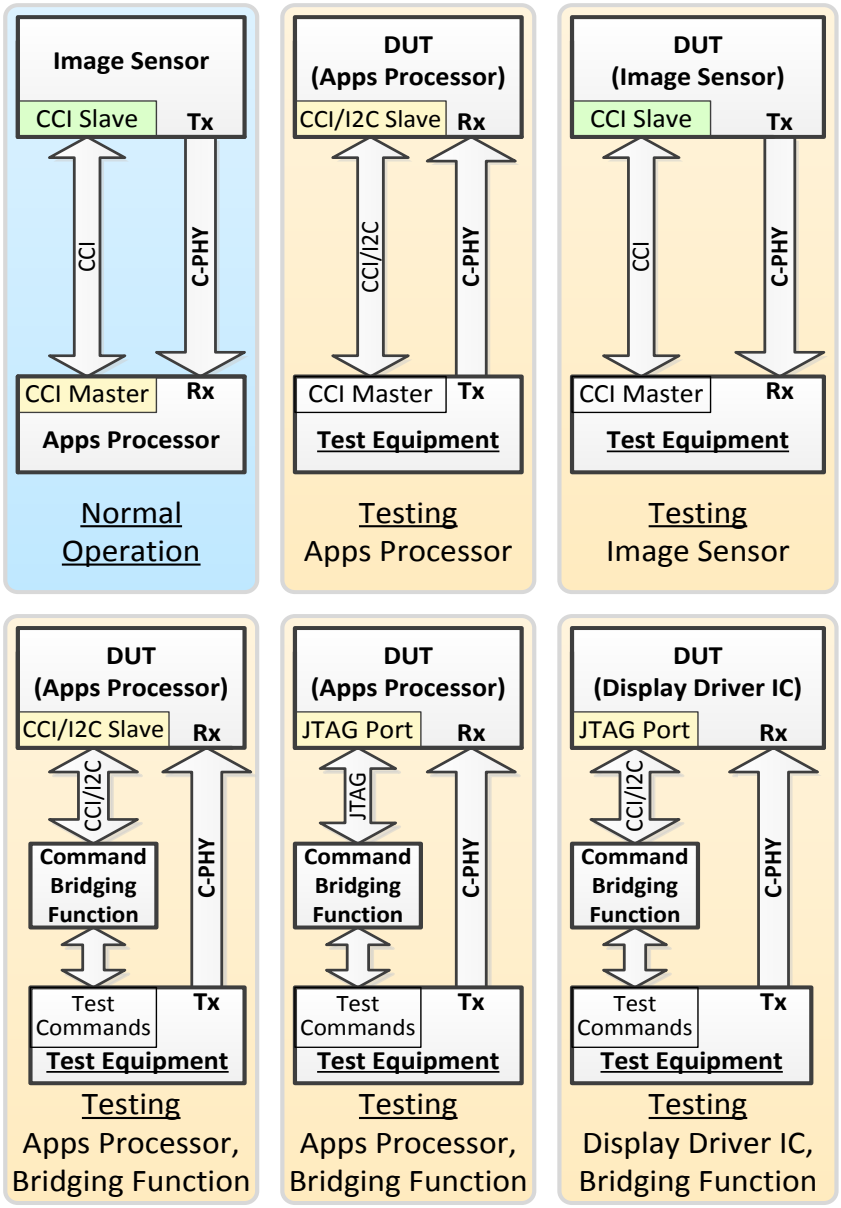

Figure 61 Use of CCI for Normal Operation and Test

The Rx Global and Lane Configuration and Status Registers can be accessed in a similar manner via the CCI slave (for test mode) in the applications processor. It is also possible for the Rx Global and Lane Configuration and Status Registers to be mapped into the CPU memory space instead of using a special CCI

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slave for test mode. The specific method of register access in the applications processor is an implementation choice. However, implementation of the specific function and address mapping of these registers defined in this chapter is recommended.

12.2.3 Register Definitions

A high-level view of the global and lane-specific test circuits is shown in Figure 62. The following sections describe the global and lane test functions for both Tx and Rx. The test circuits can be controlled and observed through registers such as those accessible via the CSI-2 CCI interface. The four primary groups of registers and the abbreviations used in the register names are as follows:

- TLRn – Tx Lane Register n, where n is the number of the lane starting at 1. There is one set of Tx Lane Configuration and Status Registers per lane. In a system having 6 lanes, TLRn could be TLR1, TLR2, TLR3, TLR4, TLR5 or TLR6. n can be larger than 6 in chips supporting multiple camera or display ports. n is limited only by the size of the address space.
- RLRn – Rx Lane Register n, where n is the number of the lane starting at 1. There is one set of Rx Lane Registers per lane. In a system having 6 lanes, RLRn could be RLR1, RLR2, RLR3, RLR4, RLR5 or RLR6. n can be larger than 6 in chips supporting multiple camera or display ports. n is limited only by the size of the address space.
- TGR – Tx Global Configuration and Status Registers, a set of read and write functions that apply to all Tx lanes in a device or to a defined group of Tx lanes in a device.
- RGR – Rx Global Configuration and Status Registers, a set of read and write functions that apply to all Rx lanes in a device or to a defined group of Rx lanes in a device.

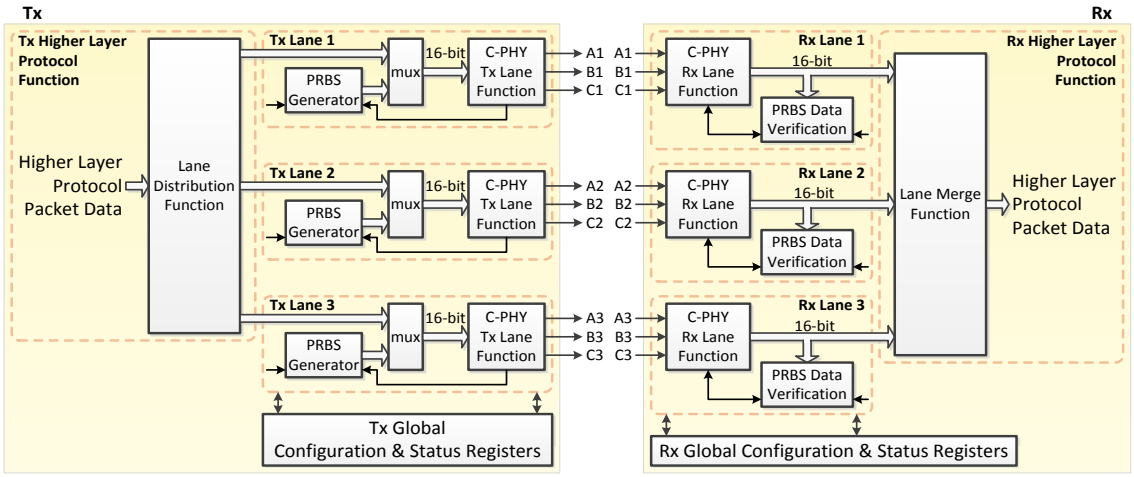

Figure 62 High-Level Tx and Rx, Global and Lane Functions

12.3 Tx Lane Test Circuitry

Figure 63 is a high-level block diagram of a single Tx lane circuit. Test circuitry is indicated by yellow fill in specific blocks. There is one set of Tx Lane Configuration and Status Registers per lane, so a 3-lane system has three sets of Tx Lane Configuration and Status Registers. The definition of each register is described in more detail later in this section.

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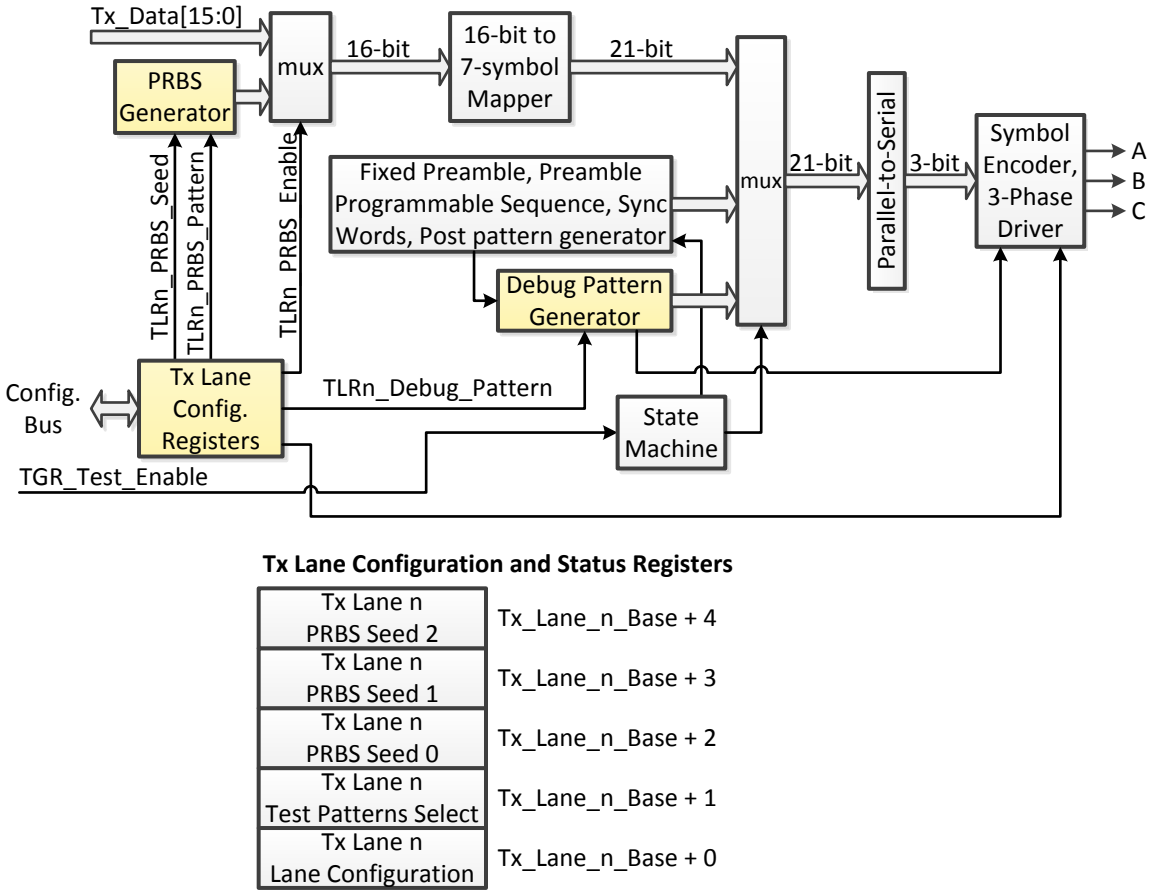

1377 **Figure 63 Transmit (Master) Lane Block Diagram with Test Circuitry**

1378 The Tx Lane Configuration and Status Registers have the following definitions:

12.3.1 TLRn_Lane_Configuration

write-only, Address: Tx_Lane_n_Base + 0

1379 The Tx Lane n Lane Configuration register is used to configure parameters that are specific to the function
1380 of the lane.

[7:0] – reserved for future use.	

12.3.2 TLRn_Test_Patterns_Select

write-only, Address: Tx_Lane_n_Base + 1

1381 The Tx Lane n Test Patterns Select register provides the means to choose a specific test pattern to be output
1382 by a transmit lane function.

[7:5] – TLRn_PRBS_Pattern	=0 – select 16-bit Tx_Data[15:0] from Lane Distribution Function (normal operation) =1 to 3 – reserved for future use =4 – select PRBS9 =5 – select PRBS11 =6 – select PRBS18 =7 – reserved for future use

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[4] – Reserved for future use	
[3:0] – TLRn_Debug_Pattern	=0 – select output of 16-to7 Mapper (normal operation) or PRBS pattern, as selected by TLRn_PRBS_Pattern =1 – debug pattern is a sequence of 14 symbols defined by the same Tx Global Registers that define the Programmable Sequence of the Preamble =2 – debug pattern is a sequence of wire states that are defined by the same Tx Global Registers that define the Programmable Sequence of the Preamble =3 to 15 – reserved for future use

Since the mux to select the TLRn_Debug_Pattern is "downstream" from the mux that selects the PRBS pattern, the TLRn_Debug_Pattern selection takes precedence over the TLRn_PRBS_Pattern setting. When the TLRn_Debug_Pattern selection is equal to 1 then the debug pattern is defined by the Tx Global Registers: TGR_Preamble_Prog_Sequence_0,1 [Tx_Global_Registers_Base_Address + 3] through TGR_Preamble_Prog_Sequence_12,13 [Tx_Global_Registers_Base_Address + 9]. These are the same registers that define the programmable sequence portion of the preamble. The 14-symbol debug pattern is repeated in the transmitted high speed data following the sync word as shown in Figure 64.

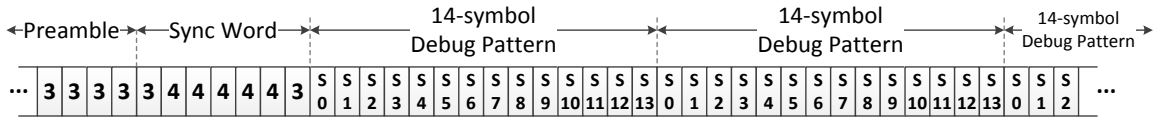

Figure 64 Repeating 14-Symbol Debug Pattern in High Speed Data

If the TLRn_Debug_Pattern field is equal to 1 then the debug pattern is a sequence of 14 symbols defined by the same Tx Global Registers that define the Programmable Sequence of the Preamble. The symbols are defined using the same 3-bit Flip Rotation Polarity format that is described in Table 4.

If the TLRn_Debug_Pattern field is equal to 2 then the debug pattern is a sequence of 14 wire states defined by the same Tx Global Registers that define the Programmable Sequence of the Preamble. The wire states are defined using the 3-bit format described in the table below. When TLRn_Debug_Pattern is set to 2 then the programmable sequence values are defined as wire states rather than symbol values. The bit numbers in the column headings of the table correspond to bit numbers in the Transmit Global Registers TGR_Preamble_Prog_Sequence_0,1 through TGR_Preamble_Prog_Sequence_12,13.

	TGR_Preamble_ Prog_Sequence…[5]	**TGR_Preamble_ Prog_Sequence…[4]**	**TGR_Preamble_ Prog_Sequence…[3]**
Wire State	**TGR_Preamble_ Prog_Sequence…[2]**	**TGR_Preamble_ Prog_Sequence…[1]**	**TGR_Preamble_ Prog_Sequence…[0]**
+x	1	0	0
-x	0	1	1
+y	0	1	0
-y	1	0	1
+z	0	0	1
-z	1	1	0

Note that the first wire state of the programmable sequence transmitted following the last bit of the Sync Word might happen to be the same wire state transmitted during the last unit interval of the Sync Word. If this happens then there will be no wire state transition at that unit interval boundary to generate a symbol clock pulse in a receiver. This is acceptable behavior because the purpose of the programmable wire state debug pattern is to evaluate electrical and timing characteristics of the driver.

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12.3.3 TLRn_PRBS_Seed_0

write-only, Address: Tx_Lane_n_Base + 2

The Tx Lane n PRBS Seed 0 register is an 8-bit value used to initialize the least significant 8 bits of the 18-bit Seed for the Tx Lane PRBS register. Figure 65 shows the method to initialize the Transmit Lane PRBS register using the fragments of the Seed value.

[7:0] – seed value for Transmit PRBS register Q[8:1]	TLRn_PRBS_Seed_0[7] → Q[8]; through TLRn_PRBS_Seed_0[0] → Q[1];

12.3.4 TLRn_PRBS_Seed_1

write-only, Address: Tx_Lane_n_Base + 3

The Tx Lane n PRBS Seed 1 register is an 8-bit value used to initialize the next least significant 8 bits of the 18-bit Seed for the Tx Lane PRBS register. Figure 65 shows the method to initialize the Transmit Lane PRBS register using the fragments of the Seed value.

[7:0] – seed value for Transmit PRBS register Q[16:9]	TLRn_PRBS_Seed_1[7] → Q[16]; through TLRn_PRBS_Seed_1[0] → Q[9];

12.3.5 TLRn_PRBS_Seed_2

write-only, Address: Tx_Lane_n_Base + 4

The Tx Lane n PRBS Seed 2 register is a 2-bit value used to initialize the most significant 2 bits of the 18-bit Seed for the Tx Lane PRBS register. Figure 65 shows the method to initialize the Transmit Lane PRBS register using the fragments of the Seed value.

[7:2] – Reserved for future use	
[1:0] – seed value for Transmit PRBS register Q[18:17]	TLRn_PRBS_Seed_2[1] → Q[18]; through TLRn_PRBS_Seed_2[0] → Q[17];

12.3.6 Tx Lane PRBS Register Operation

The Transmit Lane PRBS Register Q[16:1] is the source of data input to TxD[15:0] of the Mapper when the lane master is transmitting one of the three PRBS patterns as defined by the TLRn_Test_Patterns_Select register. The Transmit Lane PRBS Register function is defined in Figure 65. The Transmit Lane PRBS register is initialized using the seed values TLRn_PRBS_Seed_0, TLRn_PRBS_Seed_1 and TLRn_PRBS_Seed_2, as shown in Figure 65. The first word transmitted from the PRBS generator is equal to the seed value: [TLRn_PRBS_Seed_1[7:0], TLRn_PRBS_Seed_0[7:0]]. This initial 16-bit value from the PRBS register is transmitted immediately following transmission of the first Sync Word after the low-power to high-speed mode transition. The Transmit Lane PRBS Register is shifted 16 bit positions after each 16-bit word is output to minimize correlation from one data value to the next. This way no bits are re-used in successive samples.

Example Seed values and data sequences for the chosen PRBS mode are as follows:

PRBS9 – Seed = 0x789a; TLRn_PRBS_Seed_0[7:0] = 0x9a; TLRn_PRBS_Seed_1[7:0] = 0x78; TLRn_PRBS_Seed_2[7:0] value does not matter;
Transmit data sequence: 0x789a, 0x9980, 0xc651, 0xa5fd, 0x163a, 0xcb3c, 0x7dd0…

PRBS11 – Seed = 0x789a; TLRn_PRBS_Seed_0[7:0] = 0x9a; TLRn_PRBS_Seed_1[7:0] = 0x78; TLRn_PRBS_Seed_2[7:0] value does not matter;
Transmit data sequence: 0x789a, 0x5e64, 0xfee0, 0xac43, 0xa9a1, 0xe4ce, 0xfea0…

PRBS18 – Seed = 0x2789a; TLRn_PRBS_Seed_0[7:0] = 0x9a; TLRn_PRBS_Seed_1[7:0] = 0x78; TLRn_PRBS_Seed_2[7:0] = 0x02;
Transmit data sequence: 0x789a, 0x8d77, 0x0dbc, 0x74e1, 0x8108, 0x414a, 0x3915…

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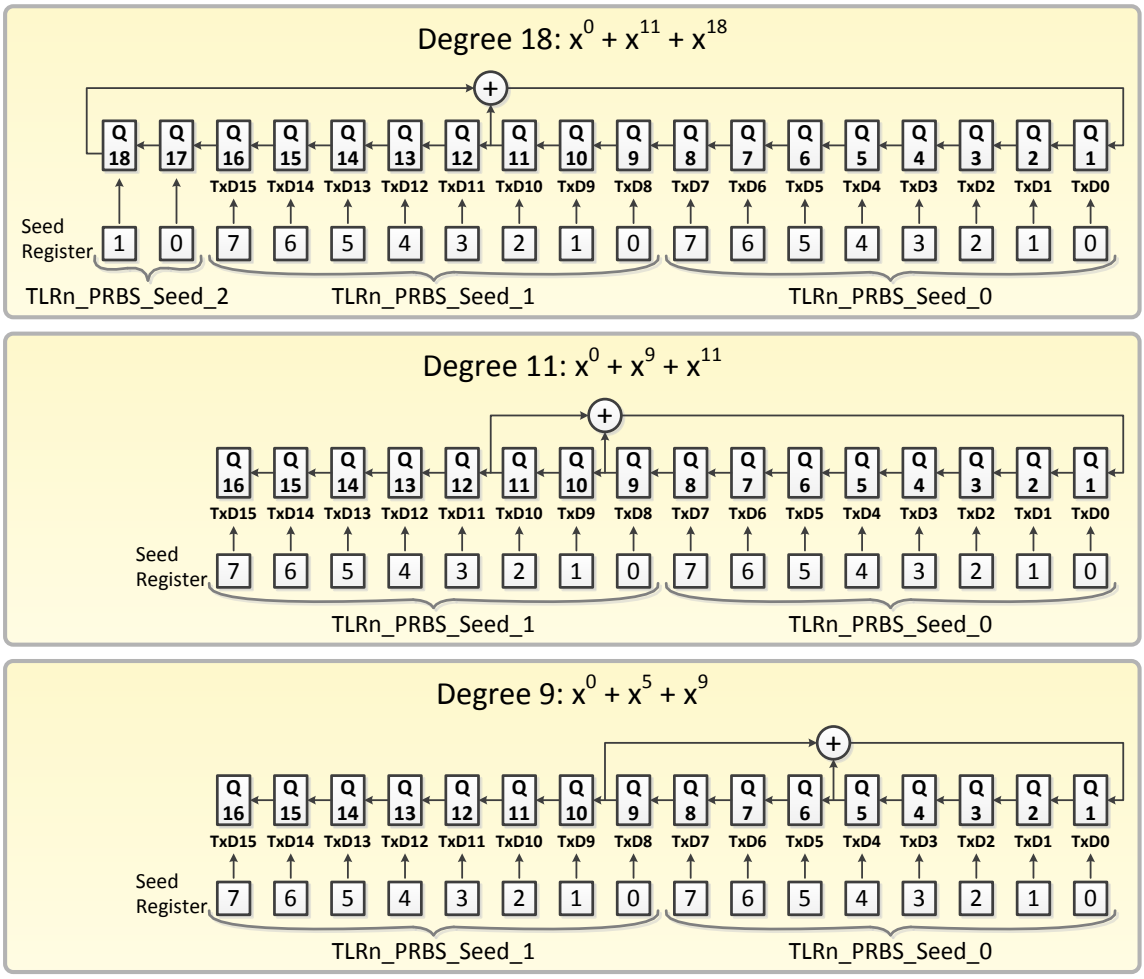

Figure 65 Tx Lane PRBS Register Function and Seed Value Initialization

12.4 Rx Lane Test Circuitry

Figure 66 shows a high-level block diagram of the Receive Lane with test circuitry.

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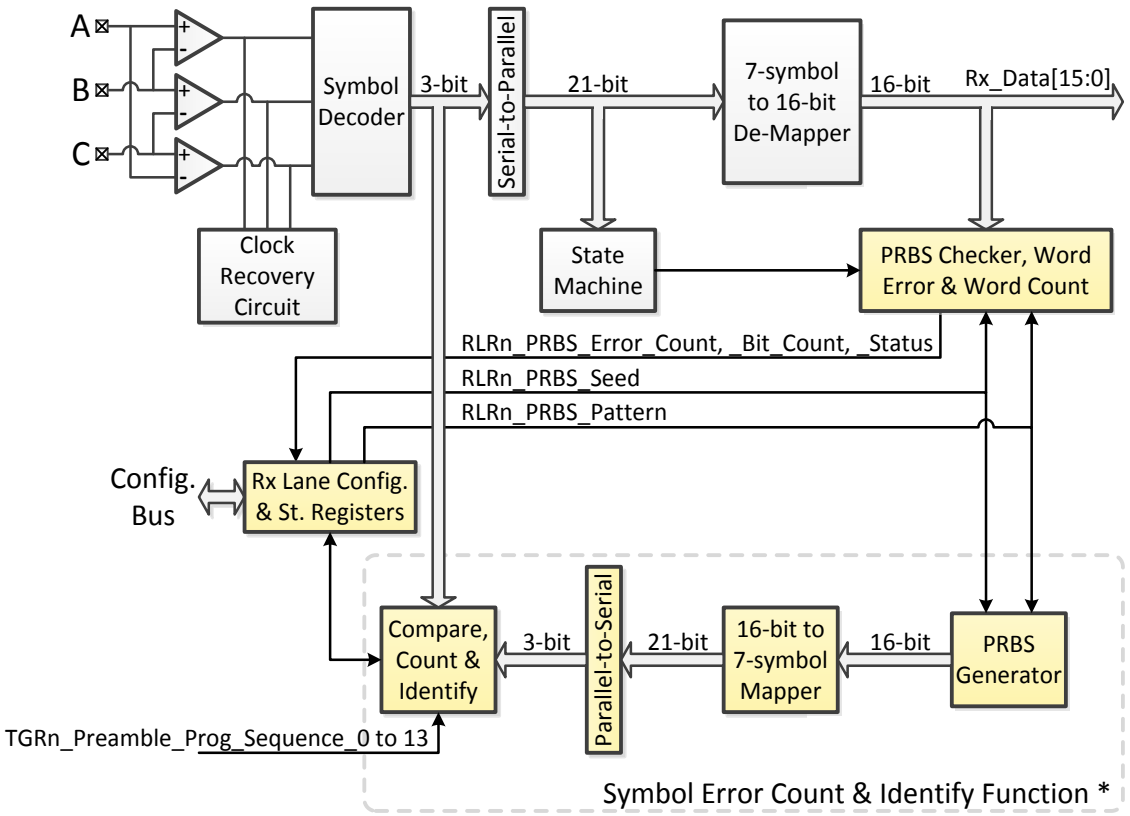

Rx Lane Configuration and Status Registers

Rx Lane n 1st Sym Error Location 5 *	Rx_Lane_n_Base + 19	Rx Lane n Word Count 2	Rx_Lane_n_Base + 9
Rx Lane n 1st Sym Error Location 4 *	Rx_Lane_n_Base + 18	Rx Lane n Word Count 1	Rx_Lane_n_Base + 8
Rx Lane n 1st Sym Error Location 3 *	Rx_Lane_n_Base + 17	Rx Lane n Word Count 0	Rx_Lane_n_Base + 7
Rx Lane n 1st Sym Error Location 2 *	Rx_Lane_n_Base + 16	Rx Lane n Word Error Count	Rx_Lane_n_Base + 6
Rx Lane n 1st Sym Error Location 1 *	Rx_Lane_n_Base + 15	Rx Lane n PRBS Seed 2	Rx_Lane_n_Base + 5
Rx Lane n 1st Sym Error Location 0 *	Rx_Lane_n_Base + 14	Rx Lane n PRBS Seed 1	Rx_Lane_n_Base + 4
Rx Lane n Symbol Error Count *	Rx_Lane_n_Base + 13	Rx Lane n PRBS Seed 0	Rx_Lane_n_Base + 3
Rx Lane n Word Count 5	Rx_Lane_n_Base + 12	Rx Lane n Status	Rx_Lane_n_Base + 2
Rx Lane n Word Count 4	Rx_Lane_n_Base + 11	Rx Lane n PRBS Pattern	Rx_Lane_n_Base + 1
Rx Lane n Word Count 3	Rx_Lane_n_Base + 10	Rx Lane n Configuration	Rx_Lane_n_Base + 0

* a Symbol Error Count Function, remove if not needed

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Figure 66 Receive (Slave) Lane Block Diagram with Test Circuitry

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The Rx Lane Configuration and Status Registers have the following definitions:

12.4.1 RLRn_Lane_Configuration

write-only, Address: Rx_Lane_n_Base + 0

The Rx Lane n Configuration register currently has no assigned bits in the register to affect the lane function.

[7:0] – reserved for future use	

12.4.2 RLRn_Test_Pattern_Select

write-only, Address: Rx_Lane_n_Base + 1

The Rx Lane n Test Pattern register provides the means to choose a specific PRBS pattern to be used by the PRBS Checker. The register contents also specify which pattern is to be used by the symbol error counting function, if the symbol error count feature is implemented.

[7:5] – RLRn_PRBS_Pattern_Select	=0 – disable error detection and counting =1 to 3 – reserved for future use =4 – select PRBS9 =5 – select PRBS11 =6 – select PRBS18 =7 – reserved for future use
[4] – reserved for future use	
[3:0] – RLRn_Symbol_Error_Count_Function	=0 – the symbol error count function, if implemented, is controlled by bits [7:5]. The symbol error count compares received symbols with the selected PRBS sequence sent through the mapper; or if bits [7:5] are all zero then the symbol error count function is disabled. =1 – the symbol error count function, if implemented, compares received symbols with the user-defined debug pattern, which is defined by the same Tx Global Registers that define the Programmable Sequence of the Preamble. For a receive-only device, the receiver would need to implement the seven Tx Global Registers that define the programmable sequence, even if that device does not contain a Tx C-PHY function. =2 to 15 – reserved for future use

It is not necessary to enable or disable the error counting function. There is no harm in counting errors all of the time, even when actual packet data is being received. The system software will know to ignore the error counter value at that time. The enable/disable setting may be useful to prevent activity in the receiver error measurement system to slightly reduce power consumption when the capability to count errors is not required.

12.4.3 RLRn_Rx_Lane_Status

read-only, Address: Rx_Lane_n_Base + 2

The Rx Lane n Status register contains status indicators relating to important events that occur when a packet is received. All bits in the register are reset when the lane detects the transition from LP-111 to LP-001. The lane status logic keeps track of each event described in the RLRn_Rx_Lane_Status register. The register contents may be valid prior to the LP-000 to LP-111 transition. The register contents contain the actual status following the LP-000 to LP-111 transition.

[7] – LP-001 to LP-000 transition was detected.	1 – The transition was detected. 0 – The transition was not detected.

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[6] – Preamble Programmable Sequence status (optional)	0 if not used. The specific function of this bit is determined by the device manufacturer.
[5] –Sync Word was detected.	1 – The Sync Word was detected. 0 – The Sync Word was not detected.
[4] – Post sequence was detected	1 – Post was detected. 0 – Post was not detected.
[3:0] – reserved for future use	

12.4.4 RLRn_PRBS_Seed_0

write-only, Address: Rx_Lane_n_Base + 3

The Rx Lane n PRBS Seed 0 register is an 8-bit value used to initialize the least significant 8 bits of the 18-bit Seed for the Receive Lane PRBS register. Figure 67 shows the method to initialize the PRBS register using the fragments of the Seed value.

[7:0] – seed value for Receive PRBS register Q[8:1]	RLRn_PRBS_Seed_0[7] → Q[8]; through RLRn_PRBS_Seed_0[0] → Q[1];

12.4.5 RLRn_PRBS_Seed_1

write-only, Address: Rx_Lane_n_Base + 4

The Rx Lane n PRBS Seed 1 register is an 8-bit value used to initialize the next least significant 8 bits of the 18-bit Seed for the Receive Lane PRBS register. Figure 67 shows the method to initialize the PRBS register using the fragments of the Seed value.

[7:0] – seed value for Receive PRBS register Q[16:9]	RLRn_PRBS_Seed_1[7] → Q[16]; through RLRn_PRBS_Seed_1[0] → Q[9];

12.4.6 RLRn_PRBS_Seed_2

write-only, Address: Rx_Lane_n_Base + 5

The Rx Lane n PRBS Seed 2 register is a 2-bit value used to initialize the most significant 2 bits of the 18-bit Seed for the Receive Lane PRBS register. Figure 67 shows the method to initialize the PRBS register using the fragments of the Seed value.

[7:2] – Reserved for future use	
[1:0] – seed value for Receive PRBS register Q[18:17]	RLRn_PRBS_Seed_2[1] → Q[18]; through RLRn_PRBS_Seed_2[0] → Q[17];

12.4.7 Rx Lane PRBS Register Operation

The Receive Lane PRBS Register Q[16:1] is the reference data that is compared with RxD[15:0] from the De-Mapper when the lane slave is operating in one of the three PRBS test modes as defined by the RLRn_PRBS_Pattern register. The Receive Lane PRBS Register function is defined in Figure 67. The Receive Lane PRBS Register is initialized using the seed values RLRn_PRBS_Seed_0, RLRn_PRBS_Seed_1 and RLRn_PRBS_Seed_2, as shown in Figure 67. The first reference word from the Receive Lane PRBS Register is equal to the seed value: [RLRn_PRBS_Seed_1[7:0], RLRn_PRBS_Seed_0[7:0]]. This first word from the Receive Lane PRBS Register is compared with the first word of received data immediately following the first Sync Word after the low-power to high-speed mode transition. The Receive Lane PRBS Register is shifted 16 bit positions after each 16-bit word of reference data is output to correspond exactly with the data that was transmitted.

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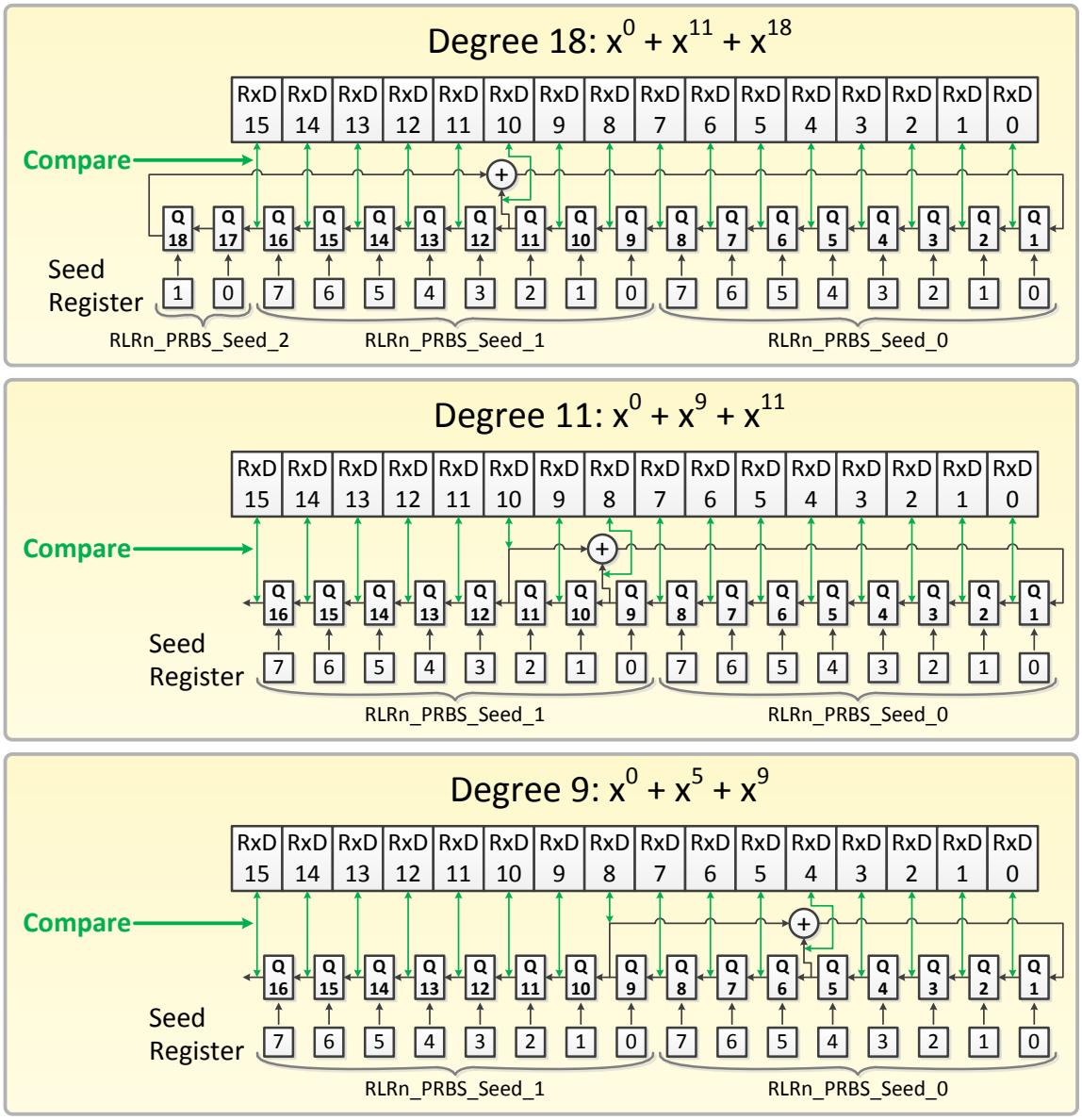

Figure 67 Rx Lane PRBS Register Function and Seed Value Initialization

12.4.8 Rx Lane Word Error Count and Word Count Functionality

The Rx Lane Word Error Count is a count of the number of word errors that were detected in the corresponding Lane. If there is one or more bit errors in the comparison of RxD[15:0] versus Q[16:1] of the Receive Lane PRBS Register then the error count is incremented by one. (Note that if there are multiple errors in the comparison of one received data word then the Rx Lane Word Error Count is incremented by only one count.) The Rx Lane Word Error Count saturates at 255, so if more than 255 errors are detected then the count stops at 255 and will not roll-over to zero. The word error count is reset to zero at the transition from low-power to high-speed mode (the LP-001 to LP-000 transition), and any detected word errors are counted beginning at the first De-Mapper output word of the Packet Data field following the Sync Word field.

The Rx Lane Word Count described below is a 48-bit integer value. The Rx Lane Word Count is recorded by the receiver because the duration of the high-speed data is controlled by an enable/disable bit in the

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Tx_Global_Configuration_Register. Knowing the word count makes it possible to accurately compute the word error rate or symbol error rate. The Rx Lane Word Count word count is sufficiently large to perform an error rate test at 2.5Gsps for slightly more than 9 days. A single word error over this maximum test interval corresponds to a symbol error rate of about $5 \cdot 10^{-16}$. If there are any symbol errors that cause missing symbol clocks then the word count will be reduced by 1/7th of a word for each such occurrence, and the error count will most likely saturate in that instance, so the calculated error rate would not be meaningful. It is anticipated that even with such a large word counter, the symbol error rates and word error rates will not be measurable unless the signal amplitude or channel conditions are degraded beyond the required limits specified in this document. If symbol errors are counted to determine the symbol error rate, then it is necessary to multiply the word count by 7 to know the symbol count for the symbol error rate calculation:

$$symbol\_error\_rate = symbol\_error\_count/(word\_count \cdot 7)$$

All 48 bits of the Rx Lane Word Count are reset to zero on the transition from low-power mode to high-speed mode (on the transition from LP-001 to LP-000). The Rx Lane Word Count can be read after the transition back to low-power mode (following the transition from LP-000 to LP-111). If the Rx Lane Word Count is read during the error rate measurement test in high-speed mode then the count can contain an invalid result, depending on the implementation of the word count read circuit.

12.4.9 RLRn_Word_Error_Count

read-only, Address: Rx_Lane_n_Base + 6

The Rx Lane n Word Error Count is a count of the number of word errors that were detected in the corresponding Lane.

[7:0] – RLRn_Word_Error_Count	Rx Lane Word Error Count

12.4.10 RLRn_Word_Count_0

read-only, Address: Rx_Lane_n_Base + 7

Rx Lane n Word Count 0 consists of bits 7 through 0 of the 48-bit Rx Lane Word Count value.

[7:0] – RLRn_Word_Count_0	Rx Lane Word Count[7:0]

12.4.11 RLRn_Word_Count_1

read-only, Address: Rx_Lane_n_Base + 8

Rx Lane n Word Count 1 consists of bits 15 through 8 of the 48-bit Rx Lane Word Count value.

[7:0] – RLRn_Word_Count_1	Rx Lane Word Count[15:8]

12.4.12 RLRn_Word_Count_2

read-only, Address: Rx_Lane_n_Base + 9

Rx Lane n Word Count 2 consists of bits 23 through 16 of the 48-bit Rx Lane Word Count value.

[7:0] – RLRn_Word_Count_2	Rx Lane Word Count[23:16]

12.4.13 RLRn_Word_Count_3

read-only, Address: Rx_Lane_n_Base + 10

Rx Lane n Word Count 3 consists of bits 31 through 24 of the 48-bit Rx Lane Word Count value.

[7:0] – RLRn_Word_Count_3	Rx Lane Word Count[31:24]

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12.4.14 RLRn_Word_Count_4

read-only, Address: Rx_Lane_n_Base + 11

Rx Lane n Word Count 4 consists of bits 39 through 32 of the 48-bit Rx Lane Word Count value.

[7:0] – RLRn_Word_Count_4	Rx Lane Word Count[39:32]

12.4.15 RLRn_Word_Count_5

read-only, Address: Rx_Lane_n_Base + 12

Rx Lane n Word Count 5 consists of bits 47 through 40 of the 48-bit Rx Lane Word Count value.

[7:0] – RLRn_Word_Count_5	Rx Lane Word Count[47:40]

12.4.16 Symbol Error Count and Symbol Error Location Functionality

The symbol error count and symbol error location capabilities might have less value than the other built-in-test capabilities; it may be sufficient to implement only the data generation and word error counting capabilities described above.

To measure the symbol error count it is necessary to duplicate the data generation, Mapping and Encoding functions of the transmitter to create a copy of the transmitted symbol stream. Then the received symbol stream can be compared to the regenerated symbol stream and any differences are counted and can be read via the RLRn_Symbol_Error_Count register. Any errors that result in a slip of the symbol clock will likely cause the symbol error count to saturate immediately following the clock slip event. It is anticipated that this is an extremely unlikely event when the link is operated under the required conditions, but the possibility of this failure is noted so the system designer is aware of it.

The Receive Lane Symbol Error Count is a count of the number of symbol errors that were detected in the corresponding Lane. The Receive Lane Symbol Error Count saturates at 255, so if more than 255 errors are detected then the count stops at 255 and will not roll-over to zero. The Receive Lane Symbol Error Count is reset to zero at the transition from low-power to high-speed mode, and errors are counted beginning at the first symbol of the Packet Data field following the first Sync Word after the low-power to high-speed mode transition.

The Receive Lane 1st Symbol Error Location values are a debug capability that allows the symbol position of the first error in the Packet Data Field to be identified. This is the value of a rather long counter (a 48-bit counter) that identifies the symbol offset of the location of the first symbol error in the Packet Data field.

12.4.17 RLRn_Sym_Error_Count

read-only, Address: Rx_Lane_n_Base + 13

Receive Lane Symbol Error Count is a count of the number of symbol errors that were detected in Lane n.

[7:0] – RLRn_Sym_Error_Count	Receive Lane Symbol Error Count

12.4.18 RLRn_1st_Sym_Err_Loc_0

read-only, Address: Rx_Lane_n_Base + 14

RLRn_1st_Sym_Err_Loc_0 consists of bits 7 through 0 of the 48-bit Receive Lane 1st Symbol Error Location value.

[7:0] – RLRn_1st_Sym_Err_Loc_0	Receive Lane 1st Symbol Error Location[7:0]

12.4.19 RLRn_1st_Sym_Err_Loc_1

read-only, Address: Rx_Lane_n_Base + 15

RLRn_1st_Sym_Err_Loc_1 consists of bits 15 through 8 of the 48-bit Receive Lane 1st Symbol Error Location value.

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[7:0] – RLRn_1st_Sym_Err_Loc_1	Receive Lane 1st Symbol Error Location[15:8]

12.4.20 RLRn_1st_Sym_Err_Loc_2

read-only, Address: Rx_Lane_n_Base + 16

RLRn_1st_Sym_Err_Loc_2 consists of bits 23 through 16 of the 48-bit Receive Lane 1st Symbol Error Location value.

[7:0] – RLRn_1st_Sym_Err_Loc_2	Receive Lane 1st Symbol Error Location[23:16]

12.4.21 RLRn_1st_Sym_Err_Loc_3

read-only, Address: Rx_Lane_n_Base + 17

RLRn_1st_Sym_Err_Loc_3 consists of bits 31 through 24 of the 48-bit Receive Lane 1st Symbol Error Location value.

[7:0] – RLRn_1st_Sym_Err_Loc_3	Receive Lane 1st Symbol Error Location[31:24]

12.4.22 RLRn_1st_Sym_Err_Loc_4

read-only, Address: Rx_Lane_n_Base + 18

RLRn_1st_Sym_Err_Loc_4 consists of bits 39 through 32 of the 48-bit Receive Lane 1st Symbol Error Location value.

[7:0] – RLRn_1st_Sym_Err_Loc_4	Receive Lane 1st Symbol Error Location[39:32]

12.4.23 RLRn_1st_Sym_Err_Loc_5

read-only, Address: Rx_Lane_n_Base + 19

RLRn_1st_Sym_Err_Loc_5 consists of bits 47 through 40 of the 48-bit Receive Lane 1st Symbol Error Location value.

[7:0] – RLRn_1st_Sym_Err_Loc_5	Receive Lane 1st Symbol Error Location[47:40]

12.5 Tx Global Configuration and Status Registers

The Tx Global Configuration and Status Registers have the following definitions:

12.5.1 TGR_Global_Configuration

write-only, Address: Tx_Global_Registers_Base + 0

TGR_Global_Configuration is a register to configure parameters and operate controls that apply to all C-PHY Lanes.

[7:1] – reserved for future use.	
[0] – TGR burst enable/disable	TGR burst enable/disable, starts or stops the high-speed test burst. =0 – Disable sending high-speed test data =1 – Enable sending high-speed test data

12.5.2 Burst Enable/Disable Functionality

When the TGR burst enable/disable bit transitions from 0 to 1, the Lane state machines should transmit LP-001, then LP-000, then Preamble, then Sync Word, then test data is sent in the Packet Data field either from the Tx Lane PRBS Generator or Debug Pattern Generator. The specific data transmitted depends on the values written to the TLRn_Test_Patterns_Select register. The Packet Data field contains only the selected test data and has no high layer protocol packet structure. The selected test data will be sent continuously, as long as the burst enable/disable bit is set to “1”. There is no limit to the length of the Packet Data field when

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test data is being transmitted. The C-PHY Lane circuit begins in the LP-111 state to respond to the 0-to-1 transition of the TGR burst enable/disable bit. If the C-PHY Lane circuit is not in the LP-111 state during the 0-to-1 transition event then the C-PHY lane will ignore the state of the TGR burst enable/disable bit until it returns to the 0 state and has a subsequent 0-to-1 transition when the Lane is in the LP-111 state.

When the TGR burst enable/disable bit transitions from 1 to 0 while sending test data, the Lane state machine causes the Post Sequence (4,4,4,4,4,4,4) to be sent and repeated by the number of times defined in TGR_Post_Length, and then the termination is disabled and the signals return to the LP-111 state. Figure 68 illustrates the functionality resulting from TGR burst enable/disable changing state.

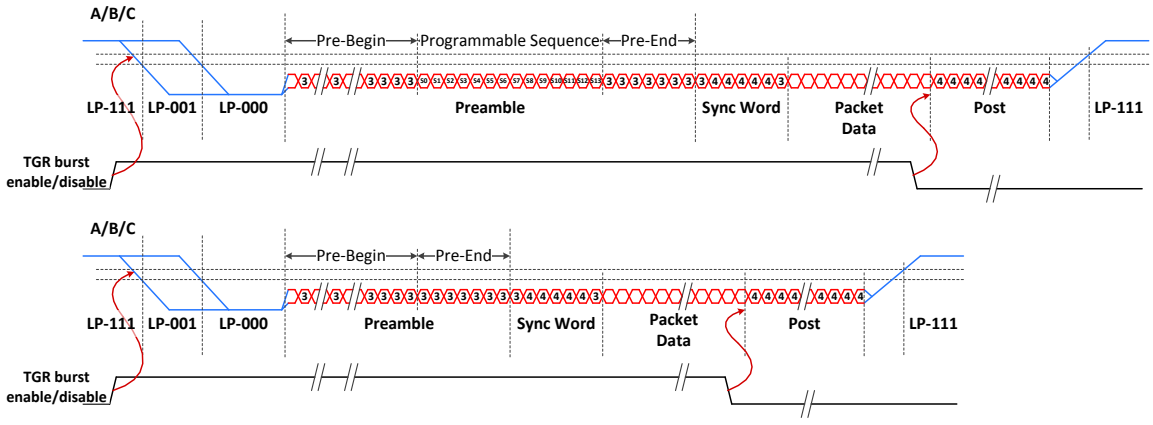

Figure 68 Example Showing Cause/Effect of TGR burst enable/disable

The lane receiver test circuitry contains a word count field that can be read from RLRn_Word_Count_0 through RLRn_Word_Count_5. From this, it is possible to compute the word error rate, or symbol error rate by also reading the word error count and symbol error count values.

Note that there are not specific global registers defined for selection of the PRBS polynomial or PRBS seed value. This allows the PRBS polynomial and seed to be chosen on a per-lane basis. When multiple lanes are tested simultaneously, it is anticipated that the most frequent use will be to select the same PRBS polynomial in all lanes and use a different seed value in each lane so that the transmitted data pattern in each lane is independent of the others.

12.5.3 TGR_Preamble_Length

write-only, Address: Tx_Global_Registers_Base + 1

TGR_Preamble_Length specifies the length of the Preamble and provides a means to enable or disable the Programmable Sequence in the Preamble.

[7] – enable/disable the Preamble Programmable Sequence	enable or disable the Preamble Programmable Sequence, refer to Figure 69 =0 – Disable the Preamble Programmable Sequence, the lower waveforms of Figure 69 =1 – Enable the Preamble Programmable Sequence, the upper waveforms of Figure 69 The default value is 0, which disables the Preamble Programmable Sequence on system reset.
[6] – reserved for future use.	
[5:0] – Begin_Preamble_Length	The number of symbols in the PreBegin section of the preamble is: (Begin_Preamble_Length + 1) · 7

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	The default value is 0x3f or 63, which sets the length of the PreBegin part of the Preamble to 64 Words on system reset.

The PreBegin part of the Preamble may range from 1 to 64 Words, or 7 to 448 symbols.

12.5.4 TGR_Post_Length

write-only, Address: Tx_Global_Registers_Base + 2

TGR_Post_Length specifies the length of the Post field.

[7:5] – reserved for future use.	
[4:0] – Post_Length	The number of symbols in the Post field is: (Post_Length + 1) · 7 The default value is 0x1f or 31, which sets the length of the PreBegin part of the Preamble to 32 Words on system reset.

The Post field may range from 1 to 32 Words, or 7 to 224 symbols.

12.5.5 TGR_Preamble_Prog_Sequence_0,1

write-only, Address: Tx_Global_Registers_Base + 3

TGR_Preamble_Prog_Sequence_0,1 specifies the values of symbols 0 and 1 in the Programmable Sequence portion of the Preamble.

[7:6] – reserved for future use.	
[5:3] – Symbol 1 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.
[2:0] – Symbol 0 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.

12.5.6 TGR_Preamble_Prog_Sequence_2,3

write-only, Address: Tx_Global_Registers_Base + 4

TGR_Preamble_Prog_Sequence_2,3 specifies the values of symbols 2 and 3 in the Programmable Sequence portion of the Preamble.

[7:6] – reserved for future use.	
[5:3] – Symbol 3 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.
[2:0] – Symbol 2 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.

12.5.7 TGR_Preamble_Prog_Sequence_4,5

write-only, Address: Tx_Global_Registers_Base + 5

TGR_Preamble_Prog_Sequence_4,5 specifies the values of symbols 4 and 5 in the Programmable Sequence portion of the Preamble.

[7:6] – reserved for future use.	

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[5:3] – Symbol 5 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.
[2:0] – Symbol 4 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.

12.5.8 TGR_Preamble_Prog_Sequence_6,7

write-only, Address: Tx_Global_Registers_Base + 6

TGR_Preamble_Prog_Sequence_6,7 specifies the values of symbols 6 and 7 in the Programmable Sequence portion of the Preamble.

[7:6] – reserved for future use.	
[5:3] – Symbol 7 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.
[2:0] – Symbol 6 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.

12.5.9 TGR_Preamble_Prog_Sequence_8,9

write-only, Address: Tx_Global_Registers_Base + 7

TGR_Preamble_Prog_Sequence_8,9 specifies the values of symbols 8 and 9 in the Programmable Sequence portion of the Preamble.

[7:6] – reserved for future use.	
[5:3] – Symbol 9 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.
[2:0] – Symbol 8 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.

12.5.10 TGR_Preamble_Prog_Sequence_10,11

write-only, Address: Tx_Global_Registers_Base + 8

TGR_Preamble_Prog_Sequence_10,11 specifies the values of symbols 10 and 11 in the Programmable Sequence portion of the Preamble.

[7:6] – reserved for future use.	
[5:3] – Symbol 11 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.
[2:0] – Symbol 10 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.

12.5.11 TGR_Preamble_Prog_Sequence_12,13

write-only, Address: Tx_Global_Registers_Base + 9

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1582 TGR_Preamble_Prog_Sequence_12,13 specifies the values of symbols 12 and 13 in the Programmable
1583 Sequence portion of the Preamble.

[7:6] – reserved for future use.	
[5:3] – Symbol 13 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.
[2:0] – Symbol 12 of the Preamble Programmable Sequence	=0 to 4 – symbol value =5 to 7 – invalid value, not a valid symbol value. The default value is 3 on system reset.

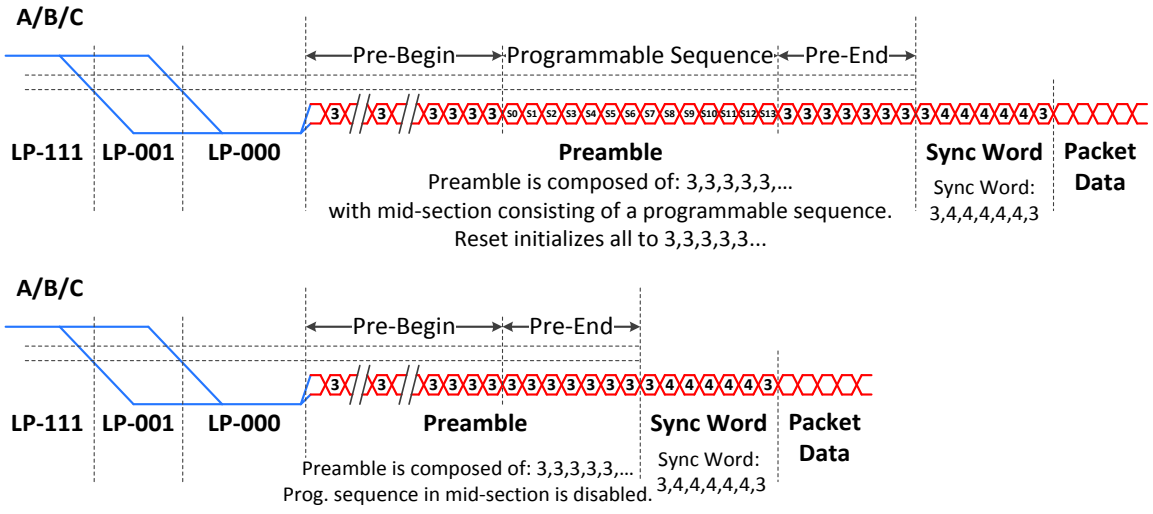

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Figure 69 Preamble Programmable Sequence, Showing Bit Order, and Enabled/Disabled

12.6 Rx Global Configuration and Status Registers

1585 There are no anticipated needs for Rx Global Configuration and Status Registers.

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Annex A Logical PHY-Protocol Interface Description (informative)

The PHY-Protocol Interface (PPI) is used to make a connection between the PHY lane modules and the higher protocol layers of a communication stack. The interface described here is intended to be generic and application independent.

This annex is informative only. Conformance to the C-PHY specification does not depend on any portion of the PPI defined herein. Because of that, this section avoids normative language and does not use words like "shall" and "should." Instead, present tense language has been used to describe the PPI, utilizing words like "is" and "does." The reader may find it helpful to consider this appendix to be a description of an example implementation, rather than a specification.

This PPI is optimized for controlling a C-PHY and transmitting and receiving parallel data. The interface described here is defined as an on-chip connection, and does not attempt to minimize signal count or define timing parameters or voltage levels for the PPI signals.

A.1 Signal Description

Table 35 defines the signals used in the PPI. For a PHY with multiple lanes, a set of PPI signals is used for each Lane. Each signal has been assigned into one of six categories: high-speed transmit signals, high-speed receive signals, escape mode transmit signals, escape mode receive signals, control signals, and error signals. Bi-directional high-speed lanes with support for bi-directional escape mode include nearly all of the signals listed in the table. unidirectional lanes include only a subset of the signals. The direction of each signal is listed as "I" or "O". Signals with the direction "I" are PHY inputs, driven from the protocol layer. Signals with the direction "O" are PHY outputs, driven to the protocol layer. For this logical interface, most clocks are described as being generated outside the PHY, although any specific PHY may implement the clock circuit differently.

The "Categories" column in Table 35 indicates for which lane module types each signal applies. The category names are described in Table 2 and are summarized here for convenience. Each category is described using a four-letter acronym, defined as [Side, HS-capabilities, Escape-Forward, Escape- Reverse]. The first letter, Side, can be M (Master) or S (Slave). The second letter, high-speed capabilities, can be F (forward data) only. The third and fourth letters indicate escape mode capability in the forward and reverse directions, respectively. The third letter can be A (All) or E (Events – Triggers and ULPS only), while the fourth letter can be A (All, including LPDT), E (Events, triggers and ULPS only), Y (Any but not None: so A or E) or N (None). Any of the four identification letters can be replaced by an X, to indicate that each of the available options is appropriate.

Table 35 PPI Signals

Symbol	Dir	Categories	Description
High-Speed Transmit Signals			
TxSymbolClkHS	I	MFXX	Lane High-Speed Transmit Symbol Clock. This clock provides the timing used to transmit high-speed symbol data over the lane interconnect. All lanes may use the same TxSymbolClkHS clock signal, or any subset of lanes down to a single lane may use a TxSymbolClkHS. Lanes may use different TxSymbolClkHS clocks as long as the inter-lane skew requirement is met.

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Symbol	Dir	Categories	Description
TxWordClkHS	I	MFXX	High-Speed Transmit Word Clock. This is used to synchronize PPI signals in the high-speed transmit clock domain. It is recommended that all transmitting lane modules share one TxWordClkHS signal. The frequency of TxWordClkHS is exactly 1/7 the high-speed symbol rate.
TxDataHS[15:0]	I	MFXX	High-Speed Transmit Data. Sixteen-bit high-speed data to be transmitted. The signal connected to TxDataHS[0] is associated with bit 0 of the C-PHY Mapping function. Data is captured on rising edges of TxWordClkHS.
TxSendSyncHS	I	MFXX	High Speed Command to Transmit Sync Word. The protocol adapter attached to the C-PHY may need to transmit Sync Words to separate multiple copies of a packet header. This command signal has the same timing as TxDataHS[15:0] on the PPI, but when TxSendSyncHS is active on a given TxWordClkHS cycle then TxDataHS[15:0] is ignored for any Word Clock cycle where TxSendSyncHS is active.
TxRequestHS	I	MFXX	High-Speed Transmit Request and Data Valid. A low-to-high transition on TxRequestHS causes the lane module to initiate a Start-of-Transmission sequence. A high-to-low transition on TxRequest causes the lane module to initiate an End-of-Transmission sequence. This active high signal also indicates that the protocol layer is driving valid data on TxDataHS to be transmitted. The lane module accepts the data when both TxRequestHS and TxReadyHS are active on the same rising TxWordClkHS clock edge. The protocol layer always provides valid transmit data when TxRequestHS is active. Once asserted, TxRequestHS remains high until the data has been accepted, as indicated by TxReadyHS. TxRequestHS is only asserted while TxRequestEsc is low.
TxReadyHS	O	MFXX	High-Speed Transmit Ready. This active high signal indicates that TxDataHS is accepted by the lane module to be serially transmitted. TxReadyHS is valid on rising edges of TxWordClkHS.
High-Speed Receive Signals			
RxWordClkHS	O	SFXX	High-Speed Receive Word Clock. This is used to synchronize signals in the high-speed receive clock domain. The RxWordClkHS is generated by dividing the recovered high-speed clock.
RxDataHS[15:0]	O	SFXX	High-Speed Receive Data. Sixteen-bit high-speed data received by the lane module. The signal connected to RxDataHS[0] is associated with bit 0 of the C-PHY De-Mapping function. Data is transferred on rising edges of RxWordClkHS.

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Symbol	Dir	Categories	Description
RxInvalidCodeHS	O	SFXX	High-Speed Invalid Code Word Detection. A high-speed status signal that indicates the present word on RxDataHS[15:0] was produced by a group of seven symbols that were not a valid code word. This is an indication that the data word being output has a low confidence of being correct. RxInvalidCodeHS is not active when either the Sync Word or the Post Pattern is presented to the De-Mapper.
RxValidHS	O	SFXX	High-Speed Receive Data Valid. This active high signal indicates that the lane module is driving data to the protocol layer on the RxDataHS output. There is no “RxReadyHS” signal, and the protocol layer is expected to capture RxDataHS on every rising edge of RxWordClkHS where RxValidHS is asserted. There is no provision for the protocol layer to slow down (“throttle”) the receive data.
RxActiveHS	O	SFXX	High-Speed Reception Active. This active high signal indicates that the lane module is actively receiving a high-speed transmission from the Lane interconnect.
RxSyncHS	O	SFXX	Receiver Synchronization Observed. This active high signal indicates that the lane module has detected the 7-symbol sync word in the received data. In a typical high-speed transmission, RxSyncHS is high for one cycle of RxWordClkHS at the beginning of a high-speed transmission when RxActiveHS is first asserted, and also prior to redundant packet headers that may appear in the data burst.
Escape Mode Transmit Signals			
TxClkEsc	I	MXXX SXXY	Escape mode Transmit Clock. This clock is directly used to generate escape sequences. The period of this clock determines the phase times for low-power signals as defined in Section 6.6.2. It is therefore constrained by the normative part of the C-PHY specification. See Section 9. Note that this clock is used to synchronize TurnRequest and is included for any module that supports bi-directional high-speed operation, even if that module does not support transmit or bidirectional escape mode.
TxRequestEsc	I	MXXX SXXY	Escape mode Transmit Request. This active high signal, asserted together with exactly one of TxLpdtEsc, TxUlpsEsc, or one bit of TxTriggerEsc, is used to request entry into escape mode. Once in escape mode, the Lane stays in escape mode until TxRequestEsc is de-asserted. TxRequestEsc is only asserted by the protocol layer while TxRequestHS is low.

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Symbol	Dir	Categories	Description
TxLpdtEsc	I	MXAX SXXA	Escape mode Transmit Low-Power Data. This active high signal is asserted with TxRequestEsc to cause the lane module to enter low-power data transmission mode. The lane module remains in this mode until TxRequestEsc is de-asserted. TxUlpsEsc and all bits of TxTriggerEsc are low when TxLpdtEsc is asserted.
TxUlpsExit	I	MXXX SXXY	Transmit ULP Exit Sequence. This active high signal is asserted when ULP state is active and the protocol layer is ready to leave ULP state. The PHY leaves ULP state and begins driving Mark-1 after TxUlpsExit is asserted. The PHY later drives the Stop state (LP-111) when TxRequestEsc is deasserted. TxUlpsExit is synchronous to TxClkEsc. This signal is ignored when the Lane is not in the ULP State.
TxUlpsEsc	I	MXXX SXXY	Escape mode Transmit Ultra-Low Power State. This active high signal is asserted with TxRequestEsc to cause the lane module to enter the Ultra-Low Power State. The lane module remains in this mode until TxRequestEsc is de-asserted. TxLpdtEsc and all bits of TxTriggerEsc are low when TxUlpsEsc is asserted.
TxTriggerEsc[3:0]	I	MXXX SXXY	Escape mode Transmit Trigger 0-3. One of these active high signals is asserted with TxRequestEsc to cause the associated Trigger to be sent across the Lane interconnect. In the receiving lane module, the same bit of RxTriggerEsc is then asserted and remains asserted until the Lane interconnect returns to Stop state, which happens when TxRequestEsc is de-asserted at the transmitter. Only one bit of TxTriggerEsc is asserted at any time, and only when TxLpdtEsc and TxUlpsEsc are both low.
TxDataEsc[7:0]	I	MXAX SXXA	Escape mode Transmit Data. This is the eight bit escape mode data to be transmitted in low-power data transmission mode. The signal connected to TxDataEsc[0] is transmitted first. Data is captured on rising edges of TxClkEsc.
TxValidEsc	I	MXAX SXXA	Escape mode Transmit Data Valid. This active high signal indicates that the protocol layer is driving valid data on TxDataEsc to be transmitted. The lane module accepts the data when TxRequestEsc, TxValidEsc and TxReadyEsc are all active on the same rising TxClkEsc clock edge.
TxReadyEsc	O	MXAX SXXA	Escape mode Transmit Ready. This active high signal indicates that TxDataEsc is accepted by the lane module to be serially transmitted. TxReadyEsc is valid on rising edges of TxClkEsc.

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Symbol	Dir	Categories	Description
Escape Mode Receive Signals			
RxClkEsc	O	MXXY SXXX	Escape mode Receive Clock. This signal is used to transfer received data to the protocol layer during escape mode. This “clock” is generated from the two low-power signals in the Lane interconnect. Because of the asynchronous nature of escape mode data transmission, this “clock” may not be periodic.
RxLpdtEsc	O	MXXA SXAX	Escape Low-Power Data Receive mode. This active high signal is asserted to indicate that the lane module is in low-power data receive mode. While in this mode, received data bytes are driven onto the RxDataEsc output when RxValidEsc is active. The lane module remains in this mode with RxLpdtEsc asserted until a Stop state is detected on the Lane interconnect.
RxUlpsEsc	O	MXXY SXXX	Escape Ultra-Low Power (Receive) mode. This active high signal is asserted to indicate that the lane module has entered the Ultra-Low Power State. The lane module remains in this mode with RxUlpsEsc asserted until a Stop state is detected on the Lane interconnect.
RxTriggerEsc[3:0]	O	MXXY SXXX	Escape mode Receive Trigger 0-3. These active high signals indicate that a trigger event has been received. The asserted RxTriggerEsc signal remains active until a Stop state is detected on the Lane interconnect.
RxDataEsc[7:0]	O	MXXA SXAX	Escape mode Receive Data. This is the eight-bit escape mode low-power data received by the lane module. The signal connected to RxDataEsc[0] was received first. Data is transferred on rising edges of RxClkEsc.
RxValidEsc	O	MXXA SXAX	Escape mode Receive Data Valid. This active high signal indicates that the lane module is driving valid data to the protocol layer on the RxDataEsc output. There is no “RxReadyEsc” signal, and the protocol layer is expected to capture RxDataEsc on every rising edge of RxClkEsc where RxValidEsc is asserted. There is no provision for the protocol layer to slow down (“throttle”) the receive data.
Control Signals			
TurnRequest	I	XRXX XFXY	Turn Around Request. This active high signal is used to indicate that the protocol layer desires to turn the Lane around, allowing the other side to begin transmission. TurnRequest is valid on rising edges of TxClkEsc. TurnRequest is only meaningful for a lane module that is currently the transmitter (Direction=0). If the lane module is in receive mode (Direction=1), this signal is ignored.

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Symbol	Dir	Categories	Description
Direction	O	XRXX XFXY	Transmit/Receive Direction. This signal is used to indicate the current direction of the Lane interconnect. When Direction=0, the Lane is in transmit mode (0=Output). When Direction=1, the Lane is in receive mode (1=Input).
TurnDisable	I	XRXX XFXY	Disable Turn-around. This signal is used to prevent a (bi-directional) Lane from going into transmit mode – even if it observes a turn-around request on the Lane interconnect. This is useful to prevent a potential “lock-up” situation when a unidirectional lane module is connected to a bidirectional lane module.
ForceRxmode	I	MRXX MXXY SXXX	Force Lane Module Into Receive mode / Wait for Stop state. This signal allows the protocol layer to initialize a lane module, or force a bi-directional lane module, into receive mode. This signal is used during initialization or to resolve a contention situation. When this signal is high, the lane module immediately transitions into receive control mode and waits for a Stop state to appear on the Lane interconnect. When used for initialization, this signal is released, i.e. driven low, only when the Dp & Dn inputs are in Stop state for time t_{INIT}, or longer.
ForceTxStopmode	I	MXXX SRXX SXXY	Force Lane Module Into Transmit mode / Generate Stop state. This signal allows the protocol layer to force a lane module into transmit mode and Stop state during initialization or following an error situation, e.g. expired time out. When this signal is high, the lane module immediately transitions into transmit mode and the module state machine is forced into the Stop state.
Stopstate	O	XXXX	Lane is in Stop state. This active high signal indicates that the lane module, regardless of whether the lane module is a transmitter or a receiver, is currently in Stop state. Note that this signal is asynchronous to any clock in the PPI interface. Also, the protocol layer may use this signal to indirectly determine if the PHY line levels are in the LP-111 state.
Enable	I	XXXX	Enable Lane Module. This active high signal forces the lane module out of “shutdown”. All line drivers, receivers, terminators, and contention detectors are turned off when Enable is low. Furthermore, while Enable is low, all other PPI inputs are ignored and all PPI outputs are driven to the default inactive state. Enable is a level sensitive signal and does not depend on any clock.

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Symbol	Dir	Categories	Description
UlpsActiveNot	O	XXXX	ULP State (not) Active. This active low signal is asserted to indicate that the Lane is in ULP state. For a transmitter, this signal is asserted sometime after TxUlpsEsc and TxRequestEsc are asserted. The transmitting PHY continues to supply TxClkEsc until UlpsActiveNot is asserted. In order to leave ULP state, the transmitter first drives TxUlpsExit high, then waits for UlpsActiveNot to become high (inactive). At that point, the transmitting PHY is active and has started transmitting a Mark-1 on the lines. The protocol layer waits for time t_{wakeup} and then drives TxRequestEsc inactive to return the Lane to Stop state. For a receiver, this signal indicates that the Lane is in ULP state. At the beginning of ULP state, UlpsActiveNot is asserted together with RxUlpsEsc. At the end of the ULP state, this signal becomes inactive to indicate that the Mark-1 state has been observed. Later, after a period of time t_{wakeup}, the RxUlpsEsc signal is deasserted.
Error Signals			
ErrSotHS	O	MRXX SXXX	Start-of-Transmission (SoT) Error. If the high-speed SoT Sync Word is corrupted, by having the least-significant symbol of the 3444443 pattern not equal to 3, this active high signal is asserted for one cycle of RxWordClkHS. This is considered to be a “soft error” in the Sync Word and confidence in the payload data is reduced.
ErrSotSyncHS	O	MRXX SXXX	Start-of-Transmission Synchronization Error. If the high-speed SoT Sync Word is corrupted in a way that proper synchronization cannot be expected, this active high signal is asserted for one cycle of RxWordClkHS. (Considered optional, this is an extremely low-probability event.)
ErrEsc	O	MXXY SXXX	Escape Entry Error. If an unrecognized escape entry command is received, this active high signal is asserted and remains asserted until the next change in line state.
ErrSyncEsc	O	MXXA SXAX	Low-Power Data Transmission Synchronization Error. If the number of bits received during a low-power data transmission is not a multiple of eight when the transmission ends, this active high signal is asserted and remains asserted until the next change in line state.
ErrControl	O	MXXY SXXX	Control Error. This active high signal is asserted when an incorrect line state sequence is detected. For example, if a turn-around request or escape mode request is immediately followed by a Stop state instead of the required Bridge state, this signal is asserted and remains asserted until the next change in line state.

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Symbol	Dir	Categories	Description
ErrContentionLP0	O	MXXX SXXY	LP0 Contention Error. This active high signal is asserted when the lane module detects a contention situation on a line while trying to drive the line low.
ErrContentionLP1	O	MXXX SXXY	LP1 Contention Error. This active high signal is asserted when the lane module detects a contention situation on a line while trying to drive the line high.

A.2 High-Speed Transmit from the Master Side

Figure 70 shows an example of a high-speed transmission on the master side. While TxRequestHS is low, the lane module ignores the value of TxDataHS. To begin transmission, the protocol layer drives TxDataHS with the first word of data and asserts TxRequestHS. This data word is accepted by the PHY on the first rising edge of TxWordClkHS with TxReadyHS also asserted. At this point, the protocol logic drives the next data word onto TxDataHS. After every rising clock cycle with TxReadyHS active, the protocol layer supplies a new valid data word or ends the transmission. After the last data word has been transferred to the lane module, TxRequestHS is driven low to cause the lane module to stop the transmission and enter Stop state. The minimum number of words transmitted could be as small as one.

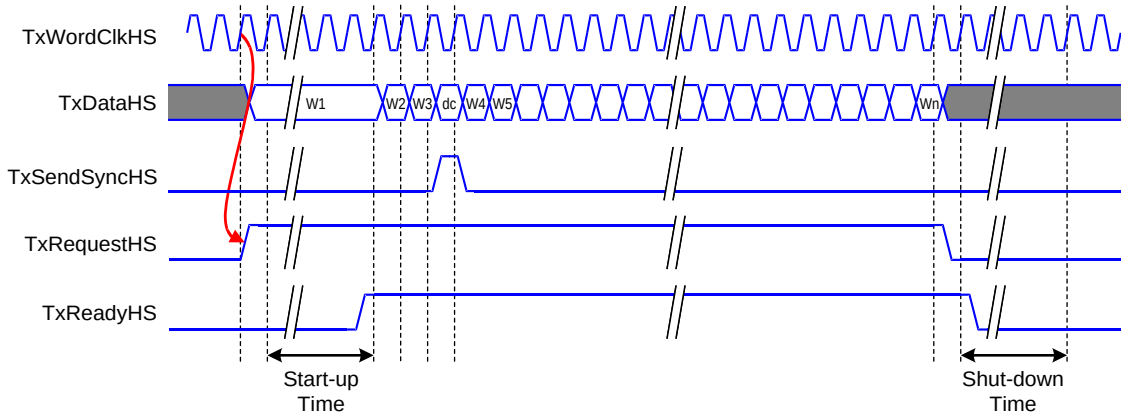

Figure 70 Example High-Speed Transmission from the Master Side

A.3 High-Speed Receive at the Slave Side

Figure 71 shows an example of a high-speed reception at the slave side. The RxActiveHS signal indicates that a receive operation is occurring. A normal reception starts with a pulse on RxSyncHS followed by valid receive data on subsequent cycles of RxWordClkHS. Note that the protocol layer is prepared to receive all of the data. There is no method for the receiving protocol to pause or slow data reception.

If EoT Processing is performed inside the PHY, the RxActiveHS and RxValidHS signals transition low following the last valid data word, Wn. Refer to Figure 71.

If EoT processing is not performed in the PHY, one or more additional words are presented after the last valid data word. The first of these additional words, shown as word “C” in Figure 71, is all ones or all zeros. Subsequent words may or may not be present, and can have any value. For a PHY that does not perform EoT processing, the RxActiveHS and RxValidHS signals transition low simultaneously sometime after word “C” is received. Once these signals have transitioned low, they remain low until the next high-speed data reception begins.

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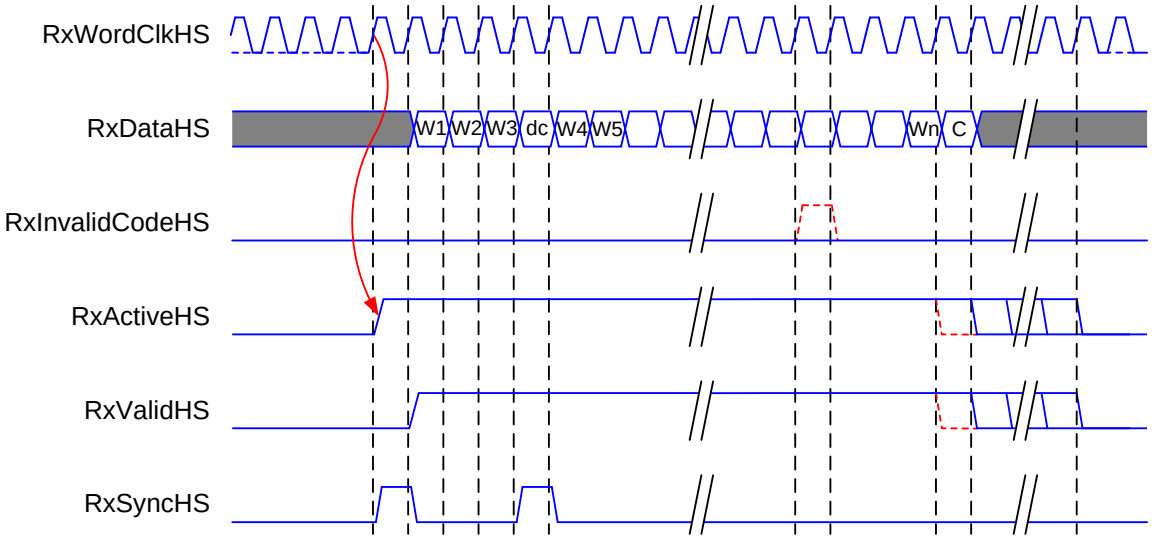

Figure 71 Example High-Speed Receive at the Slave Side

For D-PHY PPI compatibility, it is recommended that RxWordClkHS toggle continuously while the high-speed signal is present. An option shown in the waveform above is to prevent RxWordClk from toggling while RxActiveHS is inactive.

A.4 (Not Used)

Note:

This section is null for the C-PHY Specification. The section heading has been retained in order to synchronize section numbering with the D-PHY Specification [MIPI01].

A.5 (Not Used)

Note:

This section is null for the C-PHY Specification. The section heading has been retained in order to synchronize section numbering with the D-PHY Specification [MIPI01].

A.6 Low-Power Data Transmission

Furthermore, while the high-speed interface signal TxRequestHS serves as both a transmit request and a data valid signal, on the low-power interface two separate signals are used. The protocol layer directs the Lane to enter low-power data transmission escape mode by asserting TxRequestEsc with TxLpdtEsc high. The low-power transmit data is transferred on the TxDataEsc lines when TxValidEsc and TxReadyEsc are both active at a rising edge of TxClkEsc. The byte is transmitted in the time after the TxDataEsc is accepted by the lane module (TxValidEsc = TxReadyEsc = high) and therefore the TxClkEsc continues running for some minimum time after the last byte is transmitted. The protocol layer knows the byte transmission is finished when TxReadyEsc is asserted. After the last byte has been transmitted, the protocol layer de-asserts TxRequestEsc to end the low-power data transmission. This causes TxReadyEsc to return low, after which the TxClkEsc clock is no longer needed. Whenever TxRequestEsc transitions from high-to-low, it always remains in the low state for a minimum of two TxClkEsc clock cycles. Figure 72 shows an example low-power data transmission operation.

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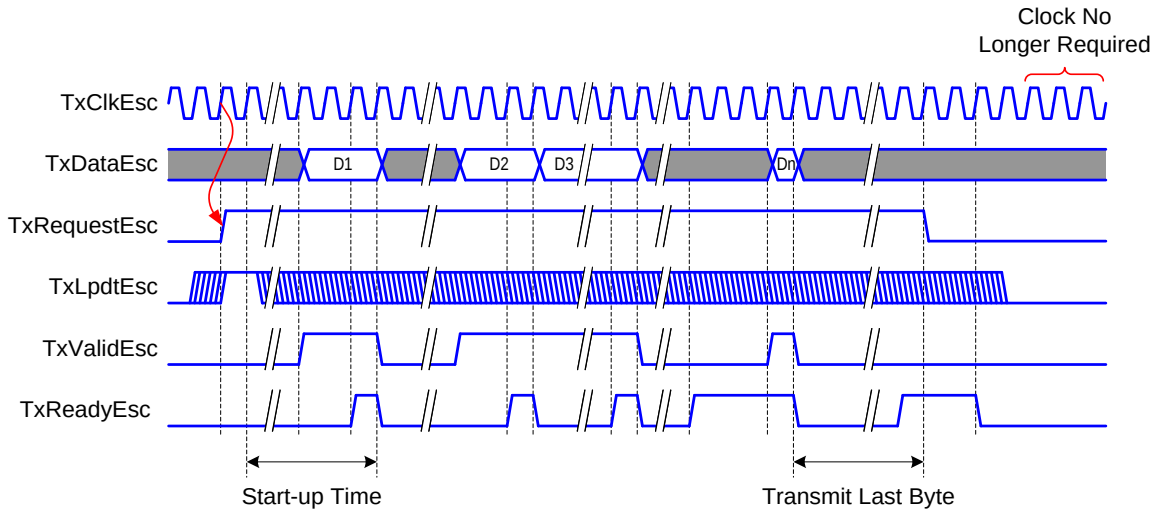

Figure 72 Low-Power Data Transmission

A.7 Low-Power Data Reception

Figure 73 shows an example low-power data reception. In this example, a low-power escape "clock" is generated from the lane interconnect by the logical exclusive-OR of the "A" and "C" signals. This "clock" is used within the lane module to capture the transmitted data. In this example, the "clock" is also used to generate RxClkEsc.

The signal RxLpdtEsc is asserted when the escape entry command is detected and stays high until the Lane returns to the Stop state, indicating that the transmission has finished. It is important to note that because of the asynchronous nature of escape mode transmission, the RxClkEsc signal can stop at any time in either the high or low state. This is most likely to happen just after a byte has been received, but it could happen at other times as well.

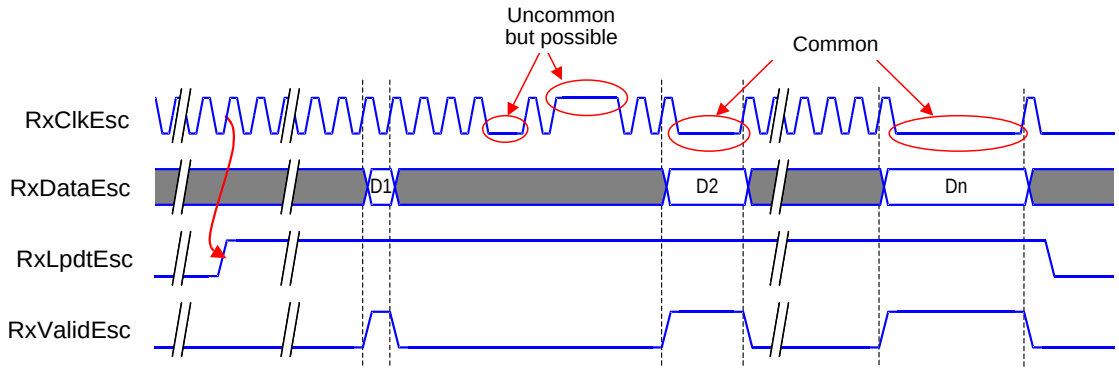

Figure 73 Example Low-Power Data Reception

A.8 Turn-around

If the master side and slave side lane modules are both bi-directional, it is possible to turn around the link for high-speed and/or escape mode signaling. Section 6.5 explains how it is determined which side is allowed to transmit by passing a "token" back and forth. That is, the side currently transmitting passes the token to the receiving side. If the receiving side acknowledges the turn-around request, as indicated by driving the appropriate line state, the direction is switched.

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Figure 74 shows an example of two turn-around events. At the beginning, the local side is the transmitter, as shown by Direction=0. When the protocol layer on this side wishes to turn the Lane around (i.e. give the token to the other side), it asserts TurnRequest for at least one cycle of TxClkEsc. This initiates the turn-around procedure. The remote side acknowledges the turn-around request by driving the appropriate states on the lines. When this happens, the local Direction signal changes from transmit (0) to receive (1).

Later in the example of Figure 62, the remote side initiates a turn-around request, passing the token back to the local side. When this happens, the local Direction signal changes back to transmit (0). Note that there is no prescribed way for a receiver to request access to the link. The current transmitter is in control of the link direction and decides when to turn the link around, passing control to the receiver.

If the remote side does not acknowledge the turn-around request, the Direction signal does not change.

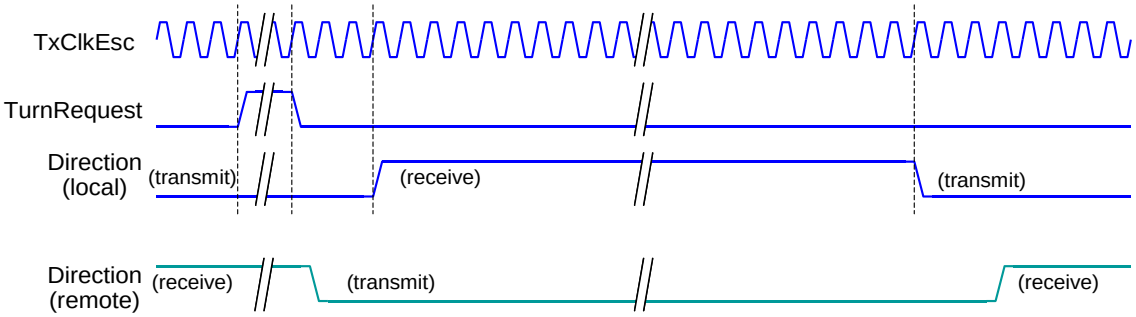

Figure 74 Example Turn-around Actions Transmit-to-Receive and Back to Transmit

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Annex B Interconnect Design Guidelines (informative)

B.1 Practical Distances

The maximum Lane flight time is defined at two nanoseconds. Assuming less than 100ps wiring delay within the RX-TX modules each, the physical distance that can be bridged with external interconnect is around 54cm/√ε. For most practical PCB and flex materials this corresponds to maximum distances around 25-30 cm.

B.2 RF Frequency Bands: Interference

The most common concern is the case where emissions from the interface are in the same frequency band as the wireless signal, and the emissions act as a jammer that degrades reception of the intended signal at the wireless receiver. The path of this interference is illustrated in Figure 75.

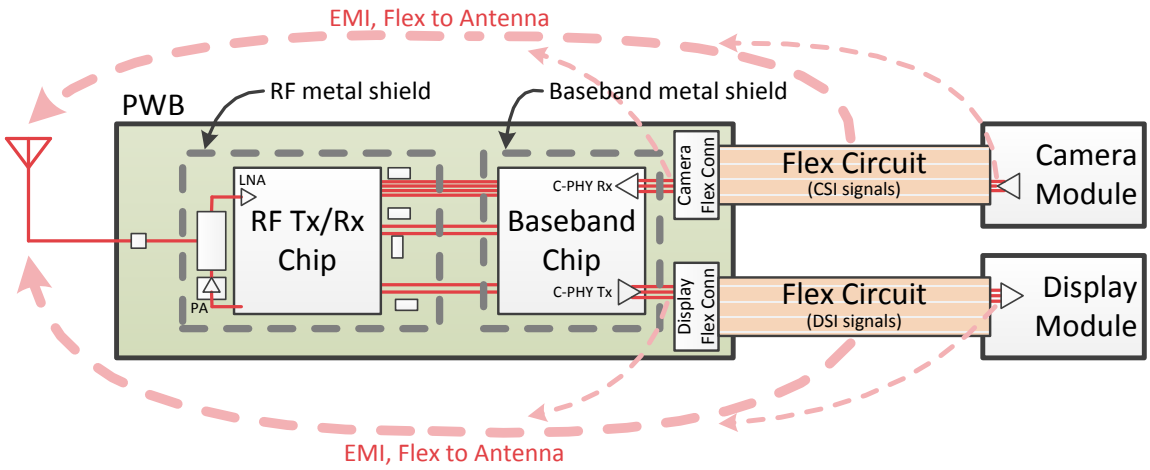

Figure 75 Radio Interference from Serial Interface Connections

The reverse of this path is also a possible concern, where a signal transmitted by the wireless transceiver is coupled to the serial interface signals in such a manner that it cannot be rejected by the common mode rejection capability of the serial interface receiver. It is also possible that the signal transmitted by the wireless transceiver is coupled in a manner that it produces an unintended differential mode signal at the serial interface receiver. Specific concerns are described below.

B.2.1 Specific Recommendations Regarding EMI and EMC

In terms of sensitivity:

- RX (downlink) is more of concern than TX (but TX might have to be considered for EMC)
- GNSS systems are almost always at sensitivity level (it is rare to get close to a satellite!) => they are the priority for EMI design
- In order of sensitivity: GNSS > Cellular > Connectivity
- Wide band systems (WCDMA/LTE/WiFi) are less sensitive to clock spurs than narrow band systems (GSM/Bluetooth/FM)

EMI design of MIPI interfaces

- Clock forwarded system (D-PHY) should avoid clock and its harmonics to fall in GNSS system bands then when feasible it should also avoid GSM bands (2, 3, 5, 8) and Bluetooth (although with frequency hopping Bluetooth is relatively robust), WCDMA, LTE and WiFi bands are less of a concern

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- For others (C-PHY/M-PHY) when frequency is low enough it should try to have a null in GNSS bands
- Noise whitening techniques are essential for data lanes to avoid energy to peak in undesired bands (note though that even for CSI and DSI that data is pretty random)

Implication for current specs

- Most bands being covered by first lobe of interface, slew control as very little benefit for interface > 1.5Gbps/GSs/lane
- Above G1 M-PHY has no real need to keep fixed frequencies for gears

Table 36 Cellular Bands Used by Mobile Devices

Band	Downlink MS RX (EMI)		Uplink MS TX (EMC)		Duplex	Common Name / region
	F_{low}	F_{high}	F_{low}	F_{high}		
Band 1	2110.0	2170.0	1920.0	1980.0	FDD	IMT / EU-Asia
Band 2	1930.0	1990.0	1850.0	1910.0	FDD	PCS / US
Band 3	1805.0	1880.0	1710.0	1785.0	FDD	DCS /EU-Asia
Band 4	2110.0	2155.0	1710.0	1755.0	FDD	AWS-1 / US
Band 5	869.0	894.0	824.0	849.0	FDD	CLR / US
Band 6	875.0	885.0	830.0	840.0	FDD	UMTS 800 / Japan
Band 7	2620.0	2690.0	2500.0	2570.0	FDD	IMT / EU
Band 8	925.0	960.0	880.0	915.0	FDD	E-GSM / EU-Asia
Band 9	1844.9	1879.9	1749.9	1784.9	FDD	UMTS 1700 / Japan DCS
Band 10	2110.0	2170.0	1710.0	1770.0	FDD	Extended AWS / US
Band 11	1475.9	1495.9	1427.9	1447.9	FDD	Lower PDC / Japan
Band 12	729.0	746.0	699.0	716.0	FDD	Lower SMH blocks A,B,C / US
Band 13	746.0	756.0	777.0	787.0	FDD	Upper SMH block C / US
Band 14	758.0	768.0	788.0	798.0	FDD	Upper SMH block D / US
Band 15	2600.0	2620.0	1900.0	1920.0	FDD	Reserved
Band 16	2585.0	2600.0	2010.0	2025.0	FDD	Reserved
Band 17	734.0	746.0	704.0	716.0	FDD	Lower SMH blocks B,C / US
Band 18	860.0	875.0	815.0	830.0	FDD	lower 800 / Japan
Band 19	875.0	890.0	830.0	845.0	FDD	upper 800 / Japan
Band 20	791.0	821.0	832.0	862.0	FDD	Digital Dividend / EU
Band 21	1495.9	1510.9	1447.9	1462.9	FDD	Upper PDC / Japan
Band 22	3510.0	3590.0	3410.0	3490.0	FDD	
Band 23	2180.0	2200.0	2000.0	2020.0	FDD	S-Band
Band 24	1525.0	1559.0	1626.5	1660.5	FDD	L-Band
Band 25	1930.0	1995.0	1850.0	1915.0	FDD	Extended PCS / US
Band 26	859.0	894.0	814.0	849.0	FDD	Extended CLR / US
Band 27	852.0	869.0	807.0	824.0	FDD	SMR
Band 28	758.0	803.0	703.0	748.0	FDD	/ APAC
Band 29	716.0	728.0	n/a	n/a	FDD	Lower SMH blocks D,E / US

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Band	Downlink MS RX (EMI)		Uplink MS TX (EMC)		Duplex	Common Name / region
	F_{low}	F_{high}	F_{low}	F_{high}		
Band 30	2350.0	2360.0	2305.0	2315.0	FDD	WCS blocks A,B / US
Band 31	462.5	467.5	452.5	457.5	FDD	
AWS-2	1995.0	2000.0	1915.0	1920.0	FDD	AWS-2 / US
AWS-3	2155.0	2180.0	1755.0	1780.0	FDD	AWS-3 / US
Band iDEN	851.0	869.0	806.0	824.0	FDD	iDEN / US
Band 33	1900.0	1920.0	1900.0	1920.0	TDD	IMT / China
Band 34	2010.0	2025.0	2010.0	2025.0	TDD	IMT / China
Band 35	1850.0	1910.0	1850.0	1910.0	TDD	PCS (Uplink) / US
Band 36	1930.0	1990.0	1930.0	1990.0	TDD	PCS (Downlink) / US
Band 37	1910.0	1930.0	1910.0	1930.0	TDD	PCS (Duplex spacing) / US
Band 38	2570.0	2620.0	2570.0	2620.0	TDD	IMT / EU-Asia
Band 39	1880.0	1920.0	1880.0	1920.0	TDD	/ China
Band 40	2300.0	2400.0	2300.0	2400.0	TDD	CM / China
Band 41	2496.0	2696.0	2496.0	2696.0	TDD	BRS / EBS
Band 42	3400.0	3600.0	3400.0	3600.0	TDD	
Band 43	3600.0	3800.0	3600.0	3800.0	TDD	
Band 44	703.0	803.0	703.0	803.0	TDD	APAC

Note:

All frequencies in MHz

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Table 37 GNSS and Connectivity Bands Used by Mobile Devices

System	Band	Downlink MS RX (EMI)		Uplink MS TX (EMC)		Duplex	Common Name / region
		F_{low}	F_{high}	F_{low}	F_{high}		
GNSS	GPS L1	1574.4	1576.4	na	na	na	/ WW
GNSS	Glonass	1597.5	1606.5	na	na	na	/ WW
GNSS	Compass	1560.1	1562.1	na	na	na	/ Asia -> WW
GNSS	Galileo	1573.4	1577.5	na	na	na	in deployment
Connectivity	Bluetooth	2400.0	2483.0	2400.0	2483.0	TDD	ISM / WW
Connectivity	802.11b/g/n/ac	2400.0	2483.0	2400.0	2483.0	TDD	ISM / WW
Connectivity	802.11a/ac	4915.0	5825.0	4915.0	5825.0	TDD	/ WW
Connectivity	802.11.ad	57000.0	66000.0	57000.0	66000.0	TDD	ISM / WW
Connectivity	802.11.af	54.0	790.0	54.0	790.0	TDD	White space WiFi
RFID	NFC	13.6	13.6	13.6	13.6	TDD	/ WW
Audio Broadcast	FM	78.0	108.0	78.0	108.0	TDD	/ WW
Audio Broadcast	FM	65.8	74.0	65.8	74.0	TDD	/ Russia
Audio Broadcast	FM	76.0	90.0	76.0	90.0	TDD	/ Japan
Audio Broadcast	DAB-VHF3	174.0	240.0	na	na	na	/ EU
Audio Broadcast	DAB-L	1452.0	1492.0	na	na	na	/ US
Video Broadcast	CMMB	470.0	860.0	na	na	na	/ China

Note:

All frequencies in MHz

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It is important to identify the lowest interference frequency with significant impact, as this sets '$f_{INT,MIN}$'. For this specification, $f_{INT,MIN}$ is decided to be 450 MHz, because it is identified as the lowest frequency of interest in the tables above.

B.3 Transmission Line Design

In most cases the transmission lines will either be designed as striplines and/or micro-striplines. The coupling between neighboring lines within a pair is small if the distance between them is >2x the dielectric thickness. For the separation of multiple pairs it is highly recommended to interleave the pairs with a ground or supply line in order to reduce coupling.

B.4 Reference Layer

In order to achieve good signal integrity and low EMI it is recommended that either a ground plane or a ground signal is in close proximity of any signal line.

B.5 Printed-Circuit Board

For boards with a large number of conductor layers the dielectric spacing between layers may become so small that it would be hard to meet the characteristic impedance requirements. In those cases a micro-stripline in the top or bottom layers may be a better solution. Hybrids consisting of a combination of micro-stripline and stripline are also viable solutions. A short segment of micro-stripline might be used near the driving or receiving IC where trace routing may be more intense. Then a short distance away a stripline may be the best option. Hybrid combinations of three-wire lanes have been evaluated with good results.

B.6 Flex Circuits

Either two conductor layers or a reasonable connected cover layer makes it much easier to meet the specifications.

B.7 Series Resistance

The DC series resistance of the interconnect should be less than 5 Ohms in order to meet the specifications. It is strongly recommended to keep the resistance in the ground connection below 0.2 Ohm. Furthermore, it is recommended that the DC ground shift be less than 50mV, which may require an even lower value if a large current is flowing through this ground. The lower this ground series resistance value can be made, the better it is for reliability and robustness.

B.8 Connectors

Connectors usually cause some impedance discontinuity. It is important to carefully minimize these discontinuities by design, especially with respect to the through-connection of the reference layer. Although connectors are typically rather small in size, the wrong choice can mess-up signals completely. Please note that the contact resistance of connectors is part of the total series resistance budget and should therefore be sufficiently low.

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