

MIPI C-PHY™: Man of the Hour

by Yogesh Chaudhary and Vikas Sharma, Mentor Graphics

INTRODUCTION

The MIPI Alliance signature dishes, C-PHY™ and D-PHY™, are becoming favorite dishes of the imaging industry. These interfaces allow system designers to easily scale up the existing MIPI Alliance Camera Serial Interface (CSI-2™) and Display Serial Interface (DSI™) ecosystems to support higher resolution image sensors and displays while keeping low power consumption at the same time. This gives them an edge to get more into the mobile systems with bigger and better pictures.

“The MIPI C-PHY specification was developed to reduce the interface signaling rate to enable a wide range of high-performance and cost-optimized applications, such as very low-cost, low-resolution image sensors; sensors offering up to 60 megapixels; and even 4K display panels,” said Rick Wietfeldt, chair of the MIPI Alliance Technical Steering Group.

“The MIPI C-PHY, D-PHY and M-PHY®, these three physical layers, combined with MIPI Alliance application protocols, address the evolving interface needs of the entire mobile device. Fundamentally, MIPI Alliance interfaces enable manufacturers to simplify the design process, reduce costs, create economies of scale and shorten time-to-market,” said Ken Drott, chair of the MIPI Alliance PHY Working Group.

The MIPI Alliance is a non-profit corporation that operates as an open membership organization. All companies in the mobile device industry are encouraged to join, including semiconductor companies, software vendors, IP providers, peripheral manufacturers, test labs and end product OEMs. The MIPI Alliance's charter is to foster standardization by developing a comprehensive set of interface specifications for mobile and mobile-influenced products. MIPI specifications impact both hardware and software in mobile devices. The MIPI Alliance has delivered more than 45 specifications within the mobile ecosystem and is now going beyond mobile devices, finding new applications in vertical segments; such as

automotive, IoT (Internet of Things), and wearables.

The MIPI Alliance helps companies interconnect components to create successful mobile designs and provides a selection of physical layer technologies to support a full range of application requirements, yielding benefits across the industry for better alignment on physical interfaces between processors and peripheral devices. The MIPI Alliance intends to reduce fragmentation and improve interoperability among system components, benefiting the entire mobile industry.



MIPI PHYs

The MIPI Alliance develops interfaces for mobile device displays and cameras using low power, low noise and high performance physical layer (PHY) serial interfaces. MIPI has defined three physical layer interface devices—D-PHY, M-PHY and C-PHY — and supporting specifications for camera, display, and chip-to-chip protocols. Each physical layer offers unique advantages and features that collectively address every important aspect of today's integrated handheld mobile devices.

These specifications are broadening the variety of interface choices available to manufacturers and opening up new opportunities for companies to differentiate their product designs based on business-specific strategies or technology requirements.

As technology has improved, sensors capture more color information and support more RGB/YCbCr multicolor formats. Extra pixels are required to absorb intense colors. To improve image quality, a system needs improvements in each component and at all the stages of the display ecosystem. MIPI Alliance understands this problem and the associated challenges, offering different



stacks and PHY options for each stage of the imaging ecosystem. This provides faster response time with quick capture and image display. MIPI CSI-2 and DSI uses the first generation MIPI physical layer interface, called D-PHY.

MIPI D-PHY: GOOD MAN

MIPI D-PHY had all good qualities, provided simple, scalable solutions and serialized whatever is required. It was a “Good Man.” The D-PHY substantially increases the bandwidth (2.5 Gigabits per lane) for transferring more pixels while consuming very low power. In addition, it maintains a low pin count, which invariably saves power. Until now, everything was running perfectly fine and the industry looked quite satisfied. However, the only thing that is constant is change, and the same applies to the imaging industry as well. Who would have thought that we would move to mega-pixel cameras from VGA cameras? Everyone now foresees more pixel requirements that require much more bandwidth. The immediate solution for this was to use compression techniques. Thus, the MIPI Alliance in collaboration with VESA incorporated DSC compression techniques (MIPI, VESA, DSC). However, bandwidth was still seen as the limiting factor, and the situation arrived where the industry could not go where it needed to go. To resolve this issue, M-PHY was developed— a “Super Man.”

MIPI M-PHY: SUPER MAN

MIPI M-PHY has superpowers and fascinating stuff like embedded clocks with clock recoveries, ultra-high bandwidth (5.8 Gigabits per lane), and great performance — all while consuming much less power. This is the next generation PHY that supports a much broader range of applications, including interfaces for advanced displays and cameras, audio, video, memory, power management, and communication between Baseband IC to Radio Frequency IC. The M-PHY has everything that is extraordinary and requires extraordinary stacks, like the MIPI Unified Protocol (UniPro™), to communicate, but the industry is still playing dirty with ordinary stacks, like MIPI CSI-2 and MIPI DSI. The existing architecture of CSI-2 and DSI, including their intermediate revisions, are ordinary and do not allow

designers to move to an extraordinary M-PHY for higher speeds from the traditionally used D-PHY. The decision to incorporate MIPI UniPro is not feasible and certainly is not a few months job because it is not an upgrade. Rather, it requires system-level architectural changes, which affects the entire imaging ecosystem and its cost. So, the industry started looking for something new, or at least something different. They started looking towards the ray of light coming through a tiny hole, which looked like a “C”, and then the “Man of the Hour” shone through – MIPI C-PHY.

MIPI C-PHY: THE MAN OF THE HOUR

MIPI C-PHY provides the best solution for the OEMs or IP vendors, which are currently using MIPI D-PHY as a PHY layer for their legacy MIPI CSI-2 and MIPI DSI stacks. The C-PHY is giving wings to the imaging ecosystem. The C-PHY satisfies the backward compatibilities with D-PHY and can be implemented on the same parallel interface (PHY Protocol Interface – PPI). The C-PHY uses the 3-Phase symbol encoding technology, which delivers approximately 2.28 bits per symbol over a three-wire group of conductors per lane. This enables higher data rates at a lower toggling frequency, further reducing power. The bandwidth (5.7 Gigabits per lane) is ultra-high in comparison to MIPI M-PHY. The C-PHY can be connected to an ordinary legacy stack (including displays and cameras) of the D-PHY via PPI and will provide the high-speed interface. It holds an embedded clock for HS transfer and clock recoveries. It has been designed specifically for moving pixels from the source to sink without any overhead and with minimal latency, by which it will provide a high-throughput performance. The data width of parallel interface (PPI) that communicates to a camera (MIPI CSI-2) and display (MIPI DSI) stack has been scaled up. Now, more data can be transferred to C-PHY within a single clock. These are the reasons that C-PHY is becoming the favorite and certainly the man of the hour. The MIPI Alliance is also working on upgrading the D-PHY to match the industry requirements.

MENTOR QVIP (QUESTA VERIFICATION IP)

The Mentor Graphics® Questa® Verification IP (QVIP) library provides the MIPI D-PHY, M-PHY and C-PHY VIP for the latest-generation physical layer solutions and protocol specifications, including imaging CSI-2 and DSI for MIPI based ecosystems. Compatible with the Questa simulator and functional verification platform, MIPI QVIPs deliver easy-to-use models and high performance with advanced debug capabilities.

Mentor's MIPI QVIP integrates seamlessly into users advanced verification environments, including testbenches built using UVM, OVM, Verilog, VHDL, and System-C, and can be very easily applied to a MIPI-based, design-under-test (DUT). The MIPI QVIPs also comes with predefined verification environments, so users can simply plug-and-play their DUT. In this way, the user is up and running in a short period of time even on their first test.

Because the connection between the testbench and the QVIP is at the transaction level, rather than at the signal interfaces, and transaction-based verification gives better control over traffic generation from the lowest to highest

abstraction levels covering all possible scenarios, it will be highly effective and could help customers in achieving their verification goals.

All Mentor QVIP delivers the following features:

- Comprehensive test suite and compliance tests
- Complete protocol coverage
- Assertion checking for protocol complexities
- Native SystemVerilog OVM and UVM tests and components
- SystemVerilog, Verilog, VHDL, and System-C testbench support
- Integrated support for verification planning and management
- Transaction-level scoreboarding, analysis, and debug

When beginning a new design, it is common to evaluate how to build a verification infrastructure in the quickest amount of time. Of course, verification has to be complete enough to improve confidence in the design. Rapid bring-up and improving the quality of your design are excellent goals. However, you should not forget that your environment should be efficient to use during the

PHY Characteristics

Characteristic	MIPI M-PHY™ v3.1	MIPI D-PHY™ v1.2	MIPI C-PHY™ v1.0
Primary use case	Performance driven, bi-directional packet/network oriented interface	Efficient unidirectional streaming interface, with low speed in-band reverse channel	Efficient unidirectional streaming interface, with low speed in-band reverse channel
HS clocking method	Embedded Clock	DDR Source-Sync Clock	Embedded Clock
Channel compensation	Equalization	Data skew control relative to clock	Encoding to reduce data toggle rate
Minimum configuration and pins	1 lane per direction, dual-simplex, 2 pins each (4 total)	1 lane plus clock, simplex, 4 pins	1 lane (trio), simplex, 3 pins
Maximum transmitter swing amplitude	SA: 250mV (peak) LA: 500mV (peak)	LP: 1300mV (peak) HS: 360mV (peak)	LP: 1300mV (peak) HS: 425mV (peak)
Data rate per lane (HS)	HS-G1: 1.25, 1.45 Gb/s HS-G2: 2.5, 2.9 Gb/s HS-G3: 5.0, 5.8 Gb/s (Line rates are 8b10b encoded)	80 Mbps to ~2.5 Gbps (aggregate)	80 Msym/s to 2.5 Gsym/s times 2.28 bits/sym, or max 5.7 Gbps (aggregate)
Data rate per lane (LS)	10kbps – 600 Mbps	< 10 Mbps	< 10 Mbps
Bandwidth per Port (3 or 4 lanes)	~4.0 – 18.6 Gb/s (aggregate BW)	Max ~10 Gbps per 4-lane port (aggregate)	Max ~17.1 Gbps per 3-lane port (aggregate)
Typical pins per Port (3 or 4 lanes)	10 (4 lanes TX, 1 lane RX)	10 (4 lanes, 1 lane clock)	9 (3 lanes)

verification process. This is where you will spend most of your time. Arguably, debugging design bugs is one of the most time consuming tasks of any project. Transaction Level Modeling (TLM) will change the way you think about debug productivity. Transaction loggers, along with the waveform transaction-debug capabilities of the Mentor QVIP reduces the time to debug and helps improve overall verification time and productivity.

CONCLUSION

All the existing imaging designs (MIPI CSI and MIPI DSI) can make use of the new MIPI C-PHY for greater throughput performance over bandwidth-limited channels to maximize the data rate. This will also increase the effective bit rate and does not require a separate clock lane. MIPI C-PHY is responsive to the emerging market requirements and backward compatible to existing designs.

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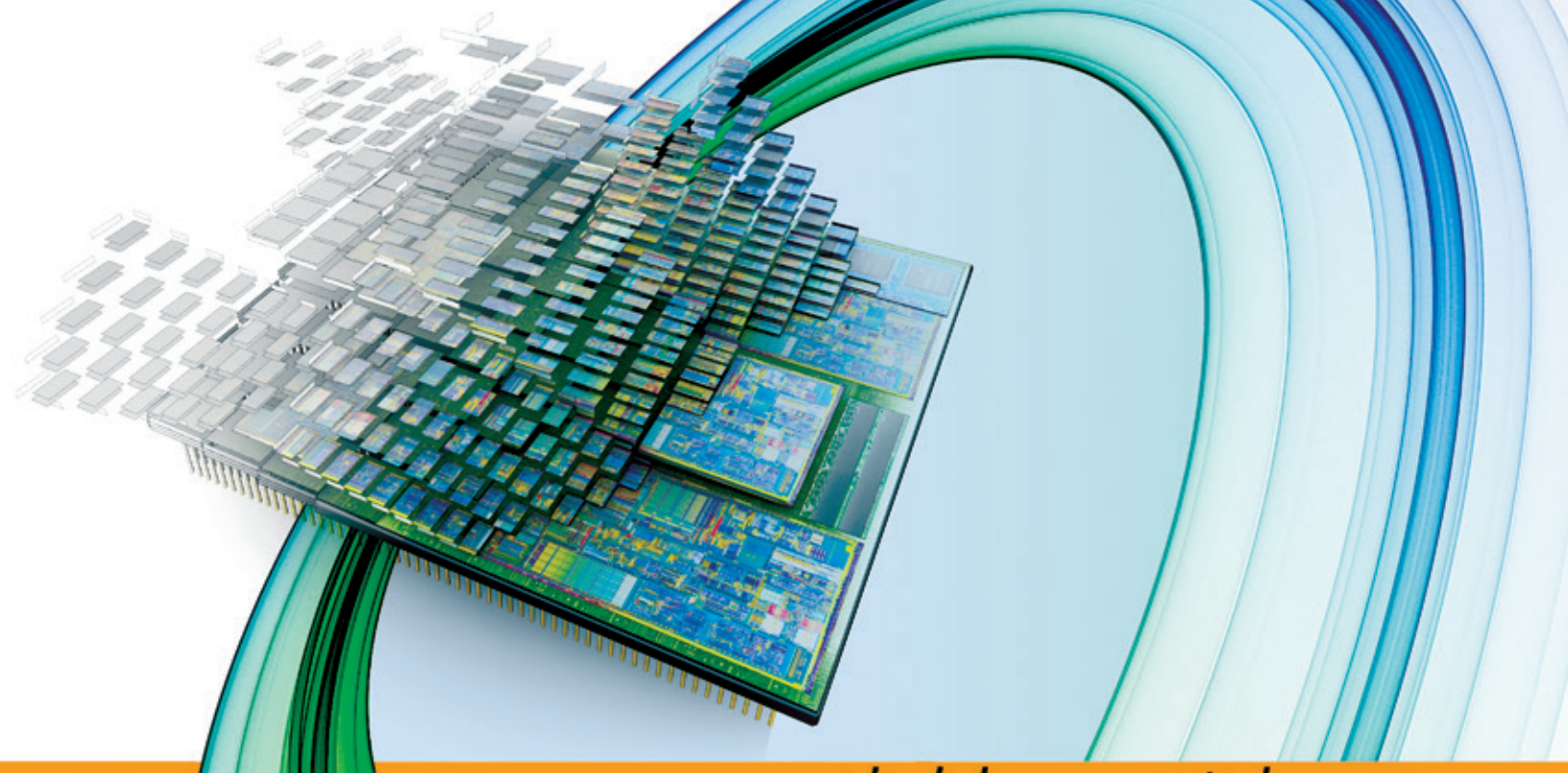
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Editor: Tom Fitzpatrick
Program Manager: Rebecca Granquist

Wilsonville Worldwide Headquarters
8005 SW Boeckman Rd.
Wilsonville, OR 97070-7777
Phone: 503-685-7000

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