

## Lab2 report

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## Ncverilog 模擬結果

```
2. nthucad.cs.nthu.edu.tw
Design hierarchy summary:
      Instances  Unique
Modules:          9      8
Primitives:       21      1
Registers:        12     12
Scalar wires:     74      -
Expanded wires:   68      3
Vectored wires:    1      -
Always blocks:     2      2
Initial blocks:    3      3
Cont. assignments: 64      5
Pseudo assignments: 6      6
Simulation timescale: 1ps
Writing initial simulation snapshot: worklib.tb:v
Loading snapshot worklib.tb:v ..... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
A = 00010001000100010001001011001111, B = 00000100010001001000010000111111, Cin = 1, sel = 0110, Y = 00010
101010101011001011100001110, Cout = 0, Negative = 0, Zero = 0, Overflow = 0

Wrong Answer Q_Q
No Bonus point 1/2
No Bonus points 2/2

score =          36 / 37 ps.without bonus points.

Simulation complete via $finish(1) at time 660 NS + 0
./ALU_tb.v:519 $finish;
ncsim> exit
[dld0117@ic25 ~/lab2]$
```

## 問題討論

- AdderSubtractor 無法傳回 overflow 的值，於是我在 AdderSubtractor 再加一個 OV 的 output 當作 overflow 的 flag。
- 0110 要 cin 但 0111 和 1000 的 cin 一定是(mode=1)，所以 AdderSubtractor 的 Cin=mode | Cin。AdderSubtractor 不知道怎麼考慮 delay，以致於 0110 的 Cin 沒有作用，所以測資不會過。