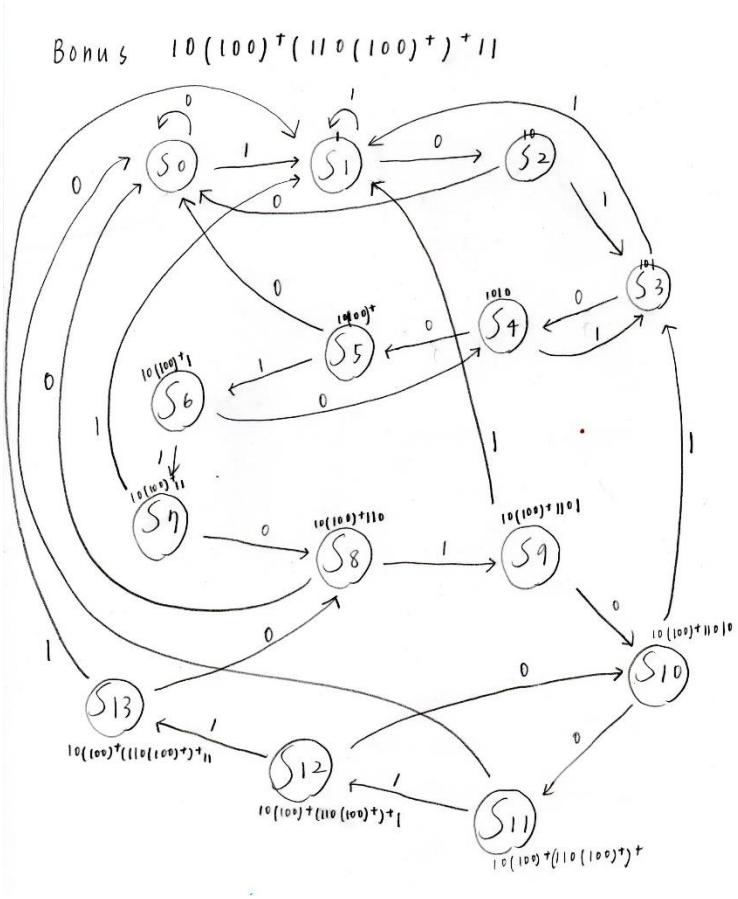
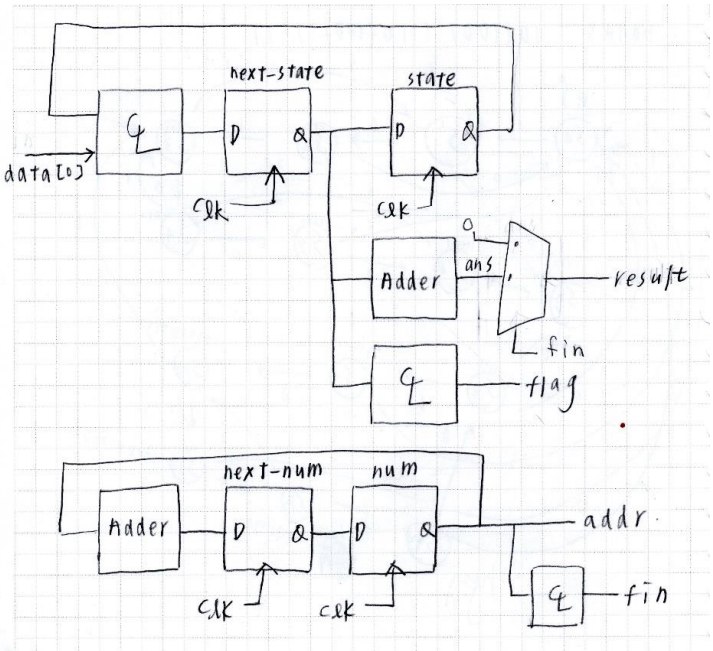
Lab 3_Bonus　106070038 杜葳葳

一、 State Transition Graph



與原題目相似，用相同方法畫出 transition，但因為此題是原 pattern 至少要重複一次，所以 state 會比較多。

二、 Block Diagram



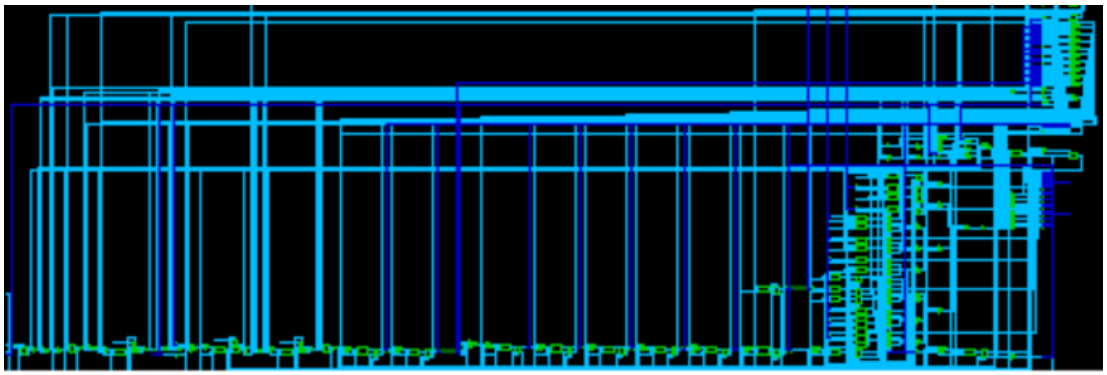
三、ncverilog 模擬結果 (sim + syn)

```
10. nthucad.cs.nthu.edu.tw
                Initial blocks:            3       3
                Cont. assignments:         4       5
                Pseudo assignments:        2       2
                Simulation timescale:  100ps
        Writing initial simulation snapshot: worklib.BON_tb:v
Loading snapshot worklib.BON_tb:v ..................... Done
*Verdi3* Loading libsscore_ius141.so
*Verdi3* : Enable Parallel Dumping.
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
FSDB Dumper for IUS, Release Verdi3_J-2014.12-SP3, Linux, 07/05/2015
(C) 1996 - 2015 by Synopsys, Inc.
*Verdi3* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are usi
ng this file.
*Verdi3* : Create FSDB file 'BON.fsdb'
*Verdi3* : Begin traversing the scopes, layer (0).
*Verdi3* : End of traversing.

GET ! addr =   18 , your_flag = 1 , ans_flag = 1
GET ! addr =   49 , your_flag = 1 , ans_flag = 1
GET ! addr =   71 , your_flag = 1 , ans_flag = 1
GET ! addr =   89 , your_flag = 1 , ans_flag = 1
GET ! addr =   95 , your_flag = 1 , ans_flag = 1
GET ! addr =  123 , your_flag = 1 , ans_flag = 1
GET ! addr =  151 , your_flag = 1 , ans_flag = 1
GET ! addr =  197 , your_flag = 1 , ans_flag = 1

Result =    8 , Answer =    8
!!!!! ACCEPTED !!!!!

Simulation complete via $finish(1) at time 6120 NS + 0
./BON_tb.v:99           $finish;
ncsim> exit
[dld0117@ic27 ~/lab3_bonus]$
```



四、nWave