Assignment - #2(Memory Management)
Operating System

1. Which of the following statements about logical address space is true?
   A. It is generated by the CPU
   B. It is also known as the physical address
   C. It is used only in static binding
   D. More than one of the above
   E. None of the above

2. Physical address space refers to:
   A. Addresses generated by the CPU
   B. Locations in the RAM
   C. Address range from secondary storage
   D. More than one of the above
   E. None of the above

3. The hardware component responsible for mapping logical to physical addresses is:
   A. Base register
   B. Memory Management Unit (MMU)
   C. Limit register
   D. More than one of the above
   E. None of the above

4. Address binding at compile-time means:
   A. Logical and physical addresses are the same
   B. Binding is done during execution
   C. Binding happens at run time
   D. More than one of the above
   E. None of the above

5. Base and limit registers help in:
   A. Segmentation
   B. Address range checking
   C. Direct hardware control
   D. More than one of the above
   E. None of the above

6. Which loading method loads a program into memory before execution?
   A. Dynamic loading
   B. Static loading
   C. Demand paging
   D. More than one of the above
   E. None of the above

7. A memory block that cannot be used due to fragmentation is called:
   A. Contiguous block
   B. Hole
   C. Internal fragmentation
   D. More than one of the above
   E. None of the above

8. Which of the following causes external fragmentation?
   A. Fixed-sized partitioning
   B. Variable-sized partitioning
   C. Paging
   D. More than one of the above
   E. None of the above

9. Logical address space is larger than physical address space in:
   A. Paging
   B. Swapping
   C. Virtual memory systems
   D. More than one of the above
   E. None of the above

10. Fragmentation that occurs within allocated blocks is called:
   A. External fragmentation
   B. Internal fragmentation
   C. Both internal and external fragmentation
   D. More than one of the above
   E. None of the above

11. Address binding can occur at:
   A. Compile time
   B. Load time
   C. Execution time
   D. More than one of the above
   E. None of the above

12. Static loading is preferred when:
   A. Memory usage is critical
   B. Programs need to load quickly
   C. Programs rarely change
   D. More than one of the above
   E. None of the above

13. Which of the following statements about dynamic loading is true?
   A. It improves memory utilization.
   B. It increases load time.
   C. It requires support from the OS
   D. More than one of the above
   E. None of the above.

14. The difference between logical and physical addresses is visible only in:
    A. Compile-time binding
    B. Load-time binding
    C. Execution-time binding
    D. More than one of the above
    E. None of the above

15. A system suffering from external fragmentation can reduce it by:
    A. Using paging
    B. Using segmentation
    C. Using swapping
    D. More than one of the above
    E. None of the above

16. The method of loading parts of a program only when they are needed during execution is called:
    A. Static loading
    B. Dynamic loading
    C. Preloading
    D. More than one of the above
    E. None of the above

17. Which of the following best describes a logical address?
    A. An address generated by the CPU
    B. The actual location in main memory
    C. The disk storage address
    D. More than one of the above
    E. None of the above

18. Which of the following types of fragmentation can be completely eliminated using paging?
    A. Internal fragmentation
    B. External fragmentation
    C. Both internal and external fragmentation
    D. More than one of the above
    E. None of the above

19. A system implementing address binding during execution uses:
    A. Absolute addressing
    B. Dynamic address translation
    C. Static relocation
    D. More than one of the above
    E. None of the above

20. Fragmentation that can occur in paging is:
    A. Internal fragmentation
    B. External fragmentation
    C. Both internal and external fragmentation
    D. More than one of the above
    E. None of the above

21. Which of the following is not a valid memory management technique?
    A. Paging
    B. Segmentation
    C. Swapping
    D. More than one of the above
    E. None of the above

22. Static binding is performed:
    A. At run time
    B. At compile time
    C. During system shutdown
    D. More than one of the above
    E. None of the above

23. Which memory management scheme is prone to external fragmentation?
    A. Paging
    B. Segmentation
    C. Fixed partitioning
    D. More than one of the above
    E. None of the above

24. In a system with base and limit registers, a process's memory access is:
    A. Unrestricted
    B. Confined to a specific range
    C. Based on paging
    D. More than one of the above
    E. None of the above

25. Which of the following statements about memory management units (MMUs) is correct?
A. MMUs translate physical addresses to logical addresses
B. MMUs handle address translation from logical to physical
C. MMUs are used only in dynamic loading
D. More than one of the above
E. None of the above

26. Address binding is dynamic when performed:
    A. At execution time
    B. At compile time
    C. Before process creation
    D. More than one of the above
    E. None of the above

27. The limit register in memory management:
    A. Stores the base address of a process
    B. Holds the size of the memory segment
    C. Ensures memory protection
    D. More than one of the above
    E. None of the above

28. Which technique minimizes external fragmentation but may suffer from internal fragmentation?
    A. Segmentation
    B. Paging
    C. Swapping
    D. More than one of the above
    E. None of the above

29. The address space visible to a programmer is the:
    A. Physical address space
    B. Logical address space
    C. Virtual address space
    D. More than one of the above
    E. None of the above

30. Effective address calculation in segmentation involves:
    A. Adding the base address to the offset
    B. Multiplying the segment size by page size
    C. Using frame numbers directly
    D. More than one of the above
    E. None of the above

31. Segment table entries contain:
    A. Base address and page number
    B. Base address and limit
    C. Logical and physical addresses
    D. More than one of the above
    E. None of the above

32. Which memory allocation strategy minimizes external fragmentation?
    A. Contiguous memory allocation
    B. Non-contiguous memory allocation
    C. Static partitioning
    D. More than one of the above
    E. None of the above

33. Paging divides memory into:
    A. Variable-sized blocks
    B. Fixed-sized blocks called pages
    C. Contiguous memory blocks
    D. More than one of the above
    E. None of the above

34. The formula to calculate the number of pages required for a process is:
    A. Process size / Frame size
    B. Process size + Frame size
    C. Process size - Frame size
    D. More than one of the above
    E. None of the above

35. In paging, the page table maps:
    A. Logical pages to physical frames
    B. Processes to their memory locations
    C. Physical addresses to logical addresses
    D. More than one of the above
    E. None of the above

36. A page table entry typically includes:
    A. Page number
    B. Frame number
    C. Protection bits
    D. More than one of the above
    E. None of the above

37. The Translation Lookaside Buffer (TLB) is used to:
    A. Speed up logical to physical address translation
    B. Store entire page tables
    C. Manage cache memory
    D. More than one of the above
    E. None of the above

38. In a two-level paging system, the first-level page table points to:
    A. Frame numbers
    B. Secondary page tables
    C. Logical addresses
    D. More than one of the above
    E. None of the above

39. A valid bit in a page table entry indicates:
    A. If the page is in memory
    B. The protection level of the page
    C. The page size
    D. More than one of the above
    E. None of the above

40. The page offset is:
    A. The size of the page
    B. The difference between frame numbers
    C. The displacement within a page
    D. More than one of the above
    E. None of the above

41. The page table size depends on:
    A. Number of processes
    B. Number of pages in logical memory
    C. Frame size
    D. More than one of the above
    E. None of the above

42. A TLB hit occurs when:
    A. The CPU finds the page in the TLB
    B. The CPU fails to find the page in the TLB
    C. The page is loaded from secondary storage
    D. More than one of the above
    E. None of the above

43. The effective memory access time considering TLB is given by:
    A. (Hit ratio × TLB access time) + (Miss ratio × 2*Memory access time)
    B. (TLB access time + Memory access time)
    C. (Hit ratio + Miss ratio) / 2
    D. More than one of the above
    E. None of the above

44. A process's logical address consists of:
    A. Page number and offset
    B. Frame number and offset
    C. Base address and limit
    D. More than one of the above
    E. None of the above

45. The frame size in paging is determined by:
    A. The operating system
    B. The hardware architecture
    C. The process requirements
    D. More than one of the above
    E. None of the above

46. When the TLB is full, the least recently used (LRU) entry is:
    A. Loaded into main memory
    B. Replaced by a new entry
    C. Moved to secondary storage
    D. More than one of the above
    E. None of the above

47. A TLB miss occurs when:
    A. The required page table entry is not in the TLB.
    B. The process is swapped out
    C. The page is not in main memory
    D. More than one of the above
    E. None of the above

48. Which of the following is true in a multi-level paging system?
    A. It reduces the size of individual page tables
    B. It increases the overall access time
    C. It requires multiple memory accesses for address translation
    D. More than one of the above
    E. None of the above

49. The page fault occurs when:
    A. A page is not found in the TLB
    B. A page is not present in main memory
    C. The page table entry is invalid
    D. More than one of the above
    E. None of the above

50. The size of a logical address space depends on:
    A. The number of bits in the address
    B. The size of physical memory
    C. The operating system type
    D. More than one of the above
    E. None of the above

51. In paging, internal fragmentation occurs when:
    A. A page is not fully utilized
    B. Memory is divided into variable-sized partitions
    C. Contiguous memory is allocated
    D. More than one of the above
    E. None of the above

52. The total number of entries in a single-level page table is determined by:
    A. The number of pages in logical memory
    B. The number of frames in physical memory
    C. The number of bits in the frame number
    D. More than one of the above
    E. None of the above

53. Paging with a TLB improves performance by:
    A. Reducing the number of memory accesses
    B. Storing all pages in main memory
    C. Eliminating internal fragmentation
    D. More than one of the above
    E. None of the above

54. Effective Access Time (EAT) is calculated to evaluate:
    A. CPU scheduling efficiency
    B. Disk access time
    C. Memory access efficiency with TLB
    D. More than one of the above
    E. None of the above

55. A high TLB hit ratio:
    A. Decreases the EAT
    B. Increases the EAT
    C. Has no impact on EAT
    D. More than one of the above
    E. None of the above

56. Segmentation is used to:
    A. Divide memory into fixed-size pages.
    B. Divide memory into variable-sized segments
    C. Improve CPU utilization.
    D. More than one of the above.
    E. None of the above.

57. A segment table maps:
    A. Pages to frames
    B. Segments to memory addresses
    C. Processes to threads
    D. More than one of the above
    E. None of the above

58. Virtual memory allows a system to:
    A. Use physical memory only
    B. Use disk space as additional memory
    C. Access files directly from cache
    D. More than one of the above
    E. None of the above

59. Demand paging loads pages:
    A. At program start
    B. Only when needed
    C. In batches at intervals
    D. More than one of the above
    E. None of the above

60. A page fault occurs in demand paging when:
    A. A page is not in the page table
    B. A page is not in memory
    C. A page exceeds its limit
    D. More than one of the above
    E. None of the above

61. Locality of reference refers to:
    A. Accessing nearby memory locations frequently
    B. Accessing random memory locations
    C. Predictable data access patterns
    D. More than one of the above
    E. None of the above

62. Temporal locality is characterized by:
    A. Repeated access to recently accessed data
    B. Access to consecutive memory locations
    C. Accessing data randomly
    D. More than one of the above
    E. None of the above

63. Spatial locality refers to:
    A. Accessing data from different locations
    B. Accessing contiguous memory locations
    C. Accessing disk pages frequently
    D. More than one of the above
    E. None of the above

64. The working set model is used to:
    A. Estimate process memory usage
    B. Improve cache performance
    C. Reduce CPU usage
    D. More than one of the above
    E. None of the above

65. Thrashing occurs when:
    A. Processes spend more time swapping pages
    B. CPU utilization is high
    C. Memory is fragmented
    D. More than one of the above
    E. None of the above

66. The primary advantage of demand paging is:
    A. Reduced memory usage
    B. Faster disk access
    C. Improved CPU scheduling
    D. More than one of the above
    E. None of the above

67. Segmentation with paging is used to:
    A. Reduce fragmentation
    B. Increase the size of segments
    C. Combine paging and segmentation
    D. More than one of the above
    E. None of the above

68. A TLB miss penalty can be reduced by:
    A. Increasing page size
    B. Increasing the TLB size
    C. Using multi-level page tables
    D. More than one of the above
    E. None of the above

69. The page replacement policy directly affects:
A. TLB hit rate.
B. Page fault rate
C. Memory access time
D. More than one of the above
E. None of the above

70. In the context of virtual memory, swapping refers to:
A. Moving processes between registers
B. Moving pages between disk and RAM
C. Exchanging data between caches
D. More than one of the above
E. None of the above

80. Segmentation fault occurs when:
A. Memory access is beyond segment limits
B. Pages are not found in TLB
C. CPU scheduling fails
D. More than one of the above
E. None of the above

81. The primary reason for using virtual memory is to:
A. Speed up disk operations
B. Allow larger programs to run
C. Reduce cache misses
D. More than one of the above
E. None of the above

82. Page table entry (PTE) includes information about:
A. Frame number
B. Valid/Invalid bit
C. Page reference bit
D. More than one of the above
E. None of the above

83. Locality of reference enhances the performance of:
A. Paging systems
B. Disk scheduling algorithms
C. CPU scheduling policies
D. More than one of the above
E. None of the above

84. A context switch involving memory management requires:
A. Updating the page table
B. Flushing the TLB
C. Saving process states
D. More than one of the above
E. None of the above

85. Temporal and spatial locality help reduce:
A. Cache misses
B. Page faults
C. CPU utilization
D. More than one of the above
E. None of the above

86. The primary component of demand paging that handles page faults is:
A. TLB.
B. Page fault handler
C. Process scheduler
D. More than one of the above
E. None of the above

87. Thrashing in a system can be mitigated by:
A. Increasing physical memory
B. Adjusting the working set size
C. Using better scheduling algorithms
D. More than one of the above
E. None of the above

88. A segment register holds:
A. A page frame number
B. The base address of a segment
C. A logical address
D. More than one of the above
E. None of the above

89. Segmentation differs from paging in that it:
A. Uses fixed-sized blocks
B. Uses variable-sized segments
C. Requires page tables
D. More than one of the above
E. None of the above

90. In segmentation, the limit register is used to:
A. Define the segment size
B. Map pages to frames
C. Store logical addresses
D. More than one of the above
E. None of the above

Answer With Explanation

1. Answer: A. It is generated by the CPU.
Explanation: Logical address space is the address space generated by the CPU during program execution. It differs from physical address space, which refers to actual locations in memory.

2. Answer: B. Locations in the RAM.
Explanation: Physical address space refers to actual addresses in the RAM (main memory).

3. Answer: B. Memory Management Unit (MMU)
Explanation: The MMU maps logical addresses to physical addresses using address translation mechanisms.

4. Answer: A. Logical and physical addresses are the same.
Explanation: In compile-time binding, the logical address is directly mapped to the physical address, making them identical.

5. Answer: B
Explanation: Base and limit registers define the range of addresses a process can access and ensure processes don't access unauthorized memory locations.

6. Answer: B. Static loading.
Explanation: Static loading loads the entire program into memory before execution starts.

7. Answer: C. Internal fragmentation
Explanation: Internal fragmentation occurs when allocated memory exceeds the memory required by the process, causing unused space inside a block.

8. Answer: B. Variable-sized partitioning.
Explanation: External fragmentation occurs when variable-sized partitions leave gaps between allocated memory blocks that are too small to be used.

9. Answer: C. Virtual memory systems
Explanation: In virtual memory systems, logical address space can exceed physical address space by using disk storage as an extension of RAM.

10. Answer: B. Internal fragmentation
Explanation: Internal fragmentation happens when allocated memory is larger than required, leaving unused space inside the allocated block.

11. Answer: D. More than one of the above.
Explanation: Address binding can occur at compile time, load time, or execution time, depending on system requirements.

12. Answer: C. Programs rarely change
Explanation: Static loading is simple and suitable for programs that rarely change, as the entire program is loaded at once.

13. Answer: D. More than one of the above
Explanation: Dynamic loading improves memory utilization by loading modules only when needed, but it requires OS support.

14. Answer: C. Execution-time binding
Explanation: Execution-time binding makes logical and physical addresses different, as translation happens dynamically.

15. Answer: D. More than one of the above
Explanation: Paging eliminates external fragmentation by dividing memory into fixed-size frames. And Segmentation can help reduce external fragmentation by allocating RAM to processes non-continuously.

16. Answer: B. Dynamic loading
Explanation: Dynamic loading loads program modules only when required, improving memory efficiency and reducing load time.

17. Answer: A. An address generated by the CPU
Explanation: A logical address is the address generated by the CPU and used by programs, translated into a physical address by the MMU.

18. Answer: B. External fragmentation
Explanation: Paging eliminates external fragmentation by breaking memory into fixed-size blocks, but internal fragmentation may still occur within a page.

19. Answer: B. Dynamic address translation
Explanation: Execution-time binding requires dynamic address translation, where logical addresses are converted to physical addresses during program execution.

20. Answer: A. Internal fragmentation
Explanation: Paging can cause internal fragmentation if the allocated page size is larger than the process needs, leaving unused space within the page.

21. Answer: E. None of the above
Explanation: Paging, segmentation, and swapping are all valid memory management techniques used to efficiently allocate and manage memory.

22. Answer: B. At compile time
Explanation: Static binding is done at compile time, where the logical addresses are directly mapped to physical addresses.

23. Answer: B. Segmentation
Explanation: Segmentation is prone to external fragmentation because segments are variable-sized, leading to gaps between allocated memory areas.

24. Answer: B
Explanation: Base and limit registers ensure that a process can only access memory within its assigned range, enhancing security and isolation.

25. Answer: B. MMUs handle address translation from logical to physical.
Explanation: MMUs are responsible for translating logical addresses generated by the CPU to corresponding physical addresses in memory.

26. Answer: A. At execution time
Explanation: Dynamic binding is performed at execution time, allowing flexible address mapping during program execution.

27. Answer: D. More than one of the above.
Explanation: The limit register holds the size of the memory segment and, together with the base register, ensures memory protection.

28. Answer: B. Paging
Explanation: Paging eliminates external fragmentation but can suffer from internal fragmentation within each fixed-size page.

29. Answer: B. Logical address space
Explanation: The logical address space is what a programmer sees and works with, as it is generated by the CPU during program execution.

30. Answer: A
Explanation: In segmentation, the effective address is calculated by adding the offset to the base address from the segment table.

31. Answer: B. Base address and limit
Explanation: Each segment table entry contains the base address and limit (size) of the segment.

32. Answer: B. Non-contiguous memory allocation
Explanation: Non-contiguous memory allocation minimizes external fragmentation by allowing processes to be allocated in different memory segments.

33. Answer: B. Fixed-sized blocks called pages
Explanation: Paging divides both logical and physical memory into fixed-sized blocks called pages (logical) and frames (physical).

34. Answer: A. Process size / Frame size
Explanation: The number of pages required is calculated by dividing the process size by the frame size, rounding up if there is a remainder.

35. Answer: A. Logical pages to physical frames
Explanation: The page table maps logical pages generated by the CPU to physical frames in the main memory.

36. Answer: D. More than one of the above
Explanation: A page table entry includes the frame number, protection bits, and other control bits, facilitating address translation and access control.

37. Answer: A. Speed up logical to physical address translation
Explanation: The TLB is a special cache that stores recently accessed page table entries to speed up address translation.

38. Answer: B. Secondary page tables
Explanation: In two-level paging, the first-level page table holds pointers to secondary page tables, which in turn map pages to frames.

39. Answer: A. If the page is in memory
Explanation: The valid bit shows whether the page is currently loaded in physical memory or resides on disk.

40. Answer: C. The displacement within a page
Explanation: The page offset specifies the exact location within a page, added to the frame base address for physical address translation.

41. Answer: B
Explanation: The size of the page table depends on the number of pages in the logical address space, as each page needs an entry.

42. Answer: A. The CPU finds the page in the TLB
Explanation: A TLB hit happens when the CPU finds the required page table entry in the TLB, avoiding a full table lookup.

43. Answer: A. (Hit ratio × TLB access time) + (Miss ratio × 2*Memory access time).
Explanation: The effective memory access time accounts for both hits and misses in the TLB, weighted by their respective probabilities.

44. Answer: A. Page number and offset
Explanation: A logical address is divided into a page number and an offset, which are used to locate the corresponding physical address.

45. Answer: A. The operating system
Explanation: The operating system determines the frame size, which typically matches the page size to simplify address translation.

46. Answer: B. Replaced by a new entry
Explanation: In a TLB using an LRU policy, the least recently used entry is replaced when a new entry needs to be loaded.

47. Answer: A. The required page table entry is not in the TLB
Explanation: A TLB miss happens when the CPU fails to find the required page table entry in the TLB, necessitating a full page table lookup.

48. Answer: D. More than one of the above
Explanation: Multi-level paging reduces individual page table sizes but increases overall access time due to multiple memory accesses.

49. Answer: B. A page is not present in main memory
Explanation: A page fault occurs when the requested page is not present in main memory, requiring it to be loaded from secondary storage.

50. Answer: A. The number of bits in the address
Explanation: The logical address space size depends on the number of bits in the logical address, determining the maximum number of addressable locations.

51. Answer: A. A page is not fully utilized
Explanation: Internal fragmentation happens when a fixed-size page is only partially filled by the process, leaving unused space within the page.

52. Answer: A. The number of pages in logical memory
Explanation: The number of entries in the page table equals the total number of pages in the logical address space.

53. Answer: A. Reducing the number of memory accesses
Explanation: The TLB improves performance by caching page table entries, reducing the need for frequent memory accesses during address translation.

54. Answer: C. Memory access efficiency with TLB
Explanation: EAT measures the efficiency of memory access considering both hits and misses in the Translation Lookaside Buffer (TLB).

55. Answer: A. Decreases the EAT
Explanation: A high hit ratio reduces EAT as more address translations are completed using the faster TLB.

56. Answer: B. Divide memory into variable-sized segments
Explanation: Segmentation divides memory into variable-sized segments, each representing a logical division of a program.

57. Answer: B. Segments to memory addresses
Explanation: The segment table maps each segment to a memory location, containing the base address and limit of each segment.

58. Answer: B. Use disk space as additional memory
Explanation: Virtual memory uses disk space to extend physical memory, allowing programs larger than physical memory to run.

59. Answer: B. Only when needed
Explanation: In demand paging, pages are loaded into memory only when they are required, reducing memory usage.

60. Answer: B. A page is not in memory
Explanation: A page fault occurs when a process tries to access a page not currently in memory, triggering a load from disk.

61. Answer: D. More than one of the above
Explanation: Locality of reference implies that programs access memory in a localized manner, either spatially (nearby locations) or temporally (recently accessed locations).

62. Answer: A. Repeated access to recently accessed data
Explanation: Temporal locality refers to the tendency of a program to access the same data repeatedly within short intervals.

63. Answer: B. Accessing contiguous memory locations
Explanation: Spatial locality implies accessing data from contiguous memory locations, leading to efficient cache use.

64. Answer: A. Estimate process memory usage
Explanation: The working set model defines the set of pages a process is currently using, helping to manage memory efficiently.

65. Answer: A. Processes spend more time swapping pages
Explanation: Thrashing happens when frequent page faults force the system to spend more time swapping pages than executing processes.

66. Answer: A. Reduced memory usage
Explanation: Demand paging reduces memory usage by loading only required pages into memory.

67. Answer: C. Combine paging and segmentation
Explanation: Segmentation with paging combines both techniques to manage memory more efficiently.

68. Answer: B. Increasing the TLB size
Explanation: Increasing the TLB size can reduce the miss penalty by caching more page table entries, improving hit rates.

69. Answer: B. Page fault rate
Explanation: A good page replacement policy minimizes the page fault rate by selecting the best page to replace when memory is full.

70. Answer: B. Moving pages between disk and RAM
Explanation: Swapping involves moving pages from disk to RAM and vice versa, depending on demand and memory availability.

80. Answer: A. Memory access is beyond segment limits
Explanation: A segmentation fault occurs when a program tries to access memory outside the bounds defined by its segments.

81. Answer: B. Allow larger programs to run
Explanation: Virtual memory allows programs larger than the available physical memory to run by using disk space as an extension.

82. Answer: D. More than one of the above
Explanation: A PTE typically includes the frame number, valid/invalid bit, and additional bits such as the reference and protection bits.

83. Answer: A. Paging systems
Explanation: Locality of reference improves the performance of paging systems by reducing page faults due to predictable memory access patterns.

84. Answer: D. More than one of the above
Explanation: During a context switch, the TLB is flushed, and the page table may need updating, along with saving the process state.

85. Answer: D. More than one of the above
Explanation: Both temporal and spatial locality reduce cache misses and page faults by improving data access patterns.

86. Answer: B. Page fault handler
Explanation: The page fault handler manages the loading of pages from disk to memory when a page fault occurs.

87. Answer: D. More than one of the above
Explanation: Thrashing can be reduced by increasing memory or tuning the working set size to fit more pages in RAM.

88. Answer: B. The base address of a segment
Explanation: Segment registers hold the base address of segments in memory, used in segmentation.

89. Answer: B. Uses variable-sized segments
Explanation: Segmentation divides memory into variable-sized segments representing logical divisions of a program.

90. Answer: A. Define the segment size
Explanation: The limit register stores the length of the segment to ensure that memory accesses stay within bounds.