Assignment-#2

Computer Organization MCQ

1. Which addressing mode uses the operand directly in the instruction?
   (A) Immediate addressing
   (B) Direct addressing
   (C) Indirect addressing
   (D) More than one of the above
   (E) None of the above

2. In which addressing mode is the effective address stored in a register?
   (A) Register addressing
   (B) Direct addressing
   (C) Indexed addressing
   (D) More than one of the above
   (E) None of the above

3. The mode where the operand's address is calculated by adding a base register and an offset is:
   (A) Indexed addressing
   (B) Immediate addressing
   (C) Indirect addressing
   (D) More than one of the above
   (E) None of the above

4. Which of the following addressing modes is used for accessing arrays?
   (A) Indexed addressing
   (B) Register addressing
   (C) Immediate addressing
   (D) More than one of the above
   (E) None of the above

5. In which addressing mode is the operand located in memory and its address is specified in the instruction?
   (A) Direct addressing
   (B) Immediate addressing
   (C) Indirect addressing
   (D) More than one of the above
   (E) None of the above

6. Associative memory is also known as:
   (A) Cache memory
   (B) Content-addressable memory
   (C) Main memory
   (D) More than one of the above
   (E) None of the above

7. Which of the following is a benefit of associative memory?
   (A) Faster data lookup
   (B) Lower cost compared to main memory
   (C) Requires more physical space
   (D) More than one of the above
   (E) None of the above

8. Associative memory compares data based on:
   (A) Memory address
   (B) Content
   (C) Data size
   (D) More than one of the above
   (E) None of the above

9. Which of the following is a primary advantage of cache memory?
   (A) Faster access time compared to main memory
   (B) Larger size than main memory
   (C) Cheaper than main memory
   (D) More than one of the above
   (E) None of the above

10. The locality of reference principle is a key concept in:
    (A) Cache memory
    (B) Virtual memory
    (C) Main memory
    (D) More than one of the above
    (E) None of the above

11. Which type of locality refers to accessing the same data repeatedly over a short period?
    (A) Temporal locality
    (B) Spatial locality
    (C) Sequential locality
    (D) More than one of the above
    (E) None of the above

12. Cache performance is improved by:
    (A) Reducing miss penalty
    (B) Increasing hit rate
    (C) Reducing cache size
    (D) More than one of the above
    (E) None of the above

13. In a multilevel cache hierarchy, which cache is typically the smallest and fastest?
    (A) L1 cache
    (B) L2 cache
    (C) L3 cache
    (D) More than one of the above
    (E) None of the above

14. The L2 cache is generally:
    (A) Larger and slower than L1 cache
    (B) Smaller and faster than L3 cache
    (C) Used to store frequently accessed data
    (D) More than one of the above
    (E) None of the above

15. Which cache mapping technique uses direct one-to-one mapping between memory blocks and cache lines?
    (A) Direct-mapped cache
    (B) Fully associative cache
    (C) Set-associative cache
    (D) More than one of the above
    (E) None of the above

16. Which cache mapping technique provides the greatest flexibility for placing data in cache?
    (A) Fully associative cache
    (B) Direct-mapped cache
    (C) Set-associative cache
    (D) More than one of the above
    (E) None of the above

17. In a set-associative cache, each block can be placed in:
    (A) Only one location in the cache
    (B) Any location in the set
    (C) Any location in the entire cache
    (D) More than one of the above
    (E) None of the above

18. Virtual memory allows:
    (A) Programs to be larger than physical memory
    (B) Memory to be accessed faster
    (C) Programs to execute without loading into RAM
    (D) More than one of the above
    (E) None of the above

19. Page tables are used in virtual memory to:
    (A) Map virtual addresses to physical addresses
    (B) Store data temporarily
    (C) Increase the size of physical memory
    (D) More than one of the above
    (E) None of the above

20. Which of the following is a commonly used page replacement algorithm?
    (A) FIFO
    (B) LRU
    (C) Optimal
    (D) More than one of the above
    (E) None of the above

21. The Least Recently Used (LRU) algorithm replaces:
    (A) The page that was used most recently
    (B) The page that has not been used for the longest time
    (C) The page that will not be used soon
    (D) More than one of the above
    (E) None of the above

22. Which interface handles data transfer between the CPU and peripherals?
    (A) PCI
    (B) USB
    (C) SCSI
    (D) More than one of the above
    (E) None of the above

23. Which of the following are standard I/O interfaces?
    (A) USB
    (B) SATA
    (C) PCIe
    (D) More than one of the above
    (E) None of the above

24. In which I/O mode does the CPU control the entire data transfer?
    (A) Programmed I/O
    (B) Interrupt-driven I/O
    (C) Direct Memory Access (DMA)
    (D) More than one of the above
    (E) None of the above

25. Which I/O data transfer mode uses the CPU only when an interrupt is received?
    (A) Programmed I/O
    (B) Interrupt-driven I/O
    (C) DMA
    (D) More than one of the above
    (E) None of the above

26. In memory-mapped I/O:
    (A) I/O devices and memory share the same address space
    (B) I/O devices have a separate address space
    (C) The CPU must use a separate instruction set for I/O
    (D) More than one of the above
    (E) None of the above

27. Which is a characteristic of I/O-mapped (Isolated) I/O?
    (A) I/O devices have a separate address space from memory
    (B) The same instructions are used for memory and I/O
    (C) I/O devices are part of the memory address space
    (D) More than one of the above
    (E) None of the above

28. In virtual memory systems, a page fault occurs when:
    (A) The requested page is not in main memory
    (B) The requested page is already in main memory
    (C) There is an error in accessing the memory
    (D) More than one of the above
    (E) None of the above

29. The technique where processes are loaded only when needed is called:
    (A) Demand paging
    (B) Segmentation
    (C) Fragmentation
    (D) More than one of the above
    (E) None of the above

30. In virtual memory, thrashing occurs when:
    (A) Too many pages are loaded in memory
    (B) Pages are swapped in and out of memory frequently
    (C) There is insufficient memory to execute the process
    (D) More than one of the above
    (E) None of the above

31. Which of the following algorithms is not a page replacement algorithm?
    (A) LRU (Least Recently Used)
    (B) FIFO (First In First Out)
    (C) Round Robin
    (D) More than one of the above
    (E) None of the above

32. In the optimal page replacement algorithm, which page is replaced?
    (A) The page that will not be used for the longest time
    (B) The page that was least recently used
    (C) The first page that was loaded into memory
    (D) More than one of the above
    (E) None of the above

33. Cache hit occurs when:
    (A) The required data is found in the cache
    (B) The required data is not found in the cache
    (C) Data needs to be loaded from main memory
    (D) More than one of the above
    (E) None of the above

34. Cache miss penalty refers to:
    (A) The time taken to retrieve data from main memory when a cache miss occurs
    (B) The time taken to search for data in the cache
    (C) The cost of implementing a cache
    (D) More than one of the above
    (E) None of the above

35. In multilevel cache systems, data is searched in:
    (A) L1 first, then L2 if L1 misses
    (B) L2 first, then L1 if L2 misses
    (C) Main memory directly
    (D) More than one of the above
    (E) None of the above

36. Which of the following memories can be used for parallel data lookup?
    (A) Associative memory
    (B) DRAM
    (C) SRAM
    (D) More than one of the above
    (E) None of the above

37. Which of the following is true for fully associative cache?
    (A) Any block of memory can be placed in any line of cache
    (B) A block of memory must be placed in a specific cache line
    (C) Cache lines are selected based on memory addresses
    (D) More than one of the above
    (E) None of the above

38. Which I/O method uses dedicated hardware to transfer data between memory and peripherals without CPU intervention?
    (A) DMA (Direct Memory Access)
    (B) Interrupt-driven I/O
    (C) Programmed I/O
    (D) More than one of the above
    (E) None of the above

39. In interrupt-driven I/O, an interrupt occurs when:
    (A) The I/O device needs attention
    (B) The CPU finishes processing data
    (C) The I/O device is idle
    (D) More than one of the above
    (E) None of the above

40. Memory-mapped I/O provides:
    (A) A shared address space for I/O devices and memory
    (B) A separate address space for I/O devices
    (C) Direct access to the I/O devices through the CPU
    (D) More than one of the above
    (E) None of the above

41. Temporal locality refers to:
    (A) Accessing the same data or instructions repeatedly within a short period
    (B) Accessing data that is physically close to the recently accessed data
    (C) Accessing different data or instructions in a random manner
    (D) More than one of the above
    (E) None of the above

42. Spatial locality refers to:
    (A) Accessing data or instructions that are located close to each other in memory
    (B) Repeatedly accessing the same memory location
    (C) Randomly accessing data in the memory
    (D) More than one of the above
    (E) None of the above

43. If a cache has 8 lines and each line holds 4 blocks, how many blocks can the cache hold in total?
    (A) 32
    (B) 8
    (C) 4
    (D) More than one of the above
    (E) None of the above

44. A cache hit rate of 80% means:
    (A) 80% of the memory accesses are found in the cache
    (B) 20% of the memory accesses are found in the cache
    (C) 80% of the time the cache misses
    (D) More than one of the above
    (E) None of the above

45. If the cache miss rate is 15% and the average memory access time is 100 ns, what is the average time required to access memory if the cache access time is 10 ns?
    (A) 25 ns
    (B) 10.15 ns
    (C) 18.5 ns
    (D) More than one of the above
    (E) None of the above

46. If a system uses FIFO for page replacement with 3 frames and the memory currently holds pages A, B and C then in that order D comes then page E comes, which page will be replaced if page E needs to be loaded?
    (A) Page A
    (B) Page B
    (C) Page C
    (D) More than one of the above
    (E) None of the above

47. If a system with 4-page frames has a reference string of 7, 0, 1, 2, 0, 3, 0, 4, how many page faults will occur using LRU page replacement?
    (A) 6
    (B) 4
    (C) 7
    (D) More than one of the above
    (E) None of the above

48. Given a reference string: 1, 2, 3, 4, 1, 2, 5, 1, 2, 3, 4, and 5, with 3 page frames available, how many page faults will occur using the optimal page replacement algorithm?
    (A) 8
    (B) 9
    (C) 7
    (D) More than one of the above
    (E) None of the above

49. For the LFU (Least Frequently Used) page replacement algorithm, which page would be replaced if the reference string is: 7, 0, 1, 2, 7, 0, 1, 3, with 3 page frames and page 0 has been used 3 times, page 1 has been used 2 times, and page 7 has been used 2 times?

(A) Page 0
(B) Page 1
(C) Page 7
(D) More than one of the above
(E) None of the above

50. Which of the following best describes Belady's anomaly?

(A) Increasing the number of page frames can lead to an increase in the number of page faults
(B) Increasing the number of page frames always decreases the number of page faults
(C) Decreasing the number of page frames increases the number of page faults
(D) More than one of the above
(E) None of the above

Answers with Explanations

1. **Immediate addressing**
   Explanation: In immediate addressing, the operand is directly specified in the instruction.
2. **Register addressing**
   Explanation: Register addressing uses a register to store the effective address.
3. **Indexed addressing**
   Explanation: Indexed addressing adds an offset to the base register to compute the effective address.
4. **Indexed addressing**
   Explanation: Indexed addressing is typically used to access elements of an array.
5. **Direct addressing**
   Explanation: Direct addressing specifies the memory address of the operand in the instruction.
6. **Content-addressable memory**
   Explanation: Associative memory is also known as content-addressable memory because it searches based on content.
7. **Faster data lookup**
   Explanation: Associative memory allows for fast data lookup by comparing data based on content.
8. **Content**
   Explanation: Associative memory compares data based on content rather than memory addresses.
9. **Faster access time compared to main memory**
   Explanation: Cache memory is faster than main memory but smaller and more expensive.
10. **Cache memory**
    Explanation: The principle of locality of reference is fundamental to cache memory.
11. **Temporal locality**
    Explanation: Temporal locality refers to the repeated access of the same data over a short time period.
12. **More than one of the above**
    Explanation: Both reducing miss penalty and increasing hit rate improve cache performance.
13. **L1 cache**
    Explanation: L1 cache is the smallest and fastest in a multilevel cache hierarchy.
14. **More than one of the above**
    Explanation: L2 cache is larger and slower than L1 but faster and smaller than L3.
15. **Direct-mapped cache**
    Explanation: In a direct-mapped cache, each block maps to exactly one cache line.
16. **Fully associative cache**
    Explanation: A fully associative cache allows a block to be placed in any cache line.
17. **Any location in the set**
    Explanation: In set-associative caches, blocks can be placed in any location within a designated set.
18. **Programs to be larger than physical memory**
    Explanation: Virtual memory allows programs to use more memory than what is physically available.
19. **Map virtual addresses to physical addresses**
    Explanation: Page tables in virtual memory map virtual addresses to physical ones.
20. **More than one of the above**
    Explanation: FIFO, LRU, and Optimal are common page replacement algorithms.
21. **The page that has not been used for the longest time**
    Explanation: The LRU algorithm replaces the least recently used page.

22. More than one of the above
    Explanation: PCI, USB, and SCSI all handle data transfer between CPU and peripherals.
23. More than one of the above
    Explanation: USB, SATA, and PCIe are all standard I/O interfaces.
24. Programmed I/O
    Explanation: In programmed I/O, the CPU controls the entire data transfer process.
25. Interrupt-driven I/O
    Explanation: Interrupt-driven I/O uses interrupts to notify the CPU, allowing it to handle other tasks.
26. I/O devices and memory share the same address space
    Explanation: In memory-mapped I/O, both I/O devices and memory use the same address space.
27. I/O devices have a separate address space from memory
    Explanation: In isolated I/O, the CPU has separate address spaces for I/O devices and memory.
28. (A) The requested page is not in main memory
    Explanation: A page fault occurs when the required page is not in memory and needs to be loaded from secondary storage.(B) is incorrect: If the page is in memory, no page fault occurs. (C) is incorrect: Page faults are not memory access errors.
29. (A) Demand paging
    Explanation: Demand paging loads a page into memory only when it is needed during program execution. (B) Segmentation refers to dividing the memory into segments, not on-demand loading. (C) Fragmentation refers to wasted memory space, not a loading technique.
30. (B) Pages are swapped in and out of memory frequently
    Explanation: Thrashing occurs when the system spends most of its time swapping pages instead of executing instructions. (A) Too many pages in memory might cause fragmentation, but not thrashing. (C) Insufficient memory might cause a program to terminate, but not thrashing.
31. (C) Round Robin
    Explanation: Round Robin is a CPU scheduling algorithm, not a page replacement algorithm. (A) LRU is a page replacement algorithm. (B) FIFO is also a page replacement algorithm.
32. (A) The page that will not be used for the longest time
    Explanation: The optimal page replacement algorithm replaces the page that will not be used for the longest time in the future. (B) LRU replaces the least recently used page, not the one that will not be used for the longest time. (C) FIFO replaces the oldest page, not the one with future usage in mind.
33. (A) The required data is found in the cache
    Explanation: A cache hit occurs when the data requested by the CPU is already present in the cache. (B) A cache miss happens when the data is not found in the cache. (C) Loading data from main memory happens after a cache miss.
34. (A) The time taken to retrieve data from main memory when a cache miss occurs
    Explanation: Cache miss penalty refers to the additional time needed to fetch data from slower main memory when it's not found in the cache. (B) The time to search for data in the cache is not referred to as miss penalty. (C) The cost of implementing cache is not related to miss penalty.
35. (A) L1 first, then L2 if L1 misses
    Explanation: In a multilevel cache system, the CPU checks L1 first. If L1 misses, it then checks L2. (B) Checking L2 first is incorrect as L1 cache is checked first in multilevel cache hierarchies. (C) Directly accessing main memory without checking caches would bypass the purpose of caches.
36. (A) Associative memory

Explanation: Associative memory (or CAM) allows parallel searching based on content rather than addresses. (B) DRAM cannot perform parallel data lookup. (C) SRAM does not perform parallel lookups based on content.

37. (A) Any block of memory can be placed in any line of cache
    Explanation: In fully associative caches, any block of memory can be stored in any cache line. (B) Direct-mapped caches have fixed positions for blocks, not fully associative caches. (C) Cache lines being selected based on memory addresses is true for direct-mapped caches.
38. (A) DMA (Direct Memory Access)
    Explanation: DMA transfers data between memory and peripherals without requiring the CPU to intervene during the transfer. (B) Interrupt-driven I/O involves the CPU processing interrupts. (C) Programmed I/O requires CPU involvement in data transfer.
39. (A) The I/O device needs attention
    Explanation: In interrupt-driven I/O, an interrupt is generated when an I/O device requires CPU attention. (B) An interrupt does not occur when the CPU finishes processing data. (C) An idle I/O device does not generate an interrupt unless it requires service.
40. (A) A shared address space for I/O devices and memory
    Explanation: In memory-mapped I/O, both I/O devices and memory share the same address space, allowing the CPU to use the same set of instructions for both memory and I/O operations.
41. (A) Accessing the same data or instructions repeatedly within a short period
    Explanation: Temporal locality is the concept of accessing the same data or instructions frequently within a short time frame. (B) Spatial locality involves accessing nearby data, not repeated access to the same data. (C) Random access does not relate to temporal locality.
42. (A) Accessing data or instructions that are located close to each other in memory
    Explanation: Spatial locality refers to the tendency to access data that is physically close to recently accessed data (B) Repeated access to the same memory location is temporal locality. (C) Random access is not a form of spatial locality.
43. (A) 32
    Explanation: If a cache has 8 lines and each line holds 4 blocks, the total number of blocks is 8 * 4 = 32. (B) 8 is the number of lines, not blocks. (C) 4 is the number of blocks per line, not total.
44. (A) 80% of the memory accesses are found in the cache
    Explanation: A cache hit rate of 80% means that 80% of the time, the data is found in the cache. (B) 20% would be the miss rate, not the hit rate. (C) The cache miss rate is 20%, not 80%.
45. (A) 19.5 ns
    Explanation: Average time to access memory = (Cache miss rate * (Average memory access time + Cache access time)) + (Cache hit rate * Cache access time)
    = 0.15 * (100 ns + 10 ns) + 0.85 * 10 ns
    = 0.15 * 110 ns + 0.85 * 10 ns
    = 16.5 ns + 8.5 ns
    = 25 ns.

46. (B) Page B
    Explanation: In FIFO page replacement, the page that has been in memory the longest is replaced. Since pages were added in the order A, B, C, D, page A will be replaced when page D is added and page B will be replaced when page E is added .
47. (A) 6
48. (C) 7

49. (B) Page 1
50. (A) Increasing the number of page frames can lead to an increase in the number of page faults