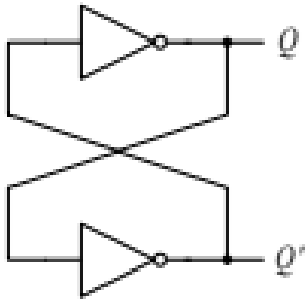
Sequential Circuit

Latches

- It is also known as a bistable-multivibrator. Because it has two stable states namely active high as well as active low.
- The simplest sequential circuit or storage element is a bistable element, which is constructed with two inverters connected sequentially in a loop.
- It works like a storage device by holding the data through a feedback lane.
- Latch is a basic building block of memory which store 1 bit of memory.
- Latch is not a synchronous system.
- A latch is level-triggered (outputs can change as soon as the inputs change).
- A bistable element has memory in the sense that it can remember the content (or state) of the circuit indefinitely.

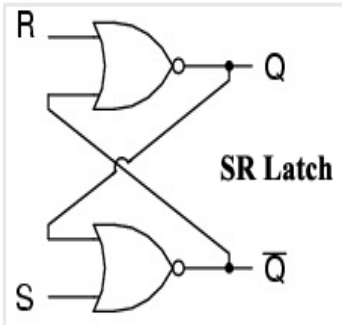


Types of Latches

- S-R Latch
- D latch
- JK Latch
- T Latch

SR Latch

- The bistable element is able to remember or store one bit of information.
- However, because it does not have any inputs, we cannot change the information bit that is stored in it.
- In order to change the information bit, we need to add inputs to the circuit.
- We replace the two inverters with two NOR or NAND gates. This circuit is called a SR latch.
- In addition to the two outputs Q and Q', there are two inputs S and R for set and reset respectively.



Truth table of SR Latch:-

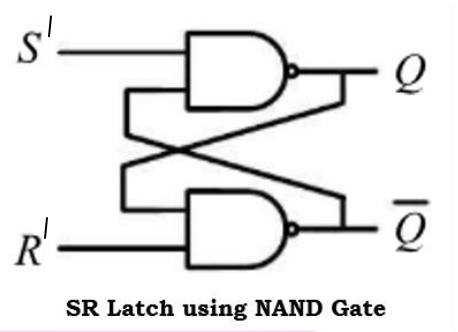
NOR table		
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

SR table			
S	R	Q	Q’
0	0	Hold(memory)	
0	1	0	1
1	0	1	0
1	1	Invalid(not used)	

SR truth table by using NAND gate:

We can also design SR Latch by using NAND Gate but it reverse the value of set and reset therefore we input inverted S (S') and inverted R (R') to get result.

SR table			
S	R	Q	Q'
0	0	Hold(memory)	
0	1	0	1
1	0	1	0
1	1	Invalid(not used)	



SR Latch using NAND Gate

Disadvantage of SR latch

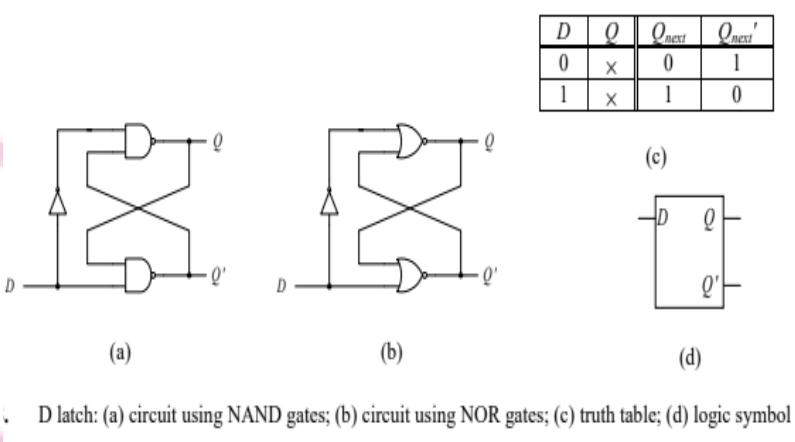
- In the SR latch we need to ensure that the two inputs, S and R, are never de-asserted at the same time.
- We prevent this situation in the D latch by adding an inverter between the original S and R inputs and replacing them with just one input D (for data).

D Latch

D latch ensures that there is no invalid condition in the circuit occurs.

Truth table of D latch:

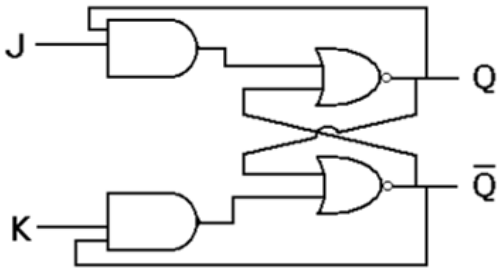
D Latch		
D	Q	Q'
0	0	1
1	1	0



D latch: (a) circuit using NAND gates; (b) circuit using NOR gates; (c) truth table; (d) logic symbol

JK Latch

- It is similar to SR Latch.
- When the JK inputs are high, the unclear states are eliminated in a JK latch, and the output is toggled.
- The main difference between SR latches and JK latches is that JK latches have the output feedback toward the inputs but SR latches does not have.



Truth table of JK latch

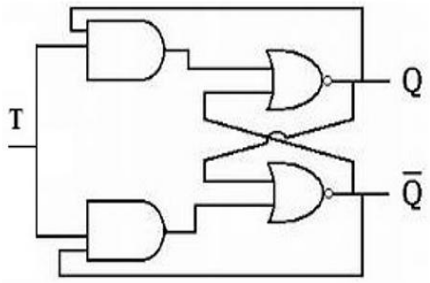
JK Latch			
J	K	Q	Q'
0	0	Hold(memory)	
0	1	0	1
1	0	1	0
1	1	toggle	

T Latch

The JK latch inputs are shorted to create the T latch. The T latch's output switches on and off when the input is set to 1 or high.When the input of T is 0 then the output will retain the same (no change).

Truth table of T latch:-

T	Q
0	No change
1	toggle



Flip Flops

- A flip-flop circuit can store and recall a single bit of information.
- Latches and flip flops are the basic storage elements but different in working.
- As name implies it has ability to "flip" or "flop" between two stable states.
- By latching a value and changing it when triggered by a clock signal, flip-flops can store data over time.
- Flip flop is edge triggered
- Flip-flops change their content only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal.
- It is also known as a Bistable Multivibrator**.**

Types of flip-flops

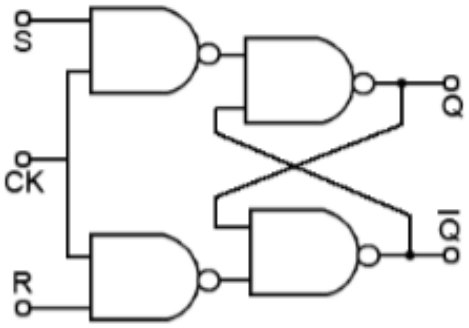
- SR Flip Flop
- JK Flip Flop
- D Flip Flop
- T Flip Flop

SR Flip flop

SR flip-flop operates with positive clock transitions or negative clock transitions. Whereas, SR latch operates with enable signal.

Truth table of SR flip flop:-

clk	S	R	Q	Q'
0	x	x	Hold(memory)	
1	0	0	Hold(memory)	
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid(not used)	



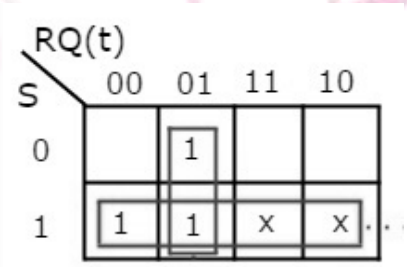
Characteristic table and excitation table for SR flip flop:

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

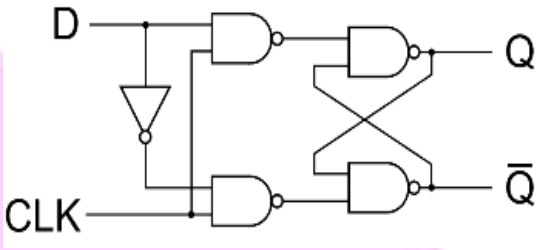
Kmap for SR flip flop Q_{n+1}:-

$Q_{n+1} = S + R'Q_n$



D flip flop

clk	D	Q_{n+1}
0	x	0
1	0	0
1	1	1



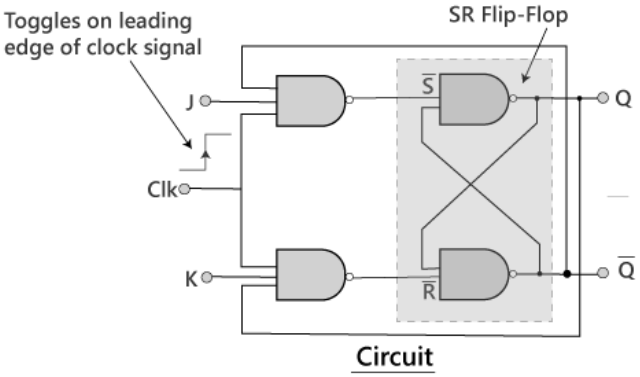
Characteristic table and excitation table for D flip flop:

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

$Q_{n+1} = D$

JK Flip Flop



Circuit

JK Flip-Flop Truth Table

J	K	$Q_{(n+1)}$	State
0	0	Q_n	No Change
0	1	0	RESET
1	0	1	SET
1	1	Q_n'	TOGGLE

Charecterstic table

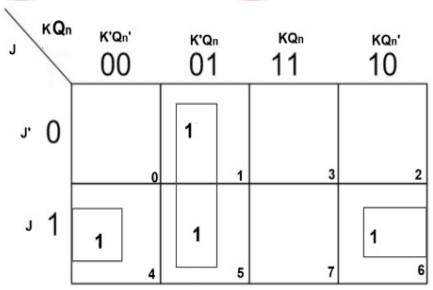
J	K	Q_n	$Q_{(n+1)}$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Excitation table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

K-map to derive the characteristic equation.

Q(n+1) = JQn' + K'Qn



Race Around Condition in JK Flip-Flop

The race condition occurs:-

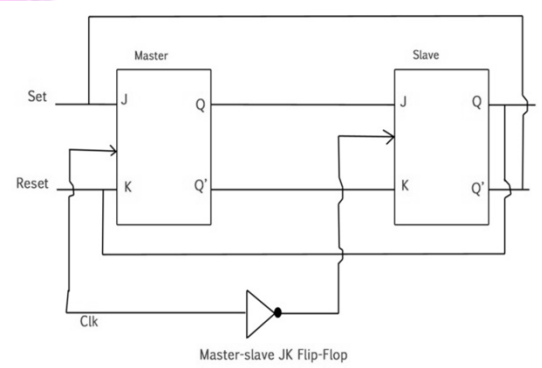
when level triggered J = K = 1 and clk pulse is high for long time than circuit propagation delay.

- For J-K flip-flop, if J=K=1, and if clk=1 for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain.
- This problem is called race around condition in J-K flip-flop.

- This problem (Race Around Condition) can be avoided by ensuring that the clock input is at logic "1" only for a very short time. This introduced the concept of Master Slave JK flip flop.

Master slave JK flip flop

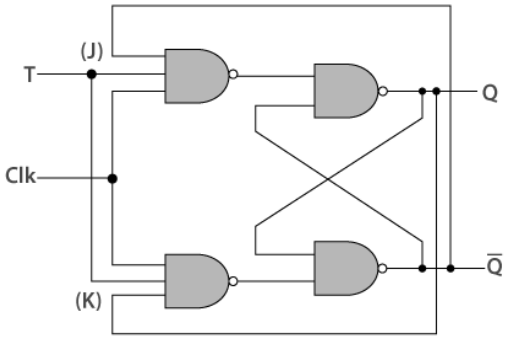
- The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration.
- Out of these, one acts as the “master” and the other as a “slave”.
- The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop.



Master-slave JK Flip-Flop

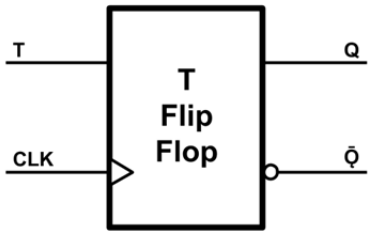
T Flip Flop

- T flip flop or to be precise is known as Toggle Flip Flop because it can able to toggle its output depending upon on the input.
- T here stands for Toggle.
- Toggle basically indicates that the bit will be flipped i.e., either from 1 to 0 or from 0 to 1.
- Here, a clock pulse is supplied to operate this flop, hence it is a clocked flip-flop.



Below you can find the truth table for T Flip-Flop:

Clk	T	Q(n)	Q’(n)
0	x	0	0
1	0	0	1
0	1	Toggle	



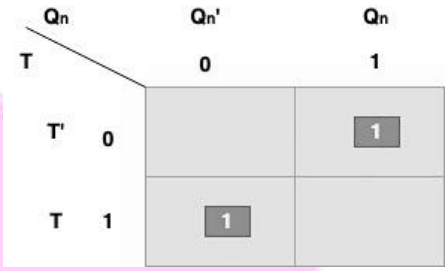
Characteristic table and Excitation table for T Flip Flop

T	Q(n)	Q(n+1)
0	0	0
0	1	1
1	0	1
1	1	0

Q_t	Q(t+1)	T
0	0	0
1	0	1
0	1	1
1	1	0

Characterstic equation of T Flip Flop:

Q(n+1) = TQn' + T'Qn = T ⊕Qn



We can find T Flip-Flop in many applications, mainly in frequency dividers, binary counters, and parallel load registers.

Counters

- A sequential circuit used to count the pulse is called a counter,
- It is collection of flip flops where the clock signal is applied
- The number of the pulse can be counted using the output of the counter.
- The main properties of a counter are timing , sequencing , and counting.

Counter works in two modes: Bidirectional counters are capable of counting in either the up direction or the down direction through any given count sequence.

- Up counter
- Down counter

Counter modes		
	Q(+ve)	**Q'(-ve)**
positive	down	Up
negative	Up	down

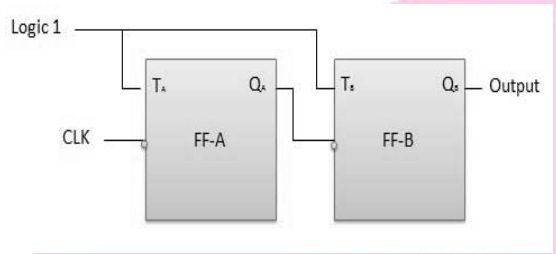
Types of counters

- **Asynchronous Counters or ripple counter**
- **Synchronous Counters**
  1. **Ring counter**
  2. **Johnson counter/twisted ring counter**

Asynchronous counter or ripple counter

- In asynchronous/ripple counter output of the first flip-flop is provided as the clock to the second flip-flop i.e flip-flop(FF) are not clocked simultaneously.
- Circuit is simpler, but speed is slow.

The logic diagram and truth table of a 2-bit ripple up counter



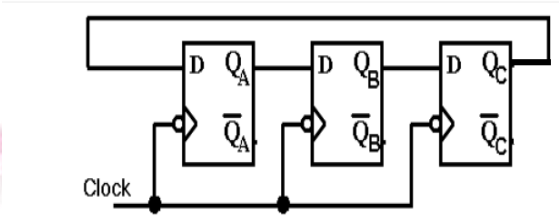
Clock	Counter output		State number	Deciimal Counter output
	Q_B	Q_A		
Initially	0	0	—	0
1st	0	1	1	1
2nd	1	0	2	2
3rd	1	1	3	3
4th	0	0	4	0

Synchronous Counter

- If the "clock" pulses are applied to all the flip-flops in a counter simultaneously, then such a counter is called as synchronous counter.

Ring counter

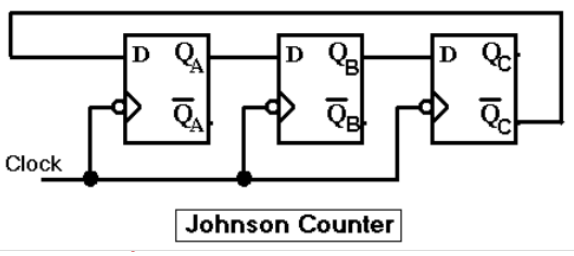
- It is also called One hot Counter.
- In this counter, the output of the last flip-flop is connected to the input of the first flip-flop.
- The main point of this Counter is that it circulates a single one (or zero) bit around the ring.
- No. of states in Ring counter = No. of flip-flop used
- A ring counter is a special type of application of the Serial IN Serial OUT Shift register.



Johnson counter

It is also known as a switch-tail ring counter, walking ring counter, or twisted ring counter.

- It connects the complement of the output of the last shift register to the input of the first register and circulates a stream of ones followed by zeros around the ring.
- In the Twisted Ring Counter, the number of states = 2 X the number of flip-flops.



Difference between synchronous and asynchronous

Key	Synchronous Counter	Asynchronous Counter
Trigger	In case of Synchronous Counters, all the constituent flip-flops are triggered with same clock simultaneously.	In case of Asynchronous Counters, there is triggering of different flip-flops with different clock.
Operation Speed	Operation speed of a synchronous counter is faster as compared to that of an asynchronous counter.	The operation speed of an asynchronous counter is comparatively slower than a synchronous counter.
Error Prone	Synchronous Counters are less error-prone; they hardly produce any decoding errors because each flip-flop is individually clocked.	Asynchronous Counters are more error-prone and produce decoding errors in the system.
Complexity	All the flip-flops in a synchronous counter coordinate with the clock, hence its design and implementation is complex as compared to that of an asynchronous counter.	In an asynchronous counter, the output of one flip-flop acts as the input of the next flip-flop, hence its design and implementation is quite simple.
Sequence	A Synchronous counter can be operated in any desired count sequence, as it could get manipulated by changing the clock sequence.	An Asynchronous counter can operate only in a fixed count sequence, i.e., UP and DOWN.
Delay	There is no propagation delay observed in case of Synchronous Counters.	In case of asynchronous counters, there is a subsequent propagation delay from one flip-flop to another.

Some important counters:

Binary counter: It is a type of counter that counts in binary, That is, it can only count up to a certain maximum number of bits before winding around and begin over from zero.

Ripple counter: A ripple counter is a type of binary counter that uses a series of flip-flops to count each bit in the binary sequence.

decade counter: A decade counter is a type of counter that counts in decimal, meaning it can count up to ten before wrapping around and starting over.

Johnson counter: A Johnson counter is a type of ring counter that uses feedback to create a sequence that can count signals.

digital timer:A digital timer is a device that uses a counter to measure the duration of an event or time interval.

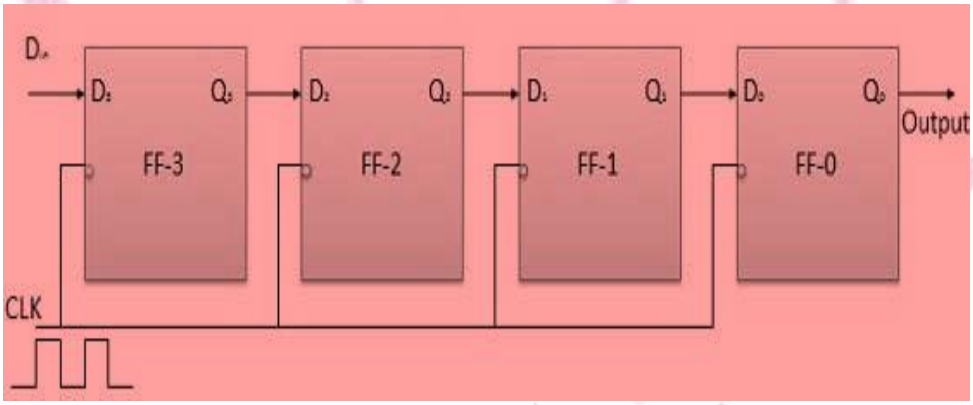
pulse counter: A pulse counter is a device that counts the number of pulses or events that occur over a specific time period.

Modulus Counter (MOD-N Counter): The modulus of a counter is the number of states in its count sequence. The maximum possible modulus is determined by the number of flip-flops.
The 2-bit ripple counter is called as MOD-4 counter and 3-bit ripple counter is called as MOD-8 counter.
So in general, an n-bit ripple counter is called as modulo-N counter.
Where, MOD number = 2^n.

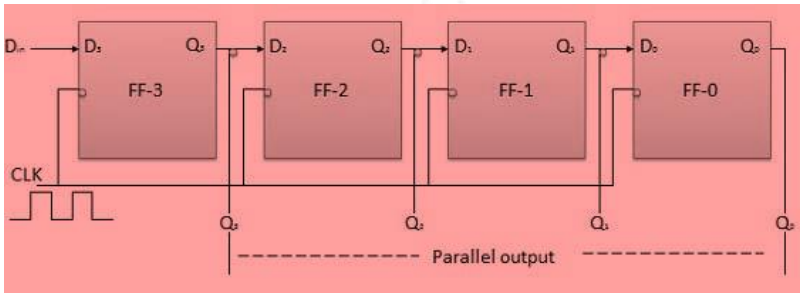
Shift Register

- A Register is a collection of flip flops.
- A flip flop is used to store single bit digital data.
- If we want to store an n-bit word, we have to use an n-bit register containing n number of flip flops.
- There are four mode of operations of a shift register.

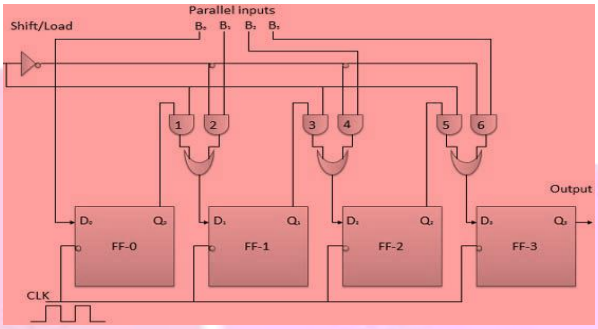
Serial Input Serial Output



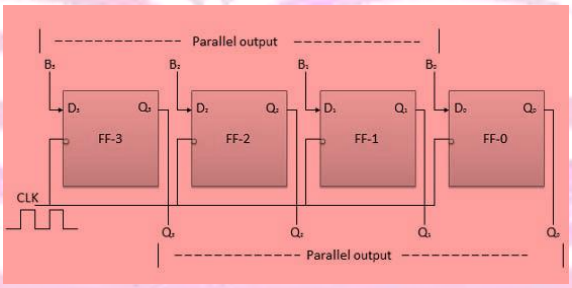
Serial Input Parallel Output



Parallel Input Serial Output



Parallel Input Parallel Output



Bidirectional Shift Register:

- For performing the multiplication and division operation using the shift register, it is required that the data should be moved in both the direction, i.e., left or right in the register. Such registers are called the "Bidirectional" shift register.
- The binary number after shifting each bit of the number to the left by one position will be equivalent to the number produced by multiplying the original number by 2.
- In the same way, the binary number after shifting each bit of the number to the right by one position will be equivalent to the number produced by dividing the original number by 2.

Universal Shift Register

A "Universal" shift register is a special type of register that can load the data in a parallel way and shift that data in both directions, i.e., right and left.