Assignment-#5

Sequential circuit

Note: Take printout of these questions try to solve and tick answer by your own

1. **Which of the following are types of latches?**
   a. **SR Latch**
   b. **D Latch**
   c. **JK Latch**
   d. **More than one of the above**
   e. **None of the above**

2. **A race condition in a digital circuit occurs when:**
   a. **Two inputs are the same**
   b. **Timing is not properly managed**
   c. **The circuit is in a stable state**
   d. **More than one of the above**
   e. **None of the above**

3. **Which latch is most commonly used in synchronous systems?**
   a. **SR Latch**
   b. **D Latch**
   c. **JK Latch**
   d. **More than one of the above**
   e. **None of the above**

4. **Which of the following is NOT a type of counter?**
   a. **Up Counter**
   b. **Down Counter**
   c. **Up/Down Counter**
   d. **More than one of the above**
   e. **None of the above**

5. **Shift registers can be used for:**
   a. **Data storage**
   b. **Data transfer**
   c. **Data manipulation**
   d. **More than one of the above**
   e. **None of the above**

6. **The purpose of a D Flip-Flop is to:**
   a. **Store one bit of data**
   b. **Transfer data between registers**
   c. **Count clock pulses**
   d. **More than one of the above**
   e. **None of the above**

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7. In a synchronous counter, the state changes occur:
    a. Based on external input
    b. Based on the clock signal
    c. Independently of the clock signal
    d. More than one of the above
    e. None of the above

8. Which shift register type shifts data only in one direction?
    a. Serial-In Serial-Out (SISO)
    b. Serial-In Parallel-Out (SIPO)
    c. Parallel-In Serial-Out (PISO)
    d. More than one of the above
    e. None of the above

9. In an SR latch, what happens when both inputs are high?
    a. The output is high
    b. The output is low
    c. The latch is in an indeterminate state
    d. More than one of the above
    e. None of the above

10. What is a major disadvantage of a ripple counter?
    a. Complexity
    b. Slow speed due to propagation delay
    c. High power consumption
    d. More than one of the above
    e. None of the above

11. Which of the following shift registers can convert parallel data to serial data?
    a. Serial-In Serial-Out (SISO)
    b. Serial-In Parallel-Out (SIPO)
    c. Parallel-In Serial-Out (PISO)
    d. More than one of the above
    e. None of the above

12. What type of flip-flop is used in a frequency divider circuit?
    a. SR Flip-Flop
    b. JK Flip-Flop
    c. D Flip-Flop
    d. More than one of the above
    e. None of the above

13. Which type of register allows data to be shifted both left and right?
    a. Shift Register
    b. Universal Register
    c. Ring Counter
    d. More than one of the above
    e. None of the above

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14. What is the primary function of an edge-triggered flip-flop?
    a. Store data
    b. Count pulses
    c. Synchronize data changes
    d. More than one of the above
    e. None of the above

15. A race condition is least likely to occur in:
    a. Synchronous systems
    b. Asynchronous systems
    c. Both synchronous and asynchronous systems
    d. More than one of the above
    e. None of the above

16. Which latch is considered the simplest form of storage?
    a. SR Latch
    b. D Latch
    c. JK Latch
    d. More than one of the above
    e. None of the above

17. In a Johnson counter, how many states are possible?
    a. 2^n
    b. 2^n - 1
    c. 2n
    d. More than one of the above
    e. None of the above

18. Which type of register is used for temporary data storage and transfer?
    a. Shift Register
    b. Counter Register
    c. Buffer Register
    d. More than one of the above
    e. None of the above

19. The characteristic equation of a JK Flip-Flop is:
    a. Q(t+1) = JQ' + K'Q
    b. Q(t+1) = JQ + K'Q'
    c. Q(t+1) = JQ + KQ'
    d. More than one of the above
    e. None of the above

20. Which of the following statements about shift registers is false?
    a. They can be used for data shifting.
    b. They are primarily used for multiplication.
    c. They can convert parallel data to serial data.
    d. More than one of the above
    e. None of the above

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21. In a D Latch, what does the output follow?
    a. Data input
    b. Clock signal
    c. Previous state
    d. More than one of the above
    e. None of the above

22. Which type of counter is used for counting specific events or pulses?
    a. Modulo-N Counter
    b. Up/Down Counter
    c. Ring Counter
    d. More than one of the above
    e. None of the above

23. In a synchronous shift register, all flip-flops are triggered by:
    a. A common clock pulse
    b. Individual clock pulses
    c. The data input
    d. More than one of the above
    e. None of the above

24. What is a characteristic of a D Flip-Flop?
    a. It has a J and K input.
    b. It transfers data on the clock edge.
    c. It only has one data input.
    d. More than one of the above
    e. None of the above

25. Which type of shift register is commonly used in digital communications?
    a. Serial-In Serial-Out (SISO)
    b. Parallel-In Parallel-Out (PIPO)
    c. Parallel-In Serial-Out (PISO)
    d. More than one of the above
    e. None of the above

26. A ring counter is a type of:
    a. Synchronous Counter
    b. Asynchronous Counter
    c. Shift Register
    d. More than one of the above
    e. None of the above

27. Which flip-flop type is used to store binary information and synchronize data?
    a. SR Flip-Flop
    b. JK Flip-Flop
    c. D Flip-Flop
    d. More than one of the above
    e. None of the above

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28. Which of the following is NOT a feature of a shift register?
    a. Data shifting
    b. Data storage
    c. Arithmetic operations
    d. More than one of the above
    e. None of the above

29. The main advantage of a synchronous counter over an asynchronous counter is:
    a. Faster speed
    b. More complex design
    c. Higher power consumption
    d. More than one of the above
    e. None of the above

30. Which of the following is a type of shift register?
    a. Ring Counter
    b. Johnson Counter
    c. Serial-In Parallel-Out (SIPO)
    d. More than one of the above
    e. None of the above

31. Which type of register can be used to implement a delay line?
    a. Shift Register
    b. Buffer Register
    c. Counter Register
    d. More than one of the above
    e. None of the above

32. A Johnson counter is a type of:
    a. Synchronous Counter
    b. Asynchronous Counter
    c. Shift Register
    d. More than one of the above
    e. None of the above

33. What is the primary use of a buffer register?
    a. Data shifting
    b. Data storage and transfer
    c. Counting events
    d. More than one of the above
    e. None of the above

34. Which latch is commonly used in memory elements?
    a. SR Latch
    b. D Latch
    c. JK Latch
    d. More than one of the above
    e. None of the above

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35. A synchronous counter has which of the following characteristics?
    a. All flip-flops are clocked by the same clock signal
    b. Flip-flops are clocked individually
    c. More complex than asynchronous counters
    d. More than one of the above
    e. None of the above

36. Which of the following can be used to implement a shift register in hardware?
    a. Flip-Flops
    b. Counters
    c. Latches
    d. More than one of the above
    e. None of the above

37. Which type of flip-flop has a feedback loop in its circuit?
    a. SR Flip-Flop
    b. JK Flip-Flop
    c. D Flip-Flop
    d. More than one of the above
    e. None of the above

38. What is the disadvantage of a ripple counter?
    a. Complexity
    b. Propagation delay
    c. Higher cost
    d. More than one of the above
    e. None of the above

39. Which shift register configuration is used for parallel-to-serial conversion?
    a. Serial-In Parallel-Out (SIPO)
    b. Parallel-In Serial-Out (PISO)
    c. Serial-In Serial-Out (SISO)
    d. More than one of the above
    e. None of the above

40. Which latch type is edge-triggered?
    a. SR Latch
    b. D Latch
    c. JK Latch
    d. More than one of the above
    e. None of the above

41. What is the function of an up/down counter?
    a. Count only in one direction
    b. Count in both directions
    c. Count in binary only
    d. More than one of the above
    e. None of the above

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42. Which type of counter shifts data in a circular fashion?
    a. Ring Counter
    b. Johnson Counter
    c. Shift Register
    d. More than one of the above
    e. None of the above

43. A flip-flop is characterized by:
    a. Two stable states
    b. High power consumption
    c. High speed operation
    d. More than one of the above
    e. None of the above

44. Which type of counter provides a sequence of states in binary order?
    a. Johnson Counter
    b. Ring Counter
    c. Binary Counter
    d. More than one of the above
    e. None of the above

45. What is the primary use of a shift register in digital circuits?
    a. Data conversion
    b. Arithmetic operations
    c. Data storage
    d. More than one of the above
    e. None of the above

46. Which type of flip-flop is most commonly used in data storage applications?
    a. SR Flip-Flop
    b. D Flip-Flop
    c. JK Flip-Flop
    d. More than one of the above
    e. None of the above

47. Which type of register is used to delay a signal by a specific number of clock cycles?
    a. Shift Register
    b. Buffer Register
    c. Counter Register
    d. More than one of the above
    e. None of the above

48. What does a Johnson counter do with the shifted data?
    a. Shifts in a circular manner
    b. Shifts in a linear manner
    c. Shifts data left or right
    d. More than one of the above
    e. None of the above

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49. Which of the following is NOT an application of a shift register?
    a. Data transmission
    b. Data conversion
    c. Data encryption
    d. More than one of the above
    e. None of the above

50. Which of the following statements about race conditions is true?
    a. They are caused by timing issues
    b. They can be avoided by using synchronous design
    c. They always result in circuit malfunction
    d. More than one of the above
    e. None of the above

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51. Which of the following statements is true about the SR latch?
    a. It can be used for data storage
    b. It has a feedback loop
    c. It can enter a metastable state
    d. More than one of the above
    e. None of the above

52. In a D Flip-Flop, what happens to the output if the D input changes just before the clock edge?
    a. The output immediately changes
    b. The output follows the D input on the next clock edge
    c. The output remains unaffected
    d. More than one of the above
    e. None of the above

53. What is a key characteristic of a T Flip-Flop?
    a. It toggles its state on each clock pulse
    b. It has a single data input
    c. It is used primarily for counting
    d. More than one of the above
    e. None of the above

54. In which of the following cases is a JK Flip-Flop used effectively?
    a. Counters
    b. Shift Registers
    c. Data storage
    d. More than one of the above
    e. None of the above

55. What is the primary advantage of a D Flip-Flop over an SR Flip-Flop?
    a. Reduced complexity
    b. No indeterminate state
    c. Increased clock speed

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d. More than one of the above
e. None of the above

56. Which flip-flop is most suitable for designing a binary counter?
a. SR Flip-Flop
b. D Flip-Flop
c. T Flip-Flop
d. More than one of the above
e. None of the above

57. A race condition is more likely to occur in which type of circuit?
a. Synchronous circuits
b. Asynchronous circuits
c. Both synchronous and asynchronous circuits
d. More than one of the above
e. None of the above

58. In a JK Flip-Flop, what is the state of Q when both J and K inputs are high?
a. Q toggles on each clock pulse
b. Q remains unchanged
c. Q is set to high
d. More than one of the above
e. None of the above

59. Which type of counter counts the number of clock pulses?
a. Modulo-N Counter
b. Ring Counter
c. Johnson Counter
d. More than one of the above
e. None of the above

60. Which shift register type allows for parallel input and serial output?
a. Serial-In Serial-Out (SISO)
b. Parallel-In Serial-Out (PISO)
c. Serial-In Parallel-Out (SIPO)
d. More than one of the above
e. None of the above

61. In a T Flip-Flop, what happens when T = 0?
a. The flip-flop toggles
b. The flip-flop holds its current state
c. The flip-flop resets to 0
d. More than one of the above
e. None of the above

62. Which type of flip-flop is best suited for implementing a frequency divider?
a. SR Flip-Flop
b. D Flip-Flop
c. JK Flip-Flop

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d. More than one of the above
e. None of the above

63. What is the output of an SR Latch when both S and R inputs are high?
a. Q = 0 and Q' = 1
b. Q = 1 and Q' = 0
c. The latch is in an indeterminate state
d. More than one of the above
e. None of the above

64. How does a D Latch differ from a D Flip-Flop?
a. D Latch is level-triggered, D Flip-Flop is edge-triggered
b. D Flip-Flop has an additional clock input
c. D Latch can only be used for storage
d. More than one of the above
e. None of the above

65. Which of the following statements about a JK Flip-Flop is incorrect?
a. It can operate as an SR Flip-Flop
b. It requires additional circuitry for toggling
c. It has no undefined states
d. More than one of the above
e. None of the above

66. In a shift register, what is the purpose of the serial input?
a. To initialize the shift register
b. To provide data to be shifted in
c. To control the shift operation
d. More than one of the above
e. None of the above

67. Which of the following flip-flops is the most complex to design?
a. SR Flip-Flop
b. D Flip-Flop
c. JK Flip-Flop
d. More than one of the above
e. None of the above

68. What is the primary function of a race condition in a circuit?
a. Enhance performance
b. Introduce unpredictable behavior
c. Ensure circuit stability
d. More than one of the above
e. None of the above

69. Which type of counter is also known as a decade counter?
a. Modulo-10 Counter
b. Ring Counter
c. Johnson Counter

d. More than one of the above
e. None of the above

70. In a shift register, what does parallel-out mean?
a. Data is shifted out serially
b. Data is accessed simultaneously from all stages
c. Data is converted to a serial format
d. More than one of the above
e. None of the above

71. What is the main limitation of an SR Flip-Flop compared to a D Flip-Flop?
a. SR Flip-Flop can enter an indeterminate state
b. D Flip-Flop requires more components
c. SR Flip-Flop is slower
d. More than one of the above
e. None of the above

72. In a JK Flip-Flop, which input configuration makes it behave as a T Flip-Flop?
a. J = 1 and K = 0
b. J = 0 and K = 1
c. J = K = 1
d. More than one of the above
e. None of the above

73. Which type of shift register can be used to implement a delay line?
a. Serial-In Serial-Out (SISO)
b. Parallel-In Serial-Out (PISO)
c. Shift Register with feedback
d. More than one of the above
e. None of the above

74. How does a T Flip-Flop differ from a JK Flip-Flop in terms of operation?
a. T Flip-Flop toggles on every clock pulse, JK Flip-Flop toggles only when both J and K are high
b. T Flip-Flop has more inputs
c. JK Flip-Flop can only be used for counting
d. More than one of the above
e. None of the above

75. Which of the following counters can count both up and down?
a. Binary Counter
b. Up/Down Counter
c. Ring Counter
d. More than one of the above
e. None of the above

76. In an SR Latch, what condition will lead to a valid output state?
a. Both S and R are low
b. S = 1 and R = 1
c. S = 0 and R = 1

d. More than one of the above
e. None of the above

77. What is the main advantage of using a D Flip-Flop in synchronous circuits?
a. Avoidance of metastable states
b. Ability to toggle states
c. Simplified design
d. More than one of the above
e. None of the above

78. Which type of shift register allows for serial input and parallel output?
a. Serial-In Parallel-Out (SIPO)
b. Parallel-In Serial-Out (PISO)
c. Serial-In Serial-Out (SISO)
d. More than one of the above
e. None of the above

79. Which flip-flop type is best for creating a divide-by-2 counter?
a. SR Flip-Flop
b. D Flip-Flop
c. JK Flip-Flop
d. More than one of the above
e. None of the above

80. What does the term "race condition" refer to in digital circuits?
a. Reliable operation of the circuit
b. Unpredictable behavior due to timing issues
c. Increased speed of the circuit
d. More than one of the above
e. None of the above

81. In a JK Flip-Flop, what happens when J = 1 and K = 0?
a. Q is set to 1
b. Q is reset to 0
c. Q toggles
d. More than one of the above
e. None of the above

82. Which type of counter is used to count specific sequences like 1, 3, 5, 7, etc.?
a. Binary Counter
b. Johnson Counter
c. Ring Counter
d. More than one of the above
e. None of the above

83. What is the main difference between a shift register and a counter?
a. Shift registers store data, counters count events
b. Counters are used for data manipulation, shift registers for storage
c. Shift registers have feedback loops, counters do not

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d. More than one of the above
e. None of the above

84. What is the typical application of a T Flip-Flop in digital circuits?
a. Data storage
b. Frequency division
c. Data conversion
d. More than one of the above
e. None of the above

85. Which of the following conditions will lead to a race condition in asynchronous circuits?
a. Close timing margins
b. Synchronization of clock signals
c. All components operating at the same speed
d. More than one of the above
e. None of the above

86. In a D Latch, what does the output follow?
a. The clock input
b. The data input
c. The enable signal
d. More than one of the above
e. None of the above

87. Which type of flip-flop is used to construct a frequency divider circuit?
a. SR Flip-Flop
b. D Flip-Flop
c. T Flip-Flop
d. More than one of the above
e. None of the above

88. What is the main advantage of using an asynchronous counter over a synchronous counter?
a. Faster operation
b. Simpler design
c. Higher accuracy
d. More than one of the above
e. None of the above

89. Which type of shift register configuration is used for converting parallel data to serial form?
a. Parallel-In Serial-Out (PISO)
b. Serial-In Parallel-Out (SIPO)
c. Serial-In Serial-Out (SISO)
d. More than one of the above
e. None of the above

90. What is the primary function of the "T" input in a T Flip-Flop?
a. To toggle the output state
b. To set the output to high
c. To reset the output to low

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d. More than one of the above
e. None of the above

91. Which type of counter provides a specific number of states before returning to zero?
a. Modulo-N Counter
b. Ring Counter
c. Johnson Counter
d. More than one of the above
e. None of the above

92. What condition must be met to prevent race conditions in flip-flops?
a. Synchronous clocking
b. Equal timing margins
c. No feedback loops
d. More than one of the above
e. None of the above

93. In a JK Flip-Flop, what is the result when J = 0 and K = 0?
a. The flip-flop toggles
b. The flip-flop holds its current state
c. The flip-flop resets to 0
d. More than one of the above
e. None of the above

94. Which type of register is used for implementing a simple delay line?
a. Shift Register
b. Buffer Register
c. Counter Register
d. More than one of the above
e. None of the above

95. What happens when both inputs are high in an SR Flip-Flop?
a. The state is stable
b. The output is indeterminate
c. The flip-flop resets
d. More than one of the above
e. None of the above

96. In which scenario is a Johnson counter particularly useful?
a. For simple binary counting
b. For counting specific patterns
c. For generating sequences of states
d. More than one of the above
e. None of the above

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97. Which of the following flip-flops is typically used for creating a counter with a known sequence of states?
    a. SR Flip-Flop
    b. D Flip-Flop
    c. JK Flip-Flop
    d. More than one of the above
    e. None of the above

98. What is the primary function of a shift register in serial communication systems?
    a. To store and transmit data sequentially
    b. To convert parallel data to serial format
    c. To perform arithmetic operations
    d. More than one of the above
    e. None of the above

99. In a counter circuit, what does the term "modulo-N" refer to?
    a. The number of states the counter can count before resetting
    b. The maximum frequency the counter can handle
    c. The type of flip-flops used
    d. More than one of the above
    e. None of the above

100. What is a common characteristic of a ripple counter?
    a. Each flip-flop is triggered by the previous one
    b. All flip-flops are clocked by a common clock signal
    c. It is faster than a synchronous counter
    d. More than one of the above
    e. None of the above

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Answers with Explanations

1. **D) More than one of the above**
   SR Latch, D Latch, and JK Latch are all types of latches.
2. **B) Timing is not properly managed**
   A race condition happens when timing issues cause unpredictable behavior.
3. **B) D Latch**
   The D Latch is most commonly used in synchronous systems for data storage.
4. **D) More than one of the above**
   Up, Down, and Up/Down counters are types of counters.
5. **D) More than one of the above**
   Shift registers are used for data storage, transfer, and manipulation.
6. **A) Store one bit of data**
   A D Flip-Flop is used to store a single bit of data.
7. **B) Based on the clock signal**
   In synchronous counters, state changes are driven by a common clock signal.
8. **A) Serial-In Serial-Out (SISO)**
   This type of shift register only shifts data in one direction.
9. **C) The latch is in an indeterminate state**
   In an SR latch, both inputs high can lead to an indeterminate state.
10. **B) Slow speed due to propagation delay**
    Ripple counters are slower due to propagation delays from one flip-flop to the next.
11. **C) Parallel-In Serial-Out (PISO)**
    PISO shift registers convert parallel data into serial data.
12. **B) JK or T Flip-Flop**
    JK or T Flip-Flops are used in frequency divider circuits.
13. **B) Universal Register**
    A Universal Register can shift data both left and right.
14. **C) Synchronize data changes**
    Edge-triggered flip-flops are used to synchronize changes based on clock edges.
15. **A) Synchronous systems**
    Race conditions are less common in synchronous systems due to synchronized clock signals.
16. **B) SR Latch**
    The SR Latch is considered one of the simplest forms of storage.
17. **c) 2n**
    A Johnson counter with n flip-flops has 2n states.
18. **A) Buffer Register**
    Buffer registers are used for temporary data storage and transfer.
19. **A) Q(t+1) = JQ' + K'Q**
    This is the characteristic equation of a JK Flip-Flop.
20. **B) It is primarily used for multiplication**
    Shift registers are used for data shifting, not multiplication.
21. **A) Data input**
    In a D Latch, the output follows the data input when the latch is enabled.

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22. A) Modulo-N Counter
    Modulo-N Counters are used for counting specific events or pulses.
23. A) A common clock pulse
    In synchronous shift registers, all flip-flops are triggered by a common clock pulse.
24. C) It only has one data input
    A D Flip-Flop has a single data input and transfers data on the clock edge.
25. C) Parallel-In Serial-Out (PISO)
    PISO shift registers are often used in digital communications for parallel-to-serial conversion.
26. A) synchronous Counter
    A ring counter is a type of synchronous counter.
27. C) D Flip-Flop
    D Flip-Flops are used for storing binary information and synchronizing data.
28. C) Arithmetic operations
    Shift registers are not used for arithmetic operations.
29. A) Faster speed
    Synchronous counters are faster than asynchronous counters due to synchronized clocking.
30. C) Serial-In Parallel-Out (SIPO)
    SIPO is a type of shift register.
31. A) Shift Register
    Shift registers are used to implement delay lines.
32. A) Synchronous Counter
    A Johnson counter is a type of synchronous counter.
33. B) Data storage and transfer
    Buffer registers are used primarily for storing and transferring data.
34. B) D Latch
    The D Latch is commonly used in memory elements for data storage.
35. A) All flip-flops are clocked by the same clock signal
    Synchronous counters have all flip-flops clocked by the same signal.
36. A) Flip-Flops
    Shift registers can be implemented using flip-flops.
37. B) JK Flip-Flop
    The JK Flip-Flop has a feedback loop in its circuit.
38. B) Propagation delay
    Ripple counters have the disadvantage of propagation delay.
39. B) Parallel-In Serial-Out (PISO)
    PISO shift registers are used for parallel-to-serial conversion.
40. D) More than one of the above
    SR, D, and JK latches can all be edge-triggered in different configurations.
41. B) Count in both directions
    Up/Down counters can count in both directions.
42. A) Ring Counter
    A ring counter shifts data in a circular fashion.
43. A) Two stable states
    Flip-flops are characterized by having two stable states.
44. C) Binary Counter
    A binary counter provides a sequence of states in binary order.

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45. D) More than one of the above
    Shift registers are used for data conversion, shifting, and storage.
46. B) D Flip-Flop
    The D Flip-Flop is most commonly used for data storage applications.
47. A) Shift Register
    Shift registers can be used to delay a signal by a specific number of clock cycles.
48. A) Shifts in a circular manner
    A Johnson counter shifts data in a circular manner.
49. C) Data encryption
    Shift registers are not typically used for data encryption.
50. D) More than one of the above
    Race conditions are caused by timing issues and can be avoided with synchronous design, but they do not always result in malfunction.

51. D) More than one of the above
    SR latches can be used for data storage and have a feedback loop. They can enter a metastable state when both inputs are high.
52. B) The output follows the D input on the next clock edge
    The D Flip-Flop captures the value of the D input on the clock edge.
53. A) It toggles its state on each clock pulse
    The T Flip-Flop toggles its state whenever the T input is high.
54. D) More than one of the above
    JK Flip-Flops are used in counters and data storage applications.
55. B) No indeterminate state
    The D Flip-Flop avoids the indeterminate state issue present in SR Flip-Flops.
56. C) T Flip-Flop
    T Flip-Flops are commonly used for binary counters.
57. B) Asynchronous circuits
    Race conditions are more common in asynchronous circuits due to timing issues.
58. A) Q toggles on each clock pulse
    With both J and K high, the JK Flip-Flop toggles its state on each clock pulse.
59. A) Modulo-N Counter
    Modulo-N Counters count the number of clock pulses up to N.
60. C) Parallel-In Serial-Out (PISO)
    PISO shift registers convert parallel data into serial data.
61. B) The flip-flop holds its current state
    When T = 0, the T Flip-Flop does not toggle and holds its current state.
62. c) JK Flip-Flop
    JK Flip-Flops are used to create frequency dividers.
63. C) The latch is in an indeterminate state
    An SR Latch with both S and R high results in an indeterminate state.
64. A) D Latch is level-triggered, D Flip-Flop is edge-triggered
    D Latch operates with a level-triggered clock, while the D Flip-Flop uses an edge-triggered clock.
65. B) It requires additional circuitry for toggling
    JK Flip-Flops do not require extra circuitry for toggling states.
66. B) To provide data to be shifted in
    The serial input provides data that will be shifted through the shift register.

67. C) JK Flip-Flop
    JK Flip-Flops are more complex due to their additional functionality compared to other flip-flops.
68. B) Introduce unpredictable behavior
    Race conditions cause unpredictable behavior in digital circuits due to timing issues.
69. A) Modulo-10 Counter
    A decade counter counts from 0 to 9 (modulo-10).
70. B) Data is accessed simultaneously from all stages
    Parallel-out shift registers provide data from all stages simultaneously.
71. A) SR Flip-Flop can enter an indeterminate state
    SR Flip-Flops can enter an indeterminate state when both inputs are high.
72. C) J = K = 1
    When J and K are both high, a JK Flip-Flop behaves like a T Flip-Flop.
73. C) Shift Register with feedback
    A shift register with feedback can implement a delay line.
74. A) T Flip-Flop toggles on every clock pulse, JK Flip-Flop toggles only when both J and K are high
    The T Flip-Flop toggles every clock pulse, while the JK Flip-Flop only toggles with J = K = 1.
75. B) Up/Down Counter
    Up/Down Counters can count in both directions.
76. A) Both S and R are low
    For a stable SR Latch state, both S and R should be low.
77. A) Avoidance of metastable states
    D Flip-Flops avoid metastable states, making them suitable for synchronous circuits.
78. A) Serial-In Parallel-Out (SIPO)
    SIPO shift registers convert serial data into parallel data.
79. B) D Flip-Flop
    D Flip-Flops are commonly used to create divide-by-2 counters.
80. B) Unpredictable behavior due to timing issues
    Race conditions lead to unpredictable behavior due to timing issues in circuits.
81. A) Q is set to 1
    With J = 1 and K = 0, the JK Flip-Flop sets Q to 1.
82. B) Johnson Counter
    Johnson Counters can count specific sequences like 1, 3, 5, 7, etc.
83. A) Shift registers store data, counters count events
    Shift registers are used for data storage, while counters are used for counting events.
84. B) Frequency division
    T Flip-Flops are often used for frequency division.
85. A) Close timing margins
    Race conditions are caused by close timing margins and timing issues.
86. B) The data input
    In a D Latch, the output follows the data input when the enable signal is active.
87. C) T Flip-Flop
    T Flip-Flops are used to create frequency dividers by toggling on each clock pulse.
88. B) Simpler design
    Asynchronous counters have a simpler design compared to synchronous counters but can be less accurate.
89. A) Parallel-In Serial-Out (PISO)
    PISO shift registers convert parallel data to serial data.

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90. A) To toggle the output state
The T input in a T Flip-Flop is used to toggle the output state.
91. A) Modulo-N Counter
Modulo-N Counters provide a specific number of states before resetting.
92. A) Synchronous clocking
Synchronous clocking helps prevent race conditions by ensuring all flip-flops are clocked simultaneously.
93. B) The flip-flop holds its current state
With J = 0 and K = 0, the JK Flip-Flop holds its current state.
94. A) Shift Register
Shift Registers are used for implementing simple delay lines.
95. B) The output is indeterminate
When both inputs are high in an SR Flip-Flop, the output is indeterminate.
96. C) For generating sequences of states
Johnson Counters are useful for generating specific sequences of states.
97. C) JK Flip-Flop
JK Flip-Flops are commonly used to create counters with known sequences of states.
98. A) To store and transmit data sequentially
Shift Registers store and transmit data sequentially in serial communication systems.
99. A) The number of states the counter can count before resetting
Modulo-N refers to the number of states a counter can count before resetting.
100. A) Each flip-flop is triggered by the previous one
In a ripple counter, each flip-flop is triggered by the output of the previous flip-flop.

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