Assignment-#6

Logic Families/ ADC/DAC/PLDs

Note: Take printout of these questions try to solve and tick answer by your own

1. **Which of the following logic families has the highest noise margin?**
   - **(A) TTL**
   - **(B) CMOS**
   - **(C) ECL**
   - **(D) More than one of the above**
   - **(E) None of the above**

2. **What is the main disadvantage of TTL logic families?**
   - **(A) High power consumption**
   - **(B) Low switching speed**
   - **(C) Low noise immunity**
   - **(D) More than one of the above**
   - **(E) None of the above**

3. **Which type of ADC uses a binary search algorithm to convert analog signals into digital signals?**
   - **(A) Flash ADC**
   - **(B) Successive Approximation Register (SAR) ADC**
   - **(C) Delta-Sigma ADC**
   - **(D) More than one of the above**
   - **(E) None of the above**

4. **Which of the following DACs provides the fastest conversion time?**
   - **(A) R-2R Ladder DAC**
   - **(B) Weighted Resistor DAC**
   - **(C) Flash DAC**
   - **(D) More than one of the above**
   - **(E) None of the above**

5. **Which logic family is known for its low power consumption and high noise immunity?**
   - **(A) TTL**
   - **(B) CMOS**
   - **(C) ECL**
   - **(D) More than one of the above**
   - **(E) None of the above**

6. **Which of the following ADCs is best suited for high-frequency signals?**
   - **(A) Dual Slope ADC**
   - **(B) Successive Approximation Register (SAR) ADC**
   - **(C) Flash ADC**
   - **(D) More than one of the above**
   - **(E) None of the above**

7. Which PLD is characterized by having a fixed OR array and a programmable AND array?
   (A) PLA
   (B) PAL
   (C) CPLD
   (D) More than one of the above
   (E) None of the above

8. Which of the following statements is true about Flash ADC?
   (A) It is very slow but accurate.
   (B) It uses a binary-weighted resistor network.
   (C) It provides an output in a single step.
   (D) More than one of the above
   (E) None of the above

9. What is the primary application of a Digital-to-Analog Converter (DAC)?
   (A) Converting digital signals to analog for display systems
   (B) Converting analog signals to digital for processing
   (C) Noise filtering in digital systems
   (D) More than one of the above
   (E) None of the above

10. In a CMOS logic family, what is the main cause of power dissipation?
   (A) Static current
   (B) Dynamic current due to switching
   (C) Leakage current
   (D) More than one of the above
   (E) None of the above

11. Which of the following logic families is the fastest?
   (A) CMOS
   (B) TTL
   (C) ECL
   (D) More than one of the above
   (E) None of the above

12. Which type of ADC is most suitable for applications requiring high resolution?
   (A) Flash ADC
   (B) Successive Approximation Register (SAR) ADC
   (C) Delta-Sigma ADC
   (D) More than one of the above
   (E) None of the above

13. Which PLD uses a matrix of AND and OR gates to implement logic functions?
   (A) PLA
   (B) PAL
   (C) FPGA
   (D) More than one of the above
   (E) None of the above

14. Which type of DAC is known for its simplicity and low cost?
    (A) R-2R Ladder DAC
    (B) Weighted Resistor DAC
    (C) Sigma-Delta DAC
    (D) More than one of the above
    (E) None of the above

15. Which logic family is typically used in high-speed applications like telecommunications?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

16. What is a significant advantage of PAL over PLA?
    (A) Flexibility in design
    (B) Faster speed due to fixed OR gates
    (C) Higher power consumption
    (D) More than one of the above
    (E) None of the above

17. Which component of an ADC determines its resolution?
    (A) Clock frequency
    (B) Number of bits
    (C) Reference voltage
    (D) More than one of the above
    (E) None of the above

18. Which of the following is a disadvantage of using a Weighted Resistor DAC?
    (A) High power consumption
    (B) High accuracy requirement for resistors
    (C) Slow conversion rate
    (D) More than one of the above
    (E) None of the above

19. Which logic family offers a trade-off between speed and power consumption?
    (A) CMOS
    (B) TTL
    (C) BiCMOS
    (D) More than one of the above
    (E) None of the above

20. Which type of ADC uses an integrator in its design?
    (A) Flash ADC
    (B) Dual Slope ADC
    (C) Successive Approximation Register (SAR) ADC
    (D) More than one of the above
    (E) None of the above

21. What is the primary feature of ECL logic family?
    (A) High power dissipation
    (B) Low noise margin
    (C) High speed
    (D) More than one of the above
    (E) None of the above

22. Which PLD can be reprogrammed multiple times?
    (A) PLA
    (B) PAL
    (C) FPGA
    (D) More than one of the above
    (E) None of the above

23. Which DAC architecture requires precise resistor matching?
    (A) R-2R Ladder DAC
    (B) Weighted Resistor DAC
    (C) Sigma-Delta DAC
    (D) More than one of the above
    (E) None of the above

24. Which type of ADC is most suitable for audio applications?
    (A) Flash ADC
    (B) Sigma-Delta ADC
    (C) Dual Slope ADC
    (D) More than one of the above
    (E) None of the above

25. Which logic family is used in low-power digital watch applications?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

26. Which type of DAC offers the best linearity?
    (A) R-2R Ladder DAC
    (B) Weighted Resistor DAC
    (C) Current Steering DAC
    (D) More than one of the above
    (E) None of the above

27. Which logic family provides the best combination of power efficiency and speed?
    (A) CMOS
    (B) TTL
    (C) BiCMOS
    (D) More than one of the above
    (E) None of the above

28. Which ADC is known for being very accurate but slow in operation?
    (A) Flash ADC
    (B) Dual Slope ADC
    (C) Successive Approximation Register (SAR) ADC
    (D) More than one of the above
    (E) None of the above

29. Which type of PLD is ideal for implementing simple combinational logic?
    (A) PLA
    (B) PAL
    (C) CPLD
    (D) More than one of the above
    (E) None of the above

30. What is the main advantage of a Flash ADC?
    (A) Low power consumption
    (B) High speed
    (C) Low cost
    (D) More than one of the above
    (E) None of the above

31. Which type of DAC is least affected by parasitic capacitance?
    (A) R-2R Ladder DAC
    (B) Weighted Resistor DAC
    (C) Current Steering DAC
    (D) More than one of the above
    (E) None of the above

32. Which logic family is typically used in high-temperature environments?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

33. Which ADC is most suitable for digital signal processing (DSP) applications?
    (A) Flash ADC
    (B) SAR ADC
    (C) Sigma-Delta ADC
    (D) More than one of the above
    (E) None of the above

34. Which PLD is preferred when multiple programmable devices are needed on a single chip?
    (A) PLA
    (B) PAL
    (C) CPLD
    (D) More than one of the above
    (E) None of the above

35. Which type of DAC requires a reference voltage for operation?
    (A) R-2R Ladder DAC
    (B) Weighted Resistor DAC
    (C) Current Steering DAC
    (D) More than one of the above
    (E) None of the above

36. Which of the following logic families offers the best power-delay product?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

37. Which ADC uses a digital-to-analog converter in its architecture?
    (A) Flash ADC
    (B) Successive Approximation Register (SAR) ADC
    (C) Sigma-Delta ADC
    (D) More than one of the above
    (E) None of the above

38. Which type of PLD allows the designer to implement both combinational and sequential logic?
    (A) PLA
    (B) PAL
    (C) FPGA
    (D) More than one of the above
    (E) None of the above

39. Which DAC is most commonly used in audio applications?
    (A) R-2R Ladder DAC
    (B) Weighted Resistor DAC
    (C) Sigma-Delta DAC
    (D) More than one of the above
    (E) None of the above

40. Which logic family is considered the most robust in terms of radiation resistance?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

41. Which type of ADC architecture is commonly used in oscilloscopes?
    (A) Flash ADC
    (B) SAR ADC
    (C) Sigma-Delta ADC
    (D) More than one of the above
    (E) None of the above

42. Which type of PLD is more flexible and supports higher density logic designs?
    (A) PLA
    (B) PAL
    (C) FPGA
    (D) More than one of the above
    (E) None of the above

43. Which DAC provides the fastest settling time?
    (A) R-2R Ladder DAC
    (B) Weighted Resistor DAC
    (C) Current Steering DAC
    (D) More than one of the above
    (E) None of the above

44. Which logic family provides the highest fan-out capability?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

45. Which type of ADC is used when low power consumption is critical?
    (A) Flash ADC
    (B) SAR ADC
    (C) Sigma-Delta ADC
    (D) More than one of the above
    (E) None of the above

46. Which PLD is known for having the lowest propagation delay?
    (A) PLA
    (B) PAL
    (C) CPLD
    (D) More than one of the above
    (E) None of the above

47. Which type of DAC is most suitable for applications requiring low glitch energy?
    (A) R-2R Ladder DAC
    (B) Weighted Resistor DAC
    (C) Current Steering DAC
    (D) More than one of the above
    (E) None of the above

48. Which logic family is used for ultra-high-speed digital circuits?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

49. Which ADC provides the best combination of speed and resolution?
    (A) Flash ADC
    (B) SAR ADC
    (C) Sigma-Delta ADC
    (D) More than one of the above
    (E) None of the above

50. Which PLD is preferred for rapid prototyping of digital circuits?
    (A) PLA
    (B) PAL
    (C) FPGA
    (D) More than one of the above
    (E) None of the above

51. Which logic family is most suitable for low-voltage applications?
    (A) TTL
    (B) CMOS
    (C) ECL
    (D) More than one of the above
    (E) None of the above

52. Which logic family has the lowest power dissipation during static operation?
    (A) TTL
    (B) CMOS
    (C) BiCMOS
    (D) More than one of the above
    (E) None of the above

53. Which logic family is known for having a high input impedance?
    (A) TTL
    (B) CMOS
    (C) ECL
    (D) More than one of the above
    (E) None of the above

54. Which of the following logic families uses bipolar junction transistors in its design?
    (A) CMOS
    (B) TTL
    (C) MOSFET
    (D) More than one of the above
    (E) None of the above

55. Which logic family provides the best noise margin for digital circuits?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

56. Which type of logic family is commonly used in battery-powered devices?
    (A) TTL
    (B) CMOS
    (C) ECL
    (D) More than one of the above
    (E) None of the above

57. Which logic family is most commonly used in analog circuit applications?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

58. Which logic family is known for its high fan-in capability?
    (A) TTL
    (B) CMOS
    (C) ECL
    (D) More than one of the above
    (E) None of the above

59. Which logic family is best suited for use in space applications due to its high radiation resistance?
    (A) TTL
    (B) CMOS
    (C) BiCMOS
    (D) More than one of the above
    (E) None of the above

60. Which logic family provides the fastest switching speed?
    (A) TTL
    (B) CMOS
    (C) ECL
    (D) More than one of the above
    (E) None of the above

61. Which of the following logic families is the most suitable for very large-scale integration (VLSI) circuits?
    (A) TTL
    (B) CMOS
    (C) ECL
    (D) More than one of the above
    (E) None of the above

62. Which logic family is characterized by low noise margin?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

63. Which of the following logic families offers a good balance between power consumption and switching speed?
    (A) CMOS
    (B) TTL
    (C) BiCMOS
    (D) More than one of the above
    (E) None of the above

64. Which logic family uses differential amplifier logic to achieve high speed?
    (A) TTL
    (B) CMOS
    (C) ECL
    (D) More than one of the above
    (E) None of the above

65. Which logic family is preferred for ultra-low power applications?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

66. Which of the following logic families operates at the highest voltage range?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

67. Which logic family is most immune to electrostatic discharge (ESD)?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

68. Which of the following logic families is typically used in high-performance computing?
    (A) TTL
    (B) CMOS
    (C) ECL
    (D) More than one of the above
    (E) None of the above

69. Which logic family offers the highest noise immunity?
    (A) TTL
    (B) CMOS
    (C) ECL
    (D) More than one of the above
    (E) None of the above

70. Which of the following logic families has the highest input capacitance?
    (A) CMOS
    (B) TTL
    (C) ECL
    (D) More than one of the above
    (E) None of the above

Answers and Explanations

1. Answer: (B) CMOS
   Explanation: CMOS logic families have the highest noise margin compared to TTL and ECL, making them more immune to noise.
2. Answer: (A) High power consumption
   Explanation: TTL logic families consume more power compared to CMOS, which is a significant disadvantage.
3. Answer: (B) Successive Approximation Register (SAR) ADC
   Explanation: SAR ADC uses a binary search algorithm to approximate the input analog signal.
4. Answer: (C) Flash DAC
   Explanation: Flash DACs are the fastest among DAC types, as they use a parallel conversion process.
5. Answer: (B) CMOS
   Explanation: CMOS is known for its low power consumption and high noise immunity compared to other logic families.
6. Answer: (C) Flash ADC
   Explanation: Flash ADC is best suited for high-frequency signals due to its fast conversion rate.
7. Answer: (B) PAL
   Explanation: PAL has a fixed OR array and a programmable AND array, making it faster than PLA but less flexible.
8. Answer: (C) It provides an output in a single step
   Explanation: Flash ADCs convert signals in a single step, making them very fast.
9. Answer: (A) Converting digital signals to analog for display systems
   Explanation: DACs are primarily used to convert digital signals to analog form, which is essential in display systems and other applications.
10. Answer: (B) Dynamic current due to switching

11. Answer: (C) ECL
    Explanation: Emitter-Coupled Logic (ECL) is the fastest logic family due to its differential amplifier design, which avoids saturation and allows for high-speed operation.
12. Answer: (C) Delta-Sigma ADC
    Explanation: Delta-Sigma ADCs provide high resolution due to oversampling and noise shaping techniques, making them ideal for high-precision applications.
13. Answer: (A) PLA
    Explanation: A Programmable Logic Array (PLA) uses both programmable AND and OR gates to implement complex logic functions, offering flexibility in design.
14. Answer: (A) R-2R Ladder DAC
    Explanation: The R-2R Ladder DAC is simple in design, requiring only two resistor values, and is cost-effective compared to other DAC types.
15. Answer: (C) ECL
    Explanation: ECL is commonly used in high-speed applications like telecommunications because of its very fast switching speed.
16. Answer: (B) Faster speed due to fixed OR gates
    Explanation: PAL devices have a fixed OR array, making them faster than PLAs, which have both programmable AND and OR arrays.
17. Answer: (B) Number of bits
    Explanation: The resolution of an ADC is determined by the number of bits in its output. More bits mean higher resolution and more precise representation of the analog input.

18. Answer: (B) High accuracy requirement for resistors
    Explanation: Weighted Resistor DACs require precise resistor values to maintain accuracy, which can be difficult and costly to achieve.
19. Answer: (C) BiCMOS
    Explanation: BiCMOS technology combines the speed of Bipolar Junction Transistors (BJT) with the low power consumption of CMOS, providing a balanced trade-off.
20. Answer: (B) Dual Slope ADC
    Explanation: Dual Slope ADCs use an integrator in their design to integrate the input signal, making them accurate but relatively slow.
21. Answer: (D) More than one of the above
    Explanation: ECL has both high power dissipation and high speed. It also has a low noise margin compared to CMOS and TTL.
22. Answer: (C) FPGA
    Explanation: Field-Programmable Gate Arrays (FPGAs) can be reprogrammed multiple times, offering flexibility and versatility in digital design.
23. Answer: (B) Weighted Resistor DAC
    Explanation: Weighted Resistor DACs need precise resistor matching to ensure accurate digital-to-analog conversion, making them sensitive to component variations.
24. Answer: (B) Sigma-Delta ADC
    Explanation: Sigma-Delta ADCs are well-suited for audio applications due to their high resolution and ability to filter out high-frequency noise.
25. Answer: (A) CMOS
    Explanation: CMOS technology is used in low-power applications like digital watches due to its low power consumption and ability to operate at low voltages.
26. Answer: (C) Current Steering DAC
    Explanation: Current Steering DACs provide excellent linearity and fast switching, making them ideal for high-precision applications.
27. Answer: (C) BiCMOS
    Explanation: BiCMOS technology provides a good balance between power efficiency and speed, combining the advantages of both CMOS and bipolar technologies.
28. Answer: (B) Dual Slope ADC
    Explanation: Dual Slope ADCs are known for their high accuracy but are relatively slow compared to other types like Flash ADCs.
29. Answer: (B) PAL
    Explanation: PAL devices are ideal for implementing simple combinational logic due to their simpler and faster architecture compared to PLAs.
30. Answer: (B) High speed
    Explanation: Flash ADCs are known for their high-speed operation as they convert analog signals to digital in a single step.
31. Answer: (A) R-2R Ladder DAC
    Explanation: The R-2R Ladder DAC is less affected by parasitic capacitance because of its uniform resistor network design.
32. Answer: (C) ECL
    Explanation: ECL is often used in high-temperature environments due to its ability to operate without the transistors going into saturation.
33. Answer: (C) Sigma-Delta ADC
    Explanation: Sigma-Delta ADCs are commonly used in digital signal processing (DSP) applications due to their high resolution and noise shaping capabilities.

34. Answer: (C) CPLD
    Explanation: Complex Programmable Logic Devices (CPLDs) support higher density logic designs on a single chip, making them more flexible.
35. Answer: (D) More than one of the above
    Explanation: Both R-2R Ladder DACs and Weighted Resistor DACs require a reference voltage to perform digital-to-analog conversion.
36. Answer: (A) CMOS
    Explanation: CMOS technology provides the best power-delay product due to its low power consumption and moderate speed.
37. Answer: (B) Successive Approximation Register (SAR) ADC
    Explanation: SAR ADCs use a digital-to-analog converter internally to approximate the input analog signal during conversion.
38. Answer: (C) FPGA
    Explanation: FPGAs allow for the implementation of both combinational and sequential logic, providing high flexibility in design.
39. Answer: (C) Sigma-Delta DAC
    Explanation: Sigma-Delta DACs are widely used in audio applications due to their high resolution and noise filtering capabilities.
40. Answer: (A) CMOS
    Explanation: CMOS logic families are known for their robustness against radiation, making them suitable for space and nuclear applications.
41. Answer: (A) Flash ADC
    Explanation: Flash ADCs are used in oscilloscopes for their high-speed conversion, which is crucial for capturing fast transient signals.
42. Answer: (C) FPGA
    Explanation: FPGAs offer high flexibility and support higher density logic designs, making them suitable for complex and large-scale digital systems.
43. Answer: (C) Current Steering DAC
    Explanation: Current Steering DACs provide fast settling times due to their architecture, which minimizes capacitance effects.
44. Answer: (B) TTL
    Explanation: TTL logic families provide high fan-out capability, meaning they can drive multiple outputs from a single input signal.
45. Answer: (B) SAR ADC
    Explanation: Successive Approximation Register (SAR) ADCs are designed for low power consumption, making them suitable for battery-operated devices.
46. Answer: (B) PAL
    Explanation: PAL devices typically have lower propagation delays due to their simpler architecture compared to other PLDs like CPLDs and FPGAs.
47. Answer: (C) Current Steering DAC
    Explanation: Current Steering DACs are most suitable for applications requiring low glitch energy due to their controlled current paths.
48. Answer: (C) ECL
    Explanation: ECL is used in ultra-high-speed digital circuits due to its very fast switching characteristics and differential amplifier design.
49. Answer: (D) More than one of the above
    Explanation: Both SAR and Sigma-Delta ADCs provide a good balance of speed and resolution, depending on the application requirements.

50. Answer: (C) FPGA
Explanation: FPGAs are preferred for rapid prototyping of digital circuits due to their reprogrammable nature and flexibility in implementing complex logic designs.

51. Answer: (B) CMOS
Explanation: CMOS (Complementary Metal-Oxide-Semiconductor) is most suitable for low-voltage applications due to its low power consumption and the ability to operate efficiently at low voltages.

52. Answer: (B) CMOS
Explanation: CMOS logic family has the lowest power dissipation during static operation as it only consumes significant power during switching.

53. Answer: (B) CMOS
Explanation: CMOS logic family is known for having a high input impedance, which results in minimal input current draw.

54. Answer: (B) TTL
Explanation: Transistor-Transistor Logic (TTL) uses bipolar junction transistors (BJTs) in its internal design.

55. Answer: (A) CMOS
Explanation: CMOS offers the best noise margin, making it highly suitable for digital circuits that require noise immunity.

56. Answer: (B) CMOS
Explanation: Due to its low power consumption, CMOS is commonly used in battery-powered devices such as calculators, digital watches, and portable electronics.

57. Answer: (A) CMOS
Explanation: CMOS is most commonly used in analog circuit applications, such as mixed-signal ICs, due to its ability to handle both analog and digital signals.

58. Answer: (C) ECL
Explanation: ECL (Emitter-Coupled Logic) has a high fan-in capability because it operates without transistor saturation, allowing for more inputs to be connected.

59. Answer: (B) CMOS
Explanation: CMOS is most suitable for space applications because of its high resistance to radiation effects, ensuring reliable performance in harsh environments.

60. Answer: (C) ECL
Explanation: ECL is the fastest logic family due to its differential amplifier configuration that avoids transistor saturation, allowing for very high-speed operation.

61. Answer: (B) CMOS
Explanation: CMOS technology is most suitable for Very Large Scale Integration (VLSI) circuits because of its low power consumption and scalability.

62. Answer: (C) ECL
Explanation: ECL has a lower noise margin compared to CMOS and TTL, making it more sensitive to noise.

63. Answer: (C) BiCMOS
Explanation: BiCMOS technology combines the advantages of CMOS (low power consumption) and bipolar transistors (high speed), providing a good balance.

64. Answer: (C) ECL
Explanation: ECL uses differential amplifier logic to achieve high-speed operation, which is its primary characteristic.

65. Answer: (A) CMOS
Explanation: CMOS is preferred for ultra-low power applications, such as battery-operated devices, due to its minimal power consumption when not switching.

66. Answer: (B) TTL
Explanation: TTL operates at a higher voltage range (typically 5V) compared to CMOS, which operates at lower voltages.

67. **Answer: (A) CMOS**
    Explanation: CMOS technology is more immune to electrostatic discharge (ESD) than other logic families because of its high input impedance and lower current levels.
68. **Answer: (C) ECL**
    Explanation: ECL is typically used in high-performance computing where speed is a critical factor, such as in supercomputers and network equipment.
69. **Answer: (A) CMOS**
    Explanation: CMOS offers high noise immunity due to its high input impedance and low power consumption, making it less susceptible to noise interference.
70. **Answer: (A) CMOS**
    Explanation: CMOS logic families tend to have higher input capacitance compared to TTL and ECL, which can affect their speed at higher frequencies.