Assignment-#1
Computer Organization MCQ

1. Flynn's Taxonomy classifies computer architectures based on:
   (A) Number of processors and Memory units
   (B) Number of instructions and data streams
   (C) Speed of processing
   (D) More than one of the above
   (E) None of the above

2. Which of the following is NOT a category in Flynn's Taxonomy?
   (A) SISD
   (B) MIMD
   (C) MISD
   (D) More than one of the above
   (E) None of the above

3. An example of SIMD architecture is:
   (A) A vector processor
   (B) A multi-core processor
   (C) A pipeline processor
   (D) More than one of the above
   (E) None of the above

4. Which Flynn's taxonomy category corresponds to parallel computers?
   (A) MIMD
   (B) SIMD
   (C) SISD
   (D) More than one of the above
   (E) None of the above

5. Which category does a traditional uniprocessor belong to in Flynn's Taxonomy?
   (A) SISD
   (B) SIMD
   (C) MIMD
   (D) More than one of the above
   (E) None of the above

6. Which of the following is a characteristic of RISC architecture?
   (A) Fewer instructions
   (B) Simple instruction set
   (C) Fixed instruction length
   (D) More than one of the above
   (E) None of the above

7. In RISC architecture, instructions are generally:
   (A) Complex
   (B) Simple
   (C) Variable in length
   (D) More than one of the above
   (E) None of the above

8. CISC architecture typically has:
   (A) Fewer instructions
   (B) More instructions
   (C) Variable instruction lengths
   (D) More than one of the above
   (E) None of the above

9. Which of the following is a major advantage of RISC over CISC?
   (A) Lower power consumption
   (B) Faster instruction execution
   (C) Simpler hardware design
   (D) More than one of the above
   (E) None of the above

10. A key feature of CISC architecture is:
    (A) Use of a large number of addressing modes
    (B) Complex microprogramming
    (C) Variable instruction length
    (D) More than one of the above
    (E) None of the above

11. Machine instructions typically include:
    (A) Operation code (Opcode)
    (B) Operands
    (C) Instruction format
    (D) More than one of the above
    (E) None of the above

12. Which of the following are examples of arithmetic instructions?
    (A) ADD
    (B) SUB
    (C) MUL
    (D) More than one of the above
    (E) None of the above

13. Branch instructions are used for:
    (A) Arithmetic operations
    (B) Data transfer
    (C) Changing the flow of execution
    (D) More than one of the above
    (E) None of the above

14. A machine instruction is executed in which phase of the instruction cycle?
    (A) Fetch
    (B) Decode
    (C) Execute
    (D) More than one of the above
    (E) None of the above

15. Which instruction type transfers data from memory to a processor register?
    (A) Arithmetic instruction
    (B) Control instruction
    (C) Data transfer instruction
    (D) More than one of the above
    (E) None of the above

16. The instruction cycle consists of:
    (A) Fetch
    (B) Decode
    (C) Execute
    (D) More than one of the above
    (E) None of the above

17. Which step comes first in the instruction cycle?
    (A) Decode
    (B) Fetch
    (C) Execute
    (D) More than one of the above
    (E) None of the above

18. During the fetch phase, the CPU:
    (A) Fetches the instruction from memory
    (B) Decodes the instruction
    (C) Executes the instruction
    (D) More than one of the above
    (E) None of the above

19. The instruction cycle ends after the:
    (A) Execute phase
    (B) Fetch phase

(C) Decode phase
(D) More than one of the above
(E) None of the above

20. The purpose of the decode phase is to:
(A) Interpret the fetched instruction
(B) Load data into registers
(C) Execute the operation
(D) More than one of the above
(E) None of the above

21. An instruction format defines:
(A) The structure of an instruction
(B) The opcode and operands
(C) The memory addresses involved
(D) More than one of the above
(E) None of the above

22. The number of bits required for an instruction format is dependent on:
(A) The number of addressing modes
(B) The number of operands
(C) The number of instructions
(D) More than one of the above
(E) None of the above

23. In a typical instruction format, the operand field contains:
(A) Operation code
(B) Data to be processed
(C) Address of data or register
(D) More than one of the above
(E) None of the above

24. A two-address instruction format typically has:
(A) Two operands
(B) One operand
(C) No operand
(D) More than one of the above
(E) None of the above

25. Which format is used for loading data into a register?
(A) Zero-address instruction
(B) One-address instruction
(C) Two-address instruction
(D) More than one of the above
(E) None of the above

26. In a single accumulator organization:
    (A) One accumulator register is used
    (B) Two accumulators are used
    (C) Data is loaded directly into memory
    (D) More than one of the above
    (E) None of the above

27. General register CPU organization:
    (A) Utilizes multiple general-purpose registers
    (B) Only uses an accumulator
    (C) Uses a single program counter
    (D) More than one of the above
    (E) None of the above

28. The stack-based CPU organization uses:
    (A) General-purpose registers
    (B) A stack for storing intermediate results
    (C) Multiple accumulators
    (D) More than one of the above
    (E) None of the above

29. Which CPU organization is most suited for high-level language support?
    (A) General register organization
    (B) Single accumulator organization
    (C) Stack organization
    (D) More than one of the above
    (E) None of the above

30. Which CPU organization typically uses two-operand instructions?
    (A) General register organization
    (B) Single accumulator organization
    (C) Stack-based organization
    (D) More than one of the above
    (E) None of the above

31. Which of the following describes a Von Neumann architecture?
    (A) Single memory for instructions and data
    (B) Separate memory for instructions and data
    (C) Single control unit
    (D) More than one of the above
    (E) None of the above

32. A Harvard architecture typically has:
    (A) Separate instruction and data memory
    (B) Unified instruction and data memory
    (C) Multiple control units
    (D) More than one of the above
    (E) None of the above

33. Which architecture is most commonly used in modern processors?
    (A) Von Neumann
    (B) Harvard
    (C) SISD
    (D) More than one of the above
    (E) None of the above

34. Which of the following describes a superscalar architecture?
    (A) Can issue multiple instructions per clock cycle
    (B) Executes instructions one at a time
    (C) Uses multiple pipelines
    (D) More than one of the above
    (E) None of the above

35. In a pipelined architecture, which stage overlaps with instruction fetch?
    (A) Execute
    (B) Decode
    (C) Write-back
    (D) More than one of the above
    (E) None of the above

36. A zero-address instruction format uses:
    (A) No operands
    (B) One operand
    (C) Two operands
    (D) More than one of the above
    (E) None of the above

37. The one-address instruction format is typically used in:
    (A) Stack-based CPUs
    (B) Accumulator-based CPUs
    (C) General register-based CPUs
    (D) More than one of the above
    (E) None of the above

38. The two-address instruction format:
    (A) Has two operand addresses
    (B) Uses an accumulator
    (C) Requires a stack
    (D) More than one of the above
    (E) None of the above

39. Three-address instruction format:
    (A) Has three operands
    (B) Requires a stack
    (C) Stores results in a register
    (D) More than one of the above
    (E) None of the above

40. Which of the following fields is not typically part of an instruction format?
    (A) Opcode
    (B) Operands
    (C) Program counter
    (D) More than one of the above
    (E) None of the above

Answer With Explanation:

1. **(B) Number of instructions and data streams**
   Explanation: Flynn's Taxonomy categorizes architectures based on the number of concurrent instruction and data streams processed by a system. Option (A), the number of processors, is indirectly relevant but not the primary focus. Speed of processing (C) is not part of the taxonomy, and hence (D) and (E) are incorrect.
2. **(E) None of the above**
   Explanation: Flynn's Taxonomy consists of SISD, SIMD, MISD, and MIMD, all of which are valid categories. Therefore, (E) is correct since all provided categories (A, B, C, D) are part of the taxonomy.
3. **(A) A vector processor**
   Explanation: SIMD (Single Instruction, Multiple Data) refers to architectures like vector processors that operate on multiple data points simultaneously using a single instruction. Multi-core processors (B) are generally categorized under MIMD. Pipeline processors (C) relate more to instruction-level parallelism, not data-level parallelism as in SIMD.
4. **(D) More than one of the above**
   Explanation: Both SIMD (B) and MIMD (A) are used for parallel processing. SIMD processes multiple data streams with a single instruction, while MIMD handles multiple instructions and data streams. Hence, more than one option is correct.
5. **(A) SISD**
   Explanation: A traditional uniprocessor belongs to the SISD (Single Instruction, Single Data) category, which processes one instruction and one data stream at a time. SIMD and MIMD handle parallel tasks, making them incorrect for this question.
6. **(D) More than one of the above**
   Explanation: RISC (Reduced Instruction Set Computer) architectures feature fewer instructions (A), a simple instruction set (B), and fixed instruction length (C). Hence, more than one option is correct.
7. **(B) Simple**
   Explanation: RISC architectures are designed around simple instructions that can be executed in a single clock cycle. Complex instructions (A) and variable lengths (C) are characteristics of CISC, not RISC.
8. **(D) More than one of the above**
   Explanation: CISC (Complex Instruction Set Computer) architectures have more instructions (B) and variable instruction lengths (C). Option (A), fewer instructions, is incorrect, making (D) the right choice.
9. **(D) More than one of the above**
   Explanation: RISC architectures generally offer faster instruction execution (B), simpler hardware design (C), and lower power consumption (A). Hence, more than one option is correct.
10. **(D) More than one of the above**
    Explanation: CISC architectures are characterized by the use of many addressing modes (A), complex microprogramming (B), and variable instruction lengths (C). Therefore, more than one option is correct.
11. **(D) More than one of the above**
    Explanation: Machine instructions typically include the opcode (A), operands (B), and instruction format (C), hence, more than one of the above.
12. **(D) More than one of the above**
    Explanation: Arithmetic instructions like ADD (A), SUB (B), and MUL (C) are examples, so more than one of the above is correct.
13. **(C) Changing the flow of execution**
    Explanation: Branch instructions alter the flow of control by directing the CPU to another instruction (not arithmetic or data transfer).

14. (D) More than one of the above
    Explanation: The machine instruction can be decoded (B), fetched (A), and executed (C) in different phases of the instruction cycle.
15. (C) Data transfer instruction
    Explanation: Data transfer instructions (C) move data from memory to registers, unlike arithmetic (A) or control instructions (B).
16. (D) More than one of the above
    Explanation: The instruction cycle includes fetch (A), decode (B), and execute (C) phases, so more than one of the above is correct.
17. (B) Fetch
    Explanation: Fetch is the first phase of the instruction cycle, where the instruction is retrieved from memory before decoding and execution.
18. Fetches the instruction from memory
    Explanation: During the fetch phase, the CPU retrieves the instruction from memory. Decoding (B) and execution (C) happen afterward.
19. Execute phase
    Explanation: The instruction cycle ends after the execute phase, where the operation specified by the instruction is performed.
20. Interpret the fetched instruction
    Explanation: In the decode phase, the CPU interprets the fetched instruction. Loading data (B) and executing (C) occur later.

21. (D) More than one of the above
    Explanation: An instruction format includes the structure (A), opcode (B), and operands or addresses (C), making more than one of the above correct.
22. (D) More than one of the above
    Explanation: The number of bits depends on the addressing modes (A), operands (B), and instructions (C), so more than one of the above is correct.
23. Address of data or register
    Explanation: The operand field typically contains the address of data or a register, not the operation code (A) or data itself (B).
24. Two operands
    Explanation: A two-address instruction format involves two operands, one for the source and one for the destination.
25. One-address instruction
    Explanation: One-address instructions are often used for loading data into registers. Zero-address (A) and two-address (C) instructions have different uses.
26. One accumulator register is used
    Explanation: In a single accumulator organization, all operations are performed using one accumulator, while other options refer to more complex architectures.
27. Utilizes multiple general-purpose registers
    Explanation: General register organizations use multiple registers, unlike accumulators (B) or stack-based organizations.

28. A stack for storing intermediate results
    Explanation: Stack-based CPUs use a stack to hold intermediate results. General registers (A) or multiple accumulators (C) are not used.
29. General register organization
    Explanation: General register organization is well-suited for high-level languages due to its flexibility and support for various instructions.
30. General register organization
    Explanation: General register organizations typically use two-operand instructions, where operations involve two general-purpose registers.
31. Single memory for instructions and data
    Explanation: In a Von Neumann architecture, both data and instructions share the same memory space. Harvard architecture (B) separates them.
32. Separate instruction and data memory
    Explanation: Harvard architecture separates instruction and data memory, unlike Von Neumann architecture (B), which uses a unified memory.
33. Von Neumann
    Explanation: Modern processors typically follow the Von Neumann architecture, while Harvard (B) is used in specialized applications like microcontrollers.
34. More than one of the above
    Explanation: A superscalar architecture can issue multiple instructions per clock cycle (A) and use multiple pipelines (C), so more than one is correct.
35. Decode
    Explanation: In a pipelined architecture, the fetch stage overlaps with the decode stage, while the execution and write-back phases occur later.
36. No operands
    Explanation: A zero-address instruction format operates with no explicit operands, often using a stack instead.
37. Accumulator-based CPUs
    Explanation: One-address instructions are common in accumulator-based CPUs, while stack-based (A) and general register-based (C) CPUs use other formats.
38. Has two operand addresses
    Explanation: A two-address instruction format uses two operands—one for the source and one for the destination—rather than relying on a stack (C).
39. Has three operands
    Explanation: A three-address instruction format specifies three operands—two source operands and one destination register—making (A) correct.
40. (C) Program counter
    Explanation: The program counter is not part of the instruction format. The opcode (A) and operands (B) are essential fields. Hence, (C) is correct.