Coursework Assignment: Full Custom Design of a Digital to Analogue Converter (DAC) in 0.18μm CMOS

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***Abstract*—In this paper, a split capacitor based digital to analogue converter (DAC) in 0.18µm CMOS technology is introduced with its design principle and functionality of main components. Since it targets to satisfy the specific requirements, the technical specifications including output clock frequency, output voltage range, related error, power dissipation and silicon area in layout are used to analyse the performance and design of DAC system. And the performance of this DAC system is assessed according to the results from both test bench and script.**

***Index Terms*—DAC, split capacitor based, 0.18µm CMOS.**

I. Introduction

DIGITAL to analogue converter acts an important role with the development of digital world. The split capacitor based DAC is one of the most popular DAC architectures. It has the various advantages such as the simplicity of design, relatively good accuracy for step size and saving the silicon area compared with the fundamental capacitive DAC [1].

II. System Overview

A. Top Level Description

The top level of DAC is designed with seven pins including two power input/output pins (*vdd!* and *gnd!*), three input pins (*SI*, *VREF* and *EN*) and two output pins (*CLK* and *VOUT*). The functionality of each pin is described in TABLE I.

TABLE I
PIN DESCRIPTION FOR DAC SYSTEM [2]

Symbol	Type	Direction	Description
vdd!	Power	I/O	Global positive voltage supply 1.8V
gnd!	Power	I/O	Global negative voltage supply 0V
SI	Digital	In	Digital input from D0 to D7
VREF	Analogue	In	Reference voltage 0.9V
EN	Digital	In	Enable
CLK	Digital	Out	Clock frequency 10MHz
VOUT	Analogue	Out	Voltage output of DAC system

B. System Design Description

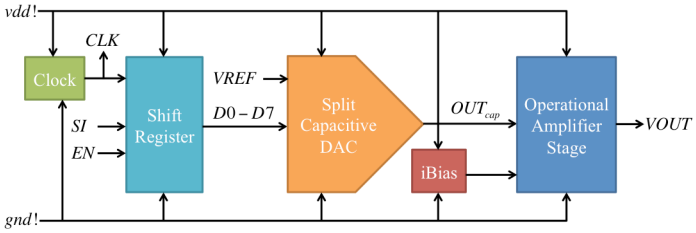

Fig. 1. Block diagram of DAC system

The block diagram of DAC in Fig. 1 mainly contains five components including clock, shift register, split capacitive DAC, operational amplifier stage and power supply. In detail, the clock generates the output clock frequency approximately 10MHz firstly. Then, it enters the shift register with the digital input signals *SI* and *EN*. Shift register is the block to generate the specific bit signals D0-D7 from *SI* and then transfer them into the split capacitive DAC when *EN*=0. Next, the split capacitive DAC converts the digital signal to the related analogue signal in certain voltage range. Lastly, this analogue signal followed by a buffer amplifier enters the non-inverting feedback amplifier stage, which scales the signal with specific voltage range 0.4-1.4V as the voltage output of DAC system. Since it is an 8-bit DAC design with the resolution as 255, the value of *VOUT* theoretically is [3]

$$VOUT = BitSignal/255 + 0.4 \quad (V) \tag{1}$$

In terms of the power supply, the global voltage supply is used as power supply for each block. In addition, the reference voltage *VREF* is used as voltage reference and also generates the substrate voltage *VSS* for the split capacitive DAC. Then, the biasing current for operational amplifier is generated from "iBias" block using Wilson current mirror with good stability.

C. Critical Technical Specifications

The target of this coursework is to design the DAC system which satisfies all the requirements as precisely as possible. There are two critical technical specifications used to assess the functional quality of the DAC system design. The relative error is one of the important parameters to estimate the system performance, which is calculated as [4]

$$ERR_{rel} = \left| Value_{ideal} - Value_{out} \right| / Value_{ideal} \tag{2}$$

Another critical technical parameter for design assessment is the power dissipation, which is generally calculated as [5]

$$P_{diss} = VDD \times I_{avg} \tag{3}$$

III. Circuit Implementation

This part is to introduce the circuit implementations of mainly components including clock, shift register, split capacitive DAC and operational amplifier stage in detail.

Generally, the top level system design shown in Fig. 2 is the practical schematic design in Cadence. It is believed that the range of output voltage is an important parameter for the DAC system. TABLE II shows the designed range for output voltage from split capacitive DAC to the operation amplifier (op-amp) stage. Since the op-amp does not work well when voltage is close to zero, the voltage offset in split capacitive DAC is implemented to solve this problem. Therefore, it is important to offset and scale the voltage range properly.

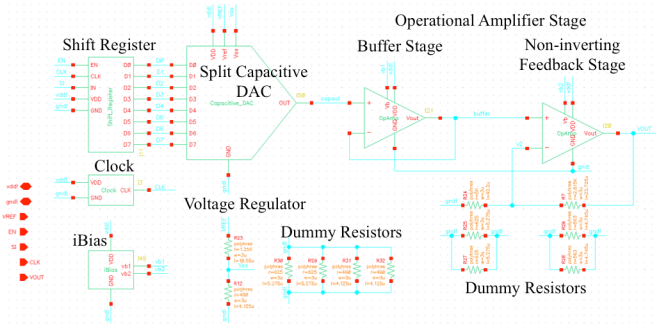

Fig. 2. Schematic of top level DAC system

TABLE II
RANGE FOR OUTPUT VOLTAGE

Symbol	Stage	Output Voltage Range (approx.)
OUT_{cap}	Split capacitive DAC	255-896mV
OUT_{buffer}	Buffer stage	255-896mV
$VOUT$	Non-inverting feedback	400-1400mV

A. Unit Capacitor

Since it is a capacitor based DAC design, it is strongly important to define the unit capacitor for both design and layout purpose. The unit capacitor used in this design is exactly five times of the minimum size capacitor in 0.18μm technology shown in TABLE III.

TABLE III
PARAMETER FOR CAPACITOR

Capacitor Size	W (μm)	L (μm)	C (fF)
Minimum size	4	4	17.6
Unit size	20	20	408

There are couple of reasons for this size. To begin with, it takes relatively short time to charge or discharge for the capacitor, which ensures the speed of digital to analogue conversion. With this size, it consums relatively small power with good performance, which satisfies the requirement of low power design. And it is obvious that the small size of capacitor saves the silicon area in layout. Lastly, it is convenient to built any capacitor in the whole design with the combination of couple of unit capacitors.

B. Clock

Clock using five-stage ring oscillator followed by a buffer is used to generate the output clock frequency approximately 10MHz. In this ring osciilator, five inverters "Inverter_B" in series generates a closed loop feedback with self start-up circuit [6]. The unit capacitor in each stage is to increase the slew rate in certain level. And two inverters "Inverter_C" in series creates the buffer as load.

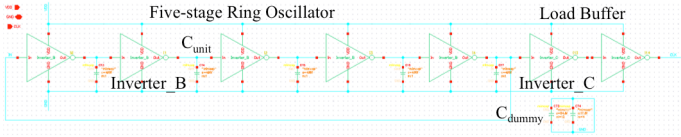

Fig. 3. Schematic of clock using ring oscillator

Technically, the geometry parameters including width and length of CMOS in TABLE IV decide the clock frequency. Specifically, the length of CMOS significantly affects the time period and width only slightly adjusts the pulse width. In detail, the fixed length for CMOS in each component makes a tidy design. And the width of PMOS is set as about twice or three times of NMOS accroding to the difference between the carrier mobility.

TABLE IV
GEOMETRY PARAMETERS FOR INVERTER

Component	W_P (μm)	W_N (μm)	$L_{P,N}$ (μm)
Inverter_B	14	4	4
Inverter_C	5	2	3.6

C. Shift Register

Shift register in Fig. 4 is to generate the 8-bit signals from input signal *SI* and transfers them to the split capacitive DAC once the digital signal is ready to convert when *EN*=0. Firstly, the fundamental D flip-flop (DFF) structure in series is used for bit signal generating. As the input signal *SI* contains data from D0 to D7, the output of DFF in order is from D7 to D0.

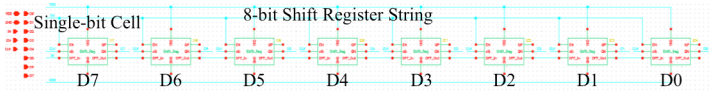

Fig. 4. Schematic of eight-cell shift register

After generating the bit signal using DFF, it holds the bit signals and transfers into the split capacitive DAC when *EN*=0 using NAND gate and SR NAND latch. The truth table for SR NAND latch displays in TABLE V.

TABLE V [7]
TRUTH TABLE FOR SR NAND LATCH

S	R	Q	$\overline{Q}$
0	0	Invalid	Invalid
0	1	1	0
1	0	0	1
1	1	No change	No change

According to the logic principles for NAND and latch, the design of "Shift_Reg" block (D0 for example) is described using the logic equation as

$$S = \overline{EN \times \overline{D0}},\quad R = \overline{EN \times D0},\quad \overline{Q} = D0 \tag{4}$$

D. Split Capacitive DAC

The split capacitive design in Fig. 5 provides relatively precise voltage level and further reduces the silicon area in the layout. Generally, it is seperated into LSB side (D0-D3) and MSB side (D4-D7). The extra capacitor with unit size on the LSB side is used to aviod floating in non input case.

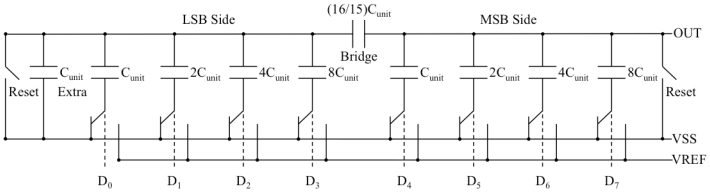

Fig. 5. Design of split capacitor based DAC

The bridge capacitor, which is used to separate the LSB and MSB side, is calculated as [8]

$$C_{bridge} = C_{unit}(C_{extra} + \sum_{i=0}^{3} C_i) / (\sum_{j=4}^{7} C_j) \tag{5}$$

In detail, the bridge capacitor in the practical design is generated by fifteen unit capacitors in series and one unit capacitor in parallel, which results as

$$C_{bridge} = (C_{1,2,...,15} inseries) \| C_0 = (\frac{1}{15} + 1) C_{unit} = \frac{16}{15} C_{unit} \quad (6)$$

Fig. 6 displays the schematic of split capacitor based DAC. Since LSB bits D0-D3 and MSB bits D4-D7 have the similar design according to Fig. 5, it is conveninent to implement "Cap_Block" for both in the practical design. Then, the simple NMOS is used as switch for the reset signal. Technically, the reset signal in this design is the inversion of global positive power supply *VDD*, which indicates that the system resets once it powers on. And the substrate power supply *VSS* for the split capacitive DAC block is generated using a resistor based voltage regulator as

$$VSS = \frac{R_2}{R_1 + R_2} VREF = \frac{490\Omega}{1.25k\Omega + 490\Omega} \times 900 = 253.4mV \quad (7)$$

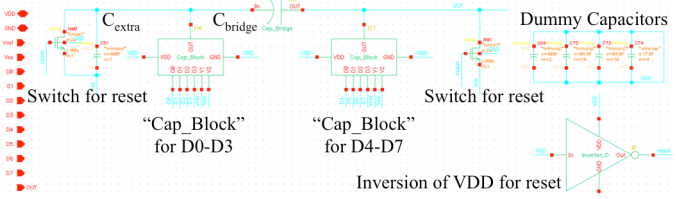

Fig. 6. Schematic of split capacitor based DAC

Considering the layout of the split capacitor based DAC, the common centroid configuration of capacitor in 7×7 matrix shown as Fig. 7 is implemented. Additional dummy capacitors are used for symmetry and guard ring.

C_{dummy}	D7	C_{15}	C_{14}	C_{13}	D7	C_{12}
D7	D6	D3	D2	D3	D6	D7
C_1	D3	D1	C_0	D5	D3	C_{11}
C_2	D2	D0	C_{extra}	D4	D2	C_{10}
C_3	D3	D5	C_{dummy}	D1	D3	C_9
D7	D6	D3	D2	D3	D6	D7
C_4	D7	C_5	C_6	C_7	D7	C_8

Fig. 7. Schematic of split capacitor based DAC

E. Operational Amplifier Stage

Operational amplifiers based on structure in Fig. 8 are used in buffer stage and non-inverting feedback amplifier. It is considered as a two-stage op-amp. On the first stage, it has a NMOS differential pair with current-mirror active load as biasing and no current mirror for stability. Then, the inverting stage using PMOS and NMOS pair on the second stage increases the gain significantly. Compensation capacitor is used to separate the two poles in the opposite direction in frequency domain, which improves the phase margin for unity frequency gain. The value of compensation capacitor is

$$C_C = C_{unit} = 2.448pF \quad (8)$$

It is proved that this operational amplifier has considerably large loop gain and proper phase margin for unity gain frequency as shown in Fig. 9. It can be implemented on the operational amplifier stage with good performance as

$$A_{OL} = 42.2dB, f_{cutoff} = 25.4kHz, PM = 68.5^\circ \quad (9)$$

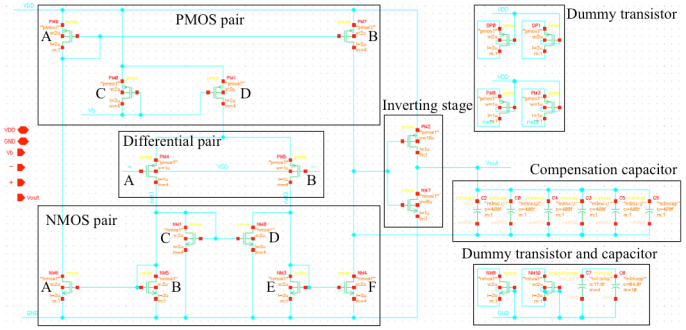

Fig. 8. Schematic of operational amplifier

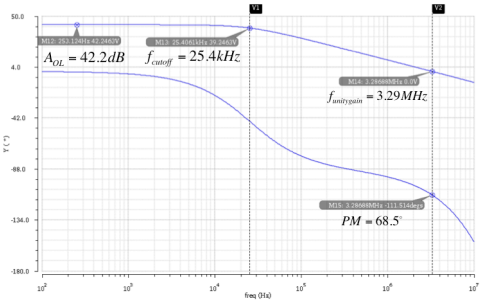

Fig. 9. AC result for operational amplifier

In terms of the layout of operation amplifier, it is important to implement the common centroid configuration for CMOS especially NMOS differential pair since it significantly affects the performance of operational amplifier. Also, it is used for the current mirror pair to make the layout more clear and tidy.

TABLE VI
COMMON CENTROID CONFIGURATION FOR CMOS

CMOS Pair	Common Centroid Configuration
Differential pair	BAABABBA
PMOS pair	DCCDBBABBCDDC
NMOS pair	DCCDAFFEFFBCDDC

Operational amplifier stage combines two stages including buffer and non-inverting feedback stage shown in Fig. 10. The output signal of split capacitive DAC circuit enters the buffer stage firstly, which is used to isolate the capacitors from the resistors on next stage. Then, the non-inverting feedback circuit scales the output voltage in proper range.

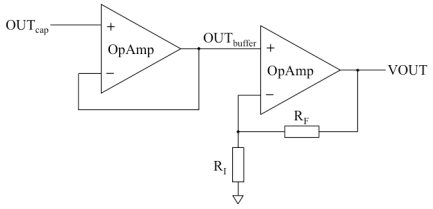

Fig. 10. Circuit of operational amplifier stage

Since the open loop gain of designed operational amplifier is significantly large, the non-inverting feedback stage scales the buffered signal with the closed loop gain approximately as

$$A_{CL} \approx 1 + \frac{R_F}{R_I} = 1 + \frac{2.815k\Omega}{5k\Omega} = 1.563 \quad (10)$$

Since the output voltage range of split capacitive DAC is about 255 to 896mV as designed, the op-amp stage scales it with the proper closed loop gain which can be describes as

$$OUT_{cap} = 255 - 896mV \xrightarrow{\times 1} OUT_{buffer} = 255 - 896mV \xrightarrow{\times 1.563} VOUT = 400 - 1400mV \quad (11)$$

IV. Simulated Results

A. Test Strategy and Test Bench Design

The test strategy of DAC system is to compare the output clock frequency and output voltage with the referenced results generated by the given verilloga symbol "TB_DAC". The test bench shown in Fig. 11 contains the power supply, block "TB_DAC", designed DAC block and load impedance.

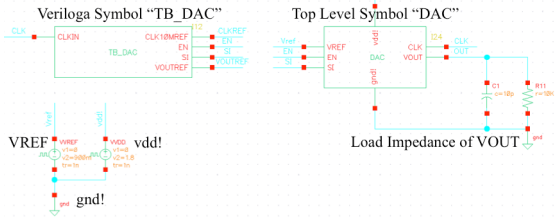

Fig. 11. Schematic of test bench

B. Test Bench and Script Results

It is said that the waveform of output voltage from test bench provides visual result and the data generated from the script provides the mathematical result of the DAC system. In terms of the test bench result, the waveform for output voltage in Fig. 12 shows its correct voltage range about 0.4 to 1.4V and step size 3.93mV. It is said that the oscillation when *EN*=1 is considerably large, while it does not affect the correction of output voltage. That is, it satisfies the requirement of signal conversion within 50μs. TABLE VII displays the output voltage for some key points with relative error less than 0.2%.

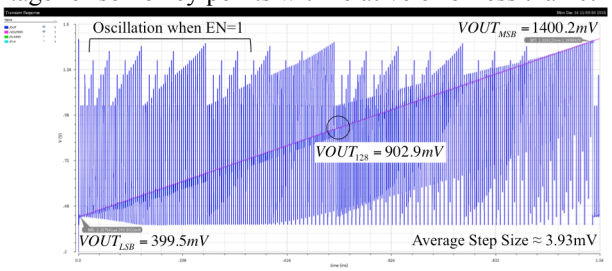

Fig. 12. Waveform of *VOUT* (ratio_fs=40)

TABLE VII
RESULT OF VOUT FOR KEY POINTS

Bit Signal	$VOUT_{desired}$ (mV)	$VOUT_{practical}$ (mV)	ERR_{rel}
00000000	400.0	399.5	0.13%
10000000	902.0	902.9	0.10%
11111111	1400.0	1400.2	0.01%

Then, the script result in Fig. 13 shows that the output clock frequency, which satisfies the technical specification as

$$f_{clk} = \frac{1}{T_{clk}} = \frac{1}{100.6164ns} \approx 9.94MHz \quad (12)$$

$$ERR_{rel} = |10MHz - 9.94MHz| / 10MHz = 0.6\%$$

```
CLK period is   100.6146 nS, relative error is     0.6146 %
Static power consumption is     1.5687 mW , dynamic power consumption is     1.5415 mW
Index    Reference       Vout    error
0           0.4000       0.3995       0.0013
1           0.4039       0.4034       0.0014
2           0.4078       0.4072       0.0015
3           0.4118       0.4111       0.0016
4           0.4157       0.4150       0.0017
```

Fig. 13. Script result for DAC system

C. Layout Results

Layout in Fig. 14 passes the DRC and LVS and it is well designed with the relatively small size as

$$Area = W \times H = 431.49\mu m \times 253.85\mu m \approx 0.1mm^2 \quad (13)$$

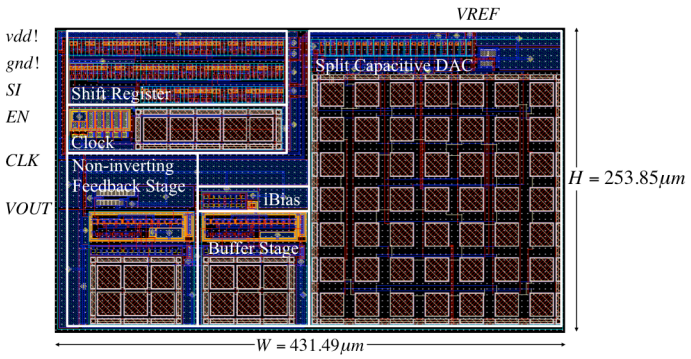

Fig. 14. Layout of DAC system

D. Possible Improvement

It is mentioned that there are some aspects that can be improved in advance. Firstly, the using of substrate power *VSS* in split capacitive DAC can be replaced by the ground if it is possible to design an ideal operational amplifier with good performance around 0V. Then, the obvious oscillation when *EN=1* in the output voltage can be stabilised using certain technology although it does not affect the output voltage result with given conversion rate. Lastly, the distance among capacitors in the common centroid configuration is suggested to reduce from 10 to 5μm to further save silicon area in layout.

V. Conclusion

The summary of the technical specifications of DAC design is shown in TABLE VIII, which indicates that the DAC design in this coursework satisfies all the technical requirements with good conversion performance. It is a low power design with power consumption approximately 1.6mW, which provides desired output voltage *VOUT* with proper range and precise step size. And the relatively small total silicon area about $0.1mm^2$ indicates the good layout design of DAC system.

TABLE VIII
TECHNICAL SPECIFICATIONS FOR DAC SYSTEM

Symbol	Specification	Desired Value	Practical Value
Area	Total silicon area	$\leq 1mm^2$	$0.1mm^2$
VDD	Power supply	$1.8V$	$1.8V$
P_{diss}	Power dissipation	$\leq 10mW$	$1.5687mW$
f_{clk}	Clock frequency	$10MHz$	$9.94MHz$
f_s	Conversion rate	$10kHz$	$10kHz$
R	Output voltage range	$0.4-1.4V$	$399.5-1400.2mV$
Z_L	Load impedance	$10k\Omega//10pF$	$10k\Omega//10pF$
ERR_{rel}	Relative error	$\leq 1.5\%$	$\leq 0.2\%$
T	Temperature	$27°C$	$27°C$

References

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