Xiwei Wang

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Educational Background

University of Waterloo **09/2025-12/2026**

- Major: Electrical and Computer Engineering
- Degree: Master (Anticipated graduate in December of 2026)

Yanshan University **09/2021-06/2025**

- Major: Electronic Science and Technology (Bachelor)
- GPA: 86/100
- Honor: Won Scholarship twice

Internship

Harbin Institute of Technology Wuhu Robot Technology Research Institute **China**

Industrial Vision Platform Development Intern **06/2025-08/2025**

- Built a C++ industrial inspection platform for real-time teacup defect detection using live camera feeds from scratch.
- Designed modular architecture with separate layers for video capture (Media Foundation), AI algorithm interface, and UI rendering.
- Collaborated with the algorithm team to connect trained models and expose standardized detection APIs per ROI.
- Deployed a local server for detection result logging, model parameter syncing, and offline frame analysis.

Sinopec Group **China**

Application Intern at the Information Center **07/2024-08/2024**

- Responsible for the successful completion of unmanned warehouse digital storage system project and Robot Control System (RCS) project
- Used **Python**'s Scikit-learn to predict inventory demand and Pyzbar to realize two-dimensional code recognition function; Utilized AI and Reinforcement Learning from Stable-Baseline3 to optimize Automated Guided Vehicle (AGV) scheduling; Used Proximal Policy Optimization algorithm to train a robot path planning model and applied it to warehouse system to realize real-time robot scheduling and path optimization

Technical Projects

High-Performance Java Server for Networked Applications **04/2025-06/2025**

- Developed a multithreaded **Java** TCP server for client–server workloads on **Linux (Ubuntu)** using ServerSocket and socket-level tuning.
- Benchmarked performance across Ubuntu servers, achieving latency reductions from 120 ms to ~40 ms, with further optimization toward <30 ms.

CUDA Convolution Acceleration **04/2024-06/2024**

- Implemented 2D convolution GPU kernels in CUDA 12.4 on RTX 3070 with **PyTorch**.
- Using **Python** to design benchmarking scripts for kernel size (K=3–11) and image sizes (1024–6144) with GFLOPs/GBps reporting.
- Explored optimization strategies such as block configuration tuning and planned integration of Winograd/Cook-Toom transforms for performance gains.

Additional Information

Languages: English (fluent), Chinese (native), French (sufficient)