Segmentation Extension Proposal

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Outline

- Why segmentation
- Segmentation hardware
- New instructions
- Benefits of segmentation
- Misc



Why Segmentation

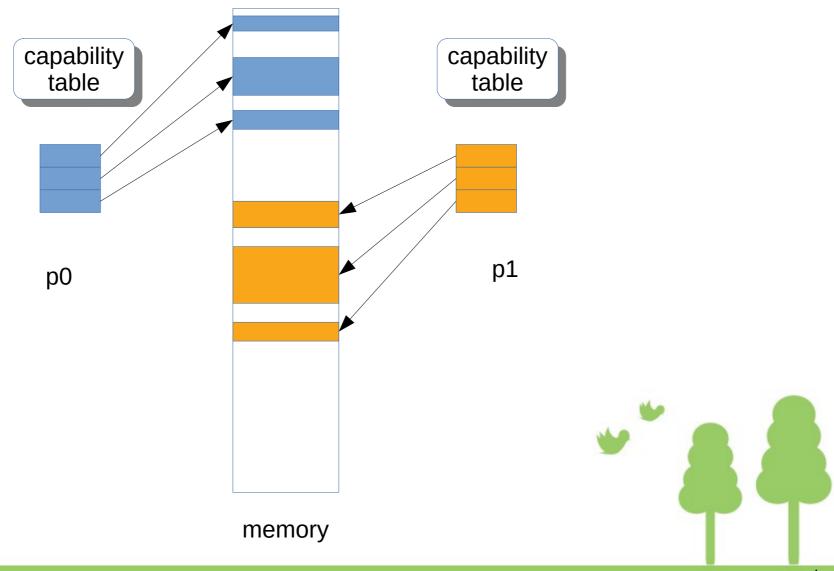
- Segmentation can be used to create multiple protection domains on a single address space
 - SASOS: Single Address Space Operating System
 - Reduce context switch overhead
 - Data sharing is easy among processes

- ...

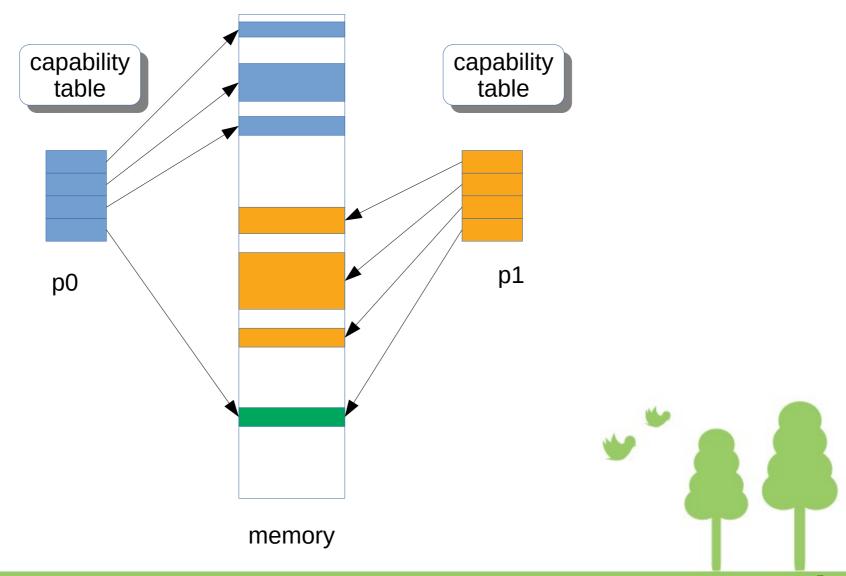
- Other benefits
 - I/O segment
 - Physical memory segment
 - Software-managed TLB
 - No PIC (Position Independent Code) is needed

- ...

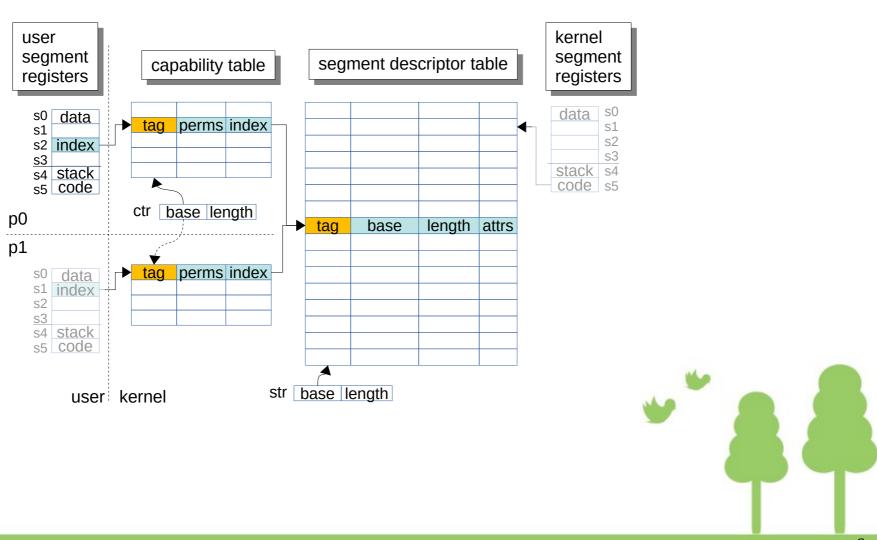
Segmentation Hardware



Segmentation Hardware (2)



Segmentation Hardware (3)



Segmentation Hardware (4)

- Segment TLB
 - Cache segment descriptors
- Segment shadow register
 - Cache capability

shadow registers

s0	data
s1	
s2	
s3	
s4	stack
s5	code

perms	token	index
perms	token	index



New Instructions

- Load/Store with segment override
 - LW x1, s1:imm[x2]
- Load/Store segment registers, ctr register and str register
 - LSR s0, imm[x1], SSR s0, imm[x1]
 - LCTR imm[x1], LSTR imm[x1]
- Far function call and return
 - For shared library
 - Far call
 - SJAL link_addr, callee_seg, imm
 - Far return
 - SJALR caller_seg, imm[x1]



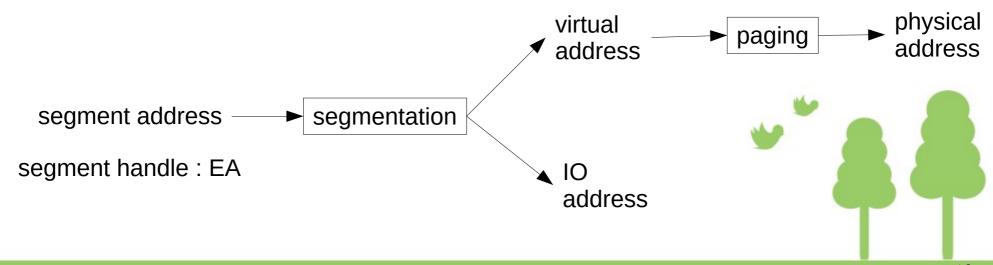
Benefits of Segmentation

- On systems without paging
 - Segmentation can be used instead of PMP (Physical Memory Protection).
 - It's more easy to implement shared library with segmentation.



Benefits of Segmentation (2)

- On systems with paging
 - I/O segment
 - No page TLB entry is needed for device driver to access its hardware device.
 - One set of load/store instructions can be used to load/store from/to either memory or I/O.



Benefits of Segmentation (3)

- On systems with paging
 - Physical memory segment
 - Improve the performance of big-memory workloads
 - Arkaprava Basu, Jayneel Gandhi, Jichuan Chang, Mark D. Hill, Michael M. Swift.
 Efficient virtual memory for big memory servers. In Proc. ISCA, 2013.

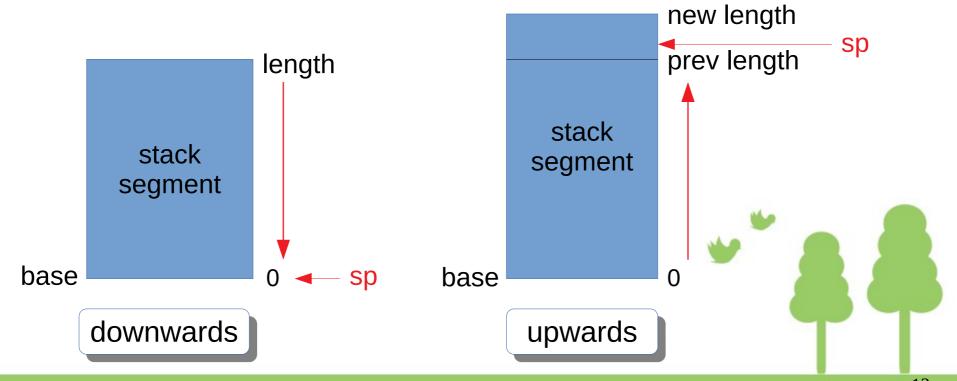


Benefits of Segmentation (4)

- Software-managed TLB
 - Prerequisite
 - Segment/page TLB miss can not happen during TLB miss handling.
 - How
 - Make kernel's code, data and stack segment as physical memory segment.
 - Make kernel's code, data and stack segment descriptors always resident in segment TLB.

Misc.

- Stack growth direction
 - Stack should grow upwards.



Misc. (2)

- Compiler support is needed.
 - Far pointer
 - Shared library
- OS change is needed.
 - MASOS → SASOS



Thanks.



Misc.

 Segment offset space sharing for data and stack segment

