CPE 333 Lab 4: Direct Map Cache

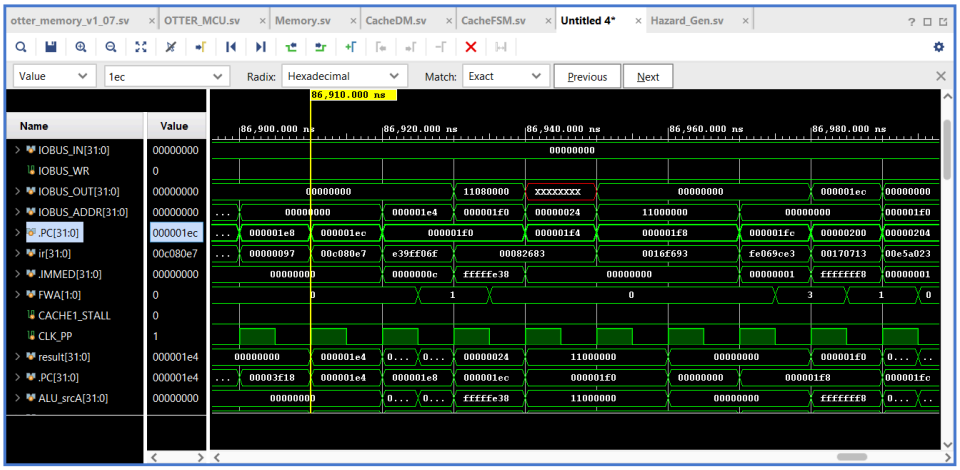
Contributions:

- Wyatt Tack: Wrote new verilog code
- Justin Rosu: Helped debug Cache
- Brayden Daly: Helped debug Cache
- Tyler Hamilton: Helped design portions of Cache

Design:

As per lab instructions, the Direct Map cache was only implemented on the instruction memory set. This Cache was implemented as a 16x32 byte cache (16x8 words). Upon a miss, a stall condition was generated, to stop the clock for the entire CPU except resource recovery tools.

Vivado Simulation:



Above is shown the TEST_ALL simulation, with a clock count of 8,691 cycles, a few more than the non-cached pipelined CPU. However, if all instructions took 2 clock cycles to fetch from memory (as would be expected in the presence of larger memory architectures), this would be a mere half of the time that the non-cached CPU would take.