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EE 431-01 F'24
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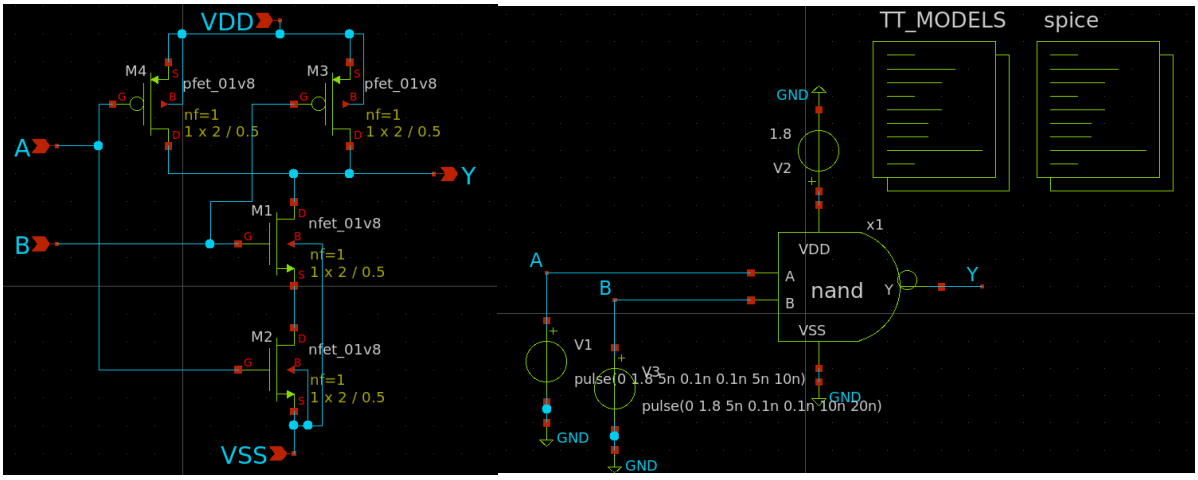
EE 431 Lab 3

Introduction:

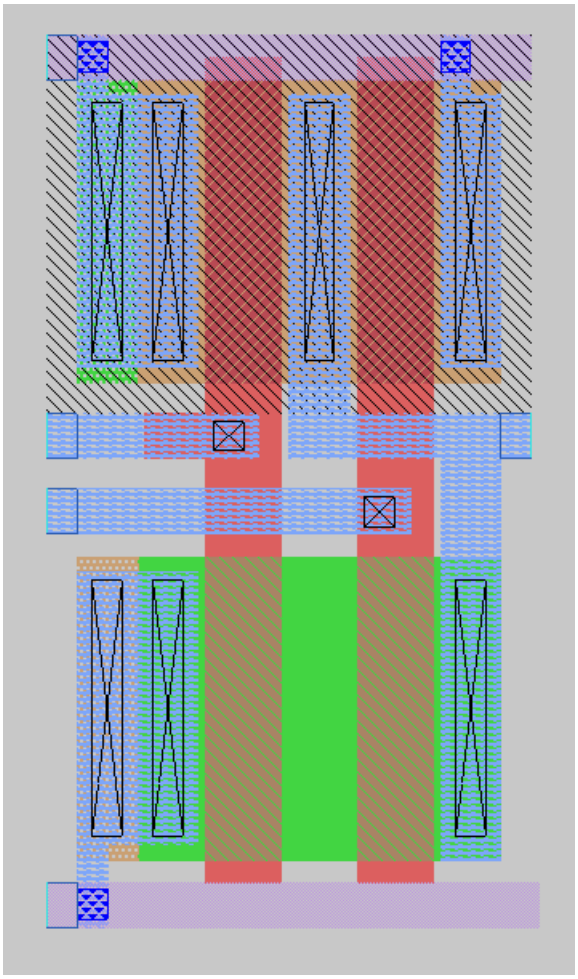
This lab was used to build off of the inverter we had created with the Magic VLSI tools, to create a new gate, being the NAND gate. All digital logic can be comprised of NAND gates, and as a NOT gate (inverter) is only single input, a dual input is necessary to compare/contrast inputs for logical actions. This lab followed the same process as Lab 2, creating a schematic, simulating the schematic, to layout and simulation, to LVS, to parasitic extraction. The NAND gate currently works as intended, with the open source PDK Skywater 130A used on Magic.

Methodology:

The first inverter was built as a simple CMOS NAND gate with two inputs, shown below. A parallel dual PMOS was used for the pull up network, while a series dual NMOS was used for the pull-down network. The size for each MOSFET and the spice model were obtained through the same Skywater PDK as was used for the layout.

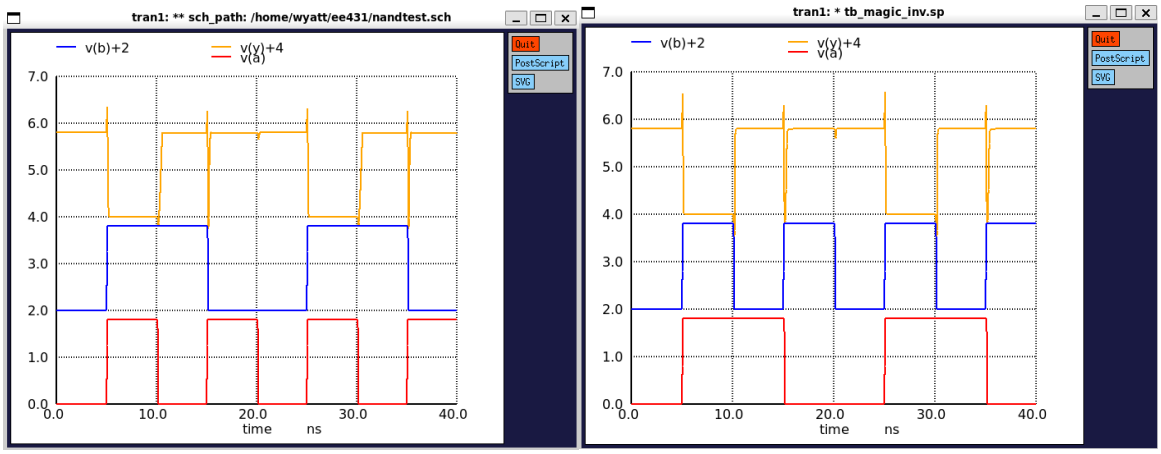


Now that our schematic does exactly what we wanted from it, we are now ready to start the layout process. Magic was opened and through using the Skywater PDK we created the logic gate. We used the same MOSFET sizes as were simulated for consistency and comparison. The PMOS were each sized to 2um/0.5um while the NMOS were each sized to 2um/0.5um. The layout created is shown below. The Layout followed closely to our inverter layout with an included channel:

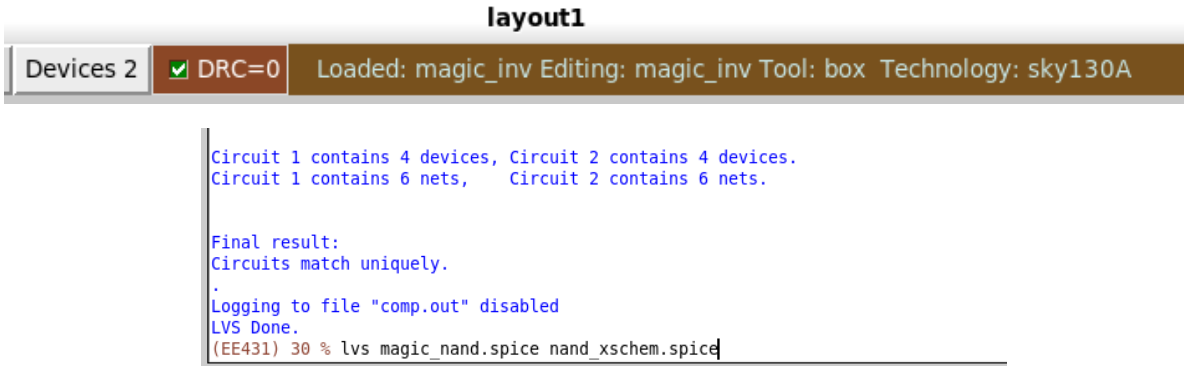


Results:

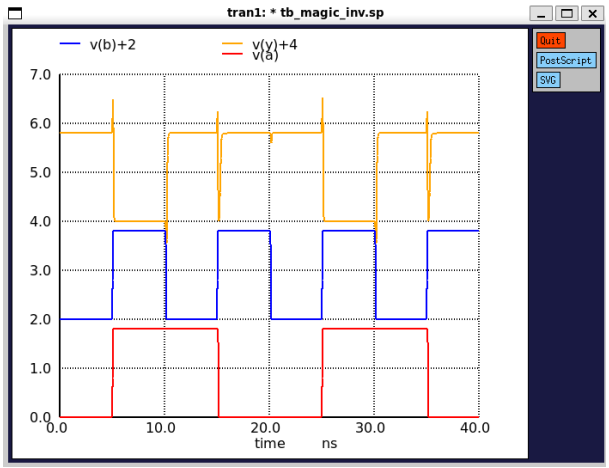
The NAND gate was given nets to connect to in NGSpice, and thus simulated to recover a time domain solution. This graph is shown below. Additionally, the schematic gate was used with NGSpice to simulate according to the test bench set up above, and time domain solution graph was obtained. These graphs are presented below, schematic on the left and layout on the right.



Furthermore, LVS (layout versus schematic) was used through Netgen to compare both the exported netlist through magic of our layout, versus the exported netlist of our schematic from Xschem which we started with. Running LVS on out two netlists produced the following, along with the DRC no errors verification from Magic:



Which shows us that our layout is consistent with what we designed. Beyond this we exported the parasitic capacitances of our layout to a spice file, in which we were able to simulate this with our final inverter design to get a more accurate plot of our transfer characteristics, with mild increase in transients during switching:



Discussion:

Both the schematic and the layout were simulated at the same voltage pulses, and when upon inspection of the time domain plots, the simulation between the schematic and the layout are indistinguishable. This lab is truly the start to more complex logic designs, as a 2-input gate is necessary to create complex logic circuits with different inputs, which we are capable of now that we have a working and tested NAND gate.

Appendix:

Spice Files for Magic Layout:

```
* NGSPICE file created from magic_nand.ext - technology: sky130A

.subckt magic_nand A B Y VDD VSS
X0 Y A VDD VDD sky130_fd_pr__pfet_01v8 ad=0.5 pd=2.5 as=0.9 ps=4.9 w=2 l=0.5
X1 Y B a_100_n230# VSS sky130_fd_pr__nfet_01v8 ad=0.9 pd=4.9 as=0.5 ps=2.5 w=2 l=0.5
X2 a_100_n230# A VSS VSS sky130_fd_pr__nfet_01v8 ad=0.5 pd=2.5 as=0.9 ps=4.9 w=2 l=0.5
X3 VDD B Y VDD sky130_fd_pr__pfet_01v8 ad=0.9 pd=4.9 as=0.5 ps=2.5 w=2 l=0.5
.ends
```

Spice Files for Xschem Schematic:

```
** sch_path: /home/wyatt/EE431/nand.sch
**.subckt nand VDD A Y B VSS
*.ipin A
*.ipin B
*.ipin VSS
*.opin Y
*.ipin VDD
XM1 Y B net1 VSS sky130_fd_pr__nfet_01v8 L=0.5 W=2 nf=1 ad='int((nf+1)/2) * W/nf * 0.29'
as='int((nf+2)/2) * W/nf * 0.29' pd='2*int((nf+1)/2) * (W/nf + 0.29)'
+ ps='2*int((nf+2)/2) * (W/nf + 0.29)' nrd='0.29 / W' nrs='0.29 / W' sa=0 sb=0 sd=0
mult=1 m=1
XM3 Y B VDD VDD sky130_fd_pr__pfet_01v8 L=0.5 W=2 nf=1 ad='int((nf+1)/2) * W/nf * 0.29'
as='int((nf+2)/2) * W/nf * 0.29' pd='2*int((nf+1)/2) * (W/nf + 0.29)'
+ ps='2*int((nf+2)/2) * (W/nf + 0.29)' nrd='0.29 / W' nrs='0.29 / W' sa=0 sb=0 sd=0
mult=1 m=1
XM4 Y A VDD VDD sky130_fd_pr__pfet_01v8 L=0.5 W=2 nf=1 ad='int((nf+1)/2) * W/nf * 0.29'
as='int((nf+2)/2) * W/nf * 0.29' pd='2*int((nf+1)/2) * (W/nf + 0.29)'
+ ps='2*int((nf+2)/2) * (W/nf + 0.29)' nrd='0.29 / W' nrs='0.29 / W' sa=0 sb=0 sd=0
mult=1 m=1
XM2 net1 A VSS VSS sky130_fd_pr__nfet_01v8 L=0.5 W=2 nf=1 ad='int((nf+1)/2) * W/nf *
0.29' as='int((nf+2)/2) * W/nf * 0.29' pd='2*int((nf+1)/2) * (W/nf + 0.29)'
+ ps='2*int((nf+2)/2) * (W/nf + 0.29)' nrd='0.29 / W' nrs='0.29 / W' sa=0 sb=0 sd=0
mult=1 m=1
**.ends
.end
```