Wyatt Tack
EE 431-01 F'24
2024-Oct-25

EE 431 Lab 2

Introduction:

This lab was used to create a first layout of an inverter, using Magic VLSI tools. The inverter is the basis of every logic circuit or device, so any time a new design is started the inverter must be present or made to be the basis of every design. This lab used xschem to create an initial simulation through NGSpice with the same transistor width and length, then used magic to lay out an inverter that was simulated with NGSpice as well, to confirm working status. Magic was used with the open source PDK Skywater 130A.

Methodology:

The first inverter was built as a simple CMOS inverter with two MOSFETs, shown below. The size for each MOSFET and the spice model were obtained through the same Skywater PDK as was used for the layout.
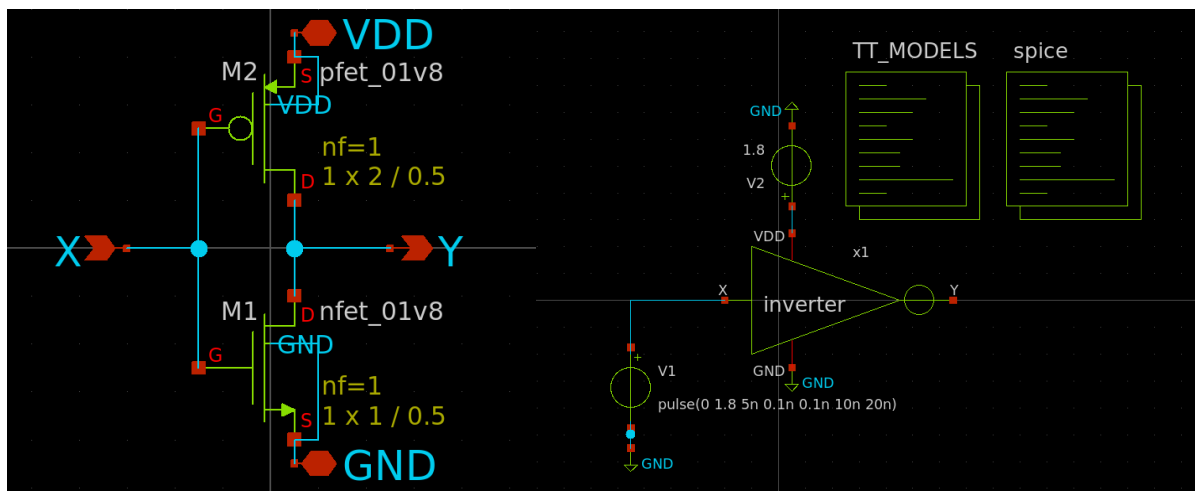
Now that our schematic does exactly what we wanted from it, we are now ready to start the layout process. Magic was opened and through using the Skywater PDK we created the inverter. We used the same MOSFET sizes as were simulated for consistency and comparison. The PMOS was sized to 2um/0.5um while the NMOS was sized to 1um/0.5um. The layout created is shown below:
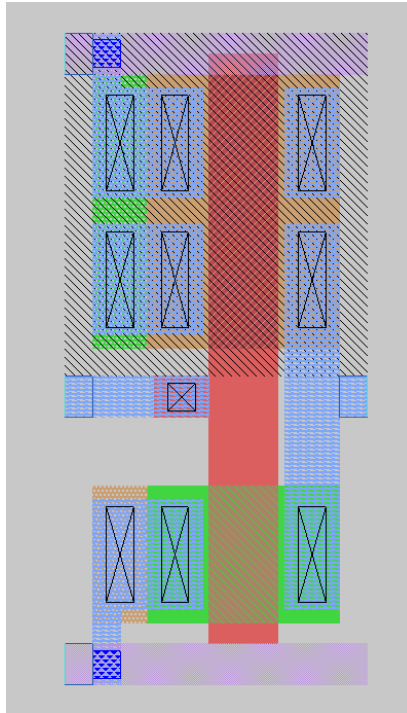
Results:

The inverter was given nets to connect to in NGSpice, and thus simulated to recover a time domain solution. This graph is shown below. Additionally, the schematic inverter was used with NGSpice to simulate according to the test bench set up above, and time domain solution graph was obtained. These graphs are presented below, schematic on the left and layout on the right.
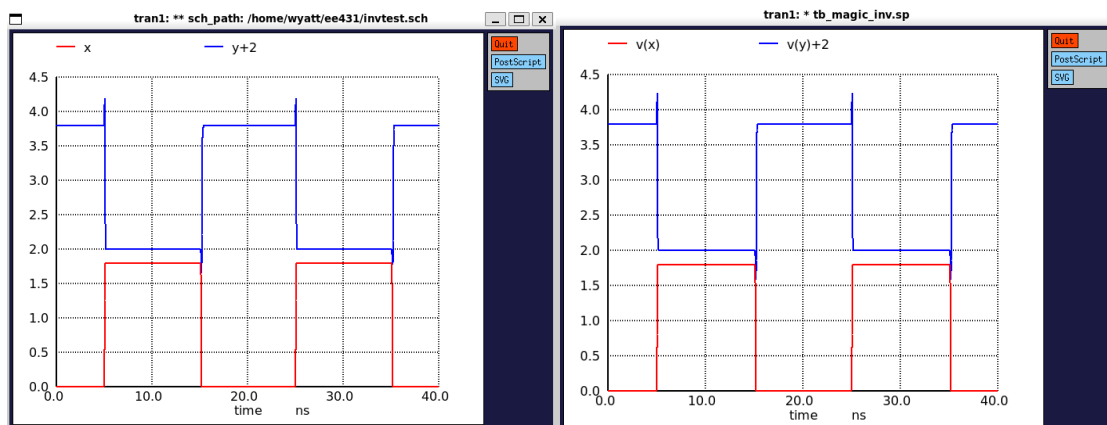
Furthermore, LVS (layout versus schematic) was used through Netgen to compare both the exported netlist through magic of our layout, versus the exported netlist of our schematic from xschem which we started with. Running LVS on out two netlists produced the following, along with the DRC no errors verification from Magic:

Which shows us that our layout is consistent with what we designed. Beyond this we exported the parasitic capacitances of our layout to a spice file, in which we were able to simulate this with out final inverter design to get a more accurate plot of our transfer characteristics, with mild increase in transients during switching:
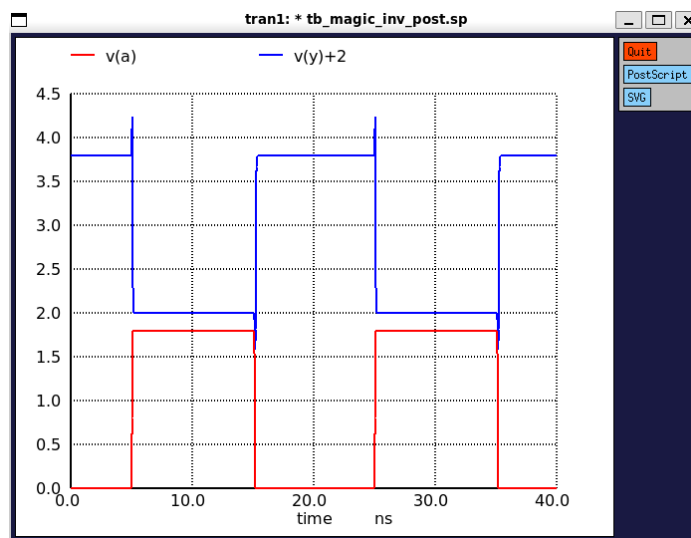
Discussion:

Both the schematic and the layout were simulated at the same voltage pulses, and when upon inspection of the time domain plots, the simulation between the schematic and the layout are indistinguishable. Although the inverter is the simplest of logic circuits, to see that the simulation is consistent to what we would expect and confirms functionality is a green light for implementation of larger circuitry.