Wyatt Tack
EE 431-01 F'24
2024-Oct-4

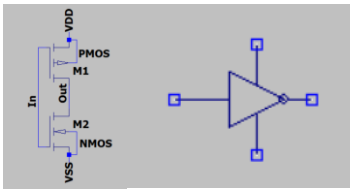
# EE 431 Lab 1

## Introduction:

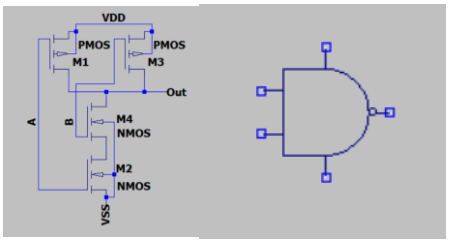
This lab was used to simulate a bottom-up process for building digital logic. Starting from a CMOS inverter, we were able to make the logic cell for an inverter, and follow suit for the NAND and NOR gates using other transistors. From these gates we were able to construct a larger, more complicated digital block, a multiplexor. Through using the few gates to make a 2-1 multiplexor, multiple of these were used to create a 4-1 multiplexor, without needing to copy each individual logic gate, and without needing to for each of those copy each transistor. This lab as well used capacitance to simulate rise and fall times changing with the variation of the capacitance, which models how logic gates act in series for fan out.

## Methodology:

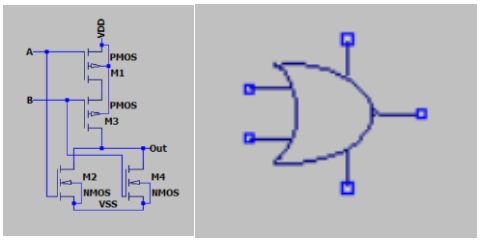
The first inverter was built as a simple CMOS inverter with two MOSFETs, shown below.



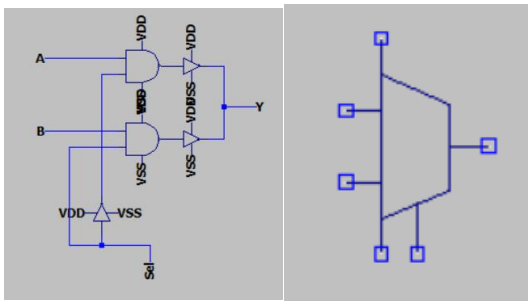

This CMOS topology was applied to create both a NAND and a NOR gate, with NAND having parallel pull up net works and series pull down networks:



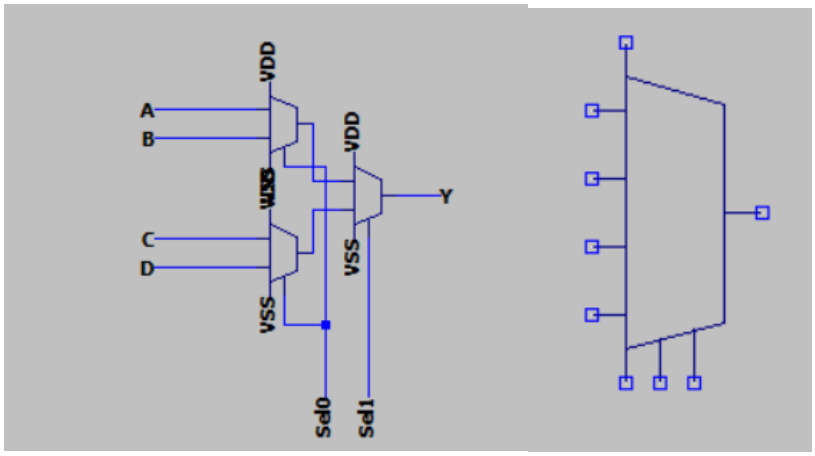

And NOR having series pull up net works and parallel pull down networks:




Using these blocks a 2 to 1 multiplexor was constructed, with 1 channel and 1 select bit:

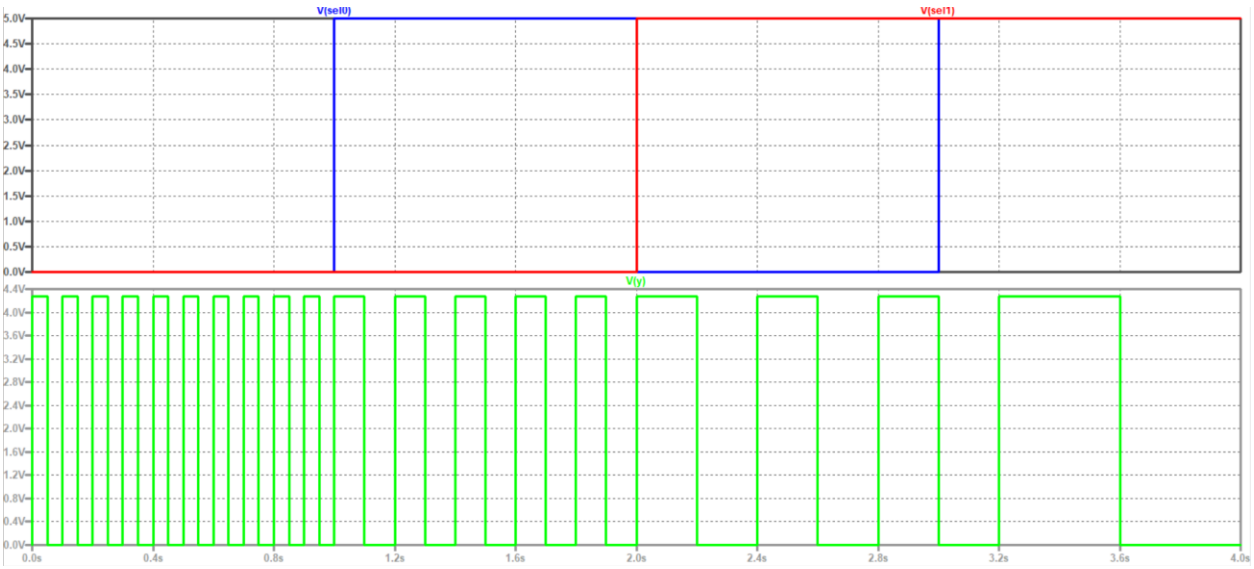



Which were then used to create a 4 to 1 multiplexor using 2 select bits for the channels:



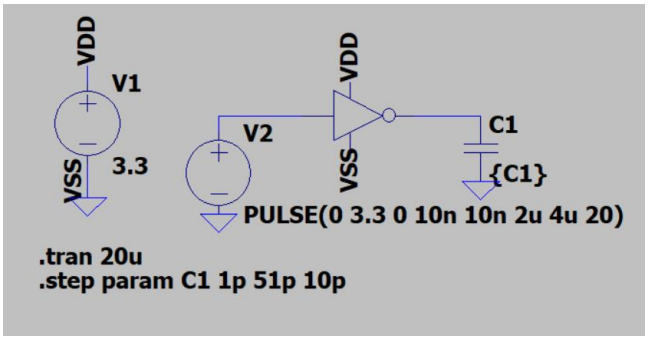
## Results:

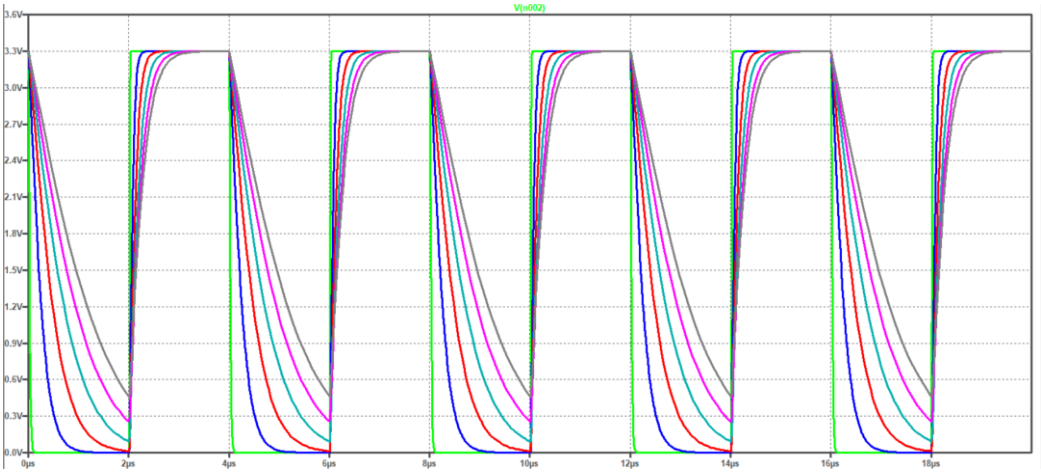
This multiplexor was then simulated as having a different pulse frequency at each input, with bits SEL0 and SEL1 being counted up in binary to select each waveform. Shown below is the simulation output, with the two select bits shown up top, and the output of the multiplexor shown below:




This simulation represents how bottom up design can save massive ammounts of time and simplify design greatly, as this same output could have been constructed on a single simulation page, with the dozens of transistors that each gate represent, represented by a single multiplexor. The bottom up desing method simplifies everything and makes design and analysis of other's designs more simple, as repeated components can be summed up by a symbol rather than needing to be repeated everywhere discretely.

Further, one individual CMOS inverter gate was tested with a steped parameter capacitance to visualize how rise time, and more evidently fall time, vary with ouptut capacitance of the gate, showing how increased fan out could lead to longer propogation delays as the parasitic and gate capacitances would need time to charge:






This second simulation however shows what we must be wary of when we incoroporate very large scale integration. Large fan out means large output capacitance, which will lead to slower propagation delays. This time needed to switch from low to high limits the bandwith of what we could communicate with, which is why design for mitigating parasitic capacitances is necessary.

## Discussion:

This lab helped put a foundation of VLSI into our minds without using the tools for layouts quite yet. Before the design we must understand the benificiality of bottom up design, as to simplify circuit and logic design, and make diagrams more understandable. When shown the block diagram for a microcontroller, not every transistor is shown packed together on a circuit diagram, but instead cells that represent a logical operation, to simplify understanding of the internals of a VLSI device. Challenges with this lab involve unformiliarities with software, as using tools like these take time to learn in and out, but with practice can be used efficiently.