

Product Specification

Product Name: VGM128036A5W02

Product Code: M01011

	Customer						
Approved by Customer							
Approved	Date:						

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Designed By	Checked By	R&D	QA			
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REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
Y01	Initial release.	2012-03-14	
A01	Update the Mechanical Data Update the Module Interface Update the Absolute Maximum Ratings Update the Electro-optical Characteristics Update the Recommended Software Initialization Update the Lifetime	2012-04-12	Page 4 Page 6 Page 8 Page 10 Page 24 Page 26
D01	Modify "Visionox Display Co.,Ltd" to "Visionox"	2014-02-19	Page 32



1 Overview

VGM128036A5W02 is a monochrome OLED display module with 128×36 dot matrix. The characteristics of this display module are high brightness, self-emission, high contrast ratio, slim/thin outline, wide viewing angle, wide temperature range, and low power consumption.

2 Features

Display Color: White
 Dot Matrix:128×36
 Driver IC: SH1106G

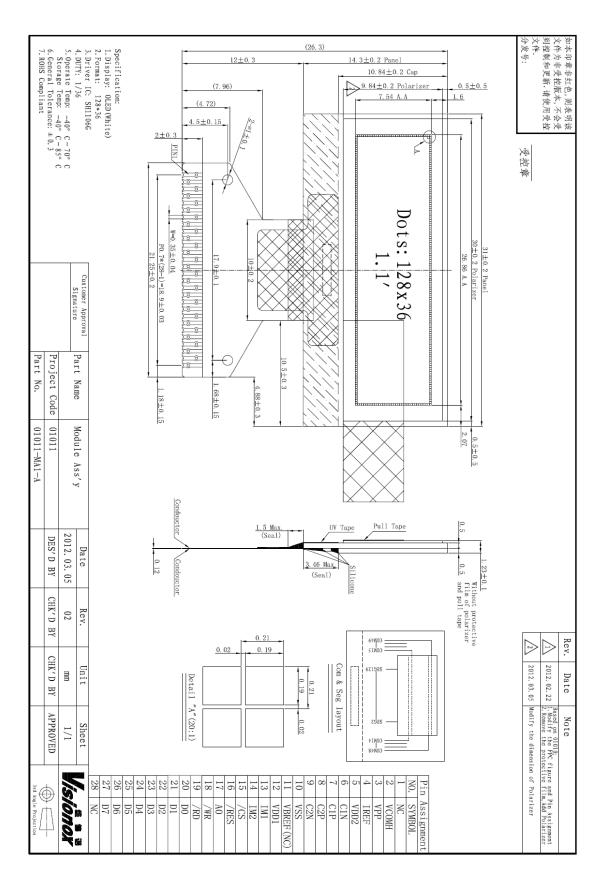
Interface: 8-bit 6800、8-bit 8080、I²C 、4-wire SPI
 Wide range of operating temperature: -40°C to 70°C

3 Mechanical Data

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128(W)×36(H)	-
2	Dot Size	0.19(W)×0.19 (H)	mm ²
3	Dot Pitch	0.21(W)×0. 21 (H)	mm ²
4	Aperture Rate	82	%
5	Active Area	26.86(W)×7.54 (H)	mm ²
6	Panel Size	31(W)×14.3(H)×1.0(T)	mm ³
7	Module Size	31(W)×26.3(H)×1.23 (T)	mm ³
8	Diagonal A/A Size	1.1	inch
9	Module Weight	$1.04 \pm 10\%$	gram



4 Mechanical Drawing





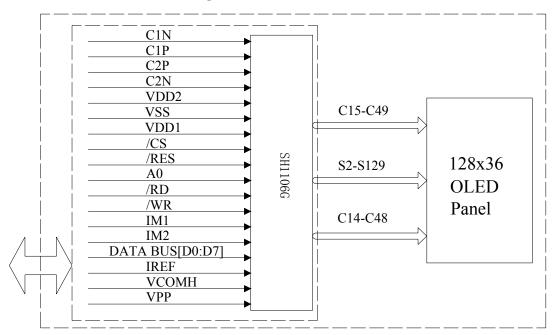
5 Module Interface

PIN NO.	PIN NAME	DESCRIPTION					
1	NC	No Connection.					
2	VCOMH	This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and VSS.					
3	VPP	OLED panel power supply. Generated by internal charge pump. Connect to capacitor. It could be supplied externally.					
4	IREF	This is a segment current reference pad. A resistor should be connected between this pad and VSS. Set the current at 10 μ A.					
5	VDD2	3.0 – 4.2V power supply pad for Power supply for charge pump circuit. This pin can be disconnedted or connect to VDD1 when VPP is supplied externally.					
6	C1N						
7	C1P	Connect to charge pump capacitor.					
8	C2P	Constitution in the second sec					
9	C2N	Connect to charge pump capacitor.					
10	VSS	Ground.					
11	VBREF(NC)	This is an internal voltage reference pad for booster circuit. Keep floating.					
12	VDD1	Power supply input: 1.65 - 3.5V					
13	IM1	Pin Name I ² C 6800 8080 4-SPI					
1.4	1) (2)	IM1 1 0 1 0					
14	IM2	IM2 0 1 1 0					
1.7	/00	This pad is the chip select input. When /CS = "L",					
15	/CS	then the chip select becomes active, and data/command I/O is enabled.					
16	/RES	This is a reset signal input pad. When /RES is set to "L", the settings are initialized. The reset operation is performed by the /RES signal level.					
17	A0	This is the Data/Command control pad that determines whether the data bits are data or a command. A0 = "H": the inputs at D0 to D7 are treated as display data. A0 = "L": the inputs at D0 to D7 are transferred to the command registers. In I ² C interface, this pad serves as SA0 to distinguish the different address of OLED driver.					
18	/WR	This is a MPU interface input pad. When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When /WR = "H": Read. When /WR = "L": Write.					
19	/RD	This is a MPU interface input pad. When connected to an 8080 series MPU, it is active LOW. This pad is connected to the /RD signal of the 8080 series MPU, and the data bus is in an output status when this signal is "L". When connected to a 6800 series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU. When /RD = "H": Enable. When /RD = "L": Disable.					
20~27	D0~D7	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance. When the I²C interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDAI). At this time, D2 to D7 are set to high impedance.					
28	NC	No Connection.					

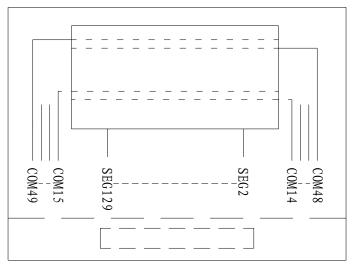


6 Function Block Diagram

6.1 Function Block Diagram



6.2 Panel Layout Diagram



Com & Seg layout



7 Absolute Maximum Ratings

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Logic supply voltage	VDD1	-0.3	3.6	V	IC maximum rating
Charge Pump Regulator Supply Voltage	VDD2	-0.3	4.3	V	IC maximum rating
OLED Operating voltage	VPP	-0.3	14.5	V	IC maximum rating
Operating Temp.	Тор	-40	70	$^{\circ}$	-
Storage Temp	Tstg	-40	85	$^{\circ}$ C	-

Note (1): All of the voltages are on the basis of "VSS = 0V".

Note (2): Permanent breakage of module may occur if the module is used beyond the maximum rating. The module can be normal operated under the conditions according to Section 8 "Electrical Characteristics". Malfunctioning of the module may occur and the reliability of the module may deteriorate if the module is used beyond the conditions.



8 Electrical Characteristics

8.1 DC Electrical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Logic Supply Voltage	VDD1	22±3°C, 55±15%R.H	1.65	3.0	3.5	V
OLED Driver Supply Voltage (Supply Externally)	VPP	22±3°C, 55±15%R.H	11.5	12	12.5	V
OLED Driver Supply Voltage (Generated by Internal DC/DC)	VPP	22±3°C, 55±15%R.H	-	9.0	-	V
Charge Pump Regulator Supply Voltage	VDD2	22±3°C, 55±15%R.H	3.0	3.7	4.2	V
High-level Input Voltage	V_{IH}	-	$0.8 \times \text{VDD1}$	-	VDD1	V
Low-level Input Voltage	$V_{\rm IL}$	-	VSS	-	$0.2 \times \text{VDD1}$	V
High-level Output Voltage	V_{OH}	-	$0.8 \times VDD1$	-	VDD1	V
Low-level Output Voltage	V_{OL}	-	VSS	-	$0.2 \times VDD1$	V

Note: The VPP input must be kept in a stable value; ripple and noise are not allowed.





8.2 Electro-optical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Normal Mode	Ι.	All pixels ON(1) (VPP generated by internal DC/DC)	100	150	-	cd/m ²
Brightness	L_{br}	All pixels ON VPP = 12V (External)	200	240	-	Cu/III
Normal Mode Power	Pt	All pixels ON(1) (VPP generated by internal DC/DC)	-	138.75	166.5	mW
Consumption	1 (All pixels ON VPP = 12V (External)	All pixels ON VPP = 12V (External)	234	288	mW
Sleep mode current consumption in VDD1 & VDD2(2)	ISP	During sleep, $TA = +25^{\circ}C$, VDD1 = 3V, $VDD2 = 3V$. (2)	-	-	5	uA
Sleep mode current consumption in VPP		During sleep, $TA = +25^{\circ}C$, $VPP = 9V$ (External)	-	-	5	uA
C.I.E(White)	(x)	x,y(CIE1931)	0.26	0.30	0.34	-
C.I.E(WIIIe)	(y)		0.29	0.33	0.37	-
Dark Room Contrast	CR	-	≥2000:1	-	-	-
Response Time	-	-	-	10	-	μs
View Angle	-	-	≥160	-	-	Degree

Note(1): Normal Mode test conditions are as follows:

- Driving voltage: VDD2:3.7V(VPP Generated by Internal DC/DC).

Contrast setting: 0xa3Frame rate: 102HzDuty setting: 1/36

- Driving voltage: External VPP Mode(VPP=12V).

Contrast setting: 0xb0Frame rate: 102HzDuty setting: 1/36

Note(2): Sleep Mode test conditions are as follows:

Disable Charge Pump:0XAD,0X8A.

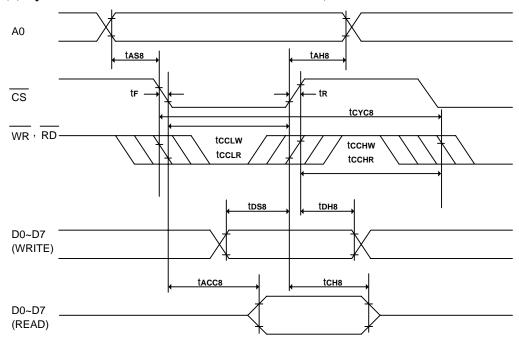
Set Display OFF:0XAE,

When the display OFF command is executed, power saver mode will be entered.



8.3 AC Electrical Characteristics

(1) System buses Read/Write characteristics 1 (For the 8080 Series Interface MPU)



$$(VDD1 = 1.65 - 3.5V, TA = +25^{\circ}C)$$

Symbol	Parameter	Min	Тур	Max	Unit	Condition
tcyc8	System cycle time	600	-	-	ns	
tass	Address setup time	0	-	-	ns	
tans	Address hold time	0	-	-	ns	
toss	Data setup time	80	-	-	ns	
t _{DH8}	Data hold time	30	-	-	ns	
tch8	Output disable time	20	-	140	ns	$C_L = 100 pF$
taccs	RD access time	-	-	280	ns	$C_L = 100 pF$
tcclw	Control L pulse width (WR)	200	-	-	ns	
tcclr	Control L pulse width (RD)	240	-	-	ns	
tcchw	Control H pulse width (WR)	200	-	-	ns	
tcchr	Control H pulse width (RD)	200	-	-	ns	
tr	Rise time	-	-	30	ns	_
tf	Fall time	_	-	30	ns	



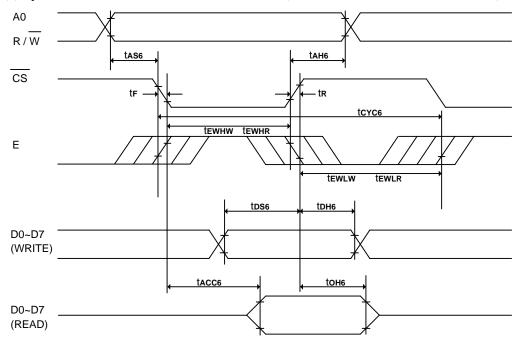


 $(VDD1 = 2.4 - 3.5V, T_A = +25^{\circ}C)$

Symbol	Parameter	Min	Тур	Max	Unit	Condition
tcyc8	System cycle time	300	-	-	ns	
tass	Address setup time	0	-	-	ns	
tan8	Address hold time	0	-	-	ns	
toss	Data setup time	40	-	-	ns	
t _{DH8}	Data hold time	15	-	-	ns	
tcH8	Output disable time	10	-	70	ns	$C_L = 100 pF$
taccs	RD access time	-	-	140	ns	$C_L = 100 pF$
tcclw	Control L pulse width (WR)	100	-	-	ns	
tcclr	Control L pulse width (RD)	120	-	-	ns	
tcchw	Control H pulse width (WR)	100	-	-	ns	
tcchr	Control H pulse width (RD)	100			ns	
tr	Rise time	-	-	15	ns	
tf	Fall time	-	-	15	ns	



(2) System buses Read/Write Characteristics 2 (For the 6800 Series Interface MPU)



$$(VDD1 = 1.65 - 3.5V, TA = +25^{\circ}C)$$

Symbol	Parameter	Min	Тур	Max	Unit	Condition
tcyc6	System cycle time	600	-	-	ns	
tas6	Address setup time	0	-	-	ns	
tан6	Address hold time	0	-	-	ns	
tDS6	Data setup time	80	-	-	ns	
tdH6	Data hold time	30	-	-	ns	
toн6	Output disable time	20	-	140	ns	$C_L = 100 pF$
tacc6	Access time	-	-	280	ns	$C_L = 100 pF$
tewnw	Enable H pulse width (Write)	200	-	-	ns	
tewnr	Enable H pulse width (Read)	240	-	-	ns	
tewlw	Enable L pulse width (Write)	200	-	-	ns	
tewlr	Enable L pulse width (Read)	200	-	-	ns	
tr	Rise time	-	ı	30	ns	
tғ	Fall time	-	-	30	ns	



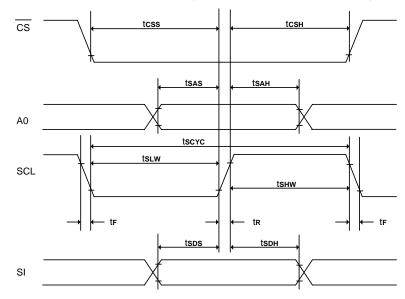


 $(VDD1 = 2.4 - 3.5V, T_A = +25^{\circ}C)$

Symbol	Parameter	Min	Тур	Max	Unit	Condition
tcyc6	System cycle time	300	-	-	ns	
tas6	Address setup time	0	-	-	ns	
tah6	Address hold time	0	ı	-	ns	
tds6	Data setup time	40	ı	-	ns	
tdH6	Data hold time	15	-	-	ns	
tон6	Output disable time	10	-	70	ns	$C_L = 100 pF$
tacc6	Access time	-	-	140	ns	C _L = 100pF
tewnw	Enable H pulse width (Write)	100	-	-	ns	
tewnr	Enable H pulse width (Read)	120	-	-	ns	
tewlw	Enable L pulse width (Write)	100	-	-	ns	
tewlr	Enable L pulse width (Read)	100	-	-	ns	
tr	Rise time	-	-	15	ns	
tғ	Fall time	-	-	15	ns	



(3) System buses Write characteristics 3(For the Serial Interface MPU)



$$(VDD1 = 1.65 - 3.5V, TA = +25^{\circ}C)$$

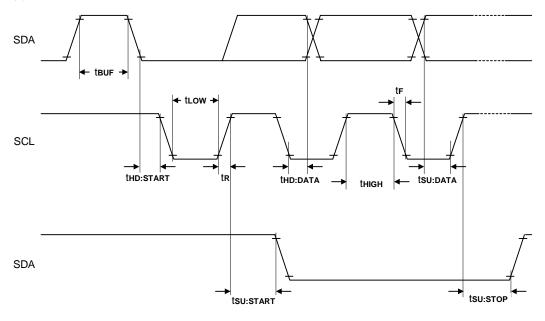
Symbol	Parameter	Min	Тур	Max	Unit	Condition
tscyc	Serial clock cycle	500	-	-	ns	
tsas	Address setup time	300	-	-	ns	
tsан	Address hold time	300	-	-	ns	
tsds	Data setup time	200	-	-	ns	
tsdн	Data hold time	200	-	-	ns	
tcss	CS setup time	240	-	-	ns	
tcsh	CS hold time time	120	-	-	ns	
tshw	Serial clock H pulse width	200	-	-	ns	
tslw	Serial clock L pulse width	200	-	-	ns	
tr	Rise time	_	-	30	ns	
tf	Fall time	-	-	30	ns	

$$(VDD1 = 2.4 - 3.5V, T_A = +25^{\circ}C)$$

Symbol	Parameter	Min	Тур	Max	Unit	Condition
tscyc	Serial clock cycle	250	-	-	ns	
tsas	Address setup time	150	-	-	ns	
tsан	Address hold time	150	-	-	ns	
tsds	Data setup time	100	-	-	ns	
tsdн	Data hold time	100	-	-	ns	
tcss	CS setup time	120	-	-	ns	
tсsн	cs hold time time	60	-	-	ns	
tshw	Serial clock H pulse	100	-	-	ns	
tslw	Serial clock L pulse	100	-	-	ns	
tr	Rise time	-	-	15	ns	
tf	Fall time	-	_	15	ns	



(4) I²C interface characteristics



$$(VDD1 = 1.65 - 3.5V, TA = +25^{\circ}C)$$

Symbol	Parameter	Min	Тур	Max	Unit	Condition
fscl	SCL clock frequency	DC	-	400	kHz	
Trow	SCL clock Low pulse width	1.3	-	-	uS	
Тнісн	SCL clock H pulse width	0.6	-	-	uS	
Tsu:data	data setup time	100	-	-	nS	
Thd:data	data hold time	0	-	0.9	uS	
Tr	SCL, SDA rise time	20+0.1Cb	-	300	nS	
TF	SCL , SDA fall time	20+0.1Cb	-	300	nS	
Cb	Capacity load on each bus line	-	-	400	pF	
Tsu:start	Setup timefor re-START	0.6	-	-	uS	
Thd:start	START Hold time	0.6	-	-	uS	
Tsu:stop	Setup time for STOP	0.6	-	-	uS	
Твиғ	Bus free times between STOP and START condition	1.3	-	-	uS	

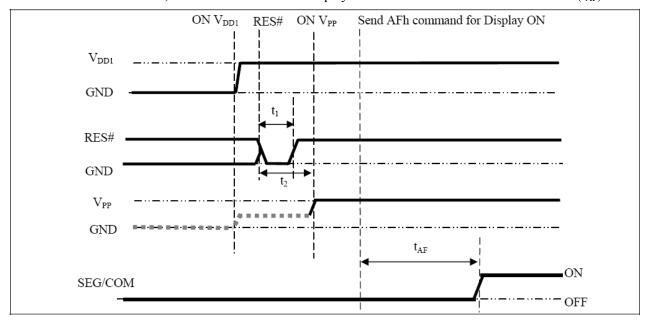


9 Functional Specification and Application Circuit

9.1 Power ON and Power OFF Sequence

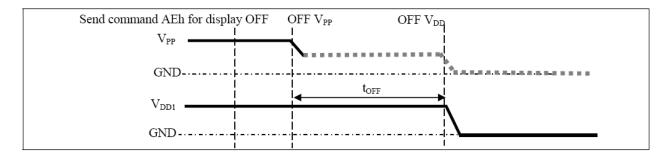
Power ON Sequence:

- 1. Power ON VDD1.
- 2. After VDD1 become stable, set RES pin LOW (logic low) for at least 5us (t₁) and then HIGH (logic high).
- 3. After set RES# pin LOW (logic low), wait for at least 5us (t₂). Then Power ON V_{PP} (1)
- 4. After VPP become stable, send command AFh for display ON. SEG/COM will be ON after 150ms(t_{AF}).



Power OFF Sequence:

- 1. Send command AEh for display OFF.
- 2. Power OFF VPP.(1), (2)
- 3. Wait for t_{OFF}. Power OFF VDD1. (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)



Note:

- (1) Since an ESD protection circuit is connected between VDD1 and VPP, VPP becomes lower than V_{DD1} whenever VDD1 is ON and VPP is OFF as shown in the dotted line of VPP in above figures.
- (2). VPP should be kept float (disable) when it is OFF.



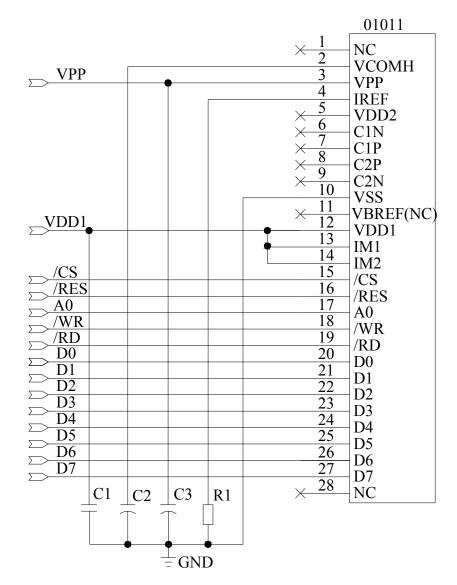
9.2 Application Circuit

9.2.1 Under external VPP Mode, the charge Pump Setting (ADh) must be set as follow:

ADh:Charge Pump Setting

8Ah:Disable Charge Pump

(1). The configuration for 8080-parallel interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: D[0:7],/RD, /WR, A0,/RES, /CS

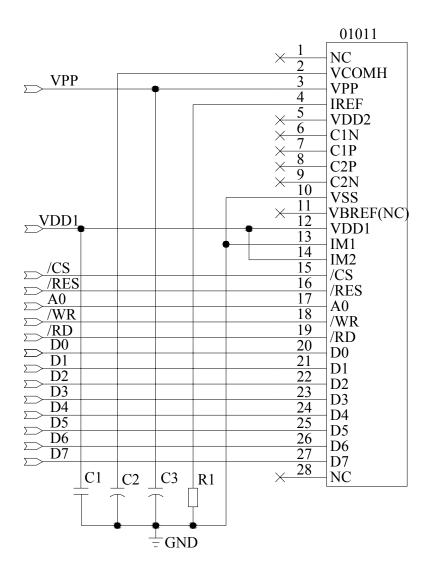
Recommended components

C1: 1uF-0603-X7R±10%.RoHS

C2,C3: 4.7µF/25V.RoHS (Tantalum Capacitors)



(2). The configuration for 6800-parallel interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: D[0:7],/RD, /WR, A0,/RES, /CS

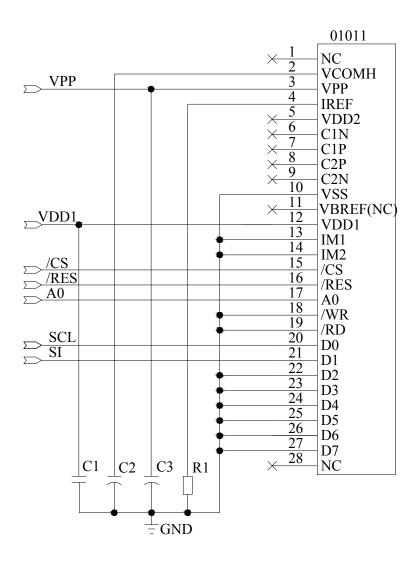
Recommended components

C1: 1uF-0603-X7R±10%.RoHS

C2,C3: 4.7µF/25V.RoHS (Tantalum Capacitors)



(3). The configuration for 4-wire SPI interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: SCL,SI, /CS,A0,/RES

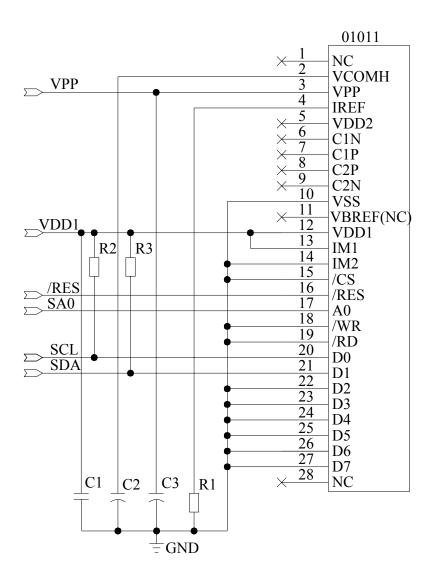
Recommended components

C1: 1uF-0603-X7R±10%.RoHS

C2,C3: 4.7µF/25V.RoHS (Tantalum Capacitors)



(4). The configuration for I²C interface mode, external VPP is shown in the following diagram:



Pin connected to MCU interface: SCL,SDA, SA0,/RES

Recommended components

C1: 1uF-0603-X7R±10%.RoHS

C2,C3: 4.7µF/25V.RoHS (Tantalum Capacitors)

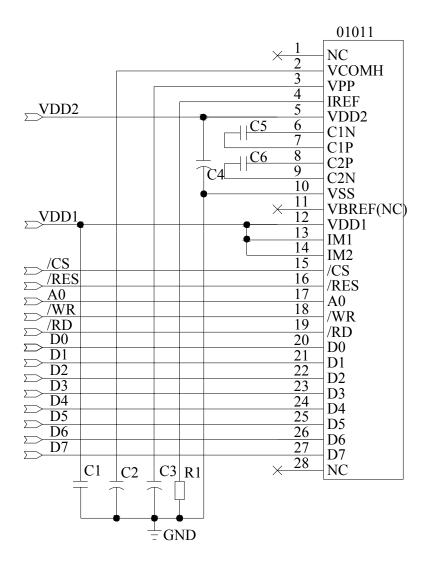
R1: 0603 1/10W +/-5% 910K ohm.RoHS



9.2.2 Under Internal DC/DC Mode, the charge Pump Setting (ADh) must be set as follow:

ADh:Charge Pump Setting 8Bh:Enable Charge Pump

The configuration for 8080-parallel interface mode, VPP Generated by Internal DC/DC Circuit is shown in the following diagram:



Pin connected to MCU interface: D[0:7], /RD, /WR, A0, /RES, /CS

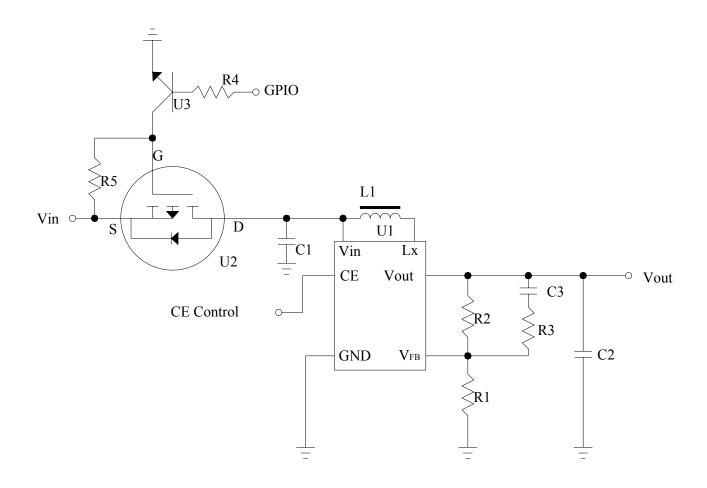
Recommended components

C1, C5, C6: 1uF-0603-X7R±10%.RoHS

C2,C3,C4: 4.7µF/25V.RoHS (Tantalum Capacitors)



9.3 External DC-DC application circuit



Recommend component

The C1 : 1 uF-0603-X7R±10%.RoHS

The C2 : 1 uF-0603-X7R±10%.RoHS

The C3 : 220pF-0603-X7R±10%.RoHS

The R1 : 0603 1/10W +/-5% 10Kohm.RoHS

The R2 : 0603 1/10W +/-5% 110Kohm.RoHS

The R3 : 0603 1/10W +/-5% 2Kohm.RoHS

The R4 : 0603 1/10W +/-5% 1Kohm.RoHS

The R5 : 0603 1/10W +/-5% 10Kohm.RoHS

The L1 : 22uH

The U1 : R1200

The U2 : FDN338P

The U3 : 8050



9.4 Display Control Instruction

Refer to SH1106G IC Specification.

9.5 Recommended Software Initialization

```
void Init IC()
{
   Write Command(0xAE);
                               //Display Off
   Write Command(0xd5);
                              //Divide Ratio/Oscillator Frequency Mode Set
   Write Command(0xC1);
                              //
   Write Command(0xA8);
                              //Multiplex Ration Mode Set
   Write Command(0x23);
   Write Command(0xD3);
                              //Display Offset Mode Set
   Write Command(0x0e);
   Write Command(0x40);
                              //Set Display Start Line
   Write Command(0xAD);
                              //DC-DC Control Mode Set
                              //DC-DC ON/OFF Mode Set
   Write Command(0x8b);
   Write Command(0x33);
                              //Set Pump voltage value
   Write Command(0xA1);
                              //Set Segment Re-map
   Write Command(0xC8);
                              //Set Common Output Scan Direction:
   Write Command(0xDA);
                              //Common Pads Hardware Configuration Mode Set
   Write Command(0x12);
   Write Command(0x81);
                              //The Contrast Control Mode Set
   Write Command(0xa3);
                              //
   Write Command(0xD9);
                              //Pre-charge Period Mode Set:
   Write Command(0x1f);
   Write Command(0xDB);
                               //VCOM Deselect Level Mode Set
   Write Command(0x40);
   Write Command(0xA4);
                              //Set Entire Display OFF/ON
   Write Command(0xA6);
                              //Set Normal/Reverse Display
   Write Command(0xAF);
                              //Display On
}
```

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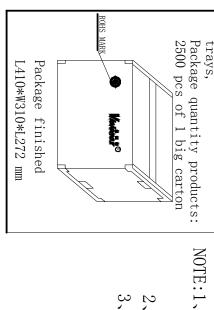
After tray be packaged, wrap the package in a

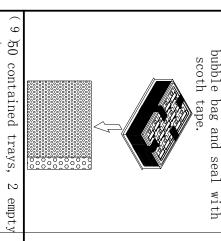
6

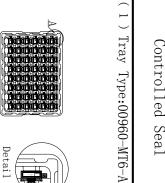
TRAY

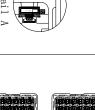


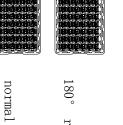
10 Package Specification













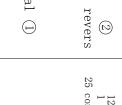
Packing Process(1)~(9)

(2)

(3) order(1)

(<u>2</u>)

(4) Use vaccum bag to package



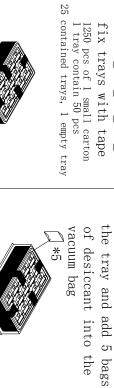






8

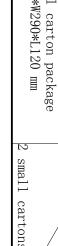








small carton package L390*W290*L120 mm



small cartons in 1 big carton

Fill up the gap with tray.

2 ယ

The inner carton

and

master carton must

be

sealed with

adhesive tape.

marking at the inner carton and master carton need adhesive new RoHS If the customer has special needs with the RoHS making,



11 Reliability

11.1 Reliability Test

NO.	ITEM	CONDITION	QUANTITY
1	High Temperature (Non-operation)	85℃,240hrs	4
2	Low Temperature (Non-operation)	-40°C,240hrs	4
3	High Temperature (Operation)	70°C,240hrs	4
4	Low Temperature (Operation)	-40°C,240hrs	4
5	High Temperature / High Humidity (Operation)	60°C,90%RH,240hrs	4
6	Thermal shock (Non-operation)	-40°C~85°C(-40°C/30min;transit/3min;85°C/30mi n;transit/3min) 1cycle: 66min,30cycles	4
7	Vibration	Frequency: 5~50Hz,0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X,Y, Z	1 Carton
8	Drop	Height: 100 cm Sequence: 1 angle, 3 edges and 6 faces	1 Carton

Test and measurement conditions

- 1. All measurements shall not be started until the specimens attain to temperature stability, the stable time is at least 15 minutes.
- 2. The degradation of polarizer is ignored for item 5.
- 3. The tolerance of temperature is $\pm 3^{\circ}$ C, and the tolerance of relative humidity is $\pm 5\%$.

Evaluation criteria

- 1. The function test is OK.
- 2. No observable defects.
- 3. Luminance: ≥50% of initial value.
- 4. Current consumption: within \pm 50% of initial value.

11.2 Lifetime

End of lifetime is specified as 50% of initial brightness and the test pattern at operating condition is 50% alternating checkerboard.

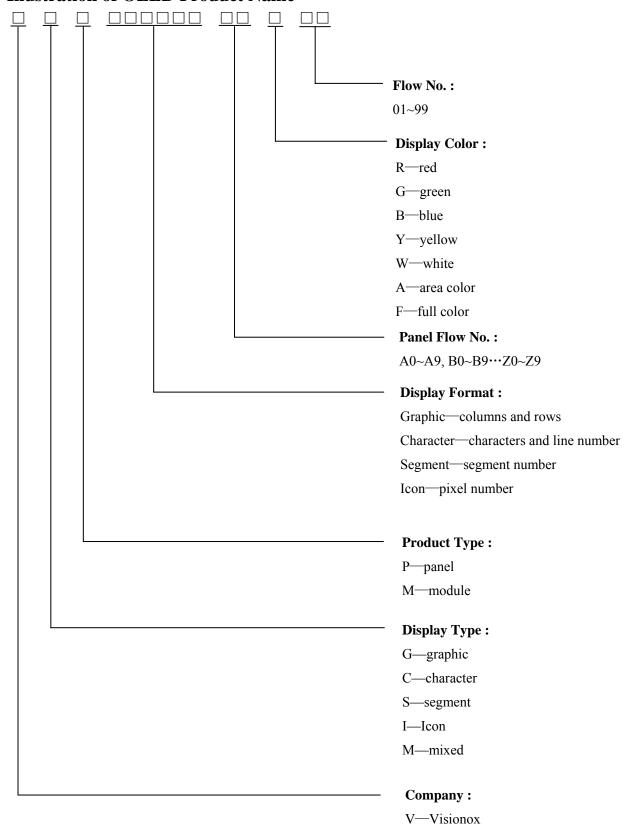
ITEM	MIN	MAX	UNIT	CONDITION
Operation Life Time	10,000	-	hrs	150 cd/m², 50% alternating checkerboard 22±3°C; 55±15% RH.

11.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 22±3°C; 55±15% RH.



12 Illustration of OLED Product Name





13 Outgoing Quality Control Specifications

13.1 Sampling Method

- (1) GB/T 2828.1-2003/ISO2859-1: 1999, inspection level II, normal inspection, single sample inspection
- (2) AQL: Major 0.65; Minor 1.0

13.2 Inspection Conditions

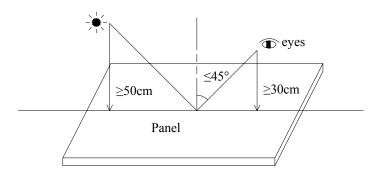
The environmental conditions for test and measurement are performed as follows.

Temperature: 22±3°C Humidity: 55±15%R.H Fluorescent Lamp: 30W

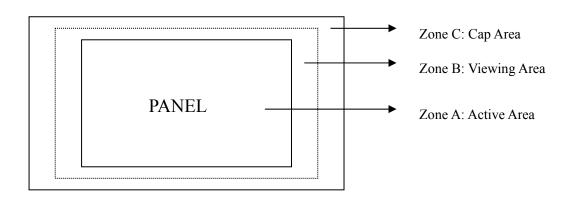
Distance between the Panel & Lamp: ≥50cm Distance between the Panel & Eyes: ≥30cm

Viewing angle from the vertical in each direction: ≤45°

(See the sketch below)



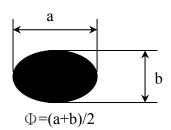
13.3 Quality Assurance Zones

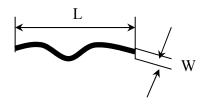




13.4 Inspection Standard

Definition of Φ&L&W (Unit: mm)





I . Appearance Defects

NO.	ITEM		CLASSIFICATION						
1	Polarizer Black or White spot, Dirty spot, Foreign matter, Dent on the polarizer	Average Diameter (mm) Φ≤0.15 0.15<Φ≤0.30 Φ>0.30	Zone	Zone A,B Ignore 3		nore 3 Ignore		Zone C	Minor
2	Scratch/line on the glass/Polarizer	Width (mm) W≤0.03 0.03 <w≤0.08 W>0.08</w≤0.08 	Length (mm) L≤5.0	Accep Zone A Ignor 3	A,B	Number Zone C Ignore	Minor		
3	Polarizer Bubble	Average Diamete (mm) Φ>0.5 0.2<Φ≤0.5 Φ≤0.2	Zo	Acceptabone A,B 0 3 gnore		umber Zone C Ignore	Minor		
4	Any Dirt & Scratch on Polarizer's Protective Film	Ignore for not affect the polarizer.					Minor		
5	Any Dirt on Cap Glass	Average Diameter (mm) Φ≤0.5 0.5<Φ≤1.0 Φ>1.0		Acceptable Number Ignore 3 0			Minor		

Propagation crack is not acceptable. Propagation crack is not acceptable. Propagation crack is not acceptable. Minor E Glass thickness Accept a≤2.0mm or b≤2.0mm, e≤t E Glass thickness Accept a≤1.5mm or b≤1.5mm, e≤t (on the contact pin) a≤3.0mm or b≤3.0mm, e≤t (outside of the contact pin) E Glass thickness Accept a≤3.0mm or b≤1.5mm, e≤t (outside of the contact pin) E Glass thickness Accept a≤1.5mm or b≤1.5mm, e≤t (outside of the contact pin) E Glass thickness Accept a≤1.5mm or b≤1.5mm, e≤t (outside of the contact pin) E Glass thickness Accept a≤1.5mm or b≤1.5mm, e≤t (outside of the contact pin) E Glass thickness Accept a≤1.5mm or b≤1.5mm, e≤t (outside of the contact pin) E Glass thickness Accept a≤1.5mm or b≤1.5mm, e≤t (outside of the contact pin) E Glass thickness Accept a≤1.5mm or b≤1.5mm, e≤t (outside of the contact pin) E Glass thickness Accept a≤1.5mm or b≤1.5mm, e≤t (outside of the contact pin) E Glass thickness Accept a≤1.5mm or b≤1.5mm, e≤t (outside of the contact pin) Minor E Glass thickness Accept a≤1.5mm or b≤1.5mm, e≤t (outside of the contact pin) E Glass thickness Accept a≤1.5mm or b≤1.5mm, e≤t (outside of the contact pin) E Glass thickness Accept a≤3.0mm or b≤3.0mm, e≤t (outside of the contact pin) Minor E Glass thickness Accept a≤1.5mm or b≤1.5mm, e≤t (outside of the contact pin) E Glass thickness Accept a≤3.0mm or b≤3.0mm, e≤t a≤1.5mm or b≤1.5mm, e	6	Glass Crack		Major
Temporaria Tem			Propagation crack is not acceptable.	
Accept a≤2.0mm or b≤2.0mm, e≤t 8	7	Corner Chip		Minor
Teglass thickness Accept a≤1.5mm or b≤1.5mm, c≤t Pad Chip on Contact Pad Chip on Face of Display Teglass thickness Accept a≤3.0mm or b≤1.5mm, c≤t (on the contact pin) Teglass thickness Accept a≤1.5mm or b≤1.5mm, c≤t (outside of the contact pin) Minor Teglass thickness Accept a≤1.5mm or b≤1.5mm, c≤t Accept a≤1.5mm or b≤1.5mm, c≤t a≤1.5mm or b≤1.5mm, c≤t Accept a≤1.5mm or b≤1.5mm, c≤t acceptable. Accept a≤1.5mm or b≤1.5mm, c≤t acceptable. Accept acceptable.			Accept	
Accept a≤1.5mm or b≤1.5mm, c≤t Pad Chip on Contact Pad t= Glass thickness Accept a≤3.0mm or b≤0.8mm, c≤t (on the contact pin) a≤3.0mm or b≤1.5mm, c≤t (outside of the contact pin) This play t= Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t (outside of the contact pin) This play t= Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t a≤1.5mm or b≤1.5mm, c≤t This play	8		to Class this lyness	Minor
9 Chip on Contact Pad 10 Chip on Face of Display 11 Chip on Cap Glass 12 Stain on Surface 13 TCP/FPC Damage 14 Dimension 15 Chip on Contact Pad 16 Chip on Face of Display 17 E Glass thickness Accept a≤3.0mm or b≤0.8mm, c≤t (on the contact pin) a≤3.0mm or b≤1.5mm, c≤t (outside of the contact pin) 10 Chip on Face of Display 11 Chip on Cap Glass 12 Stain on Surface 13 TCP/FPC Damage 14 Dimension 15 Chip on Sourface 16 Chip on Cap Glass 17 E Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t 18 Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t 19 Minor 10 Chip on Cap Glass 11 Chip on Cap Glass 12 Stain on Surface 13 TCP/FPC Damage 14 Dimension 15 Chip on Cap Glass 16 Chip on Cap Glass 17 E Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t 18 Minor Minor Minor Minor Minor Minor Major		Cup Glass		
Pad Pad F Glass thickness Accept a≤3.0mm or b≤0.8mm, c≤t (on the contact pin) a≤3.0mm or b≤1.5mm, c≤t (outside of the contact pin)				
Accept a≤3.0mm or b≤0.8mm, c≤t (on the contact pin) a≤3.0mm or b≤1.5mm, c≤t (outside of the contact pin) 10 Chip on Face of Display 11 Chip on Cap Glass 12 Stain on Surface 13 TCP/FPC Damage 14 Dimension Accept a≤1.5mm or b≤1.5mm, c≤t 16 Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t 17 Glass thickness Accept a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t 18 Minor Minor Minor Minor 19 Orack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection. Major	9		t= Glass thickness	Minor
Display t = Glass thickness Accept a≤1.5mm or b≤1.5mm, c≤t 11 Chip on Cap Glass Minor t = Glass thickness Accept a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t 12 Stain on Surface Stain removable by soft cloth or air blow is acceptable. 13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection. Major		Tuu	a \leq 3.0mm or b \leq 0.8mm, c \leq t (on the contact pin) a \leq 3.0mm or b \leq 1.5mm, c \leq t	
Accept a≤1.5mm or b≤1.5mm, c≤t 11 Chip on Cap Glass Minor t= Glass thickness Accept a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t 12 Stain on Surface Stain removable by soft cloth or air blow is acceptable. Minor TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection. Major	10			Minor
a≤1.5mm or b≤1.5mm, c≤t 11		Display		
t= Glass thickness Accept a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t 12 Stain on Surface Stain removable by soft cloth or air blow is acceptable. 13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection. 14 Dimension Checking by mechanical drawing Major				
Accept a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t 12 Stain on Surface Stain removable by soft cloth or air blow is acceptable. 13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection. 14 Dimension Checking by mechanical drawing Major	11	Chip on Cap Glass		Minor
a≤3.0mm or b≤3.0mm, c≤t/2 a≤1.5mm or b≤1.5mm, t/2≤c≤t 12 Stain on Surface Stain removable by soft cloth or air blow is acceptable. 13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection. 14 Dimension Checking by mechanical drawing Major				
a≤1.5mm or b≤1.5mm, t/2≤c≤t 12 Stain on Surface Stain removable by soft cloth or air blow is acceptable. 13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection. 14 Dimension Checking by mechanical drawing Major				
13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection. 14 Dimension Checking by mechanical drawing Major				
13 TCP/FPC Damage (1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable. (2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection. 14 Dimension Checking by mechanical drawing Major	12	Stain on Surface	Stain removable by soft cloth or air blow is accontable	Minor
(2) Terminal lead twisted or broken is not allowable. (3) Copper exposed is not allowed by naked eye inspection. 14 Dimension Checking by mechanical drawing Major			(1) Crack, deep scratch, deep hole and deep pressure mark on	
14 Dimension Checking by mechanical drawing Major			(2) Terminal lead twisted or broken is not allowable.	
	14	Dimension Unconformity		Major





II. Displaying Defects

NO.	ITEM		CLASSIFICATION		
1	Black/White spot Dirty spot Foreign matter	Average Diameter (mm) Φ≤0.10 0.10<Φ≤0.20 Φ>0.20	Pieces Permitted Zone A,B Zone C Ignore 3 Ignore 0		Minor
2	No Display	N	Major		
3	Irregular Display	N	Major		
4	Missing Line (row or column)	N	Major		
5	Short	N	Major		
6	Flicker	N	Major		
7	Abnormal Color	Ref	Major		
8	Luminance NG	Ref	Major		
9	Over Current	Ref	Major		



14 Precautions for operation and Storage

14.1 Precautions for Operation

- (1) Since OLED panel is made of glass, do not apply any mechanical shock or impact or excessive force to it when installing the OLED module. Any strong mechanical impact due to falling dropping etc. may cause damage (breakage or cracking).
- (2) The polarizer on the OLED surface is made of soft material and is easily scratched. Please take most care when handing. When the surface of the polarizer of OLED Module is contaminated, please wipe it off gently by using moisten soft cloth with isopropyl alcohol, do not use water, ketone or aromatics. If there is saliva or water on the OLED surface, please wipe it off immediately.
- (3) When handling OLED module, please be sure that the body and the tools are properly grounded. And do not touch I/O pins with bare hands or contaminate I/O pins, it will cause disconnection or defective insulation of terminals.
- (4) Do not attempt to disassemble or process the OLED module.
- (5) OLED module should be used under recommended operating conditions shown in the specification. Since the higher voltage leads to the shorter lifetime, be sure to use the specified operating voltage.
- (6) Foggy dew, moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage, the deteriorated display quality and electrochemical reaction then leads to shorter life time and permanent damage to the module probably. Please pay attention to the environmental temperature and humidity.
- (7) An afterimage is created by the difference in brightness between unused dot and the fixed dot, according to the decrease of brightness of the emitting time. Therefore, to avoid having an afterimage, the full set should be thoroughly used instead of using a fixed dot. When the fixed dot emits, an afterimage can be created.
- (8) Flicker could be come out at full on display. And it disappears when frame frequency increase, but brightness decreases too.

14.2 Soldering

- (1) Soldering should be performed only on the I/O terminals.
- (2) Use soldering irons with proper grounding and no leakage.
- (3) Iron: no higher than 300°C and 3~4 sec during soldering.

14.3 Precautions for Storage

- (1) Please store OLED module in a dark place. Avoid exposure to sunlight, the light of fluorescent lamp or any ultraviolet ray.
- (2) Keep the environment temperature between 10°C and 35°C and the relative humidity less than 60%. Avoid high temperature and high humidity.
- (3) Keep the OLED modules stored in the container when shipped from supplier before using them is recommended.
- (4) Do not leave any article on the OLED module surface for an extended period of time.

14.4 Warranty period

Visionox warrants for a period of 12 months from the shipping date when stored or used under normal condition.