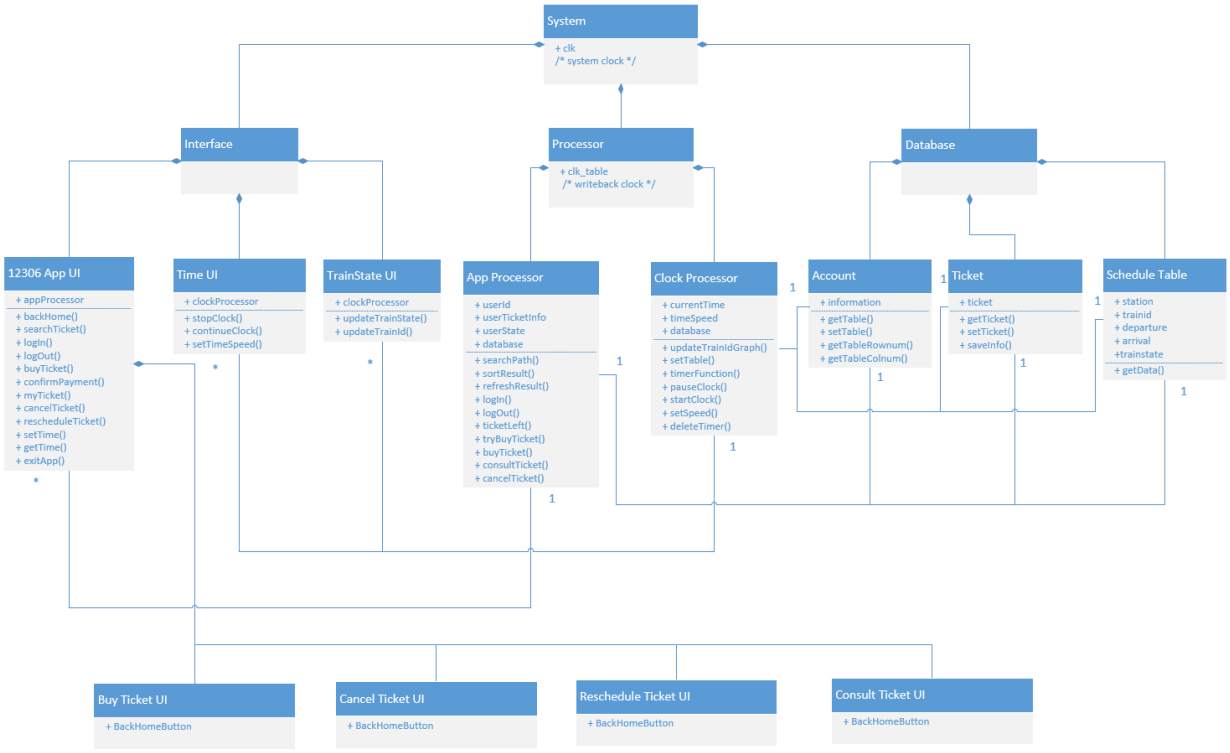
Traceability

Content

System Architecture



Software Traceability

Requirement	Implemented By	Validated By
R1 12306 APP	S0, S1, S2, S3, S4, S5, S6, S7	
R1.1	S1	T1.3, T2.1, T2.2, T2.3
R1.1.1	S1.1	T2.3.1, T2.3.2, T2.3.3
R1.1.2	S1.2	T2.1.1, T2.2.1, T2.3.3, T2.3.4, T2.3.5
R1.1.3	S1.3	T1.3.1, T1.3.3, T1.3.2, T1.3.4, T2.1.1, T2.2.1, T2.3.3, T2.3.4, T2.3.5
R1.1.4	S1.4	T2.1.1, T2.2.1, T2.3.3, T2.3.4, T2.3.5
R1.2	S2	T1.5, T2, T3
R1.2.1	S2.1	T1.5.3, T2.1.1, T2.2.1, T2.3.3, T2.3.4, T2.3.5
R1.2.2	S2.2	T1.5.3, T3.1.1, T2.3.6
R1.2.3	S2.3	T1.5.2, T3.1.1, T2.3.6
R1.3	S3	T1.2, T1.5, T2, T3
R1.3.1	S3.1	T1.5.2
R1.3.2	S3.2	T1.2.3, T1.2.2, T1.5.7, T2.1.1, T2.2.1, T2.3.3, T2.3.4, T2.3.5, T3.1.1
R1.3.3	S3.3	T2.1.1, T2.2.1, T2.3.3, T2.3.4, T2.3.5, T3.1.1
R1.4	S4	T1.3, T1.5, T2.1, T2.2, T3
R1.4.1	S4.1	T2.1, T2.2, T3.1.1
R1.4.2	S4.2	T1.3, T1.5.3, T1.5.4, T1.5.5, T1.5.6, T2.1, T2.2, T3.1.1
R1.5	S5	T1.2, T1.3, T1.5, T2.1, T2.2, T3
R1.5.1	S5.1	T1.6, T1.2.5, T1.3, T1.5.3, T1.5.4, T1.5.5, T1.5.6, T2.1, T2.2, T3.1.1
R1.5.2	S5.2	T2.1, T2.2, T3.1.1
R1.5.3	S5.3	T3.1.1
R1.6	S6	T1.1, T1.2, T1.3, T1.5, T2.1, T3.1
R1.6.1	S6.1	T2.1.1, T2.2.1, T2.3.3, T2.3.4, T2.3.5, T3.1.1
R1.6.2	S6.2	T1.1.1, T1.3, T1.5.3, T1.5.4, T1.5.5, T1.5.6, T1.5.7, T1.5.8, T2.1.1, T3.1.1
R1.6.3	S6.3, S6.5	T1.1.1, T1.2.5, T1.2.6, T1.3, T1.5.3, T1.5.4, T1.5.5, T1.5.6, T1.5.7, T1.5.8, T2.1, T3.1.1

Requirement	Implemented By	Validated By
R1.6.4	S6.4	T1.1.1, T2.3.4, T2.3.5
R1.7	S7	T1.1, T1.3, T1.5, T2.1, T3
R1.7.1	S7.1	T1.1.1, T1.3, T1.5.3, T1.5.4, T1.5.5, T1.5.6, T1.5.7, T1.5.8, T2.1.1, T3.1.1
R1.7.2	S7.2, S7.4, S7.7, S7.9	T2.1.1, T3.1.1
R1.7.3	S7.3, S7.5	T1.1.1, T1.3, T1.5.3, T1.5.4, T1.5.5, T1.5.6, T1.5.7, T1.5.8, T2.1.1, T3.1.1
R1.7.4	S7.4, S7.6, S7.8	T1.1.1, T1.3, T1.5.3, T1.5.4, T1.5.5, T1.5.6, T1.5.7, T1.5.8, T2.1.1, T3.1.1
R2 Time Controller	S8	T1.4, T2, T3
R2.1	S8	T1.4, T2.3, T3.1
R2.1.1	S8.1	T2.3, T3.1.1
R2.1.2	S8.2	T1.4.1, T2.3.1
R2.1.3	S8.3	T1.4.2, T2.3.1
R3 Train State Display	S9	T1, T2
R3.1	S9	T1.1, T1.2, T2
R3.1.1	S9.1	T1.1.1, T1.2.2, T1.2.3, T2.3.2
R3.1.2	S9.2	T1.2.7, T2
R4 Concurrency	S10	T2.3.6
R4.1	S10	T2.3.6
R4.1.1	S10.1	T2.3.6