Wire Table

Wire ID	Wire Name	Source Port ID	Source Component	Source Port Name	Destination Port ID	Destination Comonent	Destination Port Name	Bus Width
1	clk	9	Processor	clk	1	Register File	clk	1
2	gwe	48	Processor	gwe	2	Register File	gwe	1
3	rst	47	Processor	rst	3	Register File	rst	1
4	o_rs	10	Decoder	r1sel	4	Register File	i_rs	3
5	o_rt	11	Decoder	r2sel	5	Register File	i_rt	3
6	o_rd	12	Decoder	wsel	6	Register File	i_rd	3
7	o_rd_we	13	Decoder	regfile_we	8	Register File	i_rd_we	1
8	o_rd_data	14	Data Controller	wdata	7	Register File	i_wdata	16
9	o_rs_data	15	Register File	o_rs_data	17	Data Controller	r1data	16
10	o_rt_data	16	Register File	o_rt_data	18	Data Controller	r2data	16
11	nzp_we	21	Decoder	nzp_we	28	NZP Controller	nzp_we	1
12	select_pc_pl	22	Decoder	select_pc_plus_one	55	Data Controller	select_pc_plus_one	1
13	is_load	23	Decoder	is_load	34	Data Controller	is_load	1
14	is_store	24	Decoder	is_store	53	Processor	o_dmem_we	1
15								
16								
17	insn_dec	50	Processor	i_cur_insn	27	Decoder	insn	16
18	wdata_nzp	14	Data Controller	wdata	29	NZP Controller	wdata	16
19	o_nzp	30	NZP Controller	o_nzp	56	Branch Controller	o_nzp	3
20	insn_data	50	Processor	i_cur_insn	31	Data Controller	insn	16
21	i_pc1	44	Incrementer	o_pc	32	Data Controller	i_pc1	16
22	dmem_load	52	Processor	i_cur_dmem_data	33	Data Controller	dmem_load	16
23	o_pc	35	Data Controller	o_pc	49	Processor	o_cur_pc	16
24	dmem_store	37	Data Controller	dmem_store	54	Processor	o_dmem_towrite	16
25	dmem_addr	39	Data Controller	dmem_addr	51	Processor	o_dmem_addr	16
26	clk_nzp	9	Processor	clk	40	NZP Controller	clk	1
27	gwe_nzp	48	Processor	gwe	41	NZP Controller	gwe	1
28	rst_nzp	47	Processor	rst	42	NZP Controller	rst	1
29	inc_pc	49	Processor	o_cur_pc	43	Incrementer	i_pc	16
30	is_branch	25	Decoder	is_branch	57	Branch Controller	is_branch	1
31	is_control_in	26	Decoder	is_control_insn	58	Branch Controller	is_control_insn	1
32	insn_br	50	Processor	i_cur_insn	60	Branch Controller	insn	16
33	take_branch	59	Branch Controller	take_branch	38	Data Controller	take_branch	1