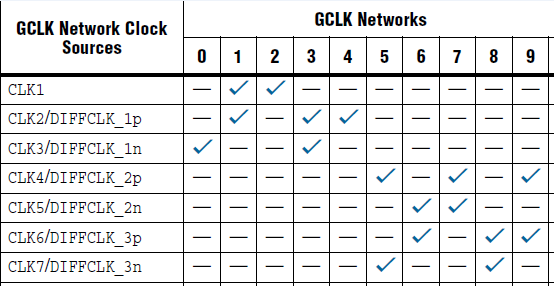
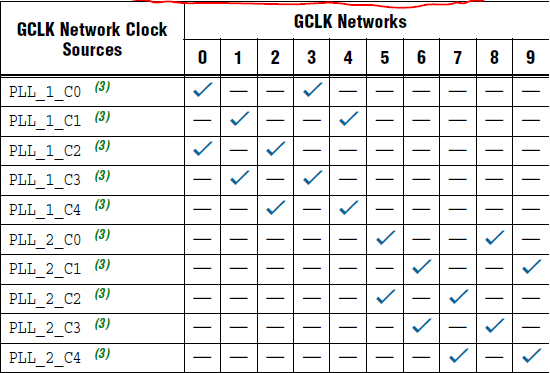
**CLOCK INFORMATION**

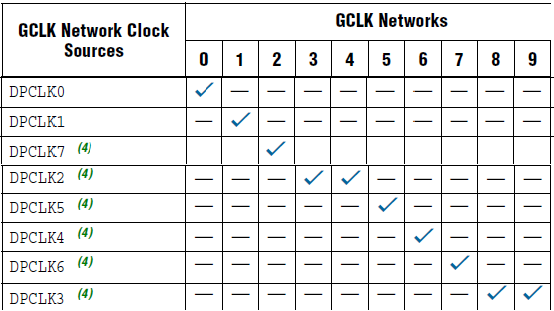
EP4CE10 devices only support three dedicated clock pins on the left side and four dedicated clock pins on the right side of the device.

**GCLK**

1. All resources in the device (I/O elements, logic array blocks (LABs), dedicated multiplier blocks and M9K memory blocks) can use GCLKs as clock sources. Use these clock network resources for control signals, such as clock enables and clears fed by an external pin.
2. Internal logic can also drive GCLKs for internally generated GCLKs and asynchronous clears, clock enables, or other control signals with high fan-out.(?)



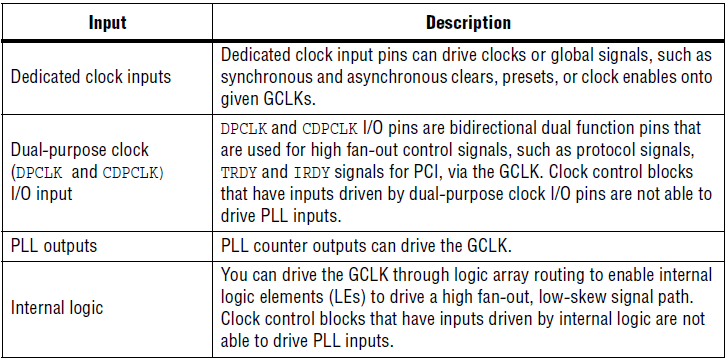




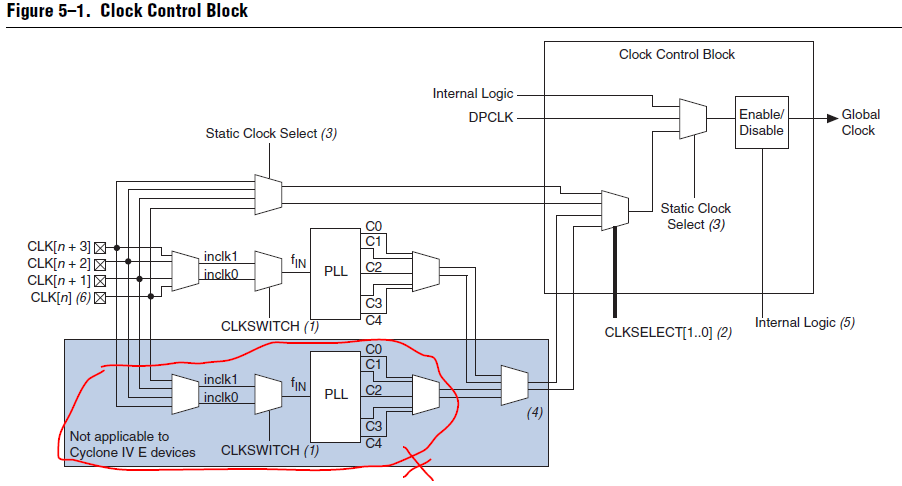
1. If you do not use dedicated clock pins to feed the GCLKs, you can use them as general-purpose input pins to feed the logic array. However, when using them as general-purpose input pins, they do not have support for an I/O register and must use LE-based registers in place of an I/O register.

**CLOCK CONTROL BLOCK**

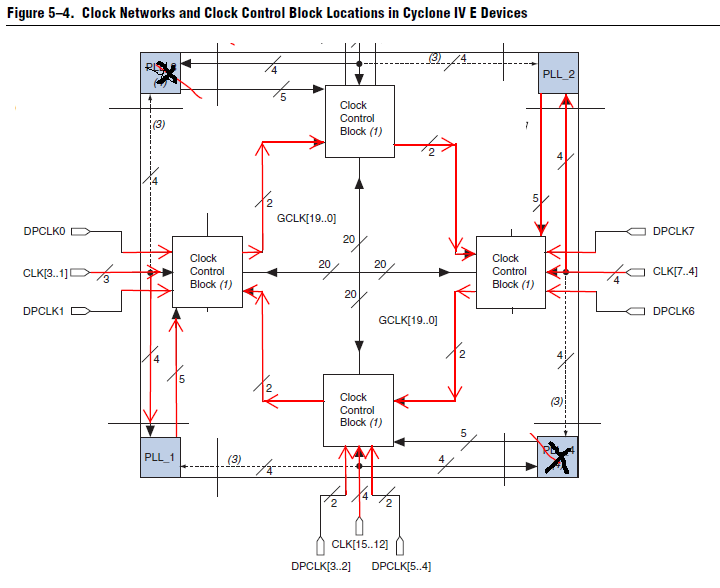
1. The clock control block drives the GCLKs. Clock control blocks are located on each side of the device, close to the dedicated clock input pins. GCLKs are optimized for minimum clock skew and delay.
2. The sources that can feed back the clock control block



The output from the clock control block in turn feeds the corresponding GCLK. The GCLK can drive the PLL input if the clock control block inputs are outputs of another PLL or dedicated clock input pins.

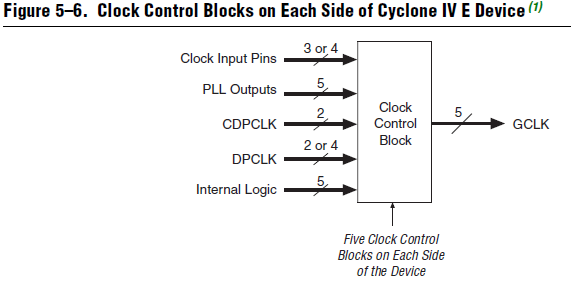


1. Clock Networks and Clock Control Block Locations in Cyclone IV E Devices



1. The inputs to the five clock control blocks on each side of the Cyclone IV E device must be chosen from among the following clock sources:

* Three or four clock input pins, depending on the specific device
* Five PLL counter outputs
* Two DPCLK pins and two CDPCLK pins from both the left and right sides and four DPCLK pins from both the top and bottom
* Five signals from internal logic



**Clock control block user guides**

Note: The IP Catalog (Tools > IP Catalog) and parameter editor replace the MegaWizard™ Plug-In Manager for IP selection and parameterization, beginning in Quartus II software version 14.0.

1. MegaWizard Parameter Settings
2. In the IP Catalog (Tools > IP Catalog), locate and double-click the name of the IP core to customize. The parameter editor appears.
3. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named <your\_ip>.qsys. Click OK.
4. Specify the parameters and options for your IP variation in the parameter editor, including one or more of the following. Refer to your IP core user guide for information about specific IP core parameters.
5. Click Generate HDL, the Generation dialog box appears. Specify output file generation options, and then click Generate. The IP variation files generate according to your specifications.
6. Specify output file generation options, and then click Generate. The IP variation files generate according to your specifications.
7. To generate a simulation testbench, click Generate > Generate Testbench System.
8. To generate an HDL instantiation template that you can copy and paste into your text editor, click Generate > HDL Example.
9. Click Finish. The parameter editor adds the top-level .qsys file to the current project automatically. If you are prompted to manually add the .qsys file to the project, click Project > Add/Remove Files in Project to add the file.
10. After generating and instantiating your IP variation, make appropriate pin assignments to connect ports.