ADN2814:

**Feature:**

Serial data input: 10 Mb/s to 675 Mb/s

Single-supply operation: 3.3 V

**THEORY OF OPERATION**

The ADN2814 is a delay- and phase-locked loop circuit for clock recovery and data retiming from an NRZ encoded data stream. The phase of the input data signal is tracked by two separate feedback loops, which share a common control voltage.

A high speed delay-locked loop path track the high frequency components of input jitter. A separate phase control loop track the low frequency components of input jitter.

Another view of the circuit is that the phase shifter implements the zero required for frequency compensation of a second-order phase-locked loop, and this zero is placed in the feedback path and, thus, does not appear in the closed-loop transfer function. Jitter peaking in a conventional second-order phase-locked loop is caused by the presence of this zero in the closed-loop transfer function. Because this circuit has no zero in the closed-loop transfer, jitter peaking is minimized.

(a second-order phase-locked loop是什么；Jitter peaking是什么；)

二阶PLL：传递函数是二阶地的