Reference Manual for the Verilog Memory Model Simulation Component

(version 0.1 draft)

Simon Southwell

August 2021

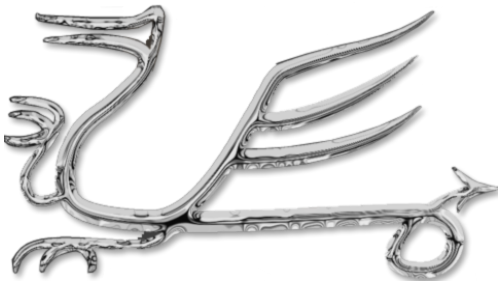
Copyright

Disclaimers

No warranties: the information provided in this document is “as is” without any express or implied warranty of any kind including warranties of accuracy, completeness, merchantability, non-infringement of intellectual property, or fitness for any particular purpose. In no event will the author be liable for any damages whatsoever (whether direct, indirect, special, incidental, or consequential, including, without limitation, damages for loss of profits, business interruption, or loss of information) arising out of the use of or inability to use the information provided in this document, even if the author has been advised of the possibility of such damages.

Simon Southwell (simon@anita-simulators.org.uk)

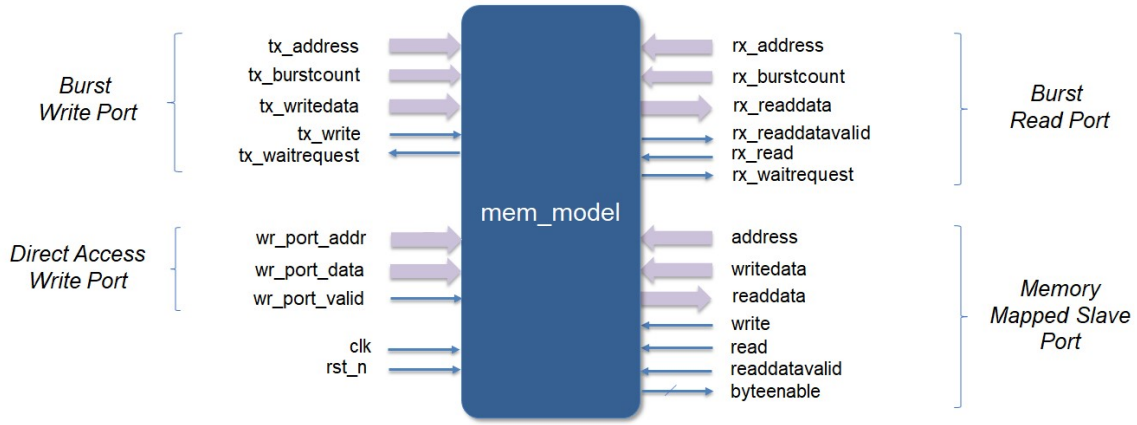
Cambridge, UK, August 2021



Introduction

The `mem_model` component is a Verilog simulation test component that allows for a very large memory address space without reserving large amounts of memory, defining large Verilog arrays, or building a truncated memory map into a test bench which could be subject to change in the design. The model uses the Verilog PLI to access a C model, pushing the majority of the functionality away from the simulator, make the test bench lightweight, and the memory accesses very fast in simulation compute time.

The component is a lightweight behavioural Verilog module, and uses the PLI interface to communicate with a set of C/C++ software to implement the actual memory model. The Verilog components itself looks like the following:



The component has a clock and reset and four data transfer interfaces.

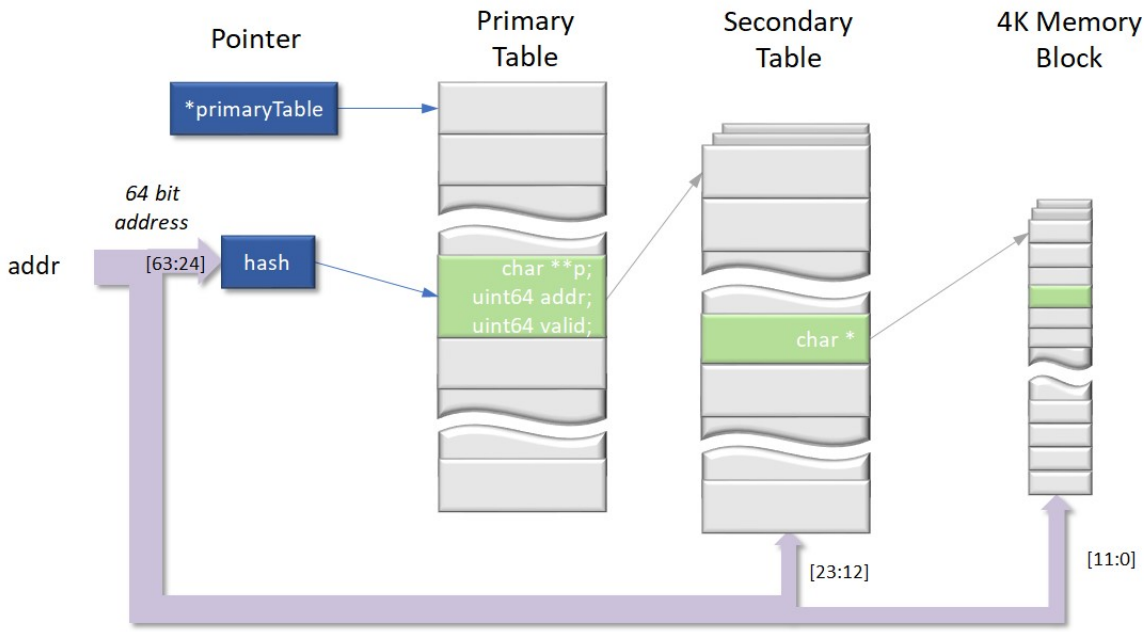
- A memory mapped slave port, for connection to, say, a CPU bus for straight forward word reads and writes with byte enables.
- A burst read port for DMA like read transfers. Note, 4K byte boundaries should not be crossed in a single burst.
- A burst write port for DMA like write transfers. Note, 4K byte boundaries should not be crossed in a single burst.
- A simple SRAM like direct access write port, useful in streaming test data directly to memory.

Not all the interfaces need to be connected, but unused interfaces should have their strobe inputs tied off to 0. If multiple interfaces are active, thought, the model will service them in parallel. If two interfaces are accessing the same location in the same cycle, though, behavior is undefined.

Internal Memory Structure

The memory model component has access to a full 32 bit address space via internal C/C++ memory model software, originally used on a PCIe verification component [1], which actually has capabilities for a full 64 bit address space. It does this with routines defined in `mem.c`, which initialise with no actual memory space allocated. As shown on the diagram, normally only `ProcessInput()` has access to the memory, and `mem.c` provides two functions for writes and reads—`WriteRamByteBlock()` and `ReadRamByteBlock()`. The user code has access to these functions, as well as some byte and word access hybrid versions.

The full 64 bit space capability relies on the fact that a simulation run cannot possibly write to all 2^{64} locations. Instead, the space is divided into 4K byte chunks which get dynamically allocated as required, and are accessed via references in a series of tables which further divided the address space. The starting point for a lookup is the `PrimaryTable`. This table has 4K entries, but maps all the top 40 bits of the address space into this space, using a simple hash, XORing the bits in a certain way and then bit reversing the 12 bit result. The `PrimaryTable` entry structure (`PrimaryTable_t`) has a valid field and an address for storing the top 40 bits of the address that hits on the location. If another address upper 40 bits hashes to the same location, then the index pointing to the table entry is simply incremented until an empty entry is found, or we searched the whole table (an error condition).



The primary table entry also contains a pointer to a pointer, which references a secondary table, dynamically allocated when first written to. The secondary tables sub-divide the address space of the lower 24 bits of the address into the 4K byte blocks required. The upper 12 bits of the lower address index into the secondary table, whose entry points to a 4K byte block of memory, dynamically allocated on first access.

Reading from a location simply involves traversing the table. The top 40 bits of the read address are hashed, and index into the primary table. The Primary table entry address is compared with the read address 40 bits and, if different, the index is incremented until a match, an invalid address is encountered or the whole table is searched. The last two cases are an error condition. The secondary table is then accessed with the next 12 bits and (if pointing to a valid byte block), the lower 12 bits used to retrieved the data. At any point in the traverse, an unallocated table entry of byte block is considered a fatal error—it is not legal to access locations that have not be written.

Compiling PLI code

The model's source code is a set of C files that must be compiled into a shared object, and entries added to a PLI table in order to add the necessary functions in the Verilog domain. The exact procedure varies somewhat between simulators, but examples for ModelSim are given here. In a file, `veriuser.c`, the following code must be present

```
#include "veriuser.h"
#include "vpi_user.h"

s_tfcell veriusertfs[] =
{
    {usertask, 0, NULL, 0, MemRead,   NULL,  "$memread",   1},
    {usertask, 0, NULL, 0, MemWrite,  NULL,  "$memwrite",  1},
    {0}
};

p_tfcell bootstrap ()
{
    return veriusertfs;
}
```

This table can only be defined once, so if there are other entries required from other PLI code, then these must be combined into a single table. For convenience, the table entries are defined in `mem.h` as a `#define` of `MEM_MODEL_TF_TBL`.

Various flags are required when compiling the code to generate a shared object, load the simulator's PLI library and ensure no (as yet) unreferenced entries are removed at link time. The verification environment (see next section) has example compilation code in a `makefile`, using the virtual processor (VProc) component [2], and calling it's `makefile`. The VProc repository has several examples of compiling a shared object, suitable for loading to various simulators, and the reader should reference these for more details.

For ModelSim, once the shared object is correctly compiled it can be loaded when running `vsim` by using the `-pli <mysharedobj>.so` command line option.

Test Environment

A Verilog test environment for the model is provided. It is dependent on VProc [2], which should be checked out into the same directory as the location of the memory model's repository. Currently it only supports ModelSim.

The test bench folder (`test`) contains the following files:

- `tb.v`: the top level test bench Verilog
- `cpu.v`: a VProc wrapper block that instantiates VProc, and drives the memory mapped master bus
- `files_vlog.tcl`: a list of all the Verilog files required by `vlog`.
- `makefile`: the compilation and execution make file
- `cleanvlib.do`, `compile.do`: ModelSim files for cleaning the Verilog work library and compiling the code, respectively.
- `sim.do`, `simg.do`, `simlog.do`: ModelSim files for running the simulation in various modes (batch, GUI, with logging).

The source code for the Virtual Processor is in a sub-folder `src`. As well as the top level VUserMain0 code (the virtual processor is set as node 0), it has some driver code for generating the access traffic on the master bus. This driver code is in `mem_vproc_api.cpp` and `mem_vproc_api.h`. The code provides some simple functions to read and write byte, half-word (16 bits) and word (32 bit) values. It is from these functions that calls to the VProc API are made, hiding the details of these, and also managing the byte enable settings with delta time updates.

References

[1] *PCIe Virtual Host Model Test Component*, https://github.com/wyvernSemi/pcievhost/blob/master/doc/pcieVHost.pdf, Simon Southwell, March 2017.

[2] *Virtual Processor (VProc),* https://github.com/wyvernSemi/vproc , Simon Southwell, June 2010