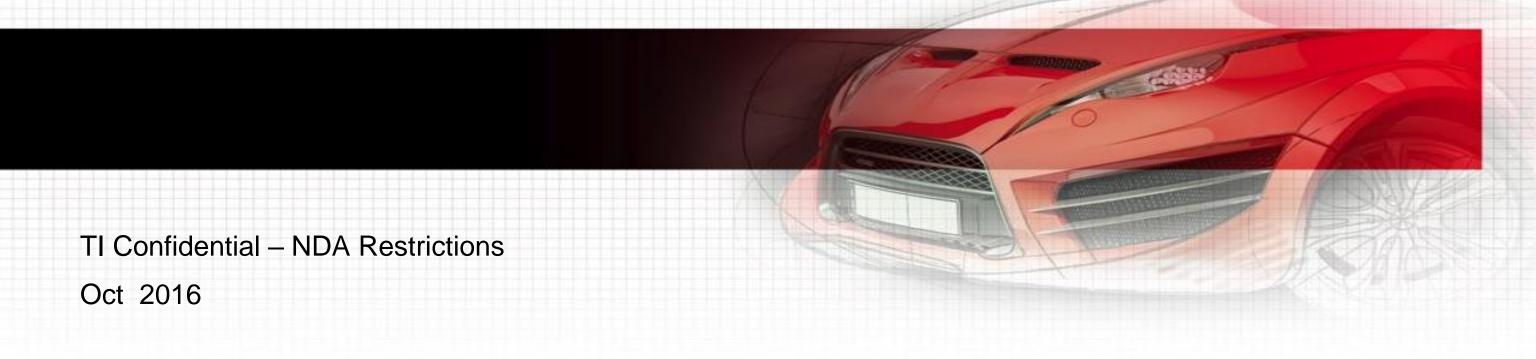
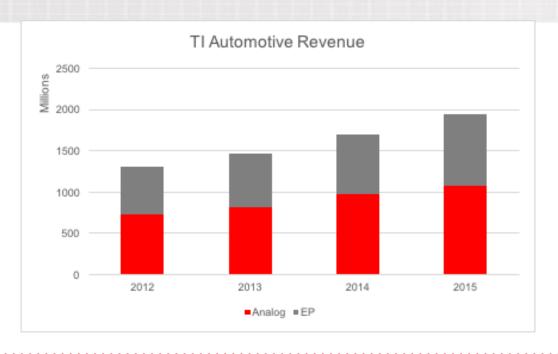
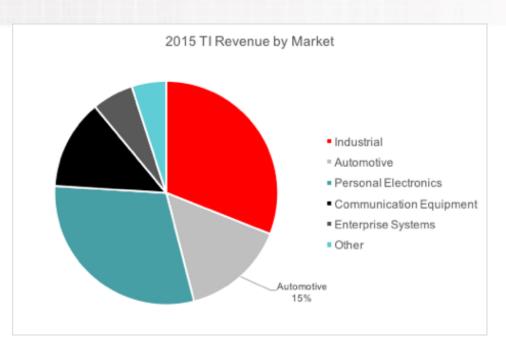
## **TI Automotive ADAS Processor Solutions**



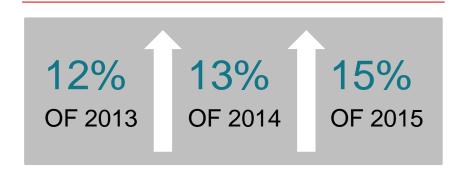
#### TI IS COMMITTED TO THE AUTOMOTIVE MARKET



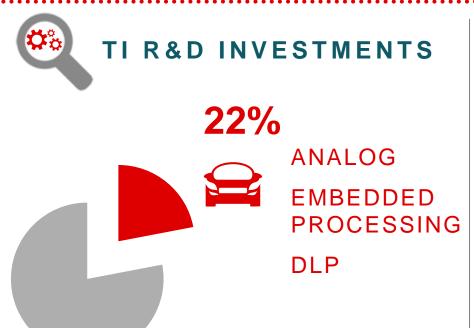
15% OF 2015 TOTAL REVENUE

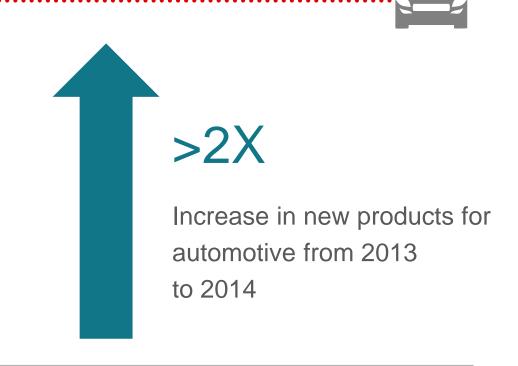


#### TI'S AUTOMOTIVE REVENUE IS:



TOTAL REVENUE







**ADAS SoC Business Unit** 



**Front Camera A**nalytics



Scalable HW Architecture

Common &

Software

Intelligent Park Assist **V**iewing



Intelligent **R**adar



ADAS Fusion

Vision SDK

Tier 1s (> 15)







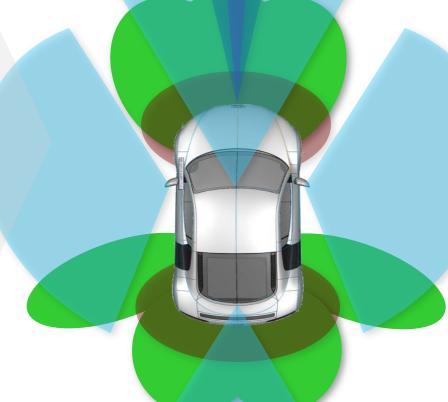


**ADAS Algorithms** 

**OEMs (> 25)** 

**Car Lines (> 100)** 

Up to 10 TI SoCs in on vehicle

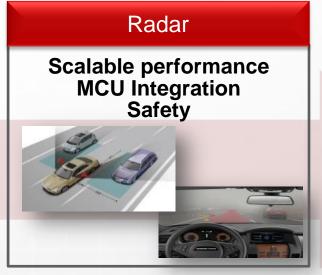


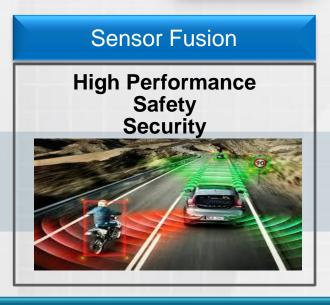
# **Target ADAS Applications**

# Scalable Performance Low Power Safety



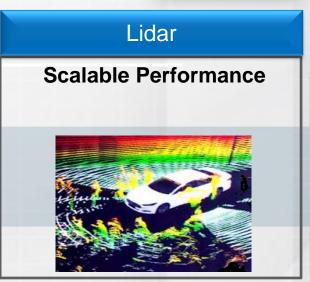










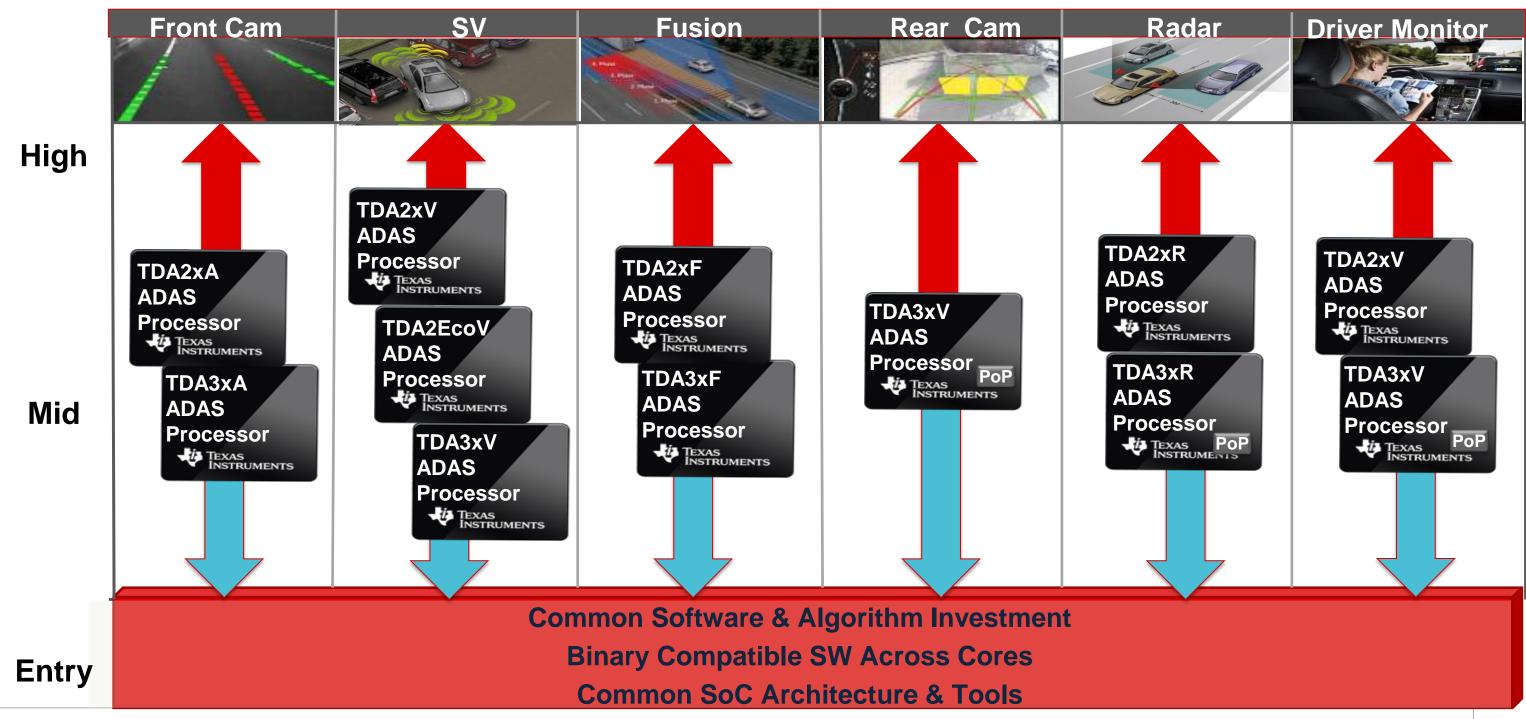


Scalable premium to entry performance solutions.

Fully programmable DSP, Vision Accelerators, and ARM cores.

Software Development Kits and Libraries provide easy portability between platforms.

## **Current Gen TDA Family Scalability**



## **ADAS Platform Evolution**

Specialized Accelerators

Imaging Accel

Multimedia Accel

**Graphics Accel** 

**Imaging Accel** 

Vision Accel

Multimedia Accel

**Graphics Accel** 

Programmable Signal Processing

**Control Code** 

Embedded Vision Engine (EVE)

C674x DSP

Embedded Vision Engine (EVE)

MMA/CNN (Matrix Multiplier)

C66x DSP

C7x DSP

C64x/C674x DSP

ARM® 32 bit

ARM® 32 bit

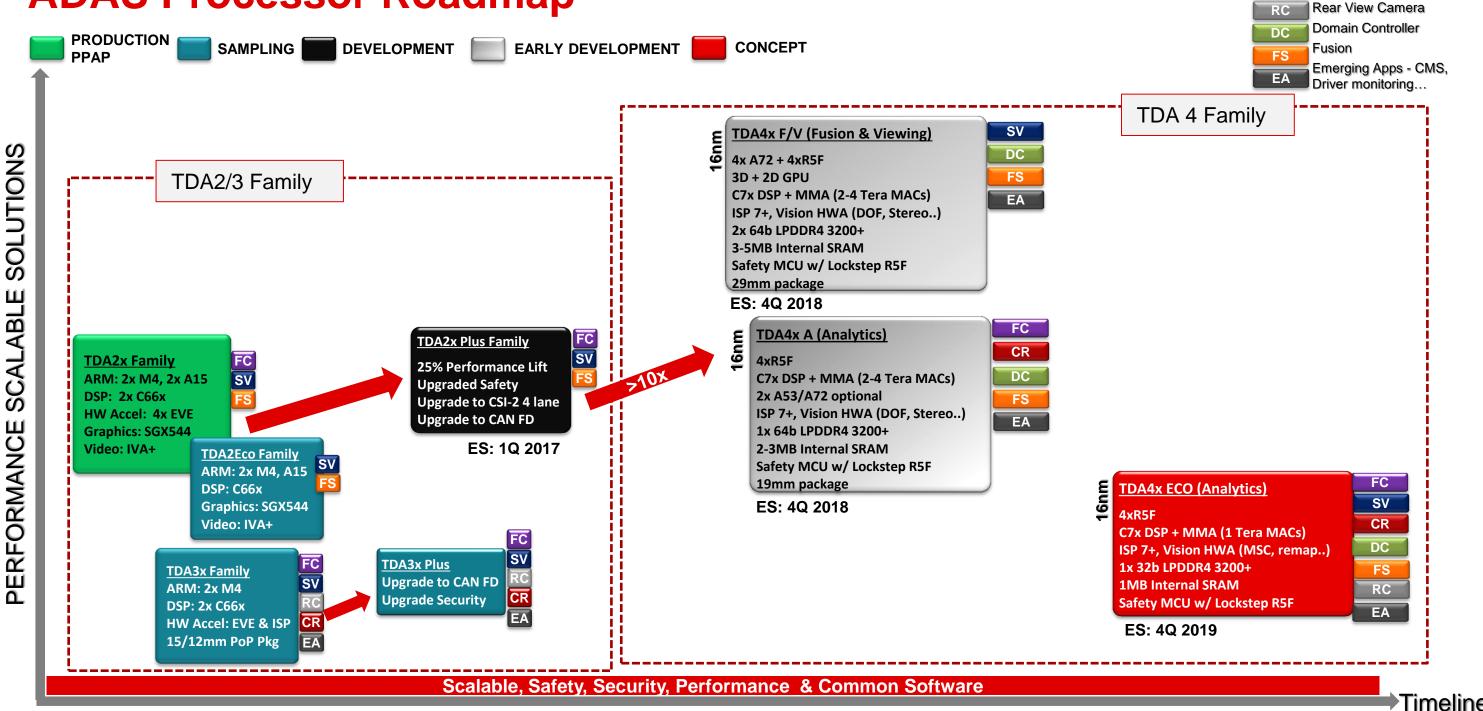
ARM® 32 bit

ARM® Cortex-M MCU ARM® 64 bit

ARM® Cortex-R Safety MCU

Generation	Gen 0/1	Gen 2	Gen 3	Gen 4
ASIL Enablement	А	В	В	С
Part Family	C67x/OMAPx/DMx	TDA1x	TDA2/3x	TDA4x

## **ADAS Processor Roadmap**



FC Front Camera

Surround View

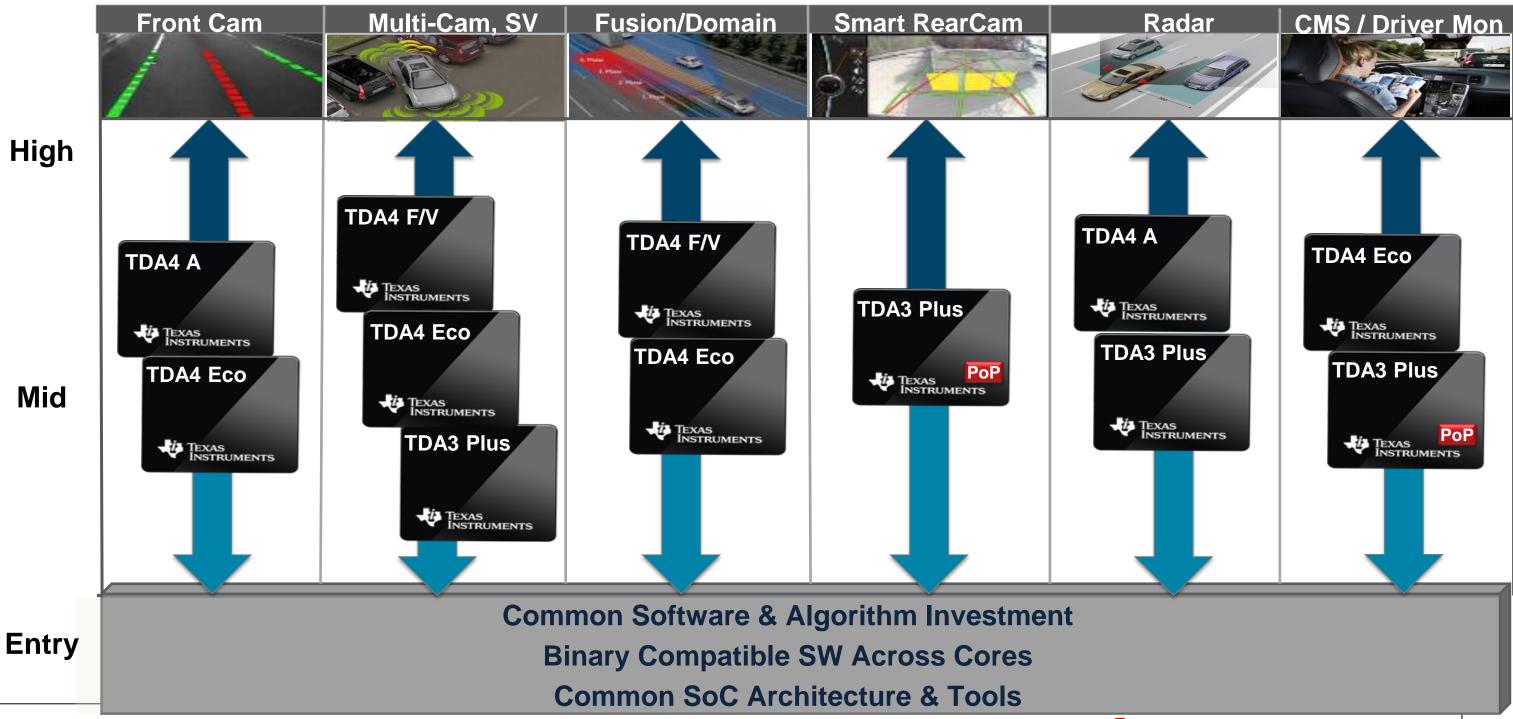
Central Radar

## **TDA4 Platform Snapshot**

CLUSTER	FEATURES	ENABLING
ARM CPU	50K DMIPs  4x Aux Cores  Lockstep SafeTI <sup>TM</sup> MCU	<ul><li>High performance Fusion DMIPS</li><li>Integrated Safe MCU</li></ul>
DSPs / Graphics	C66x+EVE -> C7000 DSP C700	<ul><li>Simplified SW Dev.</li><li>&gt;4 TeraMACs deep learning accelerator</li></ul>
Vision & Multimedia	REMAP MSC  ISP 7.x, Vision HWA  Multiple 2-4K display  Encode + Decode	<ul><li>&gt;10 2MP cameras at lowest BOM</li><li>Optimized Acceleration</li></ul>
High Speed IO	LP/DDR4  >50 Gbytes/s  PCI Supples USB 3.1  PCI Sup	<ul><li>Performance</li><li>System Flexibility</li><li>Switch integration</li></ul>
Security & Security	Enhanced Firewall Central Security & PWR Cryptos, security HWA	<ul> <li>V2V, V2X Security Ready</li> <li>Enhanced platform safety and FFI</li> </ul>
Software	ΔUT(Ø) SΔR ISO 26262	<ul><li>AutoSAR ready</li><li>ISO26262 development compliant</li></ul>



## **Next Gen Scalable TDA Family**



# Our strategy is to differentiate through...

#### Common & Scalable Platform

- Common Platform scaling from Entry, Mid to High
- Scalable compute using HyperLink™

#### Common Software

- Vision SDK baseline
- Dedicated Housekeeping MCU
- Dedicated Safety MCU w/ AUTOSAR

#### Efficient Vision Compute

- Right tradeoff of programmable vs. fixed acceleration
- Best power efficiency

#### Efficient Data Movement Architecture

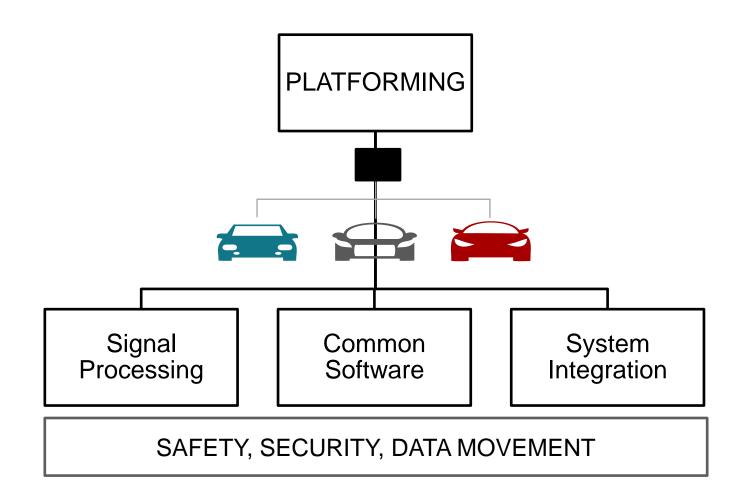
- Cache, Data & IO Coherency
- Data compression
- Streaming based architecture
- High bandwidth links with ultra low latency

#### Safety & Security

- Dedicated Safety MCU
- Dedicated Security & Device Management Processor
- Dedicated Security Accelerators

#### High System Integration

- On die. Extensive Analog Integration
- Next Gen PM Solutions
- Next Gen. Interfaces for Interprocessor communication & Chip to Chip connectivity



## **TI Vision**

Gen 2 - ADAS

**Gen 3 – Highly Autonomous Driving** 

**Gen 4 – Fully Autonomous Driving** 

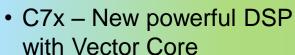






- DSP C66x
- Vision -EVE
- ISP Imaging HWA
- More cores
- C66x
- EVE
- C66x DSP
- EVE Vision coprocessor





- ISP Vision Optimized ISP
- DOF, Stereo
- MMA Powerful programmable Matrix Coprocessor optimized for CNN & other matrix operations
- High Security





- C7x plus Same architecture plus
- ISP plus enhancements & speed increase
- Vision HWA plus enhancements
  - DOF
  - Stereo
  - Other
- MMA Enhancements for more powerful CNN & Matrix operation processing
- Communication
- Bandwidth reductions & improvements

16nm FF provides 5-6X performance boost at same power

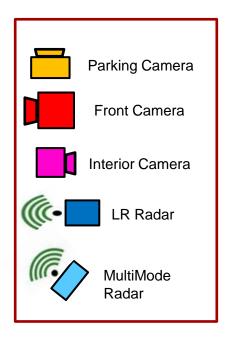
**ADAS** 

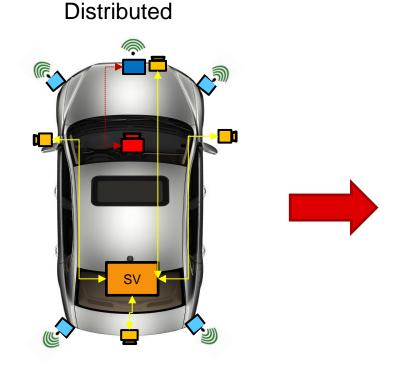
ADAS to Autonomous transition

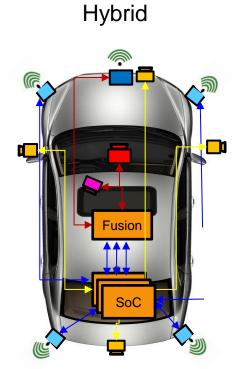
**Autonomous Driving** 



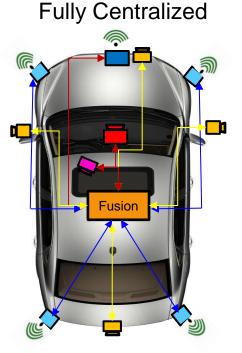
## **ADAS System Migrations**











#### **Distributed Systems**

- State of the art today
- Processing on the edge processor close to sensor
- · Easy to manage Clear ownership
- Power and size constraints

#### **Hybrid "Centralized" System**

- Hi speed transmission of RAW data to dedicated centralized processor node
- Aggregate common sensor nodes into Central Fusion ECU - Each processor node transmits object data to fusion ECU
- Easy to manage Clear ownership
- Easily Scalable
- Sensing Units can be very small
- · Processing Units Power & Size can be relaxed

#### **Full Centralized Processing**

- Very complex, expensive, and difficult to scale to lower cost vehicles (zFAS)
- Difficult to manage multi-vendor Collaboration on one chip
- Multiple vendor systems on one chip raises safety and responsibility issues

TI has extensive knowledge and market presence in each of these building blocks on a common HW & SW platform, allowing easy migration between system architectures.



# **Ecosystem - ADAS**









#### **TDA's Engineering Consultancy Partners**







**PATHPARTNER** 

#### **Graphics**

2D | 3D **IEXAS INSTRUMENTS** 





#### **ARM® Cortex®-A15**

**Graphics / HMI | Middleware | OS services** 











#### Auxiliary ARM® Cortex®-M4

**RTOS** 







Green Hills





#### C66x DSP/EVE





KPIT







#### **CODECs**



**TDAx SoC** 



#### **TDA Hardware Board Design**









# D3 Engineering – RVP

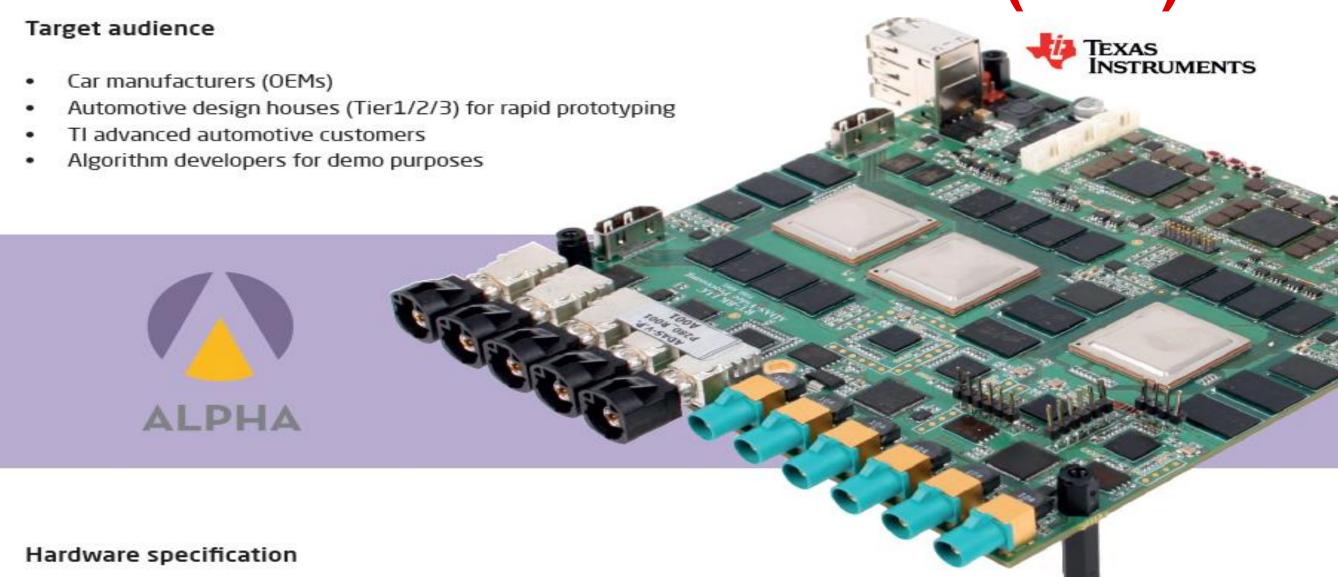
# TDAx Rugged Vision Platform



A fully functioning evaluation system speeds on-vehicle testing and development of multi-camera, real-time vision applications requiring intensive video analytics.

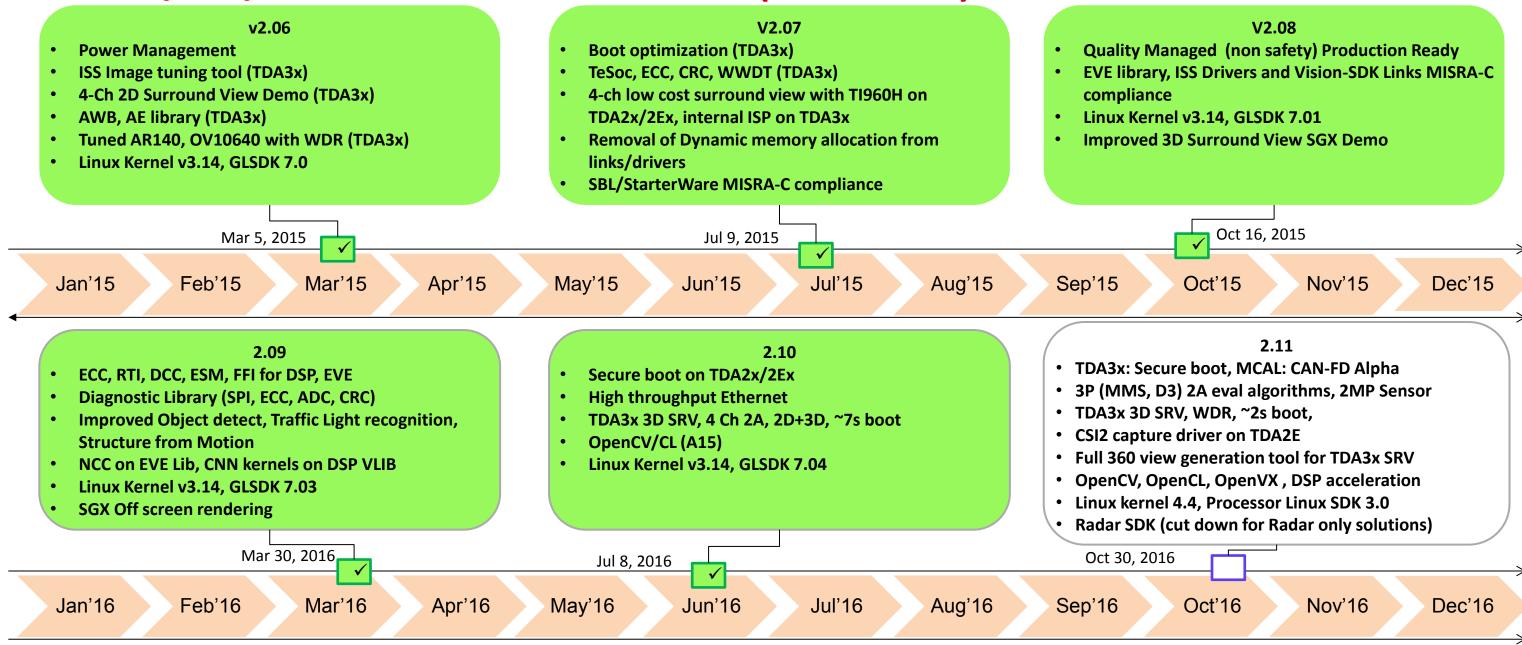


# RTRK Automotive Machine Vision (AMV)



Processors: 3 x TDA2x SoC (up to 2x ARM Cortex A15 and 2x ARM Cortex M4, 2x C66x Digital Signal Processor cores
(DSP), 4x Embedded vision Engine (EVE)).

### TDA2x/2Ex/3x - Processor SDK - Vision (Vision SDK) 2016 ROADMAP



# OpenCL, OpenVX and OpenCV

	OpenCL	OpenVX	OpenCV
Computer vision Library	NO	Yes	Yes
Defines a programming language	Yes	NO	NO
Defines an acceleration framework	Yes (Language based)	Yes (Graph based)	NO
Open standard API defined by Khronos	Yes	Yes	No (community driven open source)
Library Scope	NA	~43 vision kernels (v1.1) with user extension capability	~2500 vision and machine learning functions



# **OpenXX Availability from TI**

	OpenCL	OpenVX	OpenCV
Availability	Yes	VXLIB: Yes OpenVX API: TBD	Yes
Devices	TDA2x, AM57xx, DRA7xx & K2X	TDA2x, TDA3x, AM57xx, DRA7xx & K2X	TDA2x, AM57xx, DRA7xx & K2X
Comments	DSP exposed as generic OpenCL compute device  EVE will be exposed as custom device	OpenVX Kernels will be available on DSP (VXLIB)  OpenVX API: Under implementation	Avaialbity of modules on A15 and acceleration to EVE/DSP
Timelines	DSP (compute device): 3Q-2016  EVE (custom device): 1Q-2017	OpenVX Kernels on DSP (VXLIB): 3Q-2016 (Beta) 4Q-2016 (GA)	<ul> <li>A15</li> <li>Available</li> <li>DSP Acceleration</li> <li>4Q-2016(Beta)</li> <li>EVE Acceleration</li> <li>1Q-2017(Beta)</li> </ul>

