# Yuyang Wang

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## Appointments

**Columbia University in the City of New York** — New York, New York, USA
Postdoctoral Research Scientist, Columbia Nano Initiative — 2021–Present

## Education

**University of California, Santa Barbara** — Santa Barbara, California, USA
Ph.D. in Electrical and Computer Engineering — 2018–2021

**University of California, Santa Barbara** — Santa Barbara, California, USA
M.S. in Electrical and Computer Engineering — 2015–2018

**Tsinghua University** — Beijing, China
B.Eng. in Electronic Engineering — 2011–2015

## Publications

### Refereed Journal Papers

J1 A. James, A. Rizzo, **Y. Wang**, A. Novick, S. Wang, R. Parsons, K. Jang, M. Hattink, and K. Bergman, "Process Variation-Aware Compact Model of Strip Waveguides for Photonic Circuit Simulation," *Journal of Lightwave Technology*, vol. Early Access, pp. 1–14, 2023. doi 10.1109/JLT.2023.3238847.

J2 **Y. Wang**, P. Sun, J. Hulme, M. A. Seyedi, M. Fiorentino, R. G. Beausoleil, and K.-T. Cheng, "Energy Efficiency and Yield Optimization for Optical Interconnects via Transceiver Grouping," *Journal of Lightwave Technology*, vol. 39, no. 6, pp. 1567–1578, Mar. 2021. doi 10.1109/JLT.2020.3039489.

J3 Z. Zhang, R. Wu, **Y. Wang**, C. Zhang, E. J. Stanton, C. L. Schow, K.-T. Cheng, and J. E. Bowers, "Compact Modeling for Silicon Photonic Heterogeneously Integrated Circuits," *Journal of Lightwave Technology*, vol. 35, no. 14, pp. 2973–2980, Jul. 2017. doi 10.1109/JLT.2017.2706721.

Y.W.!

Y.W.: Aneek's JLT

### Refereed Conference Papers

C1 A. James, **Y. Wang**, A. Rizzo, and K. Bergman, "Flexible, Process-Aware Compact Model of Effective Index in Silicon Waveguides for Commercial Foundries," in *2022 International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD)*, Turin, Italy: IEEE, Sep. 2022, pp. 173–174. doi 10.1109/NUSOD54938.2022.9894784.

C2 **Y. Wang** and K.-T. Cheng, "Traffic-Adaptive Power Reconfiguration for Energy-Efficient and Energy-Proportional Optical Interconnects," in *2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, Munich, Germany: IEEE, Nov. 2021, pp. 1–9. doi 10.1109/ICCAD51958.2021.9643475.

C3 **Y. Wang**, J. Hulme, P. Sun, M. Jain, M. A. Seyedi, M. Fiorentino, R. G. Beausoleil, and K.-T. Cheng, "Characterization and Applications of Spatial Variation Models for Silicon Microring-Based Optical Transceivers," in *2020 57th ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, USA: IEEE, Jul. 2020, pp. 1–6. doi 10.1109/DAC18072.2020.9218608.

C4 **Y. Wang** and K.-T. Cheng, "Task Mapping-Assisted Laser Power Scaling for Optical Network-on-Chips," in *2019 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Westminster, CO, USA: IEEE, Nov. 2019, pp. 1–6. doi 10.1109/ICCAD45719.2019.8942146.

C5 **Y. Wang**, M. A. Seyedi, J. Hulme, M. Fiorentino, R. G. Beausoleil, and K.-T. Cheng, "Bidirectional tuning of microring-based silicon photonic transceivers for optimal energy efficiency," in *Proceedings of the 24th Asia and South Pacific Design Automation Conference*, Tokyo Japan: ACM, Jan. 2019, pp. 370–375. doi 10.1145/3287624.3287649.

C6 **Y. Wang**, M. A. Seyedi, R. Wu, J. Hulme, M. Fiorentino, R. G. Beausoleil, and K.-T. Cheng, "Energy-efficient channel alignment of DWDM silicon photonic transceivers," in *2018 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Dresden, Germany: IEEE, Mar. 2018, pp. 601–604. doi 10.23919/DATE.2018.8342079.

C7 R. Wu, M. A. Seyedi, **Y. Wang**, J. Hulme, M. Fiorentino, R. G. Beausoleil, and K.-T. Cheng, "Pairing of microring-based silicon photonic transceivers for tuning power optimization," in *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*, Jeju: IEEE, Jan. 2018, pp. 135–140. doi 10.1109/ASPDAC.2018.8297295.

C8 R. Wu, **Y. Wang**, Z. Zhang, C. Zhang, C. L. Schow, J. E. Bowers, and K.-T. Cheng, "Compact modeling and circuit-level simulation of silicon nanophotonic interconnects," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017*, Lausanne, Switzerland: IEEE, Mar. 2017, pp. 602–605. doi 10.23919/DATE.2017.7927057.

C9 A. Ghofrani, M. A. Lastras-Montaño, **Y. Wang**, and K.-T. Cheng, "In-place Repair for Resistive Memories Utilizing Complementary Resistive Switches," in *Proceedings of the 2016 International Symposium on Low Power Electronics and Design*, San Francisco Airport CA USA: ACM, Aug. 2016, pp. 350–355. doi 10.1145/2934583.2934590.

C10 C. Xu, F. X. Lin, **Y. Wang**, and L. Zhong, "Automated OS-level Device Runtime Power Management," in *Proceedings of the Twentieth International Conference on Architectural Support for Programming Languages and Operating Systems*, Istanbul Turkey: ACM, Mar. 2015, pp. 239–252. doi 10.1145/2694344.2694360.

Y.W.!

Y.W.: OFC'23 papers, George's paper

**Invited Conference Papers**

IC1 **Y. Wang**, L. Shao, M. A. Lastras-Montano, and K.-T. Cheng, "Taming Emerging Devices' Variation and Reliability Challenges with Architectural and System Solutions [Invited]," in *2019 IEEE 32nd International Conference on Microelectronic Test Structures (ICMTS)*, Kita-Kyushu City, Fukuoka, Japan: IEEE, Mar. 2019, pp. 90–95. doi 10.1109/ICMTS.2019.8730924.

Y.W.!

Y.W.: SPIE Photonics West invited

Y.W.!

Y.W.: Book chapter, invited journal

## Talks and Presentations

- Ph.D. Forum at the 57th **ACM/IEEE Design Automation Conference (DAC)**, online virtual event — Jun. 2020
  *Design and Optimization of Variation-Aware Runtime-Reconfigurable Optical Interconnects*
- Invited talk at the 4th **Optical/Photonic Interconnects for Computing Systems (OPTICS) workshop**, Dresden, Germany — Mar. 2018
  *Optimal Pairing and Non-Uniform Channel Alignment of Microring-based Transceivers for Comb Laser-Driven DWDM Silicon Photonics*
- Invited talk at the **ECE Departmental Seminar**, Hong Kong University of Science and Technology — Jan. 2018
  *Variation-Aware Modeling and Design of Silicon Photonic Systems*

## Activities

- **Teaching Assistant** at the University of California, Santa Barbara

  ECE 153B: Sensor & Peripheral Interface Design — Winter 2019
- **Reviewer** of refereed journals — 2018–Present
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, IEEE Access.
- **Textbook Translation**

T1 C. Hawkins, J. Segura, and P. Zarkesh-Ha, *CMOS Digital Integrated Circuits: A First Course (Chinese Edition)*, trans. by **Y. Wang** and Y. Yin. China Machine Press, 2016, original work published by the Institution of Engineering and Technology (IET) in 2013.

T2 S. Kundu and A. Sreedhar, *Nanoscale CMOS VLSI Circuits: Design for Manufacturability (Chinese Edition)*, trans. by **Y. Wang** and W. Xie. China Science Publishing, 2014, original work published by McGraw-Hill Education in 2010.

## References

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