Opening: Thank you for your kind introduction. What I’ll talk about today is how I use integrated silicon photonics technology to transform today’s and future data communication and computing systems.

1. Grand challenge: 5.5 minutes
   1. Moore’s Law is slowing down, but computational growth is not.
      1. AI model growth
      2. Long-distance communication unavoidable
   2. What if unaddressed?
      1. Energy growth (comparison to NYC electricity), and 3 months to train
      2. Example application affected
   3. What exactly should be addressed?
      1. Communication bottleneck – system-wide bandwidth discrepancy
2. My approach: bring photonics into the computing socket 5 minutes
   1. What is the approach and how is it different from existing?
      1. In today’s solution this distance is long, and driven fast
      2. My approach reduces distance between electronic and photonic interface
   2. What system-level impact?
   3. Significance of my approach and key factors to improvement
      1. 100x over state-of-the-art
      2. Moderate data rate per channel
      3. More parallel channels!
3. How to pack more channels? 7.5 minutes
   1. Resonator-based DWDM basics
   2. Enabling more channels:
      1. Kerr comb
      2. Scalable architecture
   3. 64 channel link design
      1. Link design walk-through, Tb/s per fiber calculation
      2. Multi-FSR channel arrangement
   4. Link validation
4. How to get the density? 4 minutes
   1. 2.5D/3D integration (best nodes for E and O, no change to computing chip)
   2. 3D integration, co-design
5. Variation management and link control 5 minutes
   1. Flat-top interleaver
   2. Interleaver control
   3. Disk vs. ring
   4. Link initialization
6. Now let’s talk about energy 5 minutes
   1. Link budget and energy calculation
   2. Go back to the FOM, can we further scale?
      1. 32 Gb/s disks at low Vpp, 4x32 transceiver
   3. What system implication? (Ref. system work, more in backup slides)
7. My other work extending this approach: use photonics for computing 5 minutes
   1. What does the system look like
   2. Why do I want to do computing within data movement
   3. How does the system work
8. Computation continues to scale, but energy brought down by ~100x
9. Future directions 5 minutes
   1. Photonics for RF
   2. 3D photonics

45 minutes

Backup slides:

300mm photonic wafer runs

128 channel and 4x32 architecture, layout for 10Tbps/mm (NAPMP)

On-chip comb (NAPMP)

Full link simulation

16/32 Gbps eyes

System reconfiguration

FWM broadcasting and switching

Silicon photonics needs diversity