Silicon Photonics Chip I/O for Ultra High-Bandwidth and Energy-Efficient Die-to-Die Connectivity

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In this paper, we present the design and characterization of a groundbreaking Kerr comb–driven silicon photonics DWDM transceiver chip, which offers a scalable architecture for ultra-high bandwidth and energy-efficient die-to-die connectivity. Our results demonstrate the feasibility of achieving a chip shoreline bandwidth density of over 2 Tbps with a sub-pJ/b energy consumption, which is significant in the context of exponentially growing traffic demands in data centers and high-performance computing systems. The multi-FSR regime adopted in this work enables the utilization of microresonators with moderate FSR for ultra-broadband DWDM with minimal crosstalk penalties. The preliminary characterization of crucial components such as the even-odd (de-)interleavers and microresonator modulators and filters has laid the groundwork for subsequent system-wide validations.

For future work, we aim to further enhance the modulator and filter designs to substantially boost the chip escape bandwidth. Link-level demonstrations will be carried out to validate the transceiver's performance systematically. With a focus on mitigating the impact of process variations and maximizing energy efficiency, future designs will also look into improving the effectiveness of wafer-scale thermal undercuts and adopting fabrication-robust device designs. The progress made in this study is a key step towards realizing the vision of seamlessly integrated photonics and electronics in future computing systems.