# COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

COLUMBIA NANO INITIATIVE

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Faculty Search Committee
Elmore Family School of Electrical and Computer Engineering
Purdue University
MSEE Building
501 Northwestern Avenue
West Lafayette, IN 47907-2045

Dear Members of the Faculty Search Committee,

Re: Application for the Tenure-Track Assistant Professor Position

I am writing in response to the advertised faculty position (**Tenure-Track Assistant Professor—Job # 28412**) in the Elmore Family School of Electrical and Computer Engineering at the Purdue University. I am currently a Postdoctoral Research Scientist at the Columbia Nano Initiative of the Columbia University under the mentorship of Prof. Keren Bergman. My Ph.D. in Electrical and Computer Engineering was awarded by the University of California, Santa Barbara in 2021, where I was co-advised by Prof. Kwang-Ting Cheng and Prof. John E. Bowers. My research portfolio, which is both diverse and synergistic, focuses on silicon photonics (SiPh) optical interconnects, with significant implications for the broad area of electrical engineering, particularly nanophotonics, optical communication, and design automation. I believe that my interdisciplinary research background positions me well to contribute to your department's ongoing excellence.

The prevalence of communication bottleneck in the era of data ubiquity—emerged in modern distributed computing infrastructures and exacerbated by the pervasiveness of data-intensive AI/machine learning applications—drives my research that seeks **transformative connectivity solutions** for future system scalability. I aim to cultivate the potential of CMOS-compatible silicon photonics to develop ultra high-bandwidth and energy-efficient optical interconnects. Building upon a unique link architecture that facilitates unprecedented channel parallelism, I envision system-level breakthroughs that boost the density, adaptability, and functionalities of optical interconnects amidst the ever-evolving data landscape.

My Ph.D. research laid the groundwork for this vision, **vertically integrating design enablement technologies** for integrated silicon photonics across device, circuit, and system levels, including modeling, simulation, and variation mitigation techniques to democratize the design of yield- and performance-optimized SiPh devices and circuits. The research resulted in publications at leading design automation conferences like DAC and ICCAD, esteemed photonics venues like OFC and JLT, and a book chapter in press with Springer, bridging electronics and photonics research communities.

Orthogonally expanding on my Ph.D. work, my postdoctoral work at the Columbia University focuses on the design and implementation of massively scalable SiPh chip I/Os, **horizontally integrating optimization techniques** across the entire design cycle, from chip layout to post-fabrication tuning and runtime reconfiguration. I spearheaded two generations of the SiPh transceiver chips—co-designed with both academia and industry partners for 3D-integrated electronic drivers and advanced packaging—integrating over 2,000 microresonators into an 8 mm × 8 mm footprint to achieve 16 Tbps chip I/O bandwidth with sub-pJ/b energy consumption. The featured link architecture played a pivotal role in securing a $35M SRC JUMP 2.0 grant involving 23 principal investigators, to which I have contributed through

proposal writing and ongoing research efforts. An invited paper detailing the chip's design and characterization is currently under review for CICC 2024, and a manuscript focusing on the end-to-end link demonstration is slated for an invited submission to *Nature Communications Physics*.

Moving forward, I anticipate an even more diverse and dynamic data landscape, shaped by the growing heterogeneity of computing applications. Emerging privacy-focused frameworks such as federated learning emphasize the exchange of models over data, which—coinciding with the expansion of large models like GPTs—further pushes the system bottleneck from computation to communication capabilities. This shift necessitates the next generation of **reconfigurable system connectivity** that can adapt on-demand to varying traffic needs while maintaining high bandwidth and energy efficiency. My foundation work in system reconfiguration techniques, built upon the scalable link architecture, will be the cornerstone of my ongoing research endeavor to equip future computing infrastructures for the ever-evolving data context.

I also foresee opportunities arising from a deeper integration of silicon photonics within computing sockets, a direction that my postdoctoral research is actively pursuing. Anticipating advances in dense 3D optical I/Os—a concept that I helped formulate for showcasing at the 2023 DARPA ERI Summit—I envision **innovative system architectures** that leverage the manifolded reach of on-board optical links. This approach could eliminate the reliance on silicon interposers, currently nearing their performance limits, and surpass the density constraints of conventional fiber optics, thus catalyzing new computational paradigms and interconnect functionalities with redefined chip-to-chip connectivity.

My research agenda is situated at the system level, deeply engaged with the interdisciplinary nexus of electronics/photonics, devices/systems, and design/applications. I am excited about the prospect of collaborating with the diverse faculty at the Purdue University, who are leading in areas such as *nanophotonics* (Peter Bermel, Alexandra Boltasseva, Minghao Qi), *post-CMOS technologies and integration* (Kaushik Roy, Saeed Mohammadi, Haitong Li), *computer architectures and systems* (Yi Ding, Timothy Rogers, Vishal Shrivastav), and *networking and distributed machine learning* (Christopher Brinton, Abolfazl Hashemi, Y. Charlie Hu), to tackle the grand challenge of revolutionizing connectivity in future computing infrastructures across the full system stack.

My training in California and New York has enriched me with diverse and inclusive academic experiences, fueling my passion to contribute to the Purdue University's community through not only research, but also teaching, mentoring, and outreach. As a teaching assistant and guest lecturer, I have taught at both undergraduate and graduate levels, focusing my teaching philosophy on the balance of engagement, conveyance, and inspiration through visualization. I also value the role of mentoring in fostering students' intellectual growth beyond technical skills and have actively mentored students tailored to their research interests and career aspirations. My advocacy for diversity and inclusion is reflected in my experiences of working with—as well as my efforts to promote the accessibility of STEM education to—underrepresented groups in my endeavors.

I am enthusiastic about joining the Elmore Family School of Electrical and Computer Engineering at the Purdue University to further its excellence in research and education. Enclosed are my application materials, and I am glad to provide additional information if required. I look forward to the possibility of discussing my qualifications and research vision with you. Thank you for considering my application, and I anticipate your response.

Yours sincerely,

Yuyang Wang

encl: Curriculum Vitae
Research Statement
Teaching Statement