

# **Energy Efficiency and Yield Optimization for Optical Interconnects via Transceiver Grouping**

Yuyang Wang, Peng Sun, Jared Hulme, M. Ashkan Seyedi, Marco Fiorentino, Raymond G. Beausoleil, and Kwang-Ting Cheng

JOURNAL OF LIGHTWAVE TECHNOLOGY, VOL. 39, NO. 6, MARCH 15, 2021

In this study, we target the application scenario where fabricated microring-based transceivers are grouped for assembling optical networks of multiple nodes. We propose two algorithms to mix and match the fabricated transceivers so that the three optimization objectives, namely the average energy efficiency, the uniformity, and the yield of the networks assembled, are optimized. We evaluated our proposed algorithms by wafer-scale measurement data of microring-based transceivers, as well as synthetic data generated based on an experimentally validated variation model. Our first algorithm based on simulated annealing (SA) can achieve up to 25% improvement in the average energy efficiency of the networks assembled, up to 94% reduction of the standard deviation of the energy efficiency, and up to 75 percentage points increase of the network yield, compared to a baseline strategy that randomly groups the transceivers. Moreover, our second algorithm based on Pareto simulated annealing (PSA) can efficiently produce multiple Pareto-optimal grouping schemes that significantly outperform the random grouping scheme in all three optimization objectives, namely the energy efficiency, the uniformity, and the yield of the networks assembled.

Incorporating data from wafer-scale measurement ensures that the optimization algorithms are tailored to actual conditions, leading to more reliable and applicable results. The enhanced accuracy and reliability of the models, informed by real process variation data and detailed in another paper of mine, are essential for predicting the performance of optical networks under varying manufacturing conditions. This ensures that the optimization strategies are both robust and relevant to real-world applications. Furthermore, this study emphasizes a top-down, application-driven method for design optimization of optical interconnects. This approach is particularly significant as it addresses the practical challenges in deploying optical interconnects, focusing on end goals like energy efficiency, uniformity, and yield.

# Energy Efficiency and Yield Optimization for Optical Interconnects via Transceiver Grouping

Yuyang Wang<sup>1</sup>, Peng Sun<sup>1</sup>, Jared Hulme, M. Ashkan Seyedi, Marco Fiorentino<sup>2</sup>, *Senior Member, OSA*,  
Raymond G. Beausoleil, *Fellow, OSA*, and Kwang-Ting Cheng<sup>3</sup>, *Fellow, IEEE*

**Abstract**—Optical interconnects enabled by silicon microring-based transceivers offer great potential for short-reach data communication in future high-performance computing systems. However, microring resonators are prone to process variations that harm both the energy efficiency and the yield of the fabricated transceivers. Especially in the application scenario where a batch of transceivers are fabricated for assembling multiple optical networks, how the transceivers are mixed and matched can directly impact the average energy efficiency and the yield of the networks assembled. In this study, we propose *transceiver grouping* for assembling communication networks from a pool of fabricated transceivers, aiming to optimize the network energy efficiency and the yield. We evaluated our grouping algorithms by wafer-scale measurement data of microring-based transceivers, as well as synthetic data generated based on an experimentally validated variation model. Our experimental results demonstrate that optimized grouping achieves significant improvement in the network energy efficiency and the yield across a wide range of network configurations, compared to a baseline strategy that randomly groups the transceivers.

**Index Terms**—Energy efficiency, microring-based transceiver, multi-objective optimization, optical interconnects, silicon photonics, simulated annealing, yield optimization.

## I. INTRODUCTION

**O**PTICAL interconnects are promising alternatives to electrical ones in modern high-performance computing (HPC) systems to accommodate traffic-intensive applications [1]. Silicon photonics has emerged as a scalable and cost-effective enabler of the optical interconnects by taking advantage of a CMOS-compatible fabrication process [2]. Silicon microring-based optical transceivers (TRx) are one of the most popular implementations that achieve dense wavelength-division

multiplexing (DWDM) with a compact footprint [3], [4]. Various conceptual designs and prototypes of optical network-on-chips (ONoC) have been reported [5]–[7] to leverage a microring-based architecture.

Despite great potential demonstrated, silicon microrings often suffer from significant process variations due to fabrication imperfection. As a result, the optical links and networks comprising these imperfect devices must be actively tuned to compensate for the process variations, for which the tuning power is non-trivial [8]. The variation issues become more prominent in the application scenario where a batch of transceivers are fabricated for assembling multiple optical networks. Specifically, some transceivers with straggling variation magnitudes may produce networks that either

- 1) demand excessive power for variation compensation or
- 2) fail to support a target data rate,

thus worsening the average energy efficiency, the product uniformity, and the yield of the networks assembled. Nevertheless, network-level variation alleviation techniques that exploit wafer-scale fabrication of microring-based transceivers have been lacking. Techniques based on channel shuffling [9], [10] and sub-channel redundancies [11]–[13] were proposed to reduce the expected power for thermally tuning the resonance wavelengths of the microrings. A hybrid strategy employing both thermal and electrical tuning was proposed in [14]. However, these techniques are limited to the link-level, rather than the network-level, and only target a single pair of transmitter (Tx) and receiver (Rx). Considering wafer-scale fabrication, an optimal pairing scheme for a batch of fabricated transceivers could further reduce the average tuning power required for pairs formed from the batch [15]. Nevertheless, all of the above techniques are restricted to the mitigation of the wavelength tuning power, while the overall energy efficiency and the yield of the transceivers are also impacted by the variations of other parameters, such as the extinction ratios and the quality factors of the microrings. Moreover, none have encompassed the application scenario where the fabricated transceivers are used for assembling communication networks of multiple nodes.

We observed from wafer-scale measurement data of microring-based transceivers that, due to the distinct variation profile of each transceiver, optical networks assembled from different transceivers will have different energy efficiency. Therefore, when a batch of fabricated transceivers are available for assembling several networks, there is an opportunity to group the transceivers in a way that the average energy efficiency of the

Manuscript received September 14, 2020; revised November 5, 2020; accepted November 15, 2020. Date of publication November 20, 2020; date of current version March 16, 2021. This work was partially supported by RGC of the Hong Kong SAR, China under a GRF Grant HKUST 16207918. (*Corresponding author: Yuyang Wang.*)

Yuyang Wang is with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA (e-mail: ywy@ece.ucsb.edu).

Peng Sun, Jared Hulme, M. Ashkan Seyedi, Marco Fiorentino, and Raymond G. Beausoleil are with Hewlett Packard Labs, Hewlett Packard Enterprise, Palo Alto, CA 94304 USA (e-mail: psun@hpe.com; jared.hulme@hpe.com; ashkan.seyedi@hpe.com; marco.fiorentino@hpe.com; ray.beausoleil@hpe.com).

Kwang-Ting Cheng is with the School of Engineering, Hong Kong University of Science and Technology, Kowloon, Hong Kong (e-mail: timcheng@ust.hk).

Color versions of one or more of the figures in this article are available at <https://doi.org/10.1109/JLT.2020.3039489>.

Digital Object Identifier 10.1109/JLT.2020.3039489

networks assembled is optimized. Meanwhile, it is also desirable, from the perspective of quality control, that the energy efficiency of the networks assembled is uniform. Moreover, some networks assembled may fail to support a target data rate, thus lowering the yield. Therefore, the grouping of the transceivers should also be optimized for the objective of meeting the target data rate. In this study, we propose *transceiver grouping* which mixes and matches a pool of fabricated transceivers to assemble networks of equal size, aiming to optimize the average energy efficiency, the uniformity, and the yield of the networks assembled.

We designed two algorithms inspired by simulated annealing to address this multi-objective optimization problem. The proposed algorithms were evaluated by wafer-scale measurement data of microring-based transceivers, as well as synthetic data generated based on an experimentally validated variation model. Our experimental results demonstrate that the proposed grouping algorithms achieve significant improvement in all three objectives, namely the average energy efficiency, the uniformity, and the yield of the networks assembled, compared to a baseline strategy that randomly groups the transceivers.

The rest of the paper is organized as follows. In Section II, we review the background of this study and some related work. In Section III, we formulate transceiver grouping as an optimization problem and present our algorithms. In Section IV, we elaborate the measurement and the synthetic data of microring-based transceivers for evaluating our algorithms. We also introduce the power models of the optical devices used in our simulations. In Section V, we evaluate our grouping algorithms for a wide range of network configurations. Finally, in Section VI, we draw the conclusion of this study.

## II. BACKGROUND AND RELATED WORK

### A. Microring-Based Optical Interconnects

An optical network is a collection of optical links that provides data communication among processing nodes. Fig. 1 illustrates an exemplar architecture of an optical network with a generic ring topology [5], where silicon microring-based transceivers are utilized to send and receive optical signals at each node. A silicon microring resonator is a highly wavelength-selective device [16], whose transmission spectrum can be characterized by a Lorentzian function:

$$T(\lambda) = 1 - \frac{1 - 1/ER}{1 + (2Q \cdot (\lambda - \lambda_r)/\lambda_r)^2}, \quad (1)$$

where  $\lambda_r$ ,  $ER$ , and  $Q$  are the resonance wavelength, the extinction ratio, and the quality factor of the microring. A microring-based transceiver, as shown in Fig. 1, achieves DWDM by deploying cascaded microring resonators along a shared waveguide. At the Tx side, applying voltages to the microring modulators can slightly shift their resonance wavelengths to perform on-off keying (OOK) modulation of the optical signal. At the Rx side, corresponding microring filters can couple the signal out for detection. The overall transmission spectrum of a Tx/Rx

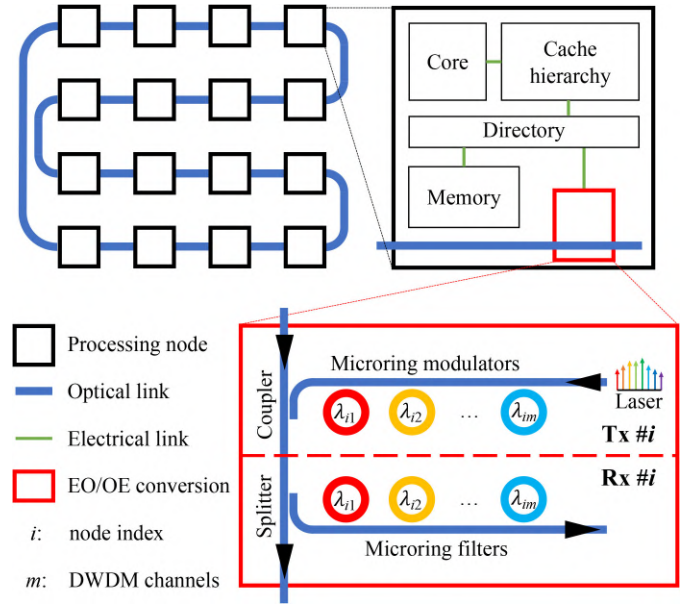


Fig. 1. Illustration of an optical network with a ring topology.

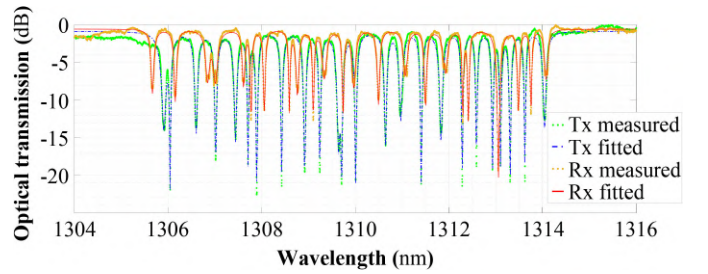


Fig. 2. Measured and fitted transmission spectra of a 24-channel transceiver.

can thus be modeled as

$$T_m(\lambda) = \prod_{i=1}^m \left( 1 - \frac{1 - 1/ER_i}{1 + (2Q_i \cdot (\lambda - \lambda_{r,i})/\lambda_{r,i})^2} \right), \quad (2)$$

where  $m$  is the number of DWDM channels. The cascaded microrings of a Tx/Rx are usually designed with incremental radii to provide a set of evenly-spaced resonance dips. However, as shown in Fig. 2, the fabricated transceivers often suffer from significant process variations that manifest themselves as the deviation of  $\lambda_r$ ,  $ER$ , and  $Q$  from their design values.

### B. Impact of Process Variations on Energy Efficiency

The energy efficiency of an optical network largely depends on the energy efficiency of the links it comprises, which, in turn, is impacted by the process variations of the microrings. First of all, the resonance wavelengths of the Tx/Rx must be tuned and aligned to a mutual set of carrier wavelengths. Besides, the variations of  $ER$  and  $Q$  affect the loss and the crosstalk noise within the optical channel, which must be compensated by an increased laser power to maintain a target data rate. As the variation magnitudes are different from device to device, optical networks comprising different transceivers will have

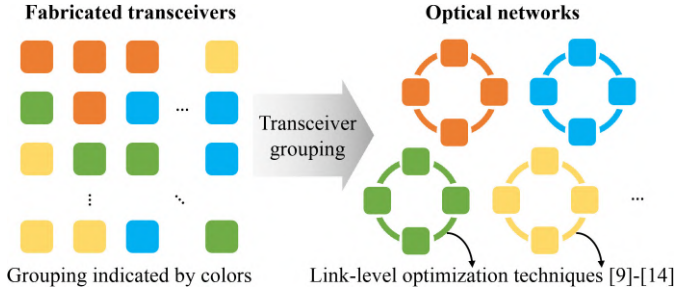


Fig. 3. Illustration of transceiver grouping and its relationship with existing link-level optimization techniques [9]–[14].

different energy efficiency. Therefore, when a batch of fabricated transceivers are available for assembling such networks, how the transceivers are grouped can directly impact the energy efficiency of each network assembled.

### C. Optimization Objectives for Transceiver Grouping

In this study, we focus on the application scenario where a pool of fabricated transceivers are grouped to assemble several optical networks, as shown in Fig. 3. We assume the networks to be assembled are of a multiple-reader-multiple-writer (MWMR) architecture. For networks of different architectures, our proposed approach would still apply except that some specifics need to be adjusted. As illustrated in Fig. 1, each network node in MWMR has both write and read access to the optical ring bus achieved by its Tx and Rx, respectively. With a proper arbitration scheme [17], any two nodes can establish point-to-point communication without the need for relay nodes. Based on this assumption, we propose the following optimization objectives for transceiver grouping.

1) *Energy Efficiency*: We propose to optimize the average energy efficiency of the networks assembled. We first quantify the energy efficiency of an optical link as its power consumption divided by its data rate. Measured in pJ/b, the smaller the value, the better the energy efficiency. Now, consider a total of  $N$  transceivers to be grouped into  $G$  networks, each with  $n$  nodes ( $G \leq N/n$ ). The energy efficiency of a network is thus a weighted sum of the energy efficiency of all its links:

$$e = \sum_{i=1}^n \sum_{\substack{j=1 \\ j \neq i}}^n p_{ij} \cdot \epsilon_{ij}, \quad (3)$$

where  $\epsilon_{ij}$  is the energy efficiency of the unidirectional link from Tx # $i$  to Rx # $j$  (hereafter *link* ( $i, j$ )), and  $p_{ij}$  is the portion of the network traffic carried out by this link. The average energy efficiency of all networks assembled is thus

$$E = \frac{1}{G} \sum_{g=1}^G e_g = \frac{1}{G} \sum_{g=1}^G \left( \sum_{i=1}^n \sum_{\substack{j=1 \\ j \neq i}}^n p_{ij} \cdot \epsilon_{g,ij} \right), \quad (4)$$

where  $\epsilon_{g,ij}$  denotes the energy efficiency of link ( $i, j$ ) in the  $g$ th network.

For a specific application,  $p_{ij}$  can be recorded by executing the application within a network simulator [18], [19] and can be different for each link. However, in this study, we assume that the network traffic results from the execution of various applications and is uniformly distributed to each link. Therefore,  $p_{ij}$  is considered identical for all links.

Note that the microring tuning schemes proposed in [9]–[14] are dedicated to improving  $\epsilon_{ij}$  of a specific link, as shown in Fig. 3. However, regardless of which technique adopted at the link level, we can always apply transceiver grouping to further optimize the average energy efficiency of the networks.

2) *Product Uniformity*: Product uniformity is another victim of the process variations, as the energy efficiency can be vastly different for each network assembled. The authors of [20] suggest binning, a widely adopted technique after the testing stage, to categorize the transceivers based on the variation magnitudes. However, different bins may end up having different performance specifications, such as the maximum data rate. On the contrary, our transceiver grouping can improve the uniformity of the energy efficiency of the networks assembled without compromising the target data rate, thus delivering products with similar performance specifications. Specifically, we propose to reduce the standard deviation of the energy efficiency across the networks assembled:

$$\sigma = \sqrt{\frac{1}{G} \sum_{g=1}^G (e_g - E)^2}, \quad (5)$$

where all networks still target the same data rate. The transceiver pairing technique proposed in [15] is a special case of our transceiver grouping with  $n = 2$ . However, our study accounts for the overall energy efficiency for communication, in contrast to [15] that only targets the microring tuning power. Moreover, we further introduce a third optimization objective for transceiver grouping, i.e., the network yield.

3) *Network Yield*: Apart from producing defective devices, the process variations could harm the yield in a way that some networks assembled cannot support a target data rate. Specifically, due to the optical nonlinearities of the silicon material, we assume a maximum optical power of 7 dBm per channel [21], which limits the highest data rate that an optical link can attain. We then propose to optimize

$$Y = G / \left\lceil \frac{N}{n} \right\rceil \cdot 100\%, \quad (6)$$

where  $G$  is the number of networks determined capable of supporting the target data rate. Note that in contrast to  $E$  and  $\sigma$ ,  $Y$  is expected to be maximized.

As suggested by Eqs. (4) and (5), both  $E$  and  $\sigma$  can be computed from  $\epsilon_{ij}$ . Therefore, for  $N$  transceivers available for grouping, it is desirable to prepare a cost matrix  $\mathcal{E} \in \mathbb{R}^{N \times N}$  so that every possible  $\epsilon_{ij}$  is computed beforehand for fast look-up. It is also noteworthy that  $\epsilon_{ij}$  is computed as the link power consumption divided by the target data rate. During the computation of  $\epsilon_{ij}$ , if the required optical power is found to exceed the maximum allowed value, the link and the network to which it belongs should be marked as not supporting the target data rate. The preparation of the cost matrix will be detailed



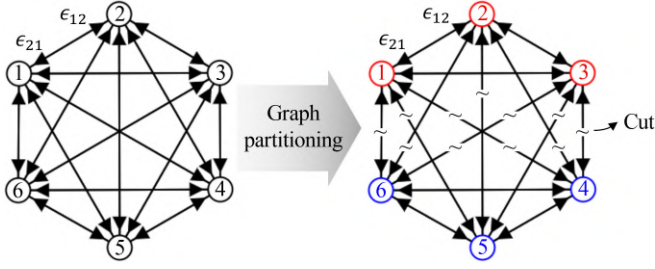


Fig. 4. Transceiver grouping as a graph partitioning problem.

---

**Algorithm 1:** Simulated Annealing (SA) for Transceiver Grouping.

---

**Input** : cost matrix  $\mathcal{E}_{N \times N}$ , initial grouping  $s_0$ ,  $w_1$ , and  $w_2$ .  
**Output** : optimal grouping  $s^*$ ,  $E^*$ ,  $\sigma^*$ , and  $Y^*$ .  
**Goal** : to minimize  $Z = E + w_1 \cdot \sigma + w_2 \cdot (1 - Y)$ .  
 /\* Initialization \*/  
 1 Set initial temperature  $T_0$ , cooling rate  $c$ , re-annealing interval  $i_{\max}$ , and rounds of annealing  $r_{\max}$ ;  
 2  $r \leftarrow 1$ ,  $s \leftarrow s_0$ ;  
 3 Compute  $Z$  from current  $s$ ; // Eqs. (4)-(6) and Eq. (9)  
 4  $Z^* \leftarrow Z$ ,  $s^* \leftarrow s$ ;  
 /\* Simulated annealing \*/  
 5 **while**  $r \leq r_{\max}$  **do**  
 6  $i \leftarrow 1$ ,  $T \leftarrow T_0$ ;  
 7 **while**  $i \leq i_{\max}$  **do**  
 8  $s' \leftarrow \text{shuffle}(s)$ ; // Eq. (8)  
 9 Compute  $Z'$  from  $s'$ ; // Eqs. (4)-(6) and Eq. (9)  
 10 **if**  $Z' < Z$  **then**  
 11  $Z \leftarrow Z'$ ,  $s \leftarrow s'$ ;  
 12 **if**  $Z' < Z^*$  **then**  
 13  $Z^* \leftarrow Z'$ ,  $s^* \leftarrow s'$ ;  
 14 **else**  
 15  $Z \leftarrow Z'$ ,  $s \leftarrow s'$  with a probability of  
 $p = P(Z, Z', T)$ ; // Eq. (10)  
 16  $i \leftarrow i + 1$ ,  $T \leftarrow T \cdot c$ ;  
 17  $r \leftarrow r + 1$ ;

---

in Section IV-C with a description of the device power models involved.

### III. PROBLEM FORMULATION

Consider a complete directed graph with  $N$  vertices and  $N(N-1)$  directed edges, as illustrated in Fig. 4. Suppose that each vertex denotes a transceiver, and each edge is weighted by  $\epsilon_{ij}$ , the energy efficiency of link  $(i, j)$ . Then, the objective of minimizing  $E$ , as suggested by Eq. (4), can be converted to finding a partition of the graph into equally sized blocks such that the sum of in-block edge weights is minimized. It is further equivalent to finding a partition of the graph with the maximum cut weights [22] with a balance constraint on the sub-graphs [23]. The NP-completeness of the graph partitioning problem has been proven [24], and several heuristic methods have been proposed for balanced partitioning [25]–[27]. However, the balance constraint in these algorithms is often formulated as a penalty to the cost function and might not be strictly satisfied. Directly applying them to transceiver grouping can result in groups of different sizes. Moreover, there exists no algorithm for balanced partitioning with multiple objectives. Therefore, we developed our customized heuristics for transceiver grouping.

---

**Algorithm 2:** Greedy Algorithm for Initial Grouping Scheme.

---

**Input** : cost matrix  $\mathcal{E}_{N \times N}$ , group size  $n$ .  
**Output** : initial grouping  $s_0$ .  
 /\* Initialization \*/  
 1  $s_0 \leftarrow$  empty array, ungrouped  $\leftarrow \{1, 2, \dots, N\}$ ;  
 /\* Greedy grouping \*/  
 2 **for**  $g \leftarrow 1$  **to**  $\lfloor N/n \rfloor$  **do**  
 3  $e^* \leftarrow \infty$ , thisGroup  $\leftarrow$  empty array;  
 4 **foreach**  $i \in \text{ungrouped}$  **do**  
 5 **forall the**  $j \in \text{ungrouped} \setminus \{i\}$  **do**  
 6 Find  $(n-1)$  transceivers with the smallest  $(\epsilon_{ij} + \epsilon_{ji})$ , indexed by  $j_{i1}, j_{i2}, \dots, j_{i(n-1)}$ ;  
 7 Compute  $e_i$  for group  $[i, j_{i1}, j_{i2}, \dots, j_{i(n-1)}]$ ; // Eq. (3)  
 8 **if**  $e_i < e^*$  **then**  
 9  $e^* \leftarrow e_i$ , thisGroup  $\leftarrow [i, j_{i1}, j_{i2}, \dots, j_{i(n-1)}]$ ;  
 10 Append thisGroup to  $s_0$ ;  
 11 ungrouped  $\leftarrow \text{ungrouped} \setminus \{\text{elements of thisGroup}\}$ ;

---

#### A. Grouping Scheme Representation

To strictly enforce groups of equal size, we encode a grouping scheme of  $N$  transceivers into a vector  $s$ , where  $s$  is a permutation of  $\{1, 2, \dots, N\}$ . Every  $n$  elements of  $s$  are automatically grouped. For example, a grouping scheme for 16 transceivers into four 4-node networks can be

$$s = [6 \ 3 \ 16 \ 11; 7 \ 14 \ 8 \ 5; 15 \ 1 \ 2 \ 4; 13 \ 9 \ 10 \ 12]. \quad (7)$$

It can be observed that any permutation of the elements within a group does not change the grouping scheme. However, such a representation allows us to easily generate new schemes by *shuffling* a current one:

$$s' = [\dots s'_u \dots s'_v \dots] = \text{shuffle}(s) = [\dots s_v \dots s_u \dots], \quad (8)$$

where  $u$  and  $v$  are randomly chosen from two different groups.

#### B. Proposed Algorithms

1) *Simulated Annealing*: Heuristics based on simulated annealing (SA) [28] can take advantage of the shuffling operation to explore various grouping schemes. We first present an SA-based algorithm (outlined in Algorithm 1) that aims to minimize a unified cost function:

$$Z = E + w_1 \cdot \sigma + w_2 \cdot (1 - Y). \quad (9)$$

Here, the objective  $E$  has a constant weight of 1, while the objectives  $\sigma$  and  $(1 - Y)$  are weighted by  $w_1$  and  $w_2$ , respectively. In other words, the energy efficiency of the networks assembled is always an optimization target, while the significance of the uniformity and the yield, as a second and a third optimization target, can be adjusted by the values of  $w_1$  and  $w_2$ . At each SA iteration, a new grouping scheme  $s'$  is generated by shuffling the current  $s$ , and its corresponding cost  $Z'$  is evaluated based on Eqs. (4)–(6) and Eq. (9). The algorithm decides whether to accept the new grouping scheme with a probability of  $p = P(Z, Z', T)$ :

$$P(Z, Z', T) = \begin{cases} 1 & Z' < Z \\ \frac{1}{1 + \exp((Z' - Z)/T)} & Z' \geq Z \end{cases}, \quad (10)$$

where  $T$  is the current temperature. When  $Z'$  is no better than  $Z$ , there is still a probability between 0 and 1/2 to accept the new grouping scheme in order to avoid local minima.

The SA-based algorithm is seeded by an initial grouping scheme  $s_0$  which is produced by a greedy algorithm (outlined in Algorithm 2). At each iteration, the algorithm greedily groups  $n$  transceivers for the best network energy efficiency determined by Eq. (3), until  $\lfloor N/n \rfloor$  groups are formed.

2) *Pareto Simulated Annealing*: The SA-based algorithm allows the user to prioritize the three minimization targets, namely  $E$ ,  $\sigma$ , and  $(1 - Y)$ , by specifying  $w_1$  and  $w_2$ . However, it presents another challenge to determine the proper values for  $w_1$  and  $w_2$ . A straightforward approach is to sweep  $w_1$  and  $w_2$  within a given range. Alternatively, one may employ another optimization solver that takes  $w_1$  and  $w_2$  as input variables to explore their impact on the optimization results. Nevertheless, both methods involve an execution of the SA-based algorithm for each pair of  $w_1$  and  $w_2$  and thus can be time-consuming. To address this challenge, we further propose an algorithm based on Pareto simulated annealing (PSA) [29] to efficiently explore the trade-off between  $E$ ,  $\sigma$ , and  $Y$ . Without the need to specify  $w_1$  and  $w_2$ , the PSA-based algorithm directly targets

$$\mathbf{Z} = [z_1, z_2, z_3] = [E, \sigma, Y] \quad (11)$$

to find a Pareto front of the three optimization objectives where improving any objective will require sacrificing another. During the PSA iterations, a new solution ( $Z'$ ) is said to dominate an old one ( $Z$ ) if all three objectives of  $Z'$  are improved compared to that of  $Z$ . Accordingly, the rule for deciding whether to accept a new grouping scheme is modified into

$$P(\mathbf{Z}, \mathbf{Z}', \boldsymbol{\Gamma}, T) = \begin{cases} 1 & \mathbf{Z}' \text{ dominates } \mathbf{Z} \\ \frac{1}{1 + \exp(\sum_{i=1}^3 (\gamma_i (z'_i - z_i)) / T)} & \text{otherwise} \end{cases}, \quad (12)$$

where  $\boldsymbol{\Gamma}$  is a vector of weights associated with each optimization objective and automatically updated during the optimization. The larger is the weight of an objective, the lower is the probability of accepting the new grouping scheme if it worsens the objective. At each PSA iteration, multiple new schemes can be generated and evaluated in parallel. Algorithm 3 outlines the main steps of our PSA-based algorithm.

#### IV. DATA PREPARATION

We now introduce the measurement and the synthetic data of microring-based transceivers for evaluating our algorithms. We also elaborate the computation of the cost matrix and the device power models involved.

##### A. Measurement Data

We measured the transmission spectra of some 24-channel microring-based transceivers fabricated by STMicroelectronics on a 300 mm silicon-on-insulator (SOI) wafer. As illustrated in Fig. 5, the transceivers are organized into 66 dies, each die consisting of a transmitter and a receiver. The microrings in each Tx/Rx start with a 5  $\mu\text{m}$  radius and ramp-up to a 5.046  $\mu\text{m}$  radius

#### Algorithm 3: Pareto Simulated Annealing (PSA) for Transceiver Grouping.

```

Input : cost matrix  $\mathcal{E}_{N \times N}$ , initial grouping  $s_0$ , population size  $n_p$ ,
        and weight adjustment factor  $a$ .
Output : a Pareto front of  $E$ ,  $\sigma$ , and  $(1 - Y)$ .
/* Initialization */
1 Set initial temperature  $T_0$ , cooling rate  $c$ , re-annealing interval  $i_{\max}$ ,
  and rounds of annealing  $r_{\max}$ ;
2 Generate a set  $S$  of  $n_p$  grouping schemes by shuffling  $s_0$ ; // Eq. (8)
3 forall the  $s \in S$  do
4   Compute  $\mathbf{Z}$  from  $s$  and update the Pareto front  $F$ ; // Eqs. (4)-(6)
   and Eq. (11)
5  $r \leftarrow 1$ ;
/* Pareto simulated annealing */
6 while  $r \leq r_{\max}$  do
7    $i \leftarrow 1$ ,  $T \leftarrow T_0$ ,  $\boldsymbol{\Gamma} \leftarrow [1/3, 1/3, 1/3]$ ;
8   while  $i \leq i_{\max}$  do
9     foreach  $s \in S$  do
10       $s' \leftarrow \text{shuffle}(s)$ ; // Eq. (8)
11      Compute  $\mathbf{Z}'$  from  $s'$ ; // Eqs. (4)-(6) and Eq. (11)
12      if  $\mathbf{Z}'$  dominates  $\mathbf{Z}$  then
13        Update the Pareto front with  $\mathbf{Z}'$  added;
14         $s \leftarrow s'$ ;
15      else
16        for  $i \leftarrow 1$  to # of objectives do
17          if  $z'_i \geq z_i$  then
18             $\gamma_i \leftarrow \gamma_i \cdot a$ ;
19          else
20             $\gamma_i \leftarrow \gamma_i / a$ ;
21         $s \leftarrow s'$  and update the Pareto front with  $\mathbf{Z}'$  with a
        probability of  $p = P(\mathbf{Z}, \mathbf{Z}', \boldsymbol{\Gamma}, T)$ ; // Eq. (12)
22       $i \leftarrow i + 1$ ,  $T \leftarrow T \cdot c$ ;
23    $r \leftarrow r + 1$ ;

```

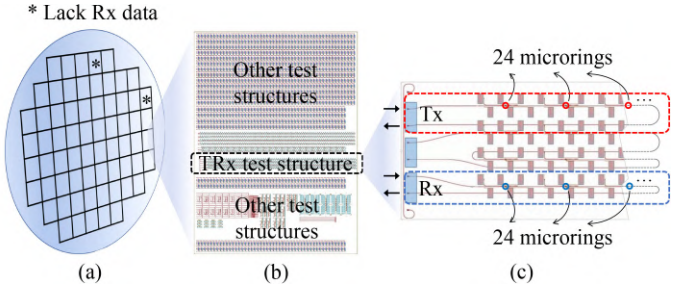


Fig. 5. Organization of measured devices: (a) 66 dies on a wafer; (b) each die consisting of one TRx; and (c) each Tx/Rx consisting of 24 microrings.

with a step size of 2 nm. The Rx spectra of two dies were not measured correctly, as indicated in Fig. 5(a). Thus, we have the measurement data of 64 fabricated transceivers for evaluating our grouping algorithms.

##### B. Synthetic Data

To emulate situations where more transceivers are available for grouping, we generate synthetic data of transceivers to evaluate our grouping algorithms. We first extracted the resonance wavelength ( $\lambda_r$ ), the extinction ratio ( $ER$ ), and the quality factor ( $Q$ ) of each fabricated microring by fitting Eq. (2) to the measured spectra (Fig. 2). Then, we effectively characterized the spatial variations of  $\lambda_r$ ,  $ER$ , and  $Q$  by applying our well-established variation modeling method [30]. Specifically,

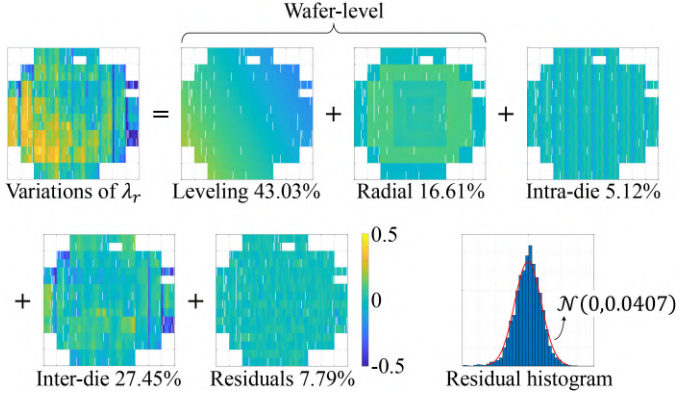


Fig. 6. Wafer-scale variation characterization for  $\lambda_r$ . Same process applied to  $ER$  and  $Q$ .

TABLE I  
SUMMARY OF SPATIAL VARIATION DECOMPOSITION

|             | Wafer-level |        | Intra-die | Inter-die | Residual | Residual distribution    |
|-------------|-------------|--------|-----------|-----------|----------|--------------------------|
|             | Leveling    | Radial |           |           |          |                          |
| $\lambda_r$ | 43.03%      | 16.61% | 5.12%     | 27.45%    | 7.79%    | $\mathcal{N}(0, 0.0407)$ |
| $ER$        | 0.04%       | 1.60%  | 32.67%    | 18.61%    | 47.08%   | $\mathcal{N}(0, 0.0891)$ |
| $Q$         | 1.59%       | 2.31%  | 29.47%    | 21.72%    | 44.91%   | $\mathcal{N}(0, 0.0940)$ |

we attribute the location dependency of the variation magnitude on a wafer to three systematic components, namely wafer-level, intra-die, and inter-die components. This hierarchical method, detailed in [30], involves the usage of

- 1) robust regression [31] to fit the measurement data with several wafer-level basis functions, followed by
- 2) a spatial-frequency-domain analysis to extract the intra-die variation patterns, and
- 3) low-rank tensor factorization [32] to extract the inter-die variation patterns.

Finally, we fit the residuals from this hierarchical decomposition process with a normal distribution  $\mathcal{N}(\mu, \sigma)$  that is assumed spatially-stationary across the wafer. Fig. 6 visualizes the variation modeling process for  $\lambda_r$  as an example. The variations of  $ER$  and  $Q$  were modeled in the same manner, and the results are summarized in Table I.

We generate wafer-level data for  $\lambda_r$ ,  $ER$ , and  $Q$  following the variation model and synthesize them into transceiver spectra based on Eq. (2). To validate that our synthetic transceivers can closely resemble the fabricated ones in terms of power and energy estimation, we simulated the microring tuning power and the communication energy efficiency for the fabricated transceivers and ten wafers of synthetic transceivers. Fig. 7 plots the simulation results in ascending order for a data rate of 30 Gb/s per channel, showing a considerable resemblance of the synthetic transceivers to the fabricated ones. The power models used in these simulations are the same as those used for the computation of  $\epsilon_{ij}$  and will be detailed in Section IV-C.

### C. Cost Matrix

For  $N$  transceivers available for grouping, a cost matrix  $\mathcal{E} \in \mathbb{R}^{N \times N}$  is computed where the entry  $\epsilon_{ij}$  is the energy

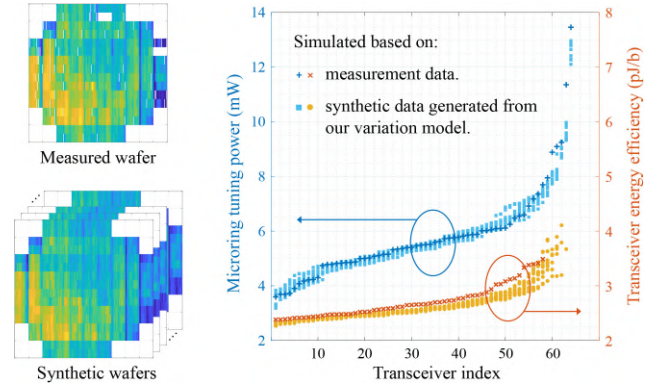


Fig. 7. Synthetic data generation and validation.

TABLE II  
MODELS AND ASSUMPTIONS FOR LINK POWER COMPUTATION

|                            |  |                     |              |
|----------------------------|--|---------------------|--------------|
| <b>Laser</b>               |  |                     |              |
| Wall-plug efficiency       | 20% [33]                                     |                     |              |
| <b>Data rate-dependent</b> |  |                     |              |
| $P_{\text{sensitivity}}$   | [34]   | $P_{\text{driver}}$ | [8]          |
| <b>Microring losses</b>    |  |                     |              |
| Passing                    | 0.2 dB                                       | Drop-port           | 1 dB         |
| Insertion                  | Computed for a modulation distance of 0.2 nm |                     |              |
| <b>Waveguide losses</b>    |  |                     |              |
| Coupling                   | 1 dB [34]                                    | Propagation         | 1 dB/cm [34] |

efficiency of a unidirectional link from Tx  $\#i$  to Rx  $\#j$  at a given data rate,  $i, j \in \{1, 2, \dots, N\}$ . We compute  $\epsilon_{ij}$  as the power consumption of the link divided by the aggregated data rate of all DWDM channels. The power consumption includes those of the laser, microring wavelength tuning, and Tx/Rx driver circuitry. Therefore, we have

$$\epsilon_{ij} = \frac{P_{\text{laser}} + P_{\text{tuning}} + P_{\text{driver}}}{m \cdot \text{DR}}, \quad (13)$$

where  $m$  is the number of DWDM channels, and DR is the target data rate per channel. The power models and assumptions are listed in Table II and explained as follows.

1) **Laser Power:** We assume a quantum dot comb laser [33] that can generate a group of evenly-spaced frequency combs to cover the free spectrum range (FSR) of the microrings. We further assume a Gaussian-shaped comb spectrum, as illustrated in Fig. 8, with a spectrum efficiency  $\eta = P_{\text{usable}}/P_{\text{total}} \approx -3.2$  dB [35]. The optical power provided at the laser output must be high enough so that the following power budget equation holds for any channel  $k \in \{1, 2, \dots, m\}$ :

$$P_{\text{comb},k} \cdot \text{PL}_k \geq P_{\text{sensitivity}}. \quad (14)$$

Here,  $P_{\text{comb},k}$  is the optical power of the  $k$ th comb line;  $\text{PL}_k \in (0, 1)$  is the overall power loss of the  $k$ th channel, which is the product of several losses (listed in Fig. 8) as the light travels;  $P_{\text{sensitivity}}$  is the sensitivity requirement of the receiver and is modeled as a function of the data rate in [34]. The laser is characterized by the wall-plug efficiency (WPE) when converting



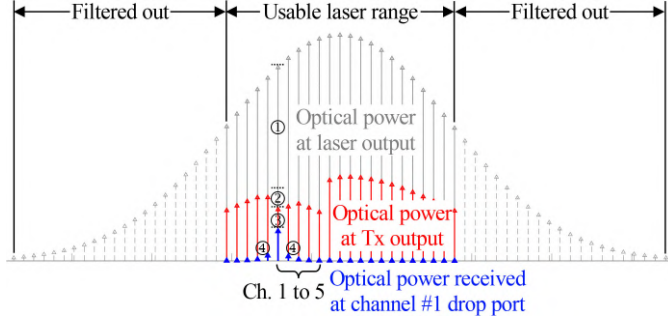


Fig. 8. Power losses in a microring-based optical link, plotted for five channels for illustration purpose, including ① coupling loss and modulator passing loss; ② modulator insertion loss; ③ coupling loss, propagation loss, and Rx drop-port loss; and ④ crosstalk noise.

the electrical power into the optical power:

$$P_{\text{laser}} = \left( \sum P_{\text{comb}} \right) / \text{WPE}. \quad (15)$$

Based on Eqs. (14) and (15), the laser power consumption can be computed for various data rates and is consistent with what reported in [33]. Note that if the required optical power for Eq. (14) to hold exceeds the maximum power allowed (7 dBm as per [21]), the link is marked as not supporting the target data rate.

2) *Microring Tuning*: The  $P_{\text{tuning}}$  term in Eq. (13) is the tuning power required to align the microring resonance wavelengths of Tx # $i$  and Rx # $j$  to a mutual set of laser comb lines. We assume that thermal tuning is adopted to redshift the resonance wavelengths of the microrings with a tuning efficiency of 0.15 nm/mW [36]. If some resonance wavelengths fall out of the usable laser range, channel shuffling [9], [10] is applied to utilize a neighboring mode for alignment.

3) *Driver Circuitry*: We consider the modulator drivers, the receiver transimpedance amplifiers (TIA), and the serializer/deserializer (SerDes) circuitry as the main components of the driver circuitry of an optical link, thus:

$$P_{\text{driver}} = P_{\text{mod}} + P_{\text{TIA}} + P_{\text{SerDes}}. \quad (16)$$

A decent analysis is provided in [8] that models the power of the driver circuitry as a function of the data rate. In this study, we made lookup tables for  $P_{\text{driver}}$  at various data rates for the computation of  $\epsilon_{ij}$ .

Note that for network topologies other than the generic ring bus described in Section II-C, one can adjust Eq. (13) accordingly for computing  $\epsilon_{ij}$ , which is the energy efficiency of a unidirectional link from Tx # $i$  to Rx # $j$  including relay nodes (if there are any), so that the transceiver grouping algorithms proposed in Section III-B can be directly applied without modification.

## V. EVALUATION

We evaluated our SA- and PSA-based algorithms for transceiver grouping based on the data of 64 measured transceivers and up to 256 synthetic transceivers for a wide range of network configurations.

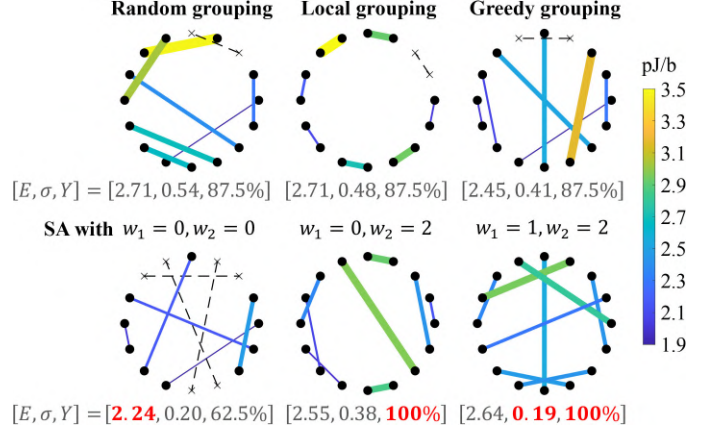


Fig. 9. Illustration of grouping schemes for  $N = 16$  and  $n = 2$  at a target data rate of 30 Gb/s per channel.

### A. SA-Based Grouping Algorithm

1) *Effectiveness*: We first present a few case studies to demonstrate the effectiveness of our SA-based algorithm (Algorithm 1). Fig. 9 shows an example for  $N = 16$  and  $n = 2$  at a target data rate of 30 Gb/s per channel. Several grouping schemes are illustrated in the form of graphs, including random grouping, local grouping, greedy grouping, and three grouping schemes produced by the SA-based algorithm with different  $w_1$ 's and  $w_2$ 's. The nodes in each graph represent the transceivers available for grouping (i.e., pairing when  $n = 2$ ). The energy efficiency of each group (pair) is computed from the data of the first 16 measured transceivers. The thinner an edge, the better the energy efficiency. A dashed line, however, indicates that the link cannot support the target data rate.

We observed from Fig. 9 that, compared to a random grouping scheme, the local grouping scheme that groups neighboring transceivers on a wafer only achieves marginal improvement in  $E$  and  $\sigma$ . It might seem non-intuitive, as local grouping should mitigate the impact of wafer-level variations. However, Table I suggests that even neighboring transceivers still suffer from significant inter-die variations. The observation justifies the need for more sophisticated grouping algorithms. We further observed that

- the greedy algorithm achieves considerable improvement in  $E$  but not  $\sigma$ , as the transceivers that lead to better energy efficiency are greedily grouped at earlier steps, leaving the remaining ones grouped at later steps incurring significantly worse energy efficiency;
- the SA-based algorithm, which initiates the optimization by shuffling the greedy grouping scheme, can further improve  $E$  when  $w_1 = w_2 = 0$ , but may converge to a solution with a low yield;
- the SA-based algorithm can also improve  $\sigma$  and  $Y$  by increasing their corresponding weights, at the cost of less improvement in other objectives.

We then used the *energy-yield curves* to compare different grouping schemes for other network configurations. Fig. 10 provides two more cases for  $N = 32$  and  $64$ ,  $n = 4$ , at a target



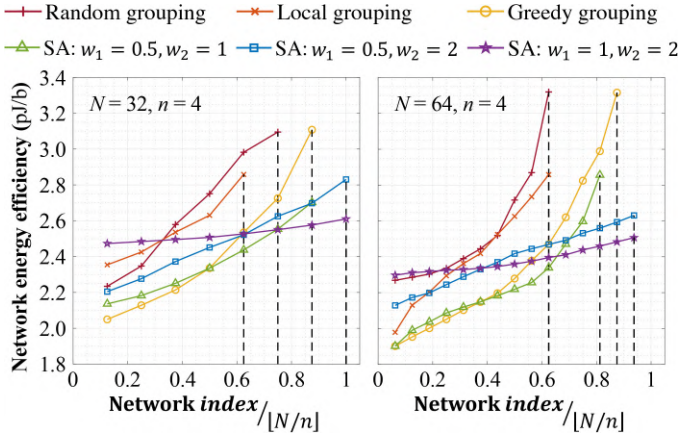


Fig. 10. Comparison of grouping schemes for  $N = 32, 64$  and  $n = 4$  at a target data rate of 30 Gb/s per channel.

data rate of 30 Gb/s per channel. Specifically, for each grouping scheme, we plotted the energy efficiency of all networks assembled in ascending order, so that the average energy efficiency and the uniformity of the networks assembled can be visualized by the position and the slope of a curve. On the other hand, the horizontal axis of the plot, i.e., the network index  $g \in \{1, 2, \dots, G\}$ , was normalized by  $\lfloor N/n \rfloor$ . Then, as defined by Eq. (6), the network yield of a grouping scheme can thus be visualized by the  $x$ -coordinate of the ending point of the corresponding curve, as indicated by the vertical dashed lines in Fig. 10. The energy-yield curves again verified that our SA-based algorithm, with a proper assignment of  $w_1$  and  $w_2$ , can achieve significant improvement in the average energy efficiency and the yield of the networks assembled, while drastically improving the uniformity compared to a random grouping scheme.

2) *Scalability*: We further evaluated our SA-based algorithm for a variety of network configurations that cover  $N \in \{16, 32, 64, 128, 256\}$ ,  $n \in \{2, 4, 8, 16\}$ , and a target data rate ranging from 20 Gb/s to 30 Gb/s per channel. We computed the improvement in  $E$ ,  $\sigma$ , and  $Y$  achieved by our SA-based algorithm over random grouping. Note that the improvement in  $E$  and  $\sigma$  is measured by the percentage of reduction compared to that of the random grouping scheme, while the improvement in  $Y$  is measured by the arithmetic difference of the yields (a.k.a. *percentage points* or *p.p.*) of the two grouping schemes. For example, improving the yield from 50% to 80% is considered as an increase of 30 percentage points, rather than a 60% increase. Overall, our SA-based algorithm with  $w_1 = 1$  and  $w_2 = 2$  achieves up to 25% improvement in the average energy efficiency of the networks assembled, up to 94% reduction of the standard deviation of the energy efficiency, and up to 75 percentage points increase of the network yield, compared to a random grouping scheme for the network configurations evaluated. Furthermore, we observed several trends from the evaluation results that are noteworthy:

- As shown in Fig. 11(a), for a given network size ( $n$ ) and a target data rate, the energy efficiency improvement achieved by our SA-based algorithm increases with  $N$ ,

i.e., the total number of transceivers. In other words, with more transceivers available for grouping, there is a greater opportunity to optimize the average energy efficiency of the networks assembled.

- As shown in Fig. 11(b), for a given number of transceivers available for grouping, the reduction of the standard deviation of the energy efficiency, achieved by our SA-based algorithm, is more significant for a larger  $n$ . In other words, when the networks to be assembled are of a larger size, there is a greater opportunity to group the transceivers in a way that the networks assembled have relatively similar energy efficiency.
- As shown in Fig. 11(c), for a given number of transceivers available for grouping, the yield improvement achieved by our SA-based algorithm is greater for a larger  $n$  and a higher data rate. It was observed that the network yield resulted from a random grouping scheme drastically decreases with the network size and the target data rate. Especially for  $n = 16$ , none of the randomly assembled networks could support a target data rate of 30 Gb/s. Nevertheless, our SA-based algorithm can maintain a reasonably high yield for all network configurations evaluated.

The execution time of our SA-based algorithm was recorded for an initial temperature of 100, a cooling rate of 0.95, a re-annealing interval of  $(10 \times N)$  iterations, and 50 rounds of annealing. Thus, each optimized grouping scheme was produced from a total of  $(500 \times N)$  annealing iterations. According to Fig. 12, this setting was empirically found adequate for Eq. (9) to converge to a steady value. As shown in Fig. 11(d), the execution time of our SA-based algorithm grows polynomially with the number of transceivers and is largely independent of other network parameters. Limited within 40 s for  $N = 256$ , the execution time of our SA-based algorithm is considered a small overhead to the test time of the fabricated transceivers.

## B. PSA-Based Grouping Algorithm

The SA-based algorithm requires a proper combination of  $w_1$  and  $w_2$  to be specified. To avoid excessive trials only to determine the values for  $w_1$  and  $w_2$ , the SA-based algorithm is best suited for situations where

- 1) either the uniformity or the yield of the networks assembled has an overriding priority over the other, so that having  $w_1$  or  $w_2$  equal to zero generally works well; or
- 2) the proper values for  $w_1$  and  $w_2$  are already learned from past runs for the network configuration of interest.

For situations where the proper values for  $w_1$  and  $w_2$  are unknown, our PSA-based algorithm (Algorithm 3) can effectively and efficiently explore the trade-off between the three optimization objectives, namely the energy efficiency, the uniformity, and the yield of the networks assembled. By giving a set of Pareto-optimal solutions in a single run, our PSA-based algorithm allows one to select a desired grouping scheme without the need to specify  $w_1$  and  $w_2$ . We compared our PSA-based algorithm to two other methods that explore the same trade-off by varying the combination of  $w_1$  and  $w_2$ :

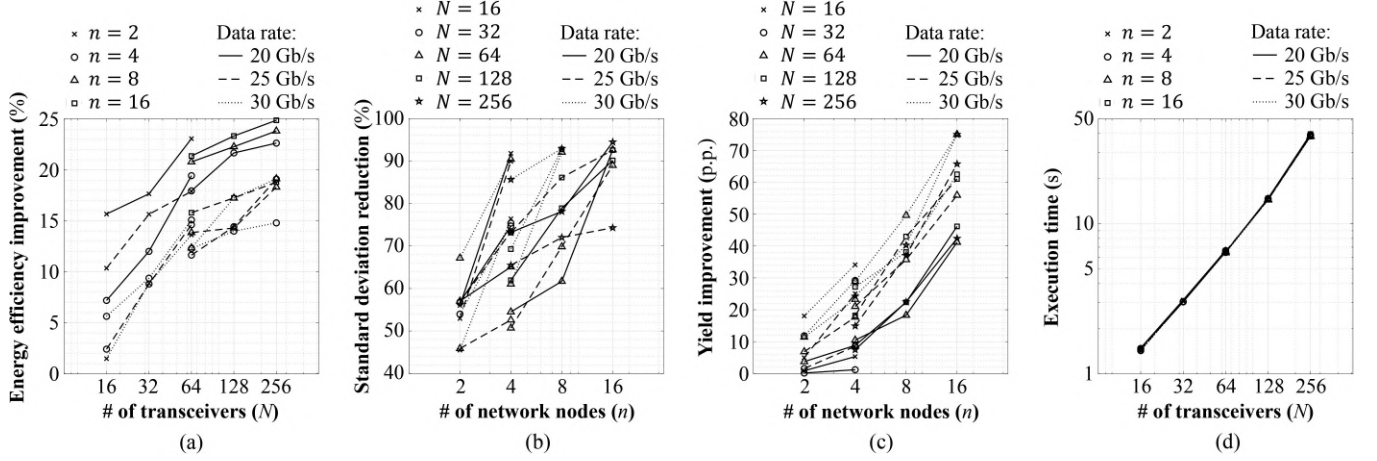


Fig. 11. (a)–(c) Improvement achieved by our SA-based algorithm with  $w_1 = 1$  and  $w_2 = 2$  over the random grouping scheme in energy efficiency, yield, and uniformity, evaluated for various network configurations. (d) Execution time of our SA-based algorithm for various network configurations.

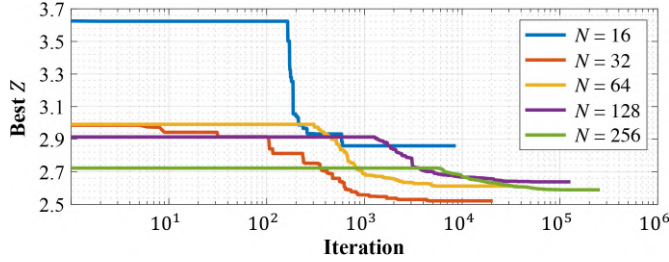


Fig. 12. Evolution of the cost value with SA iterations, plotted for  $n = 4$  and 30 Gb/s per channel as an example.

- 1) To sweep  $w_1$  and  $w_2$  within a given range (hereafter the *SWEEP* method). For each combination of  $w_1$  and  $w_2$ , the SA-based algorithm is called to optimize Eq. (9). The Pareto front of  $E$ ,  $\sigma$ , and  $Y$  is derived after the sweeping by eliminating the dominated solutions.
  - 2) To employ another optimization solver that takes  $w_1$  and  $w_2$  as input variables. In this study, we modified an existing implementation of Multi-Objective Particle Swarm Optimization [37] (hereafter the *MOPSO* method). In each generation, the MOPSO method generates multiple combinations of  $w_1$  and  $w_2$  and calls the SA-based algorithm to optimize Eq. (9) for each combination. The Pareto front of  $E$ ,  $\sigma$ , and  $Y$  is updated at the end of each generation, and new combinations of  $w_1$  and  $w_2$  are generated for the next generation based on the current Pareto front.
- 1) *Effectiveness*: For each network configuration, i.e., given  $N$ ,  $n$ , and a target data rate, a Pareto front of  $E$ ,  $\sigma$ , and  $Y$  was explored by SWEEP, MOPSO, and our PSA-based algorithm with the following settings, respectively:

**SWEEP** We swept both  $w_1$  and  $w_2$  from 0.2 to 2 with a step size of 0.2. Thus, a total of 100 different combinations of  $w_1$  and  $w_2$  were explored. For each combination of  $w_1$  and  $w_2$ , a grouping scheme was optimized through  $(500 \times N)$  SA iterations.

**MOPSO** We specified a population size of 10 for the MOPSO method, i.e., ten combinations of  $w_1$  and  $w_2$

generated and evaluated in each generation. Thus, a total of 100 combinations of  $w_1$  and  $w_2$  were explored in 10 generations, each producing a grouping scheme optimized through  $(500 \times N)$  SA iterations.

**PSA** We executed our PSA-based algorithm for  $(500 \times N)$  iterations with a population size of 100, where each individual in the population is a candidate grouping scheme. In other words, 100 grouping schemes were simultaneously optimized through  $(500 \times N)$  PSA iterations.

Fig. 13 shows the results for  $N = 32, 64, n = 4$ , and  $N = 128, 256, n = 8$ , at a target data rate of 30 Gb/s per channel. Specifically, each plotted point corresponds to a grouping scheme, whose  $E$  and  $\sigma$  can be read from its  $x$ - and  $y$ -coordinates, respectively. The value of  $Y$  is color-coded from light yellow (lowest) to dark blue (highest). Therefore, a grouping scheme is considered a better one if it is closer to the bottom left corner and darker in color. The random, local, and greedy grouping schemes are also marked in each plot. We compared the Pareto-optimal grouping schemes produced by SWEEP, MOPSO, and our PSA-based algorithm and made the following observations:

- The yield of the networks assembled, as suggested by Eq. (6), can only take a few discrete values. Thus, the Pareto front of  $E$ ,  $\sigma$ , and  $Y$  appears as multiple curves that correspond to different yield values. Taking Fig. 13(a) as an example, for a network configuration of interest, one may pick a grouping scheme from the Pareto front by first specifying an acceptable yield value, then selecting a grouping scheme on the corresponding curve that reflects the desired trade-off between  $E$  and  $\sigma$ .
- In all four plots of Fig. 13, most of the Pareto-optimal solutions given by SWEEP and MOPSO are overlaid by solutions given by our PSA-based algorithm. In other words, our PSA-based algorithm can produce Pareto-optimal grouping schemes as good as those identified by SWEEP and MOPSO.

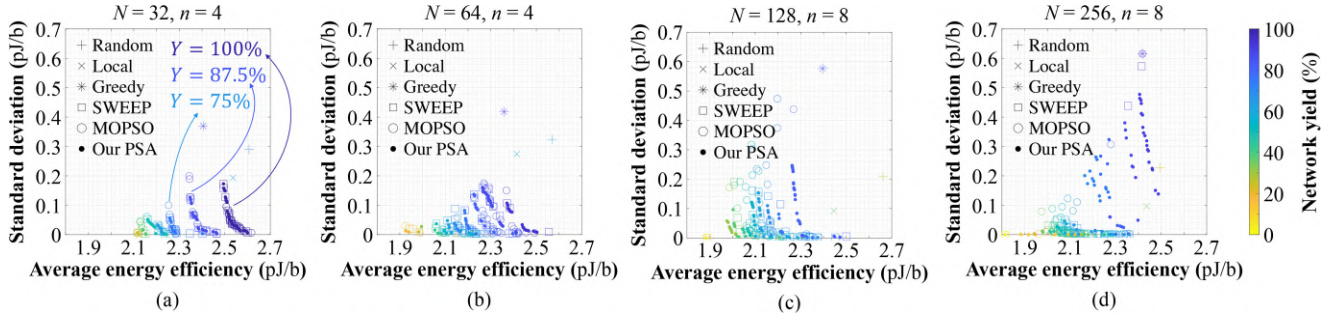


Fig. 13. Comparison of the Pareto fronts of  $E$ ,  $\sigma$ , and  $Y$  produced by SWEEP, MOPSO, and our PSA-based algorithm for (a)  $N = 32$ ,  $n = 4$ , (b)  $N = 64$ ,  $n = 4$ , (c)  $N = 128$ ,  $n = 8$ , and (d)  $N = 256$ ,  $n = 8$ , at a target data rate of 30 Gb/s per channel.

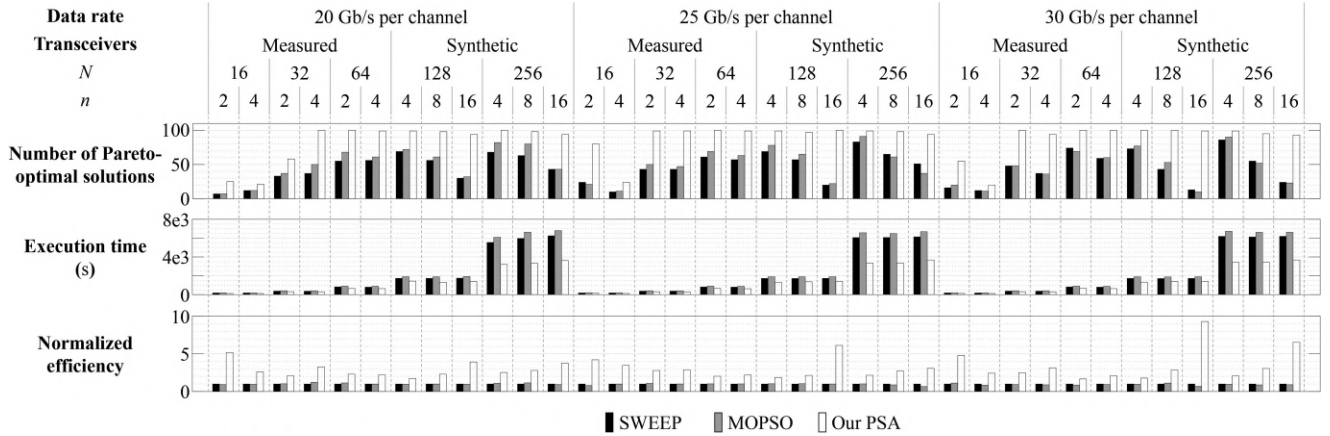


Fig. 14. Number of Pareto-optimal solutions, execution time, and efficiency comparison of SWEEP, MOPSO, and our PSA-based algorithm.

- For  $N = 128$  and  $256$ , both SWEEP and MOPSO tend to produce grouping schemes with a low yield. Nevertheless, our PSA-based algorithm can still explore various grouping schemes with a reasonably high yield.
- Our PSA-based algorithm can always identify multiple grouping schemes that are significantly better than the random grouping scheme in all three optimization objectives, namely  $E$ ,  $\sigma$ , and  $Y$ .

2) *Efficiency*: We defined the efficiency of SWEEP, MOPSO, and our PSA-based algorithm as the number of Pareto-optimal grouping schemes that can be produced in unit time. Using the settings specified in Section V-B1, the number of candidate grouping schemes to be optimized by each method was 100, while some of the optimized grouping schemes ended up not on the Pareto front. Fig. 14 compares the efficiency of our PSA-based algorithm to that of SWEEP and MOPSO for various network configurations, and the following observations were made:

- The MOPSO method brought a minor increase in the number of Pareto-optimal grouping schemes compared to the SWEEP method, at the cost of longer execution time for the same amount of candidates evaluated. On average, the MOPSO method only achieved 0.97x efficiency compared to the SWEEP method.

- Our PSA-based algorithm, compared to both SWEEP and MOPSO, can produce significantly more Pareto-optimal grouping schemes within a shorter execution time for all network configurations evaluated. Overall, our PSA-based algorithm achieved 1.67x to 9.30x improvement in terms of efficiency with an average of 3.13x, compared to the SWEEP method.

In a nutshell, when a proper combination of  $w_1$  and  $w_2$  is unknown, our PSA-based algorithm can explore a larger solution space with better efficiency compared to SWEEP and MOPSO, producing more Pareto-optimal grouping schemes for selection.

## VI. CONCLUSION

In this study, we target the application scenario where fabricated microring-based transceivers are grouped for assembling optical networks of multiple nodes. We propose two algorithms to mix and match the fabricated transceivers so that the three optimization objectives, namely the average energy efficiency, the uniformity, and the yield of the networks assembled, are optimized. We evaluated our proposed algorithms by wafer-scale measurement data of microring-based transceivers, as well as synthetic data generated based on an experimentally validated



variation model. Our first algorithm based on simulated annealing (SA) can achieve up to 25% improvement in the average energy efficiency of the networks assembled, up to 94% reduction of the standard deviation of the energy efficiency, and up to 75 percentage points increase of the network yield, compared to a baseline strategy that randomly groups the transceivers. Moreover, our second algorithm based on Pareto simulated annealing (PSA) can efficiently produce multiple Pareto-optimal grouping schemes that significantly outperform the random grouping scheme in all three optimization objectives, namely the energy efficiency, the uniformity, and the yield of the networks assembled.

## REFERENCES

- [1] R. G. Beausoleil, M. McLaren, and N. P. Jouppi, "Photonic architectures for high-performance data centers," *IEEE J. Sel. Top. Quantum Electron.*, vol. 19, no. 2, pp. 3700109–3700109, Mar. 2013.
- [2] R. G. Beausoleil, "Large-scale integrated photonics for high-performance interconnects," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 7, no. 2, pp. 1–54, Jun. 2011.
- [3] C.-H. Chen *et al.*, "Concurrent multi-channel transmission of a DWDM silicon photonic transmitter based on a comb laser and microring modulators," in *Proc. IEEE Int. Conf. Photon. Switch. (PS)*, Sep. 2015, pp. 175–177.
- [4] M. A. Seyed *et al.*, "Concurrent DWDM transmission with ring modulators driven by a comb laser with 50GHz channel spacing," in *Proc. 21st Optoelectron. Commun. Conf.*, 2016, pp. 9–11.
- [5] P. Grani and S. Bartolini, "Design options for optical ring interconnect in future client devices," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 10, no. 4, pp. 1–25, May 2014.
- [6] S. Werner, J. Navaridas, and M. Luján, "A survey on optical network-on-chip architectures," *ACM Comput. Surv.*, vol. 50, no. 6, pp. 1–37, Jan. 2018.
- [7] J. Bashir, E. Peter, and S. R. Sarangi, "A survey of on-chip optical interconnects," *ACM Comput. Surv.*, vol. 51, no. 6, pp. 1–34, Feb. 2019.
- [8] R. Polster, Y. Thonnart, G. Waltener, J.-L. Gonzalez, and E. Cassan, "Efficiency optimization of silicon photonic links in 65-nm CMOS and 28-nm FDSOI technology nodes," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 24, no. 12, pp. 3450–3459, Dec. 2016.
- [9] A. V. Krishnamoorthy *et al.*, "Exploiting CMOS manufacturing to reduce tuning requirements for resonant optical devices," *IEEE Photon. J.*, vol. 3, no. 3, pp. 567–579, Jun. 2011.
- [10] M. Georgas, J. Leu, B. Moss, C. Sun, and V. Stojanovic, "Addressing link-level design tradeoffs for integrated photonic interconnects," in *Proc. IEEE Cust. Integr. Circuits Conf.*, Sep. 2011, pp. 1–8.
- [11] Yan Zheng, P. Lisherness, S. Shamsiri, A. Ghofrani, Shiyuan Yang, and K.-T. Cheng, "Post-fabrication reconfiguration for power-optimized tuning of optically connected multi-core systems," in *Proc. 17th Asia South Pacific Des. Autom. Conf.*, Jan. 2012, pp. 615–620.
- [12] Y. Zheng *et al.*, "Power-efficient calibration and reconfiguration for optical network-on-chip," *J. Opt. Commun. Netw.*, vol. 4, no. 12, pp. 955–966, Dec. 2012.
- [13] Y. Wang *et al.*, "Energy-efficient channel alignment of DWDM silicon photonic transceivers," in *Proc. IEEE Des. Autom. Test Eur. Conf. Exhib.*, Mar. 2018, pp. 601–604.
- [14] Y. Wang, M. A. Seyed, J. Hulme, M. Fiorentino, R. G. Beausoleil, and K.-T. Cheng, "Bidirectional tuning of microring-based silicon photonic transceivers for optimal energy efficiency," in *Proc. 24th Asia South Pacific Des. Autom. Conf.*, Jan. 2019, pp. 370–375.
- [15] R. Wu *et al.*, "Pairing of microring-based silicon photonic transceivers for tuning power optimization," in *Proc. IEEE 23rd Asia South Pacific Des. Autom. Conf.*, Jan. 2018, pp. 135–140.
- [16] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon electro-optic modulator," *Nature*, vol. 435, no. 7040, pp. 325–327, May 2005.
- [17] G. Hendry *et al.*, "Time-division-multiplexed arbitration in silicon nanophotonic networks-on-chip for high-performance chip multiprocessors," *J. Parallel Distrib. Comput.*, vol. 71, no. 5, pp. 641–650, May 2011.
- [18] Z. Wang *et al.*, "A case study on the communication and computation behaviors of real applications in NOC-based mpsoes," in *Proc. IEEE Comput. Soc. Annu. Symp.*, Jul. 2014, pp. 480–485.
- [19] R. K. V. Maeda *et al.*, "JADE: A heterogeneous multiprocessor system simulation platform using recorded and statistical application models," in *Proc. 1st Int. Work. Adv. Interconnect Solution Technol. Emerg. Comput. Syst.*, 2016, pp. 1–6.
- [20] P. Sun *et al.*, "Statistical behavioral models of silicon ring resonators at a commercial CMOS foundry," *IEEE J. Sel. Top. Quantum Electron.*, vol. 26, no. 2, pp. 1–10, Mar. 2020.
- [21] Q. Li *et al.*, "Experimental characterization of the optical-power upper bound in a silicon microring modulator," in *Proc. IEEE Opt. Interconnects Conf.*, May 2012, vol. 5, pp. 38–39.
- [22] C. W. Commander, *Maximum Cut Problem, MAX-CUT*. Berlin, Germany: Springer, 2009, pp. 1991–1999.
- [23] K. Andreev and H. Räcke, "Balanced graph partitioning," in *Proc. Sixteen Annu. ACM Symp. Parallelism Algorithms Archit.*, 2004, pp. 120–124, vol. 16.
- [24] M. R. Garey and D. S. Johnson, *Computers and Intractability: A Guide to the Theory of NP-Completeness*. New York, NY, USA: W. H. Freeman, 1990.
- [25] B. Chamberlain, "Graph partitioning algorithms for distributing workloads of parallel computations," Univ. Washington, Tech. Rep. UW-CSE-98-10-03, 1998.
- [26] R. Baños, C. Gil, M. G. Montoya, and J. Ortega, "A new pareto-based algorithm for multi-objective graph partitioning," in *Proc. Lect. Notes Comput. Sci. (including Subser. Lect. Notes Artif. Intell. Lect. Notes Bioinform.)*, 2004, vol. 3280, pp. 779–788.
- [27] K. Aydin, M. Bateni, and V. Mirrokni, "Distributed balanced partitioning via linear embedding," *Algorithms*, vol. 12, no. 8, pp. 1–27, Aug. 2019. [Online]. Available: <https://www.mdpi.com/1999-4893/12/8/162>
- [28] D. Bertsimas and J. Tsitsiklis, "Simulated annealing," *Statist. Sci.*, vol. 8, no. 1, pp. 10–15, Feb. 1993.
- [29] P. Czyżak and A. Jaskiewicz, "Pareto simulated annealing," in *Proc. Multi-Criteria Decis. Making*, 1997, pp. 297–307.
- [30] Y. Wang *et al.*, "Characterization and applications of spatial variation models for silicon microring-based optical transceivers," in *Proc. IEEE 57th ACM/IEEE Des. Autom. Conf.*, Jul. 2020, pp. 1–6.
- [31] P. J. Huber, *Robust Statistics*. Berlin, Germany: Springer, 2011, pp. 1248–1251.
- [32] T. G. Kolda and B. W. Bader, "Tensor decompositions and applications," *SIAM Rev.*, vol. 51, no. 3, pp. 455–500, Aug. 2009.
- [33] D. Livshits *et al.*, "High efficiency diode comb-laser for DWDM optical interconnects," in *Proc. IEEE Opt. Interconnects Conf.*, May 2014, vol. 6, pp. 83–84.
- [34] M. Bahadori *et al.*, "Energy-performance optimized design of silicon photonic interconnection networks for high-performance computing," in *Proc. IEEE Des. Autom. Test Eur. Conf. Exhib.*, Mar. 2017, pp. 326–331.
- [35] M. J. R. Heck and J. E. Bowers, "Energy efficient and energy proportional optical interconnects for multi-core processors: Driving the need for on-chip sources," *IEEE J. Sel. Top. Quantum Electron.*, vol. 20, no. 4, pp. 332–343, Jul. 2014.
- [36] K. Yu *et al.*, "A 25 Gb/s hybrid-integrated silicon photonic source-synchronous receiver with microring wavelength stabilization," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2129–2141, Sep. 2016.
- [37] C. Coello Coello and M. Lechuga, "MOPSO: A proposal for multiple objective particle swarm optimization," in *Proc. IEEE Congr. Evol. Comput.*, 2002, vol. 2, pp. 1051–1056.

**Yuyang Wang** received the B.Eng. degree in electronic engineering from Tsinghua University, Beijing, China in 2015, and the M.S. degree in computer engineering from the University of California, Santa Barbara (UCSB), CA, USA, in 2018. He is currently a Ph.D. candidate with the Department of Electrical and Computer Engineering, UCSB. He was a Design Engineering Intern at Cadence Design Systems in 2018 and a Visiting Intern at the Hong Kong University of Science and Technology in 2019. His research interests include variation-aware modeling, design, and optimization of silicon photonic interconnects and systems.

**Peng Sun** received the Ph.D. degree in electrical engineering from Ohio State University, Columbus, OH, USA, in 2012. He was a Senior Engineer with Luxtera Inc., Carlsbad, CA, USA, from 2012 to 2018. He is currently a Research Engineer with Hewlett Packard Labs, Palo Alto, CA, USA.

**Jared Hulme** received the master's and the Ph.D. degrees in electrical and computer engineering with an emphasis on silicon photonics from the University of California, Santa Barbara, CA, USA, in 2012 and 2017, respectively. He has continued to research photonics with Hewlett Packard Labs, Palo Alto, CA, USA. His research interests include photonic component design and automation of test photonic devices.

**M. Ashkan Seyedi** received the dual bachelors degrees in electrical and computer engineering from the University of Missouri, Columbia, MO, USA and the Ph.D. degree from the University of Southern California, Los Angeles, CA, USA, working on photonic crystal devices, high-speed nanowire photodetectors, efficient white LEDs, and solar cells. While with Hewlett Packard Enterprise as a Research Scientist, he has been working on developing high-bandwidth, efficient optical interconnects for exascale and high-performance computing applications.

**Marco Fiorentino** (Senior Member, OSA) received the Ph.D. degree in physics from the University of Napoli, Naples, Italy in 2000, working on quantum optics. He is a Distinguished Technologist with the Systems Architecture Laboratory, HPE Labs, Palo Alto, CA, USA. Before joining HPE Labs in 2005, he worked at Northwestern University, University of Rome, Roma, Italy and Massachusetts Institute of Technology, Cambridge, MA, USA. In the past he has worked on optics, high precision measurements, and optical communications. He has authored or coauthored more than 60 papers in peer-reviewed journals and given numerous contributed and invited talks to international conferences. He is a Senior Member of the Optical Society of America.

**Raymond G. Beausoleil** (Fellow, OSA) received the B.S. degree from Caltech, Pasadena, CA, USA, in 1980, and the Ph.D. degree from Stanford University, Stanford, CA, USA, in 1986, both in physics. He is currently an HPE Senior Fellow with the System Architecture Laboratory, Hewlett Packard Labs, Palo Alto, CA, USA, where he leads the Large-Scale Integrated Photonics Research Group. He has authored or coauthored more than 400 papers and conference proceedings (including many invited papers and plenary/keynote addresses) and five book chapters. He has more than 150 patents issued, and more than four dozen pending. Prior to HPE, his research was focused on high-power all-solid-state laser and nonlinear optical systems, as well as numerical algorithms for computer firmware (leading to the navigation algorithms for the optical mouse). At Hewlett Packard Labs, he performs basic and applied research in microscale and nanoscale classical and quantum optics for information processing technologies. He is an Adjunct Professor of Applied Physics with Stanford University, and is a Fellow of the American Physical Society and the Optical Society of America.

**Kwang-Ting Cheng** (Fellow, IEEE) received the Ph.D. degree in electrical engineering and computer sciences from the University of California, Berkeley, CA, USA, in 1988. He is the Dean of Engineering with the Hong Kong University of Science and Technology (HKUST) Hong Kong, in concurrence with his appointment as a Chair Professor jointly with the Department of Electronic and Computer Engineering and with the Department of Computer Science and Engineering. Before joining HKUST, he was a Professor with Electrical and Computer Engineering, the University of California, Santa Barbara (UCSB), CA, USA, where he had been serving since 1993. Prior to UCSB, he spent five years, at AT&T Bell Laboratories. He has been very active in providing professional services to the IEEE and to the academic community at large. He was the Editor-In-Chief of IEEE Design & Test of Computers, on the boards of the IEEE Council on Electronic Design Automations Board of Governors and the IEEE Computer Society's Publications Board, and on various technology advisory or working groups including the International Technology Roadmap for Semiconductors (ITRS).