

Highly Uniform Thermally Undercut Silicon Photonic Devices in a 300 mm CMOS Foundry Process

Robert Parsons¹, Kaylx Jang¹, Yuyang Wang¹, Asher Novick¹, A. Matthew Smith², Christopher C. Tison², Yonas Gebregiorgis³, Venkatesh Deenadayalan³, Matthew van Niekerk³, Lewis Carpenter⁴, Tat Ngai⁴, Gerald Leake⁴, Daniel Coleman⁴, Xiang Meng¹, Stefan Preble³, Michael L. Fanto², Keren Bergman¹, and Anthony Rizzo^{2,5,*}

¹Department of Electrical Engineering, Columbia University, New York, NY 10027, USA

²Air Force Research Laboratory Information Directorate, Rome, NY 13441, USA

³Electrical and Microelectronic Engineering, Rochester Institute of Technology, Rochester, NY 14623, USA

⁴American Institute for Manufacturing Integrated Photonics (AIM Photonics), Albany, NY 12203, USA

⁵Thayer School of Engineering, Dartmouth College, Hanover, NH 03755, USA

*anthony.j.rizzo@dartmouth.edu

ABSTRACT

Silicon photonic devices fundamental to high-density wavelength-division multiplexed (DWDM) optical links and photonic switching networks, such as resonant modulators and Mach-Zehnder interferometers (MZIs), are highly sensitive to fabrication variations and operational temperature swings. However, thermal tuning to compensate for fabrication and operational temperature variations can result in prohibitive power consumption, challenging the scalability of energy-efficient photonic integrated circuits (PICs). In this work, we develop and demonstrate a wafer-scale thermal undercut process in a 300 mm complementary metal oxide semiconductor (CMOS) foundry that dramatically improves the thermal isolation of thermo-optic devices by selectively removing substrate material beneath the waveguides and resonators. This approach significantly reduces the power required for thermal tuning across multiple device architectures, achieving almost a 5× improvement in tuning efficiency in a state-of-the-art 4.5 μm radius microdisk modulator and a 40× improvement in efficiency for a MZI phase shifter. To the best of the authors' knowledge, we demonstrate the first wafer-scale comparison of non-undercut and undercut silicon photonic devices using comprehensive wafer-scale measurements across 64 reticles of a 300 mm silicon-on-insulator (SOI) wafer. Further, we demonstrate a comprehensive wafer-scale analysis of the influence of undercut trench opening geometry on device tuning efficiency. Notably, we observe highly uniform performance across the full 300 mm wafer for multiple device types, emphasizing that our process can be scaled to large-scale photonic circuits with high yield. These results open new opportunities for large-scale integrated photonic circuits using thermo-optic devices, paving the way for scalable, low-power silicon photonic systems.

Introduction

Silicon photonic devices, such as resonant modulators, resonant filters, and Mach-Zehnder interferometers (MZIs), are foundational elements in dense wavelength-division multiplexed (DWDM) optical links and photonic switching systems due to their compact size, high-speed operation, and low energy consumption^{1–10}. These devices leverage silicon's strong thermo-optic effect for efficient tuning and configurability, making them highly attractive for large-scale photonic integrated circuits (PICs) in data centers and high-performance computing (HPC) environments¹¹. Static fabrication variations and dynamic temperature variations can significantly shift the optical properties of these devices, necessitating the use of integrated micro-heaters to stabilize and tune their performance¹². As silicon photonics scales towards dense integration with electronic components in co-packaged optical interconnects, the demand for precise thermal tuning increases. While some resonant modulators with high electro-optic tuning abilities^{13,14} have been proposed to reduce the reliance on thermal tuning, their tuning range is below what is required for realistic temperature swings in co-packaged interconnects. Trimming the refractive index of devices post-fabrication has also been proposed¹⁵, which compensates for fabrication variations, but does not solve the challenge of large temperature swings within the package. Therefore, thermal tuning of these devices is still required. However, conventional thermal tuning approaches, which require constant heating to counter localized temperature swings, impose a high power consumption burden. For instance, micro-heaters in resonant modulators can consume up to 25 mW P_π, which is unsustainable for energy-efficient DWDM links and switching networks, where minimizing energy per bit is a critical requirement^{16–18}. Reducing the energy consumption of these thermal tuning elements is essential for enabling scalable, low-power photonic systems^{19,20}.

In this work, we address the challenge of thermal management and energy reduction by introducing a selective thermal substrate undercut technique across a range of key silicon photonic devices, including microdisk modulators, microring & racetrack modulators, and linear thermo-optic phase shifters in MZIs. These devices, widely used for modulation, wavelength multiplexing, and switching, all rely on thermal tuning for stable operation²¹. By selectively removing the substrate material beneath the waveguides and resonators, the thermal undercut creates a region of enhanced thermal isolation, which significantly reduces the power required for thermo-optic tuning. This approach improves thermal efficiency while maintaining the performance and compactness of the devices. Previous demonstrations of thermal undercut show ample improvements in thermo-optic tuning efficiency, however these demonstrations have the disadvantages of requiring backside etching²², low-volume electron-beam lithography^{23,24}, or not achieving full release from the substrate²⁵. Recent foundry-supported thermal undercut demonstrations yield moderate improvement factors, limited by the sealing of the undercut^{26,27}. Substrate undercut has also been applied to other contexts, including enabling integrated photonic MEMS²⁸.

Resonant modulators, which are crucial for high-speed modulation in DWDM systems due to their inherent wavelength selectivity, benefit from reduced tuning power with the thermal undercut technique. We apply the wafer-scale thermal undercut to microring modulators, racetrack-style ring modulators, and state-of-the-art vertical junction microdisk modulators. Our experimental results demonstrate significant gains in tuning efficiency, achieving almost a 5× improvement for the microdisk modulators, while maintaining CMOS-compatible drive voltages. Linear thermo-optic phase shifters in MZIs, crucial for interleaving, switching, and routing in photonic networks, exhibit even greater reductions in power consumption, with over 40× improvement in tuning efficiency with optimized trench geometries. We show large-scale uniformity in performance for each device type, exhibiting the robustness of the substrate removal process across full 300 mm wafers. Furthermore, we demonstrate the capability of arbitrarily defined undercut openings, providing room for future improvement in all designs with optimized opening geometry.

To the best of the authors' knowledge we present, for the first time, comprehensive wafer-scale comparisons of non-undercut and undercut silicon photonic devices across multiple device types and heater geometries. Additionally, we illustrate tuning efficiency trends of undercut microdisk modulators based on systematically varied undercut geometric parameters. By sweeping the dimensions and shapes of the undercut openings beneath these microdisk modulators, we observe that wider and more elongated trenches yield significantly improved thermal isolation and reduced power consumption. These measurements reveal the critical role of trench geometry in optimizing thermal performance, providing key insights for design strategies that maximize tuning efficiency across photonic systems. The reduction in power consumption achieved through this optimized undercut geometry has broad implications for DWDM links and other high-density photonic systems. In DWDM links, where minimizing power per channel is essential for scalability²⁹, the improved thermal efficiency allows for higher channel counts and lower energy-per-bit metrics, critical for data center and telecom applications. Similarly, in efficient large-scale photonic switching systems³⁰, the power savings gained through thermal undercut can alleviate the thermal load, enabling increased switching density with minimized power consumption.

Results

We design and demonstrate robust wafer-scale thermal undercut in collaboration with a 300 mm CMOS foundry³¹, ensuring that the process can extend to high-volume manufacturing. This thermal undercut process was designed to maintain full compatibility with the standard AIM Photonics Actives Process, as highlighted by the process cross section in Fig. 1a. As shown in Fig. 1b, design of experiment test structures with both circular and square trench geometries validate the ability to process a range of arbitrary shapes in a standard CMOS fabrication process. This flexibility is essential for optimizing thermal isolation across different device architectures and confirms the robustness of the undercut technique for varied applications. Comprehensive design rules ensure devices retain structural integrity when surrounded by undercut trenches. The thermal undercut process employed in this work involves selectively removing silicon substrate material³². This creates an air-filled trench that significantly enhances thermal isolation by lowering the effective thermal conductivity surrounding the active photonic device. Silicon, with a thermal conductivity of approximately 150 W/m·K^{33,34}, provides a highly conductive pathway for heat dissipation, causing significant thermal leakage from the micro-heater to the bulk substrate. Further, the buried oxide has a thermal conductivity of approximately 1.4 W/m·K^{35,36}, representing reduced thermal confinement. By introducing an undercut trench filled with air, which has a thermal conductivity of roughly 0.025 W/m·K³⁷, we reduce both heat dissipation pathways, effectively creating an insulating barrier around the device. This drastic reduction in thermal conductivity between the heater and the substrate allows the device to reach higher temperatures with lower input electrical power, significantly improving thermal tuning efficiency. Since the foundry process does not include a metal heater layer such as titanium nitride, we implement our resistive heaters using doped silicon in the silicon device layer (Fig. 1a). We use a suite of standard n-type and p-type ion-implanted doping layers³¹ to modulate the resistance of the silicon microheater and form ohmic contacts between the metal vias and silicon. Depending on the heater geometry (length, width, etc.) and the target resistance for the heater, we employ a mix of low, medium, and high doping levels ($\approx 1e18 \text{ cm}^{-3}$, $1e19 \text{ cm}^{-3}$, and $1e20 \text{ cm}^{-3}$, respectively). The metal vias

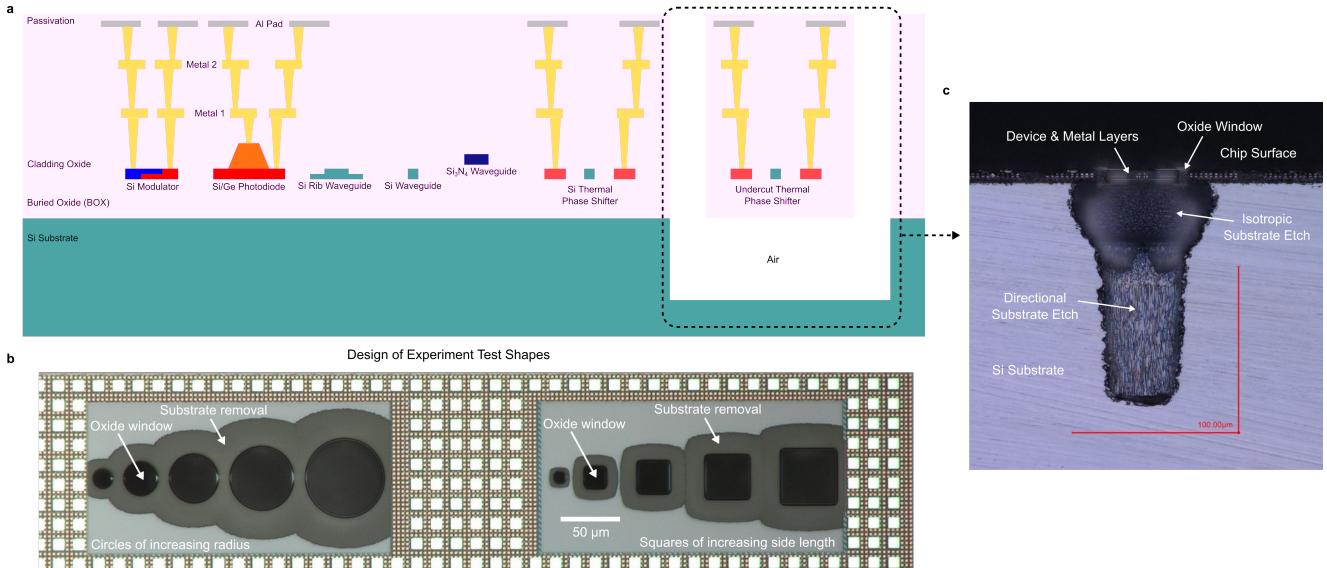


Figure 1. Fabrication process cross section and inspection of undercut design-of-experiment (DoE) structures.

a, Complete process cross-section of the AIM Photonics Active Process including silicon and silicon nitride waveguides, free carrier-based high-speed modulators, germanium photodiodes, and doped-silicon thermal phase shifters. This work extends the process to include undercut thermal phase shifters for higher energy efficiency (far right). **b**, Optical microscope image of design-of-experiment test structures to evaluate the lateral extent of the isotropic substrate removal etch. These shapes include circles of increasing radius (left) and squares of increasing side length (right). The dark black regions indicate the extent of the oxide window etch through the cladding and buried oxide (BOX), and the lighter gray regions indicate the lateral extent of the silicon substrate removal beyond the extent of the oxide window. These DoE structures additionally demonstrate the ability of our undercut fabrication process to extend to arbitrary trench shapes. **c**, Optical microscope image of the chip cross-section after mechanically dicing through the center of an undercut device. The key features of the undercut fabrication are visible in the micrograph including the cladding, device, and metal layers (top), the oxide windows exposing access to the substrate from the chip surface, the first isotropic substrate removal etch to form the undercut, and a final directional substrate etch that arises from the Bosch etch used to define deep trench facets for edge coupling.

and routing layers are fabricated using standard copper and aluminum back end of line (BEOL) processing³¹.

Thermal simulations³⁸ were performed for a microdisk modulator both with and without undercut to compare their transient thermal responses³⁹. The mask layout for a microdisk modulator surrounded by thermal undercut is shown in Fig. 2a. The comprehensive device design is detailed in ref.⁴⁰, and preliminary results of the undercut device are shown in ref.⁴¹. Although outside the scope of this work, recent improvements to the microdisk modulator RF contact geometry have yielded devices capable of 32 Gb/s on-off-keying non-return-to-zero (OOK-NRZ) transmission with low peak-to-peak driving voltages³. Simulations in which 1 mW of power was applied through the integrated micro-heater show a significantly higher temperature increase in the undercut microdisk compared to the nominal device, underscoring the enhanced thermal isolation achieved by the trench (Fig. 2d). This heightened temperature response for the same input power demonstrates the potential for lower power consumption, as less energy is required to reach the desired tuning temperatures in devices with thermal undercut. Additionally, transient thermal simulations were performed to provide insight into the dynamic response of the undercut device, revealing longer rise and fall times compared to the nominal device. Specifically, the nominal device had a rise time of 11.0 μ s and a fall time of 11.3 μ s, while introducing the undercut resulted in a rise time of 96.7 μ s and a fall time of 95.7 μ s. The approximately 8–9× slower heating and cooling transients are a result of the reduced thermal conductivity around the microdisk due to the air gap created by the undercut. This effect can be advantageous in applications where slower thermal responses improve stability by reducing sensitivity to temperature fluctuations.

Microdisk modulator test structures were measured across two 300 mm wafers. Two variants of the device were measured on each reticle: modulators both with and without thermal undercut. A micrograph of a microdisk modulator with thermal undercut is shown in Fig. 2c, which confirms that the device is fully released from the substrate. Further demonstrating the full release of the device, a micrograph of the side profile is shown in Fig. 1c. A dicing saw was used to make a precise cut close to the undercut modulator on a singulated die to enable capture of the cross-section. The optical spectrum of a nominal microdisk modulator without thermal undercut at different applied thermo-optic phase shifter powers showing the shift in resonance is displayed in Fig. 2e. A drastic increase in the resonance shift for similar applied powers is shown in Fig. 2f, where

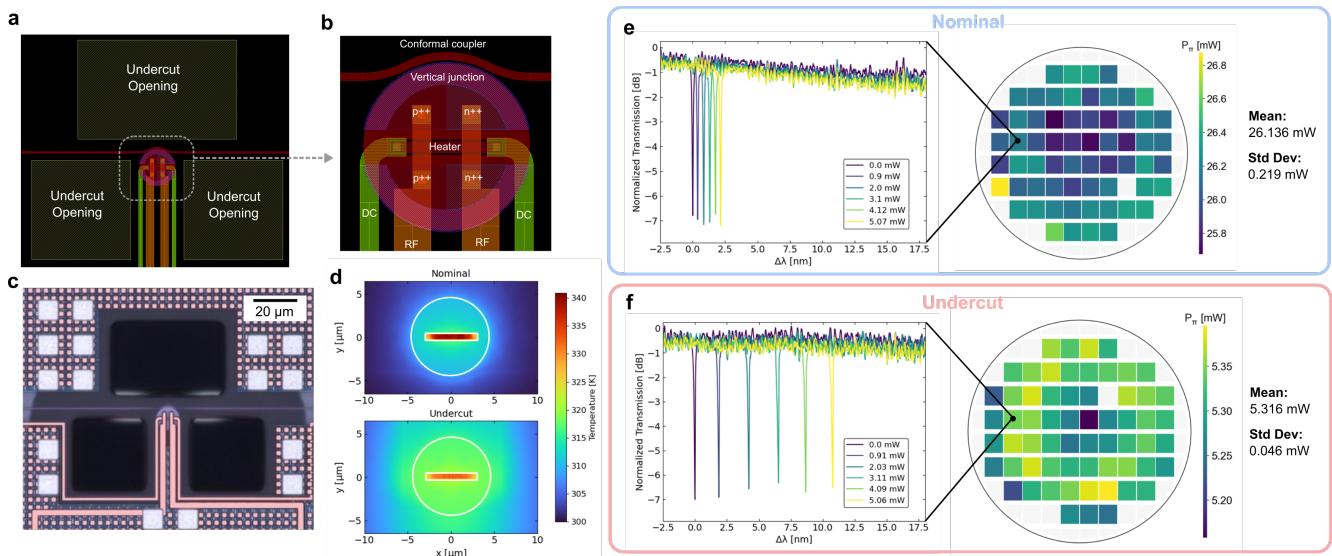


Figure 2. Undercut microdisk modulator wafer-scale thermo-optic measurements. **a**, Mask layout of the undercut microdisk modulator highlighting the layers for the directional oxide etch ('undercut opening'). **b**, Mask layout of the microdisk modulator highlighting the device geometry including the vertical junction doping around the disk perimeter, conformal phase-matched coupler for selective excitation of the fundamental mode, heavily doped contact regions with vias, and DC/RF metal traces. **c**, Micrograph of the fabricated device corresponding to the mask layout in **a**. **d**, Simulated temperature profile of the microdisk with (bottom) and without (top) undercut given 1 mW of power dissipated from the heater, showing a dramatic increase in the temperature throughout the disk for the same amount of applied power. **e**, Wafer map and representative thermal tuning spectrum for a nominal non-undercut device, showing the inter-reticle statistics across the full 300 mm wafer. **f**, Wafer map and representative thermal tuning spectrum for the undercut device, showing a dramatic improvement in P_π while maintaining consistent performance across the entire wafer.

the optical spectrum of a representative thermally undercut microdisk modulator is displayed. This large increase in tuning efficiency is additionally observed at the wafer-scale; the wafer maps are shown in Figs. 2e and 2f, showing the P_π of the nominal non-undercut and undercut microdisks, respectively. The P_π for the undercut microdisks is on average 5.316 mW with standard deviation 0.046 mW, which is an improvement of 4.92 as compared to the P_π of 26.136 mW with standard deviation 0.219 mW exhibited by the devices without undercut. Furthermore, these wafer-scale measurements confirm the structural integrity and high yield of the undercut devices.

To demonstrate the wide applicability of the undercut process, two other types of resonant modulators were fabricated, both with and without thermal undercut. The first device is a lateral junction microring modulator with a radius of 20 μm. The micrograph of this microring modulator with thermal undercut is shown in Fig. 3b. The thermo-optic phase shifter is located concentrically inside the ring. Trench openings were placed both inside and outside the microring and alongside the access waveguide, as shown in the schematic in Fig. 3a. The second device is a racetrack-style ring modulator; a micrograph of a representative device is shown in Fig. 3f. A linear thermo-optic phase shifter is located internal to the ring along the straight access section. The PN-junction for high-speed modulation is located along the opposite straight section. For this modulator design, trench openings were placed both internally and externally along the straight sections of the ring and alongside the access waveguide, as shown in the schematic in Fig. 3e. The P_π measured across a wafer is shown for the non-undercut microring modulator and racetrack ring modulator in Fig. 3c and Fig. 3g, respectively. The P_π wafer maps of the undercut microring and racetrack modulators are displayed in Fig. 3d and Fig. 3h, respectively. We observe an average tuning efficiency improvement of 25.1, from average P_π of 100.01 mW and standard deviation 4.46 mW without undercut to average P_π of 3.99 mW and standard deviation 0.05 mW with undercut for the microring modulator. In the case of the racetrack-style ring modulator, the tuning efficiency improvement on average is 48.1, from average P_π of 63.11 mW and standard deviation 3.43 mW without undercut to average P_π of 1.31 mW and standard deviation 0.01 mW with undercut. Both undercut devices exhibit drastic increases in tuning efficiency, indicating full release from the substrate.

While all the fully-released undercut resonant devices show substantial improvements in tuning efficiency, the improvement factor is more pronounced for less efficient thermo-optic phase shifter designs. The baseline tuning efficiencies of the microring and racetrack modulators without undercut have P_π values of 100.01 mW and 63.11 mW, respectively. In comparison, the already relatively efficient microdisk modulator exhibits a P_π of 26.136 mW without undercut. The higher baseline efficiency

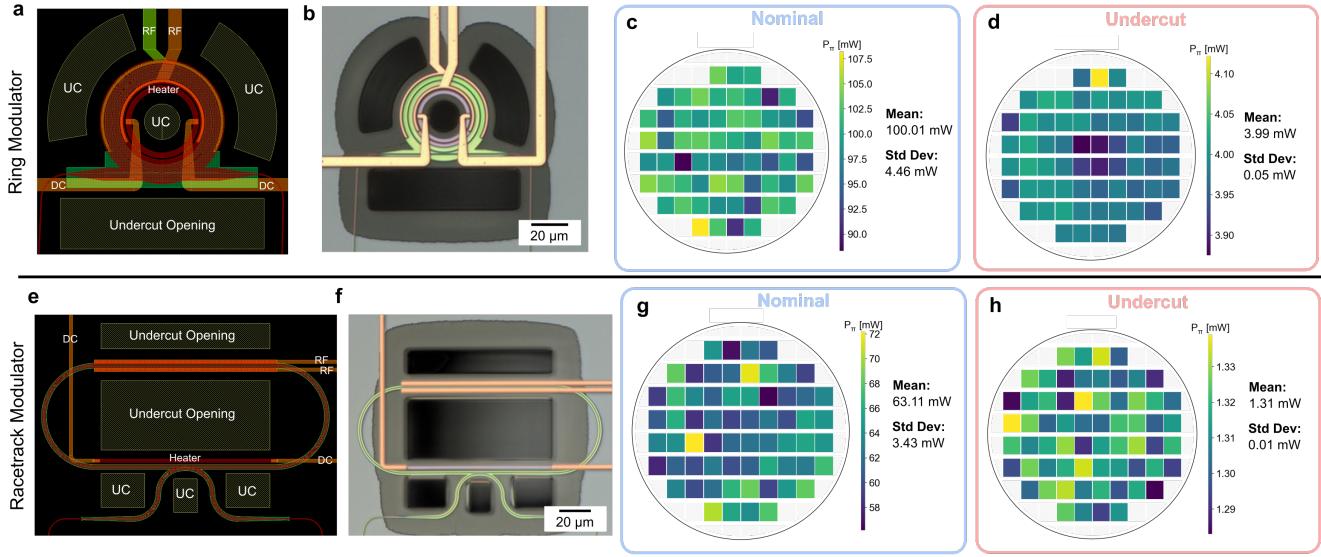


Figure 3. Undercut microring and racetrack modulator wafer-scale thermo-optic measurements. **a**, Mask layout of the microring modulator highlighting the location of the undercut trench openings, interior doped silicon heater, high speed RF traces, and DC heater traces. **b**, Corresponding micrograph of undercut microring modulator. **c**, Wafer map of thermal tuning power required for a π phase shift (P_π) of the nominal microring modulator. **d**, Wafer map of P_π for the undercut microring modulator, showing a dramatic decrease relative to the nominal design. **e**, Mask layout of the racetrack modulator highlighting the location of the undercut trench openings, interior doped silicon heater, high speed RF traces, and DC heater traces. **f**, Corresponding micrograph of undercut racetrack modulator. **g**, Wafer map of P_π for the nominal racetrack modulator. **h**, Wafer map of P_π for the undercut racetrack modulator, showing a dramatic decrease relative to the nominal design.

of the microdisk can be attributed to its integrated thermo-optic phase shifter, which is surrounded by only a thin 100 nm oxide layer for electrical isolation⁴². The proximity of the phase shifter to the optical mode, with silicon as the dominant material between them, ensures effective thermal conduction due to silicon's higher thermal conductivity compared to oxide. In contrast, the thermo-optic phase shifters in the microring and racetrack modulators are positioned farther from the optical mode, separated by a larger oxide gap. This separation significantly reduces thermal efficiency and confinement in these devices compared to the microdisk. As a result, the microring and racetrack modulators benefit more, relatively speaking, from the enhanced thermal isolation provided by the substrate undercut, achieving greater improvement factors in tuning efficiency. Consequently, more conservative phase shifter designs, such as those designed to incur negligible optical loss, can still achieve state-of-the-art tuning efficiency once undercut.

In addition to resonant devices, we designed and fabricated linear thermo-optic phase shifters both with and without undercut. The mask layout and a representative micrograph of the phase shifter with undercut are shown in Figs. 4a and 4b and Fig. 4c, respectively. The phase shifter consists of two doped silicon strips parallel to the waveguide. These doped silicon strips are placed at a distance away from the optical mode to avoid excess optical losses, resulting in the insertion loss being dominated by the intrinsic waveguide propagation loss. A 125 μm device length and 2 dB/cm propagation loss yields a total insertion loss of 0.025 dB. To extract the tuning efficiency of the phase shifter, it was placed within an imbalanced MZI so the interference fringes could be tracked at varying heater powers. The transmission spectrum of the MZI without undercut and with undercut under different applied heater powers is shown in Fig. 4e and Fig. 4f, respectively. The undercut phase shifter requires significantly less power to induce a larger shift in interference fringe wavelength. This is demonstrated in the wafer maps showing P_π for the phase shifters without undercut and phase shifters with undercut in Fig. 4e and Fig. 4f, respectively. An improvement factor of 40.5 is shown, moving from a non-undercut average P_π of 43.46 mW and standard deviation 0.94 mW to an average P_π of 1.07 mW and standard deviation 0.01 mW for the undercut device. To characterize the time-dependent transient effects of substrate undercut on thermal modulation, we apply a square wave to the phase shifter. The transient is shown for both the nominal and undercut phase shifter in Fig. 4d (top and bottom, respectively). A pulse width of 100 μs was applied to the non-undercut device, resulting in a rise time of 12.6 μs and a fall time of 25.3 μs . For the undercut device, a pulse width of 10 ms was used, resulting in a rise time of 1.853 ms and a fall time of 1.258 ms. The increase in rise/fall time has implications on the performance of these phase shifters in the context of optical switches and multiplexers. For instance, the increase in rise/fall time results in a slower optical switching speed. However, the reduced switching speed disadvantage is

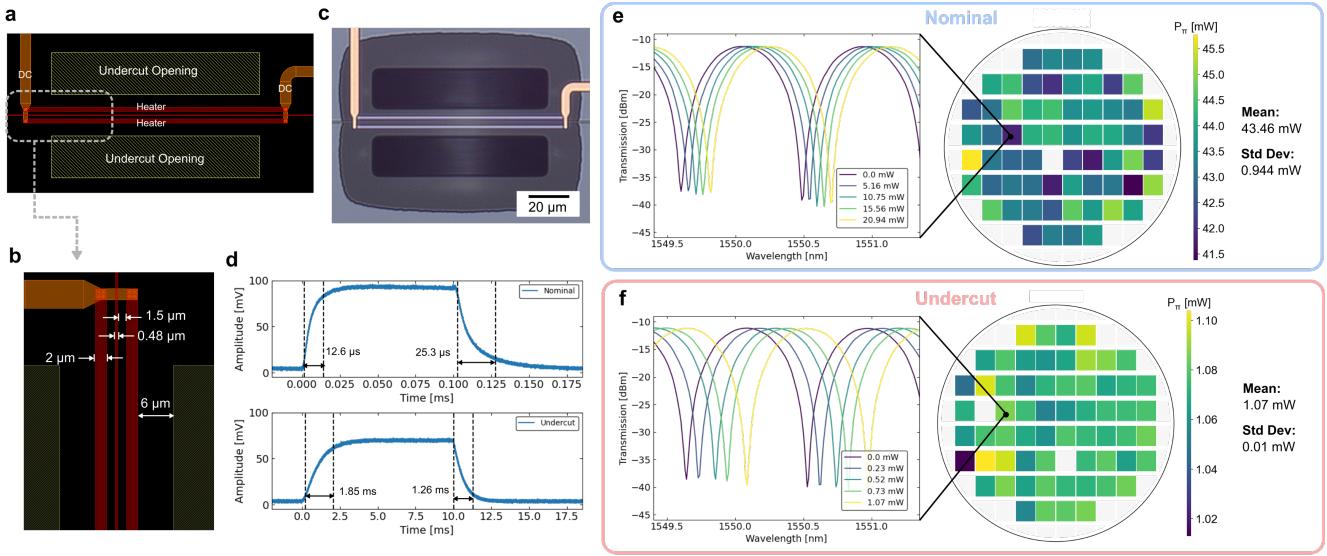


Figure 4. Undercut linear thermo-optic phase shifter wafer-scale measurements. **a**, Mask layout of the undercut linear thermo-optic phase shifter highlighting the location of the undercut trench openings, doped silicon heaters on both sides of the waveguide, and DC heater traces. **b**, Zoomed view of the mask layout showing the dimensions of the waveguide width (0.48 μm), heater separation from the waveguide (1.5 μm), heater width (2 μm), and heater separation from the undercut trench openings (6 μm). **c**, Corresponding micrograph of the undercut thermo-optic phase shifter. **d**, Heater response to a square wave drive signal applied to the heater anode and cathode terminals, highlighting the rise and fall times for the nominal (top) and undercut (bottom) devices. The extreme thermal isolation of the undercut devices results in dramatically longer thermal time constants. **e**, Wafer map of P_π and representative thermal tuning spectrum for the nominal linear thermo-optic phase shifter, **f**, Wafer map of P_π and representative thermal tuning spectrum for the undercut linear thermo-optic phase shifter.

mostly negated if the network topology is configured before application runtime^{43,44}. Further, the increase in rise/fall time can be leveraged when considering time-multiplexed driving signals for many thermo-optic phase shifters to reduce electrical I/O⁴⁵.

To elucidate the impact of undercut geometry on the tuning efficiency of devices, we swept the undercut geometric parameters across a number of microdisk modulator devices. A micrograph of the test structure sweep of undercut microdisk modulators is shown in Fig. 5a. While keeping the microdisk modulator design constant for all cases, both the undercut opening size and separation were varied according to the schematic in Fig. 5b. The tuning efficiency of each microdisk modulator in the undercut parameter sweep was extracted across two full wafers. The tuning efficiency of each modulator in the parameter sweep, averaged across the first wafer, is shown in Figs. 5c and 5d, where the top trench length is 20 and 40 μm , respectively. Similarly, the tuning efficiencies of the modulators from the second full wafer are shown in Figs. 5e and 5f. First, there is a clear trend in increased tuning efficiency (reduced P_π) in all cases as the trench width is increased from 10 μm to 25 μm . The larger trench opening increases the lateral undercut, ensuring the devices are fully released from the substrate. However, we see diminishing returns when increasing the trench width from 20 μm to 25 μm , suggesting the tuning efficiency of the devices is dominated by the volume of remaining buried oxide and substrate contacting the bottom of the device. Additionally, there is a trend in increased P_π when the trench separation is increased, which corresponds to wider oxide bridges between the trench openings. This trend explains the limited gains in tuning efficiency seen in processes using a sealed substrate undercut^{26,27,46}; heat from the phase shifter is less confined to the device without the trench openings. Another notable trend is the marked consistency and uniformity in tuning efficiency of the undercut modulators between both wafers, demonstrating the mechanical robustness and reliability of the substrate removal process. Only when aggressively pushing the boundaries of trench separation far beyond the foundry design rules do we see mechanical damage to the bus waveguide and metal traces. Using Fig. 5b as a reference, we observed mechanical damage at a trench separation (TS) of 1 μm , but observed no damage and high mechanical stability at a trench separation of at least 2 μm .

The small size of microdisk modulators causes strong light confinement, leading to high optical power density and nonlinear effects like thermal bistability⁴⁷. Thermal isolation exacerbates this by trapping heat in the microdisk, complicating high-power management in resonant modulators⁴⁸. We studied the effects of high optical power in thermally undercut microdisk modulators, and thermal instability even at -14 dBm input power is observed⁴⁹. The modulator is thermally isolated using wafer-scale undercut, shown in Fig. 6a. We examined electro-optic modulation of the PN-junction at varying laser powers. At low input laser power (-17.5 dBm), the DC spectral response showed a modulation efficiency of 65 pm/V under bias voltages from

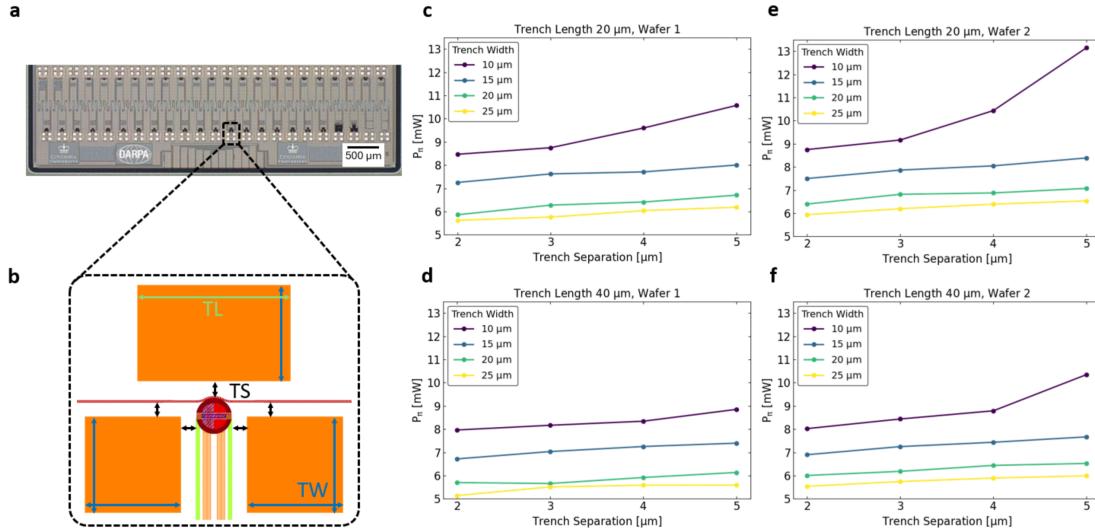


Figure 5. Influence of undercut geometry on device thermo-optic performance. **a**, Optical microscope image of the undercut microdisk modulator test structures with parameter sweeps of opening geometry. **b**, Schematic layout of the microdisk modulator with undercut openings illustrating the swept design parameters. TS: trench separation; TL: trench length; TW: trench width. **c-f**, Average tuning power required for π phase shift over varying trench width and trench separation with trench length of 20 μm on first wafer (**c**), trench length of 40 μm on first wafer (**d**), trench length of 20 μm on second wafer (**e**), trench length of 40 μm on second wafer (**f**).

0.5 V to -2.5 V (Fig. 6b). However, increasing laser power caused nonlinear spectral shifts with resonance red-shifting and broadening due to thermal instability, as shown in Fig. 6c⁵⁰. Near-resonance laser light is partially absorbed via two-photon and free-carrier absorption, generating heat. This effect is enhanced by the thermal isolation of the undercut structure, leading to significant thermal instability at laser optical powers as low as -14 dBm (Fig. 6d).

Despite this, robust high-speed modulation was achievable over a broad spectral range at higher powers, up to -4 dBm. Thermally-induced resonance red-shifting enabled modulation over a range $6\times$ wider than the resonator's passive linewidth. We present an experimental investigation of optical modulation in thermally undercut microdisk modulators, focusing on the advantages of optically induced thermal nonlinearity. As laser power increases, the spectral shift of the resonator becomes nonlinear, accompanied by a redshift and resonance broadening due to thermal instability. We also explored the modulation behavior across varying operating frequencies and input optical powers. A 2 V peak-to-peak square wave was applied at different frequencies, and the peak-to-peak optical modulation was measured and normalized to compare modulation depths. Across all modulation frequencies, the spectral range broadens with increased laser power. However, at low frequencies (<1 MHz, Fig. 6e), although the spectral range expands, the peak-to-peak modulation decreases at higher laser powers, likely due to the device's thermal response. In contrast, at higher data frequencies (>25 MHz, Figs. 6f-h), the modulation depth remains stable as laser power increases, achieving modulation over a spectral range six times broader than the resonator's linewidth at an optical power of -4 dBm. Therefore, at high data rates, the device's thermal sensitivity becomes a beneficial nonlinear effect, enabling robust modulation across a wide spectral range. Thermal isolation thus enhances modulation efficiency and reduces micro-heater tuning requirements.

Discussion

In conclusion, we developed and experimentally verified a wafer-scale thermal undercut process in a 300 mm CMOS foundry applied to a range of fundamental silicon photonic devices with state-of-the-art performance and yield. We show an excellent $40\times$ improvement in tuning efficiency of linear thermo-optic phase shifters with undercut, enabling a drastic reduction in power consumption of large-scale silicon photonic circuits. Undercut microring and racetrack-style modulators also exhibit high tuning efficiency, owing to their ability to accommodate both larger and elongated external trench openings along with an internal trench opening. Further, we apply the developed undercut etch to state-of-the-art microdisk modulators, achieving an almost $5\times$ improvement in tuning efficiency. These efficiently tunable compact vertical-junction microdisk modulators with high modulation efficiency are fully compatible with CMOS driving voltages, enabling scalable, ultra efficient DWDM links. Through comprehensive wafer-scale measurements comparing nominal non-undercut and undercut devices, we show high

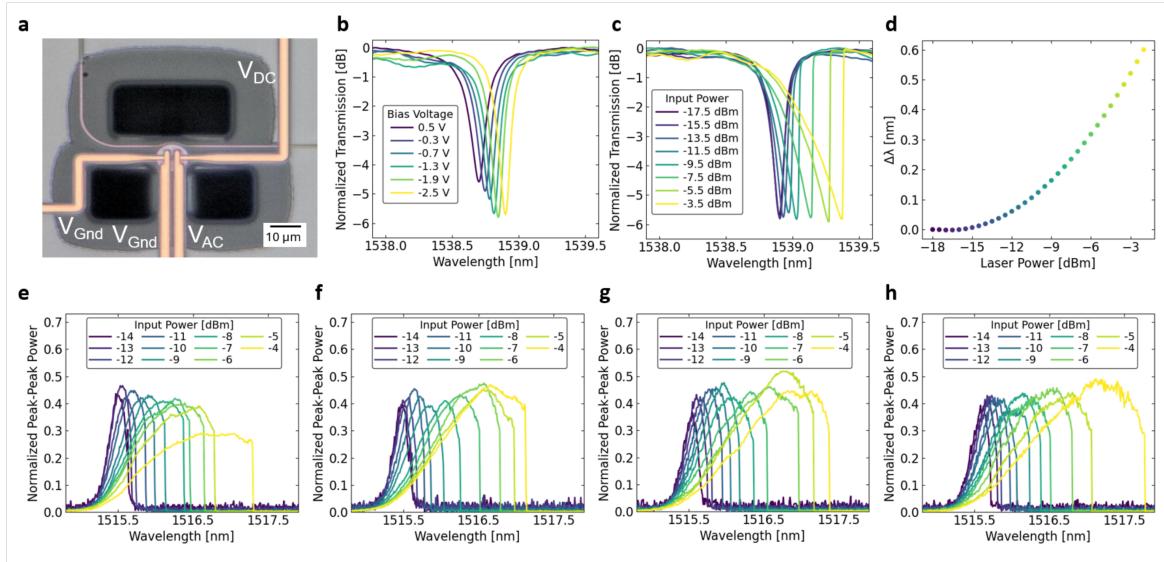


Figure 6. Nonlinear spectral shifts in undercut microdisk modulator. **a**, Optical microscope image of the undercut resonant device with heater and RF electrical inputs annotated. **b**, Electro-optic depletion response of the device, swept from 0.5 V to -2.5 V at low optical power (-17.5 dBm). **c**, Transmission spectrum of the device with fixed -2.5 V DC bias and increasing laser powers. **d**, Induced spectral shift due to input optical power. **e-h**, Modulation at different input optical powers and modulation frequencies of **(e)** 1 MHz, **(f)** 50 MHz, **(g)** 300 MHz, and **(h)** 600 MHz.

uniformity in P_π across entire 300 mm wafers, indicating high yield and reproducibility for the developed process. Notably, we observe that high nominal power consumption (large P_π) can be largely offset by thermally undercutting the device, greatly relaxing the heater design requirements and allowing the heater to be placed far from the optical mode.

Furthermore, by systematically varying the undercut trench geometry and measuring tuning efficiencies across multiple full wafers of microdisk modulators, we identified key trends that reveal how trench dimensions impact thermal tuning efficiency. Wider and more elongated trenches consistently provide improved thermal isolation, resulting in significant reductions in the power required for thermal tuning. Further, reduced trench separation also resulted in higher tuning efficiency. This finding suggests that trench geometry optimization can serve as a powerful design parameter for further minimizing power consumption in future device designs. By establishing predictable efficiency gains based on trench geometry, we provide a robust framework for integrating thermal undercut as a standardized process across different CMOS fabrication lines, ensuring reproducibility and consistency at the scale required for high-volume production. This level of scalability is critical for enabling low-cost, high-throughput manufacturing of photonic integrated circuits where consistent thermal performance is essential.

Methods

Thermal Undercut Fabrication Process

The thermal undercut fabrication process is run on a 300 mm, CMOS compatible, silicon photonic process³¹. The thermal undercut is run within the back-end-of-line (BEOL) giving it flexibility to be used with photonic, electronic and optoelectronic devices. The undercut can be combined with optical facets and waveguide access via trenches to both silicon and silicon nitride layers. The process consists of two primary steps: 1) silica and 2) silicon etching to ensure efficient and controlled reactive ion etching (RIE) of the different materials. Within each step photolithography is used to define the thermal undercut opening, a ~10 μm photoresist is spun, baked, and exposed using i-line photolithography. Careful optimization of the thermal undercut opening sizes (Fig. 5b TW and TL) and the proximity to the device (Fig. 5b TS) is used to ensure RIE does not damage waveguides or metallization. The RIE etches of both the silica and silicon portion are closely monitored to ensure undercutting of optical facets does not happen and optical facets are produced with smooth straight surfaces.

Wafer-scale Measurements

All optical measurements were taken using a ficonTEC TL1200 Wafer-Level and Component-Level Tester⁵¹. The wafer-level tester, with a temperature-controlled chuck, two six-axis stages with optical probes, and two five-axis stages with electrical probes, enables comprehensive wafer-scale measurements. Three dies per reticle, across 64 reticles, were measured to

characterize a variety of silicon photonic devices both with and without thermal undercut. The first die contains many grating-coupled microdisk modulators with a sweep of undercut opening geometric parameters. An angled fiber array was coupled to each microdisk modulator with an automated alignment process, and simultaneously multi-contact DC electrical probes were landed to control the integrated thermo-optic phase shifter. A high-precision DC power supply (Keithley 2280S-32-6) was used to bias the thermo-optic phase shifter. After tuning the polarization to select for the fundamental transverse-electric (TE) mode with an internal polarization controller (Thorlabs MPC320), a tunable laser source (Keysight 81608A), lightwave measurement system (Keysight 8164B), and optical power meter (Keysight N7744A) were used to sweep the optical spectrum of each device at each phase shifter bias point.

A lidless periscope fiber array was used to edge-couple to the microring modulators, racetrack modulators, and imbalanced Mach Zehnder interferometers (MZIs) on the other two dies on each reticle. The periscope fiber arrays, manufactured by Keystone Photonics, enable wafer-scale low-loss edge-coupling by extending 3D-printed optics into the dicing trench⁵². Following edge-coupling, the optical spectra of each device at different thermo-optic phase shifter bias points were measured using the same methodology as the microdisk modulators. In total, two wafers without thermal undercut were measured, and two wafers with thermal undercut were measured.

The tuning efficiency of each device was calculated by finding the resonance or interference fringe shift at each thermo-optic phase shifter bias point. A peak-finding algorithm was used to find the resonance or fringe wavelength from each optical spectrum sweep. Together with the recorded electrical power dissipated in the thermo-optic phase shifter and the measured free spectral range, the P_π , i.e. the power required for a phase shift of π , was calculated for each device.

The transient responses of the microdisk modulator and imbalanced MZI were measured both with and without thermal undercut. A tunable laser was aligned to the wavelength of the resonance and interference fringe of the microdisk and MZI, respectively. Next, the optical output was switched to a photodiode (Thorlabs PDA10CS), connected to an oscilloscope (Tektronix MSO5204B) set to trigger on the rising edge. An arbitrary function generator (Keithley 3390) was used to send a square wave to the thermo-optic phase shifter, with the resultant transient captured by the oscilloscope. The rise and fall times of each device were extracted by finding the 10% and 90% thresholds of each optical transient.

References

1. Bogaerts, W. *et al.* Silicon microring resonators. *Laser & Photonics Rev.* **6**, 47–73 (2012).
2. Chen, C.-H. *et al.* A comb laser-driven DWDM silicon photonic transmitter based on microring modulators. *Opt. Express* **23**, 21541 (2015).
3. Novick, A., Wang, S., Rizzo, A., Gopal, V. & Bergman, K. Ultra-efficient interleaved vertical-junction microdisk modulator with integrated heater. In *Optical Fiber Communication Conference*, W2A–21 (Optica Publishing Group, 2024).
4. Parsons, R. *et al.* Efficient silicon photonic add-drop microdisk filters for dwdm systems. In *CLEO: Science and Innovations*, JW2A–127 (Optica Publishing Group, 2023).
5. Manganelli, C. L. *et al.* Large-fsr thermally tunable double-ring filters for wdm applications in silicon photonics. *IEEE Photonics J.* **9**, 1–10 (2017).
6. Luo, L.-W. *et al.* High bandwidth on-chip silicon photonic interleaver. *Opt. Express* **18**, 23079 (2010).
7. Horst, F. *et al.* Cascaded Mach-Zehnder wavelength filters in silicon photonics for low loss and flat pass-band WDM (de-)multiplexing. *Opt. Express* **21**, 11652 (2013).
8. Espinola, R., Tsai, M., Yardley, J. & Osgood, R. Fast and low-power thermooptic switch on thin silicon-on-insulator. *IEEE Photonics Technol. Lett.* **15**, 1366–1368 (2003).
9. Lee, B. G. & Dupuis, N. Silicon photonic switch fabrics: Technology and architecture. *J. Light. Technol.* **37**, 6–20 (2018).
10. Huang, Y., Cheng, Q., Rizzo, A. & Bergman, K. Push—pull microring-assisted space-and-wavelength selective switch. *Opt. Lett.* **45**, 2696–2699 (2020).
11. Rizzo, A. *et al.* Massively scalable kerr comb-driven silicon photonic link. *Nat. Photonics* **17**, 781–790 (2023).
12. Rizzo, A. *et al.* Fabrication-robust silicon photonic devices in standard sub-micron silicon-on-insulator processes. *Opt. Lett.* **48**, 215–218 (2023).
13. Timurdogan, E. *et al.* An ultralow power athermal silicon modulator. *Nat. communications* **5**, 1–11 (2014).
14. Gevorgyan, H., Khilo, A., Wade, M. T., Stojanović, V. M. & Popović, M. A. Miniature, highly sensitive moscap ring modulators in co-optimized electronic-photonic cmos. *Photonics Res.* **10**, A1–A7 (2022).
15. Jayatilleka, H. *et al.* Post-fabrication trimming of silicon photonic ring resonators at wafer-scale. *J. Light. Technol.* **39**, 5083–5088 (2021).

16. Masood, A. *et al.* Comparison of heater architectures for thermal control of silicon photonic circuits. In *10th International Conference on Group IV Photonics*, 83–84 (IEEE, 2013).
17. Jacques, M. *et al.* Optimization of thermo-optic phase-shifter design and mitigation of thermal crosstalk on the soi platform. *Opt. express* **27**, 10456–10471 (2019).
18. Liu, S. *et al.* Thermo-optic phase shifters based on silicon-on-insulator platform: state-of-the-art and a review. *Front. Optoelectronics* **15**, 9 (2022).
19. Zortman, W. A., Trotter, D. C. & Watts, M. R. Silicon photonics manufacturing. *Opt. express* **18**, 23598–23607 (2010).
20. Wang, Y. *et al.* Co-designed silicon photonics chip i/o for energy-efficient petascale connectivity. *IEEE Transactions on Components, Packag. Manuf. Technol.* (2024).
21. Padmaraju, K. & Bergman, K. Resolving the thermal challenges for silicon microring resonator devices. *Nanophotonics* **3**, 269–281 (2014).
22. Cunningham, J. E. *et al.* Highly-efficient thermally-tuned resonant optical filters. *Opt. express* **18**, 19055–19063 (2010).
23. Dong, P. *et al.* Thermally tunable silicon racetrack resonators with ultralow tuning power. *Opt. express* **18**, 20298–20304 (2010).
24. Sun, P. & Reano, R. M. Submilliwatt thermo-optic switches using free-standing silicon-on-insulator strip waveguides. *Opt. express* **18**, 8406–8411 (2010).
25. Fang, Q. *et al.* Ultralow power silicon photonics thermo-optic switch with suspended phase arms. *IEEE Photonics Technol. Lett.* **23**, 525–527 (2011).
26. Giewont, K. *et al.* 300-mm monolithic silicon photonics foundry technology. *IEEE J. Sel. Top. Quantum Electron.* **25**, 1–11 (2019).
27. Fang, Y. *et al.* Comparison of thermo-optic phase shifters in imec’s silicon photonics platform. In *European Conference on Integrated Optics*, 337–342 (Springer, 2024).
28. Jo, G. *et al.* Wafer-level hermetically sealed silicon photonic mems. *Photonics Res.* **10**, A14–A21 (2022).
29. Wang, Y. *et al.* Silicon photonics chip i/o for ultra high-bandwidth and energy-efficient die-to-die connectivity. In *2024 IEEE Custom Integrated Circuits Conference (CICC)*, 1–8 (IEEE, 2024).
30. Tu, X., Song, C., Huang, T., Chen, Z. & Fu, H. State of the art and perspectives on silicon photonic switches. *Micromachines* **10**, 51 (2019).
31. Fahrenkopf, N. M. *et al.* The aim photonics mpw: A highly accessible cutting edge technology for rapid prototyping of photonic integrated circuits. *IEEE J. Sel. Top. Quantum Electron.* **25**, 1–6 (2019).
32. van Niekerk, M. *et al.* Wafer-scale-compatible substrate undercut for ultra-efficient soi thermal phase shifters. In *2022 Conference on Lasers and Electro-Optics (CLEO)*, 1–2 (IEEE, 2022).
33. Shanks, H., Maycock, P., Sidles, P. & Danielson, G. Thermal conductivity of silicon from 300 to 1400 k. *Phys. Rev.* **130**, 1743 (1963).
34. Slack, G. A. Thermal conductivity of pure and impure silicon, silicon carbide, and diamond. *J. Appl. physics* **35**, 3460–3466 (1964).
35. Cahill, D. G. Thermal conductivity measurement from 30 to 750 k: the 3ω method. *Rev. scientific instruments* **61**, 802–808 (1990).
36. Grove, A. S. *Physics and technology of semiconductor devices* (Wiley, 1967).
37. Stephan, K. & Laesecke, A. The thermal conductivity of fluid air. *J. physical chemical reference data* **14**, 227–234 (1985).
38. Coenen, D. *et al.* Thermal modelling of silicon photonic ring modulator with substrate undercut. *J. Light. Technol.* (2022).
39. Ansys Lumerical. 3d heat transport simulator. <https://www.ansys.com/products/optics/multiphysics> (2024).
40. Rizzo, A. *et al.* Petabit-scale silicon photonic interconnects with integrated kerr frequency combs. *IEEE J. Sel. Top. Quantum Electron.* **29**, 1–20 (2022).
41. Rizzo, A. *et al.* Ultra-efficient foundry-fabricated resonant modulators with thermal undercut. In *2023 Conference on Lasers and Electro-Optics (CLEO)*, 1–2 (2023).
42. Murthy, V. *et al.* Mitigation of parasitic junction formation in compact resonant modulators with doped silicon heaters. In *Laser Resonators, Microresonators, and Beam Control XXIV*, vol. 11987, 114–125 (SPIE, 2022).

43. Wu, Z., Yuan Dai, L., Wang, Y., Wang, S. & Bergman, K. Flexible silicon photonic architecture for accelerating distributed deep learning. *J. Opt. Commun. Netw.* **16**, A157–A168 (2024).
44. Jouppi, N. *et al.* Tpu v4: An optically reconfigurable supercomputer for machine learning with hardware support for embeddings. In *Proceedings of the 50th Annual International Symposium on Computer Architecture*, 1–14 (2023).
45. Ribeiro, A. *et al.* Column-row addressing of thermo-optic phase shifters for controlling large silicon photonic circuits. *IEEE J. Sel. Top. Quantum Electron.* **26**, 1–8 (2020).
46. Pal, S. *et al.* Low p π -value thermal phase-shifters in si-photonics technology. In *2022 IEEE International Conference on Emerging Electronics (ICEE)*, 1–5 (IEEE, 2022).
47. Almeida, V. R. & Lipson, M. Optical bistability on a silicon chip. *Opt. Lett.* **29**, 2387–2389 (2004).
48. Zheng, X. *et al.* Enhanced optical bistability from self-heating due to free carrier absorption in substrate removed silicon ring modulators. *Opt. express* **20**, 11478–11486 (2012).
49. Gebregiorgis, Y. *et al.* Wide spectral modulation in highly efficient thermally undercut foundry fabricated resonant modulators. In *2024 Conference on Lasers and Electro-Optics (CLEO)*, 1–2 (IEEE, 2024).
50. De Cea, M., Atabaki, A. H. & Ram, R. J. Power handling of silicon microring modulators. *Opt. express* **27**, 24274–24285 (2019).
51. ficonTEC. Photonics automated assembly & testing. <https://www.ficontec.com/> (2024).
52. Dietrich, P.-I. *et al.* In situ 3d nanoprinting of free-form coupling elements for hybrid photonic integration. *Nat. Photonics* **12**, 241–247 (2018).

Acknowledgements

This work was supported in part by the U.S. Advanced Research Projects Agency–Energy under ENLITENED Grant DE-AR000843, in part by the U.S. Defense Advanced Research Projects Agency under PIPES Grant HR00111920014, and in part by the Center for Ubiquitous Connectivity (CUbiC), sponsored by the Semiconductor Research Corporation (SRC) and DARPA under the JUMP 2.0 program. This material is based on research sponsored by the United States Air Force (FA8750-23-C-1001) and Air Force Research Laboratory under AIM Photonics (agreement number FA8650-21-2-1000) and also FA8750-21-2-0004. The U.S. Government is authorized to reproduce and distribute reprints for Governmental purposes notwithstanding any copyright notation thereon. The views and conclusions contained herein are those of the authors and should not be interpreted as necessarily representing the official policies or endorsements, either expressed or implied, of the United States Air Force, the Air Force Research Laboratory or the U.S. Government. Approved for Public Release; Distribution A Unlimited: AFRL-2025-1217.

Author contributions statement

A.R. and A.N. conceived the device designs, performed initial simulations, and completed the mask layout of the undercut geometry sweeps. V.D. and M.vN. designed and completed the mask layout of the microring, racetrack, and linear thermal phase shifters. L.C., G.L., and D.C. developed the undercut process and fabricated the wafers. C.C.T., A.M.S, and M.L.F. contributed to earlier versions of the undercut design, measurements, and data analysis. Y.G. performed the wide spectral modulation experiments. R.P. led the wafer-scale measurements with assistance from K.J. and the data analysis with assistance from Y.W. and X.M. All authors reviewed the manuscript and contributed to the writing. A.R., K.B., M.L.F, and S.P. supervised the project.

Additional information

Competing interests

The authors declare no competing interests.

Data Availability

The data that support the plots within this paper and other findings of this study are available from the corresponding author upon reasonable request.

Correspondence

Correspondence and requests for materials should be addressed to A.R. (email: anthony.j.rizzo@dartmouth.edu).