

Scalable Architecture for Sub-pJ/b Multi-Tbps Comb-Driven DWDM Silicon Photonic Transceiver

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ABSTRACT

The explosive growth of data-centric artificial intelligence applications calls for the next generation of optical interconnects for future hyperscale data centers and high-performance computing (HPC) systems. To unleash the full potential of dense wavelength-division multiplexing, we present the design and exploration of a novel transceiver architecture based on silicon photonic micro-resonators featuring a broadband Kerr frequency comb source and fabrication-robust (de-)interleaving structures. In contrast to the traditional single-bus architecture, our architecture de-interleaves the comb onto multiple buses before traversing separate banks of cascaded resonant modulators/filters, effectively doubling the channel spacing with each stage of de-interleaving. With a closed-form free spectral range (FSR) engineering technique guiding the micro-resonator design, the architecture is scalable toward hundreds of parallel channels—spanning much wider than the resonator FSRs—with minimal crosstalk penalty and thermal tuning overhead. This unique architecture, designed with co-packageability in mind, thus enables a multi-Tbps aggregated data rate with moderate per-channel data rates, paving the way for sub-pJ/b ultra-high-bandwidth chip-to-chip connectivity in future data centers and HPC systems.

Keywords: silicon photonics, optical transceiver, micro-resonator, multi-FSR, even-odd interleaving, dense wavelength-division multiplexing

1. INTRODUCTION

Optical interconnects, compared to traditional electrical ones, provide substantial benefits in terms of bandwidth capacity, energy efficiency, and propagation latency.¹ With continuous evolution of nanophotonic technologies over the past few decades, the adoption of optical interconnects have gradually unrolled from the long-reach telecom to the short-reach datacom regime to accommodate the expansion of network data volume.² In recent years, the explosive growth of data-centric artificial intelligence (AI) applications has sparked research emphases on improving computational capabilities through aggressive hardware parallelism and specialization, which further shifts the performance bottleneck of parallel computing infrastructures from computation toward communication.³ For avoiding data-starved computation nodes, recently reported bandwidth requirements for data centers and high-performance computing (HPC) systems running AI workloads have exceeded hundreds of Gbps,⁴ a data rate at which traditional electrical interconnects become uneconomical even for short distances at intra-rack, intra-cabinet, and chip-to-chip scales.⁵ As a promising enabler of the next-generation optical interconnects for alleviating this communication bottleneck,⁶ silicon photonics (SiPh) have demonstrated remarkable scalability and cost-effectiveness by supporting dense wavelength-division multiplexing (DWDM) through a fabrication process compatible with standard complementary metal–oxide–semiconductor (CMOS).^{7–9} Notably, recent advances in optical frequency comb sources^{10,11} and SiPh micro-resonators^{12–15} have facilitated investigations of DWDM link architectures based on cascaded micro-resonators from both academia and industry.^{16–19} Co-packaged SiPh optical input/output (I/O)—leveraging a tighter integration of these link architectures with their electrical driving

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circuitry and payload integrated circuits (ICs)—have also demonstrated great potential for achieving manifolded energy efficiency and bandwidth density compared to the traditional pluggable optical I/O.^{20–22}

CMOS-compatible micro-resonator-based Kerr frequency combs in the silicon nitride (Si_3N_4) platform have demonstrated the ability to generate hundreds of evenly-spaced low-noise wavelength channels from a single continuous-wave (CW) laser source in a compact footprint.^{23, 24} In particular, Si_3N_4 Kerr combs operating in the normal group velocity dispersion (GVD) regime are of growing interest to DWDM applications due to their better conversion efficiency, power per line, and spectral flatness compared to soliton Kerr combs operating in the anomalous GVD regime.^{25–29} To unleash the full potential of DWDM through this massively parallel wavelength scaling, a fundamental limitation of the traditional link architecture based on a single bus of cascaded micro-resonators must be overcome, namely the limited free spectral range (FSR) of the resonators. Specifically, the usable bandwidth of a traditional single-bus link is upper bounded by the resonator FSR—physically limited by the minimum resonator radius¹⁵ and much smaller than the spectral bandwidth of state-of-the-art frequency comb implementations²⁹—while packing more channels into a single FSR risks introducing excessive crosstalk penalties due to reduced channel spacing.³⁰ To this end, multi-FSR channel arrangement schemes have been proposed, which circumvents the channel count limit through the use of de-interleaved channels on multiple buses of cascaded micro-resonators and a novel FSR engineering technique that minimizes the crosstalk from resonance aliases, opening the possibility of future ultra-broadband optical interconnects with Pbps-class package escape bandwidth.³¹

In this work, we present the practical design and exploration of a SiPh micro-resonator-based DWDM optical transceiver with scalability and co-packageability in mind, targeting over 1 Tbps/fiber data transmission with a chip shoreline bandwidth density of over 2 Tbps/mm and a sub-pJ/b energy consumption. The transceiver features a scalable architecture that takes full advantage of the massive channel parallelism provided by the Kerr frequency comb with the novel use of fabrication-robust (de-)interleavers achieving even-odd channel interleaving and compact micro-resonators working in the multi-FSR regime guided by a closed-form FSR engineering technique. The architecture demonstrated thus provides a feasible pathway for ultra-energy-efficient multi-Tbps chip-to-chip connectivity with hundreds of wavelength channels for future data centers and HPC systems.

2. SCALABLE TRANSCEIVER ARCHITECTURE

Comb-driven micro-resonator-based DWDM has become more favorable to short-reach datacom applications in terms of its compact footprint and better energy efficiency,^{32, 33} compared to alternative architectures employing arrays of CW lasers³⁴ and/or non-resonant modulators/filters requiring dedicated (de-)multiplexing structures.³⁵ A widely recognized architecture features a single bus of cascaded micro-resonators with varying radii to modulate/filter distinct wavelength channels while appearing nearly transparent to other channels on the bus.¹⁷ However, this traditional single-bus architecture hits restrictions on further up-scaling when the comb bandwidth exceeds the resonator FSR. Specifically, since the resonance dips of a resonator exhibits periodicity at every integer multiple of its FSR, these unwanted resonances (*resonance aliases*) could overlap with non-target comb lines and result in severe crosstalk. Meanwhile, packing more channels into a single FSR risks introducing excessive inter-modulation crosstalk due reduced channel spacing, with experiments showing < 100 GHz channel spacing infeasible.³⁰ While micro-resonators with larger FSRs have been demonstrated by using smaller radii,^{36–38} it is unsustainable as a solution to massive wavelength scaling due to physical limitations on the micro-resonator size and accompanying design/manufacturing complexities regarding integrated heaters, radio frequency (RF) contacts, as well as electrical parasitic and process variation containment. An alternative approach, a.k.a. *band interleaving*, divides the incoming comb lines into sub-bands narrower than the resonator FSR.³¹ However, this approach faces device-level design challenges achieving sharp pass-band roll-off, crosstalk suppression, and tunability, and thus is pending on the maturity of design and fabrication of novel devices such as on-chip dichroic filters^{39, 40} and contra-directional couplers.^{41, 42} In these cases, we present a novel architecture for Kerr comb-driven micro-resonator-based DWDM transceivers with two hallmark features that address the scalability restrictions from two orthogonal dimensions, namely 1) *even-odd channel interleaving*, and 2) *multi-FSR channel arrangement*, allowing the use of denser comb lines with a total spectral bandwidth much wider than the resonator FSRs.

2.1 Even-Odd Channel Interleaving

Even-odd channel interleaving subdivides the incoming comb lines alternately into “even” and “odd” groups before traversing separate banks of cascaded micro-resonators.³¹ Assuming a (de-)interleaver FSR twice the channel spacing of the comb and perfect alignment between the (de-)interleaver pass/stop-bands and the comb lines, each stage of de-interleaving effectively doubles the spacing and halves the number of the output channels seen on each bus. To better tolerate the spectral misalignment in practice due to silicon waveguide GVD and fabrication process variations, broadband (de-)interleaving structures based on modified Mach-Zehnder interferometers (MZIs), such as ring-assisted MZIs (RAMZIs) or MZI-lattice filters,^{43–47} have been proposed to provide a flat-top response in the pass- and stop-bands. The resulting relaxation of crosstalk and insertion loss (IL) constraints on each bus thus allows the use of comb sources with a smaller channel spacing, e.g., $\leq 100\text{ GHz}$, for achieving denser wavelength-division multiplexing at the system level while maintaining device-level design constraints of an effectively larger channel spacing for sophisticated devices like the micro-resonators.

Fig. 1a illustrates the scalable transceiver architecture based on even-odd channel interleaving,³¹ featuring two stages of (de-)interleaving. The link is designed to be driven by a Si₃N₄ dual-ring normal GVD Kerr comb due to

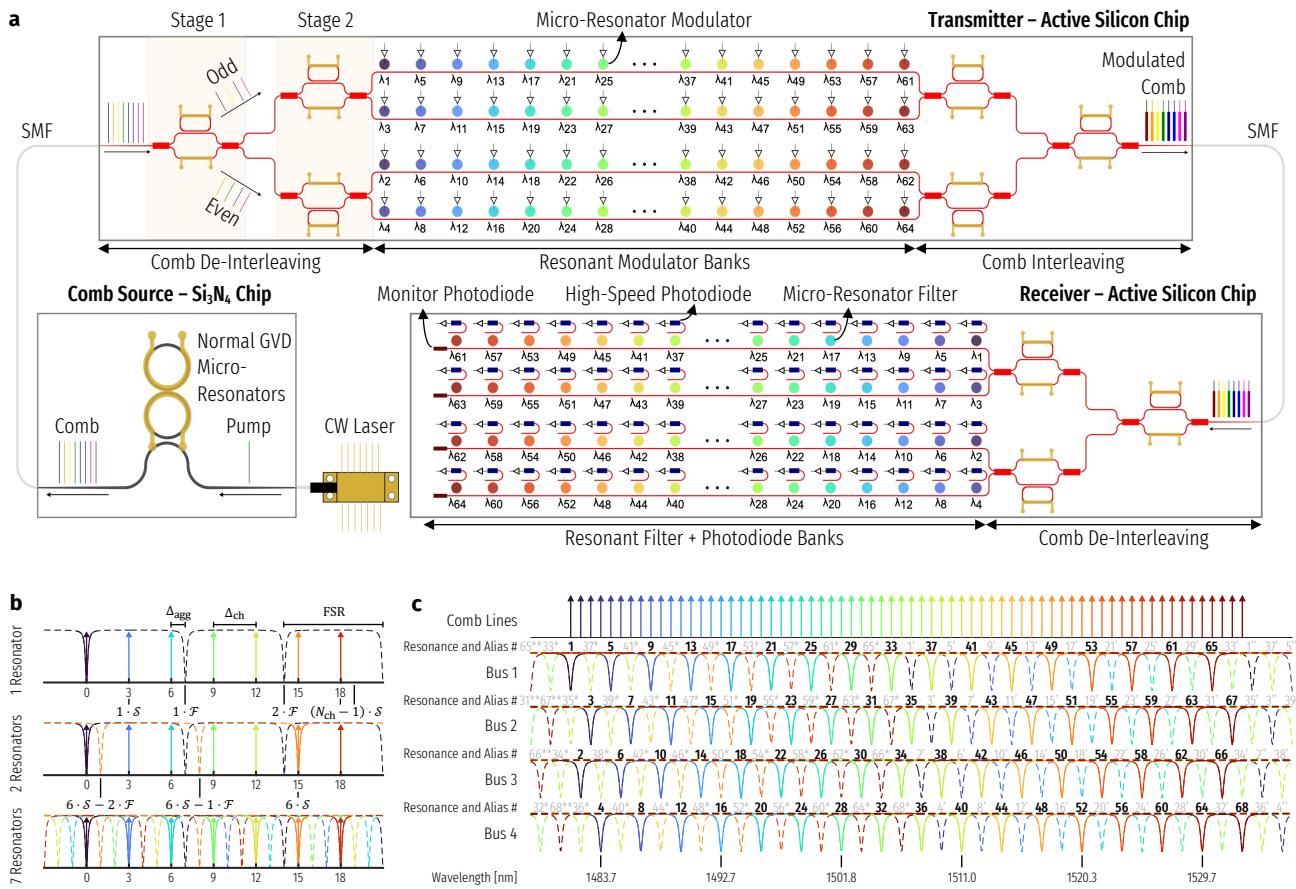


Figure 1. **(a)** Scalable transceiver architecture with even-odd channel interleaving, where each stage of de-interleaving effectively doubles the channel spacing while nearly preserving the total comb bandwidth on each bus.³¹ Multi-FSR channel arrangement is required for fully utilizing the comb spectral bandwidth on each bus with a moderate resonator FSR. **(b)** An exemplar multi-FSR arrangement plotted for a single bus with $S = 3$ and $F = 7$ [Eqs. (1a) and (1b)] showing the placement of resonance aliases (dashed) in between channels ensured by the co-prime rule.³¹ **(c)** A valid multi-FSR arrangement plotted for all four buses of the above transceiver architecture with $S = 2$ and $F = 17$, allowing at most 17 channels on each bus with a 25.69 nm resonator FSR. Asterisks (primes) denote the aliases to the blue (red) end of the nominal resonance.

its high conversion efficiency and power per line, as well as its relative spectral uniformity.²⁹ At the transmitter (Tx) side, two stages of even-odd de-interleavers based on RAMZIs (Sec. 3.1) subdivide the comb into four groups, each traversing a separate bank of cascaded micro-resonator modulators (Sec. 3.2). The modulated comb is then recombined by two stages of RAMZI-based interleavers into a single fiber output. Similarly, at the receiver (Rx) side, the modulated comb is de-interleaved onto respective banks of cascaded micro-resonator filters (Sec. 3.2) that drop each channel onto a photodetector (PD) for sensing. Assuming a comb channel spacing of 100 GHz, with 16 micro-resonator modulators/filters placed 400 GHz apart on each bus, the transceiver can effectively perform 64-channel DWDM targeting a 1.024 Tbps/fiber bandwidth capacity at a moderate data rate of 16 Gbps/channel.

2.2 Multi-FSR Channel Arrangement

Since the de-interleaved even and odd groups of comb lines nearly preserve the spectral bandwidth of the original comb, it is challenging, if not infeasible, to design micro-resonators with an FSR greater than the comb bandwidth due to a prohibitively small physical dimension that raises manufacturability and bend loss concerns.¹⁵ To this end, the resonator FSR must be carefully chosen to prevent resonance aliases from overlapping with non-target comb lines. A multi-FSR channel arrangement scheme thus aims to put resonance aliases in between the modulated channels while maintaining an adequate spacing between each channel and its nearest aggressor for crosstalk minimization. To mathematically formulate the problem of finding a valid multi-FSR channel arrangement, we define the following two auxiliary variables:³¹

$$\left\{ \begin{array}{l} \mathcal{S} = \frac{\Delta_{ch}}{\Delta_{agg}}, \\ \mathcal{F} = \frac{FSR}{\Delta_{agg}}, \end{array} \right. \quad (1a)$$

$$\left\{ \begin{array}{l} \mathcal{S} = \frac{\Delta_{ch}}{\Delta_{agg}}, \\ \mathcal{F} = \frac{FSR}{\Delta_{agg}}, \end{array} \right. \quad (1b)$$

where Δ_{ch} is the effective channel spacing on each bus after de-interleaving, Δ_{agg} is the reduced spacing between a channel and its nearest aggressor alias, and FSR is the resonator free spectral range (Fig. 1b). The quantities \mathcal{S} and \mathcal{F} represent the channel spacing and the resonator FSR normalized to the aggressor spacing. For a given comb design, the number of de-interleaver stages determines Δ_{ch} . Then, to find a valid resonator FSR, one would need to find a proper pair of integers for \mathcal{S} and \mathcal{F} satisfying Eqs. (1a) and (1b) under the constraint of Δ_{agg} being adequately large to minimize crosstalk. It has been shown that a valid multi-FSR solution occurs when the following two conditions are simultaneously met: 1) \mathcal{S} and \mathcal{F} are co-prime integers, i.e., having no common factors other than 1, and 2) \mathcal{F} is greater than or equal to N_{ch} , the desired number of channels on each bus.³¹ Fig. 1b shows an example for $\mathcal{S} = 3$ and $\mathcal{F} = N_{ch} = 7$, allowing at most 7 resonators placed on each bus while reducing the aggressor spacing to one third of the channel spacing. While a smaller \mathcal{S} is more favorable in terms of yielding a larger Δ_{agg} , it requires a larger resonator FSR for the same \mathcal{F} which is lower bounded by the desired number of channels on each bus. $\mathcal{S} = 1$ falls back to the single-FSR regime, requiring a resonator FSR greater than the total spectral bandwidth of the channels. Meanwhile, a larger \mathcal{F} (co-prime with \mathcal{S}) allows for more channels on each bus without reducing Δ_{agg} . Therefore, for the 4×16 transceiver architecture illustrated in Fig. 1a, a valid multi-FSR channel arrangement is found to be $\mathcal{S} = 2$ and $\mathcal{F} = 17$, as illustrated Fig. 1c, allowing at most 17 channels on each bus with the use of a moderate 25.69 nm FSR, which is well within a reasonable design space of micro-resonator-based modulators and filters.⁴⁸ The resulting aggressor spacing is approximately 200 GHz for an assumed 100 GHz comb after two stages of de-interleaving, at which the crosstalk penalty have been shown negligible in previous studies.^{30,49} Alternative solutions such as $\mathcal{S} = 2$ and $\mathcal{F} = 19$ can also be achieved with a slightly larger resonator FSR, legally supporting more channels and granting greater flexibility in the channel allocation of the 16 resonators on each bus, leveraging either *a priori* knowledge of the comb spectral shape or post-fabrication reconfiguration through thermal tuning. A more in-depth exploration of the multi-FSR design space is provided in a separate work.³¹

3. ENABLING DEVICES AND COMPONENTS

This scalable transceiver architecture is only realizable through the integration of its constituent devices, each of which requiring both independent and co-dependent design optimizations. One critical parameter that must be designed around is the channel spacing of the comb source driving the link. As mentioned, the proposed

transceiver architecture relies upon dual-ring normal GVD comb sources,²⁹ as illustrated in Fig. 1a, due to their high conversion efficiency and power per line, as well as their relative spectral uniformity. These sources can provide dozens of DWDM carriers across a broad spectrum and at an inherently fixed channel spacing in the frequency domain. The first device-level design challenge is then to operate uniformly across such a broad optical bandwidth, so as to minimally impact the performance of channels near the edge of the optical band. For passive devices and subcomponents, such as fiber couplers and power splitters, this obstacle is simply a question of optimizing physical device geometries for uniform and broadband spectral performance.

Passive optical device and subcomponent design can be subject to well established numerical optimization techniques, for example, metaheuristics like particle swarm optimization (PSO), genetic algorithm, and simulated annealing;⁵² bayesian optimization;⁵³ as well as inverse design (ID) algorithms.⁵⁴ PSO can be used to design compact, broadband, and low-error multi-mode interferometers (MMIs),⁵⁵ an example of such an MMI is

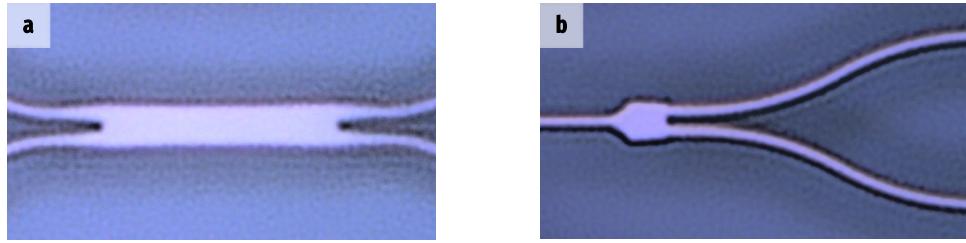


Figure 2. Microscope images of fabricated SiPh (a) PSO-generated 2×2 MMI and (b) ID-generated 1×2 Y-splitter. Each employs a series of numerical simulations to solve for a set of vertices along the device length and form the polygon via cubic interpolation between the solved points.

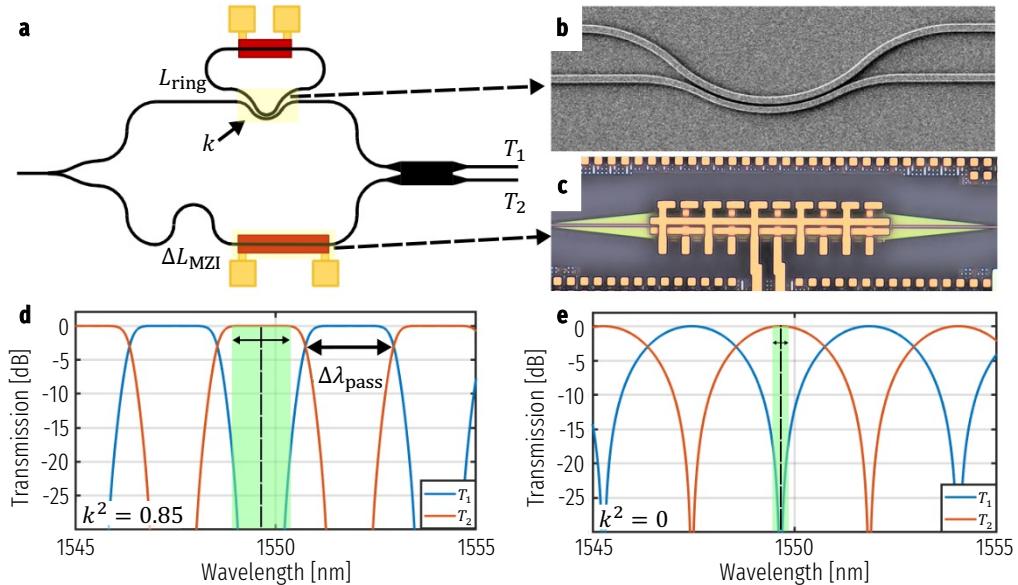


Figure 3. (a) Schematic of a single-ring RAMZI. The MZI FSR is determined by ΔL_{MZI} on the lower arm and the band flattening and sharpened roll-off occur when the ring resonances are aligned with every 3 dB crossing of the MZI, so the ring FSR, determined by L_{ring} , must be half the MZI FSR.⁴⁷ (b) SEM image of a bent directional coupler for broadband, compact, and low-loss asymmetric coupling between the MZI arm and the ring.⁵⁰ For flat single-ring RAMZI pass-bands, the optimal E-field coupling coefficient into the ring should be $k \approx 0.92$. (c) Microscope image of a low-loss and efficient doped silicon thermo-optic phase shifter,⁵¹ embedded in the ring and MZI arms to allow for post fabrication compensation to align the MZI fringes and ring resonances. Exemplar transmission spectra of (d) an ideal single-ring RAMZI, showing as much as 70 % of the pass-band within 0.1 dB of peak transmission, and (e) an equivalent MZI ($k = 0$), showing only 18 % of the pass band within 0.1 dB of peak transmission.

shown in Fig. 2a. ID-based design, either topological or parametric, has resulted in edge coupler and Y-splitter geometries with demonstrated low-loss and ultra-broadband performance,^{56,57} an example given in Fig. 2b. For the proposed architecture, we use these algorithmically optimized devices to construct more complex compound interferometric devices, utilizing the inherent wavelength-selectivity of the combined structures to perform critical multiplexing and de-multiplexing operations. We also propose using edge couplers to couple fiber into and out of our transceiver, as they typically boast improved coupling efficiency relative to grating couplers,⁵⁶ particularly over the ultra-broadband optical spectrum that our DWDM system requires.

3.1 Even-Odd (De-)Interleavers

As described in Sec. 2.1 and illustrated in Fig. 1a, even-odd (de-)interleavers are required to expand the effective channel spacing to accommodate the resonance aliases present in the multi-FSR channel arrangement of the cascaded resonator arrays. Our architecture uses a modification of the MZI, known as an RAMZI, for the required even-odd (de-)interleaving operation. RAMZIs are ideal for this purpose primarily due to their low-loss and relative tolerance to both FSR mismatch and fabrication variations.⁴⁷ They are also mostly composed of the aforementioned passive subcomponents, allowing for extremely efficient and modular implementation, as shown in Figs. 3a and 3b. A key subcomponent is the thermal phase shifter, as shown in Fig. 3c, which is critical for compensating both static (fabrication) and dynamic (environmental) phase errors that might otherwise malalign the MZI interference fringes from the design target.⁴⁷

The sharpened band roll-off and flattened pass-band transmission allow for a permissible range of FSR mismatch far beyond what would be available with a regular unassisted MZI. As shown in Fig. 3d, a carrier frequency can be $\pm 0.35 \cdot \Delta\lambda_{\text{pass}}$ displaced from the center of the RAMZI pass-band while still maintaining ≥ 16 dB of crosstalk suppression and suffering only 0.1 dB IL. With the same 0.1 dB threshold for IL, the equivalent spectral alignment tolerance for an unassisted MZI is only $\pm 0.09 \cdot \Delta\lambda_{\text{pass}}$ (Fig. 3e). While similar interleaver pass-band flattening can be achieved using an MZI-lattice finite impulse response filter, for the same order of filter the RAMZI infinite impulse response filter has a more compact footprint, lower loss, steeper roll-off, and is less sensitive to power splitting errors in the constituent devices.^{43,44} To address fabrication-induced phase errors that could cause spectrum shift and distortion, automated tuning algorithms have been demonstrated for similar cascaded MZI-based (de-)multiplexers,^{46,58} leveraging a tap monitoring PD on either one of the two output buses due to symmetry.

3.2 Cascaded Micro-Resonator Arrays

Resonant modulators and filters allow for wavelength-selective data encoding and decoding in an efficient and compact form factor. Cascading several micro-resonators along a single bus waveguide creates an array where each resonator independently interacts with the co-propagating carrier wavelengths. Microdisk modulators with vertical junction depletion-mode modulation has proven to be an effective choice for modulation, capable

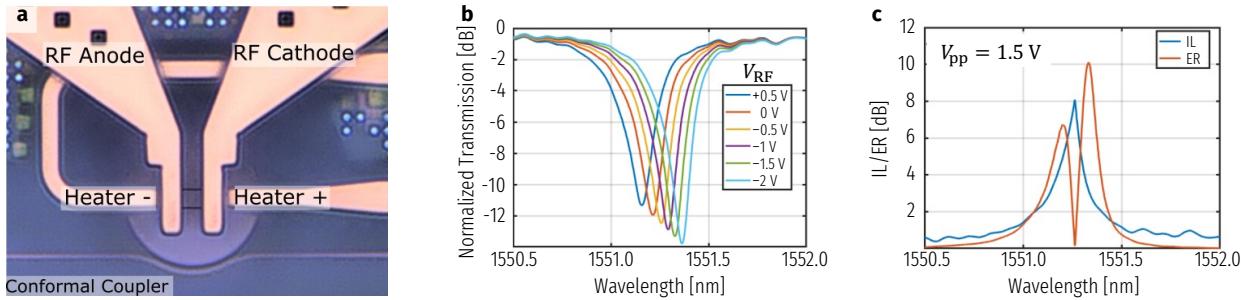


Figure 4. (a) Microscope image of a fabricated SiPh microdisk modulator, with notable features annotated, oxide barrier electrically isolating the doped silicon heater from RF modulation circuitry.³¹ (b) Measured DC depletion response of a microdisk modulator with voltage applied across the RF contacts. (c) Detuning wavelength-dependent modulation characteristics extracted from the depletion response, assuming modulation between $V_{RF} = 0$ V and $V_{RF} = -1.5$ V for a peak to peak voltage, $V_{pp} = 1.5$ V.

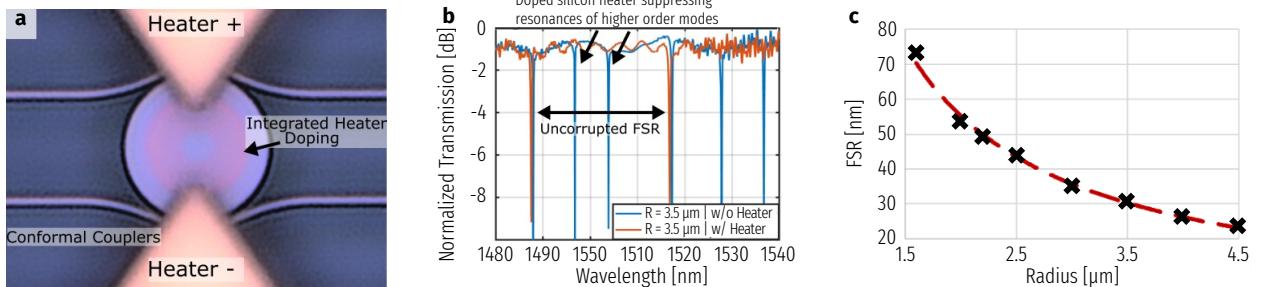


Figure 5. (a) Microscope image of a fabricated SiPh microdisk filter, with a radius, $R = 3.5 \mu\text{m}$ and the doped silicon integrated heater visible w/o image enhancement. (b) Measured spectra for the same disk design with and without the doped silicon, the conformal coupler phase matched coupling to TE0 and dopings demonstrably suppress higher order modes, effectively increasing the resonator FSR. (c) Measured relationship between nominal disk filter radius and FSR, averaged over the optical S- and C-bands, the \times markers denoting measured data points with the dashed line being a good exponential fit.

of supporting per-channel data rates up to 25 Gbps while driven by modest CMOS-compatible voltages and consuming only several fJ/b.^{14, 15, 31} In addition to the improved modulation efficiency of the vertical junction, the internal contact scheme and highly confined whispering gallery disk mode allow for a far greater FSR than the alternative single-mode ring constructed out of a ridge waveguide.^{15, 31} Fig. 4a shows a custom microdisk modulator fabricated through the American Institute for Manufacturing Integrated Photonics (AIM Photonics),⁵⁹ while Figs. 4b and 4c are representative measurement results of the direct current (DC) response and modulation characteristics. Of a particular concern with microdisk modulators, namely the risk of exciting higher order modes, we thus employ a conformal coupling scheme to phase match between the fundamental waveguide and resonator modes.³¹ Additionally, contact doping and vias are carefully placed to selectively attenuate the higher order modes, resulting in their resonances suppressed due to under-coupling and a large uncorrected FSR.

At the receiver, we propose disk filters, despite the ubiquity of single-mode ring filters in existing integrated SiPh DWDM architectures.³⁶ The same design principles of the modulators to suppress higher order mode resonances applies equally to the disk filter, as demonstrated in Figs. 5a and 5b. The link architecture proposed here is optimized for massively parallel DWDM and energy efficiency, rendering disk filters optimal for de-multiplexing due to their mitigated fabrication variation and increased maximum FSR (Fig. 5c). An additional benefit of employing disk filters is having matched dispersion characteristics between the resonant modulators and filters, reducing the overall design space complexity via symmetry.

4. SYSTEM DESIGN AND CONSIDERATIONS

When integrating the various devices and components described in Sec. 3 into a photonic IC (PIC) of the transceiver architecture featured in Fig. 1a, system-level design considerations must be given regarding the PIC aggregated bandwidth and bandwidth density, co-packageability with electronic ICs (EICs) and fiber array units (FAUs), design for testability, as well as proactively accounting for non-idealities in device performance, fabrication processes, and operating environments through architectural design variations.

4.1 PIC Design Overview

We designed a transceiver PIC in a process being co-developed with AIM Photonics, which includes custom vertical junction implants with optimized doping conditions and wafer-scale substrate undercuts for improved thermal tuning efficiency.³¹ The PIC floor plan is shown in Fig. 6a. Each PIC consists of four groups of Tx/Rx arrays each targeting a 4.096 Tbps/group data rate. Each group of Tx/Rx array consists of four 1.024 Tbps links featuring the architecture described in Sec. 2.1 and Fig. 1a. For illustration, Fig. 6b highlights one of the four links in Group 3, showing the (de-)interleaving structures and the multi-bus architecture. For EIC co-packageability, the PIC signal pads are placed at a 55 μm pitch and routed with considerations of minimizing the parasitic

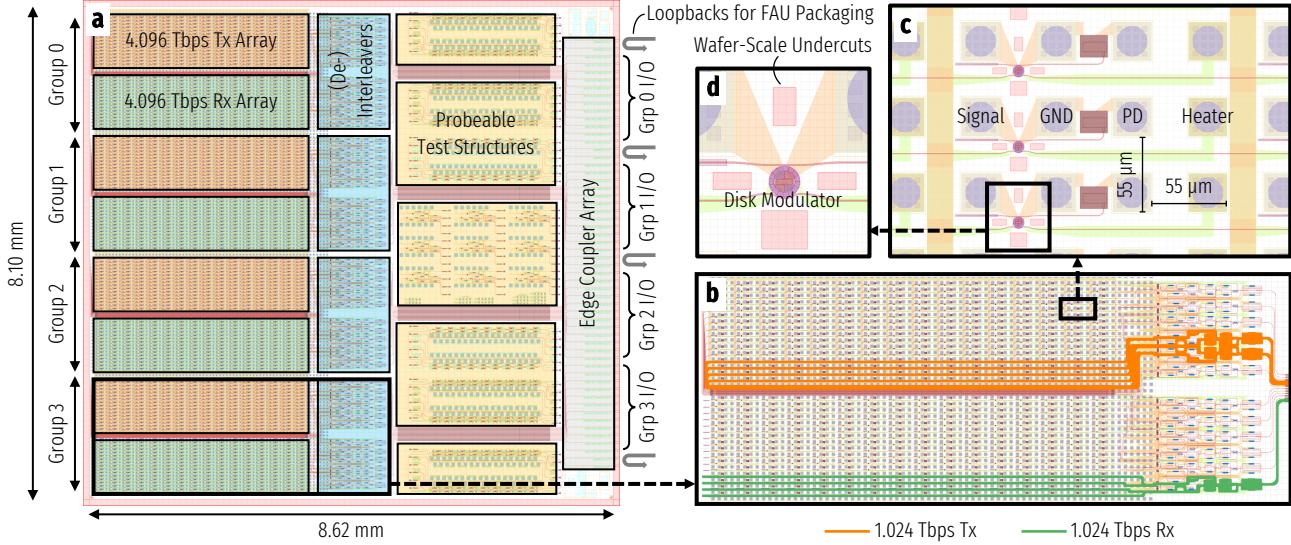


Figure 6. Transceiver PIC design overview, where each (a) $8.10\text{ mm} \times 8.62\text{ mm}$ chip consists of four groups of Tx/Rx arrays targeting 4.096 Tbps/group , probeable test structures of link subcomponents for pre-packaging monitoring of process variations and screening of KGDs, and edge couplers providing optical I/O. Each (b) 4.096 Tbps transceiver block consists of four 1.024 Tbps links featuring the architecture of Fig. 1a. The Tx/Rx arrays feature (c) electrical pads of a $55\text{ }\mu\text{m}$ pitch for EIC co-packageability and (d) wafer-scale substrate undercuts for improving the thermal tuning efficiency of and reducing the thermal crosstalk between the thermal phase shifters.

resistance and capacitance of RF traces. Fig. 6c shows the pad arrays of the Tx cells as an example. The PDs after the resonator drop-ports provide electrical input to an EIC that aims to lock the resonance wavelengths to their target carriers through closed-loop control. Notable implementations of such EICs with different control logics have been reported leveraging the drop-port PD signal.^{60–64} The PIC pads will be μ -bumped after fabrication and ready for flip-chip bonding with the EIC driver chip designed accordingly, an approach demonstrated feasible in past works.^{65,66} Wafer-scale substrate undercuts are placed near the resonant modulators/filters as well as the interleavers (Fig. 6d) for improving the thermal tuning efficiency of and reducing the thermal crosstalk between the thermal phase shifters.^{67,68} The edge coupler array is placed at a $127\text{ }\mu\text{m}$ pitch along a single side of the PIC for optical I/O, including four pairs of loopbacks (Fig. 6a) for FAU alignment. Between the edge couplers and the (de-)interleavers is a keep-out zone (KOZ) reserved for packaging. However, grating-coupled probeable test structures of the link subcomponents are placed in the KOZ (Fig. 6a) and can be accessed before packaging for identifying known good dies (KGDs) and providing qualitative insights on link performance and yield. Finally, a 16.384 Tbps aggregated bandwidth is able to escape from a single 8.10 mm side of the PIC, resulting in a shoreline bandwidth density of 2.023 Tbps/mm at 1.024 Tbps/fiber .

4.2 Practical Design Considerations

Non-idealities must be accounted for in the detailed transceiver design, whether they are borne from imperfect fabrication processes, dynamic operating environments, or non-ideal comb sources.

4.2.1 Process and Thermal Variation Awareness

The first system-level design consideration is given to the process and thermal variations present in PIC fabrication and operation, which could cause spatially and/or temporally varying device performance. As shown in Fig. 6a, by having grating-coupled probeable test structures in the region between the edge couplers and the (de-)interleavers, it is possible to qualitatively predict the performance and yield of the fabricated links at the wafer scale, notably before expensive and time-consuming dicing and packaging processes. This is achieved by placing exact copies of the link subcomponents, e.g., micro-resonator arrays and multi-stage (de-)interleavers, in the KOZ, an area otherwise reserved for packaging. While probing the μ -bumped devices within the transceiver links would likely degrade the quality and yield of the flip-chip bonding process, we are able to directly probe the dedicated

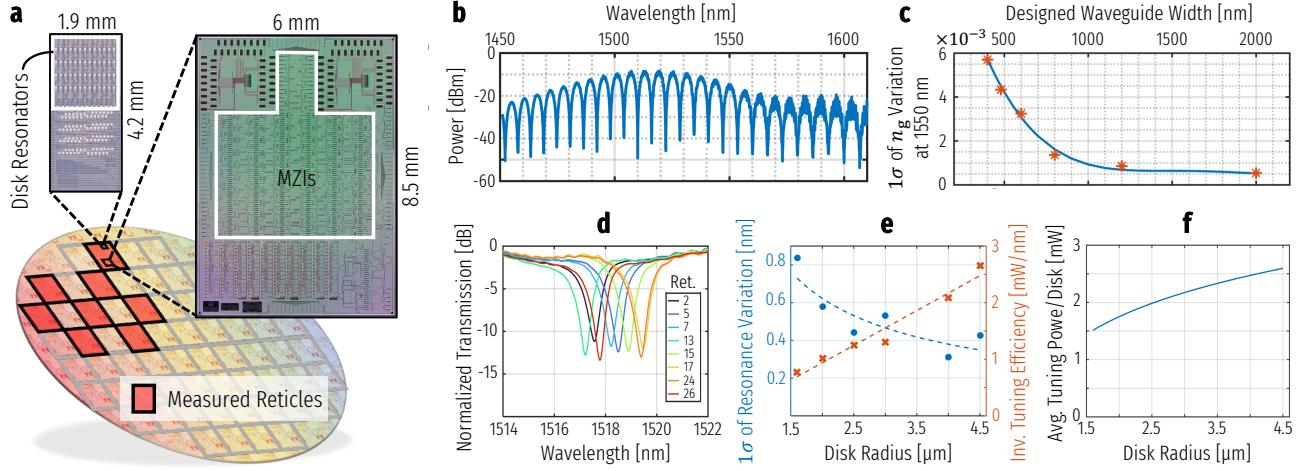


Figure 7. Characterization of fabrication robustness, where (a) eight representative reticles containing MZI and disk resonator test structures were measured on a custom 300 mm wafer; (b) the MZI interference fringes were used to extract the group index, n_g , of each individual waveguide width; (c) calculated σ_{n_g} at 1550 nm for six waveguide widths (asterisks) and curve fitting confirm measured reduction of process variations for wider waveguides;⁷⁵ (d) transmission spectra of microdisk filters of each individual design measured across eight reticles quantifies the process variation of the design; (e) 1σ of resonance locations decreases with larger disk radius, indicating greater fabrication robustness, yet inversely related to the thermal tuning efficiency; and (f) average thermal tuning power per disk is calculated from the measured variations and tuning efficiencies, assuming a 3σ design offset relative to the target resonance location. Designing for a wavelength 3σ lower than the target allows for $\sim 99.7\%$ of the fabricated disks to be tuned to the correct carriers assuming a normal distribution.⁷⁶

test structures whose key performance metrics—including their sensitivity to process variations and thermal fluctuations—are closely correlated to their corresponding intra-link counterparts due to spacial proximity.^{69,70} In addition to enabling this post-fabrication and pre-packaging qualitative analysis, we also incorporated a number of variation-aware design choices at both device and system levels for maximizing the likelihood of the proposed architecture resulting in the greatest possible performance and yield despite being subject to wafer-scale process variations and runtime thermal fluctuations.

Process variation mitigation At the device level, we leverage the principles of fabrication-robust multi-mode waveguides⁷¹ to construct the RAMZIs almost entirely using adiabatic Euler bends to maintain single-mode operation and reduce the impact of etch bias and sidewall roughness.^{72–74} The improved fabrication stationarity directly and positively impacts both expected yield and thermal tuning requirements by reducing the uncertainty in waveguide group index, n_g (Fig. 7c).⁷⁵ This enables that the assistive ring resonances and the MZI fringes both appear where expected and align with one another in the RAMZI devices with significantly reduced tuning effort.

We achieve a similar gain in robustness to fabrication errors using multi-mode disk modulators and filters in the transceiver instead of single-mode rings (Fig. 7e). In terms of waveguide geometric parameters subject to process variations, single-mode ring waveguides have three axes of possible perturbation—height, outer sidewall, and inner sidewall—compared to the two axes present in disks—only height and outer sidewall. Furthermore, the fundamental TE0 mode of a disk resonator is intrinsically more resilient to fabrication variations along the outer sidewall due to its improved confinement.^{14,31} For example, we observed variations of $1\sigma_{\text{ring}} \approx 1.1 \text{ nm}$ in resonance locations across a quarter of a 300 mm wafer for a single-mode ring, as opposed to the variations of $1\sigma_{\text{disk}} \approx 0.44 \text{ nm}$ for a disk resonator with the same FSR $\approx 40 \text{ nm}$.⁷⁷

Thermal variation tolerance At the system level, we leverage a barrel-shifted channel alignment scheme to account for potential in-package temperature elevation and fluctuations. Depending on the package thermal dissipation mechanism and the runtime workload of the co-packaged EIC, information regarding the PIC operating

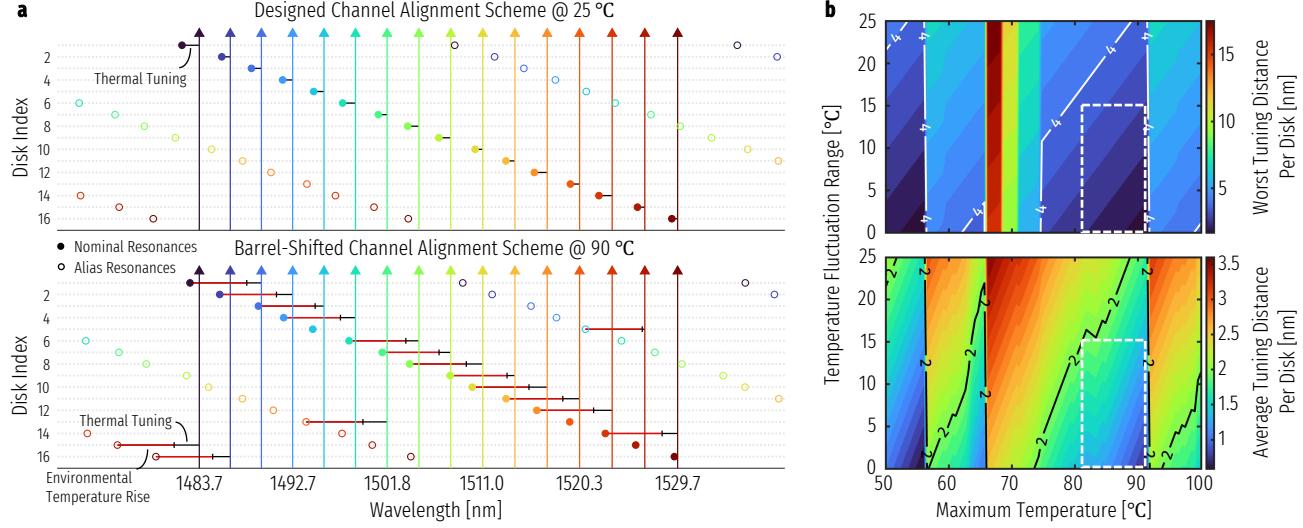


Figure 8. (a) Illustration of the barrel-shifted channel alignment scheme for reducing the total thermal tuning required at elevated temperatures, the case for one bus with 16 resonators shown. (b) Simulated heatmaps of the worst-case (top) and the average (bottom) tuning distance per disk w.r.t. various maximum temperatures and fluctuation ranges. The abrupt changes in tuning distance occur when a different channel alignment scheme is required. The heatmaps can provide helpful insights into packaging co-design by identifying desirable temperature ranges (dashed boxes) that the thermal dissipation mechanism should target.

temperature may not be accurate within the PIC design cycle. However, assuming the existence of a long-term maximum temperature and a finite fluctuation range below the maximum, the PIC can remain operable if initialized at or above the maximum temperature and employing a wavelength locking implementation^{60–64} that keeps track of the channel alignment scheme through thermal tuning once initialized. In this case, it is desirable that the thermal tuning requirement is minimized and well within the capability of the integrated thermal phase shifters for achieving both the initial channel alignment scheme at an elevated temperature and tracking it in the events of thermal fluctuations. Channel shuffling/re-ordering techniques have been proposed for the traditional single-FSR regime, which barrel-shifts the mapping between physical resonators and their target channels for reducing the total tuning distance required.^{78,79} In Fig. 8a, we illustrate the case for the multi-FSR regime where resonance aliases exist within the operational optical bandwidth and can be used as acting resonances in a barrel-shifted channel alignment scheme at a higher temperature. To enable this, our custom disk modulators and filters are designed to have broadband couplers and exceptional suppression of higher order modes, resulting in resonance aliases with as good optical characteristics as the nominal ones.³¹ By sweeping the anticipated maximum temperature and range of fluctuation in simulation with knowledge of process variation σ_s and resonance drift in nm/°C, it is possible to shed light on the desirable temperature range where both the average and the worst-case tuning distance per disk can be well contained, as marked by dashed boxes in Fig. 8b, providing useful information for packaging co-design.

4.2.2 Architectural Design Variations

On account of wavelength-dependent power penalties of the transceiver link, we also present two major architectural design variations, the first meant to address the spectral non-uniformity of the comb source and the second meant to take advantage of the asymmetric design constraints in resonant modulators and filters.

Nominal+ Resonator Array The normal GVD comb source that this architecture is designed around is notable for its relative spectral flatness compared to the more common anomalous GVD Kerr soliton comb sources.²⁹ However, the mode crossing adjacent to the pump wavelength often results in several lines near the center of the spectrum with insufficient power to close the link budget. With the *Nominal* micro-resonator arrays designed to interact with 64 consecutive carrier wavelengths, the channels near the mode crossing will inevitably

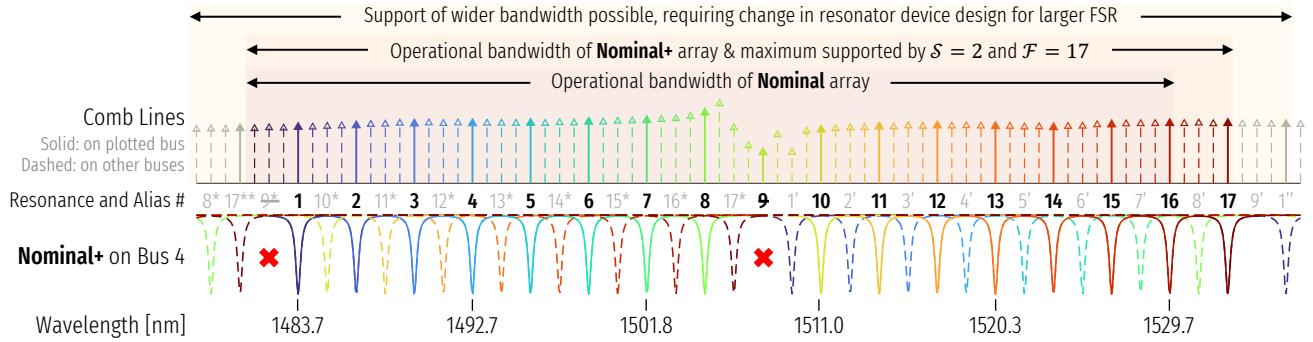


Figure 9. Illustration of the Nominal+ resonator array allowing for skipping one resonator per bus without altering the device design, assuming foreknowledge of the comb mode-crossing locations.

suffer, rendering the target aggregated data rate of the transceiver unachievable. Instead, with foreknowledge of the mode-crossing locations, we can opt to effectively skip those wavelengths expected to be problematic at the PIC layout stage. Referring to Fig. 1c where $S = 2$ and $F = 17$, it is possible to remove up to one resonator from each 17-channel bus and maintain at least 64 operational channels in the link without altering the device design. It is further illustrated in Fig. 9 where a modeled comb with mode-crossing imperfections and one of the four buses shown for clarity. Skipping the low-power central comb lines in favor of the higher-power lines at the spectrum edge comes at the cost of minor increase in the total operational optical bandwidth, but with the exemplar multi-FSR arrangement this *Nominal+* configuration does not significantly strain the bandwidth of the link design since an extra resonator on each bus is already permitted.

Stage-Reduced Receiver As discussed in Sec. 2.2, a multi-FSR arrangement defined by the co-prime integer pair, (S, F) , is only deemed valid if the derived resonator FSR is manufacturable. For microdisk resonators, the FSR is almost entirely determined by the device radius for a fixed waveguide height. The intrinsic bend loss of a multi-mode resonator is permissive of high-Q resonators with FSRs > 70 nm, corresponding to device radii $< 2 \mu\text{m}$.⁸⁰ While this is the case with intrinsic passive silicon devices, for RF modulation and efficient thermal tuning, there must be electrical circuitry—comprised of metal traces and vias contacting the heavily doped silicon—to create practical disk modulators, as shown in Fig. 4a. Adding the foundry design rules on top of the said constraints to fit circuitry for both modulation and thermal tuning within the disk radius considerably reduces the maximum device FSR achievable. On the other hand, for disk filters, only the thermal tuning circuitry is mandatory, as shown in Fig. 5a, allowing for a more compact device with a larger FSR. As a result of this asymmetry in design constraints, it is possible to utilize disk filters with double the FSR of the corresponding disk modulators, thus halving the number of interleaver stages at the receiver side relative to the transmitter side of the link. Reducing the number of RAMZIs, even only on the receiver end, can potentially reduce broadband IL, simplify control complexity, and increase areal bandwidth density of the overall link.

4.3 Full-Link Simulation and Energy Efficiency Evaluation

We validate the efficacy and performance of the proposed scalable architecture through a comprehensive link model simulation. The link model framework is implemented in Python and Lumerical INTERCONNECT, allowing exceptional device model accuracy and control through co-simulation.⁸¹ We simultaneously simulate all channels across the entire link optical bandwidth to include practical architectural and device design implications, such as the crosstalk, insertion loss, and jitter.

Each constituent device, as described in Sec. 3, is modeled using previously measured characteristics. The Kerr comb laser model uses experimentally measured line powers, along with measured coupling losses to fiber. The (de-)interleavers are modeled for the same structures placed in the layout in Fig. 6b, which were designed using measured transmission spectra of couplers and MMIs. We also integrate accurate component models of both the custom disk modulators and disk filters in the simulation, including dispersion characteristics from extensive finite difference eigenmode (FDE) simulations, experimentally measured depletion response, and measured off-resonance

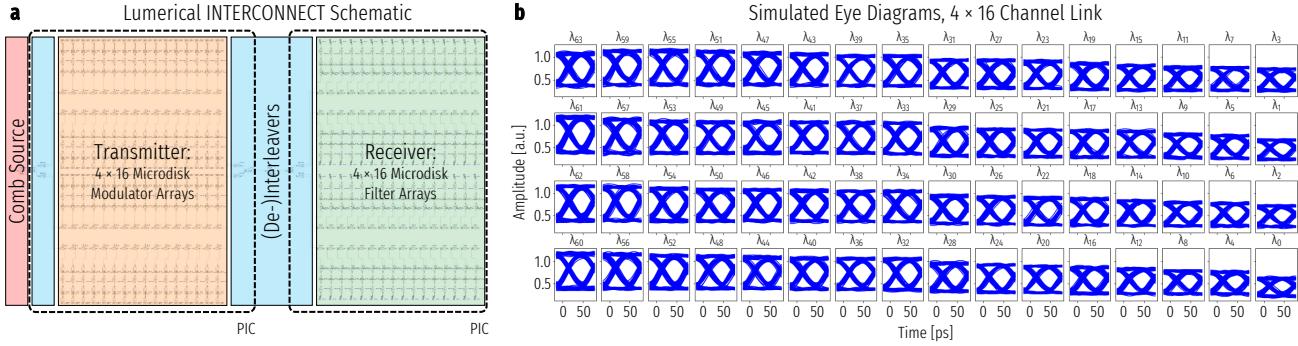


Figure 10. (a) Schematic of generated Lumerical INTERCONNECT circuit for end-to-end link simulation, annotated to show constituent components. (b) 64 simulated eye diagrams, 4 buses of 16 channels each, obtained from the link simulation. All 64 channels were simulated simultaneously across the same optical bandwidth. Eye amplitude decreases further into receiver due to off-resonance IL.

IL. These component models, defined and calculated in the Python environment, are automatically placed within the INTERCONNECT environment, as shown in Fig. 10a, for co-simulation.

We obtain eye diagrams for all 64 channels through the end-to-end link simulation, as highlighted in Fig. 10b. Non-idealities in the transmitter and receiver EICs are included in the model, such as realistic rise/fall time, jitter, and frequency response of the analog front-end. To ensure that these characteristics match those expected from the fabricated EIC, we used simulations of the EIC circuitry to validate our electrical models. Incorporation of the electrical component models, in addition to the measurement-based optical link model, allows the generation of eye diagrams for all channels with a pseudo random bit sequence (PRBS) of length 2^7 (PRBS-7). With an average comb laser power of 0 dBm per line, we achieve a calculated bit error rate (BER) of less than 10^{-9} for all channels, error free transmission for most channels based on calculated BER, and error free transmission for all channels based on simulator-measured BER. We note that these results do not include an optical amplifier within the link, which enables us to meet the exceedingly low energy-per-bit metrics.

We estimate the thermal energy consumption for control of most constituent devices within the link, necessary due to variations in fabrication and changes in environmental temperature. Integrated micro-heaters are used for either of the dual rings of the Kerr comb for initialization and stability. Previously fabricated integrated Kerr combs indicate a thermal energy consumption of 49–100 fJ/b. As we continue through Tab. 1, we note that each 1.024 Tbps link consists of 9 (de-)interleaving structures, in which each structure contains 3 thermo-optic phase shifters for the (de-)interleaver MZI arm, the monitoring MZI arm, and the assistive ring, respectively. These integrated heaters, as shown in Fig. 3c, are necessary for interleaver alignment and flat-top response. Accounting for assumed $\pi/16$ – $\pi/8$ phase errors due to fabrication variations, we expect a required interleaver thermal energy consumption of about 70–132 fJ/b. The disk modulators and filters also utilize integrated heaters, as shown in Figs. 4a and 5a, respectively, to achieve high efficiency in thermal tuning. Based on previously measured

Table 1. Expected thermal energy consumption of both constituent components and total link, obtained by dividing the expected power dissipation by the link data rate. The expected energy efficiency for devices with substrate undercuts is also listed.

Component	w/o Undercuts	w/ Undercuts
Comb Source [fJ/b]	49–100	5–10
(De-)Interleavers [fJ/b]	70–132	7–13
Disk Modulators [fJ/b]	80–160	8–16
Disk Filters [fJ/b]	80–160	8–16
Total Thermal Energy [fJ/b]	279–552	28–55

statistical data regarding resonance variations and tuning efficiency, shown in Fig. 7e, and the anticipated operating temperature, we expect 80–160 fJ/b for both disk modulators and disk filters. We note, as shown in the last column of Tab. 1, that we expect at least a tenfold increase in energy efficiency with undercuts. Etching around the device and removing the immediate substrate result in an undercut device, surrounded by mostly air instead of oxide. Such a decrease in thermal conductivity results in a more concentrated temperature increase for a given power dissipation, which leads to vastly improved thermal energy efficiency.^{67,68}

5. CONCLUSION

We presented the design and exploration of a Kerr comb–driven SiPh micro-resonator–based DWDM optical transceiver with a novel and scalable architecture enabled by even-odd channel interleaving and multi-FSR channel arrangement. The proposed architecture features a 1 Tbps/fiber data rate with a sub-pJ/b energy efficiency. We also discussed several practical design considerations and yield improvement strategies at device, architecture, and system levels, supported by a comprehensive link model simulation based on accurate device models made out of measurement results. We have taped out the transceiver PIC of the proposed architecture designed with co-packageability in mind—targeting an aggregated data rate of over 16 Tbps with a chip shoreline bandwidth density of over 2 Tbps/mm—and its architectural design variations on a custom 300 mm wafer through AIM Photonics, along with dedicated test structures of all constituent devices, subcomponents, and links for future validation and demonstration. The proposed transceiver architecture represents a feasible pathway for future ultra-energy-efficient multi-Tbps chip-to-chip connectivity with massively parallel wavelength channels for data center and HPC applications.

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