Compact Modeling and Circuit-Level Simulation of Silicon Nanophotonic Interconnects

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***Abstract*—Nanophotonic interconnects have been playing an increasingly important role in the datacom regime. Greater integration of silicon photonics demands modeling and simulation support for design validation, optimization and design space exploration. In this work, we develop compact models for a number of key photonic devices, which are extensively validated by the measurement data of a fabricated optical network-on-chip (ONoC). Implemented in SPICE-compatible Verilog-A, the models are used in circuit-level simulations of full optical links. The simulation results match well with the measurement data. Our model library and simulation approach enable the electro-optical (EO) co-simulation, allowing designers to include photonic devices in the whole system design space, and to co-optimize the transmitter, interconnect, and receiver jointly.**

I. Introduction

Light is an ideal medium for data transmission because of its high bandwidth, low loss, and low parasitics. Optical communications have been dominating long-haul and metro telecommunications (telecom) for decades, and are now beginning to be widely deployed for short-reach datacom [1]. A key enabler of the short-reach optical interconnects is the integrated photonics. The fast growing complexity of photonic integrated circuits (PICs) drives the need for photonics design automation tools [2]. A number of system- and link- level studies for optical interconnects have been reported [3]–[6], but due to the analog nature of photonics, it is imperative to perform accurate circuit-level (or equivalently SPICE-level) modeling and simulation of nanophotonic interconnects. Circuit-level compact models of a variety of photonic devices have been reported, e.g., carrier-injection [7], [8] and carrier-depletion [9] based silicon microring modulator, Mach-Zehnder modulator [10], VCSEL laser [11], etc. However, there is a lack of effort for integrating such models to enable simulation, validation, and optimization of a full optical link.

In this work, we study an optical network-on-chip (ONoC) which was fabricated on heterogeneous silicon platform [12]. The ONoC has a circular bus waveguide architecture with eight wavelength-division-multiplexing (WDM) transceiver nodes (Fig. 1). Each transmitter (Tx) has eight continuous wave distributed feedback (DFB) lasers, eight electroabsorption modulators (EAM), and an arrayed waveguide grating (AWG) as an optical multiplexer. Each receiver (Rx) has an AWG as an optical demultiplexer, and eight InGaAs/silicon photodetectors (PD).

We develop accurate circuit-level models for all of the photonic devices in the ONoC. These models are implemented in Verilog-A so that the optical interconnects can be simulated in a SPICE environment. The photonic device models are validated in several aspects using the measurement data from our implemented ONoC. Using these models, we simulate a full optical link in Cadence, and the simulation results are also verified by the link measurement data. Our models and simulation approach enable the electro-optical (EO) co-design and optimization of the photonic devices with electronic interface circuits that have been designed separately in the past. Additionally, the enrichment of photonic device library paves the way to a process design kit (PDK) for silicon photonics, and an EDA-style design process for PICs and electro-optical systems.

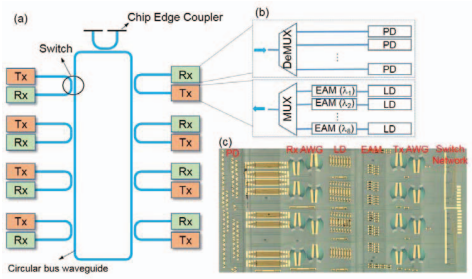

Fig. 1. (a)(b) Our ONoC architecture with a zoom-in of a transmitter (Tx) and a receiver (Rx), where LD: laser diode, EAM: electroabsorption modulator, PD: photodetector, $\lambda_{1\sim8}$: channel wavelengths; (c) The microscopic image of the fabricated ONoC including 8 transceiver nodes.

II. Device Modeling and Parameter Extraction

A. Laser

Diode lasers utilize carrier injection in a p-i-n junction to provide stimulated emission and optical gain. A diode laser can be used for either continuous wave (CW, or static) operation with an external modulator or direct modulation, where the former mode is used in this work. The output light power vs. driving current (LI) of a diode laser can be expressed by (1) [13].

$$P = \eta_d \frac{h\nu}{q}(I - I_{th}) \tag{1}$$

The two performance parameters in the LI model are the threshold current I_{th} and differential quantum efficiency η_d. The DC electrical characteristics of the diode laser follows the Shockley diode equation as shown in (2).

$$I = I_0 \exp \frac{q(V - IR)}{nkT} \tag{2}$$

Where R is the series resistance, n is the emission factor, I_0 is the saturation current, k is the Boltzmann constant, and T is the temperature.

Model Validation: The optical and electrical models of diode lasers are implemented in Verilog-A and simulated in SPICE, where the optical power is described by the potential between an optical signal line and a dummy optical ground. Fig. 2 shows the simulated and measured LI and IV curves, which have good agreements. With these two models, designers can accurately determine the driving voltage and power of the laser based on the optical link's power budget.

B. Electroabsorption Modulator (EAM)

EMAs utilize a reverse biased p-i-n junction to apply electrical field and to modulate the optical absorption coefficient [13]. We find that the dependency of the EAM optical transmission on the bias voltage can be described by the logistic equation in (3).

$$T_{opt}(V_j) = IL \cdot \left(\frac{1-b}{1+\exp(-k(V_j - V_0))} + b\right) \tag{3}$$

Where V_j is the voltage on the p-i-n junction, *IL* is the insertion loss, V_0 is the transition voltage, b is the residual optical transmission at a

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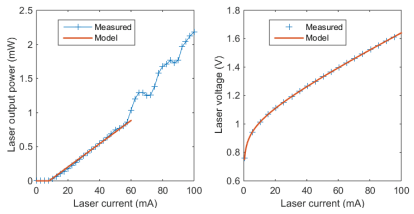

Fig. 2. Measured and model simulated LI and IV curves of the DFB laser (light output is from one facet). The kinks in L-I curve may be due to the mode hopping of the high injection current, which will not be used in single mode communication.

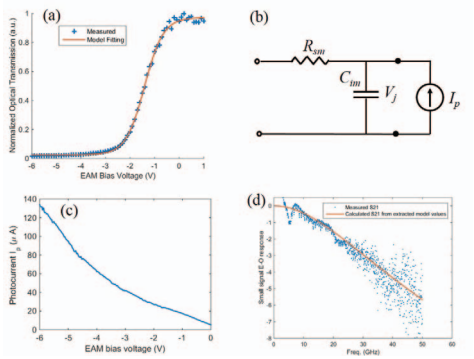

Fig. 3. EAM: (a) Measured and model fitted optical transmission at 1550 nm wavelength; (b) Equivalent circuit model; (c) Measurement photocurrent generated by the absorbed optical power (input optical power = 316 μW); (d) Directly measured and model calculated small-signal E-O (electrical-to-optical) responses. (The measurement setup has a 50 Ω configuration.)

strong bias voltage. Fig. 3 (a) shows that our proposed model in (4) matches the measurement data well. By applying a DC bias around V_0 and an AC modulation driving signal, the EAM can perform on-off keying (OOK) modulation of the optical signal.

The electrical characteristics of the EAM can be described by an equivalent circuit model as shown in Fig. 3 (b), where R_{sm} is the device series resistance, C_{im} is the junction capacitance, V_j is the junction voltage that determines the optical absorption and transmission in (3), and I_p is the photocurrent generated by the absorbed optical power and fed back into the electrical circuit [14]. Fig. 3(c) shows the IV curve of the photocurrent element, which can be equivalent to a resistance of multi kilo-Ohm. The photocurrent element has trivial influence on the EAM's scattering parameters S11 and S21, since the R_{sm} is in the order of 10 Ω.

The values of C_{im} and R_{sm} are extracted from the scattering parameter S11 data measured by a lightwave component analyzer (LCA). The measured S11 is first converted to the device or load impedance (Z_L), as shown in Fig. 4. Then it is observed that the imaginary part of the device impedance is inversely proportional to the frequency, from which the C_{im} value is extracted. Meanwhile, the R_{sm} can be estimated from the Z_L real part at high frequency. Based on the extracted C_{im} and R_{sm} values, we in return calculate the S11, which is in good agreement with the directly measured S11 data as shown in Fig. 4. This agreement is one of the key evidences of the validity of our EAM circuit model.

Model Validation: An EAM's total bandwidth is subject to both RC limit and carrier transit time limit. However, the EAM in this work has a thin intrinsic region and a small carrier transit time. Therefore, the EAM here is only subject to RC limit, and we can use the extracted R_{sm} and C_{im} values to predict the EAM's frequency response. Fig. 3 (d) shows that our model predicted electrical-to-optical frequency

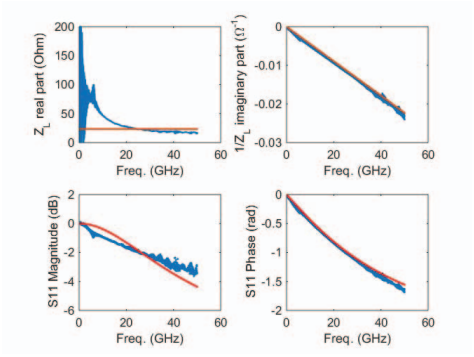

Fig. 4. S11 and device impedance data of the EAM, where blue dots represent measurement data and red lines show model results.

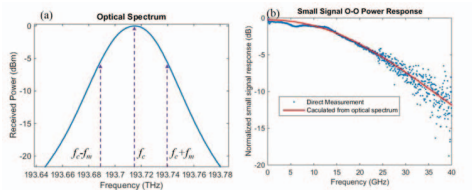

Fig. 5. (a) Measured optical spectrum of a commercial bandpass filter (BPF); (b) Measured and calculated small signal responses of the BPF.

response matches well with the directly measured S21 data, which is another piece of evidence for the validity of our model.

C. Multiplexer and Demultiplexer

The structure of the multiplexer and demultiplexer in our design is an AWG, which utilizes phased-array to multiplex or demultiplex the light at a series of wavelengths with certain channel spacing [15]. A typical AWG spectrum is shown in Fig. 6 (a), where eight colors represent eight channels. Each channel of the AWG functions as a bandpass filter, and can route the optical signal at its center wavelength in or out of the bus waveguide.

The AWG will reduce the amplitude of the high speed optical signal due to its spectral filtering effect [16]. In order to illustrate the spectral filtering effect, we plot the optical spectrum of a commercial bandpass filter (BPF) in Fig. 5 (a), where f_c is the central carrier frequency, and f_m is the modulation frequency. By modulating the optical carrier wave using a sine wave, two sidebands located at $f_c \pm f_m$ appear, which will be suppressed by the slope of the filter's optical spectrum. The small signal optical-to-optical (O-O) response of the filter can be calculated as $T(f_c + f_m)/T(f_c)$, where $T(f)$ is the optical power transmission at frequency f. Fig. 5 (b) shows that our calculated frequency response using this approach agrees well with the directly measured frequency response using an LCA.

During our experiments we observed that the small signal response of the AWG cannot be directly measured by LCA due to large edge coupling loss. Therefore, we calculate the AWG's O-O small signal response based on the optical spectrum that can be easily measured using the aforementioned approach, as shown in Fig. 6 (b)(c). Because the measured AWG spectrum is asymmetric, the average of the spectrum's left-side slope and right-side slope is used to calculate the small signal response. The AWG's small signal response can be well approximated by a two-pole low-pass filter (LPF) as described in (4) up to 45 GHz.

$$H(f) = \frac{1}{(1 + j \cdot f/f_{LPF})^2} \tag{4}$$

Based on this approximation, we implement the AWG's dynamic

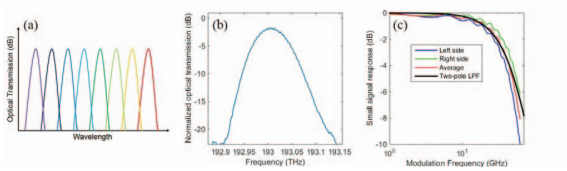

Fig. 6. (a) A theoretical optical spectrum of an AWG; (b) Measured single channel optical spectrum of the AWG; (c) The calculated frequency response using AWG's optical spectrum, with an approximation by a low pass filter (black line).

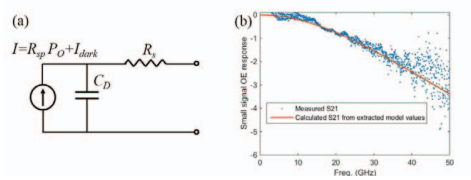

Fig. 7. (a) PD's equivalent circuit model; (b) Directly measured and model calculated small-signal O-E (optical-to-electrical) responses of the PD at -3V bias. (The measurement setup has a 50 Ω configuration.)

model in Verilog-A using integral operators. The AWG Verilog-A model also includes the insertion loss effect, which is 1.5 dB in our experiments when the channel center wavelength is well aligned with the laser wavelength. Our AWG model does not include multi-channel wavelength information, since our focus is on modeling and simulating the dynamic characteristics of the device and the link at one channel wavelength. However, extension to considering multi-channel wavelengths should be quite straightforward.

D. Photodetector

The PD studied in this work is made of reverse-biased p-i-n junction, which generates photocurrent when there is light input. The PD's responsivity R_{sp} is defined as the photocurrent over input optical power. The electrical characteristics of the PD can be modeled by an equivalent circuit as illustrated in Fig. 7 (a), where the current source represents the photocurrent generated by the input light with power P_O and the dark current I_{dark}, C_D is the diode capacitance under reverse bias, and R_s is the series resistance. The values of C_D and R_s can be extracted in a similar approach as the EAM. Fig. 8 shows how the C_D and R_s are extracted from Z_L real part and imaginary part respectively, and that the calculated S11 agrees well with the measured data which validates our model.

Model Validation: Similar to the EAM, the PD in this study is also only subject to the RC limit since its intrinsic region is thin (400 nm). So we can calculate the PD's frequency response using

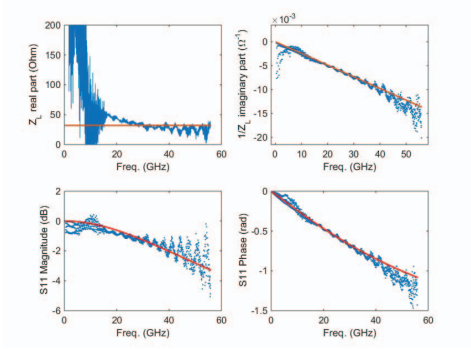

Fig. 8. S11 and device impedance data of the PD at -3V bias, where blue dots represent measurement data and red lines show model results.

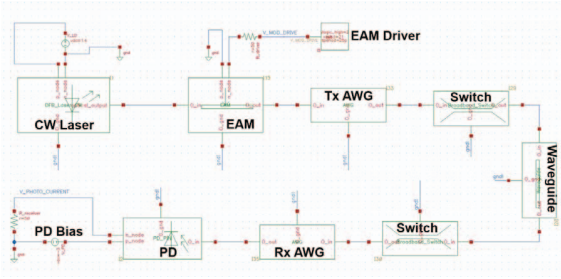

Fig. 9. The Virtuoso simulation schematic of the entire transceiver link using our developed models.

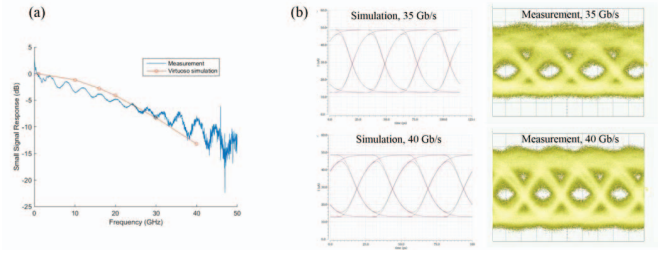

Fig. 10. Simulated and measured frequency responses (a) and eye diagrams (b) of a single channel transceiver link.

the extracted R_s and C_D values. Fig. 7 (b) shows that the predicted frequency response agrees well with the measured O-E S21 frequency response, which is a strong piece of evidence of the validity of our PD model.

III. Link Simulation and Design Space Exploration

A. Full Link Simulation

We simulate an end-to-end single channel transceiver link using our photonic models in Cadence Virtuoso. Fig. 9 shows the simulation schematic that reproduces the measurement setup. The measurement setup has a 50 Ω configuration (i.e., all testing equipment, RF cables and probes are 50 Ω matched), so in the simulation schematic two 50 Ω resistances are added at the EAM driver and the PD receiver, respectively. The EAM is driven by a random bit sequence source swinging between -1∼-2 V, and the PD is biased at -3 V. The broadband switch model simply describes its insertion loss effect, since our switch has a wide wavelength operation range (1550∼1570 nm) and will not impose a bandwidth limitation to the link [12].

We first perform AC simulations of the full transceiver link. Fig. 10 (a) shows that the simulated frequency response matches well with the measurement data. Then transient simulations are run to get the eye diagrams of the link. Fig. 10 (b) demonstrates that the simulated eye diagrams have good agreements with the measured ones. The simulations accurately capture the transmission bandwidth limit and pattern dependent noise of the optical link. The measured eye diagrams are noisier than the simulated ones because the large signal measurements includes noises and degradations from electrical components (e.g., RF probes, cables, amplifiers). Both the simulated and measured eye diagrams show that the link's data rate is close to its bandwidth limit seen from the increasing inter-symbol interference (ISI) and decreasing optical modulation amplitude (OMA). Therefore, we can conclude that the AC and transient simulations give us high confidence that our models are sufficiently accurate.

B. Design Space Exploration of the PD Design

Our photonic chip includes a large variety of individual PD test structures with different device lengths and widths, only a subset

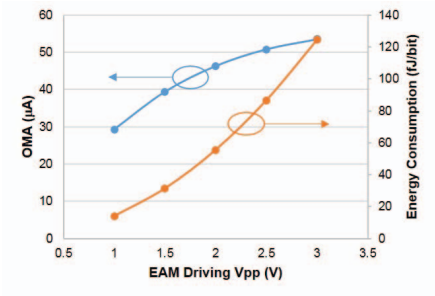

Fig. 11. The OMA and modulation energy consumption with respect to different EAM driving Vpps.

of which are used in the fabricated full transceiver links due to layout space limitation. Table I shows the key parameters of several exemplar PD designs, where the PD# 1 is used in the full transceiver link in Section IV. A. The bandwidth (BW) is calculated by the (R+50)C constant from the PD's extracted capacitance and resistance at -3V bias, considering a 50 Ω receiver. It can be observed that the responsivity increases while the bandwidth decreases with the PD length.

TABLE I
PD DESIGN SPACE AND SIMULATED OMA

PD #	Width (μm)	Length (μm)	Resp. (A/W)	Cap. (fF)	Res. (Ω)	BW (GHz)	OMA (μA)
1	4	30	0.45	38.9	38.9	46.0	29.3
2	2	50	0.48	38.6	52.0	40.4	30.6
3	2	75	0.56	54.8	36.0	33.8	34.4
4	2	100	0.66	71.5	29.4	28.0	38.3

The PD# 2∼4 have a higher responsivity but a lower bandwidth than the PD# 1. Therefore, it is possible to replace the PD# 1 with 2∼4 to trade bandwidth for responsivity to get a higher OMA. We then use PD# 2, 3, and 4 respectively in the full link simulation to get the link eye diagrams at 40 Gb/s, and then extract the OMA values as shown in the last column in Table I. The simulation results show that PD# 4 leads to the highest OMA mainly because of its high responsivity. A higher OMA will result in a better signal to noise ratio (SNR) and, in turn, a lower bit error rate (BER). This study of PD designs demonstrates that, with our models, the designers can now include photonic device designs in whole system optimization.

C. Optimization of the EAM Driving Voltage

In the link simulations above, 1 Vpp voltage is used to drive the EAM, which saves energy but compromises the OMA. This can also be seen from the EAM's transmission vs. voltage curve in Fig. 3 (a), where 1 Vpp is not enough to swing the optical transmission to the maximum or minimum point. We increase the EAM's driving Vpp, re-simulate the eye diagrams at 40 Gb/s, and extract the OMA and modulation energy consumption as plotted in Fig. 11 (other device parameters and driving conditions are the same as those in Section IV. A). The simulation results show that the OMA could be enhanced by increasing the EAM driving Vpp at the cost of consuming more transmitter power. A higher OMA reduces the requirement for the receivers sensitivity, which in turn reduce the receiver's power consumption [17]. Therefore, with our photonic models and simulation methodology, the transmitter and receiver could be co-optimized for minimizing the overall power consumption while meeting the transmission quality requirement.

IV. CONCLUSION

We develop accurate circuit-level models for silicon photonic devices based on their electrical and optical properties. Our models have been successfully validated in multiple aspects based on the measurement data of the fabricated photonic devices. Using our SPICE-compatible Verilog-A models, we have simulated a full optical transceiver link in SPICE, and demonstrated an excellent agreement between the measured and simulated results. Additionally, our photonics-aware design space explorations reveal the benefits of exploring photonic devices for design optimization, and the trade-off between transmitter power, OMA, and receiver power. Overall, our models and simulation methodology could enable electro-optical co-simulation, allowing designers to co-optimize photonic devices with electronic circuits seamlessly.

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REFERENCES

[1] R. G. Beausoleil, "Large-scale integrated photonics for high-performance interconnects," *ACM Journal on Emerging Technologies in Computing Systems*, vol. 7, no. 2, p. 6, 2011.
[2] L. Chrostowski *et al.*, "Design methodologies for silicon photonic integrated circuits," *SPIE Smart Photonic and Optoelectronic Integrated Circuits Conf.*, pp. 1–15, 2014.
[3] L. Duong *et al.*, "Coherent crosstalk noise analyses in ring-based optical interconnects," in *DATE*, 2015.
[4] H. Li *et al.*, "Thermal aware design method for vcsel-based on-chip optical interconnect," in *DATE*, 2015.
[5] R. Wu *et al.*, "Variation-aware adaptive tuning for nanophotonic interconnects," in *ICCAD*, 2015.
[6] M. Georgas *et al.*, "Addressing link-level design tradeoffs for integrated photonic interconnects," in *Custom Integrated Circuits Conf. (CICC)*, pp. 1–8, IEEE, 2011.
[7] R. Wu *et al.*, "Compact models for carrier-injection silicon microring modulators," *Optics Express*, vol. 23, no. 12, pp. 15545–15554, 2015.
[8] R. Wu *et al.*, "Large-signal model for small-size high-speed carrier-injection silicon microring modulator," in *Integrated Photonics Research, Silicon and Nanophotonics Conf. (IPR)*, pp. IW1B–4, Optical Society of America, 2016.
[9] J. Rhim *et al.*, "Verilog-a behavioral model for resonance-modulated silicon micro-ring modulator," *Optics express*, vol. 23, no. 7, pp. 8762–8772, 2015.
[10] K. Zhu *et al.*, "Compact verilog-a modeling of silicon traveling-wave modulator for hybrid cmos photonic circuit design," in *Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 615–618, IEEE, 2014.
[11] B. Wang *et al.*, "A comprehensive vertical-cavity surface-emitting laser model for optical interconnet transceiver circuit design," *Optical Engineering*, 2016.
[12] C. Zhang *et al.*, "8× 8× 40 gbps fully integrated silicon photonic network on chip," *Optica*, vol. 3, no. 7, pp. 785–786, 2016.
[13] L. A. Coldren *et al.*, *Diode lasers and photonic integrated circuits*, vol. 218. John Wiley & Sons, 2012.
[14] Y. Tang, *Study on electroabsorption modulators and grating couplers for optical interconnects*. PhD thesis, 2010.
[15] M. K. Smit and C. Van Dam, "Phasar-based wdm-devices: Principles, design and applications," *IEEE Journal of Selected Topics in Quantum Electronics*, 1996.
[16] M. A. Seyedi *et al.*, "Crosstalk analysis of ring resonator switches for all-optical routing," *Optics Express*, vol. 24, no. 11, pp. 11668–11676, 2016.
[17] C. Li *et al.*, "A ring-resonator-based silicon photonics transceiver with bias-based wavelength stabilization and adaptive-power-sensitivity receiver," in *Int'l Solid-State Circuits Conf. (ISSCC)*, IEEE, 2013.