SIEMENS EDA

Calibre® xL User's Manual

Software Version 2021.2
Document Revision 14

SIEMENS

Support Center: support.sw.siemens.com
Send Feedback on Documentation: support.sw.siemens.com/doc_feedback_form

Revision History

Revision	Changes	Status/ Date
14	Modifications to improve the readability and comprehension of the content. Approved by Lucille Woo. All technical enhancements, changes, and fixes listed in the *Calibre Release Notes* for this products are reflected in this document. Approved by Michael Buehler.	Released April 2021
13	Modifications to improve the readability and comprehension of the content. Approved by Lucille Woo. All technical enhancements, changes, and fixes listed in the *Calibre Release Notes* for this products are reflected in this document. Approved by Michael Buehler.	Released January 2021
12	Modifications to improve the readability and comprehension of the content. Approved by Lucille Woo. All technical enhancements, changes, and fixes listed in the *Calibre Release Notes* for this products are reflected in this document. Approved by Michael Buehler.	Released October 2020
11	Modifications to improve the readability and comprehension of the content. Approved by Lucille Woo. All technical enhancements, changes, and fixes listed in the *Calibre Release Notes* for this products are reflected in this document. Approved by Michael Buehler.	Released July 2020

Author: In-house procedures and working practices require multiple authors for documents. All associated authors for each topic within this document are tracked within the Siemens EDA documentation source. For specific topic authors, contact the Siemens Digital Industries Software documentation department.

Revision History: Released documents maintain a revision history of up to four revisions. For earlier revision history, refer to earlier releases of documentation which are available on https://support.sw.siemens.com/.

Table of Contents

List of Figures

List of Tables

Chapter 1
Introduction to Calibre xL

Calibre® xL is a tool that extracts parasitic inductance on interconnects in IC layouts. It can also calculate frequency-dependent self impedance and mutual impedance.

This chapter includes sections that provide an overview of the Calibre xL product.

Calibre xL Overview

Calibre xL offers designers parasitic on-chip inductance extraction, which is crucial for accurate physical verification and timely tape-out of high-frequency RF, mixed signal and custom digital designs.

Calibre xL is a software tool that extracts *parasitic inductance* on interconnects in IC layouts. This tool also calculates frequency-dependent *self impedance* and *mutual impedance*.

Use the Calibre xL tool to assess and minimize the effect of inductance and inductive coupling on designs that operate at *high frequencies*. At high frequencies, parasitic inductance has a major impact on chip performance and can cause chip failure if inductance is not properly detected and corrected.

For information on the inductance problems that Calibre xL addresses for analog designs, radio frequency (RF) designs, and digital designs and the extraction models used to address these problems, see “Types of Inductance Problems and Extraction Models” on page 17.

Calibre xL Tool Flow

The Calibre xL tool runs as a supplementary step in the parasitic extraction flow.

Data from the Calibre xL tool feeds back into the Calibre® xRC™ formatter, which produces the parasitic netlist. Figure 1-1 shows how Calibre xL fits into the parasitic extraction flow. For more information, refer to Table 1-1.

Figure 1-1. Calibre xL in the Parasitic Extraction Flow

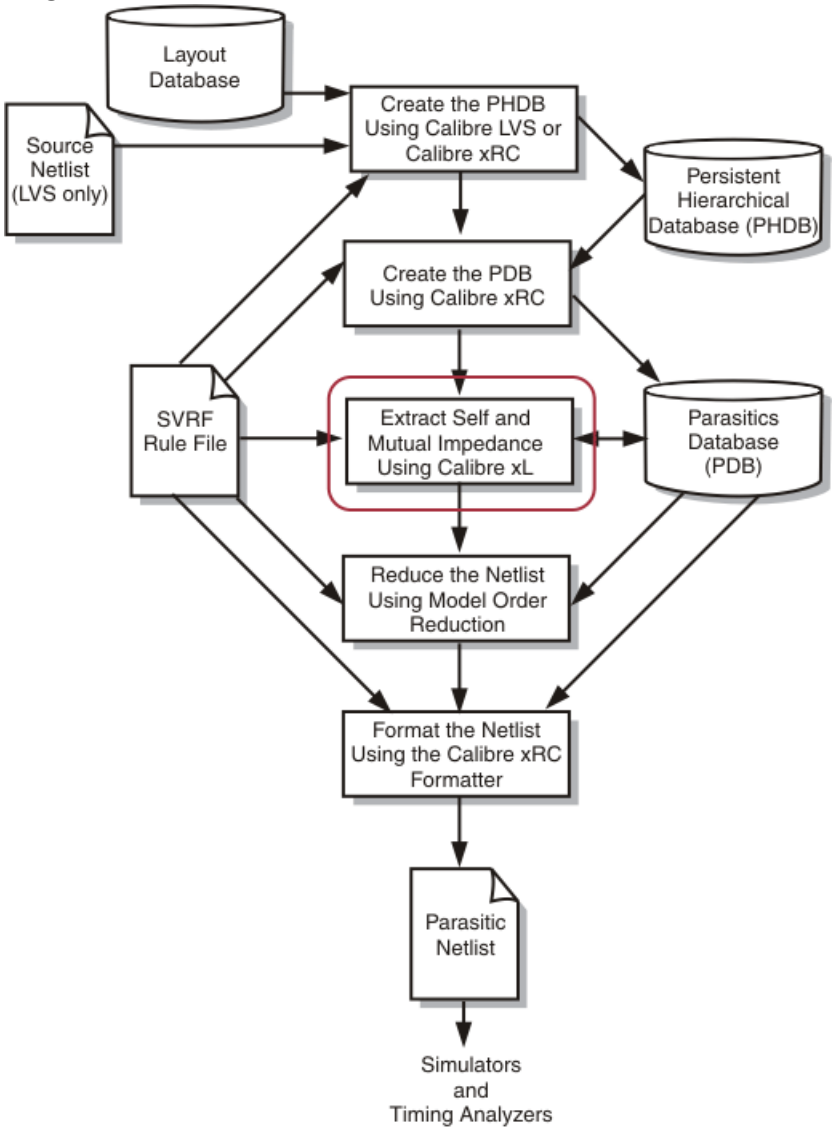


Table 1-1. Using Calibre xL in the Parasitic Extraction Flow

Step	Action	Comments
1	Create the PHDB.	The Persistent Hierarchical Database, usually referred to as the PHDB, contains information about your design's layout, connectivity, and the devices necessary for calculating the parasitic information. You can create the PHDB with the Calibre® nmLVS-H™ tool or the Calibre xRC tool.
2	Create the PDB.	The Parasitics Database, usually referred to as the PDB, stores the parasitic models for each extracted net. You create the PDB using the Calibre xRC tool. You can run this step multiple times without regenerating the PHDB.

Table 1-1. Using Calibre xL in the Parasitic Extraction Flow (cont.)

3	Extract self and mutual impedance.	You add inductance rules to the SVRF rule file if not already added, identify the *path* of *victim nets*, and then run the Calibre xL tool to extract self and mutual impedance. Inductance information is added to the PDB. **Note:** You can create the PHDB, create the PDB, and extract self and mutual impedance in one run if desired. The Calibre xL tool produces a report file containing information about the paths included in mutual impedance extraction.
4	Reduce the netlist.	Before formatting the netlist, you turn on reduction so the netlist is more easily simulated.
5	Format the netlist.	You produce and format the netlist using the Calibre xRC formatter. The parasitic netlist can be produced in any of the following formats: • Eldo • SPEF • SPECTRE • HSPICE • CalibreView • DSPF

Calibre xL Requirements

Running Calibre xL extraction requires that certain condition be met.

You must have the following to run the Calibre xL tool:

- A layout database for which connectivity is defined.
- An optional source netlist if you require schematic names for the nets in the parasitic netlist.
- An SVRF rule file containing Calibre-specific SVRF statements and operations.
- Calibre version 2007.1 or higher.
- All necessary licenses. At a minimum, you must have a Calibre xL license. Additional licenses may be required depending on the operations performed. For licensing information, see the "Calibre xL Licensing" section of the *Calibre Administrator's Guide*.

How to Run Calibre xL

Calibre xL can be run from the command line or through a graphical user interface.

You can run the Calibre xL tool using either of following methods:

- Creating a shell script and running it from the command line. See "Running Calibre xL From the Command Line" on page 25.
- Interactively from the Calibre® Interactive™ graphical user interface. See "Running Calibre xL From Calibre Interactive" on page 31.

Syntax Conventions

The command descriptions use font properties and several metacharacters to document the command syntax.

Table 1-2. Syntax Conventions

Convention	Description
Bold	Bold fonts indicate a required item.
Italic	Italic fonts indicate a user-supplied argument.
`Monospace`	Monospace fonts indicate a shell command, line of code, or URL. A bold monospace font identifies text you enter.
Underline	Underlining indicates either the default argument or the default value of an argument.
UPPercase	For certain case-insensitive commands, uppercase indicates the minimum keyword characters. In most cases, you may omit the lowercase letters and abbreviate the keyword.
[ ]	Brackets enclose optional arguments. Do not include the brackets when entering the command unless they are quoted.
{ }	Braces enclose arguments to show grouping. Do not include the braces when entering the command unless they are quoted.
‘ ’	Quotes enclose metacharacters that are to be entered literally. Do not include single quotes when entering braces or brackets in a command.
| or ||	Vertical bars indicate a choice between items. Do not include the bars when entering the command.
…	Three dots (an ellipsis) follows an argument or group of arguments that may appear more than once. Do not include the ellipsis when entering the command.

Table 1-2. Syntax Conventions (cont.)

Example:

DEVice {***element_name*** [‘(’*model_name*‘)’]}
device_layer {***pin_layer*** [‘(’*pin_name*‘)’] …}
[‘<’*auxiliary_layer*‘>’ …]
[‘(’*swap_list*‘)’ …]
[BY NET | BY SHAPE]

Chapter 2
Types of Inductance Problems and Extraction Models

Calibre xL provides different solutions depending on your inductance analysis needs.

This chapter provides information on the different types of inductance problems Calibre xL addresses and the models used to address these problems.

Problems Calibre xL Addresses

Inductance problems vary depending on the design type.

The Calibre xL tool addresses the different types of inductance problems depending on the following types of designs:

- Analog Designs
- Radio Frequency Designs
- Digital Designs

Analog Designs

The Calibre xL tool addresses the following inductance problems in analog designs:

- Ringing
- Instability
- Degradation of noise figure
- Reflections due to impedance mismatch in signal and control lines

The Calibre xL tool provides accurate circuit representation for the wires valid for any frequency less than 50 GHz. The circuit representation includes dynamic resistance and self and mutual inductance. You can use the Calibre xL tool in narrow frequency mode or broadband mode.

The Calibre xL tool addresses the inductance problems in analog designs with the following:

- High Accuracy Extraction
- Self Impedance Extraction
- Mutual Impedance Extraction for noise applications
- Model Order Reduction

Radio Frequency Designs

The Calibre xL tool addresses the following inductance problems in radio frequency (RF) designs:

- Drift in voltage controlled oscillator (VCO) frequency of oscillation and degradation of low noise amplifier (LNA) noise for block-level signal lines. These problems are caused by sensitivity to small changes in impedance.
- Reduced gain and bandwidth of RF system for system-level integration.

The Calibre xL tool provides the following output for circuit analysis to these problems:

- Self Impedance Extraction and Differential Pair Extraction
- Model Order Reduction
- Skin and Proximity Effects when it matters

Digital Designs

The Calibre xL tool addresses the following inductance problems in digital designs:

- Cross-talk noise and delay for signal lines where it matters
- Clock skew for clock

The Calibre xL tool provides accurate broadband circuit netlist representation incorporating frequency dependent effects. You can control the following features:

- Net Filtering
- Model Order Reduction
- Trade-off between speed and accuracy
- Selected Net Extraction

Extraction Models

Calibre xL supports several extraction models.

Common extraction models supported by Calibre xL include:

- Self Impedance Extraction
- Mutual Impedance Extraction
- Skin and Proximity Effects
- Broadband Netlist Generation
- Differential Pair Extraction
- Partial RLK Extraction

Self Impedance Extraction

Using the Calibre xL tool, you can extract frequency dependent loop self impedance from your layout. Self impedance can be significant when your design contains nets with long paths that are not shielded. Loop self impedance is inductance associated with a signal and its current return path. Loop impedance is the joint impedance of the signal line and all its return wires.

Mutual Impedance Extraction

Using the Calibre xL tool, you can extract mutual impedance from your layout. Mutual impedance can be significant when your design contains nets with long paths. Mutual impedance measures the full electromagnetic effect of one current loop over another. Mutual impedance extraction is based on paths. A path is a unique two-point terminal connection (belonging to a wire net) between two devices. You can identify victim paths in either of two ways:

- Directly by creating an ASCII file containing PEX Inductance Victim statements that specify the victim net names.
- Interactively using the Calibre® Interactive™ tool.

The Calibre xL tool automatically determines the victim paths. You can identify pairs of nets targeted for mutual impedance extraction by using the PEX Inductance Victim statement in your SVRF rule file as follows:

```
PEX INDUCTANCE VICTIM NET1 NET1 t tube_radius
PEX INDUCTANCE VICTIM NET2 NET2 t tube_radius
```

The tube_radius value specified in microns, must be larger than the maximum distance between NET1 and NET2 if you want to ensure mutual inductance is extracted between them. A return path must also be specified and present in the GDS layout in order to perform this type of extraction. For more information on specifying a return path, see PEX Inductance Returnpath statement.

Skin and Proximity Effects

Using the Calibre xL tool, you can model skin and proximity effects. Usually, skin effect is present in IC layout designs that operate at frequencies above 15 GHz. Proximity effect materializes at about 1 GHz. Skin and proximity effects influence the self and mutual impedance on interconnects in the layout. The Calibre xL tool determines the proper number of filaments for all nets and at any frequency, in order to achieve the best accuracy and performance. Skin effects are calculated by default for all nets.

Broadband Netlist Generation

For accurately capturing broadband ($0 < f < f_{max}$) behavior of impedance, use a broadband model. To specify f_{max} for a broadband model, use the following statements in your SVRF rule file:

- PEX Inductance ... Switch Time to specify the switching time.
- PEX Inductance Frequency with the MAXIMUM keyword option to specify the maximum operating frequency.

A broadband model permits the emulation of a linear circuit with impedance coefficients that are constant. This circuit provides a similar response to the frequency dependent one. A broadband model is especially useful for circuit simulation in the time domain.

Differential Pair Extraction

You can identify a pair of signal nets operating in a differential signaling mode by specifying the PEX Inductance Differential Pair statement in your SVRF rule file. For nets specified as members of a differential pair, Calibre xL extracts the partial self and mutual inductance, and not loop inductance as in the case of single-ended signals where power or ground nets serve as return paths. Power and ground nets can not be specified as part of a differential pair. A PEX Inductance Differential Pair statement can be specified for each differential pair in your design. For example, the following statements extract partial self and mutual inductance for NET1 and NET2, and for NET3 and NET4:

```
PEX INDUCTANCE DIFFERENTIAL PAIR SOURCENAMES NET1 NET2
PEX INDUCTANCE DIFFERENTIAL PAIR LAYOUTNAMES NET3 NET4
```

A design can have signal nets marked as differential pairs and regular single-ended signals. If the PEX Inductance Returnpath NONE statement is specified with the PEX Inductance Differential Pair statement, then only partial quantities for the differential pair nets are computed and netlisted. When specified with one of the GROUND, POWER, GANDP, or GANDPAVG keywords, Calibre xL extracts and netlists partial inductance quantities for the differential pairs and loop quantities for the single-ended signals.

Partial RLK Extraction

Partial RLK extraction is based on an implementation of the Partial Element Equivalent Circuit method[1](PEEC). All length and frequency filtering applicable to loop-L inductance is also applicable to PEEC inductance.

Interconnect conductors do not provide the same shielding effect for inductive interactions as they do for capacitive ones; therefore, inductive coupling is a longer-range effect than capacitive coupling. In LOOP mode, inductive interactions between signal interconnects and the return current paths are taken into account and incorporated in the loop self-inductances. In PEEC mode, these interactions appear as mutual inductors in the extracted netlist. Thus PEEC mode produces a larger number of parasitic inductances in the extracted netlist compared to LOOP mode. Care should be taken when selecting nets and layers for partial inductance extraction, especially if they involve large power or ground nets.

Details of PEEC mode in Calibre xL:

- PEEC mode is only valid for select net extraction using the -select command line parameter during the parasitic extraction stage (-pdb -select) and the PEX Extract Include statement to specify the nets. Power and ground nets may be part of the selected net set. If the PEX Inductance Mode PEEC statement is specified and you do not specify the -select command line option, Calibre xL generates an error and stops.
- The -rl and -rlm extraction options are equivalent in PEEC mode since mutual inductors are extracted and netlisted by default. Calibre xL automatically determines all significant inductive couplings in the layout and extracts the corresponding mutual inductors.Calibre xL also automatically identifies nets, which at certain high frequencies develop the “skin effect”, and takes this into account while calculating the parasitic inductive impedance values.
- Some inductance SVRF statements that control inductance extraction in LOOP mode are not pertinent for partial inductance extraction and are ignored. See Table 5-2 for a list of inductance SVRF statements that can be specified in PEEC mode.

See “Extracting Partial RLK Parasitics” on page 55 for an example on how to perform partial RLK extraction.

Netlist Reduction Techniques

You can reduce the size of the parasitic netlist by selecting specific nets for extraction, filtering nets, and performing model order reduction.

1. E.Ruehli, “Equivalent Circuit Models for Three Dimensional Multiconductor Systems”, IEEE Trans. Microwave Theory Tech. vol. MTT-22, pp. 216-222, March 1974

This section describes the following netlist reduction techniques:

- Selected Net Extraction
- Net Filtering
- Model Order Reduction

Selected Net Extraction

You can include or exclude certain nets from extraction or limit the parasitic extraction to a list of specified nets. To include certain nets, use either of the following:

- The PEX Extract Include statement in your SVRF rule file and specify the -select parameter on the command line.
- The PEX "Extract parasitics for specified nets" option in Calibre Interactive.

To exclude certain nets (such as ground and power) from an extraction run, use the PEX Extract Exclude statement in your SVRF rule file. For information on the PEX Include Distributed and PEX Exclude Distributed statements, see the *Standard Verification Rule Format (SVRF) Manual*.

Net Filtering

You can filter out short paths to reduce the netlist size and enable full-chip simulation and analysis. The filtering is done on a per-path basis. Only signal paths that violate the filtering conditions are excluded from impedance extraction.

To apply this filter let the tool approximate the location of the two terminals of the paths (driver and receiver) or you may specify the driver and receiver paths in a file yourself. Note that the value of the rise time or maximum frequency also participate in the path length calculation, that is the criteria for filtering. For more information, see "Driver and Receiver File Generation" on page 56.

To specify the nets to include in the return path, use either of the following:

- The PEX Inductance Returnpath statement in your SVRF rule file.
- The PEX "Nets to include in return path" option in Calibre Interactive.

Model Order Reduction

You can reduce the parasitic netlist size to enable an efficient simulation using the TIme Constant Equilibration Reduction (TICER) algorithm. This algorithm reduces the model order while accurately preserving network response for specified upper frequency limits. You can specify the highest frequency of interest up to which the reducer accurately preserves network response. For consistency, this frequency should be less than or equal to the frequency specified for extraction. The TICER algorithm is an efficient method of reduction and does not change

the electrical behavior of the circuit below the specified cut-off frequency. The specified cut-off frequency is used as the basis for minimizing the number of parasitics added to the netlist.

To specify model order reduction, use either of the following:

- The PEX Reduce TICER statement in your SVRF rule file.
- The PEX "Enable TICER Reduction Below" option in Calibre Interactive.

Net Frequency

The Calibre xL tool extracts impedance using a global operating frequency for all the signal nets in the design.

The global operating frequency specifies the operating frequency of the circuit and the frequency to use on nets during impedance extraction. The default value for the frequency is 10 GHz. To change the default, use either of the following:

- The PEX Inductance Frequency statement in your SVRF rule file.
- The PEX "Operating Frequency" option in Calibre Interactive.

You can also use the PEX Inductance Frequency statement to specify the global maximum operating frequency for all the signal nets in the design.

Chapter 3
Running Calibre xL From the Command Line

The commands for Calibre xL can be entered at the console prompt or in a batch file.

This chapter provides information on how to run the Calibre xL tool from the command line.

Before Running Calibre xL

Running Calibre xL extraction from the command line requires that certain condition be met.

Before running Calibre xL, you need to:

- Update the Standard Verification Rule Format (SVRF) rule file with inductance rules. For more information, see "Calibre xL SVRF Rule File Reference".
- Set the path to the Siemens EDA software. For details, see "Setting the CALIBRE_HOME Environment Variable".

Step 1: Create the PHDB

You can create the PHDB with the Calibre nmLVS-H tool or the Calibre xRC tool.

Follow one of these methods to create the Persistent Hierarchical Database (PHDB).

Prerequisites

You must have the following:

- A layout database for which connectivity is defined. It is recommended that you name the nets in your layout database to traceable results in the parasitic netlist. The Calibre software can read GDS, OASIS®[1], and LEF/DEF formats. For information on using a

1. OASIS® is a registered trademark of Thomas Grebinski and licensed for use to SEMI®, San Jose. SEMI® is a registered trademark of Semiconductor Equipment and Materials International.

LEF/DEF input layout database, see "How to Run With LEF/DEF Input" in the *Calibre xRC User's Manual*.

- A source netlist if you require schematic names for the nets in the parasitic netlist. The source netlist must be in SPICE format and identified in the SVRF rule file or through Calibre Interactive.
- An SVRF rule file containing Calibre-specific SVRF statements and operations. For information on SVRF rules used by the Calibre® nmLVS™ and Calibre xRC tools, see the *Standard Verification Rule Format (SVRF) Manual*. For information on SVRF rules used by the Calibre xL tool, see "Calibre xL SVRF Rule File Reference" on page 39.

Procedure

1. **Using Source Names** — Follow this method when you want the parasitic netlist to use source names for the nets.
2. In the SVRF rule file, specify Source Path and Source Primary in addition to Layout Path and Layout Primary.
3. From the shell command line, enter the following:

   ```
   calibre -lvs -hier -spice directory_path/filename.sp rule_file_name
   ```

   For the output to be used in extraction, *directory_path* must match the *directory_path* specified in the Mask SVDB Directory statement, and *filename* must be the cell name of the Layout Primary statement.

   For more information on the command line options, see "calibre -lvs" and the "Calibre nmLVS and Calibre nmLVS-H Command Line" section of the *Calibre Verification User's Manual*.

   The following files are output:

   - PHDB — The PHDB is stored in the Standard Verification Database (SVDB) and used in creating the PDB.
   - layout netlist — This is the SPICE netlist that the Calibre xRC tool will use for input in the next step, Step 2: Create the PDB. This file is named after the top-level cell.
   - *lvs.rep* file — This ASCII file contains the results of the LVS run. It is not used in parasitic extraction.
   - *lvs.rep.ext* file — This ASCII file contains the results of the circuit extraction. It is not used in parasitic extraction.
4. **Using Layout Names** — Follow this method when you want the parasitic netlist to use layout names for the nets.
5. In the SVRF rule file, specify Layout Path and Layout Primary.

6. From the shell command line, enter the following:

   ```
   calibre -xrc -phdb rule_file_name
   ```

   For a complete list of command line options, see “calibre -xrc -phdb” on page 48.

   The PHDB is only generated once per layout. You do not need to regenerate the PHDB unless your design changes, or you modify the SVRF connectivity rules.

   The following files are output:

   - PHDB — The PHDB is stored in the Standard Verification Database (SVDB) and used in creating the PDB.
   - layout netlist — This is a SPICE netlist that the Calibre xRC tool will use for input in the next step, Step 2: Create the PDB. This file is named after the top-level cell.

Step 2: Create the PDB

Create the PDB with Calibre xRC.

If you want to extract capacitance and resistance in one run before extracting impedance, refer to the *Calibre xRC User’s Manual* for information on creating the PDB; otherwise, skip to Step 3: Extract Self and Mutual Impedance.

Step 3: Extract Self and Mutual Impedance

Follow this procedure when you need to create the PDB and extract self and mutual impedance from your layout. This step can be run multiple times without regenerating the PHDB.

Prerequisites

- You must have created the PHDB; if not, see “Step 1: Create the PHDB”. If you are performing multiple runs, you must use the same PHDB each time. The PHDB must be in the SVDB directory.
- You must have created an SVRF rule file containing capacitance and resistance statements. These statements are usually provided by the foundry or a corporate CAD group and included by reference. For information on the statements you need to add to your SVRF rule file, refer to the *Calibre xRC User’s Manual.*
- You must have updated your SVRF rule file with the Calibre xL basic statements you want to use. Following are the Calibre xL optional basic statements:
  - PEX Inductance Frequency — Specifies the global maximum operating frequency of impedance extraction for all the signal nets in the design.

- PEX Inductance Returnpath — Specifies the type of nets (ground or power) that may be considered as candidates for return path in impedance extraction. Only linear paths along layout axes are recognized.
- PEX Ground — Specifies one or more ground net names to consider during impedance extraction.
- PEX Power — Specifies one or more power net names to consider during impedance extraction.

Following are the Calibre xL optional statements that affect self impedance extraction:

- PEX Generate Driver File Tag — Specifies to generate a driver and receiver file.
- PEX Inductance Driver File — Specifies the location of the driver and receiver file.
- PEX Inductance Filter — Specifies whether or not to filter paths for impedance extraction.
- PEX Inductance Self — Specifies the self impedance value to use on wire segments that are filtered.

For a list of advanced statements, see Table 5-1.

- You must have an xcell file if you are performing hierarchical extraction. If you are performing a transistor-level extraction, you do not need an xcell file.

Procedure

1. Create a victim file with the name *victim.xl* and specify one or more victim nets with the PEX Inductance Victim statement.
2. In the SVRF rule file, add an Include statement to specify the location of the victim file.

   ```
   INCLUDE "location/victim"
   ```

3. From the command line shell, enter the following on one line:

   ```
   calibre -xrc -pdb extraction_options parasitic_options\
   additional_options rule_file_name
   ```

   Table 3-1 summarizes the command-line invocation when extracting parasitics. You can specify only one extraction option and one parasitic option per run. For more information on the command line options, see "calibre -xrc -pdb".

Table 3-1. Invocation Line for Extracting Parasitics

Required	Extraction Options[1]	Parasitic Options[1]	Additional Options	Required
	no switch (flat)	-l	-cb	
calibre -xrc -pdb	-xcell ***xcell_file***	-m	-asic/-noasic	***rule_file***
	-xcell ***xcell_file*** -full	-rl	-select	

Table 3-1. Invocation Line for Extracting Parasitics (cont.)

Required	Extraction Options[1]	Parasitic Options[1]	Additional Options	Required
	-xcell ***xcell_file*** -incontext	-lm	-nocheck	
		-rcl	-pdb_info	
		-rccl		
		-rlm		
		-rclm		
		-rcclm		

1. Choose only one from this column.

Examples

Example 1

The following statement instructs the Calibre xL tool to perform incremental self impedance extraction using the SVRF rule file named *my_rules*.

```
calibre -xrc -pdb -l my_rules
```

Example 2

The following statement instructs the Calibre xL tool to perform self and mutual impedance extraction using the xcell named *hcell_list3* and the SVRF file named *my_rules*.

```
calibre -xrc -pdb -lm -xcell hcell_list3 my_rules
```

Step 4: Reduce the Netlist

If you have not already done so, edit your SVRF rule file to specify netlist reduction during the formatter stage.

You can add the PEX Reduce TICER statement to your SVRF rule file to reduce the netlist. You can also reduce the netlist using threshold-based and tolerance-based reduction. Refer to the *Calibre xRC User's Manual* for details.

Step 5: Format the Netlist

You can run the Calibre xRC formatter any number of times without rerunning the Calibre xL tool. Normally, you rerun the formatter multiple times to get different results for different analyses, such as R-only for IR drop analysis or RCLM for inter-stage matching.

Follow this procedure to produce a parasitic netlist.

Prerequisites

- You must have created the PDB; if not, see "Step 2: Create the PDB" on page 27.
- You must have the PEX Netlist statement in the SVRF rule file. For more information, see "Other Required SVRF Statements" on page 43.

Procedure

From the command line shell, enter the following:

```
calibre -xrc -fmt option rule_file
```

Table 3-2 describes the options for formatting the contents of the PDB into a parasitic netlist. For complete information, see "calibre -xrc -fmt" on page 53.

Table 3-2. Formatter Options

Option	Result
-rl	Writes only resistance and inductance models into the netlist.
-rcl	Writes resistance, inductance, and capacitance models into the netlist.
-rccl	Writes resistance, inductance, and coupled capacitance models into the netlist.
-rcc	Writes resistance and coupled capacitance models into the netlist.
-all[1]	Writes distributed results; it does not produce lumped capacitance.

1. This is the default and is recommended for most netlists.

Examples

```
calibre -xrc -fmt -all my_rules
```

Chapter 4
Running Calibre xL From Calibre Interactive

The Calibre xL tool can be run from Calibre's Graphical User Interface (GUI) tool known as Calibre Interactive.

The following procedures explain the steps necessary to run Calibre xL from Calibre Interactive. For additional details, see "Using Calibre Interactive to Perform Parasitic Extraction" in the *Calibre Interactive User's Manual*.

Before Running Calibre xL

Running Calibre xL extraction from Calibre Interactive requires that certain condition be met.

Before running the Calibre xL tool, you need to:

- Update the Standard Verification Rule Format (SVRF) rule file with inductance rules. For more information, see the appropriate sections in this chapter and "Calibre xL SVRF Rule File Reference" on page 39.
- Set the path to the Siemens EDA software. For details, see "Setting the CALIBRE_HOME Environment Variable" on page 45.

Step 1: Create the PHDB

Follow this procedure when you need to create the Persistent Hierarchical Database (PHDB).

Note

The following procedure describes how to create the PHDB using the Calibre xRC tool. For information on how to create the PHDB using the Calibre nmLVS tool, see the *Calibre Verification User's Manual*.

Prerequisites

You must have the following:

- A layout database for which connectivity is defined. It is recommended that you name the nets in your layout database to get traceable results in the parasitic netlist. The Calibre software can read GDS, OASIS, and LEF/DEF formats. For information on using a LEF/DEF input layout database, see "How to Run With LEF/DEF Input" in the *Calibre xRC User's Manual*.
- A source netlist if you require schematic names for the nets in the parasitic netlist. The source netlist must be in SPICE format and identified in the SVRF rule file or through Calibre Interactive.
- An SVRF rule file containing Calibre-specific SVRF statements and operations. You might create this file by editing a template provided by your CAD group or by loading a generic runset in Calibre Interactive and then modifying the settings through the Calibre Interactive interface. For information on SVRF rules used by the Calibre nmLVS and Calibre xRC tools, see the *Standard Verification Rule Format (SVRF) Manual*. For information on SVRF rules used by the Calibre xL tool, see the "Calibre xL SVRF Rule File Reference" on page 39.

Procedure

1. Enter the following command to start the Calibre DESIGNrev™ viewer:

   calibredrv

2. Choose **File > Open Layout Files** and select your design.
3. Choose **Verification > Run PEX**.

   The Calibre Interactive — PEX window opens. The Load Runset File dialog box also opens.

4. Type in a runset file name and click **OK**, or click **Cancel**.
5. Click the **Rules** button.
6. Click '**…**' next to the entry box for PEX Rules File to select the SVRF rule file, and click **Load**.
7. Click '**…**' next to the entry box for PEX Run Directory to select the run directory.
8. Click **Inputs**.
9. Click '**…**' next to the File entry box to select the name and location of the layout file.
10. Select the Format of the file.
11. Click **Outputs**.

12. Select the Extraction Type, and select the type of parasitics to extract (for example, “R + C + CC”).

    Note

    For information on the parasitic extraction types, see the *Calibre xRC User’s Manual*. You will select the type of parasitic inductance extraction later in “Step 3: Extract Self and Mutual Impedance” on page 34.

13. Click the **Netlist** tab.
14. Select the output netlist Format HSPICE.
15. Select LAYOUT for Use Names From.
16. Enter the desired parasitic netlist file name for File.
17. Click **Run Control**.
18. Click the **Advanced** tab.
19. Select “Run PHDB-generation step,” and unselect the other Run boxes.
20. Click **Run PEX**. The PHDB has been created when the run finishes without errors.

Step 2: Create the PDB

Follow this procedure to create the parasitic database (PDB).

You can run this step multiple times without regenerating the PHDB. Parasitics are added incrementally to the PDB. This is useful if you want to extract certain parasitics from a set of nets. You can also create the PHDB, create the PDB, extract inductance, and generate a parasitic netlist in one run. However, you need to set up for mutual impedance extraction before extracting inductance.

Note

This procedure assumes you are only creating the PDB and extracting parasitics using the Calibre xRC tool. If you want to create the PDB and extract inductance in one run, skip to “Step 3: Extract Self and Mutual Impedance” on page 34.

Prerequisites

- You must have created the PHDB; if not, see “Step 1: Create the PHDB” on page 31. If you are doing multiple runs, you must use the same PHDB each time. The PHDB must be in the SVDB directory.
- You must have created an SVRF rule file. For this step of parasitic extraction, the SVRF rule file must contain capacitance and resistance statements. These statements are usually provided by the foundry or a corporate CAD group and included by reference.

For information on the statements you need to add to your SVRF rule file, refer to the Calibre xRC User's Manual.

- You must have created an xcell file if you are doing a hierarchical extraction. If you are doing a transistor-level extraction, you do not need an xcell file.

Procedure

1. Click **Run Control**.
2. On the **Advanced** tab, select "Run PDB-generation step" and unselect the "Run PHDB-generation step".
3. Click **Run PEX**. The PDB has been created when the run finishes without errors.

Step 3: Extract Self and Mutual Impedance

Follow this procedure when you want to extract self and mutual impedance from your layout.

This step can be run multiple times without regenerating the PHDB. You will identify victim nets, update the SVRF rule file, and select the inductance extraction options.

Prerequisites

- You must have created the PHDB; if not, see "Step 1: Create the PHDB" on page 31.
- You must have created the PDB; if not, see "Step 2: Create the PDB" on page 33.

Procedure

1. From Calibre Interactive, click **Start RVE** to open the Calibre — RVE window.
2. Choose **Tools > Mutual Inductance**.
3. Select a target net (victim net) from the droplist of available nets or click on the layout icon () to select the nets interactively in the Calibre DESIGNrev layout viewer window. The **Driver** will automatically be identified.
4. The tags you can specify are "b" for base, "c" for collector, "d" for drain, "e" for emitter, "g" for gate, "n" for negative, "p" for positive, "s" for source, and "t" for text port. For example, if you know you want to select a drain or source as the driver, type "d s" in the **Driver Tags** entry box. This prevents you from selecting a device pin or port that is not a drain or source **Driver** list box. To change the list of tags that specify which of the device pins and ports you can select as the driver, edit the list of tags in the **Driver Tags** entry box.
5. To change a driver select one from the available list of drivers in the droplist. The selected driver for the **Target Net** appears in the **Driver** entry.

6. Enter the **Tube Radius** you want to use for the target net. The default entry is 60 microns. For more information, see "Controlling How Calibre xL Selects Aggressor Nets" on page 57.
7. Click **Select Net** to add the selected net into the list to be exported to the victim file.
8. Repeat steps 3 through 7 for each victim net you want to add to the list.

Note

To view a victim net in the layout, select the net in the Selected Nets box, right click and select **Highlight Net** from the pop-up menu to view the net in the Calibre DESIGNrev window. This is useful when you want to examine the layout to see that you have specified the correct net or the appropriate tube radius. To delete a victim net from the list, select the net in the Selected Nets box and right click to select **Delete** from the pop-up menu.

9. When you finish selecting target nets, click **Save Victim File**. This creates the victim file that contains the victim nets.
10. Click **OK** to accept the default file name *victim.xl*, type a new file name, or select a different file name from the directory listing shown. By default, the Calibre RVE viewer saves this file in your working directory.
11. You may close the Mutual Inductance tab when you finish.
12. Update the SVRF rule to specify the location of the victim file using the Include statement:

```
INCLUDE "location/victim"
```

where *location* is the path to the file. By default, the Calibre RVE viewer stores these files in your working directory.

13. Return to the Calibre Interactive window, and select **Setup > PEX Options**.
14. From the **Netlist** tab click the **Reduction and CC** tab. Select "Enable TICER Reduction Below" to set up for netlist reduction during the netlist formatter stage, and type in a value for the highest frequency of interest up to which the reducer accurately preserves network response. For complete information, see PEX Reduce TICER statement.
15. Click the **Misc** tab.
16. The following options can be specified for controlling inductance extraction:
    - Power nets — Select whether or not to use layout or source net names when specifying power nets.
        - Layout — Use layout net names.
        - Source — Use source net names.

      For complete information, see PEX Power statement.

- Ground nets — Select whether or not to use layout or source net names when specifying ground nets.
  - Layout — Use layout net names.
  - Source — Use source net names.

  For complete information, see PEX Ground statement.
- Generate driver/receiver file — Select whether or not to generate a driver and receiver file for use in Calibre xRC extraction. If you selected this option, type in the driver and receiver file. The default driver file is *driver.xl*. Also, type in the tags for the driver and receiver file. For complete information, see PEX Generate Driver File Tag statement.

17. Click the **Inductance** tab.
18. The following options can be specified for controlling inductance extraction:
    - Broadband — Select whether or not to use broadband mode. Enabling Broadband enables the Switch Time entry box.
    - Operating Frequency — Type in a value for the global maximum operating frequency in GHz for any signal net in the design. The default is 10 GHz. For complete information, see PEX Inductance Frequency statement.
    - Switch Time — If you selected Broadband, you may alternatively select Switch Time to specify a global switch time. Type in a value for the global switch time in seconds to use during inductance extraction. For complete information, see PEX Inductance Switch Time statement.
    - Net Filter — Select the type of net filtering to apply:
      - Off — Do not filter nets.
      - Approx — Approximate an end point as driver (default).
      - File — Use drivers and receivers from the file specified using the PEX Inductance Driver File statement to recognize the current paths before applying filtering.

      For complete information, see PEX Inductance Filter.
    - Driver/Receiver File — If you selected File for Net Filter, you may then type in the path to a file containing driver and receiver information for inductance extraction, or click to browse for the file. The default is *driver.xl*. If you want to view the file, click **View**. For more information on the driver and receiver file, see “Driver and Receiver File Generation” on page 56 and PEX Inductance Driver File statement.
    - Driver/Receiver Tags — If you selected File for Net Filter, type in an optional list of values that specifies how to generate a driver and receiver file. For complete information, see PEX Inductance Filter statement.

- Use Victim Nets File — Select whether or not to use a victim nets file. The default is *victim.xl*. If you select this option, type in the filename or click to browse for the file.
- Inductance Range — Specifies how far to search from a given net segment for the return paths to be included in self impedance calculations. Select Cell Extent or type in a value in microns. The default is the extent of the chip. For complete information, see PEX Inductance Range statement.
- Nets to include in return path — Specifies the type of nets (Average, Ground, Power, Ground and Power, or None) that may be considered as candidates for return path in inductance extraction. The default is "Ground". For complete information, see PEX Inductance Returnpath statement.

19. Click **Outputs**.
20. For Extraction Type, select the type of parasitic inductance to extract "L (Self Inductance)" or "L + M (Self + Mutual Inductance)".
21. Click **Run Control**.
22. On the **Advanced** tab, check that the "Run PDB-generation step" is selected.

    Note

    If you want to extract inductance and create the parasitic netlist in one run, select "Run parasitic netlist generation step."

23. Click **Run PEX**. The PDB has been appended with inductance information when the run finishes without errors.

Step 4: Reduce the Netlist

Follow this procedure to perform reduction of distributed RC extraction data.

Procedure

1. Select PEX Options.
2. On the **Netlist** tab check that you selected "Enable TICER Reduction Below" and typed in a value for the highest frequency of interest up to which the reducer accurately preserves network response.

Step 5: Format the Netlist

Follow this procedure to generate a parasitic netlist.

Prerequisites

- You must have created the PHDB; if not, see "Step 1: Create the PHDB" on page 31.

- You must have created the PDB; if not, see “Step 2: Create the PDB” on page 33.
- You must have appended the PDB with inductance information; if not, see “Step 3: Extract Self and Mutual Impedance” on page 34.
- You must have added the PEX Netlist statement to the SVRF rule file.

Procedure

1. Click **Run Control**.
2. Click the **Advanced** tab.
3. Select “Run parasitic netlist generation step,” and deselect the “Run PDB-generation step.”
4. Click **Run PEX**. The parasitic netlist has been created when the run finishes without errors.

Chapter 5
Calibre xL SVRF Rule File Reference

Calibre xL has a specialized set of SVRF statements used to control inductance extraction.

This chapter provides detailed information on the Calibre xL SVRF statements:

SVRF Rule File Requirements

A Standard Verification Rule Format (SVRF) rule file is an ASCII text file containing SVRF statements and operations.

The Calibre tools use the SVRF rule file for reading in the layout data, processing the layer data, and extracting data. Operations control data manipulation, and statements prepare the environment in which the operations work.

You need to supply an SVRF rule file containing SVRF statements for:

- Parasitic impedance extraction for the Calibre xL tool — see "Calibre xL Statements" on page 41.
- Connectivity extraction and intentional device recognition for the Calibre nmLVS tool if you want schematic names in the parasitic netlist — see "Other Required SVRF Statements" on page 43.
- Parasitic resistance statements for the Calibre xRC tool — see "Other Required SVRF Statements" on page 43.

Optionally, you can specify other SVRF statements that affect parasitic impedance extraction. See "Other Optional SVRF Statements" on page 44.

For more information about the SVRF rule file, see the *Standard Verification Rule Format (SVRF) Manual*.

Calibre xL Rules

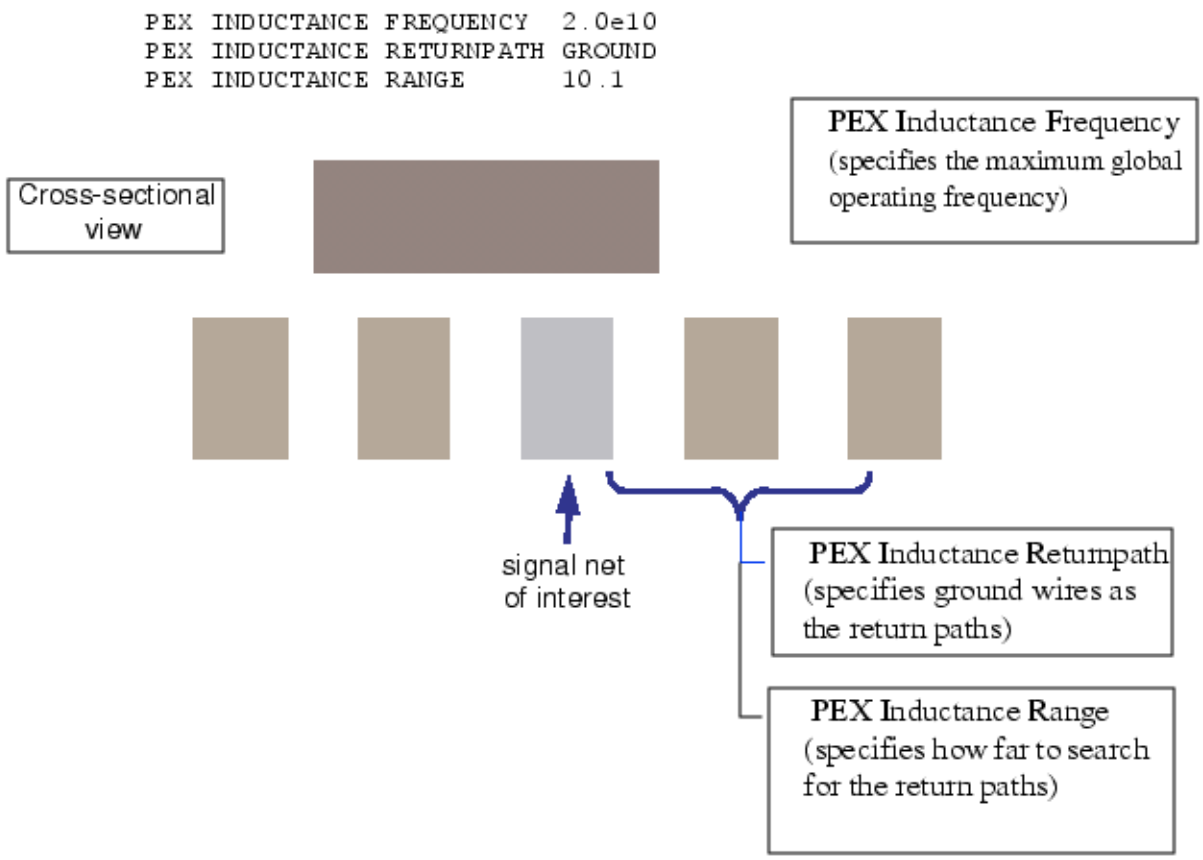
Use Calibre xL inductance rules to control parasitic impedance extraction.

Following are the categories of SVRF rules for parasitic impedance extraction:

- Layout database layer information rules — define the stacking height and thicknesses of conductor layers, some impedance information for each conductor layer, and equivalent layer information. See "Layer-Specific SVRF Statements" on page 59.
- Parasitic impedance rules — define the frequency, range, return path, and other parameters. See "Calibre xL Statements" on page 41.

Figure 5-1 shows how you control parasitic impedance extraction by specifying inductance rules in the SVRF rule file.

Figure 5-1. Explanation of Inductance Rules



Calibre xL Statements

There are several statements you can use in your SVRF rule file to control how the Calibre xL tool extracts parasitic inductive impedance.

The statements shown in Table 5-1 are used by the loop inductance extraction mode, which is the default inductance extraction mode. For more information on these statements, refer to the *Standard Verification Rule File (SVRF) Manual*.

Table 5-1. Calibre xL Statement Summary

SVRF Statement	Description
PEX Ignore Inductance	Causes inductance for the specified layer(s) or connections to be ignored during extraction.
PEX Inductance Differential Pair	Specifies two nets operating as a differential pair.
PEX Inductance Driver Summary	Specifies whether or not to output the driver summary data to the Calibre transcript during inductance extraction.
PEX Inductance Extract Layers	Specifies to process only geometries on the specified layers during inductance extraction.
PEX Inductance Frequency	Specifies the global operating frequency to use for impedance extraction for all the signal nets in the design.
PEX Inductance Minlength	Specifies the minimum path length used to accurately compute self inductance.
PEX Inductance Switch Time	Specifies the global switch time to use for all nets in the design.
PEX Inductance Range	Specifies how far to search from a given net segment for the return paths to include in self impedance calculations.
PEX Inductance Returnpath	Specifies the type of nets (ground or power) that may be considered as candidates for return path in impedance extraction.
PEX Ground	Specifies one or more ground net names to consider during impedance extraction.
PEX Power	Specifies one or more power net names to consider during impedance extraction.
Unit Inductance	Specifies the unit of inductance to use for calculating the self inductance of vias and bonding wires.
PEX Generate Driver File Tag	Specifies to generate a driver and receiver file. (This statement is used by the Calibre xRC tool.)
PEX Inductance Driver File	Specifies the location of the driver and receiver file.

Table 5-1. Calibre xL Statement Summary (cont.)

SVRF Statement	Description
PEX Inductance Filter	Specifies whether or not to filter paths for impedance extraction.
PEX Inductance Self	Specifies the PUL inductance value to use on wire segments that are filtered.
PEX Netlist Mutual Resistance	Specifies whether or not to use current-controlled voltage sources to model mutual resistance.
PEX Inductance Victim	Specifies a victim net.
PEX Inductance ... Frequency	Overrides the global operating frequency for specific nets.
PEX Inductance Max Returns	Specifies the maximum number of return paths used for inductance calculations.
PEX Inductance Mode	Specifies whether loop or partial inductive impedances are extracted.
PEX Inductance ... Switch Time	Overrides the global switch time for specific nets.

The statements shown Table 5-2 in are used by the PEEC inductance extraction mode.

Table 5-2. Statements Supported in PEEC Inductance Extraction Mode

SVRF Statement	Description
PEX Inductance Frequency	Specifies the global operating frequency to use for impedance extraction for all the signal nets in the design.
PEX Inductance Minlength	Specifies the minimum path length used to accurately compute self inductance.
PEX Ground	Specifies one or more ground net names to consider during impedance extraction.
PEX Power	Specifies one or more power net names to consider during impedance extraction.
PEX Inductance Filter	Specifies whether or not to filter paths for impedance extraction.
PEX Netlist Mutual Resistance	Specifies whether or not to use current-controlled voltage sources to model mutual resistance.
PEX Inductance Mode	Specifies whether loop or partial inductive impedances are extracted.

Other Required SVRF Statements

You need to specify the ground and power nets that you want the Calibre xL tool to consider during impedance extraction.

To do this, use either of these statements:

- PEX Ground or LVS Ground Name
- PEX Power or LVS Power Name

If the PEX Ground or PEX Power statement is not specified, the Calibre xL tool searches for LVS Ground Name and LVS Power Name statements to identify ground and power nets. If none of these statements are specified, the Calibre xL tool identifies nets with the name VSS? and GND? as ground nets and VDD? and VCC? as power nets. Ground and power nets must be linear and not skew.

You need to include one of the following three statements to set sheet resistance:

- Resistance Sheet — Specifies the sheet resistance.
- Resistance Rho — Specifies the rho (bulk resistivity) of a layer.
- Parasitic Variation — Enables you to modify nominal resistance calculations to more accurately model your fabrication process and account for in-die variations.

To view the parasitics in RVE, add the secondary keywords RLOCATION and RLAYER. For more information about the SVRF rule file, see the *Standard Verification Rule Format (SVRF) Manual*.

Inductance Reporting

You can optionally include the PEX Inductance Driver Summary statement in your SVRF rule file to control inductance information reported to the Calibre transcript.

The PEX Inductance Driver Summary statement controls whether or not to output the driver summary to the transcript. The Net column contains the net names and the Driver column

contains the driving pin name and tag for that net. The format of the summary looks similar to the following:

```
-------------------------------------------------------
DRIVER SUMMARY:

Net       Driver

VCTRL     "VCTRL T"
15        "X2 MINUS"
16        "X0 PLUS"
17        "X0 MINUS"
18        "X25/X0 MINUS"
19        "X24/X0 MINUS"
20        "X20/X0 MINUS"
21        "X21/X0 MINUS"
VGS       "VGS T"
25        "X1 D"
VOUT_L    "VOUT_L T"
VOUT_R    "VOUT_R T"
```

Other Optional SVRF Statements

Calibre xL uses various other SVRF statements that can affect inductance extraction output.

You can optionally include the following statements in your SVRF rule file:

- PEX Reduce Minmutual — Specifies to remove parasitic mutual inductance below a threshold value to reduce netlist size.
- PEX Reduce TICER — Specifies the highest frequency of interest up to which the reducer accurately preserves network response.
- PEX Inductance Extract Layers — Specifies to process only geometries on the specified layers during impedance extraction.
- PEX Extract Exclude — Specifies the nets to exclude from parasitic extraction.

  Note

  During a *compound run*, return paths are not excluded regardless of whether or not they are specified as excluded nets (for example, in the PEX Exclude Distributed statement). If you are running the Calibre xL tool using the -select switch, the Calibre xL tool extracts return path nets if they have not already been extracted.

- PEX Extract Include — Specifies the nets to include in parasitic extraction.

Chapter 6
Calibre xL Invocation Reference

Calibre xL command line options allow you to perform inductance extraction from the command line or with a run script.

This chapter provides detailed information on the command line options you can use to create the PHDB, the PDB, extract inductance, and format the parasitic netlist with Calibre xL.

Setting the CALIBRE_HOME Environment Variable

Calibre tools require that the CALIBRE_HOME environment variable be set.

See the "Setting the CALIBRE_HOME Environment Variable" section of the Calibre Administrator's Guide for details.

Command Descriptions

Inductance extraction with Calibre xL is a multiple stage process with various options at each stage.

This section covers the following tool invocation commands:

- For connectivity and device recognition — calibre -lvs
- For extraction and analysis of nets — calibre -xrc -phdb
- For parasitic data extraction — calibre -xrc -pdb
- For formatting the netlist or report — calibre -xrc -fmt

calibre -lvs

Runs the Calibre nmLVS-H tool and creates the Persistent Hierarchical Database (PHDB) for use by the Calibre xRC and Calibre xL tools.

Usage

calibre -lvs -hier -spice *directory_path/layout_primary.sp rule_file_name*

Description

When you invoke the Calibre nmLVS-H tool, you must specify an explicit path to the SVDB directory using the following syntax:

directory_path/layout_primary.sp

where:

- ***directory_path*** is the path you specified in the Mask SVDB Directory SVRF statement in the rule file.
- ***layout_primary.sp*** is the design's top-level cell you specified with the Layout Primary SVRF statement in the rule file.

For complete Calibre nmLVS-H information, see the "Calibre nmLVS and Calibre nmLVS-H Command Line" section of the *Calibre Verification User's Manual*.

Note

In standard nmLVS usage, you can specify any directory name for the SPICE netlist. To use the nmLVS output in the PDB stage, however, *directory_path* must match the Mask SVDB Directory setting.

Arguments

None.

Examples

The SVRF rule file is *design.rules* and contains the following SVRF statements:

```
LAYOUT PRIMARY "ring"
MASK SVDB DIRECTORY "/scratch1/design/svdb" XRC
```

You would invoke the Calibre nmLVS-H tool from the command line using the following syntax:

```
calibre -lvs -hier -spice /scratch1/design/svdb/ring.sp design.rules
```

calibre -xrc -phdb

Performs connectivity extraction and device recognition and writes results to a Persistent Hierarchical Database (PHDB).

Usage

calibre -xrc -phdb
[-cb | {[-turbo [*nmbr_of_cpus*] [-turbo_all] [-remote *host*[,*host*…] | -remotefile *filename*]}]
[-hcell *hcell_list*] [-E *output*] ***rule_file_name***

Description

Performs connectivity extraction and device recognition, and writes the results to a Persistent Hierarchical Database (PHDB). This command also generates a layout netlist from a layout. After this step, you create the Parasitic Database (PDB) and format the netlist.

You must regenerate the PHDB if it is inconsistent with a current run; this can occur if you change the rule file.

Arguments

- **-xrc**

  A required argument that performs parasitic extraction using the Calibre xRC tool. For the PHDB step, the netlists will contain layout names. Use calibre -lvs for schematic names.

- **-phdb**

  A required argument that runs connectivity extraction and device recognition on the layout database specified in the rule file and generates a PHDB.

  The resulting PHDB is named *layout_primary.phdb*, where *layout_primary* is the name specified by the Layout Primary specification statement in the rule file.

  This command also generates a layout netlist named *layout_primary.sp*, which is input to the Calibre xRC formatter.

  The Calibre xRC tool places both the PHDB and layout netlist in the SVDB directory.

- -cb

  See the *Calibre xRC User's Manual* for information.

- -turbo *number_of_cpus*

  An optional argument set that specifies using multi-threaded parallel processing for PHDB creation. The *number_of_cpus* argument is a positive integer specifying the number of processors (CPUs) to use in the processing. If you omit this number, the Calibre xRC tool runs on the maximum available for which you have licenses. If you do not apply the -turbo option, it defaults to running on two processors if available. To force the Calibre xRC tool to run on only one processor, specify "-turbo 1" on the command line.

  For more information on this option, refer to the *Calibre Administrator's Guide*.

- -turbo_all

  An optional argument used with the -turbo argument. This argument halts the invocation if it cannot secure the exact number of CPUs specified using -turbo.

- -remote *host*[, *host*…]

  An optional argument set used to run the software on remote hosts using the MTflex multi-threaded, parallel processing architecture. It must be specified in conjunction with the -turbo option. It enables multi-threaded operation on remote hosts of a distributed network. You must specify at least one *host* name. A list of hosts is comma-delimited and specifies that multiple hosts participate in multi-threaded operations. You must have the required number of licenses for your job.

  For more details, see the *Calibre Administrator's Guide*.

- -remotefile *filename*

  An optional argument set that is part of the MTflex multi-threaded, parallel processing architecture, which enables multi-threaded operation on remote hosts of a distributed network. It must be specified in conjunction with the -turbo option, which specifies the number of processors you are using, including those on the remote hosts. The *filename* specifies the pathname of a configuration file containing information for the local and remote hosts. You must have the required number of licenses for your job.

  For more details, see the *Calibre Administrator's Guide*.

- -hcell *hcell_list*

  An optional argument set that specifies the path to and name of the hcell file. For more information on hcells and xcells, see the *Calibre xRC User's Manual*.

- -E *output*

  An optional argument set that specifies an output file name for SVRF code generated by the TVF processor. If ***rule_file_name*** contains no TVF statements, *output* is empty. TVF code is processed before the run is started.

- ***rule_file_name***

  A required argument that specifies the path to and name of the SVRF rule file.

Examples

The following statement instructs the Calibre xRC tool to create the PHDB using the hcell file named *hcells* and the rule file named *my_rules*.

```
calibre -xrc -phdb -hcell hcells my_rules
```

calibre -xrc -pdb

Extracts parasitic data and performs analysis on the data within the PHDB.

Usage

calibre -xrc -pdb {**-l** | **-m** | **-rl** | **-lm** | **-rcl** | **-rccl** | **-rlm** | **-rclm** | **-rcclm**}
[-cb | [-turbo [*nmbr_of_cpus*] [-turbo_all]]]
[-xcell *xcell_file* [-incontext] | [-full]]
[-select] [-asic | -noasic]
[-nocheck] [-pdb_info]
[-E *output*] ***rule_file_name***

Note

As of the 2021.1 release, the -erc command line argument has been deprecated.

Description

Extracts parasitic data, depending on the option chosen, and performs analysis on the data within the PHDB. It also generates the Parasitic Database (PDB) containing the electrical data for each net.

Arguments

- **-xrc**

  A required argument that performs parasitic extraction using the Calibre xRC tool.

- **-pdb**

  A required argument that specifies to extract parasitic information and creates the PDB.

- **-l** | **-m** | **-rl** | **-lm** | **-rcl** | **-rccl** | **-rlm** | **-rclm** | **-rcclm**

  A required argument that specifies the extraction mode. You must specify one of the following:

  -l — Specifies incremental self impedance extraction. If the PDB has not been created, the Calibre xL tool runs the *-rl* option.

  -m — Specifies incremental mutual impedance extraction. If the PDB has not been created, the Calibre xL tool runs the *-rlm* option.

  -rl — Specifies parasitic resistance and self impedance extraction. It also overwrites selected nets.

  -lm — Specifies incremental self and mutual impedance extraction. If the PDB has not been created, the Calibre xL tool runs the *-rlm* option.

  -rcl — Specifies parasitic resistance, intrinsic capacitance, and self impedance extraction. It also overwrites selected nets.

  -rccl — Specifies parasitic resistance, coupled capacitance, and self impedance extraction. It also overwrites selected nets.

-rlm	Specifies parasitic resistance and self impedance and mutual impedance extraction. It also overwrites selected nets.
-rclm	Specifies parasitic resistance, lumped capacitance, and self and mutual impedance extraction. It also overwrites selected nets.
-rcclm	Specifies parasitic resistance, coupled capacitance, and self and mutual impedance extraction. It also overwrites selected nets.

- -cb

  See *Calibre xRC User's Manual* for information.

- -turbo *number_of_cpus*

  An optional argument set that specifies using multi-threaded parallel processing for PDB creation. The *number_of_cpus* argument is a positive integer specifying the number of processors to use in the processing. If you omit this number, the Calibre xRC tool runs on the maximum available for which you have licenses. If you do not apply the -turbo option, it defaults to running on two processors if available. To force the Calibre xRC tool to run on only one processor, specify "-turbo 1" on the command line.

  For more information on this option, refer to *Calibre Administrator's Guide*.

- -turbo_all

  An optional argument used with the -turbo argument. This argument halts the invocation if it cannot secure the exact number of CPUs specified using -turbo.

- -xcell *xcell_list*

  An optional argument set that specifies to create the PDB hierarchically. It specifies the path to and the name of the file containing a list of cells to be preserved during extraction (xcells). For more information on xcells, see the *Calibre xRC User's Manual*.

  When -xcell is specified without -incontext or -full, the primary cell is extracted to the boundaries of the xcells.

- -incontext

  An optional argument used with the -xcell argument to extract only those instances specified in the xcell list with a -C and a layout path. For more information, see the *Calibre xRC User's Manual*.

- -full

  An optional argument used in conjunction with the -xcell argument to perform hierarchical extraction with fully netlisted xcells. For more information, see the *Calibre xRC User's Manual*.

- -select

  An optional argument that specifies exclusively extracting nets using the net names you specify with PEX Extract Include SVRF statement.

- -asic | -noasic

  An optional argument that specifies whether or not to use ASIC optimizations. By default, ASIC optimizations are on for LEF/DEF input, and off for other formats. ASIC optimizations should only be used with gate-level extraction.

- -nocheck

  An optional argument that continues the extraction run with only a warning if file date stamps (commented checksums) are inconsistent with each other. If -nocheck is not specified and the date stamps are inconsistent, the extraction run stops.

- -pdb_info

  An optional argument that controls whether thresholding, driver recognition, and differential pair filtering messages from the analyzer are printed to the transcript. If you add the switch to the command line, messages from the analyzer are printed to the transcript. If you do not use the option, messages from the analyzer are not printed to the transcript.

- -E *output*

  An optional argument set that specifies an output file name for SVRF code generated by the TVF processor. If ***rule_file_name*** contains no TVF statements, *output* is empty. TVF code is processed before the run is started.

- ***rule_file_name***

  A required argument that specifies the path to and name of the SVRF rule file.

Examples

Example 1

The following statement instructs the Calibre xL tool to perform incremental self impedance extraction using the SVRF rule file named *my_rules*.

```
calibre -xrc -pdb -l my_rules
```

Example 2

The following statement instructs the Calibre xL tool to perform self and mutual impedance extraction using the xcell named *hcell_list3* and the SVRF rule file named *my_rules*.

```
calibre -xrc -pdb -lm -xcell hcell_list3 my_rules
```

calibre -xrc -fmt

Produces netlists and reports from the contents of the PDB.

Usage

calibre -xrc -fmt {**-l** | **-m** | **-lm** | **-rl** | **-rcl** | **-rccl** |**-rlm** | **-rclm** | **-rcclm** | **-all**}
[-cb] [-incontext |-full] [-corner {*corner*[,*corner*]… | all}] [-E *output*] ***rule_file_name***

Description

Produces netlists and reports from the contents of the PDB. Specifies the output formats and filename locations using the PEX Netlist statement in your SVRF rule file.

Arguments

- **-xrc**

  A required argument that performs parasitic extraction using the Calibre xRC tool.

- **-fmt**

  A required argument that produces netlists and reports from parasitic data stored in PDB. The format of the output netlist is HSPICE, DSPF, Eldo, Spectre or CalibreView, depending on the setting specified in the PEX Netlist statement.

- **-l** | **-m** | **-lm** | **-rl** | **-rcl** | **-rccl** | **-rlm** | **-rclm** | **-rcclm** | **-all**

  A required argument that specifies the output mode. Choose one of the following:

  -l — Distributed netlist; suppresses writing of any parasitic capacitors, resistors, or mutual inductance; exits if the PDB does not contain self inductance data.

  -m — Distributed netlist; suppresses writing of any parasitic capacitors, resistors, or self inductance; exits if the PDB does not contain mutual inductance data.

  -lm — Distributed netlist; suppresses writing of any parasitic capacitors or resistors; exits if the PDB does not contain inductance data.

  -rl — Distributed netlist; suppresses writing of any parasitic capacitors; exits if the PDB does not contain inductance and resistance.

  -rcl — Distributed netlist; grounds coupled capacitances; exits if the PDB does not contain inductance, capacitance, and resistance.

  -rccl — Distributed netlist; exits if the PDB does not contain inductance, coupled capacitance, and resistance data.

  -rlm — Distributed netlist; suppresses any parasitic capacitors; exits if the PDB does not contain self and mutual inductance and resistance.

  -rclm — Distributed netlist; grounds coupled capacitance; exits if the PDB does not contain inductance, capacitance, and resistance.

  -rcclm — Distributed netlist; exits if the PDB does not contain inductance, coupled capacitance, and resistance.

-all Distributed netlist; writes the contents of the PDB into the netlist. Exits if the PDB contains lumped capacitance only. This parameter is the default.

- -cb

  See *Calibre xRC User's Manual* for information.

- -incontext

  An optional argument that causes the formatter to netlist all in-context cells in the PDB when extraction was run with gate-level in-context rather than full (hybrid) extraction.

- -full

  An optional argument used for hierarchical netlisting. For more information, see the *Calibre xRC User's Manual*.

- -corner {*corner*[,*corner*]… | all}

  An optional argument set that selects the process corners to write out. If you specify two or more corner names, do not place a space between names. If the rules define multiple corners and you do not use this option, only the typical corner is netlisted.

- -E *output*

  An optional argument set that specifies an output file name for SVRF code generated by the TVF processor. If ***rule_file_name*** contains no TVF statements, *output* is empty. TVF code is processed before the run is started.

- ***rule_file_name***

  A required argument that specifies the path to and name of the SVRF rule file.

Note

For more information on the Calibre xRC formatter options, see the calibre -xrc -fmt section of the *Calibre xRC User's Manual*.

Examples

The following statement instructs the Calibre xRC tool to write the contents of the PDB into the netlist using the rule file named *my_rules*.

```
calibre -xrc -fmt -all my_rules
```

Appendix A
Advanced Features

Advanced features in Calibre xL are controlled with SVRF statements.

This appendix includes the following sections that provide information on features you can use to control self and mutual impedance extraction:

Extracting Partial RLK Parasitics

Use the Calibre xL incremental extraction flow to extract the partial RLK parasitics for nets “S1”, “S2”, and “GND”.

To perform partial RLK inductance extraction you must:

- Specify PEX Inductance Mode PEEC statement in your rule file. This statement controls the inductance extraction mode used by the Calibre xL tool during select net extraction.
- Specify particular nets using the PEX Extract Include statement in your rule file. PWR and GND nets may be part of the selected net set.
- Specify the -select command line option in the PDB generation step.

Prerequisites

You must have the following:

- Calibre software is installed.
- Calibre xRC and Calibre xL licenses are available.
- Either the $MGC_HOME or $CALIBRE_HOME environment variables are defined.
- A top-level control file (*pex.rules*) that includes all necessary foundry rule decks used to extract parasitics.

Procedure

1. Include the following statements in your top-level control file (*pex.rules*):

```
PEX INDUCTANCE MODE PEEC
PEX EXTRACT INCLUDE LAYOUTNAMES "S1" "S2" "GND"
```

2. Perform Calibre xL extraction with the following set of commands:

```
calibre -lvs -hier -spice svdb/ADC_5bit_sc_5.sp pex.rules
```

   Extract resistance and capacitance for all nets with Calibre xRC:

```
calibre -xrc -pdb -rcc -turbo pex.rules
```

   Perform a select net run with Calibre xL:

```
calibre -xrc -pdb -rl -turbo -select pex.rules
```

   Generate the netlist:

```
calibre -xrc -fmt -all pex.rules
```

Results

Check the transcripts for any errors. The run creates a netlist containing RCC information for all nets and RCCLK information for the selected nets S1, S2, and GND.

Driver and Receiver File Generation

The driver and receiver file (*driver.xl*) is an optional file that identifies the paths to evaluate for self and mutual impedance extraction.

You can generate the driver and receiver file using either of these statements in the SVRF rule file:

- PEX Generate Driver File Tag
- PEX Inductance Filter with the FILE TAG *tags* option

You can edit the driver and receiver file. Additionally, you can specify to use a driver and receiver file using either of the following:

- The PEX Inductance Filter statement with the FILE TAG *tags* option
- The "Use Driver/Receiver File" option on the **Inductance** tab in Calibre Interactive

Figure A-1 shows a sample driver and receiver file.

Figure A-1. Sample Driver and Receiver File

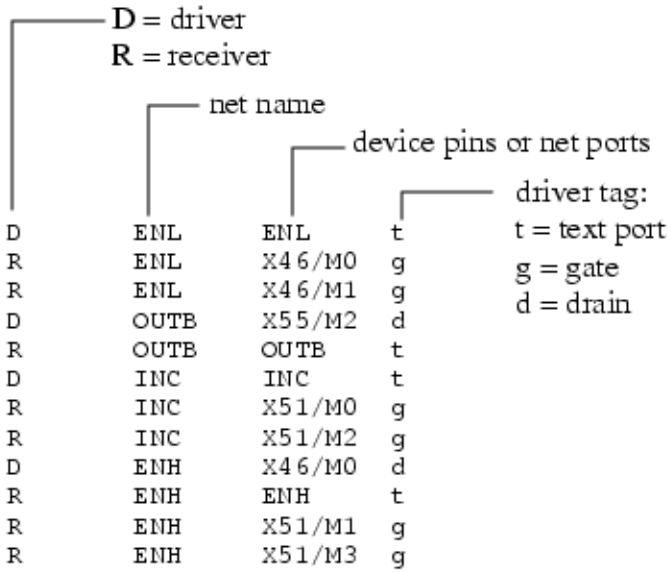
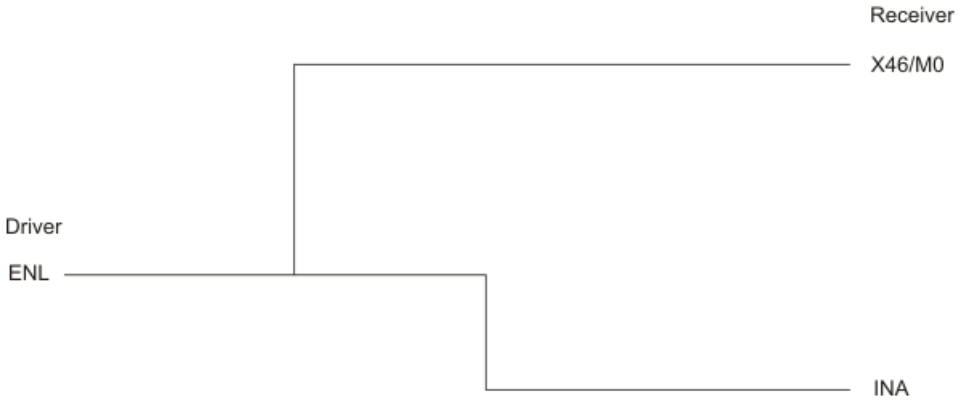


Figure A-2 shows an example of a path (ENL-X46/M0) that will be considered for mutual impedance extraction based on the driver and receiver file shown in Figure A-1.

Figure A-2. Path Identified by the Driver and Receiver File



Controlling How Calibre xL Selects Aggressor Nets

For the selected victims, the Calibre xL tool automatically identifies the aggressors based on an imaginary tube placed around the victim paths.

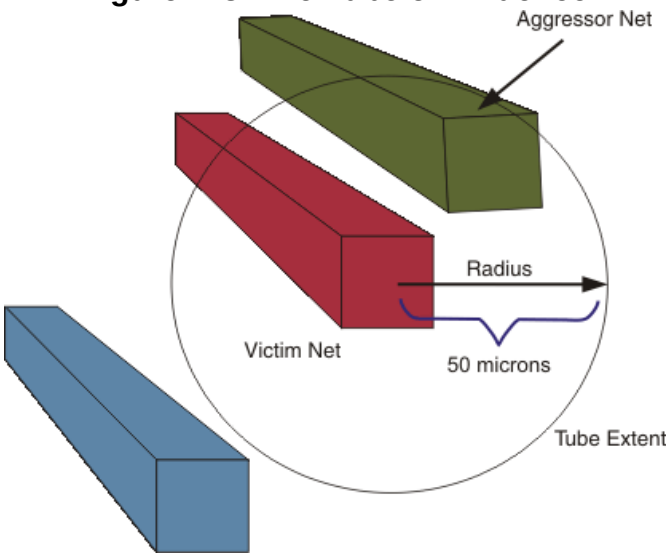
You can control the radius of the tube using any of the following:

- The PEX Inductance Victim statement with the tube radius=*value* option.

- The “Tube Radius” field on the **Select Nets for Mutual Inductance** dialog in the Calibre RVE viewer.

Figure A-3 shows a cross-sectional representation of the tube.

Figure A-3. The Tube of Influence

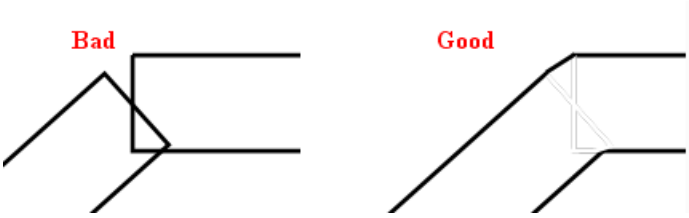


Handling Corners

Spirals drawn with non-flush corners produce extra couplings and incorrect results.

To avoid this, ensure that corners do not have notches as shown in Figure A-4.

Figure A-4. Corner Handling



Appendix B
Layer-Specific SVRF Statements

There are specialized SVRF statements that you can use to define your layout layer information.

This chapter includes the following sections that provide information on these layer-specific statements:

About Calibre xL Layer Information

For each conductor layer in your layout, you need to identify the height above the substrate.

You obtain this information using the xCalibrate™ tool; refer to the *xCalibrate Batch User's Manual* for details.

Note that when process information is created using the xCalibrate tool, the conductor layer names used in the layer profile may differ from the conductor layer names you use in your layout. In this case, you need to specify layer name equivalence using the PEX Map or PEX Elayer statement in your SVRF rule file.

Layer-Specific Statements

This section describes the SVRF statements used to define your layout layer information.

Table B-1. Layer-Specific SVRF Inductance Statements

Rule	Description
PEX Elayer	Specifies conductor layer equivalency and maps layer names in the layout to layer names you use (if different) when defining layer height information in the xCalibrate tool.
PEX Inductance Extract Layers	Declares the layers to process during inductance extraction.

Sample Calibre xL SVRF Rule File

Here is an example of a Calibre xL rule file.

Example B-1 shows the rule file containing Calibre xRC and Calibre xL tool statements. For details on how to construct an SVRF rule file for the Calibre xL tool, see “Calibre xL SVRF Rule File Reference” on page 39.

Example B-1. Sample Calibre xL SVRF Rule File

```
LAYOUT PATH    "./simple.hp3.gds"
LAYOUT PRIMARY "simple"
LAYOUT SYSTEM   GDSII

LAYOUT CASE     no

SOURCE PATH    "simple_source.sp"
SOURCE PRIMARY "simple"
SOURCE SYSTEM   HSPICE

MASK SVDB DIRECTORY "svdb" XRC by gate

//Inductance (xL) statements
PEX INDUCTANCE SELF 9.0e-4
PEX INDUCTANCE FREQUENCY 10.0e9
PEX INDUCTANCE RETURNPATH ground
PEX INDUCTANCE FILTER OFF
PEX INDUCTANCE EXTRACT LAYERS M1 M2
PEX GENERATE DRIVER_FILE TAG s c d t
PEX INDUCTANCE DRIVER FILE "./pix_rules.xl"

//Layer definitions
LAYER   NWELL      1
LAYER   rawPOLY    6
LAYER   PDIF       2
LAYER   NDIF       8
LAYER   PIMP       7
LAYER   CONT      13
LAYER   VIA       15
LAYER    M1       14
LAYER    M2       12

  bulk = extent
  psub = bulk not NWELL
  diff =  PDIF or NDIF
  gate =  rawPOLY and  diff
  POLY = rawPOLY not gate
  pgate = gate and PIMP
  ngate = gate not pgate
  alldiff = diff not gate
  pdiff = alldiff and PIMP
  ndiff = alldiff not pdiff
  ncont = ndiff and NWELL
  pcont = pdiff and psub
CONNECT M1 M2 BY 15
CONNECT M1 POLY by CONT  mask
CONNECT M1 pdiff by CONT mask
CONNECT M1 ndiff by CONT mask
CONNECT ndiff NWELL by ncont   mask
CONNECT pdiff psub  by pcont   mask
CONNECT POLY gate

LAYOUT TEXT INA 232.5  0     20 "simple"
LAYOUT TEXT INB 218.5  0     20 "simple"
LAYOUT TEXT INC 19     0     20 "simple"
```

```
LAYOUT TEXT IND 218.5  248   20 "simple"
LAYOUT TEXT ENL 0      230   20 "simple"
LAYOUT TEXT VCC 0      0     20 "simple"
LAYOUT TEXT VSS 0      114.5 20 "simple"
LAYOUT TEXT OUTA 232.5 230.5 20 "simple"
LAYOUT TEXT OUTB 0     248   20 "simple"
LAYOUT TEXT ENH 55     230   20 "simple"
ATTACH 20 M1

PORT LAYER TEXT 20
PORT LAYER TEXT M1
PORT LAYER TEXT M2
TEXT LAYER 20
TEXT LAYER M1
TEXT LAYER M2
TEXT DEPTH PRIMARY

//Standard PEX statements
CAPACITANCE ORDER pdiff ndiff POLY M1 M2
INCLUDE "rules.C" //capacitance calculations
INCLUDE "rules.R" //resistance statements

PEX MAP P0 rawPOLY poly
PEX MAP metal1 m1
PEX MAP metal2 m2

PEX NETLIST SIMPLE "z_netlist.simple" LAYOUTNAMES LOCATION
PEX REPORT "z_report.lumped" LAYOUTNAMES

PEX EXTRACT INCLUDE "ENH" "VSS"
PEX REPORT "z_report.dist" LAYOUT
PEX NETLIST "z_netlist.dist"  HSPICE 1e-6 LAYOUTNAMES GROUND VSS LOCATION
RLOCATION RWIDTH RLAYER

//nmLVS Options
LVS  ABORT ON SUPPLY ERROR yes
LVS  POWER NAME VCC
LVS  GROUND NAME VSS
LVS ALL CAPACITOR PINS SWAPPABLE no
LVS REDUCE PARALLEL MOS yes
LVS REDUCE PARALLEL BIPOLAR yes
LVS FILTER UNUSED   MOS no
LVS FILTER UNUSED   BIPOLAR no
LVS REDUCE SERIES   CAPACITORS yes
LVS REDUCE PARALLEL CAPACITORS yes
LVS REDUCE SERIES   RESISTORS yes
LVS REDUCE PARALLEL RESISTORS yes
LVS RECOGNIZE GATES all
LVS REDUCE SPLIT GATES yes
LVS COMPONENT TYPE PROPERTY element
LVS COMPONENT SUBTYPE PROPERTY model
LVS PIN NAME  PROPERTY phy_pin
LVS IGNORE PORTS yes
LVS REPORT "z_lvs.rep"
LVS REPORT MAXIMUM 50

//DRC RuleChecks
MIN_SPACING_M2_M2 {
```

```
   EXTERNAL M2 <   2.500  NOT CONNECTED
   @ Minimum spacing between M2 and M2.
}
MIN_SPACING_M1_M1 {
   EXTERNAL M1 <   3.00  NOT CONNECTED
   @ Minimum spacing between M1 and M1.
}
GROUP CONTINUOUS_DRC
        MIN_SPACING_M2_M2
        MIN_SPACING_M1_M1

INCLUDE "device_definitions.svrf"
```

Glossary

aggressor nets
The switching nets that induce noise on victim nets.

broadband model
A circuit composed of one resistor in parallel with one inductor used for modeling frequency dependent behavior of RL interconnects.

compound run
A run in which inductance is extracted in conjunction with resistance and capacitance; for example, when you specify the -rcl switch.

differential pairs
One or more complementary pair of nets that provide noise immunity used for isolating paths without return paths.

dynamic resistance
The ratio of the change in current.

forward coupling
In mutual impedance, a magnetic interaction between two different wire segments belonging to the same wire path.

high frequencies
Frequency beyond which inductance becomes important.

inductance
The measure of the magnetic flux generated by a time-varying current (source) that traverses an area enclosed by the loop formed by the circuit (victim) for a unit source current. When the source and victim are the same, this is referred to as self impedance. When the source and victim are different, this is referred to as mutual impedance.

intentional inductors
Design inductors created by IC designers as part of the design intent to produce a certain electrical effect based on the IC's specification. Intentional inductors are also referred to as "spiral inductors" or "spirals."

loop impedance
The joint impedance of the signal line and all its return wires.

loop self impedance
Inductance associated with a signal and its current return path.

model order reduction
A way to reduce the number of elements in your parasitic netlist.

mutual impedance
Magnitude that measures the full electromagnetic effect of one current loop over another.

mutual resistance
Any nonzero real parts of the off-diagonal elements in the loop impedance matrix.

parasitic inductance
Unintentional inductance generated as a result of interconnect wiring in high frequency ICs.

path
A unique two-point terminal connection (belonging to a wire net) between two devices.

self impedance
A property of a circuit whereby a change in current causes a change in voltage.

skin depth
Length scale that represents the typical penetration of currents inside a conductor from its surface.

skin effect
A phenomenon occurring at high frequencies in which the current in a conductor’s cross section tends to crowd near its surface.

victim nets
Nets on which noise is generated.

Index

— L —

— M —

— N —

— O —

— P —

— Q —

— R —

— S —

— U —

— V —

Third-Party Information

Details on open source and third-party software that may be included with this product are available in the *<your_software_installation_location>/legal* directory.