

SIEMENS Calibre® 3DSTACK Quick Reference

Software Version 2021.2

Command Line Invocation

calibre -3dstack [-help] [-turbo [number_of_processors]] {[-create assembly assembly name [-system {OASIS | GDS}]] [-use assembly assembly_path] [-assembly assembly_name] } [-run_dir directory] [-compile_only] rule_file_name

Calibre Interactive 3DSTACK

Launch Calibre Interactive 3DSTACK, use this command:

calibre -gui -3dstack [-runset runset file]

Launch Calibre Interactive 3DSTACK from Calibre DESIGNrev: **Verification > Run 3DSTACK**

Calibre 3DSTACK Output Files

The following output files are created in your working directory: 3dstack assembly.oas — assembled view of the chip stack. 3dstack assembly.oas.layerprops — layer properties file. 3dstack assembly.oas.layermap — SVRF layer definitions generated from the assembly process.

3dstack_cross_section.oas — x, y, and z view of your stack. 3dstack cross section.oas.layerprops— layer properties file 3dstack overlay generator.tcl — a Tcl script used to generate the chip stack layout view from the individual layouts.

3dstack.rdb — RDB file containing analysis results. RDB files are also created for each layout file in the chip stack.

3dstack.dfmdb (directory) — DFMDB analysis results.

<3dstack+ rules>.3dstack — compiled 3DSTACK+ rule file.

3dstack.log — transcript of the complete run.

3dstack.warnings — collection of all warnings issued by the run. readerprefs — saved exception settings.

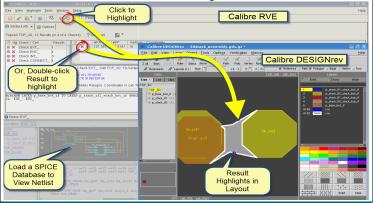
Browse 3DSTACK Results in Calibre RVE

Calibre RVE highlights Calibre 3DSTACK results to the associated geometry in the layout viewer.

Enter the following command to open the results in Calibre RVE:

calibre -rve 3dstack.rdb

Database Results Browsing with Calibre RVE



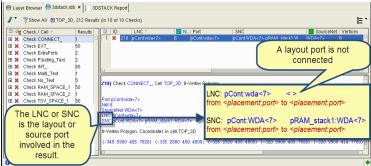
Opening a 3DSTACK DFMDB in Calibre RVE

Cross-referencing between source and layout is supported in Calibre RVE if a source netlist is specified at runtime.

- 1. Open 3dstack_assembly.oas in a supported layout editor.
- 2. Start Calibre RVE from the layout editor's interface:
 - o Calibre DESIGNrev Verification > Start RVE.
 - Other supported layout viewers Calibre > Start RVE.
- 3. In the Calibre RVE dialog box, select **DFM** database and enter the path to your 3dstack.dfmdb database.

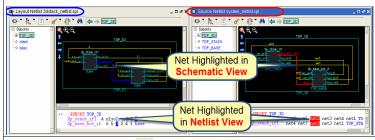
- 4. Set up the Internal Schematic Viewer to display source and layout netlists as follows:
 - Choose Setup > Options and click Schematic Viewer.
 - Enable Show netlist schematics when highlighting connectivity objects.
 - o Enable Schematic, Hierarchy and Text and click Apply.
- 5. Choose View > Schematics > All.

Cross-Reference Database Results in Calibre RVE



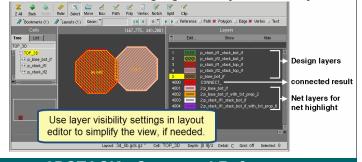
Click on the layout net and source net icons to highlight them in the Internal Schematic Viewer. The layout net is also highlighted in the lavout viewer.





The highlight button (🔆) in the highlight toolbar browses directly to the result in the layout viewer.

Click Schematic Nets to Highlight the Layout Geometry



3DSTACK+ Command Reference

The 3DSTACK+ command file defines the physical assembly of a 3D or 2.5D IC. It follows these formatting and syntax rules:

- The file must consist only of Calibre 3DSTACK commands and standard Tcl constructs.
- The file must begin with the following two statements:

#!3dstack+ set_version -version 1.0

- The assembly commands are die, config, and stack.
- All distances are specified in microns.

config and process Commands

```
Specifies system configuration and control options for the run.

config [-layout_primary name] [-layer_props_file props_file]
[-netlist '{'-file file_name -format {SPICE | VERILOG version | CSV | MGC} [-case {YES | NO}] [-hier] [-wrap name] '}'] [-order {list}]
[-subckt_pins {type}] [-apply_bboxing cell_list]
[-report '{'-file report_path [-max_results value]
        [-child_rdbs {NO | YES }] -report_ignored_pins {NO | YES} '}']
[-ignore_trailing_chars char_list] [-layout_case {no | yes}]
```

| MGC | SPICE | XSI }] ...
[-pin_map -pins pins -to name] [-import_pin_map -file file]
[-net_map -nets nets -to name] [-import_net_map -file file]
[-svrf_specs svrf_file] [-set_rve_cto_file cto_file]
[-set_auto_rve_show_layers {NO | YES}] [-units [-distance {um | mm | nm}] [-power {W | mW | uW}] [-time {s | hr | min | ms | us}]]

[-export_connectivity '{'-file output_file [-format {VERILOG | AIF

process process_layer_information

die Command

```
Specifies information about a single die in the assembly.
```

```
die -die_name die_name
{-layout '{' -path layout_path [-type {gdsii | oasis}]
    [-primary name] [-depth {all | top-only}] [-precision value]'}'
    | {-lefdef '{' -lef tech_lef [lef_file ...] -def def_file '}' }
[-thickness die_thickness]
```

[-text '{' layer_numbers [-depth {number ...}] [-no_update] | [-net_text layers] '}' [-pex_map layer_name] [-rc_model] [-ext_connect die_name ...] [-icrx -file file | -mipt -file file] [-texted] [-texttype] [-top | -bottom] [-virtual] [-via] } ...
'}' } ...

[-anchor '{'-name anchor_name {-placement x_offset y_offset | -layer number -text label}'}'] ...

[-interposer | -package | -laminate | -substrate]

[-import_text_labels file {xsi_args}] [-rename_text "expression ..."] [-wb_connect layer1 layer2 [BY layer3] [-use_in_svrf]]

component Command

Allows you to define objects in your assembly that are not dies. The syntax is the same as die with one additional option (-swappable).

component -component_name name

{ die_command_options ... [-swappable pin_list] }

stack Command

Defines the locations of dies and stacks of dies in an assembly.

stack -stack_name name {die_stack | tier_spec | stack_ref }...

die_stack Usage

tier_spec Usage

stack -tier '{' {die_stack | stack_ref }...'}'

stack_ref Usage

stack -stack stack_name

'}' [-z_origin vertical_height]

Rule Check Commands

The following options apply to geometrical rule check commands: [-comment "comment"] [rve_option ...]

centers -check_name check_name

-layer_type1 type1 [-same_die] [-layer_type2 type2]
-constraint "constraint_value" [-overlapping]
[-alignment {octagonal_only | orthogonal_only }] [-square]

[-black_box | -white_box] [-net_mismatch {ALL | MULTI_NAME | MISMATCH | MISSING_NAME}] [-no_dangling_ports] [-no_extra_ports] [-no_missing_ports] [-isolate_path] [-pin_list pins_to_report]

copy -check_name check_name -layer_type placed_layertype

custom_check -check_name check_name

[-stack stack_list] [-direction {up | down | both}]

-layer_type1 '{' placed_layer_type1... [-merge] '}'

[-layer_type2 '{' placed_layer_type2 ... [-merge] '}']

-tvf '{' tvf_body '}'

{ dangling_ports | dangling_no_text | extra_ports | missing_ports } -check_name name -layer_types types_list

unconnected_ports-check_name name
{-layer_types types_list} | {-dies die_list}

density -check_name check_name

-layer_types {placed_layertype ...}
[-expression "density_expression"] -constraint "expression"

[-window {wxy | wx wy} [-step {sxy | sx sy}]]

[-window_type {truncate | backup | ignore | wrap}] [-inside { extent | placed_layer }] [-centers value]

{enclosure | external | internal } -check_name check_name -layer_type1 type1 [-layer_type2 type2] -constraint "value"

floating_pads -check_name name -layer_type layer_type

{ floating_texts | multi_texts | no_texts }

-check_name check_name -layer_types layer_types_list

locations -check_name check_name

{-layer_type1 placed_layertype [-layer_type2 placed_layertype]} [-constraint "constraint_value"] [-text_only | -overlap_only] [-direction {both | up | down} | {both | direct | reverse}]]

offgrid_centers -check_name check_name

-layer_type placed_layertype -resolution {resolution_value |
x_resolution_value y_resolution_value } [-hint]

overlap -check_name check_name -placement1 placed_layer1 { -layer_type placed_layertype [placed_layertype] } -constraint "constraint_expression" [by_area] [-intersection] [-merge]

same_size -check_name check_name
-layer_type1 placed_layertype -layer_type2 placed_layertype

{select_checks | unselect_checks}
{ -check_names '{'chk_pattern [chk_pattern...]'}'
| -layer_types '{'type_pattern [type_pattern ...] '}' }

3dstack_block '{' body '}'

'{' 3dstack_cmds '}'— Block of standard syntax commands

