# SIEMENS Calibre® xACT™ Quick Reference

Software Version 2021.2

## Overview

Calibre xACT is a high-performance, high-accuracy parasitic extraction tool for leading-edge transistor-level and digital design. Calibre® xACT 3D is a high-accuracy parasitic extraction tool that uses fast field solver technology for capacitance extraction.

Use Calibre xACT or Calibre xACT 3D to generate simulatable parasitic netlists.

## Documentation

Refer to the *Calibre xACT User's Manual* for details on how to set up and run Calibre xACT and the *Standard Verfication Rule Format (SVRF) Manual* for details on SVRF statements.

## PEX Rule File

The top-level rule file (*pex.rules*) contains the SVRF statements necessary to run Calibre xACT and Calibre xACT 3D.

Use PEX statements described in the *Standard Verification Rule Format (SVRF) Manual* to customize and tune parasitic and netlist output. The following is a GDS flow example using source names:

```
// design layout information
LAYOUT PRIMARY "topcell"
LAYOUT PATH "design/topcell.gds"
LAYOUT SYSTEM GDSII

// design netlist information
SOURCE PRIMARY "topcell"
SOURCE PATH "design/topcell.src.net"
SOURCE SYSTEM SPICE

// extracted netlist output specification
PEX NETLIST "netlist.fmt" format SOURCENAMES
//PEX NETLIST "netlist.fmt" format LAYOUTNAMES
PEX EXTRACT EXCLUDE SOURCENAMES VDD VSS
PEX EXTRACT TEMPERATURE 27
PEX REDUCE ANALOG YES
UNIT CAPACITANCE fF

// LVS and calibrated rule files
INCLUDE rules/layers.svrf
INCLUDE rules/lvs_rules.svrf
INCLUDE rules/rules.C
INCLUDE rules/rules.R
INCLUDE rules/rules.xact
```

where ***format*** is one of the following keywords: DSPF, HSPICE, SPEF, SPECTRE, ELDO, or CALIBREVIEW.

## Command Line

The Calibre xACT command line invocation is:

```
calibre -xact -model pex.rules
```

The Calibre xACT 3D command line invocation is:

```
calibre -xact -3d -model pex.rules
```

where *model* is one of the following:

```
[ -c | -r | -rc | -rcc | -rl | -rlm | -rcl
     | -rclm | -rccl | -rcclm | -simple]
```

| | |
|---|---|
| -c | Lumped capacitance |
| -r | Resistance only |
| -rc | Resistance and distributed capacitance |
| -rcc | Resistance with distributed capacitance and coupled capacitance between nets (default) |
| -rl | Resistance and inductance |
| -rlm | Resistance, inductance and mutual inductance |
| -rcl | Resistance, capacitance, inductance |
| -rclm | Resistance, capacitance, inductance, and mutual inductance |
| -rccl | Resistance with distributed capacitance and coupled capacitance between nets and inductance |
| -rcclm | Resistance with distributed capacitance and coupled capacitance between nets, inductance, and mutual inductance |
| -simple | No parasitics |

## Calibre Interactive - xACT

From a layout or schematic editor choose:

**Run xACT** from **Calibre** menu.

From the command line:

```
calibre -gui -xact
```

## Calibre xACT Output

A Calibre xACT run ends with a summary of errors and warnings. The current working directory will contain the requested netlist and reports.

If you are running from the GUI, you can use Calibre® RVE™ to highlight parasitic elements in the layout viewer. To run Calibre RVE, the SVDB must have RVE cross-references. For detailed information on how to use the Calibre Results Viewing environment for PEX, see "Using Calibre RVE for PEX" in the *Calibre RVE User's Manual*.

## Transistor-Level Extraction

**Using Layout Names:**

1. In your PEX rule file, specify your design layout database using statements:
   - Layout Primary
   - Layout Path
   - Layout System
2. Determine the netlist output you need. Specify the LAYOUTNAMES keyword in the PEX Netlist statement.
3. Optionally specify any reduction or ignore statements in your PEX rule file.
4. Decide which parasitic *model* you need.
5. Run Calibre xACT from the command line:

```
calibre -xact -model pex.rules
```

**Using Source Names:**

Use sourcenames when you want your output netlist to have source names.

1. In your PEX rule file, specify your design layout database and source input statements:
   - Layout Primary
   - Layout Path
   - System Path
   - Source Primary
   - Source Path
   - Source System
2. Determine the netlist output you need. Specify the SOURCENAMES keyword in the PEX Netlist statement.
3. Optionally specify any reduction or ignore statements in your PEX rule file.
4. Decide which parasitic *model* you need.
5. Run LVS to perform device recognition:

```
calibre -lvs -hier pex.rules
```

6. Run Calibre xACT from the command line:

```
calibre -xact -model pex.rules
```

## Calibre xACT 3D

Use Calibre xACT 3D to run field solver extraction on a small to medium sized design block. The PEX Fieldsolver Mode statement specifies the capacitance extraction accuracy mode used.

200 — faster, coarser grid. This is the default.

600 — slower, finer grid, used as reference-level solver.

The -3d command line option activates the field solver. For example:

```
calibre -xact -3d -model pex.rules
```

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## Digital Extraction

Calibre xACT can generate a full-chip digital design netlist from a LEF/DEF design. Power and ground nets are automatically excluded when using LEF and DEF as input.

In the *layers.svrf* file, use PEX Map statements to map the calibrated rule file layer names to the LVS layer names so that the layers can inherit the parasitic properties. Use PEX DEF Map statements to map the layer names in the LEF/DEF database to the LVS layer names in order to establish connectivity; use the metal layer names found in the LEF technology file.

In the PEX rule file, the following statements are needed to run the Calibre xACT digital flow:

- Layout Path — Specifies the LEF and DEF files.
- Layout System LEFDEF — Specifies the layout is a set of LEF and DEF files.
- DFM Database — Specifies the path to the DFM database.
- PEX DEF Extract Blockages NO — Specifies to exclude DEF placement and routing blockage areas from parasitic extraction.
- PEX XACT Fill FLOATING — Specifies to model metal fill as floating.
- PEX Extract Temperature — Controls the temperature dependence which can affect resistance.
- PEX Netlist — Specifies the parasitic netlist output format.

The following is a digital PEX rule file example:

```
// design layout information
LAYOUT PRIMARY "top"
LAYOUT PATH "design/LEF/tech.lef"
            "design/LEF/pads.lef"
            . . .
            "design/DEF/top.def"
LAYOUT SYSTEM LEFDEF
MASK SVDB DIRECTORY "svdb" XACT
DFM DATABASE "dfmdb" OVERWRITE
PEX NETLIST "netlist.fmt.gz" SPEF LAYOUTNAMES
              MAPNAMES NOINSTANCEX
PEX LEF EXTRACT CELL OBSTRUCTIONS YES
PEX DEF EXTRACT BLOCKAGES NO
PEX XACT FILL FLOATING
PEX REDUCE DIGITAL YES
PEX EXTRACT TEMPERATURE 27
// LVS and calibrated rule files
INCLUDE rules/layers.svrf
INCLUDE rules/lvs_rules.svrf
INCLUDE rules/rules.C
INCLUDE rules/rules.R
INCLUDE rules/rules.xact
```

## Inductance Extraction

Inductance can be extracted for transistor-level, analog, and digital designs as a part of any Calibre xACT direct netlisting flow when a Calibre® xL license is available and the specified model includes inductance(l) and/or mutual inductance(m). See "Getting Started: Calibre xACT Inductance Extraction Using Batch Mode" in the *Calibre xACT User's Manual* for detailed information on performing inductance extraction.

## Netlist Generation

Use either of the following SVRF statements for parasitic netlist generation:

- Use PEX Netlist to generate a netlist with parasitic elements in one of the following *formats*: HSPICE, DSPF, SPEF, SPECTRE, ELDO, or CALIBREVIEW. Several keywords are available to tailor the netlist to your specific needs. The minimum syntax is:

```
PEX NETLIST netlist_name format
  { LAYOUTNAMES | SOURCENAMES [filename]
    | SOURCEBASED | SCHEMATICONLY [filename]}
```

- Use PEX XACT Control when you want to control how certain nets are handled during netlist generation. The syntax is:

```
PEX XACT CONTROL [
 EXTRACT_CONTROL {
   NET: netname
   MODEL: [rcclk | rccl | rcc | rclk | rcl | rc
          | rlk | rl | r | c | cg }
    [{ R_LAYERS_SELECT: | R_LAYERS_EXCLUDE: }
       [layer ...] [VIA layer1 layer2
         [VIANAME vlayer [vlayer...]]...]
    [{L_LAYERS: | L_LAYERS_EXCLUDE: }
       [layer...]]
 }
 NETLIST_CONTROL {
   MODEL: {rcclk | rccl | rcc | rclk | rcl | rc
          | rlk | rl | r | c | cg | none }
   {NETLIST: netlist_name
    NETLIST_FORMAT: {DSPF | HSPICE | SPEF
                | SPECTRE | ELDO | CALIBREVIEW}
      [LAYOUTNAMES | SOURCENAMES | SOURCEBASED]
      [TOPLEVEL | RECURSIVE]
     [NET: netname [netname...]
      [LAYOUTNAMES | SOURCENAMES]
      [TOPLEVEL | RECURSIVE]
        [MODEL: {rcclk | rccl | rcc | rclk
                | rcl | rc | rlk | rl | r | c
                | cg | none } ]
    ]
   }
 }
]
```

See the *SVRF* manual for more PEX Netlist statements with syntax descriptions and examples.

## Reduction Statements

Use reduction statements to control netlist size and simulation performance. If no reduction statements are specified, then Calibre uses optimized settings based on the layout design type (GDS, LEF/DEF, or OASIS). The reduction statements supported by Calibre xACT and Calibre xACT 3D are:

- PEX Extract Floating Nets — Controls how floating nets are handled during extraction.
- PEX Reduce Analog — Performs reduction of extracted data optimized for analog designs.
- PEX Reduce CC — Performs reduction of coupled capacitance on a net basis.
- PEX Reduce Digital — Performs reduction of extracted data optimized for digital designs.
- PEX Reduce Mincap — Combines or removes capacitors below a threshold value.
- PEX Reduce Minmutual — Removes parasitic mutual inductance below a threshold value.
- PEX Reduce Minres — Combines or shorts parasitic resistors below a threshold value.
- PEX Reduce ROnly — Performs reduction of resistance-only extracted data.
- PEX Reduce Stub — Controls whether or not to remove dangling nets.
- PEX Reduce TICER — Performs TICER reduction of distributed RC extraction data using a specified frequency value.

## Ignore Statements

Use ignore statements to ignore parasitics on certain layers or for certain connections. The ignore statements supported by Calibre xACT and Calibre xACT 3D are:

- PEX Ignore Capacitance — Ignores certain types of capacitance models and capacitance types between specific layers. Calibre xACT 3D supports ALL, ALL SUBSTRATE (single and multi layer), INTRINSIC ALL, DEVICE, and ALL VIA.
- PEX Ignore Capacitance Vianame— Ignores capacitance for specified LVS layers. Do not use in the Calibre xACT digital flow.
- PEX Ignore Inductance — Ignores inductance for the specified layer or connections.
- PEX Ignore Resistance — Ignores parasitic resistance for the specified layer or via connections.
- PEX Ignore Resistance Marker— Ignores parasitic resistance within a marker region.

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