SIEMENS EDA

Calibre® Job Deck Editor User's Manual

Software Version 2021.2

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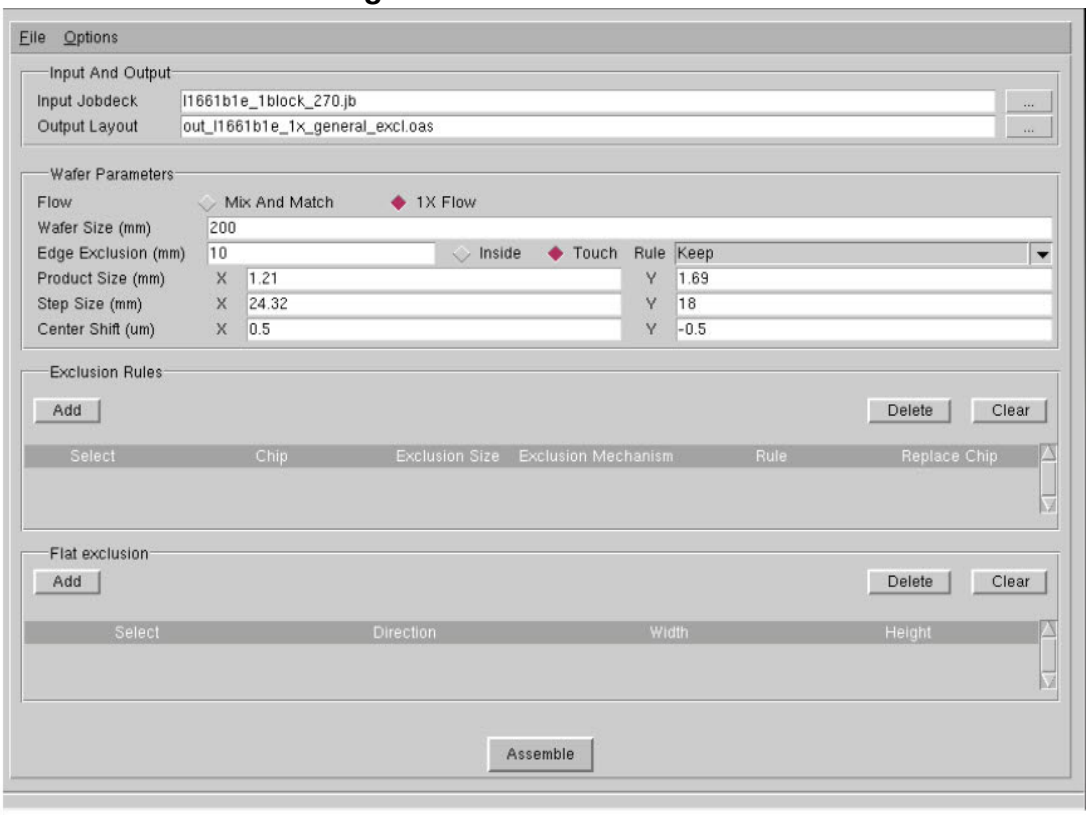
Chapter 1
Introduction to the Calibre Job Deck Editor

The Calibre® Job Deck Editor is a feature of Calibre® WORKbench™ and Calibre® MDPview™ used to generate an optimized chip placement on the wafer, with the ability to manually edit chips in the job deck, following one of the two mask flows.

- **1x Mask** — All layers for a product are exposed on 1x mask.
- **Mix and Match** — Only the non-critical backend layers are exposed with 1x masks (full wafer exposure), while the front end layers are exposed using reduction reticles.

You can use the Calibre Job Deck Editor to perform job deck assembly, enabling you to automatically exclude chips according to an exclusion mechanism, through a single interface. You can also use the editing capabilities of Calibre WORKbench and Calibre MDPview to manually correct any errors in the job deck itself.

Figure 1-1. Job Deck Editor



Calibre Job Deck Editor Input and Output

This section describes the input and output options for the Calibre Job Deck Editor.

The input of the Job Deck Editor is:

- 1x MEBES job deck that contains the product chip layout with KERF structures or an OASIS®[1] file using the following hierarchy:
  - Top Cell > Full Product chip > Chips to be assembled
- Parameters for wafer map optimization:
  - Wafer size
  - Edge exclusion size
  - Main Product size
  - Step size in x and y directions

The output of the Job Deck Editor is:

- OASIS layout
- MEBES job deck fractured from OASIS layout

Calibre Job Deck Editor Prerequisites

There are several prerequisites prior to invoking the Calibre Job Deck Editor.

- **Platform support** — Calibre MDPview is available on all supported platforms found in the *Calibre Administrator's Guide*. Refer to that document for instructions on how to install Calibre software.
- **Licensing** — To run the Job Deck Editor, you must have a license for either Calibre® WORKbench™ or Calibre® MDPview™ and the Calibre Job Deck Editor. For more information on licensing, refer to the *Calibre Administrator's Guide.*
- **Required files** — 1x MEBES job deck or Wafer Map (for the Mix and Match Flow only).

1. OASIS® is a registered trademark of Thomas Grebinski and licensed for use to SEMI®, San Jose. SEMI® is a registered trademark of Semiconductor Equipment and Materials International.

For further information on all products related to the Job Deck Editor, refer to the following table.

Table 1-1. Related Products and Their Manuals

Related Products	Documentation
Calibre® FRACTUREc™ Calibre® FRACTUREh™ Calibre® FRACTUREi™ Calibre® FRACTUREj™ Calibre® FRACTUREm™ Calibre® FRACTUREn™ Calibre® FRACTUREp™ Calibre® FRACTUREt™ Calibre® FRACTUREv™ Calibre® MDPmerge™ Calibre® MDPstat™ Calibre® MDPverify™ Calibre® MPCpro™ Calibre® MASKOPT™ Calibre® MDP Embedded SVRF	*Calibre Mask Data Preparation User's and Reference Manual* *Calibre Release Notes*
Calibre® MDPview™	*Calibre MDPview User's and Reference Manual* *Calibre Release Notes*
Calibre® Interactive™ Calibre® RVE™	*Calibre Interactive User's Manual* *Calibre RVE User's Manual*
Calibre® nmDRC™ Calibre® nmDRC-H™	*Calibre Release Notes* *Calibre Verification User's Manual* *Standard Verification Rule Format (SVRF) Manual*
Calibre® WORKbench™	*Calibre WORKbench User's and Reference Manual*
Tcl/Tk Batch Commands	*Calibre DESIGNrev Reference Manual*
Calibre® Metrology API (MAPI)	*Calibre Metrology API (MAPI) User's and Reference Manual*

Table 1-1. Related Products and Their Manuals (cont.)

Related Products	Documentation
Calibre® Job Deck Editor	*Calibre Job Deck Editor User's Manual*
Calibre® nmMPC™ Calibre® nmCLMPC	*Calibre nmMPC and Calibre nmCLMPC User's and Reference Manual*
Calibre® MDPDefectAvoidance™	*Calibre MDPDefectAvoidance User's Manual*
Calibre® MPCverify	*Calibre MPCverify User's and Reference Manual*
Calibre® DefectReview™	*Calibre DefectReview User's Manual*
Calibre® MDPAutoClassify™	*Calibre MDPAutoClassify User's Manual*
Calibre®DefectClassify™	*Calibre DefectClassify User's Manual*

Calibre Job Deck Editor Workflow

There are two basic process flows for using the Job Deck Editor.

- 1x Mask: All layers for a product are exposed on 1x mask
- Mix and Match: Only the non-critical backend layers are exposed with 1x masks (full wafer exposure), while the front end layers are exposed using reduction reticles.

1x Mask

For this flow there is no predefined wafer map, the tool needs to generate an optimized wafer map to give the maximum number of yielding die on the wafer, based on certain user inputs. The input is either a MEBES job deck or OASIS file.

The 1x Mask Process flow is summarized in Table 1-2:

Table 1-2. 1x Mask Process

Stage	Description
Stage 1 - Input Layer	Input a 1x mask job deck containing the product layout and a wafer map.
Stage 2 - Full Chip Placement	Generate an optimized full-wafer placement of this product layout according to user inputs.
Stage 3 - Exclude Chips From Exposure	Select an exclusion rule to be applied on chips that lay on the excluded zone either to be deleted or replaced by other chips.
Stage 4 - Manual Editing	Manually correct any problems by editing the OASIS file.
Stage 5 - Generate a Job Deck	Either save the work as an OASIS layout or fracture to generate a MEBES job deck.

The full process is documented in the section “1x Mask Flow” on page 17.

Mix and Match

For this flow, the wafer map and the optimized chip placement parameters are provided as an input file. The geometry to be placed is also given in MEBES pattern format.

The work flow for the Mix and Match process is summarized in Table 1-3:

Table 1-3. Mix and Match Process

Stage	Description
Stage 1 - Input Wafer Map	Input a 1x job deck containing the product layout and a wafer map.
Stage 2 - Reading Chip Placement	The chip placement is already done and provided by the input wafer map file.
Stage 3 - Exclude Chips From Exposure	Chip placement can be controlled by specifying the allowed placements for this chip.
Stage 4 - Manual Editing	Manually correct any problems by editing the OASIS file.
Stage 5 - Generate Job Deck	Either save the work as an OASIS layout or fracture to generate a MEBES job deck.

The full process is documented in the section "Mix and Match Flow" on page 23.

Calibre Job Deck Editor Modes of Operation

The Job Deck Editor is accessed from the Calibre WORKbench or Calibre MDPview interface.

Procedure

1. Invoke the Job Deck Editor using one of the following methods:
   - From the command line:

     ```
     calibrewb -jobedit
     ```

   - From Calibre WORKbench or Calibre MDPview, select **Tools > Jobdeck Editor**.
   - Interactive GUI mode: When you invoke in the Interactive GUI mode, you have access to both the viewer and the shell (also called terminal) window. In the viewer, you issue commands using the mouse, menus, and dialog boxes. In the shell window, you issue commands by typing them. You invoke in interactive GUI mode whenever you invoke Calibre WORKbench or Calibre MDPview without a script name or use the -a or -shell arguments.
   - Batch mode: The Job Deck Editor can also be run in batch mode from the Calibre WORKbench or MDPview command shell.In the command shell, input the following command to run Job Deck Editor commands in batch mode:

     ```
     JobdeckEditor::runBatch filename
     ```

     where the *filename* is a ".jde" file (the saved session from the GUI). This file is generated by saving session in the GUI mode, or you can edit this file and change its values in any text editor. Alternatively, the Job Deck Editor can work in batch mode

without opening the calibtrewb./calibremdpv window using the following command:

```
calibrewb -jobedit -gui -a "JobdeckEditor::filename"
```

2. Begin using the Job Deck Editor to generate an optimized chip placement on the wafer using the flows described in this document.

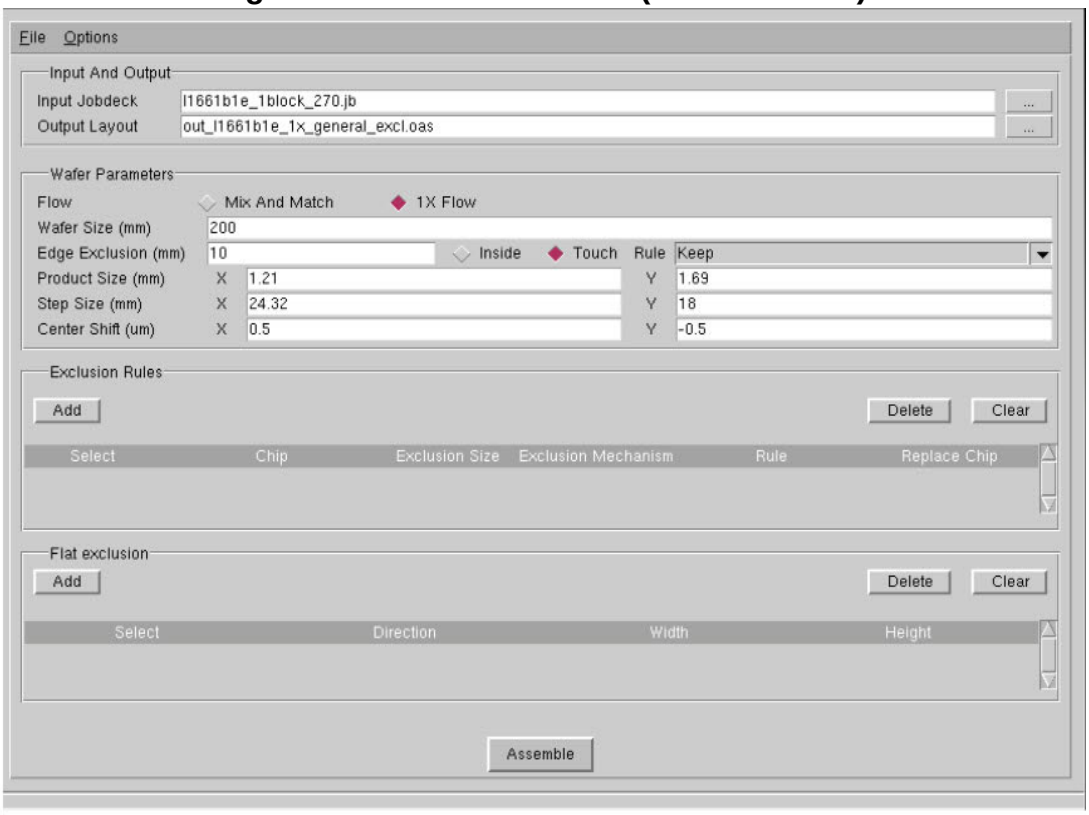
Chapter 2
Using the Calibre Job Deck Editor

There are two main workflows of the Calibre Job Deck Editor: 1x Mask and Mix and Match.

1x Mask Flow

For this flow, there is no predefined wafer map, the tool needs to generate an optimized wafer map to give the maximum number of yielding die on the wafer, based on certain user inputs.

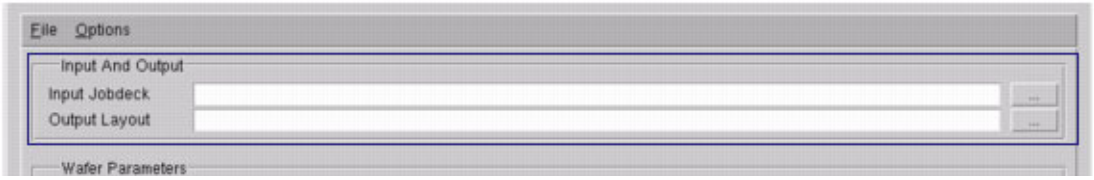
Figure 2-1. Job Deck Editor (1x Mask Flow)



Procedure

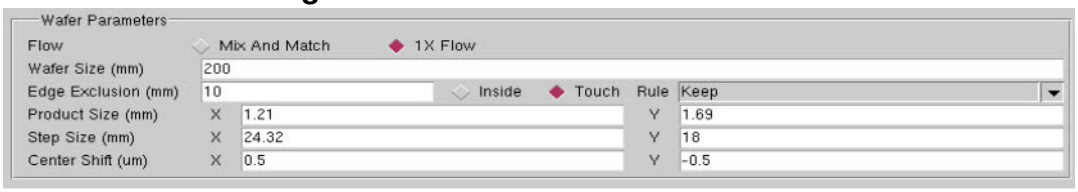
1. Invoke Calibre WORKbench or Calibre MDPview, and select **Tools > Jobdeck Editor**. This invokes the Job Deck Editor (see Figure 2-1).
2. At the top of the Job Deck Editor, enter the input job deck and output layout. The input job deck should be either a 1x mask MEBES job deck that contains the product chip layout with KERF structures or an OASIS file.

Figure 2-2. Select Input and Output (1x Mask Flow)



3. In the Wafer Parameters section (see Figure 2-3), select**1 X Flow**. This reveals several 1 X Flow-specific optimization parameters that must be filled in as input. These include:
   - **Wafer size** — Enter the wafer size.

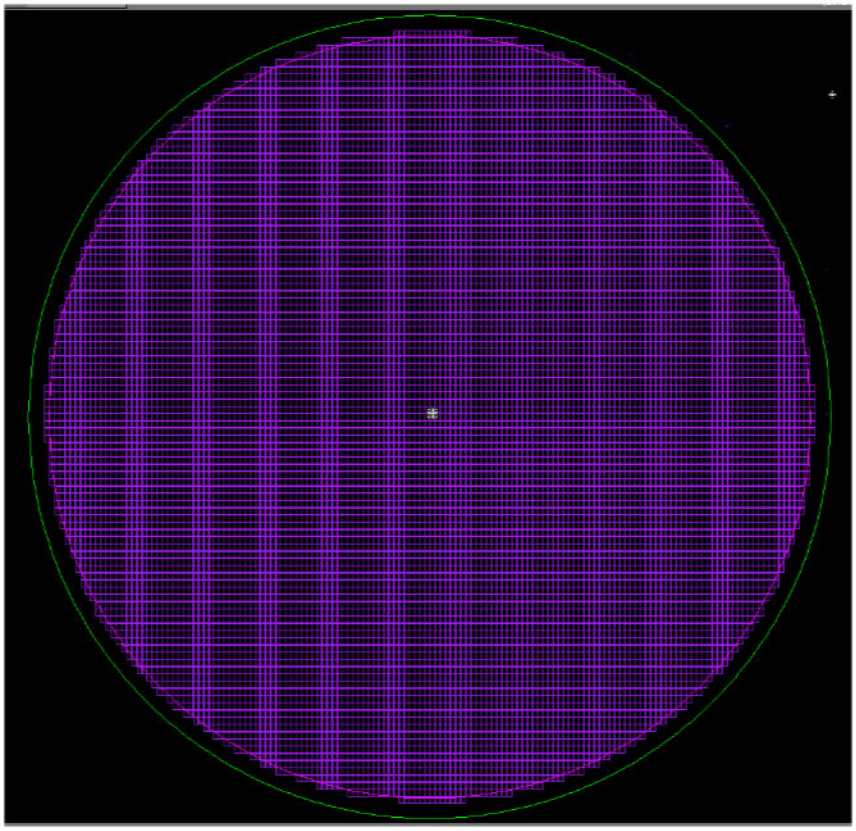
Figure 2-3. Enter Wafer Parameters



   - **Edge exclusion size** — Enter an exclusion size value as well as an exclusion mechanism (Inside or Touch) and an exclusion rule (Remove or Keep).
   - **Product size** — Enter X and Y coordinates for the main product size.
   - **Step Size** — Enter X and Y coordinates.
   - **Center Shift** — Enter center shift X and Y values from which to start the placement of chips. Center Shift is used to shift the wafer map for the generation of 1X job decks. The 1X job deck places a frame with its center shifted by the specified value from the center of the original 1X mask and generates the new 1X mask considering the exclusion rules provided.

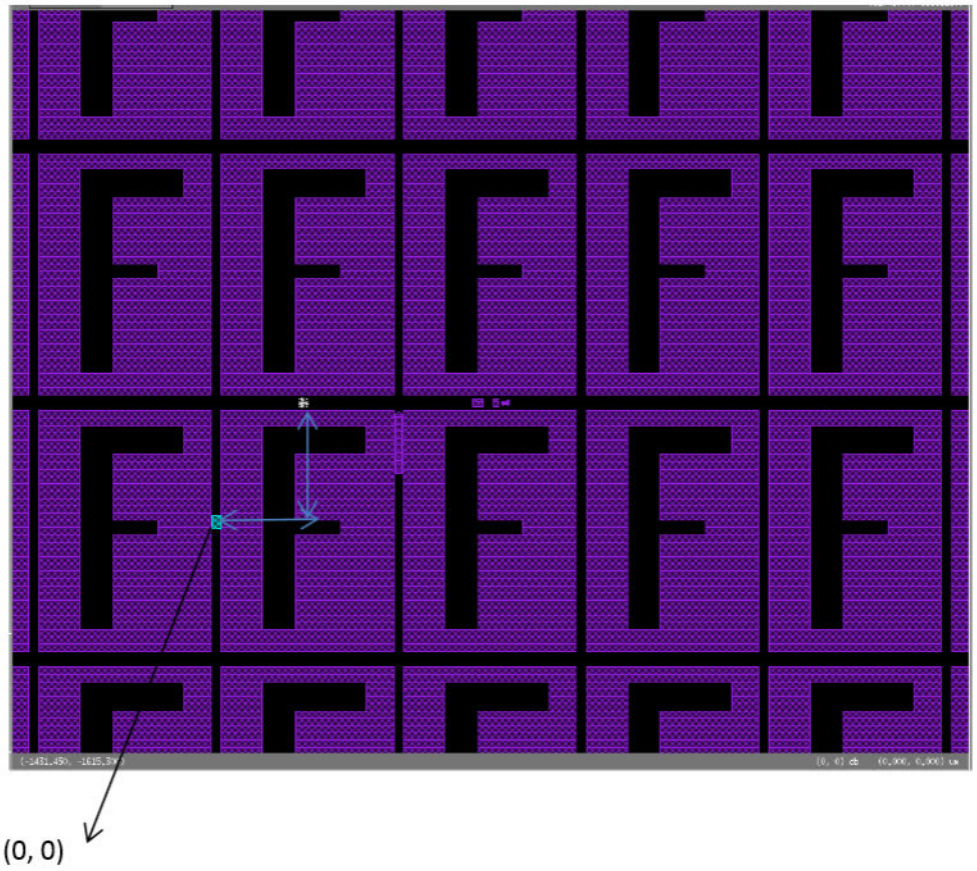
For example following figure shows the JDE run result with the automatic center calculation:

Figure 2-4. Automatic Center Calculation



The center of the placement is shifted from the center of the wafer circle (0,0) as shown in the following figure:

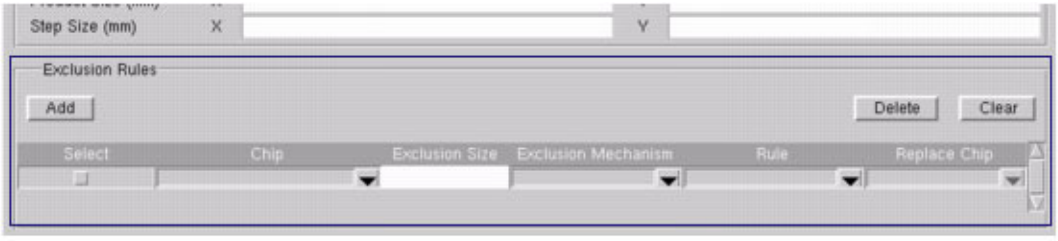
Figure 2-5. X- and Y-Shift From Center of Wafer Circle



The Job Deck Editor issues a warning if these values are not numeric values, and are saved and loaded with the normal JDE sessions. If these fields are empty, the tool automatically calculates the center as before.

4. In the Exclusion Rules section (see Figure 2-6), click the **Add** button to begin adding exclusion rules. A new input row appears each time you click the **Add** button.

Figure 2-6. Add Exclusion Rules



5. Select an exclusion rule to be applied to chips that lay on the excluded zone either to be deleted or replaced by other chips. You can choose the exclusion mechanism to be

applied on a selected chip, select all placements, and apply the exclusion size and mechanism as required. In the input row, enter or select the following information:

- Chip
- Exclusion Size
- Exclusion Mechanism: Select one of the following mechanisms:
  - Inside: All chips inside of the edge exclusion line are contained
  - Touch: Chips touching the edge exclusion line are contained
- Rule: Select one of the following:
  - Keep: Keep the existing pattern
  - Remove: Remove the pattern
  - Replace: Replace with another pattern
- Replace Chip: Specify the chip to replace the excluded chips.

In addition, there is a flat exclusion for flat and notch areas. In this area, you can add multiple flat exclusion rules by clicking the **Add** button. Enter the direction of the notch/flat areas with the width and length of area to be cleared.

Figure 2-7. Flat Exclusion

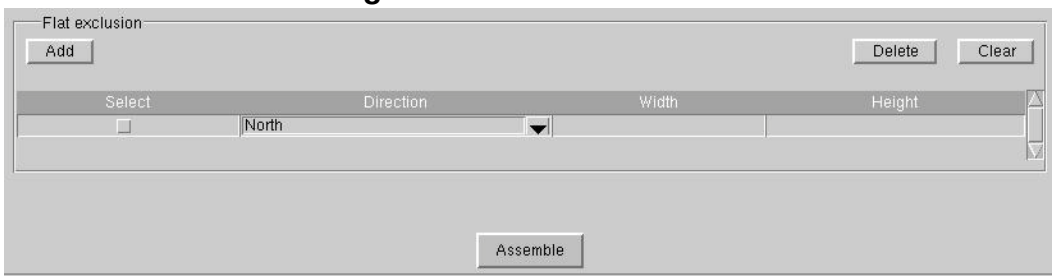


Figure 2-8 and Figure 2-9 show what happens when exclusion is applied for a touch edge.

Figure 2-8. Green Chips to be Contained if Touching Edge Exclusion Boundary

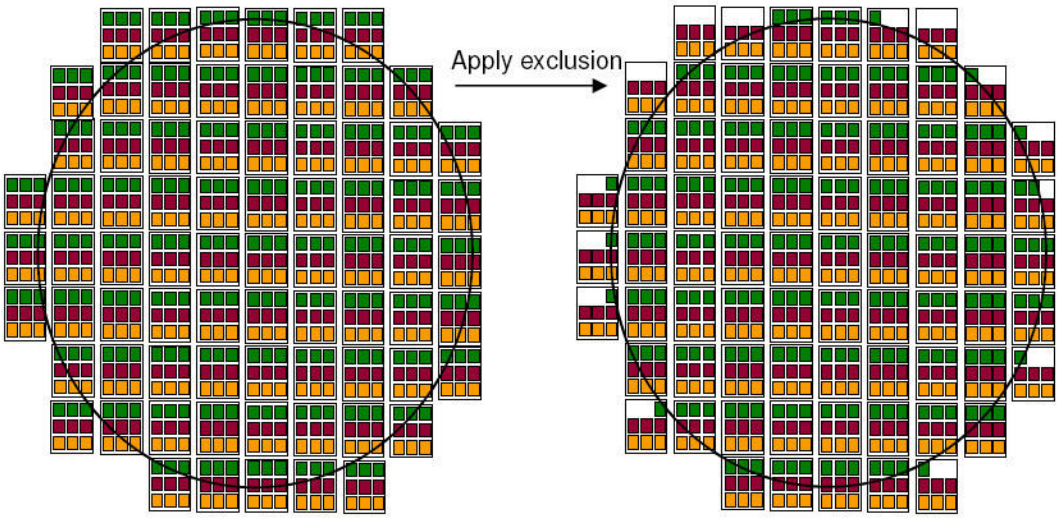
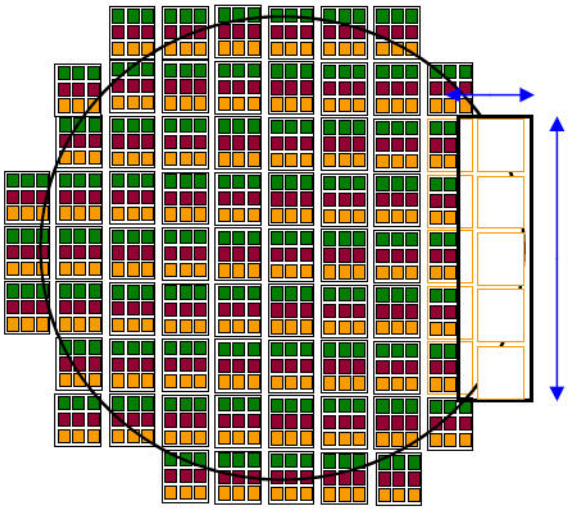


Figure 2-9. Edge Exclusion Boundary



Exclusions are saved in exclusion rule files (.exl). See “Exclusion Rule File Format” on page 31 for complete details on the exclusion rule files.

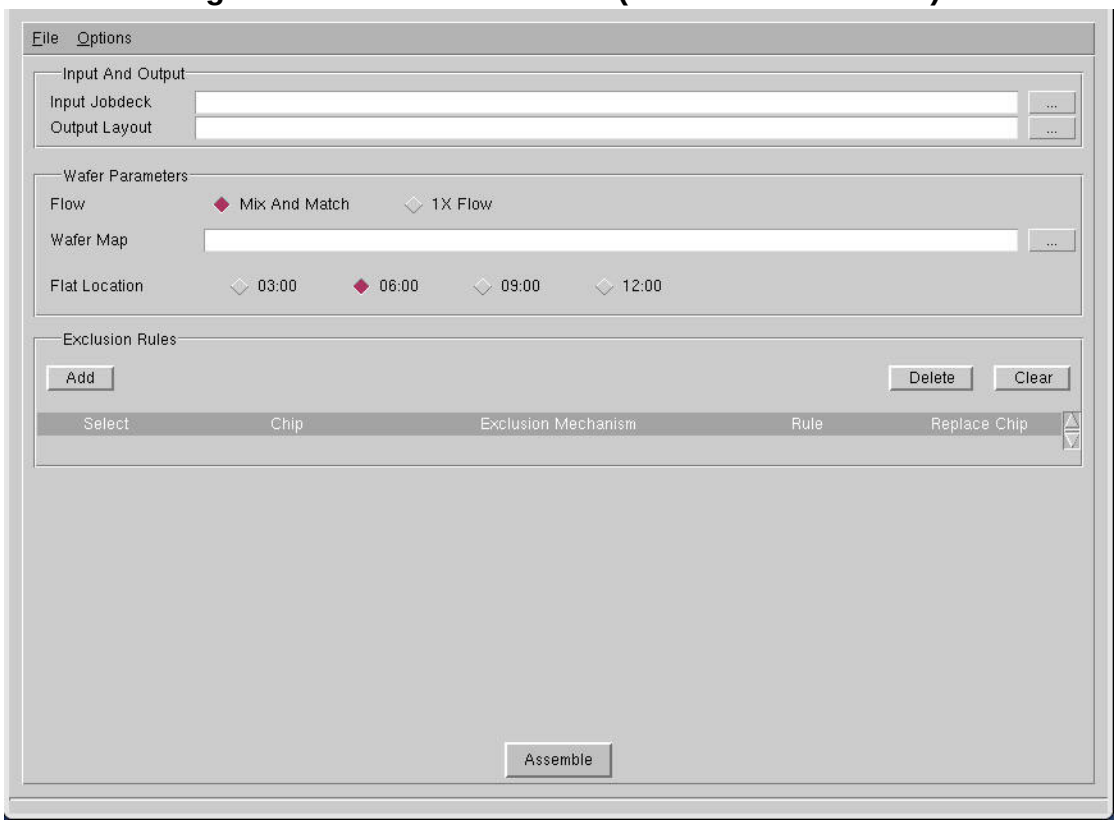
6. You can use Calibre WORKbench or MDPview to make manual adjustments to the chip itself (see “Manual Job Deck Editing” on page 26 for possible operations).
7. Click the **Assemble** button. The tool generates an OASIS layout, which is then fractured to a MEBES pattern and added to the job deck.

   You can also save the session by selecting **File > Save Session** (you can reload the session by selection **File > Load Session**). The session is saved as a .jde file.

Mix and Match Flow

For this flow, the wafer map and the optimized chip placement parameters are provided as an input file. The geometry to be placed is also given in MEBES pattern format.

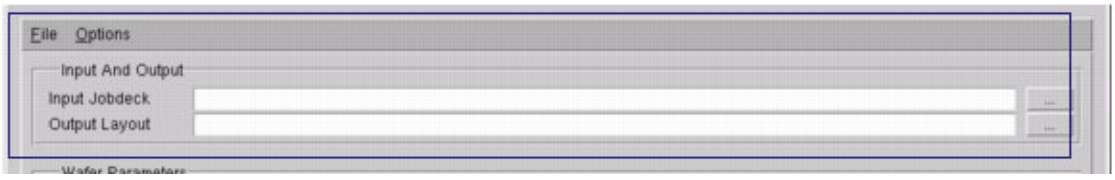
Figure 2-10. Job Deck Editor (Mix and Match Flow)



Procedure

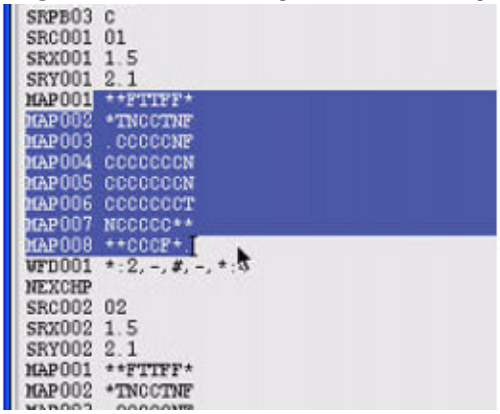
1. Invoke Calibre WORKbench or Calibre MDPview, and select **Tools** > **Jobdeck Editor**. This invokes the Job Deck Editor (see Figure 2-1).
2. At the top of the Job Deck Editor, enter the input job deck and output layout.

Figure 2-11. Select Input and Output (Mix and Match Flow)



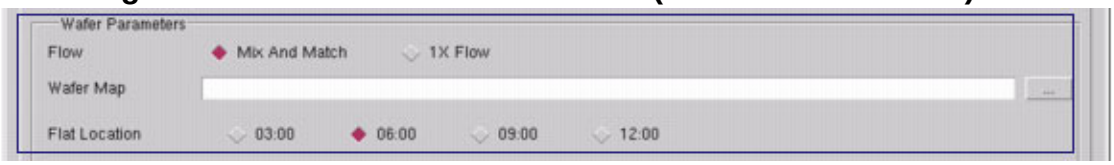
3. In the Wafer Parameters section (see Figure 2-13), select **Mix and Match**. This reveals a specific Mix and Match Flow parameter, the Wafer Map.

Figure 2-12. Example Wafer Map



Enter the wafer map as input. The chip placement is already done and provided by the input wafer map file.

Figure 2-13. Enter Wafer Parameters (Mix and Match Flow)



In Flat Location, set the flat/notch location by rotating the assembled placements in one of the 4 directions (clock positions) listed (03:00, 06:00, 09:00, and 12:00).

4. In the Exclusion Rules section (see Figure 2-14), click the **Add** button to begin adding exclusion rules. A new input row appears.

Figure 2-14. Add Exclusion Rules (Mix and Match Flow)

5. In the input row, you can control chip placement by specifying the allowed placements for this chip. Enter the following:
   - Chip: Select the chip.
   - Exclusion Mechanism: Select one of the following mechanisms:
     - Center on wafer — Non-productive chip with center on the wafer
     - Chip on wafer — Non-productive chip completely on wafer
     - Center outside wafer in shot
     - Center outside wafer off shot

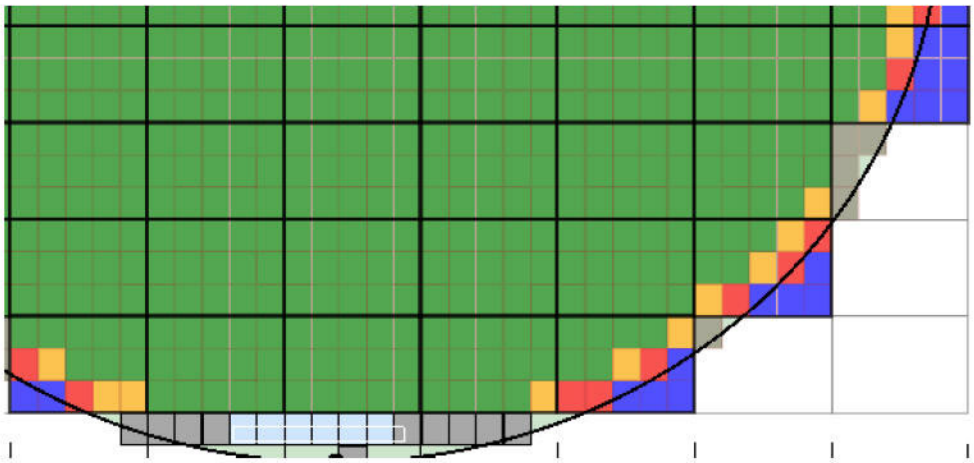
- Center inside wafer off shot

The following exclusion parameters are for Frame/Kerf structures:

- Shot not exposed
- Shot partially off wafer

For example, in Figure 2-15, chips that are not in green are to be controlled by the user for each pattern.

Figure 2-15. Exclude Chips from Exposure



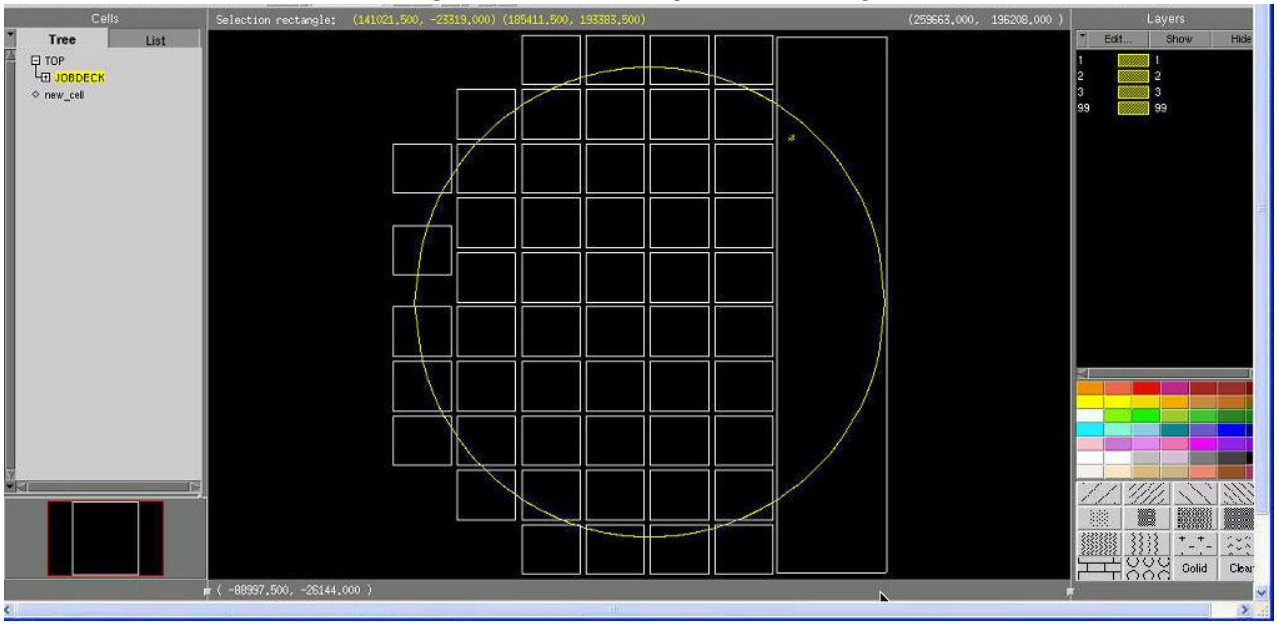
Exclusions are saved in exclusion rule files (.exl). See "Exclusion Rule File Format" on page 31 for complete details on the exclusion rule files.

- Rule: Given the results of the exclusion mechanism, you can select one of the following:
  - Keep — Keeps the existing placements
  - Replace — Replaces with another pattern
- Replace Chip: Specify the chip to replace the excluded chips.

6. You can use Calibre WORKbench or MDPview to make manual adjustments to the chip itself (see "Manual Job Deck Editing" on page 26 for possible operations).
7. Click the **Assemble** button. The tool generates an OASIS layout, which is then fractured to a MEBES pattern and added to the job deck.

   You can also save the session by selecting **File> Save Session** (you can reload the session by choosing **File > Load Session**). The session is saved as a *.jde* file.

Figure 2-16. Example Assembly



Manual Job Deck Editing

You can use Calibre WORKbench or MDPview to perform additional manual editing operations of the job deck .

The following operations are largely described in the *Calibre DESIGNrev User's Manual*. These include:

- Delete a chip.

  Select the chip in the layout and press the **Delete** key.

- Add a chip using **Object > Import Cell**.

  Select the pattern to be added with its X and Y location. Identical chips can also be created as Cell References, which enables you to place references of the same cell in the design rather than the actual cell itself.

- Add an array of chips while specifying each of the following:

  - The number of chips
  - The step x and step y for this array
  - The starting position for this array

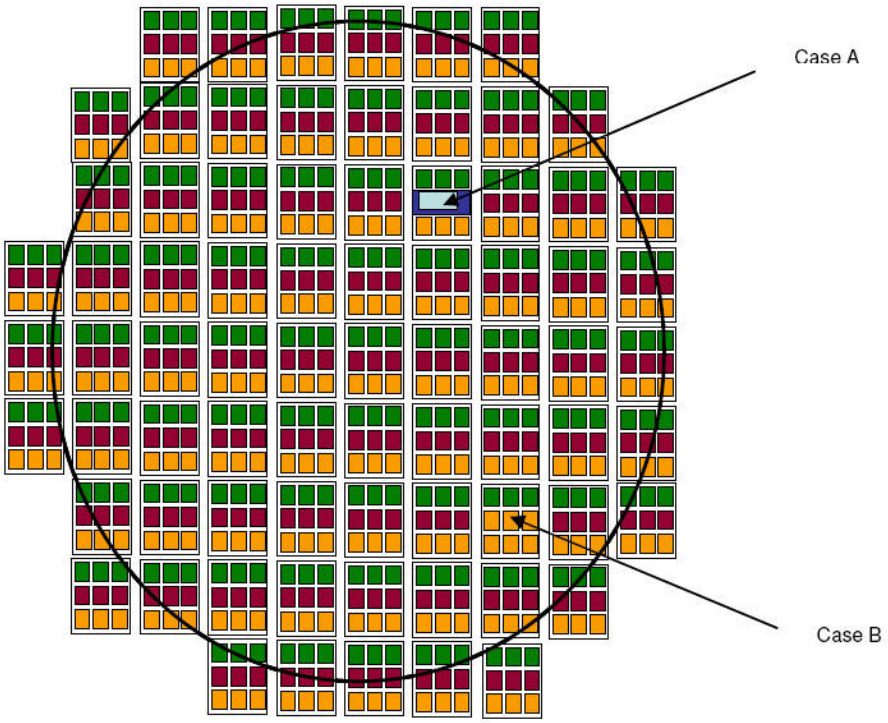
  Arrays of chips can be created by creating Array References, and placing the references in the design in place of arrays of cells (much as you would with cell references).

- Replace a chip or more using **Object > Replace Cell**.

If you created cell references, one replacement can replace all referenced cells.

- Selected chip placements to be replaced by only one placement of another chip with different extent (illustrated as Case A in Figure 2-17).
- Selected chip placements to be replaced by the same number of placements of another chip (illustrated as Case B in Figure 2-18).

Figure 2-17. Case A and Case B Illustrated



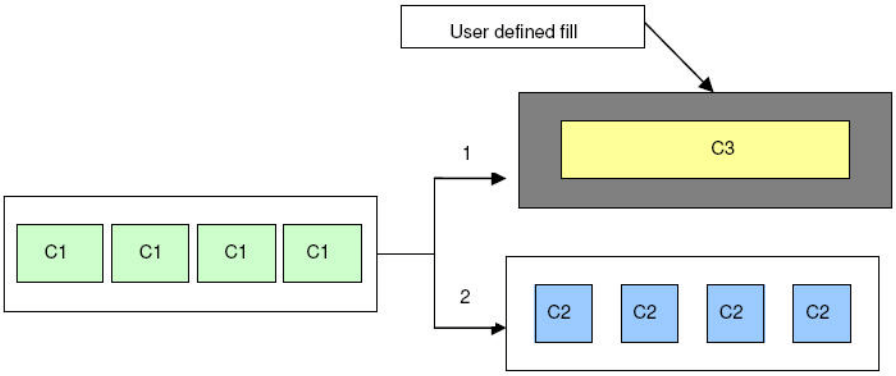
- Clear some locations from the wafer layout by performing a Boolean operation with a user defined layout.
- Move a chip

  Select a chip in Calibre WORKbench or Calibre MDPview and click the **Move** button to move the location.

Tip

You can fill the area between the new placed chips and their neighboring chips. Add the fill pattern as a new cell (as mentioned in in the section "Manual Job Deck Editing" on page 26), then place a reference from this newly imported cell to fill the blank area between the newly-placed cells and their neighboring cells. See Figure 2-18 for an illustration.

Figure 2-18. User-Defined Fill Region

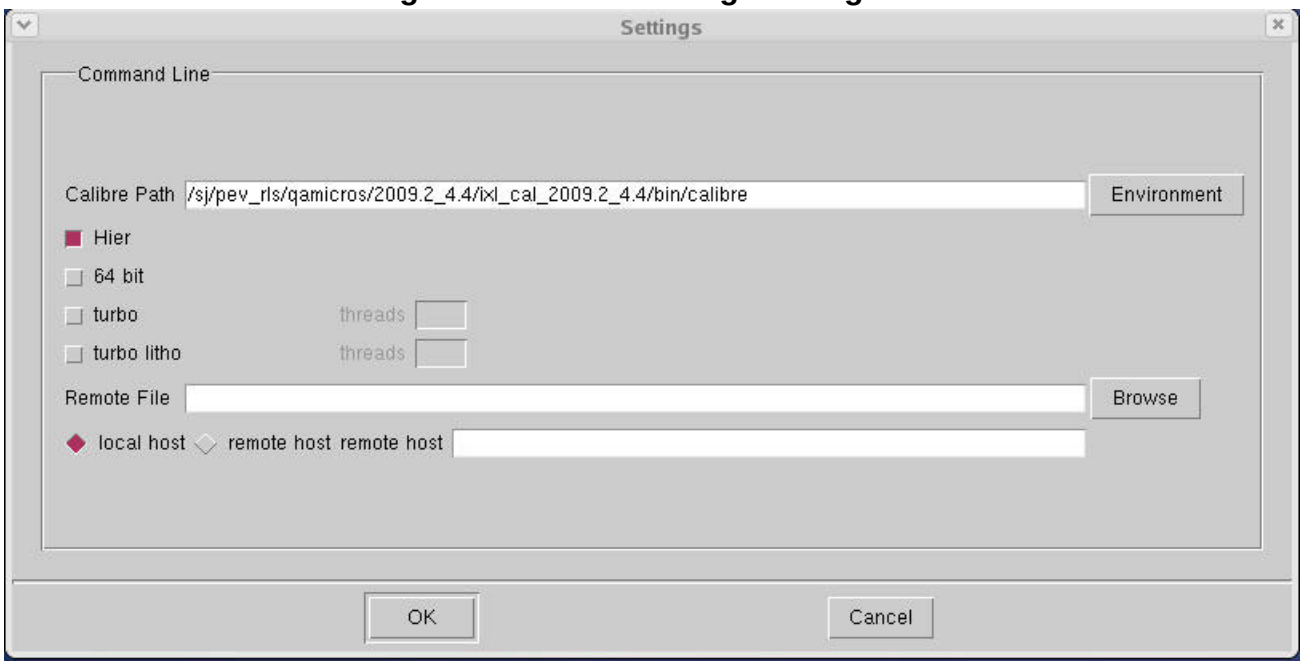


Job Deck Editor File and Options Operations

The Job Deck Editor has a number of operations accessible from the **File** and **Options** menus.

- **File Menu**
  - **Save Session** — Saves the current Job Deck Editor settings (.jde).
  - **Load Session** — Loads a previously saved Job Deck Editor session.
  - **Save Exclusion File** — Saves the exclusion rules to a file (.exl).
  - **Load Exclusion File** — Loads previously-saved exclusion rules.
- **Options Menu**
  - **Run Settings** — Set Calibre options for the execution run (see Figure 2-19).

Figure 2-19. Run Settings Dialog Box



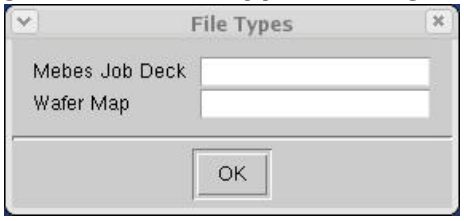
The controls are summarized in Table 2-1.

Table 2-1. Run Settings Dialog Box Controls Summary

Control	Description
Calibre Path	Enter the path to the Calibre executable or click **Environment** to browse for the path.
Run mode	Select **Hier** (hierarchical), 64-bit, turbo, or turbo litho.
Remote File	Enter the name of the remote file.
Host controls	Select local host or remote host.

- **File Types**: Enter the input file names, either a MEBES Job Deck file, or the Wafer Map.

Figure 2-20. File Types Dialog Box



Appendix A
Exclusion Rule File Format

The Calibre Job Deck Editor uses exclusion rule files (.exl files) to specify exclusions used during the workflows.

Exclusion File Syntax

The exclusion file consists of parameters and corresponding values, with the starting and ending delimiters between each subsequent rule. The parameter name is 5 characters

Usage

Number_rule
number_value
Rule_ 1
param_1
...
[*param_ n*]
Rule_end
[Rule_ *n*
...
Rule_end]
End

Arguments

- **Number_rule *number_value***

  Specifies the number rule as the header of the rule exclusion file. The ***number_value*** is an integer number.

- Rule_ 1...[Rule_*n*]

  Begins a particular rule, serving as a delimiter between different rules. The *n* is a numerical value.

- ***param_1*** ...[*param_n*]

  Specifies a rule parameter. The parameter can be one of the following:

  - ExMec *value*— Specifies an exclusion mechanism. Possible *value*s include:
    - Inside: All chips inside of the edge exclusion line are contained.
    - Touch: Chips touching the edge exclusion line are contained.
    - One of the keywords specified in Table A-1.

Table A-1. Rule Parameter Keywords

Value	Description
N	Non-productive chip with center on the wafer.
T	Non-productive chip completely on the wafer but outside the area confined by the technology border.
F	Chip with center outside the wafer included in a placed shot.

Table A-1. Rule Parameter Keywords (cont.)

Value	Description
*	Chip with center outside the wafer of a fictitious not exposed shot.
.	Chip with center inside the wafer of a fictitious not exposed shot.
&	Shot not exposed. This is used for Frame/Kerf structures.
D	Shot partially off wafer. This is used for Frame/Kerf structures.
R	Marks reference chip locations.
Ink	Indicates “ink” fill location.
Out	Indicates “out” fill location.
Skip	Indicates “skip” fill location.

  - ExRul *value* — Specifies an exclusion rule. Possible *value*s include:
    - Delete — Removes the chip.
    - Replace — Replaces the chip with another chip.
    - Keep — Retains the current chip.
  - ExSiz *num* — Specifies the exclusion size as a floating number (the *num* value).
  - ExChp *value* — Specifies the chip to apply the exclusion rule on. Possible *value*s can be:
    - A string that contains the name of the chip.
    - ALL for layer specified exclusion rule.
  - ReChp *value* — Specifies the name of the chip to replace the excluded chip. Possible *value*s include:
    - A string contains the name of the chip.
    - NA for no replace.
  - State *value* — Activates or deactivates the execution of the rule.

- Rule_end

  Specifies the end of a rule.

- End

  Specifies the end of the file.

Examples

Example 1

```
Number_rule  2
Rule_ 1
State Enabled
ExChp S0ZZ09LH2.C2_15_2_0
ExMec F
ExRul  Replace
ReChp  S0ZZ09LH2.C3_15_3_0
Rule_end
Rule_ 2
ExChp S0ZZ09LH2.C1_15_1_0
ExMec N
ExRul  Keep
Rule_end
End
```

Example 2

```
Number_rule  2
Rule_ 1
State Disabled
ExChp S0ZZ09LH2.C1_15_1_0
ExSiz 80
ExMec Touch
ExRul  Replace
ReChp  S0ZZ09LH2.C2_15_2_0
Rule_end
Rule_ 2
ExChp S0ZZ09LH2.C1_15_1_0
ExSiz 110
ExMec Touch
ExRul  Replace
ReChp  S0ZZ09LH2.C6_15_6_0
Rule_end
End
```

Example 3

```
Number_rule  0
Rule_ 1
State Disabled
ExChp S0ZZ09LH2.C6_15_0
ExSiz 16
ExMec Touch
ExRul  Keep
Rule_end
End
```

Import Chips from Different Layouts or Patterns

You can automatically import chips from different layouts/patterns in the Job Deck Editor batch mode. To enable this feature, add the fields described in this section to the exclusion file.

Usage

Imported_cells
cell_ *n*
CelNm *cellname*
SrcCl *source_cell*
SrcLy *layernum*
DesLy *layernum*
SrcPh *path*
cell_imported

Arguments

- **Imported_cells**

  Specifies the beginning of import new cell selection.

- **cell_ *n***

  Specifies the start of new imported cell.

- **CelNm *cellname***

  Specifies the cell name.

- **SrcCl *source_cell***

  Specifies the source cell.

- **SrcLy *layernum***

  Specifies the source layer.

- **DesLy *layernum***

  Specifies the destination layer.

- **SrcPh *path***

  Specifies the layout/pattern path.

- **cell_imported**

  Specifies the end of import new cell section.

Examples

```
Imported_cells
cell_1
CelNm ink
SrcCl TOP
SrcLy 0
DesLy 211
SrcPh /export/home/FILL270B1.A2
cell_imported
```

If the Job Deck Editor encounters the following conditions in the exclusion rule file:

- An exclusion rule with replace
- The rule file does not contain chip information

Calibre issues a warning message and the run will fail to complete.

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Third-Party Information

Details on open source and third-party software that may be included with this product are available in the *<your_software_installation_location>/legal* directory.