Virtuoso Glossary

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Contents

Glossary

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A

abutment

Operation allowing devices to be automatically overlapped, aligned, and electrically connected without introducing a design rule violation or connectivity error. Abutment reduces both the area occupied by a circuit and the length of the interconnect wiring.

AEL expression

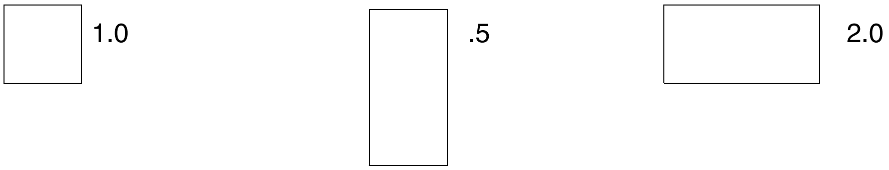
Analog Expression Language (AEL) expressions are used to define design parameters as functions of variables. These expressions are used by the mixed signal and analog netlisters.

analog placement

The placement of physical devices in an analog cell.

aspect ratio

The width-to-height ratio of a layout. Setting a 1:1 ratio results in a square shape.



B

bbox

See **bounding box**.

binder

Layout XL mechanism used to determine and maintain **device correspondence** between a schematic and layout cellview pair.

block rings

Wires around one or more block instances, on a set of specified layers with a specific offset between boundaries of the blocks and the power rings. Rings can follow the contour of the blocks or form a rectangle around the blocks.

bounding box

A rectangular area, identified by a lower left point and an upper right point. Typically used to identify the area of an object (a path or an instance) or a collection of objects (the selected set).

C

CDF

See **Component Description Format**.

.cdsinit

The file that defines the startup environment of the Cadence® software.

cell

A component of a design; a collection of different aspects (representations) of component implementations, such as its schematic, layout, or symbol representations. A design object consisting of a set of views that can be stored and referenced independently. A cell can include other cells, forming a hierarchical design. A cell is an individual building block of a chip or system. In the database, a cell contains all the cellviews of that cell.

An inverter and a buffer are examples of a small cell. A decoder register, arithmetic logic unit (ALU), memories, complete chips, and printed circuit boards are examples of large cells.

cell plan

A plan for cell layout that specifies that devices be placed into specific areas of the cell during analog placement.

cell row straps

Connecting wire straps along aligned power pins of standard cells. The straps can be extended to the end of rows or to the last cell in a physical row.

cellview

A specific representation (view) of a cell. A particular representation of a particular component, such as the physical layout of a flip-flop or the schematic symbol of a NAND gate. A database object containing all the information unique to a particular representation of a particular component. Cellviews are classified by their view type. Each cellview has a view name and can have one or more versions.

chaining

Device abutment where a list of MOS transistors (or the fingers of folded transistors) are chained in a specific order. Chaining helps reduce layout area and capacitance.

CIW

See **Command Interpreter Window**.

clone

A layout structure that has been replicated from a specified source structure already implemented in the layout view. Each clone inherits its physical characteristics from the layout structure on which it is based and connectivity information from the associated schematic structure.

clone family

Multiple clones that have been generated as members of a single synchronized family. The source structure and each individual clone in the family are linked so that changes made to one member are automatically reflected in all other members of the same family.

cloning

The process of identifying and generating **clones**.

Command Interpreter Window (CIW)

The window that launches any Virtuoso Studio design environment application. The CIW logs your design session and reports messages.

Component Description Format (CDF)

A feature that lets you assign attributes, properties, and parameters to libraries and cells for such purposes as assigning parameter names and values, allocating units and default values, checking that values lie within specified ranges, dynamically changing how parameters are displayed depending on predefined conditions, and executing Cadence® SKILL programming language functions whenever certain information is changed (callback functions). A cell CDF lets you store information specific to a cell with that cell. For more information, see *Component Description Format*.

component type

A categorization of layout cellviews that share common characteristics, such as component class, parameter and terminal names, and folding threshold value. Devices must be assigned to component types to facilitate folding, chaining, and the identification pseudoparallel nets in Layout XL, and for the placement of devices in rows by the Virtuoso Custom Digital Placer.

complex binding

When a one-to-one, one-to-many, or many-to-one relationship between the bound schematic and layout devices cannot be determined, the binding is defined as being complex.

conduit router

An automatic router that assigns tracks for the globally routed design and, guided by the global routes, lays down as many wires as possible along routing conduits. When conduit routing is complete, guides indicate where connections need to be completed in the detail route stage. The Space-based Router strives to make these guides short in length and ensure that spacing violations can be corrected in the final step.

Configure Physical Hierarchy (CPH)

Utility that lets you specify how a layout implementation is generated from a schematic or a Verilog-driven design. *Hierarchy Configuration* mode controls how the physical hierarchy is generated from your logical design; *Component Types* mode lets you view and change component types, which identify NMOS and PMOS transistor cells and set the parameters for folding, chaining, and the identification of pseudoparallel nets; *Soft Block* mode lets you configure and specify bindings for the soft blocks that will be created by the *Floorplan – Generate Physical Hierarchy command*.

Connectivity-driven design

A connectivity-driven design is the one that relies on connectivity information on its devices to achieve correct construction.

connectivity extraction

The process of propagating the connectivity of a physical implementation, verifying that it is legal, and generating markers to show open and short circuits, illegal overlaps, and pin model and technology rule violations in the design.

constraint

The restrictions set on objects in a layout or schematic to meet the routing or placement requirements in a design.

constraint aware editing

The constraintAwareEditing switch ensures that the Move, Stretch, and Rotate commands honor the following constraints: Symmetry, Matched Parameters, Orientation, Relative Orientation, Alignment, Fixed, and Locked.

constraint group

A collection of constraints and process rules created for a technology database or specific design.

Constraint Manager

A dockable assistant pane that lets you define, manage, and transfer constraints throughout the custom IC design flow. You can define constraints that affect design elements such as nets, instances, devices, parameterized cells (Pcells), and ROD objects.

core rings

Pads connected around the core of a design if the design has pads. Core rings route around the entire design if there are no pads.

current directory

The directory in which you started the Cadence® software.

D

DRD

Design Rule Driven editing provides real-time design rule feedback to facilitate correct by construction layout.

default value

The value used by the software unless you specify otherwise. The default is frequently the initial state.

design

The collection of all data in a cellview, including all nested data, starting at the top and expanding the hierarchy.

design library

A library that contains data for the current design. It is usually in the designer's own directory or in the design group's directory.

detail router

An automatic router that runs multiple passes in cycles to complete the routing of all nets and resolve violations. The initial routing passes attempt to connect all the unroutes and resolve violations such as different net and same net spacing, minimum area, grids, and weak connects. Subsequent routing passes modify the routed wiring using rip-up and retry methods that strive to continuously improve overall results. Additional cycles deal with any remaining DRC violations including same net violations, minimum width, minimum area, and minimum enclosed area violations.

device

A design element that has both a symbol view and a layout view, with corresponding pins.

device correspondence

The mapping between the components in a schematic and layout cellview pair in Layout XL. Device correspondence is determined automatically during Layout XL initialization (based on the connectivity of the design) and is updated incrementally during interactive editing. You can also force specific mappings using the Define Device Correspondence command.

Dynamic Selection Assistant

Docked assistant facilitating the identification and selection of specific objects of interest from a densely-populated design window with many overlapping or hierarchical objects. The assistant lists all the objects currently under the mouse pointer in the layout window, ordered by the layer-purpose pair on which a particular object is drawn. The display is updated whenever the mouse pointer is moved in the design window.

E

environment

The hardware and software setup and conditions within which the system operates.

externally connected pins

See **must-connect pins**.

F

feedthrough pin

A pin that forms connections by passing through a cell or instance.

floorplanning

Creating a rough plan to estimate whether a design meets timing and routability criteria.

folding

The process by which a transistor or transistor chain is broken into two or more layout instances with terminals all connected in parallel to the same nets. Used to change the aspect ratio of a transistor or transistor chain and thereby optimize the efficiency of a design.

G

geometric wire

Geometric wires are created using paths, pathSegs, and vias that are not contained within a route. Paths cannot be placed in routes, therefore paths are always geometric data.

Geometric wires are used for special routing (power, ground, clock, etc.). Geometric wires can be used to create custom interconnect that auto signal routers will not modify when re-routing, rip-up, and pushing wires. Geometric wires correspond to the DEF SPECIALNETS statement definition.

global router

An automatic router that replaces all open connections with global routes. The global router also reroutes to reduce congestion so the resulting interconnect closely approximates a legally routed design. Information from the global router can be used to seed the detailed routing stages and provide a good estimation of the detailed routes.

guard ring

A ring-shaped conductor used around one or more sensitive devices or circuit sections. It helps guard against spurious or unwanted signals or leakage to or from that device or circuit section.

H

halo

An obstruction or blockage. Common halo blockage types are: placement, routing, slot, pin, fill, feedthru, screen.

hierarchy

Nested design levels, such as instances within a cell. By default, you open the top level in the hierarchy when you open a cellview.

hierarchy configuration

Specification of how the physical hierarchy is generated from your logical design, including which logical components are to be generated or ignored in the physical implementation and which physical views are used to implement logical components. *See* **Configure Physical Hierarchy**.

highlights

Graphical emphases of certain design objects or routing conditions to help identify them.

I

instance

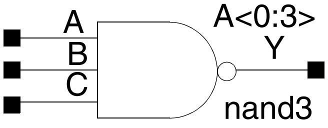
A database object that creates a level of hierarchy. An instance creates an occurrence of the referenced cellview.

internally connected pins

See **strongly connected pins**.

iterated instances

A compact way of displaying repeated instances of a symbol in a schematic, particularly useful in bus-type or data-flow architectures that have identical structures to handle each bit on the bus. To add several instances of the same type, you can express multiple unique names with an iterative expression. For example, A<0:3> generates one graphic representing four instances: A0, A1, A2, and A3.



L

LAM file

See **library and attributes mapping file**.

layer

A layer refers to a mask material. Various database shape objects are created referencing a layer and a purpose. See LPP (layer purpose pair).

Layer Selection Window (LSW)

A window that lets you choose the design layer for objects in the layout, make design objects.
IC6.1.5 release onwards, Palette Assistants replace the LSW. The Palette assistants are available by default. To enable the LSW, set the CDS_PALETTE_OFF environment variable.

library

A library is a logical collection of design data implemented as a physical collection of directories and files that can reside anywhere in the file system. A library can be shared by all users or controlled by a single person. For complete description of library, see *Cadence Library Structure*.

library and attributes mapping file

Text file used in **hierarchy configuration** to store the symbol properties that drive layout generation, the component type information for a given library, and the library- and cell-level mapping information for a specific design. The file is stored in the following location: `*library*/.cadence/dfII/cph/lam/cph.lam`.

Library Manager

The Cadence® tool that displays the list of available libraries in your search path as well as any open libraries. You can use the Library Manager to search through your libraries, cells, views, cellviews, and versions.

local router

An automatic router that adds pin escapes.

Logical connectivity

Logical connectivity on an instance can be defined as the connectivity derived when the instance terminals of an instance are assigned to a net, and there may be no overlapping shapes or routing shapes present that physically connect the instance.

Logical connectivity gets created on an instance when:

- ❑ Propagating Nets by using the *Propagate Nets* command.
- ❑ Running the incremental binder. The binder propagates connectivity from the bound schematic instance to the layout instance.
- ❑ Running a Generate command, such as *Generate All From Source*, in Layout XL adds logical connectivity to the layout instances.

LPP (layer purpose pair)

A physical or other design entity used as a visual representation of different types of information, such as mask geometries and interconnection in schematics. Each unique layer purpose pair has its own colors, highlighting, menus, and design objects. See layer.

LSW

See **Layer Selection Window**.

LVS-clean design

A design for which the Layout versus Schematic check has resulted in no major violations or mismatches is called an LVS-clean design.

M

master cell

Any layout cell you have placed in another cell. The placed copy of the cell is called a **cell instance**.

master symbol

A representation of a design, such as an arithmetic logic unit (ALU) or register. In a schematic, an instance is linked to the master symbol; it is not a copy of the master symbol.

You can create a master symbol for a design and then place virtual copies (instances) of it throughout other designs.

modgen

A complex, highly matched, structured array of multiple Pcell instances.

multipart path (mpp)

A multipart path is a named path that has relative object design (ROD) information associated with it. You can create simple one-part paths or complex paths containing several parts, such as a guard ring, transistor, bus, or shielded path. A path that consists of more than one part is called a multipart path.

must-connect pins

Pins, all of which, are connected only outside a cell and are not connected inside the cell. They are also called externally connected pins. Examples of such pins include feedthroughs, I/O pad ring structures, and pins in cells depending on external shorting connections.

N

Navigator

A dockable assistant that provides a hierarchical snapshot of all the devices, nets, and pins that exist in the design area. It helps you navigate through a hierarchical design to find the components you are looking for. Selecting a component in the Navigator selects the corresponding device in the design area. Similarly, selecting a component in the design areas selects the component in Navigator.

net

A logical signal connection between a set of pins on different instances. After routing, a net consists of routed wires on the routing layers.

P

pad rings

Pad rings are routed between pads on the periphery of a design. You can route to rail pins and/or edge pins on pads.

pan

To view a design by moving it in the window.

parameterized cell (Pcell)

A master cell that has parameters such as length and width. When creating an instance, you can change these parameters without changing the master cell. Parameterized cells are often called “Pcells.”

path

A path object is a shaped based object represented by a point array with a specified width, style, and layer-purpose pair. Paths support anyAngle mode. When used to create non-orthogonal routing, paths can lead to off-grid vertices depending on the width and angle being used.

pathSeg

A pathSeg is a specialized shaped based object represented by a specified width, a layer-purpose pair, and a two-point routing segment with a style associated with each of the points. PathSegs can either be orthogonal or diagonal and can be used to create on grid 45 degree wires. Custom end styles containing octagonal edges are used in diagonal pathSegs to put all vertices on grid.

Pcell

See **parameterized cell**.

physical binding

Binding defined in CPH. Physical binding indicates which layout cellview should be used for a schematic occurrence, instance, or cell. But, it does specify which instance of this cell in the layout to bind to, which is indicated by instance binding.

physical configuration cellview

Cellview comprising a number of different files that store design-specific overrides, including the schematic expansion rules that drive layout generation; design component types; and cell and instance mapping rules. Every Layout XL session operates in the context of a physical configuration view.

Physical connectivity

Physical connectivity is the connectivity derived from overlapping shapes and instances in the layout, such as pins and labels.

pin

A physical implementation of a terminal. You can place pins on any layer. Pins have a figure defining the physical implementation and a terminal defining the type, such as input, output, jumper, etc. Pins also have names, access directions and placement status.

pin permutation

Process of exchanging the connectivity or net connections of the pins of a component in order to facilitate abutment or remove a short created by moving or stretching a shape or by any other operation that changes connectivity. Pins to be permuted must belong to different nets and must first be defined as permutable terminals.

pin-to-trunk connections

Connections between power pins on blocks or power pads and existing power rings or stripes.

post-route refinement

Checks for and attempts to fix specific types of violations by ripping up wiring and rerouting. Refinement also improves wiring by rerouting short connections and removing unnecessary vias.

power router

An automatic router for routing power nets in a design. The power router supports the following routing styles: pad ring, core ring, block ring, stripes, cell rows, pin to trunk, vias.

process rule

A rule that constrains the implementation of a design based on the physical characteristics of the process technology being used.

Process Rule Editor

Enables creating new process rules and constraint groups and apply them to objects, constraints, designs, or technology databases, and change or remove existing process rules and constraint groups already defined.

property

Properties are a name/value pair defining an attribute or characteristic. Properties can be created on any database object. A property can be edited and deleted. Certain properties are mandatory for certain applications. Properties are defined and managed by the application.

pseudoparallel connection

A group of instance terminals on the same net that must be physically connected at the current hierarchy level. Similar to a must-connect; the only difference is that it is implemented not using pins but using instance terminals that belong to a specified net. Recognizing that a connection can be made pseudoparallel saves space because less routing is required to connect it.

R

reference point

The point used to measure the exact distance between objects or line segments as you draw. The distance between reference points is shown in the *Dist* field at the bottom right of the window.

reference library

A library that contains design data for cells placed in the current design, usually a well-verified collection of design objects shared and existing in a public system library.

relative object design (ROD)

A set of high-level functions for defining simple to complex layout objects and their relationships to each other, without the need for using low-level Cadence® SKILL language functions.

ROD

See **relative object design**.

route cells

Route cells are device-less cells that are added in the layout only for routing purposes.

routing

Physically connecting objects in a design according to design rules set in the reference library or technology file.

S

schematic cellview

A cellview that describes the connectivity, gate widths, and gate lengths of transistors.

scheme

A power routing scheme defines environment variables that control options for power routing styles. Each power routing style has a related scheme package: pad ring, core ring, block ring, stripes, cell rows, pin to trunk, vias.

search path

The list of directories the software searches for files, libraries, and commands.

segment of a path

Part of an individual path object. A section of a path.

selection

Choosing one or more objects to put in a selected set for the purpose of performing an action on the selected set.

SKILL

The Cadence® SKILL language is a high-level programming language. Menu commands execute SKILL commands. SKILL is based on the LIS Processing (LISP) programming language but uses a C-like syntax. It is accessible only from within software.

Space-based Router

An automatic constraint driven router allowing gridded or gridless routing of regular and power signals, including specialty routing such as symmetry, differential pairs, and shielding.

stripes

Wires that form a power mesh in the core area of a design. You specify parameters such as which layers to use for the given nets, the clearance required between nets, pin clearance, the location and interval for the stripes. In a later step, vias are inserted in connect the stripes with the mesh to the rings.

strongly connected pins

Pins that are connected inside a cell and one or more than one of them is externally connected. Strongly connected pins share both pin and terminal name. They are also called internally connected pins.

symbolic wire

Symbolic wires are created using pathSegs and vias that are contained within routes. Symbolic wires are typical used for signal routing which is the default for creating wires in Virtuoso. The Virtuoso Shaped-based router only creates well-formed symbolic wires with matching end points.

Symbolic wires correspond to the DEF NETS statement definition.

symmetric nets

Nets having one of the following characteristics.

- ❑ mirror symmetry - two nets mirrored over an axis
- ❑ self symmetry - a single net mirrored over an axis
- ❑ cross symmetry - two nets allowed to cross the symmetry line using one or more instances of crossover cells
- ❑ partial symmetry - nets that are mirror symmetric, self symmetric, or cross symmetric, but do not have the same number of terminals or a portion of the wires are unique on either side of the axis

synchronous clone

Clone generated as a member of a synchronized family. The source structure and each individual synchronous clone in the family are linked so that changes made to one synchronous clone are automatically reflected in all other synchronous clones in the family.

T

technology file

The ASCII technology file is made up of sections and subsections. The various sections of the technology file allow you to specify and define technology file controls for design layers, layer attributes, sites, vias, and devices; design constraints; and layer display in the layer selection window (LSW). For more information, see *The ASCII Technology File and Display Resource File*, in the *Virtuoso Technology Data ASCII Files Reference*.

terminal

The electrical input or output of a net. See pin.

top-down design

An approach to hierarchical design that uses estimates and floorplanning to start at the top level of a design.

U

uniquification

The process of making the occurrence of a module unique in the embedded module hierarchy (EMH). Uniquification of the entire module hierarchy needs to be done before performing any edit operations on the design, which can possibly change the internal hierarchy of the EMH.

V

variants

An instance of data created with one piece of Pcell code. Typically, one Master Pcell produces many instances/variants.

viaDefs

The via definition section of the technology file. The viaDefs section contains both standard via definitions (stdViaDefs) and custom via definitions (customViaDefs).

via insertion

Power routing step that adds vias between power stripes, rings, and block pins. You specify parameters such as the layer range and type of cut array to use.

via pile (via stack)

A set of overlapping vias on adjacent layers that are on the same net. Also called a via stack.

view

The view is a directory contained in the cell directory, which is contained in the library directory. The view directory contains the cellview data. Each view within a cell is a separate file system directory in which Cadence locates all of the files pertaining to a particular view of a given cell.

The view name is user defined. Different views can be used to represent different levels of abstraction of a design (behavior, gate) or different stages in the design process (rtl, postsynthesis). Views can also be used to contain different types of data about a cell (schematic, symbol, layout, vhdl).

view type

Each cellview has a viewType. View types are defined by the database. Based on the viewType, the software can determine the correct editor (application) to for a cellview. For example, Virtuoso Layout Suite L is the application for viewType `maskLayout`.

The following are legal database view types:

```
maskLayout
schematic
schematicSymbol
netlist
wafer
verilogAMSText
VHDLAMSText
verilogText
VHDLText
verilogAText
oaHierDesign
```

W

weakly connected pins

Pins that are connected inside a cell and only one of them is externally connected. Weakly connected pins share the terminal name.

well

A relatively deep, doped area in which devices are fabricated. CMOS requires at least one well because NMOS requires a P background doping and PMOS requires an N background doping.

wire

Wires are interconnect that can be composed of a combination of paths, pathSegs and vias.

wire editor

Design rule correct interactive routing and editing.

X

.Xdefaults

An X Window System startup file that defines the X environment. Your system might have a default .Xdefaults file, or you might have your own .Xdefaults file in your home directory.

XL-compliant design

Designs that can fully leverage the connectivity-driven capabilities and features provided by the Virtuoso Layout Suite XL are called XL-compliant designs. These designs have the correct top-level pins and full device correspondence between schematic and layout with no ungenerated or unbound instances.

For a design to be XL-compliant, it should bring in the connectivity information that is required by the various XL features.