

Electromagnetic Solver Task Assistant

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Contents

1	4
Electromagnetic Solver Task Assistant	4
How to configure process settings for an IC layout?	5
How to configure process setup for a package layout?	5
How to configure setup for a cross fabric design?	6
How to configure simulation settings for Clarity or AXIEM?	7
Related Help Topics	7
How to create ports for models?	7
How to define a model for a full cellview?	8
How to define a model for selected cells and instances?	8
How to simplify shapes?	9
Related Help Topic	9
What are the steps involved in running a simulation?	10
Related Help Topics	10

Electromagnetic Solver Task Assistant

The Electromagnetic Solver assistant provides an interface to create 3D models for passive devices by running s-parameter extraction. The tool allows you to run full wave [3D Solvers, Clarity and 3D EM, or the AXIEM 3D planar solver](#).

You can perform the following tasks to create EM Models:

Configure Process Setup

- [How to configure process settings for an IC layout?](#)
- [How to configure process setup for a package layout?](#)

Define Models

- [How to define a model for a full cellview?](#)
- [How to select nets and instances for models?](#)
- [How to create ports for models?](#)
- [How to simplify shapes?](#)

Run Simulation

- [How to configure simulation settings for Clarity or AXIEM?](#)
- [What are the steps involved in running a simulation?](#)

Create Extracted Views

- [How to create an extracted view?](#)

Related Content: [Electromagnetic Solver User Guide](#) 

How to configure process settings for an IC layout?

For an IC layout, you need to provide process setup information in **.emproc** files that are saved in a process corner directory, which is by default set to the `.cadence/dfII/Sigrity/corners` directory in the current working directory. The EM Solver assistant reads the directory and loads the process corner names in the *Corner* column of the *Models* section.

- [Where to save the process settings for an IC layout?](#) 

When the layer stack information is available in an ICT or QRC technology file:

- Add a reference to the external ICT or QRC technology file along with the mapping information to map the external layers to Virtuoso layer.
- Provide details about substrates, height adjustment values for layers, values for dielectric simplification, and a list of layer-purpose pairs from which shapes are to be extracted.

Related Topics:

- [Syntax of a corner referring to an external stackup](#) 

When the layer stack information is not available in an ICT or QRC technology file:

- Create a custom stackup with details about dielectric, metal, and via layers.
- Provide details about substrates, height adjustment values for layers, values for dielectric simplification, and a list of layer-purpose pairs from which shapes are to be extracted.

Related Topic: [Syntax of a corner defining a custom stackup](#) 

How to configure process setup for a package layout?

For a package layout, the process setup information is read from the technology file and loaded in Virtuoso. If you have imported the layout from Allegro, the settings are also imported. You can validate the settings as described below.

Layer Stackup

1. Choose *RF - Module- Setup - Layer Stack Editor* to open the Layer Stack Editor form.
2. Check the values of thickness, conductivity, and permittivity of each metal and dielectric layer.
3. If required, modify these settings and click *OK*.

Review the dielectric layer above and below the package layer. If needed, use the *Add Layer* command to add layer above and below it.

Related Topic: [Layer Stack Editor](#) 

BGA Balls and Flip Chip Bump Setup

1. Select a BGA or IC instance.
2. Choose *RF - Module- Setup - Bump and Ball Editor* to open the Bump and Ball Editor form.
3. Validate the settings.
4. If required, modify these settings and click *OK*.

Related Topic: [Bump and Ball Settings Editor](#) 

How to configure setup for a cross fabric design?

Cross-fabric extraction allows you to create a model across IC, package and board. It captures the full coupling between fabrics in a single 3D simulation. Each layer has its own models. The objective is to extract a model for the outer-most fabric, which is a board layout. Each fabric in the stack references the models of other fabrics placed within it.

To create a electromagnetic model for a cross fabric design:

1. Ensure that the **prerequisites** are met:
 - Each package and board fabric has a dielectric layer on top and bottom.
 - The height of the balls and bumps for each abstract instance equal to or higher than the height of the solder mask.
1. Open the outer-most fabric in VLS EXL and enable **Co-Design** mode.
2. Following the **bottom-up approach**, open the layout of the lowest fabric and define a model using the required objects from this layout.
3. Switch to the layer above the previous layer. Create a new model by selecting objects from

this layer and **adding a reference** to the die abstracts to be included in the model.

4. Similarly, create models for all fabrics up to the top layer by using references to the other die abstracts.
5. Choose *Simulation – Create and Edit* to run simulation and create n-ports that are saved in an S-param touchstone file.

Related Help Topic

[Extracting Models for a Cross-Fabric Design](#) 

How to configure simulation settings for Clarity or AXIEM?

You can configure the settings to be used by these simulators by using the Simulation Settings form. This form contains a specific tab for each simulator.

Related Help Topics

[Simulation Settings for Clarity](#) 

[Simulation Settings for AXIEM](#) 

How to create ports for models?

If the instances have pins or the selected nets have top-level pins, you can use the auto-generation feature to create ports that you can later review and adjust according to your specifications.

If you want full control on the placement of the ports and their edges, you can choose to create ports manually. Options for port configuration change depending on the simulator.

For more details, see:

[How to create ports for Clarity or 3D-EM models?](#) 


[How to create ports for AXIEM models?](#) 

How to define a model for a full cellview?

If the IC layout is a passive device, we can characterize that layout cellview as an S-parameter cellview. In addition, you can create a symbol view, which you can use to instantiate the model in a schematic.

To specify that you need to extract a model for the full cellview:

- On the *Selection* tab in the Electromagnetic Solver assistant, select .


After the model is created, use the  (*Create S-Parameter View*) command on the toolbar of the assistant to create an s-parameter view and an optional symbol view for your cellview. The new views are added to the cell and are also displayed in the Library Manager. You can create instances of this newly-created s-parameter view in your design schematic.

Related Help Topic

[Extracting S-Parameter Models from Complete Layout Cellviews](#) 

How to define a model for selected cells and instances?

When you are characterize selected parts of a layout, select those parts, nets or instances, for a model:

1. Select a model in the *Models* section of the Electromagnetic Solver assistant.
2. Select an instance or net on the layout canvas or in the Navigator assistant.
3. Click  on the *Selection* tab of the assistant.
The selected shape is added to the *Object Selection* list.
4. Similarly, select more nets or instances.
5. If only a specific part of the selected nets or instances is relevant, create a cutting boundary

around the selected objects.



6. When using the Clarity model, for an IC layout, you need to specify a few additional settings:
 - a. *Current Return Path* on the *Selection* tab.
 - b. The scale type and percentage for the die ground.

How to simplify shapes?

By simplifying shapes, you can reduce the fine details in those areas of the layout that might not impact the result of electromagnetic simulation. For example, you can remove small dangling shapes or merge closely placed shapes. This improves the simulation runtime.

To simplify shapes:


1. Click *Setup* on the *Pre-Process* tab of the Electromagnetic Solver Assistant.
The Simplify layout for EM simulations form is displayed.
2. On this form, specify setup for shape simplification.
 - a. Choose the layer-purpose pairs for which you need to remove dangling shapes, merge shapes, stripe shapes, or smooth shape steps.
 - b. Specify the rules to be considered while performing these changes.
3. (Optional) Click *Save As* to save the setup in a recipe file, which can be later loaded to reuse the settings.
4. Click *OK* to close the form.
5. Click *Preview Pre-Preprocessed Layout* on the *Pre-Process* tab.
A preview of simplified shapes is displayed. If required, you can further modify the rules.
6. To protect certain shapes from modifications even if they meet the rules, select those shapes and click *Protect Selected* on the *Pre-Process* tab.

Related Help Topic

[Simplifying Shapes](#) 

What are the steps involved in running a simulation?

Related Help Topics

- [Running a simulation using Clarity](#) 
- [Running a simulation using AXIEM](#) 