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# Digital Mixed-Signal Option to Xcelium Single Core Simulator

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# Digital Mixed-Signal Option to Xcelium Single Core Simulator

The digital mixed-signal option (DMS) to the Xcelium™ Single Core Simulator provides a high-performance, digital-centric, mixed-signal verification environment for full-chip verification. Digital-centric refers to designs that are mostly digital, with some small analog part. Using DMS, you can perform mixed-signal verification on your digital-centric full-chip designs, at near-digital speeds, using digital simulators only.

You can use DMS to perform high-volume, digital-centric nightly regression tests.

Today's full-chip SoC simulations require more accuracy than digital Verilog/VHDL alone can offer. Using real-value models, you can model analog portions of your design discretely. You can move your real-value models between the Virtuoso® design environment and the Incisive verification environment. You can use real-value models as the hand-off between analog and digital designers.

While a single behavioral model can capture both performance and functionality, it is important to consider other practical concerns such as model complexity and simulation speed. Adding functionality to a performance-oriented model can cause a simulation speed penalty. Removing functionality can improve simulation performance, but sometimes at the expense of accuracy. Using real-modeling constructs, such as the Verilog®-AMS `wreal`data type, you can create functional behavioral models with improved simulation performance.

The following links to the *Spectre AMS Designer and Xcelium Simulator Mixed-Signal User Guide* and the *Cadence® Verilog-AMS Language Reference* provide you with details about the Verilog®-AMS language features you can use in your otherwise purely digital designs, depending on whether you have the Xcelium Single Core Simulator with or without the DMS Option (this product is the digital mixed-signal option to the Xcelium Single Core Simulator).

See the following topics for more information:


- Basic Features for Digital Mixed-Signal in Incisive Enterprise Simulator-XL on page 2
- Advanced Features of the Digital Mixed-Signal Option on page 2



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## Basic Features for Digital Mixed-Signal in Incisive Enterprise Simulator-XL

The Xcelium Single Core Simulator supports the basic wreal features of the AMS Designer Simulator such that you can use the Verilog-AMS `wreal` data type in your otherwise purely digital designs.

## Advanced Features of the Digital Mixed-Signal Option

The digital mixed-signal option to the Xcelium Single Core Simulator (DMS Option to XLM) lets you use the Verilog-AMS `wreal` data type and the Verilog-AMS `$table_model` function in your otherwise purely digital designs.

See the following topics for details:

- Advanced wreal Features of the AMS Designer Simulator
- Interpolating with Table Models

  In particular, read about how you can use the `$table_model` function in the digital context (in an `initial` or an `always` block).


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