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Spectre AMS Designer and Xcelium Simulator Known Problems and Solutions

Product Version 22.09
September 2022

Contents

About This Manual

This Known Problems and Solutions document describes important change requests (CCRs) for the Spectre AMS Designer and Xcelium simulator with the mixed-signal option simulators. And, informs you how to solve or work around these problems.

Be aware that the CCR ID format has changed starting with this Xcelium release. Instead of reporting a purely numeric ID such as the following:

CCR 494428: <ccr_title>

New items use an AVSREQ ID as shown:

CCR AVSREQ-114065: <ccr_title>

⚠ The Planned Release information that is included for the CCRs listed in this document reflects the Cadence estimate, at the time of publishing, of when the resolution will be incorporated in the product. Communication of this Planned Release information is for informational purposes only and should not be considered a warranty of any kind. Cadence reserves the right to alter the planned release at any time without notice.

Updated Known Problems and Solutions documents are published at regular intervals. You can view on Cadence Online Support the most up-to-date information about the status of their CCRs.

Product: AMSD

Product Level 2: AMSD

AVSREQ-110428 AMS test case with SV interface to Spice fails when using -ms_perf for multi-supply

> **OS:** ALL **Version:** ALL
>
> **Description**: Custom connect rules are not supported with SystemVerilog-AMS Connect modules (UDN to UDN IE)
>
> This AMS test case crashes when using -ms_perf switch and displays the following message:
>
> ```
> xmelab: *F,INTERR: INTERNAL EXCEPTION
> ```
>
> **Solution**: Currently, there is no workaround.
>
> **Planned Release**: Not currently planned.

CCR 02070704/2072065: SV-AMS connectmodules are not supported via VAMS connrules

OS: ALL **Version:** ALL

Description: Custom connect rules are not supported with SystemVerilog-AMS Connect modules (UDN to UDN IEs). The tool generates the following error when you specify custom connect rules with SV-AMS connect modules

```
xmelab: *E,CUCCSA (./crules.vams,14|6): SVAMS connect module 'EEnet_2_E' is in user defined VAMS
connect rule, which is not allowed.
```

Solution: Currently, there is no workaround. You must use the `-custom_udn_cr` option and the tool automatically creates the connect rules for the SV-AMS connect modules.

Planned Release: Not currently planned.

CCR 02001471: Issue with 'packngo_agent'

OS: ALL **Version:** ALL

Description: With `xrun -packngorec..` option, during `xmelab`, following errors are generated:

However, the issue does not affect the feature functionality.

Solution: None

Planned Release: Not currently planned.

CCR 1946797: Simulation fails when using Xcelium with Spectre17.1ISR6 and displays the message "*E,SIGUSR: Unix Signal SIGILL raised"

OS: ALL **Version:** ALL

Description: When running an AMS SystemC simulation with SPECTRE 17.1 ISR6 or above, and boost library version older than 1.56 is used in the user SystemC code, an error may be encountered. This issue may especially occur when `auto_ptr` is used.

Solution: It is recommended to use boost library version 1.56 or above to run AMS SystemC simulations with SPECTRE 17.1 ISR6 or above.

Planned Release: Not currently planned.

CCR 1702460: AMS simulation with skipdc=sigrampup gives incorrect outputs

OS: ALL **Version:** ALL

Description: The SST2 format waveform does not support minus values in the time axis.

Solution: To work around this problem, do one of the following:

- Switch to the SST2/PSFXL unified format and add the following `xrun` argument in

command-line mode:

```
–amsformat psfxl_all
```

○ In ADE, select *Output>Save All>Output Format>psfxl*.

Planned Release: Not currently planned.

CCR 1331095: Getting MMSIM tokens on multiple servers with a granularity of 1 token when queuing is enabled

OS: ALL **Version:** ALL

Description: If a simulation requires two or more MMSIM tokens that are available on different servers, AMS checks out the MMSIM tokens only from one server, locks the token(s), and waits for other tokens to be available on the same server for the simulation to run when the `–licqueue` option is turned on. For example, if a digital solver requires two MMSIM tokens and one MMSIM token is available on server 1 and the other is available on server 2 and the `–licqueue` option is turned on, AMS checks out the MMSIM token from server1 and even if the token is available in server2, it locks the token from server1 and waits for the token to be available on server1.

Solution: To work around this problem, remove the `–licqueue` option to enable the feature in INCISIV 14.2.

Planned Release: This limitation will be removed in a future release.

CCR 617209: Error loading mdl/libSpectreEH_sh.so in ibmrs/aix platform

OS: AIX **Version:** ALL

Description: Spectre solver reports error as:

```
=============================


Error in opening shared object:     0509-022 Cannot load module
/grid/avs/install/ius/8.2/08.20.001-p/tools.ibmrs/spectre/lib/mdl/libSpectreEH_sh.so.

=============================
```

This problem is noticed if both `LIBPATH` and `LD_LIBRARY_PATH` variables are set.

Solution: Do the following:

```
%unsetenv LD_LIBRARY_PATH
%setenv LIBPATH <ius_install_dir>/tools/lib
```

That solves the problem and the *mdl* library is loaded properly.

Planned Release: Not currently planned.

CCR 560646: ncsim internal error and wrong ELF class message when running 64-bit AMS-

Spectre on Solaris 10 x86_64

OS: SOL86 **Version:** 10

Description: On the Solaris 10 x86_64 platform, running the AMS Designer simulator with the Spectre solver, if you run the 64-bit version of `ncsim` by specifying the *install_dir*`/tools/bin/64bit` directory first in your path, `ncsim` terminates with an internal error: `ncsim: *F,INTERR: INTERNAL ERROR`.

Solution: To work around this problem, do the following:

a. Remove *install_dir*`/tools/bin/64bit` from your path.

b. Use the 32-bit version to run in 64-bit mode by using either the `-64bit` command-line option when you run the executable or by setting the `INCA_64BIT` environment variable.

Planned Release: Not currently planned.

CCR 440028: ncelab cannot resolve hierarchical Verilog-A modules

OS: ALL **Version:** ALL

Description: When you define a Verilog-A top module and Verilog-A submodules in the same file, only the top-level cell has a cellview (veriloga + symbol).

For example, if the file `veriloga.va` contains:

```
`include "constants.vams"
`include "disciplines.vams"

module top (qin, qout);
input qin;
output qout;
electrical qin, qout;
electrical aa1;

sub vd1 (qin, aa1);
sub vd2 (aa1, qout);
endmodule

module sub (in, out);
input in;
output out;
electrical in, out;

analog
V(out) <+ 2.0 * V(in);
endmodule
```

`ncelab` fails with an error message such as the following:

```
ncelab: *E,CUCFUN: instance 'vd1' of the unit 'sub' is unresolved in
'hierVerilogA.hierarchical_mpa:veriloga'.
```

Solution: To work around the problem, do the following:

a. Create a file containing the following statement, where the `ahdl_include` file contains the `veriloga.va` contents printed above.

```
ahdl_include .../veriloga_file.va
```

b. In the hierarchy editor (HED), right-click the cell and choose *Set Cell View -> Source File*.

c. Use the *Browse* button on the form that appears to select the Verilog-A source file.

d. Click *OK*.

Planned Release: Not currently planned.

CCR 305235: AMS Designer has a run-time dependency on ELF libs when run on SUSE Linux 9.0

OS: LINUX **Version:** SLES9_64

Description: When it runs on a SUSE Linux 9.0 system, AMS Designer has a run-time dependency on a particular version of the ELF libs (`libelf.so.1`). The version of `libelf.so` in a typical SUSE Linux 9.0 installation differs from a typical Red Hat Linux installation. Due to this incompatibility in the versions of the ELF libs, some test cases fail to run on the SUSE Linux machine.

Solution: When running on a SUSE Linux machine, add *your_install_dir*`/tools/lib/SuSE` to your `LD_LIBRARY_PATH`. For example:

```
setenv LD_LIBRARY_PATH $AMSHOME/tools/lib/SuSE:...
```

Planned Release: Not currently planned.

CCR 303934: AMS Designer does not support hierarchical node names

OS: ALL **Version:** ALL

Description: AMS Designer running with the Spectre solver cannot handle hierarchical node names. For example:

```
module top(); TB_amp_test uut ();
Vsin_source Vin (top.uut.vin); \<-- Cannot use hierarchical node name
vsource #(.dc(5.0)) Vdd (cds_globals.\vdd! ,cds_globals.gnd );
```

```
vsource #(.dc(-5.0)) Vss (cds_globals.\vss! ,cds_globals.gnd ); endmodule
```

```
subckt Vsin_source (a)V1 (a 0) vsource dc=1 mag=1 type=sine sinedc=0 ampl=50m freq=1Mends
Vsin_source
```

For this kind of usage, ncelab issues an error message such as the following:

```
Vsin_source Vin (top.uut.vin);
|
ncelab: *E,CUILDP (./top.v,6|28): defparam is not allowed on parameters of
analog primitives.
```

Solution: Do the following:

    a. In your `top.v` module, add code like this:

```
`ifdef ams_mode
Vsin_source
Vin (cds_globals.net1);
`else Vsin_source
Vin (top.uut.vin);
`endif
```

    b. Add a declaration of `net1` in the `cds_globals` module.

```
electrical net1;
```

    c. Add a global statement in the SPICE netlist.

```
.global net1
```

    d. Add a `V0` vsource in the analog control file.

```
simulator lang=spice
V0 net1 top.uut.vin vsource dc=0
```

    e. Add the `-define ams_mode` option in the `ncvlog` command.

Planned Release: Not currently planned.

CCR 144885: Incomplete support for the digital variable in I/O statements

OS: ALL **Version:** ALL

Description: When you use an I/O statement such as `$display`, `$write`, `$fdisplay`, or `$fwrite`, to print a digital variable that:

    ○ contains bits of `x` or `z`, and

○ is used in the analog block,

the simulation fails. For example:

```
module top;
wire control;
assign control = 1''bz;

analog $display( "control = %d\n", control );
endmodule
```

In this example, the simulation fails because the digital variable `control` contains bit `z`.

Solution: Print the digital variable in the digital context.

Planned Release: Not currently planned.

CCR 98772: SST2 interface error in restarting a snapshot when debugging analog HDL code

OS: ALL **Version:** ALL

Description: When the following two conditions are true, restarting snapshot results in an SST2 interface error message:

○ You are using an SST2 database opened either from within the analog simulation control file or by a TCL database or probe command, and

○ The simulation is being controlled from within the analog debugger.

Solution: If the simulation is running within an analog interactive debug session or stopped at an analog breakpoint, use the `run -clean` command before restarting.

Here is an example:

```
ncsim>run [-phase|-next|-step]
ncsim>run -clean
ncsim>restart state1
```

Planned Release: Not currently planned.

CCR 67622: AMS Designer does not support checklimit analysis

OS: ALL **Version:** ALL

Description: The checklimit analysis, as supported by Spectre beginning with the 5.0.33 release is not supported by AMS Designer.

Solution: None.

Planned Release: Not currently planned.

CCR 43793: The run -timepoint command leaves a waveform gap between last 2 solutions

OS: ALL **Version:** ALL

Description: The Tcl command `run -timepoint` runs to the next absolute time point, which might require processing by either the analog or digital solver. When that time point is processed by the analog solver, the `run -timepoint` command does not update the database used to display waveforms. As a result, the time displayed by the Tcl `time` command does not always agree with the final time shown for the waveform.

Solution: Use the `run -clean` command to finish the processing for the time point and to write the results to the waveform database.

Planned Release: Not currently planned.

CCR 31724: SST2 file created from analog control file does not keep index for analog bus

OS: ALL **Version:** ALL

Description: If your design contains an analog bus and the waveform is saved in the SST2 format by specifying the format (`rawfmt=sst2`) in an analog simulation control (`.scs`) file, the individual bits of the bus do not show a bit index.

Solution: Probe the analog bus from the Tcl prompt to see the correct waveform.

Planned Release: Not currently planned.

CCR 13907: Auto-inserted connect modules not viewable in SimVision

OS: ALL **Version:** ALL

Description: Currently auto-inserted connect modules cannot be stepped into or probed. You can access the values on both ports but nothing inside of the connect module.

Solution: If you need visibility into connect module for debugging, manually insert the connect module into the design. Then, you have full use of the debug capabilities provided by Tcl commands and SimVision. After debugging your design, you can restore the automatically-inserted connect modules.

Planned Release: Not currently planned.

Product Level 2: AMSVF

CCR 65445: Mixed-signal hierarchies beneath instance arrays are not supported

OS: ALL **Version:** ALL

Description: AMS Designer supports only pure digital hierarchies for instance arrays. As a result, the following limitations apply:

- If Verilog-AMS or VHDL-AMS content is found inside instance array hierarchies, an error

is generated.

- When an analog node is declared and connected to an instance array, an error is generated.

- Dynamic parameter declarations inside hierarchies beneath instance arrays are not supported.

- If connection modules are manually inserted as instance arrays, the elaborator generates an error.

- Inherited connection attributes declared inside hierarchies beneath instance arrays are not supported.

- Analog primitives cannot be instantiated as arrays.

- If a wire attached to an instance array has an OOMR analog node declaration, the elaborator generates an error.

Solution: None.

Planned Release: Not currently planned.

Product Level 2: DMS_ELAB

AVSREQ-115742 Elaboration crash with SystemC with -disres detailed by default in some cases

OS: ALL **Version:** ALL

Description: Elaboration crashes sometimes when `-disres detailed` option is specified with AMS+SystemC designs.

Solution: Add the `-dms_perf` option to resolve the crash with AMS-SystemC interactions in that discipline resolution mode.

Planned Release: Not currently planned.

AVSREQ-109778 xmelab: *F,INTERR:::: part-select of concatenation expression is passed to VHDL entity with <+force_ms>

OS: ALL **Version:** ALL

Description: Tool crashes during elaboration when a design having part-select of concatenation expression is passed to VHDL entity using the `-force_ms` option.

Solution: Currently there is no workaround. Specifying bit/part/ipart select of concatenation expression is not supported in mixed signal designs.

Planned Release: Not currently planned.

Product Level 2: ANALOG_ELAB

CCR 910511: Parameter Expressions used in array declaration cause elaboration error

OS: LINUX **Version:** 4.0_X86_64

Description: The elaborator issues an error when you use parameter expressions instead of constant value inside array declaration. Below is a simple example where parameter `ANASWEN_MUX_WIDTH` is used in an expression in the array declaration of `ipt_anaswen_demux`.

```
parameter ANASWEN_MUX_WIDTH = 3; output [(2**ANASWEN_MUX_WIDTH)-1:0] ipt_anaswen_demux;
```

Solution: To avoid the elaboration error, use const value inside array declaration. For example, to avoid the elaboration error in the above example, evaluate the parameter expression before the array declaration and assign the evaluated value in the array, as shown below.

```
parameter ANASWEN_MUX_WIDTH = 3; Parameter BUS_WIDTH = (2**ANASWEN_MUX_WIDTH)-1; output
[BUS_WIDTH :0] ipt_anaswen_demux;
```

Planned Release: Not currently planned.

CCR 560104: ncelab internal error (Failed to open Spectre library) on Linux platforms

OS: LINUX **Version:** 4.0_X86_64

Description: If you are running the AMS Designer simulator on Linux using the three-step method (`ncvlog`, `ncelab`, `ncsim`), and you do not specify the `lib` directory correctly (and first) in the `LD_LIBRARY_PATH` variable, an error such as the following appears during elaboration:

```
ncelab: *N,SFEDPL: Deploying new SFE in analog engine.
ncelab: *F,INTERR: INTERNAL ERROR
```

This problem does not occur if you are running `irun` or running the AMS Designer simulator from the AMS Designer environment.

Solution: Add the `tools/lib` location at the beginning of your `LD_LIBRARY_PATH` setting, before any other library locations. If you are using the 64-bit version of the software, add the `tools/lib/64bit` location first.

Planned Release: Not currently planned.

CCR 396225: AMS Designer simulator does not support using an OOMR for passed_mfactor value

OS: ALL **Version:** ALL

Description: The elaborator fails if you use an out-of-module reference (OOMR) as the value of `passed_mfactor`. For example, you cannot use a statement such as the following because `cds_globals.r` is an OOMR.

```
child #(.m(cds_globals.r)) (* integer passed_mfactor = "m"; *) c1();
```

Solution: Pass `passed_mfactor` values directly instead of using OOMRs.

Planned Release: Not currently planned.

CCR 26067: Declaring global aliases makes ncelab fail

OS: ALL **Version:** ALL

Description: When there are aliases defined in a design (which instantiates `cds_alias` from `basic`) the elaboration fails with a message like the following:

```
ncelab: *E,DLPAKW: Attempt to write module basic.cds_alias:functional (SAM)
<0x00000001> into a read-only library.Error found by spectre.

   Error: Unable to instantiate master "basic:cds_alias.functional" as
"cds_globals.ams_alias_inst_1"
ncelab: *E,DLPAKW: Attempt to write module basic.cds_alias:functional (SDB)
into a read-only library.
ncelab: *F,SSIGF: Spectre Simulation Image generation failed!.
```

Solution: Set TMP directory in the `cds.lib` file and, in the command line, run `ncvlog` to compile `basic:cds_alias.functional` (`verilog.v`) into the TMP directory. For example, add the following lines to your `cds.lib` file:

```
DEFINE basic $CDSHOME/tools/dfII/etc/cdslib/basic
ASSIGN basic TMP ./basic_local
```

Then run the `ncvlog` command as follows:

```
ncvlog -use5x -ams
$CDSHOME/tools/dfII/etc/cdslib/basic/cds_alias/functional/verilog.v -work basic
```

Planned Release: Not currently planned.

CCR 8473: Analog functions cannot call another function if it is forward declared

OS: SUN4U ALL **Version:** NONE

Description: Analog user-defined functions fail elaboration if they call other analog functions that are not defined prior to their use (call).

An example of this situation is:
```
analog
```

```
begin
 V(n2) <+ maxVal(4.0, 5.0);
end
```

```
analog function real maxVal;
 input n1, n2;
 real n1, n2;
 real g;
 begin
  g = (n1 > n2) ? n1 : n2;
  maxVal = add5(g);
 end
endfunction
```

```
analog function real add5;
 input a;
 real a;
 begin
  add5 = a + 5;
 end
endfunction
```

The above fragment fails during elaboration with the following error:

```
maxVal = add5(g);
|
ncelab: *E,SYERROR: Unknown user defined function
```

Solution: Ensure that analog user-defined functions are defined prior to their use in another analog function.

Planned Release: Not currently planned.

Product Level 2: Auto-Incremental Elaboration with RNM

CCR 02011260: Auto-MSIE partition file is generated even when the simulation has TYCMPAT elab error

OS: ALL **Version:** ALL

Description: In some scenarios, the tool performs auto-partitioning of designs and generates an invalid partition file, even when a TYCMPAT elab error is issued.

This issue is related to part select of UDN array, which leads to mismatched size connection. This has been enabled in monolithic flow; however, not yet in the incremental elaboration flow.

Solution: None

Planned Release: Not currently planned.

Product Level 2: CONNECT_MOD

CCR 972832: Incorrect `timescale value causes unexpected 'x' state on the logic side of the E2L connect module.

OS: LINUX **Version:** RHEL5.0_64

Description: The `` `timescale `` value (1ns/100ps) is hardcoded in the E2L connect module. When you specify the tr/tf values as less than 12.5ps, an unexpected x state is added to the rising/falling edge of the logic side of E2L. The x state leads to wrong functions in the subsequent logic, and is hard to debug. The root cause of this condition is that the second precision `` `timescale `` value (100ps) exceeds eight times the specified `` tr/tf `` value, which does not conform to the algorithm in E2L conversion.

Solution: To work around this issue, you can modify the E2L file and include it in the `irun` command to replace the built-in E2L file, or use the following `ncelab`/`irun` options:

- ncelab -timescale 1ns/10ps -OVERRIDE_Precision
- irun -timescale 1ns/10ps -OVERRIDE_Precision

Planned Release: Not currently planned.

Product Level 2: INTERACTIVE

CCR 1062751: Drivers for Wreal and/or SVDC Net Types cannot be traced

OS: LINUX **Version:** ALL

Description: The SimVision T*race Driver in side bar* feature erroneously reports `No Drivers Available` for WREAL and SVDC net types.

Solution: As a workaround, use the Tcl `drivers` command to report the drivers for WREAL and/or SVDC net types.

Planned Release: Not currently planned.

CCR 8130: Problems when evaluating integer analog array objects

OS: ALL **Version:** NONE

Description: When evaluating the value of integer analog arrays, several formatting and

valuation problems exist.

Solution: To ensure that you see the correct and complete values of integer analog arrays, use the `%d` formatting option for these objects.

Planned Release: Not currently planned.

Product Level 2: NCELAB

CCR 212139: Supply-sensitive connect module does not work with top digital test bench

OS: ALL **Version:** ALL

Description: When you have a behavioral test bench driving an analog or SPICE block at the top level, automatically inserted connect modules (AICMs) used between the block and the test bench do not inherit the supply sensitivity value from the digital test bench.

Solution: Create a dummy top level and make sure the supply-sensitive AICMs are all one level below the top level.

Planned Release: Not currently planned.

CCR 152870: AMS supply sensitivity attributes in IEEE 1364-2001 format are ignored

OS: ALL **Version:** ALL

Description: AMS Designer supply sensitivity attributes in IEEE 1364-2001 format are ignored by the simulation flow. Attributes in this form are unsupported.

Solution: Use the IEEE 1364-1995 format to write AMS Designer supply sensitivity attributes.

Planned Release: Not currently planned.

CCR 115386: Supply/ground sensitivity does not work in default discipline resolution mode

OS: ALL **Version:** ALL

Description: The `ncelab` tool does not support supply and ground sensitivity attributes in the default discipline resolution mode. As a result, analog nodes are left floating (and grounded) leading to incorrect simulation results.

The supply and ground sensitivity attributes *are* supported in the detailed discipline resolution mode.

Solution: Use the `-detailed` discipline resolution option to the `ncelab` command instead of the `-default` option.

Planned Release: Not currently planned.

CCR 68807: Error when more than two disciplines are used in a connectrule statement

OS: ALL **Version:** ALL

Description: If the connectrule statement includes three or more disciplines, the elaborator generates an error when you attempt to use the connectrule to resolve only two disciplines.

For example, you have the connectrule:

```
connect electrical, magnetic, thermal resolveto magnetic;
```

and you have the following instantiation statements:

```
vams_a  aa1 (net1); // has electrical portvams_b  bb1 (net1); // has magnetic port
```

The elaborator generates an error if you try to resolve these two ports (an electrical one and a magnetic one) to magnetic, using a connectrule that includes three disciplines.

Solution: To resolve ports that are of only two different disciplines, be sure that the connectrule to be used has only a pair of disciplines. For the example above, you can rewrite the connectrule as:

```
connect electrical, magnetic resolveto magnetic;
```

If you need to resolve ports of more than two different disciplines, you can continue to use a connectrule that includes more than two disciplines.

Planned Release: Not currently planned.

CCR 19328: Hypotenuse function with param argument does not parse in AMS

OS: ALL **Version:** ALL

Description: The hypotenuse function does not work in AMS Designer if at least one of the arguments is a parameter.

Solution: Use the full equation, with the `sqrt` and `**2` functions.

Planned Release: Not currently planned.

Product Level 2: NCSIM

CCR 1079842: Simvision does not display interface elements during live simulation

OS: ALL **Version**: ALL

Description: If you use the ncsim/irun `-gui` option or the ADE debugging mode, interface elements are not always displayed as marching waveforms during live simulation.

Solution: You can verify the interface elements during post-processing.

CCR 648450: AMS Designer does not support wreal array assignments

OS: ALL **Version:** ALL

Description: AMS Designer does not support wreal array assignments. For example,

```
module mid(p,r);
  output wreal r [1:0][1:0];
  input wreal p [1:0][1:0];

  assign r=p;
  // The following is working fine:
  // assign r[0][0]=p[0][0];
  // assign r[0][1]=p[0][1];
  // assign r[1][0]=p[1][0];
  // assign r[1][1]=p[1][1];

endmodule
```

Solution: Wreal array support is beyond the Verilog-AMS LRM requirement. Cadence extends the support of wreal array (among other extensions) to benefit wreal customers. In earlier releases, wreal array assignment was not supported, and the workaround was to assign bit by bit, that is, `wreal_a[1]=wreal_b[1]`, which was time-consuming if the array had a big dimension. In this release, you can perform wreal array assignment in a more convenient way through a predefined macro as follows:

- In the Verilog-AMS model file, define a macro with pre-compiler directive, as follows:

  'define ASSIGN_ARRAY(a,b,c) genvar i; generate for (i=0;i<c;i=i+1) assign a[i]=b[i];
  endgenerate

- Within the model, call the macro as follows:

  'ASSIGN_ARRAY(myDes, myAssign, 5)

  > ⚠ Note: `myAssign` and `myDes` are 5-element arrays where `myDes<=myAssign`. There is no ";" at the end of the line, since it just calls the macro.

CCR 548909: digital signal cannot be plotted with simvision after ams simulation killed in SGE

OS: LINUX **Version:** EE3.0

Description: It occurs in a certain situation. The `ncsim` saves the digital waveform to database only when the memory is full. When the simulation is killed using SIGKILL(-9) in SGE AND the

waveform memory is not full, the digital signal will not be saved properly.

Solution: There is a SGE setting workaround for this problem:

By default, the `qdel` command gives the SIGKILL(-9) signal, but you can change it to SIGTERM, which can terminate the simulator in a normal way using next method:

Edit queue files in next directory:

```
$SGE_ROOT/$SGE_CELL/spool/qmaster/cqueues/
```

Before the change:

```
terminate_method none
```

After the change:

```
terminate_method SIGTERM
```

Re-invoke the SGE deamon and run the simulation from ADE selecting the queue you have changed. `qdel` the simulation now and the result waveform data is kept well and can be plotted without problem.

You will get DP log inform as next:

```
> -------------------------------------------
> Job 658 (cmdLineRunDistrib) Complete
> User             = yanyan
> Queue            = cdsj139@cdsj139.Cadence.COM
>  Host             = cdsj139.Cadence.COM
>  Start Time       = 05/21/2008 07:20:06
>  End Time         = 05/21/2008 07:20:42
> User Time        = 00:00:30
>  System Time      = 00:00:03
>  Wallclock Time   = 00:00:36
>  CPU              = 00:00:33
>  Max vmem         = 333.016M
>  Exit Status      = 0
> -------------------------------------------
```

Planned Release: Not currently planned.

CCR 222957: Unprobed bits of analog bus also show non-empty waveforms in amsfastspice mode

OS: ALL **Version:** ALL

Description: When you probe an individual bit of an analog bus, all the bits of that bus show up with non-empty waveforms. For example, you try to probe just bit `vd[1]` with the following commands,

```
probe -shm top.IdealDac.vd[1]probe -shm -flow top.IdealDac.vd[1]
```

where `vd` is an 8-bit analog bus.

After the simulation, you find that the SST2 waveform database for these Tcl commands contains waveforms for all the bits of the bus `vd`.

Solution: None.

Planned Release: Not currently planned.

CCR 93385: Mixed-case library name must be escaped when used in MAPN2D specification

OS: ALL **Version:** ALL

Description: If you want to use a `MAPN2D` specification for a VHDL-AMS nature defined in a library whose name is a mixed-case identifier, you must escape the library name in the `MAPN2D` specification.

Example:

```
MAPN2D amsPLL.std_decls.electrical electrical -- INCORRECT
MAPN2D \amsPLL\.std_decls.electrical electrical -- CORRECT
```

Solution: Always escape mixed-case library names that are used in `MAPN2D` specifications.

Planned Release: Not currently planned.

CCR 7827: Tcl drivers command omits auto-inserted connect modules

OS: ALL **Version:** NONE

Description: When the Tcl `drivers` command is applied to a mixed-net and an automatically-inserted connect module is driving that net in the design, the connect module is not included in the `drivers` command output listing.

Solution: You can list all the connect modules in a particular scope of the design with the `scope` command (see `help`). In this way, you can determine if a problematic mixed-signal net has such a hidden driver.

By editing your design, you can also replace automatically inserted connect modules with identical manually inserted connect modules. Then you have full use of the debug capabilities provided by Tcl commands and SimVision. After debugging your design, you can restore the automatically inserted connect modules.

Planned Release: Not currently planned.

Product Level 2: NCVHDL

CCR 40597: Restrictions to the simultaneous IF statement

OS: ALL **Version:** ALL

Description: The `IF` statement must be balanced. Every `IF` statement must contain an `else` clause. Any free or interface quantity of mode out must be referenced in a simultaneous statement.

Solution: Support for the simultaneous `if` statement is limited so that the `else` clause, which according to the standard is optional, is required for the model to successfully pass the solvability balance check.

Example:
The following code snippet while LRM compliant fails in the parser:

```
FAILS:if (vd > −5.0) use
q1 == 5.0;
elsif (vd <= −5.0) use
q1 == 6.0;
end use;
```

It needs to be re-written like this to pass through:

```
PASSES:if (vd > −5.0) use
q1 == 5.0;
else
q1 == 6.0;
end use;
```

A modeling constraint is also placed such that the `If` statement has to be balanced. In other words, the number of simultaneous statements in the `if` and `else` blocks must be equal.

For example:

```
PASSES:if (vd > 6.0) use
q1 == 6.0;
q2 == -6.0;
elsif (vd > 0.0) use
q1 == vd;
q2 == -vd;
else
q1 == 0.0;
q2 == 0.0;
end use;
FAILS:if (vd > 6.0) use
q1 == 6.0;
q2 == -6.0;
elsif (vd > 0.0) use
q1 == vd;
q2 == -vd;
else
q1 == 0.0; -- this path has different number of expressions
end use;
```

A dependency check is also performed to ensure that any free or interface quantity of mode out is referenced in a simultaneous statement.

Example (assume the quantities `q1`, `q2` and `q3` are not referenced in any other simultaneous statements outside the block below). This example passes the balance check but fails the dependency check.

```
FAILS_2:if condition_1 use
if condition_2 use
q1 == 0.0;
else
q1 == 1.0;
end use;
q2 == 2.0; --q3 is not referenced in the design.
else
q1 == 3.0;
q3 == 4.0; --q2 is not referenced in the design.
end use;
PASSES:if condition_1 use
if condition_2 use
q1 == 0.0;
else
q1 == 1.0;
end use;
q2 == 2.0;
q3 == 5.0;
else
q1 == 3.0;
q2 == 5.0;
q3 == 6.0;
end use;
```

Planned Release: Not currently planned.

Product Level 2: NCVLOG

CCR 73352: Digital signals not detected in @cross expression

OS: ALL **Version:** ALL

Description: Using digital signals in the `@cross` expression can slow down simulation because, effectively, the digital signal does not cross the 0.0 threshold. Although the *Language Reference Manual* does not declare this usage to be illegal, Cadence recommends that you avoid using digital signals in this way.

Solution: Use digital events such as `@posedge`, `@negedge`, or just `@`, to detect changes in digital signals. These events are supported in the analog context.

Planned Release: Not currently planned.

CCR 144136: Inherited connections that resolve to implicit nets cause an elaboration error

OS: ALL **Version:** ALL

Description: An inherited connection that resolves to an implicit net causes a `CUVHNF` error during elaboration.

During inherited connection processing, the elaborator searches in the parent hierarchy for the target net. Because the net is implicit, it is not found. As a result, the elaborator is unable to establish the connection and issues an error.

Solution: Explicitly declare all nets that are used as inherited connections. One way to do this is to declare the target inherited connection as a wire within the parent hierarchy.

Planned Release: Not currently planned.

Product Level 2: OUTPUT

CCR 938845: Analog signals or vectors are not saved by default in the AIUM flow

OS: ALL **Version:** ALL

Description: In AMS-Spectre or AMS-APS, when you save or probe analog signals or vectors using the AIUM flow (Verilog-Spice or VHDL-Spice), these vectors are not saved.

Solution: You can work around this problem by using the following two methods:

    a. Add `save=selected` to the `tran` command card or statement, as follows:

       Spice format: `.tran 1ns 10ns save=selected .probe v(*) depth=3`

Spectre format: `simulator lang=spectre tran1 tran stop=10ns save * depth=3`

b. Use the Spectre option `save=selected`, as follows:

`simulator lang=spectre myopt options save=selected`

Planned Release: Not currently planned.

CCR 898494: Run multiple simulations from the same directory

OS: ALL **Version:** ALL

Description: When you run multiple simulations on the same case from the same directory, the following two important options are used:

- **`-nclibdirname`**: All intermediate outputs for digital and mixed-signal (The generic irun `INCA_lib` output, AIUM internal material, like skeleton, portmap file, and so on.)

- **`-outdir`**: All analog solver outputs.

However, the location of the final waveform database is determined by the `database -into` command in Tcl file, and not the `-outdir` command.

Solution: To work around this problem, set the waveform location in the `database -into` command in TCL file the same as the value of the irun option of the `-outdir` command.

Planned Release: Not currently planned.

CCR 8002: Long term: port probe problem in hierarchy

OS: ALL **Version:** NONE

Description: Port probes do not consider current contributions of instantiated components inside of a hierarchical design. As a result, the accumulated value of a port probe does not reflect the complete current through the port.

Solution: Manually (explicitly) create a port probe in the module by introducing an internal node. The internal node should be connected to the port using a zero-volts source. All references to the port in the module should be replaced by a reference to the internal node. Then the port probe can be created by probing between the port and the internal node.

For example, rewrite;

```
module test(a,b);
inout a,b;
electrical a,b, gnd;
ground gnd;
real r1, r2;

resistor #(.r(10)) R3 (a, gnd);

analog begin
    r1 = I(<a>);
    I(a,b)  <+ V(a,b)/10;
    I(b,gnd) <+ V(b,gnd)/10;
    $display(" I(<a>) = %g \n", r1);
end

endmodule
```

as:

```
module test(a,b);
inout a,b;
electrical a,b, gnd;
ground gnd;
real r1, r2;

electrical a2;
resistor #(.r(10)) R3 (a2, gnd);

analog begin
    V(a,a2)  <+ 0;
    r1 = I(a,a2);
    I(a2,b)  <+ V(a2,b)/10;
    I(b,gnd) <+ V(b,gnd)/10;
    $display(" I(<a>) = %g \n", r1);
end
endmodule
```

Planned Release: Not currently planned.

Product Level 2: SAVE-RESTART

CCR 1071048: The SystemC-AMS SaveRestart feature does not work on SLES11

OS: LINUX **Version: SLES11_64**

Description: If you try to perform save & restart on a SystemC-AMS design that uses both SystemC and AMS languages on SLES11, AMS may crash when restarting the simulation.

Solution: Use this feature only on platforms other than SLES11.

Planned Release: Not currently planned.

Product Level 2: SIMVISIONMS

AVSREQ-138349: No highlight on port that is also a conversion point

OS: AIX **Version:** ALL

Description: A ports that are also a conversion point is not highlighted in the Browse Currents sidebar.

Solution: None.

Planned Release: Not currently planned.

AVSREQ-133883: No conversion point annotation on the low power mixed-signal boundary where ISO is inserted

OS: AIX **Version:** ALL

Description: Low power circuitry is constructed during elaboration based on the UPF/CPF specification. For the case where the connectivity of this circuit is a mixed net and this net connects to a low power isolation elements, connections to these isolation elements will not be present the mixed-net database.

Solution: None.

Planned Release: Not currently planned.

AVSREQ-133431: Incorrect connections in SimVision for electrical signal connected to EEnet/UDN multi-field signals

OS: AIX **Version:** ALL

Description: Incorrect connections may be shown in SimVision Schematic Tracer in cases where the top electrical bus connects to lower level EEnet signals.

Solution: None.

Planned Release: Not currently planned.

AVSREQ-131964: No conversion point annotation in SPICE_on_Top case connections

OS: AIX **Version:** ALL

Description: For SPICE-on-Top configurations, wrappers are automatically created to establish connectivity of the design. If this connectivity is a mixed net, the extraction of the mixed-net data may be incomplete. This would be notable in missing hierarchical connections and Prim connections for that mixed net.

Solution: None.

Planned Release: Not currently planned.

AVSREQ-131050: No conversion point annotation on inherited connections

OS: AIX **Version:** ALL

Description: The conversion points on the inherited connection do not get annotated on the schematic.

Solution: None.

Planned Release: Not currently planned.

AVSREQ-126977: SimVision Schematic Tracer shows only one highlighted conversion point during IE optimization for SPICE-logic-SPICE scenario

OS: AIX **Version:** ALL

Description: When an IE is highlighted in the Mixed Net Browser and the net is a B2B net, where it is electrical-logic-electrical scenario and IE optimization replaced the E2L+L2E by a bidirectional pin, then the bidirectional pin is displayed only in one of the ports.

Solution: None.

Planned Release: Not currently planned.

AVSREQ-125128: NON-SIE mode is not supported

OS: AIX **Version:** ALL

Description: Hierarchical connections are not listed in the `mxnet.dump` file for E2L connect module connections to wire with non-AMS-SIE mode connect modules.

Solution: `-amsie` is the default simulation option. When using a non-SIE mode, remove the `-disable_amssie` option.

Planned Release: Not currently planned.

AVSREQ-123900: No conversion point annotation of VHDL module

OS: AIX **Version:** ALL

Description: Mixed Net abstraction is rooted in Verilog/Verilog-AMS scope where AICM instances are inserted. Connections from a Mixed Net to VHDL/VHDL-AMS are not considered during mixed net abstraction. These boundaries are not part of the mixed net database.

Solution: None.

Planned Release: Not currently planned.

CCR 2333834: Contents of DSPF do not show when schematic is replaced with DSPF

OS: AIX **Version:** ALL

Description: Cell defined in `netlist.vams` gets replaced with the cell defined in the DSPF file by `dspf_include`.

Solution: None.

Planned Release: Not currently planned.

CCR 2333017: "inv" keyword is mapped to a symbol in Schematic Tracer, but other names are not

OS: AIX **Version:** ALL

Description: A cell named "inv" will map to an inverter symbol, but "inv_2V" does not, even if it is put in the mapping file.

Solution: None.

Planned Release: Not currently planned.

CCR 2325496: Post-layout analog circuit is not supported in Schematic Tracer

OS: AIX **Version:** ALL

Description: Post-layout analog circuit from a DSPF file or extracted view is not supported well as large number of parasitic devices may cause performance issues. Meanwhile, large number of R/C will be difficult to view in Schematic Tracer.

Solution: None.

Planned Release: Not currently planned.

CCR 2311979: Check-point based save/restart is not supported

OS: AIX **Version:** ALL

Description: Save and restart based on check-point is not supported with SimVision MS.

Solution: Use process-based save/restart, add the `-process_save` option in xrun.

Planned Release: Not currently planned.

CCR 2257182: Encrypted modules do not show connectivity and do not open in Source Browser

OS: AIX **Version:** ALL

Description: In Schematic Tracer, encrypted modules are drawn as a block without connectivity. Source files of such modules will not open in Source Browser.

Solution: None.

Planned Release: Not currently planned.

CCR 2198299: Verilog-AMS use model and behavior in SimVision MS

OS: AIX **Version:** ALL

Description: Verilog-AMS from `ahdl_include` is not supported in SimVision MS.

Solution: None.

Planned Release: Not currently planned.

CCR 2195179: Source Browser viewing issues with MTS subcircuit

OS: AIX **Version:** ALL

Description: A scoped subcircuit definition may not be correctly identified in a MTS application.

Solution: None.

Planned Release: Not currently planned.

CCR 2195168: analogLib mutual inductor cannot be plotted in Schematic Tracer

OS: AIX **Version:** ALL

Description: Mutual inductor in the GUI is a symbol that indicates the relation between two inductors. Currently, in SimVision MS, there is no mechanism to have a device, such as a mutual inductor, that represents relationship rather than connection.

Solution: None.

Planned Release: Not currently planned.

Product Level 2: SPECTRE

CCR 1072379: Linter message tags do not work on ibmrs platform

OS: AIX **Version:** ALL

Description: AMS checks for static and dynamic linter issues when the `-spectre_args -ahdllint` option is used. When issues are encountered, linter gives the warning as below.

```
WARNING (AHDLLINT-5008): "test.va", line 139: Detected discrete expression on the
right side of a contribution statement. It is recommended that you apply the
transition function on discrete values by specifying the transition rise and fall
time when the logic or discrete expression value changes.
```

In the ibmrs platform, the warning is stil issued but the reference tag is missing as below:

```
"test.va", line 139: Detected discrete expression on the right side of a
con  tribution statement. It is recommended that you apply the transition function
on   discrete values by specifying the transition rise and fall time when the
logic   or discrete expression value changes.
```

This may hinder extracting further info about the warning using ahdlhelp or to track the issue when `-ahdllint=error` is used.

Solution: Use non-ibmrs platforms.

Planned Release: Not currently planned.

CCR 870372: tclspice probing does not work in ibmrs platform

OS: ALL **Version:** ALL

Description: The tclspice probing feature is not turned on in the AIX platform.

Solution: Use other platforms for this feature.

Planned Release: Not currently planned.

CCR 836468: Multithreading not enabled in AMS Designer on AIX platform

OS: ALL **Version:** ALL

Description: Starting with MMSIM10.1, multithreading is enabled with the Spectre and APS solvers on AIX platform. However, multithreading remains disabled in AMS Designer with Spectre or APS solver on AIX platform.

Solution: None.

Planned Release: Not currently planned.

CCR 523791: Default minimum time step for the analog solver causes AMS-Spectre to hang

OS: ALL **Version:** ALL

Description: In very rare customer test cases, the AMS Designer simulator with the Spectre solver hangs when using the default minimum time step of the Spectre analog solver. While the default minimum time step of the analog solver typically yields accurate results, the default minimum time step can lead to a quantity blow-up or convergence issue for some designs that feature digital-to-analog events such as Verilog-AMS `logic`-to-`electrical` conversions or VHDL-AMS `break` statements. On occasion, the simulation might just hang.

For example, consider a typical VHDL-AMS design that has a stop time of 1.2 ms, a liberal mode maxstep of 120 us, and 16 time steps during simulation without `break` statements. If you add `break` statements, the simulation has 28 time steps, which amounts to a minimum time step that is 12 orders of magnitude less than the previous setup without the `break` statements. In this way, the simulation time can increase significantly.

Solution: Use the `d2aminstep` option on the `tran` statement to define a different minimum time step for the Spectre analog solver. For example, the following statement (in an analog control file) demonstrates how you might define a `d2aminstep` (minimum time step) of 1e-12 for AMS-Spectre simulation of a 1Ghz design:

```
amsAnalysis tran stop=100u d2aminstep=1e-12
```

Usually a larger `d2aminstep` value can speed up the simulation as well as prevent the simulator from hanging. It can also prevent non convergence during tran analysis. However, it must not be too large to cause missing signal transition. Tune the option to make sure there is no `d2aminstep` warning message in the simulation log.

Planned Release: Not currently planned.

CCR 446913: Wrong analog/digital signal transitions during transient analysis using skipdc

OS: LINUX **Version:** RHEL4.0_32

Description: Using the AMS Designer simulator with the Spectre solver, you should not set the `skipdc` transient analysis option to anything other than `no` as doing so can result in incorrect analog-to-digital signal transitions. The default value for the `skipdc` option is `no`. (You set transient analysis options using the `tran` statement in your analog simulation control file.) <no>If you used this option, a warning message appears in your simulation log file and you can search for the `AMSD` keyword to find the message.

Solution: None.

Planned Release: Not currently planned.

CCR 8448: @final_step does not always run

OS: ALL **Version:** NONE

Description: In the following simulation termination scenarios, `@final_step` does not run and the last analog solution is not always written to the database.

- The digital solver encounters `$finish()` in behavioral code.

- The analog solver is interactive (Tcl prompt) at some behavioral statement when the Tcl `finish` command is issued.

- The digital solver is interactive at some behavioral statement when the Tcl `finish` command is issued.

- The analog solver is interactive at a time advance when the Tcl `finish` command is issued.

- The digital solver is interactive at a time advance when the Tcl `finish` command is

issued.

Solution: None.

Planned Release: Not currently planned.

Product Level 2: VHDL_AMS

CCR 43803: Simultaneous case statement implementation constraints

OS: ALL **Version:** ALL

Description: The `case` statement must be balanced, so that the number of simultaneous statements in each case of the statement is the same. The simultaneous `case` statement must also pass the dependency check.

For information about the dependency check, refer to the entry for CCR 40597 ("Restrictions to the simultaneous IF statement") in this document.

Solution: None.

Planned Release: Not currently planned.

CCR 30746: Expressions and implicit quantities cannot be actuals in quantity port map

OS: ALL **Version:** ALL

Description: Only the following types of quantities can be used as actuals in a component port map (having quantity ports): across quantities, through quantities, and free quantities. This restriction means that you cannot use the following types of quantities in a quantity port map:

- Implicit quantities (quantity valued attributes such as `S''RAMP` or `Q''DOT`). As a result, statements like the following are not supported.

  ```
  i1: TEST_ENT1 PORT MAP(s3''RAMP(1.0/10.0, 1.0/20.0));
  ```

- Expressions (like 2.0, 1.5 * q3 where q3 is a quantity reference). As a result, statements like the following are not supported.

  ```
  i1: TEST_ENT1 PORT MAP(2.0 * q3);
  ```

Solution: Declare an additional free quantity and assign it to the unsupported type (the implicit quantity or expression) using a simple simultaneous statement. Use this new quantity in the quantity port map. For example, the unsupported statement

```
i1: TEST_ENT1 PORT MAP(s3''RAMP(1.0/10.0, 1.0/20.0));
```

can be recoded as

```
quantity q4 : real;
q4 == s3''RAMP(1.0/10.0, 1.0/20.0);
i1: TEST_ENT1 PORT MAP(q4);
```

Similarly, the unsupported statement

```
i1: TEST_ENT1 PORT MAP(2.0 * q3);
```

can be recoded as

```
quantity q4 : real;
q4 == 2.0 * q3;
i1: TEST_ENT1 PORT MAP(q4);
```

Be aware that quantity initialization is unsupported. This means that if you replace an expression with a free quantity, the free quantity might not initially have the same value as the expression it replaces.

Planned Release: Not currently planned.

CCR 29392: Incorrect initialization of Q''ABOVE(E) signal

OS: ALL **Version:** ALL

Description: The implicit signal `Q'ABOVE(E)` is incorrectly initialized to `FALSE` even when the quantity `Q` is assigned an initial value greater than the value of the expression `E`. Depending on how the implicit signal is used in the design, the incorrect initialization might or might not impact the simulation result.

Shown below are two examples. In the first, there is no impact on the simulation result; in the second, there is an impact.

    a. In this example, `q''above` is used in the analog context.

```
architecture TEST_ARCH of TEST_ENT is
    quantity q1 : real := 10.0;
    quantity q2 : real;
begin
    q1 == 1.0;
    if (q1''ABOVE(0.5)) use
        q2 == 1.0;
    else
        q2 == 2.0;
    end use;
end architecture TEST_ARCH;
```

    In the above example, the initial guess for `q1` is 10.0 and the DC value is 1.0. The

`q1''ABOVE(0.5)` is incorrectly initialized to `FALSE` but at DC it identifies the value to be `TRUE` (because `q1` is now 1.0) and correctly chooses the equation `q2 == 1.0`. So, in this example, the incorrect initial value of `q1''above(0.5)` has no impact on the simulation result.

b. In the next example, the incorrect `q1''above(0.5)` initialization causes unexpected behavior. In this architecture, `q''above` is used in the digital context in the sensitivity clause of the `process` statement.

```
architecture TEST_ARCH of TEST_ENT is
   quantity q1 : real := 1.0;
   begin
     q1 == 1.0;
     process(q1"above(0.5))
      begin
        report "When working correctly should print exactly once. " &
            "Currently q1"above(0.5) (=" &
            Boolean"IMAGE(q1"above(0.5)) &
            ") is true.";
        report " ";
      end process;
end architecture TEST_ARCH;
```

In the above example, `q1''above(0.5)` is incorrectly initialized to `FALSE`. So, during the first digital run, the report statement is executed and reports the value of `q1''above(0.5)` to be `FALSE`. However, during DC computation, `q1` is set to 1.0, thereby switching the value of `q1''above(0.5)` from `FALSE` to `TRUE`.

This causes the `process` statement to be executed one additional time. The incorrect `q1''above(0.5)` initialization causes the process block to be executed twice when only one execution is expected.

Solution: None.

Planned Release: Not currently planned.