WEIZHE **GAN**

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EDUCATION

2014 SEP – 2018 JUN (*EXPECTED*)

BACHELOR, ZHEJIANG UNIVERSITY

Major: Electronic Engineering
GPA: 3.92/5 (top 10)
Thesis: *FPGA-based Digital Integrated Experimental Platform Design*

PROJECT EXPERIENCE

2016 MAY – 2O17 MAY

SMART LAUNDRY: AUTO RETRACTABLE RACK ON INTEL MCS-51

- Designed and implemented a SMART retractable rack system, which could be controlled by: 1) SMS message, 2) Timer, or 3) Rain Sensor.
- Designed the hardware circuits and implementing on Printed Circuit Board.
- Programmed in C for main Control Logic and Communication among multi peripheral chips.

2017 JUL – 2017 AUG

SOKOBAN: A FPGA-BASED TRANSPORT PUZZLE GAME

- Led a 3 people team to design and implement a 4 Levels 8X8 Sokoban game on FPGA.
- Programmed in Verilog for game control and all SVGA (Super Video Graphic Array) signal processing and output.

2017 OCT – 2018 JAN

CRALLOGAG: A DSP-BASED REAL-TIME VOICE CHANGER

- Designed and implemented a Digital Signal Processing System that collects, stores, converts, and replays voice signals.
- Worked on CCS (Code Composer Studio) IDE with C language for the DSP chip programming and installation.

SKILLS

- Programming Languages: C, Verilog, MATLAB
- Language: English (CET-6, Proficiency Fluent)
- Operating System: Windows, Linux/Unix
- Knowledge: Data Structure, Algorithm, Computer Architecture

AWARDS AND HONORS

- Zhejiang University Third Prize Scholarship (2015-2017)
- Zhejiang University Student Research Training Program (SRTP)