```
kernel 3.18.7
/{
    model = "Pegmatite SoC";
    compatible = "marvell,pegmatite";
    interrupt-parent = <&gic>;
};
由于在root device node中指定了interrupt-parent property为gic,这样如果child device node中没有特别显式指定,那
么该device的interrupt都连接到gic。否则每个
device node中都要注明"interrupt-parent"是谁。
Granite2 and Gemstone有两大类interrupt controller.
    gic (one)
    gic: interrupt-controller@d1d01000 {
        compatible = "arm,cortex-a15-gic", "arm,cortex-a9-gic";
        #interrupt-cells = <3>;
        #address-cells = <0>;
        interrupt-controller;
        reg = <0 0xd1d01000 0 0x1000>,
            <0 0xd1d02000 0 0x100>;
    };
```

```
gic interrupt specifier的说明:
        #interrupt-cells = <3>;
比如
    uart0: uart@d4030000 {
        compatible = "mrvl,pxa-uart";
        reg = <0 0xd4030000 0 0x1000>;
        interrupts = <0 16 4>;
        clocks = <&uart0_clkgate>;
        status = "disabled";
#interrupt-cells = <3>;
使得of code (in drivers/of)能够正确地parse device node中的"interrupt" property。使用interrupt specifier来parse
"interrupt" property的code在
of_irq_parse_raw() function in drivers/of/irq.c.
但是of_irq_parse_raw()只是辨认出一个interrupt由多少数字表示,即0,16,4这3个数字表示一个gic上的interrupt,
但这3个数字的意义,它是不负责解释的(它也不知道意义)。
负责解释的是对应interrupt controller的irq domain.在这里就是gic的irq domain。
in drivers/irqchip.irq/gic.c
static struct gic_chip_data gic_data[MAX_GIC_NR] __read_mostly;
struct gic_chip_data用于描述 gic.
struct gic_chip_data {
    union gic_base dist_base;
```

```
union gic_base cpu_base;
#ifdef CONFIG CPU PM
    u32 saved_spi_enable[DIV_ROUND_UP(1020, 32)];
    u32 saved spi conf[DIV ROUND UP(1020, 16)];
    u32 saved_spi_target[DIV_ROUND_UP(1020, 4)];
    u32 percpu *saved ppi enable;
    u32 __percpu *saved_ppi_conf;
#endif
    struct irq_domain *domain;
    unsigned int gic_irqs;
#ifdef CONFIG_GIC_NON_BANKED
    void __iomem *(*get_base)(union gic_base *);
#endif
};
而irq domain中的irq_domain_ops中的xlate()负责解释这些数字的含义。
/**
* struct irq_domain_ops - Methods for irq_domain objects
* @match: Match an interrupt controller device node to a host, returns
      1 on a match
* @map: Create or update a mapping between a virtual irq number and a hw
     irg number. This is called only once for a given mapping.
* @unmap: Dispose of such a mapping
* @xlate: Given a device tree node and interrupt specifier, decode
      the hardware irq number and linux irq type value.
* Functions below are provided by the driver and called whenever a new mapping
* is created or an old mapping is disposed. The driver can then proceed to
```

```
* whatever internal data structures management is required. It also needs
* to setup the irq desc when returning from map().
*/
struct irq domain ops {
     int (*match)(struct irq_domain *d, struct device_node *node);
     int (*map)(struct irg domain *d, unsigned int virg, irg hw number t hw);
     void (*unmap)(struct irq_domain *d, unsigned int virq);
    int (*xlate)(struct irq_domain *d, struct device_node *node,
             const u32 *intspec, unsigned int intsize,
             unsigned long *out_hwirq, unsigned int *out_type);
};
static const struct irq_domain_ops gic_irq_domain_ops = {
     .map = gic_irq_domain_map,
     .unmap = gic_irq_domain_unmap,
     .xlate = gic_irq_domain_xlate,
};
static int gic_irq_domain_xlate(struct irq_domain *d,
                   struct device_node *controller,
                   const u32 *intspec, unsigned int intsize,
                   unsigned long *out_hwirq, unsigned int *out_type)
{
     unsigned long ret = 0;
     if (d->of_node != controller)
          return -EINVAL;
```

```
return -EINVAL;
    /* Get the interrupt number and add 16 to skip over SGIs */
    *out_hwirq = intspec[1] + 16;
                                                 1
    /* For SPIs, we need to add 16 more to get the GIC irq ID number */
    if (!intspec[0]) {
                                                         2
         ret = gic_routable_irq_domain_ops->xlate(d, controller,
                                 intspec,
                                 intsize,
                                 out_hwirq,
                                 out_type);
         if (IS_ERR_VALUE(ret))
             return ret;
    }
    *out_type = intspec[2] & IRQ_TYPE_SENSE_MASK;
                                                            3
    return ret;
3个数字intspec[0],intspec[1] and intspec[2]都得到解释。
G2使用的是gic-400,所有interrupt分为3类。
1.0-15, SGI
2.16-31, PPI
```

if (intsize < 3)

}

SGI + PPI产生的interrupt是由特定core服务的,而SPI则是由gic动态决定送往哪一个core.

同时SGI并不是由device触发的interrupt,它通过write GICD_SGIR register来trigger interrupt.

1

intspec[1] + 16就是gic的hardware interrupt number (引入irq domain后, kernel就只关心virtual interrupt number.而 hardware interrupt number到

virtual interrupt number的mapping则是irq_domain_ops struct中map() function的责任。virtual interrupt number实际上就是kernel维护interrupt handling

的核心数据结构struct irq_desc array的index.这里 + 16,是因为gic的前16个interrupts是留给SG的。

2

intspec[0]为0,表示该interrupt是SPI. SPI从32开始。

```
const struct irq_domain_ops *gic_routable_irq_domain_ops =
    &gic_default_routable_irq_domain_ops;
```

```
static const struct irq_domain_ops gic_default_routable_irq_domain_ops = {
    .map = gic_routable_irq_domain_map,
    .unmap = gic_routable_irq_domain_unmap,
    .xlate = gic_routable_irq_domain_xlate,
};
static int gic_routable_irq_domain_xlate(struct irq_domain *d,
                 struct device_node *controller,
                 const u32 *intspec, unsigned int intsize,
                 unsigned long *out_hwirq,
                 unsigned int *out_type)
{
    *out_hwirq += 16;
    return 0;
}
其实就是在原来①的基础上再加上16,就是原来值的基础上加了32.
3
intspec[2]是interrupt trigger type
in include/linux/irq.h
IRQ_TYPE_NONE
                              = 0x00000000,
IRQ_TYPE_EDGE_RISING
                            = 0x00000001,
IRQ_TYPE_EDGE_FALLING = 0x00000002,
IRQ_TYPE_EDGE_BOTH
                                 = (IRQ_TYPE_EDGE_FALLING | IRQ_TYPE_EDGE_RISING),
```

```
IRQ_TYPE_LEVEL_HIGH
                          = 0 \times 000000004,
IRQ_TYPE_LEVEL_LOW
                         = 0 \times 000000008,
IRQ_TYPE_LEVEL_MASK
                              = (IRQ_TYPE_LEVEL_LOW | IRQ_TYPE_LEVEL_HIGH),
IRQ TYPE SENSE MASK = 0x00000000f,
IRQ_TYPE_DEFAULT
                            = IRQ_TYPE_SENSE_MASK,
    uart0: uart@d4030000 {
        compatible = "mrvl,pxa-uart";
        reg = <0 0xd4030000 0 0x1000>;
        interrupts = <0 16 4>;
        clocks = <&uart0_clkgate>;
        status = "disabled";
这样可以解释uart0 device的interrupts property的含义了。
0 --- gic的SPI interrupt, 即还interrupt是属于Shared (SPI中"S"), 即uart0的interrupt将被某个ARM core服务, uart0并
不关心是哪个core运行的interrupt handler, core 0, core 1, core 2, core 3(Granite2有4 cores), 无所谓。
16 --- uart0在gic上的真正的interrupt number是16 + 32 = 48
4 --- IRQ_TYPE_LEVEL_HIGH,表高电平触发,即uart0 device的interrupt pin是高电平时就表示需要interrupt服务了。
2. gpio interrupt controller (eight)
    gpio0: gpio@d4019000 {
        compatible = "marvell,peg-gpio";
        #address-cells = <2>;
        #size-cells = <2>;
        reg = <0 0xd4019000 0 0x1000>;
        gpio-controller;
```

```
#gpio-cells = <2>;
interrupts = <0 36 4>, <0 119 4>, <0 120 4>, <0 121 4>, <0 122 4>, <0 123 4>, <0 221 4>, <0 222 4>;
interrupt-names = "gpio_mux";
interrupt-controller;
#interrupt-cells = <2>;
clocks = <&apbus_apb_clkgate>;
ranges;
gcb0: gpio@d4019000 {
    reg = <0 0xd4019000 0 0x4>;
};
gcb1: gpio@d4019100 {
    reg = <0 0xd4019100 0 0x4>;
};
gcb2: gpio@d4019200 {
    reg = <0 0xd4019200 0 0x4>;
};
gcb3: gpio@d4019300 {
    reg = <0 0xd4019300 0 0x4>;
};
gcb4: gpio@d4019400 {
    reg = <0 0xd4019400 0 0x4>;
};
gcb5: gpio@d4019500 {
```

```
reg = <0 0xd4019500 0 0x4>;
        };
        gcb6: gpio@d4019600 {
            reg = <0 0xd4019600 0 0x4>;
        };
        gcb7: gpio@d4019700 {
            reg = <0 0xd4019700 0 0x4>;
        };
    };
8个GPIO banks都是interrupt controller.它们级联在gic主controller上。
在gpio@d4019000 device node中,其有8个子设备(gcb0 to gcb7)。这8个device即是gpio-controller,又是interrupt-
controller。8个gpio bank的本生级联在gic上,
在gic对应的interrupt为interrupts = <0 36 4>, <0 119 4>, <0 120 4>, <0 121 4>, <0 122 4>, <0 123 4>, <0 221 4>, <0
222 4>;
interrupt-controller property表明它也是"interrupt controller"。凡是interrupt controller必须申明。
interrupt-names = "gpio_mux";
这个property好象不是标准(ePAPR)定义的,不知道派什么用处!
start_kernel()
    I
init_IRQ()
```

```
in arch/arm/kernel/irq.c
void __init init_IRQ(void)
{
    int ret;
    if (IS_ENABLED(CONFIG_OF) && !machine_desc->init_irq)
         irqchip_init();
     else
         machine_desc->init_irq();
     if (IS_ENABLED(CONFIG_OF) && IS_ENABLED(CONFIG_CACHE_L2X0) &&
       (machine_desc->l2c_aux_mask || machine_desc->l2c_aux_val)) {
         outer_cache.write_sec = machine_desc->l2c_write_sec;
         ret = I2x0_of_init(machine_desc->I2c_aux_val,
                     machine_desc->l2c_aux_mask);
         if (ret)
              pr_err("L2C: failed to init: %d\n", ret);
    }
}
in drivers/irqchip/irqchip.c
void __init irqchip_init(void)
{
     of_irq_init(__irqchip_of_table);
}
```

```
/**
* of_irq_init - Scan and init matching interrupt controllers in DT
* @matches: 0 terminated array of nodes to match and init function to call
* This function scans the device tree for matching interrupt controller nodes,
* and calls their initialization functions in order with parents first.
*/
void __init of_irq_init(const struct of_device_id *matches)
{
     struct device_node *np, *parent = NULL;
     struct intc_desc *desc, *temp_desc;
     struct list_head intc_desc_list, intc_parent_list;
     INIT_LIST_HEAD(&intc_desc_list);
     INIT_LIST_HEAD(&intc_parent_list);
    for_each_matching_node(np, matches) {
         if (!of find property(np, "interrupt-controller", NULL) ||
                    !of_device_is_available(np))
               continue;
         /*
          * Here, we allocate and populate an intc_desc with the node
          * pointer, interrupt-parent device_node etc.
          */
          desc = kzalloc(sizeof(*desc), GFP_KERNEL);
          if (WARN_ON(!desc))
               goto err;
```

```
desc->dev = np;
     desc->interrupt_parent = of_irq_find_parent(np);
     if (desc->interrupt_parent == np)
          desc->interrupt_parent = NULL;
     list_add_tail(&desc->list, &intc_desc_list);
}
* The root irq controller is the one without an interrupt-parent.
 * That one goes first, followed by the controllers that reference it,
* followed by the ones that reference the 2nd level controllers, etc.
*/
while (!list_empty(&intc_desc_list)) {
     /*
     * Process all controllers with the current 'parent'.
      * First pass will be looking for NULL as the parent.
     * The assumption is that NULL parent means a root controller.
     */
     list_for_each_entry_safe(desc, temp_desc, &intc_desc_list, list) {
          const struct of_device_id *match;
          int ret;
          of_irq_init_cb_t irq_init_cb;
          if (desc->interrupt_parent != parent)
               continue;
          list_del(&desc->list);
          match = of match node(matches, desc->dev);
```

```
if (WARN(!match->data,
        "of_irq_init: no init function for %s\n",
       match->compatible)) {
          kfree(desc);
          continue;
     }
     pr_debug("of_irq_init: init %s @ %p, parent %p\n",
           match->compatible,
           desc->dev, desc->interrupt_parent);
     irq_init_cb = (of_irq_init_cb_t)match->data;
     ret = irq_init_cb(desc->dev, desc->interrupt_parent);
     if (ret) {
          kfree(desc);
          continue;
     }
     * This one is now set up; add it to the parent list so
     * its children can get processed in a subsequent pass.
     */
     list_add_tail(&desc->list, &intc_parent_list);
/* Get the next pending parent that might have children */
desc = list_first_entry_or_null(&intc_parent_list,
                    typeof(*desc), list);
if (!desc) {
     pr_err("of_irq_init: children remain, but no parents\n");
```

}

```
break;
        }
        list_del(&desc->list);
        parent = desc->dev;
        kfree(desc);
    }
    list_for_each_entry_safe(desc, temp_desc, &intc_parent_list, list) {
        list_del(&desc->list);
        kfree(desc);
    }
err:
    list_for_each_entry_safe(desc, temp_desc, &intc_desc_list, list) {
        list_del(&desc->list);
        kfree(desc);
    }
}
该function就是负责初始化device tree中的所有interrupt controller(凡是带有"interrupt controller" property的device
node).
由于interrupt controller由依赖关系,即child依赖parent,这里就是gpio interrupt controller依赖gic interrupt
controller。所以
初始化时要先parent后child。试想一下,如果先初始化gpio interrupt controller,则gpio初始化时要向gic register
interrupt,但gic
这是都还没初始化,自然失败。
在gpio0 device node中
#interrupt-cells = <2>;
```

in drivers/gpio/gpio-pxa.c

```
const struct irq_domain_ops pxa_irq_domain_ops = {
     .map
              = pxa_irq_domain_map,
     .xlate
              = irq_domain_xlate_twocell,
};
in kernel/irq/irqdomain.c
/**
* irq_domain_xlate_twocell() - Generic xlate for direct two cell bindings
* Device Tree IRQ specifier translation function which works with two cell
* bindings where the cell values map directly to the hwirq number
* and linux irq flags.
*/
int irq_domain_xlate_twocell(struct irq_domain *d, struct device_node *ctrlr,
              const u32 *intspec, unsigned int intsize,
              irq_hw_number_t *out_hwirq, unsigned int *out_type)
{
     if (WARN_ON(intsize < 2))
         return -EINVAL;
     *out_hwirq = intspec[0];
                                                                4
     *out_type = intspec[1] & IRQ_TYPE_SENSE_MASK;
                                                             (5)
     return 0;
}
4
```

intspec[0]是某个gpio bank上的0 - 31中的one pin。

```
(5)
```

```
intspec[1], interrupt trigger type.
```

在Gemstone2 board上没有device的interrupt是连接到8个GPIO bank上的,所以没有device node的"interrupt-parent" property是GPIO的。

```
如果有的话,我想应该是这样的,
```

```
fake_device@XXXX {
......

interrupt-parent = <&gcb1>;

interrupts = <0x3 0x4>;
.....
```

这里interrupt-parent必须指向某个特定的gpio bank,而不能是gpio@d4019000。

0x3表示gcb1 gpio bank的0x3 pin作为该device的interrupt pin。

如果interrupt-parent = <&gpio0>,那么现在的gpio0 device node的#interrupt-cells = #interrupt-cells = <2>是错的。

正确的应该是

};

```
gpio0: gpio@d4019000 {
    compatible = "marvell,peg-gpio";
    #address-cells = <2>;
    #size-cells = <2>;
    reg = <0 0xd4019000 0 0x1000>;
    gpio-controller;
```

```
#gpio-cells = <2>;
         interrupts = <0 36 4>, <0 119 4>, <0 120 4>, <0 121 4>, <0 122 4>, <0 123 4>, <0 221 4>, <0 222 4>;
         interrupt-names = "gpio_mux";
         interrupt-controller;
         #interrupt-cells = <3>;
         clocks = <&apbus_apb_clkgate>;
         ranges;
    };
而
fake_device@XXXX {
    interrupt-parent = <&gpio0>;
    interrupts = <0x1 0x3 0x4>;
};
这里interrupts中的0x1表示gpio bank 1。
当然gpio-pxa.c中相应的interrupt controller相关code也要稍作改写。
```

root@granite2:/# cat /sy	/s/kernel/debug/irq_do	main_mapp	oing
name mapped	linear-max direct-ma	ax devtree-r	node
mv-pegmatite-u3d	1 1 0 /us	b3_top@d42	220000
GPIO 256	256 0 /gpio@	d4019000	
GIC 288	288 0 /interru	pt-controller	@d1d01000
irq hwirq chip name	chip data active	type	domain
16 0x00010 GIC	0xc0609154	LINEAR	GIC
17 0x00011 GIC	0xc0609154	LINEAR	GIC
18 0x00012 GIC	0xc0609154	LINEAR	GIC
19 0x00013 GIC	0xc0609154	LINEAR	GIC
20 0x00014 GIC	0xc0609154	LINEAR	GIC
21 0x00015 GIC	0xc0609154	LINEAR	GIC
22 0x00016 GIC	0xc0609154	LINEAR	GIC
23 0x00017 GIC	0xc0609154	LINEAR	GIC
24 0x00018 GIC	0xc0609154	LINEAR	GIC
25 0x00019 GIC	0xc0609154	LINEAR	GIC
26 0x0001a GIC	0xc0609154	LINEAR	GIC
27 0x0001b GIC	0xc0609154	LINEAR	GIC
28 0x0001c GIC	0xc0609154	LINEAR	GIC
29 0x0001d GIC	0xc0609154 *	LINEAR	GIC
30 0x0001e GIC	0xc0609154 *	LINEAR	GIC
31 0x0001f GIC	0xc0609154	LINEAR	GIC
32 0x00020 GIC	0xc0609154	LINEAR	GIC
33 0x00021 GIC	0xc0609154	LINEAR	GIC
34 0x00022 GIC	0xc0609154	LINEAR	GIC
35 0x00023 GIC	0xc0609154	LINEAR	GIC
36 0x00024 GIC	0xc0609154	LINEAR	GIC

37 0x00025 GIC	0xc0609154	* LINEAR	GIC
38 0x00026 GIC	0xc0609154	LINEAR	GIC
39 0x00027 GIC	0xc0609154	* LINEAR	GIC
40 0x00028 GIC	0xc0609154	LINEAR	GIC
41 0x00029 GIC	0xc0609154	LINEAR	GIC
42 0x0002a GIC	0xc0609154	* LINEAR	GIC
43 0x0002b GIC	0xc0609154	LINEAR	GIC
44 0x0002c GIC	0xc0609154	LINEAR	GIC
45 0x0002d GIC	0xc0609154	LINEAR	GIC
46 0x0002e GIC	0xc0609154	LINEAR	GIC
47 0x0002f GIC	0xc0609154	* LINEAR	GIC
48 0x00030 GIC	0xc0609154	* LINEAR	GIC
49 0x00031 GIC	0xc0609154	LINEAR	GIC
50 0x00032 GIC	0xc0609154	LINEAR	GIC
51 0x00033 GIC	0xc0609154	LINEAR	GIC
52 0x00034 GIC	0xc0609154	LINEAR	GIC
53 0x00035 GIC	0xc0609154	LINEAR	GIC
54 0x00036 GIC	0xc0609154	LINEAR	GIC
55 0x00037 GIC	0xc0609154	* LINEAR	GIC
56 0x00038 GIC	0xc0609154	LINEAR	GIC
57 0x00039 GIC	0xc0609154	* LINEAR	GIC
58 0x0003a GIC	0xc0609154	LINEAR	GIC
59 0x0003b GIC	0xc0609154	* LINEAR	GIC
60 0x0003c GIC	0xc0609154	LINEAR	GIC
61 0x0003d GIC	0xc0609154	* LINEAR	GIC
62 0x0003e GIC	0xc0609154	* LINEAR	GIC
63 0x0003f GIC	0xc0609154	LINEAR	GIC
64 0x00040 GIC	0xc0609154	* LINEAR	GIC
65 0x00041 GIC	0xc0609154	LINEAR	GIC

66 0x00042	GIC	0xc0609154		LINEAR	GIC
67 0x00043	GIC	0xc0609154		LINEAR	GIC
68 0x00044	GIC	0xc0609154		LINEAR	GIC
69 0x00045	GIC	0xc0609154		LINEAR	GIC
70 0x00046	GIC	0xc0609154	*	LINEAR	GIC
71 0x00047	GIC	0xc0609154	*	LINEAR	GIC
72 0x00048	GIC	0xc0609154		LINEAR	GIC
73 0x00049	GIC	0xc0609154		LINEAR	GIC
74 0x0004a	GIC	0xc0609154	*	LINEAR	GIC
75 0x0004b	GIC	0xc0609154		LINEAR	GIC
76 0x0004c	GIC	0xc0609154		LINEAR	GIC
77 0x0004d	GIC	0xc0609154		LINEAR	GIC
78 0x0004e	GIC	0xc0609154	*	LINEAR	GIC
79 0x0004f	GIC	0xc0609154		LINEAR	GIC
80 0x00050	GIC	0xc0609154		LINEAR	GIC
81 0x00051	GIC	0xc0609154		LINEAR	GIC
82 0x00052	GIC	0xc0609154		LINEAR	GIC
83 0x00053	GIC	0xc0609154		LINEAR	GIC
84 0x00054	GIC	0xc0609154		LINEAR	GIC
85 0x00055	GIC	0xc0609154	*	LINEAR	GIC
86 0x00056	GIC	0xc0609154	*	LINEAR	GIC
87 0x00057	GIC	0xc0609154	*	LINEAR	GIC
88 0x00058	GIC	0xc0609154	*	LINEAR	GIC
89 0x00059	GIC	0xc0609154		LINEAR	GIC
90 0x0005a	GIC	0xc0609154		LINEAR	GIC
91 0x0005b	GIC	0xc0609154		LINEAR	GIC
92 0x0005c	GIC	0xc0609154		LINEAR	GIC
93 0x0005d	GIC	0xc0609154		LINEAR	GIC
94 0x0005e	GIC	0xc0609154		LINEAR	GIC

95 0x0005f GIC	0xc0609154	LINEAR	GIC
96 0x00060 GIC	0xc0609154	LINEAR	GIC
97 0x00061 GIC	0xc0609154	LINEAR	GIC
98 0x00062 GIC	0xc0609154	LINEAR	GIC
99 0x00063 GIC	0xc0609154	LINEAR	GIC
100 0x00064 GIC	0xc0609154	LINEAR	GIC
101 0x00065 GIC	0xc0609154	LINEAR	GIC
102 0x00066 GIC	0xc0609154	LINEAR	GIC
103 0x00067 GIC	0xc0609154	LINEAR	GIC
104 0x00068 GIC	0xc0609154	LINEAR	GIC
105 0x00069 GIC	0xc0609154	LINEAR	GIC
106 0x0006a GIC	0xc0609154	LINEAR	GIC
107 0x0006b GIC	0xc0609154	LINEAR	GIC
108 0x0006c GIC	0xc0609154	LINEAR	GIC
109 0x0006d GIC	0xc0609154	LINEAR	GIC
110 0x0006e GIC	0xc0609154	LINEAR	GIC
111 0x0006f GIC	0xc0609154	LINEAR	GIC
112 0x00070 GIC	0xc0609154	LINEAR	GIC
113 0x00071 GIC	0xc0609154	LINEAR	GIC
114 0x00072 GIC	0xc0609154	LINEAR	GIC
115 0x00073 GIC	0xc0609154	LINEAR	GIC
116 0x00074 GIC	0xc0609154	LINEAR	GIC
117 0x00075 GIC	0xc0609154	LINEAR	GIC
118 0x00076 GIC	0xc0609154	LINEAR	GIC
119 0x00077 GIC	0xc0609154	LINEAR	GIC
120 0x00078 GIC	0xc0609154	LINEAR	GIC
121 0x00079 GIC	0xc0609154	LINEAR	GIC
122 0x0007a GIC	0xc0609154	LINEAR	GIC
123 0x0007b GIC	0xc0609154	LINEAR	GIC

124	0x0007c GIC	0xc0609154	LINEAR	GIC	
125	0x0007d GIC	0xc0609154	LINEAR	GIC	
126	0x0007e GIC	0xc0609154	LINEAR	GIC	
127	0x0007f GIC	0xc0609154	LINEAR	GIC	
128	0x00080 GIC	0xc0609154	LINEAR	GIC	
129	0x00081 GIC	0xc0609154	LINEAR	GIC	
130	0x00082 GIC	0xc0609154	LINEAR	GIC	
131	0x00083 GIC	0xc0609154	LINEAR	GIC	
132	0x00084 GIC	0xc0609154	LINEAR	GIC	
133	0x00085 GIC	0xc0609154	LINEAR	GIC	
134	0x00086 GIC	0xc0609154	LINEAR	GIC	
135	0x00087 GIC	0xc0609154	LINEAR	GIC	
136	0x00088 GIC	0xc0609154	LINEAR	GIC	
137	0x00089 GIC	0xc0609154	LINEAR	GIC	
138	0x0008a GIC	0xc0609154	* LINEAR	GIC	
139	0x0008b GIC	0xc0609154	* LINEAR	GIC	
140	0x0008c GIC	0xc0609154	LINEAR	GIC	
141	0x0008d GIC	0xc0609154	LINEAR	GIC	
142	0x0008e GIC	0xc0609154	LINEAR	GIC	
143	0x0008f GIC	0xc0609154	LINEAR	GIC	
144	0x00090 GIC	0xc0609154	LINEAR	GIC	
145	0x00091 GIC	0xc0609154	LINEAR	GIC	
146	0x00092 GIC	0xc0609154	LINEAR	GIC	
147	0x00093 GIC	0xc0609154	LINEAR	GIC	
148	0x00094 GIC	0xc0609154	LINEAR	GIC	
149	0x00095 GIC	0xc0609154	LINEAR	GIC	
150	0x00096 GIC	0xc0609154	LINEAR	GIC	
151	0x00097 GIC	0xc0609154	LINEAR	GIC	
152	0x00098 GIC	0xc0609154	LINEAR	GIC	

153	0x00099	GIC	0xc0609154	LINEAR	GIC
154	0x0009a	GIC	0xc0609154	LINEAR	GIC
155	0x0009b	GIC	0xc0609154	LINEAR	GIC
156	0x0009c	GIC	0xc0609154	LINEAR	GIC
157	0x0009d	GIC	0xc0609154	LINEAR	GIC
158	0x0009e	GIC	0xc0609154	LINEAR	GIC
159	0x0009f	GIC	0xc0609154	LINEAR	GIC
160	0x000a0	GIC	0xc0609154	LINEAR	GIC
161	0x000a1	GIC	0xc0609154	LINEAR	GIC
162	0x000a2	GIC	0xc0609154	LINEAR	GIC
163	0x000a3	GIC	0xc0609154	LINEAR	GIC
164	0x000a4	GIC	0xc0609154	LINEAR	GIC
165	0x000a5	GIC	0xc0609154	LINEAR	GIC
166	0x000a6	GIC	0xc0609154	LINEAR	GIC
167	0x000a7	GIC	0xc0609154	LINEAR	GIC
168	0x000a8	GIC	0xc0609154	LINEAR	GIC
169	0x000a9	GIC	0xc0609154	LINEAR	GIC
170	0x000aa	GIC	0xc0609154	LINEAR	GIC
171	0x000ab	GIC	0xc0609154	LINEAR	GIC
172	0x000ac	GIC	0xc0609154	LINEAR	GIC
173	0x000ad	GIC	0xc0609154	LINEAR	GIC
174	0x000ae	GIC	0xc0609154	LINEAR	GIC
175	0x000af	GIC	0xc0609154	LINEAR	GIC
176	0x000b0	GIC	0xc0609154	* LINEAR	GIC
177	0x000b1	GIC	0xc0609154	LINEAR	GIC
178	0x000b2	GIC	0xc0609154	LINEAR	GIC
179	0x000b3	GIC	0xc0609154	LINEAR	GIC
180	0x000b4	GIC	0xc0609154	LINEAR	GIC
181	0x000b5	GIC	0xc0609154	LINEAR	GIC

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187 0x000bb GIC	0xc0609154	LINEAR	GIC	
188 0x000bc GIC	0xc0609154	LINEAR	GIC	
189 0x000bd GIC	0xc0609154	LINEAR	GIC	
190 0x000be GIC	0xc0609154	* LINEAR	GIC	
191 0x000bf GIC	0xc0609154 '	* LINEAR	GIC	
192 0x000c0 GIC	0xc0609154	* LINEAR	GIC	
193 0x000c1 GIC	0xc0609154	* LINEAR	GIC	
194 0x000c2 GIC	0xc0609154	* LINEAR	GIC	
195 0x000c3 GIC	0xc0609154	* LINEAR	GIC	
196 0x000c4 GIC	0xc0609154	* LINEAR	GIC	
197 0x000c5 GIC	0xc0609154	* LINEAR	GIC	
198 0x000c6 GIC	0xc0609154	* LINEAR	GIC	
199 0x000c7 GIC	0xc0609154	* LINEAR	GIC	
200 0x000c8 GIC	0xc0609154	* LINEAR	GIC	
201 0x000c9 GIC	0xc0609154	* LINEAR	GIC	
202 0x000ca GIC	0xc0609154	* LINEAR	GIC	
203 0x000cb GIC	0xc0609154	* LINEAR	GIC	
204 0x000cc GIC	0xc0609154	* LINEAR	GIC	
205 0x000cd GIC	0xc0609154	* LINEAR	GIC	
206 0x000ce GIC	0xc0609154	* LINEAR	GIC	
207 0x000cf GIC	0xc0609154 *	* LINEAR	GIC	
208 0x000d0 GIC	0xc0609154	* LINEAR	GIC	
209 0x000d1 GIC	0xc0609154	* LINEAR	GIC	
210 0x000d2 GIC	0xc0609154	LINEAR	GIC	

211	0x000d3	GIC	0xc0609154	*	LINEAR	GIC
212	0x000d4	GIC	0xc0609154	*	LINEAR	GIC
213	0x000d5	GIC	0xc0609154	*	LINEAR	GIC
214	0x000d6	GIC	0xc0609154		LINEAR	GIC
215	0x000d7	GIC	0xc0609154		LINEAR	GIC
216	0x000d8	GIC	0xc0609154		LINEAR	GIC
217	0x000d9	GIC	0xc0609154		LINEAR	GIC
218	0x000da	GIC	0xc0609154		LINEAR	GIC
219	0x000db	GIC	0xc0609154		LINEAR	GIC
220	0x000dc	GIC	0xc0609154		LINEAR	GIC
221	0x000dd	GIC	0xc0609154	*	LINEAR	GIC
222	0x000de	GIC	0xc0609154	*	LINEAR	GIC
223	0x000df	GIC	0xc0609154	*	LINEAR	GIC
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225	0x000e1	GIC	0xc0609154	*	LINEAR	GIC
226	0x000e2	GIC	0xc0609154	*	LINEAR	GIC
227	0x000e3	GIC	0xc0609154	*	LINEAR	GIC
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232	0x000e8	GIC	0xc0609154		LINEAR	GIC
233	0x000e9	GIC	0xc0609154		LINEAR	GIC
234	0x000ea	GIC	0xc0609154		LINEAR	GIC
235	0x000eb	GIC	0xc0609154		LINEAR	GIC
236	0x000ec	GIC	0xc0609154	*	LINEAR	GIC
237	0x000ed	GIC	0xc0609154	*	LINEAR	GIC
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243 0x000f3 GIC	0xc0609154	* LINEAR	GIC
244 0x000f4 GIC	0xc0609154	LINEAR	GIC
245 0x000f5 GIC	0xc0609154	LINEAR	GIC
246 0x000f6 GIC	0xc0609154	LINEAR	GIC
247 0x000f7 GIC	0xc0609154	LINEAR	GIC
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254 0x000fe GIC	0xc0609154	LINEAR	GIC
255 0x000ff GIC	0xc0609154	LINEAR	GIC
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269 0x0010d GIC		LINEAR	
270 0x0010e GIC		LINEAR	GIC
271 0x0010f GIC	0xc0609154	LINEAR	GIC
272 0x00110 GIC	0xc0609154	LINEAR	GIC
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281 0x00119 GIC	0xc0609154	LINEAR	GIC
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287 0x0011f GIC	0xc0609154	LINEAR	GIC
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399 0x0006f GPIO	(null)	LINEAR	GPIO
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413 0x0007d GPIO	(null)	LINEAR	GPIO

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415 0x0007f GPIO	(null)	LINEAR	GPIO
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417 0x00081 GPIO	(null)	LINEAR	GPIO
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419 0x00083 GPIO	(null)	LINEAR	GPIO
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513 0x000e1 GPIO	(null)	LINEAR	GPIO
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516 0x000e4 GPIO	(null)	LINEAR	GPIO
517 0x000e5 GPIO	(null)	LINEAR	GPIO
518 0x000e6 GPIO	(null)	LINEAR	GPIO
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520 0x000e8 GPIO	(null)	LINEAR	GPIO
521 0x000e9 GPIO	(null)	LINEAR	GPIO
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535 0x000f7 GPIO	(null)	LINEAR	GPIO	
536 0x000f8 GPIO	(null)	LINEAR	GPIO	
537 0x000f9 GPIO	(null)	LINEAR	GPIO	
538 0x000fa GPIO	(null)	LINEAR	GPIO	
539 0x000fb GPIO	(null)	LINEAR	GPIO	
540 0x000fc GPIO	(null)	LINEAR	GPIO	
541 0x000fd GPIO	(null)	LINEAR	GPIO	
542 0x000fe GPIO	(null)	LINEAR	GPIO	
543 0x000ff GPIO	(null)	LINEAR	GPIO	
544 0x00000 mv-pegmatit	e-u3d 0xc	06a8c50 *	LINEAR	mv-pegmatite-u3d