

CONFIG_NR_CPUS=4

CONFIG_HOTPLUG_CPU=y

对Gemstone2 , CONFIG_NR_CPUS=2

CONFIG_HOTPLUG_CPU好像不应该enable?

kernel/cpu.c

kernel/smp.c

kernel/smpboot.c

arch/arm/kernel/smp.c

arch/arm/kernel/head.S

drivers/platform/pegmatite/smp/

in devicetree-ulmage-mv6270-toc.dtb

```
1.      cpus {
2.          #address-cells = <0x1>;
3.          #size-cells = <0x0>;
4.
5.          cpu@0 {
6.              device_type = "cpu";
7.              compatible = "arm,cortex-a53";
8.              reg = <0xffff00>;
9.          };
10.
11.         cpu@1 {
12.             device_type = "cpu";
13.             compatible = "arm,cortex-a53";
14.             reg = <0xffff01>;
15.             enable-method = "marvell,pegmatite-apmu-boot";
16.         };
17.
18.         cpu@2 {
19.             device_type = "cpu";
20.             compatible = "arm,cortex-a53";
21.             reg = <0xffff02>;
22.             enable-method = "marvell,pegmatite-apmu-boot";
23.         };
24.
25.         cpu@3 {
26.             device_type = "cpu";
27.             compatible = "arm,cortex-a53";
28.             reg = <0xffff03>;
29.             enable-method = "marvell,pegmatite-apmu-boot";
30.         };
31.     };
```

in devicetree-ulmage-mv6220-toc.dtb

```

1.     cpus {
2.         #address-cells = <0x1>;
3.         #size-cells = <0x0>;
4.
5.         cpu@0 {
6.             device_type = "cpu";
7.             compatible = "arm,cortex-a53";
8.             reg = <0xffff00>;
9.         };
10.
11.        cpu@1 {
12.            device_type = "cpu";
13.            compatible = "arm,cortex-a53";
14.            reg = <0xffff01>;
15.            enable-method = "marvell,pegmatite-apmu-boot";
16.        };
17.    };
18.
19.
20.    squ@d1000000 {
21.        compatible = "mmio-sram";
22.        reg = <0x0 0xd1000000 0x0 0x18000>;
23.        clocks = <0x2>;
24.        #address-cells = <0x1>;
25.        #size-cells = <0x1>;
26.        ranges = <0x0 0x0 0xd1000000 0x18000>;
27.        linux,phandle = <0x4>;
28.        phandle = <0x4>;
29.
30.        smpboot-sram@0 {
31.            compatible = "marvell,pegmatite-smpboot-sram";
32.            reg = <0x0 0x20>;
33.        };
34.    };

```

对gemstone2 / granite2而言，0xd1000000 to 0xd1000019存放如下code

```

1.  c04423f8 <pegmatite_smp_jump>:
2.  c04423f8:      e59f100c      ldr     r1, [pc, #12]    ; c044240c <pegmatite_smp
   _jump_table>
3.  c04423fc:      ee100fb0      mrc     15, 0, r0, cr0, cr0, {5}
4.  c0442400:      e200000f      and     r0, r0, #15
5.  c0442404:      e7911100      ldr     r1, [r1, r0, lsl #2]
6.  c0442408:      e12fff31      blx     r1
7.
8.  c044240c <pegmatite_smp_jump_table>:
9.  c044240c:      00000000      .word   0x00000000

```

boot core会修改CIU，使得secondary core reset以后从physical address的0xd1000000开始运行！

c044240c <pegmatite_smp_jump_table>:

c044240c: 00000000 .word 0x00000000

会被boot core指向 function address array, array size是core number。

(*pegmatite_smp_jump_table) [0]是无用的，因为它对应的是boot core

(*pegmatite_smp_jump_table) [1] = pegmatite_secondary_startup()