1. upc.ko is loaded

Make ARM Formater core and IO core both run upc_int.bin

2. cat upc_int.bin > /dev/upc0

3. cat upc_int.bin > /dev/upc1

4. upc_start_stop -o start

5. generate interrupts

```
--------------------------------------------

root@granite2:~/upc# devmem 0xf9808128 w 1    ①


ISR 0x07c00010

mailbox 0 = 0x00000001

Exit

root@granite2:~/upc# devmem 0xf980812C w 1    ②


ISR 0x07c00020

mailbox 1 = 0x00000001

Exit

root@granite2:~/upc# devmem 0xf9809130 w 1    ③


ISR 0x07c00040

mailbox 2 = 0x00000001

Exit
```

```
root@granite2:~/upc# devmem 0xf9809134 w 1    ④


ISR 0x07c00080

mailbox 3 = 0x00000001

Exit

root@granite2:~/upc# devmem 0xf9809138 w 1    ⑤


ISR 0x07c00100

mailbox 4 = 0x00000001

Exit

root@granite2:~/upc# devmem 0xf980913c w 1    ⑥


ISR 0x07c00200

mailbox 5 = 0x00000001

Exit

------------------------------------------
```

Notes:

①② command make upc0 code run

③④⑤⑥ command make upc1 code run

I don't know why ！

```
$ cat upc_int.bin > /dev/upc0
$ cat upc_wait.bin > /dev/upc1
```

Run ①② command, you will get messages, but run ③④⑤⑥ command, you will get nothing. Because upc_wait.bin running on upc1 will not handle interrupts.

```
$ cat upc_int.bin > /dev/upc1
$ cat upc_wait.bin > /dev/upc0
```

Run ①② command, you will get nothing, but run ③④⑤⑥ command, you will get messages.

So I know the interrupts from mailbox0 and mailbox1 are handled by upc0 core, the ones from mailbox2, mailbox3, mailbox4 and mailbox5 are handled by upc1 core.

mailbox data registers' address in Gr2

| | |
|---|---|
| mailbox0 | 0xF980,8128 |
| mailbox1 | 0xF980,812C |
| mailbox2 | 0xF980,9130 |
| mailbox3 | 0xF980,9134 |
| mailbox4 | 0xF980,9138 |
| mailbox5 | 0xF980,913C |