是否可以参考uart?

in arch/arm/boot/dts/pegmatite-clocks.dtsi

```
1.            uart0_clk: uart0clk {
2.                    compatible = "marvell,pegmatite-clkgen";
3.                    #clock-cells = <0>;
4.                    reg = <0 0xd0630528 0 0xc>;
5.                    prediv-shift = <26>;
6.                    clocks = <&ref_clk25mhz>, <&system_pll_gate>, <&ddr_pll_spread>;
7.                    clock-source = <0>;
8.                    max-divide = <4>;
9.                    clock-frequency = <25000000>;
10.           };
11.
12.           uart0_clkfd: uart0clkfd {
13.                   compatible = "marvell,pegmatite-clkfd";
14.                   #clock-cells = <0>;
15.                   reg = <0 0xd0630528 0 0xc>;
16.                   clocks = <&uart0_clk>;
17.                   clock-frequency = <11059200>;
18.           };
19.
20.    uart0_clkgate: uart0clkgate {
21.                   compatible = "marvell,pegmatite-clkgate";
22.                   #clock-cells = <0>;
23.                   reg = <0 0xd0630528 0 0xc>;
24.                   clocks = <&uart0_clkfd>;
25.           };
```

in arch/arm/boot/dts/pegmatite.dtsi

```
1.          uart0: uart@d4030000 {
2.                  compatible = "mrvl,pxa-uart";
3.                  reg = <0 0xd4030000 0 0x1000>;
4.                  interrupts = <0 16 4>;
5.                  clocks = <&uart0_clkgate>;
6.                  status = "disabled";
7.          };
```

in arch/arm/boot/dts/mv6220-toc.dts

```
1.          uart0: uart@d4030000 {
2.                  status = "okay";
3.          };
```

in pegmatite-clocks.dtsi

```
preaudio_clk: preaudioclk {
        compatible = "marvell,pegmatite-clkgen";
        #clock-cells = <0>;
        reg = <0 0xf9080100 0 0x8>;
        prediv-shift = <25>;
        clocks = <&system_pll_gate>, <&ref_clk25mhz>;
        clock-source = <0>;
        max-divide = <30>;
        clock-frequency = <83333333>;
};

audio_clk: audioclk {
        compatible = "marvell,pegmatite-clkgen";
        #clock-cells = <0>;
        reg = <0 0xf9080108 0 0x8>;
        clocks = <&preaudio_clk>;
        max-divide = <60>;
        clock-frequency = <1536000>;
};

audio_clkgate: audioclkgate {
        compatible = "marvell,pegmatite-clkgate";
        #clock-cells = <0>;
        reg = <0 0xf9080108 0 0x8>;
        clocks = <&audio_clk>;
};
```

audio-ddac是否只要refer to audio_clkgate即可?

for example:

audio-ddac@f80c0000 {

COMPATIBLE = "mrvl,audio-ddac";

reg = <0 0xf80c0000 0 0x10>;

clocks = <&audio_clkgate>;

cdmaid = <0x18>;

};