Gr2 / Gs2使用的是ARM的GIC400 interrupt controller

For example:

```
uart@d4016000 {
        compatible = "mrvl,pxa-uart";
        reg = <0x0 0xd4016000 0x0 0x1000>;
        interrupts = <0x0 0x13 0x4>;
        clocks = <0xc>;
        status = "disabled";
};
```

Documentation/devicetree/bindings/arm/gic.txt describes the definition for "interrupts"

```
The 1st cell is the interrupt type; 0 for SPI interrupts, 1 for PPI
interrupts.

The 2nd cell contains the interrupt number for the interrupt type.
SPI interrupts are in the range [0-987].  PPI interrupts are in the
range [0-15].

The 3rd cell is the flags, encoded as follows:
        bits[3:0] trigger type and level flags.
                1 = low-to-high edge triggered
```

2 = high-to-low edge triggered

4 = active high level-sensitive

8 = active low level-sensitive

bits[15:8] PPI interrupt cpu mask. Each bit corresponds to each of the 8 possible cpus attached to the GIC. A bit set to '1' indicated the interrupt is wired to that CPU. Only valid for PPI interrupts.