

```

1.      @ENTRY
2.
3.      .global ExceptionTable
4. ExceptionTable:
5.      LDR PC, ResetAddr
6.      LDR PC, UndefinedAddr
7.      LDR PC, SwiAddr
8.      LDR PC, PrefetchAddr
9.      LDR PC, AbortAddr
10.     NOP
11.     LDR PC, IrqAddr
12. @    LDR PC, FiqAddr
13.
14.     SUB r14,r14,#4          @// Adjust lr to proper address.
15.     STMFD r13!,{r0-r7,r12,r14} @// Save registers to stack.
16.
17.     LDR r12,=Hal_Fsr
18.     MOV r14,pc              @// Store the return address (=pc+4) in r14 (=lr
19. ).
20.     BX r12                  @// Branch to address pointed to by r12.
21.
22.     LDMFD r13!,{r0-r7,r12,pc}^ @// Restore registers and return to
code that was interrupted.

```

显然ExceptionTable必须位于96M memory的边界处，因为r4 core在"reset"后被设置成从这儿开始取指运行。

```

1. Disassembly of section .reset:
2.
3. 06000000 <ExceptionTable>:
4.
5.     @ENTRY
6.
7.     .global ExceptionTable
8. ExceptionTable:
9.     LDR PC, ResetAddr
10. 60000000: e59ff02c    ldr pc, [pc, #44]    ; 60000034 <ResetAddr>
11.     LDR PC, UndefinedAddr
12. 60000004: e59ff02c    ldr pc, [pc, #44]    ; 60000038 <UndefinedAddr>
13.     LDR PC, SwiAddr
14. 60000008: e59ff02c    ldr pc, [pc, #44]    ; 6000003c <SwiAddr>
15.     LDR PC, PrefetchAddr
16. 6000000c: e59ff02c    ldr pc, [pc, #44]    ; 60000040 <PrefetchAddr>
17.     LDR PC, AbortAddr
18. 60000010: e59ff02c    ldr pc, [pc, #44]    ; 60000044 <AbortAddr>
19.     NOP
20. 60000014: e320f000    nop {0}
21.     LDR PC, IrqAddr
22. 60000018: e59ff02c    ldr pc, [pc, #44]    ; 6000004c <IrqAddr>
23. @    LDR PC, FiqAddr
24.
25.     SUB r14,r14,#4        @// Adjust lr to proper address.
26. 6000001c: e24ee004    sub lr, lr, #4
27.     STMFD r13!,{r0-r7,r12,r14}    @// Save registers to stack.
28. 60000020: e92d50ff    push {r0, r1, r2, r3, r4, r5, r6, r7, ip, lr}
29.
30.     LDR r12,=Hal_Fsr
31. 60000024: e59fc048    ldr ip, [pc, #72]    ; 60000074 <FiqHandler>
32.     MOV r14,pc            @// Store the return address (=pc+4) in r14 (=lr
33. ).
34. 60000028: e1a0e00f    mov lr, pc
35.     BX r12                @// Branch to address pointed to by r12.
36. 6000002c: e12fff1c    bx ip
37.
38.     LDMFD r13!,{r0-r7,r12,pc}^    @// Restore registers and return to
39. code that was interrupted.
40. 60000030: e8fd90ff    ldm sp!, {r0, r1, r2, r3, r4, r5, r6, r7, ip, pc}^

```

Hal/6220/build/hal_init_gnu.asm

Hal/6220/build/hal_2nd_init_gnu.asm

```

1. InvokeMain:
2.     MOV r1, #0 @ argv == NULL
3.     MOV r0, #0 @ argc == 0
4.     BL main

```

Hal/6220/build/hal_main.c

```
1.  int main(void)
2.  {
3.      .....
4.
5.      uartPreInit(&_uart);
6.
7.      static UART_CONFIG _config = { 115200,
8.          UART_DATA_BITS_8,
9.          UART_STOP_BITS_1,
10.         UART_PARITY_NONE };
11.
12.     uartSetConfig(_uart, &_amp;_config);
13.
14.     AppInit_Initialize();
15.
16.     while ( 1 )
17.         ;
18. }
```

AppInit_Initialize() is in ApplicationMrvl/init/app_init.c

```

1. void AppInit_Initialize(void)
2. {
3.     SYS_INIT_CFG *cfg = { SYS_INIT_USECASE_SDK };
4.
5.
6.     const volatile uint8_t * hook = (const volatile uint8_t *)&set_speed[0];
7.     // chip speed is application specific - must be done before any other hw
    init or scheduler start
8.     if (*hook == 4) SysApiSystem_set_speed(2);        // fast
9.     if (*hook == 2) SysApiSystem_set_speed(1);
10.    if (*hook == 1) SysApiSystem_set_speed(0);
11.    // if none of bit[0:2] is set no speed change happens
12.
13.
14.    /*
15.     we have no tool to set the print mask before firmware start, or to modify
    it from outside after firmware start. driver?
16.     this is a hack to enable/disable output by patching the firmware binary
    - look for the "PrintBuf" string, etc..
17.     */
18.     uint32_t suppress_dbgcomp = 0;
19.     suppress_dbgcomp = APP_DBGCOMP_LAN | APP_DBGCOMP_LAN_RX | APP_DBGCOMP_LAN_TX | APP_DBGCOMP_LAN_ISR; // this is a lot of output. you don't want to see it usually.
20.     hook = (const volatile uint8_t *)&initial_print_mask[0];
21.     if (*hook == '0') SysApiPrint_ConfigFlags(0xffffffff ^ suppress_dbgcomp, APP_DBGCOMP_LAN); // switch off debug prints
22.     if (*hook == '1') SysApiPrint_ConfigFlags(0xffffffff ^ suppress_dbgcomp, APP_DBGCOMP_LAN); // switch on most(?) of the debug prints
23.     if (*hook == '2') SysApiPrint_ConfigFlags(0xffffffff, APP_DBGCOMP_LAN); // switch on all debug prints
24.     // other values of initial_print_mask[0] will leave the debug print masks unchanged
25.
26.
27.     SysApiInit_Initialize(cfg);
28.
29. }

```

in Sys/init/sys_init.c

```

1. void SysApiInit_Initialize(SYS_INIT_CFG* Cfg)
2. {
3.
4.     HalApiMemory_RamInit();
5.
6.     SysPrint_Init();
7.
8.
9.     if (HalApiReset_WasCold()) {
10.         /*
11.          * sram memory has random content after power on (or clearing reset?).
12.          * thats why uninitialized variables have also random values.
13.          * in this case we do not print anything at this point.
14.          */
15.     } else {
16.         /* this is a warm start. we print using masks from previous run. */
17.         SysApiPrint_Write_varg("I", 0xffffffff, 0xffffffff, "%s/%d %s %s (%s
18.         )\n", __func__, __LINE__, __DATE__, __TIME__, Version_Info);
19.     }
20.
21.     const volatile uint8_t dump_nvm[] = "0=dump_nvm";
22.     if (dump_nvm[0]=='1') HalApiMemory_dump_nvm();
23.
24. #ifdef OS_threadx
25.
26.     tx_kernel_enter();
27. #elif defined OS_freertos
28.     intInit();
29.
30.     SysApi_InitApplModules(NULL);
31.     extern uint32_t pxCurrentTCB;
32.     SysApiPrint_Write_varg("I", 0xffffffff, 0xffffffff, "%s/%d pxCurrentTCB=
33.     %08x\n", __func__, __LINE__, pxCurrentTCB);
34.     vTaskStartScheduler();
35.
36. #endif
37.     while ( 1 )
38.     ;
39. }

```

vTaskStartScheduler();

启动freertos embedded OS.