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Test Strategies for Adaptive Equalizers

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Abstract- **This paper provides an overview of the test strategies for both continuous-time and digitally-assisted adaptive equalizers. Conventionally, an equalizer is characterized by the explicit measurement of the eye diagram at its output, which requires a lengthy testing time and is too costly for production testing. Design for testability and special test stimuli have been developed to facilitate circuit performance characterization and go/no-go production testing. In addition, for digitally-assisted adaptive equalizers, digital signatures extracted from the tap coefficients in the digital adaptation unit can be used for performance prediction and fault detection.**

I. Introduction

Equalizers (EQ) are important building blocks in high-speed serial links (HSSL) that compensate for the inter-symbol interference (ISI) resulting from the channels' limited bandwidth [1]. Although equalizers can be implemented in either the transmitters or the receivers, receiver-side equalizers are the more popular choices because the channel information is often not available at the transmitter. In addition, because the channel characteristics are time variant and unknown in advance, designers often incorporate adaptive schemes in equalizers to dynamically adjust their responses according to the channel conditions. Such equalizers are called adaptive equalizers [2].

A standard method for testing equalizers is to measure their eye qualities using external scopes. This is not, however, an easy task because the lack of direct access to the equalizer output in an HSSL. Even though connecting the equalizer output to an external access point, as shown in Figure 1, is a potential solution, not only is an extra pin count needed, but the signal integrity of the interconnects also degrades as a result of the probe contact. Therefore, the eye characteristics captured through external probing differs from that captured by the clock and data recovery (CDR) circuits. In addition, measuring eye diagrams demands a lengthy testing time and is not cost-effective for production testing. Several testing techniques and strategies have recently been developed to address these issues for test quality improvement and test cost reduction. We will review some of these developments in this paper.

In the next section, we review the basic architectures of both continuous-time and digitally-assisted adaptive equalizers. In Section III, we summarize the general testing strategies for equalizers, in which we focus on eye-diagram monitoring and loopback testing approaches. Sections IV and V present some of the recent developments in testing both continuous-time and digitally-assisted adaptive equalizers.

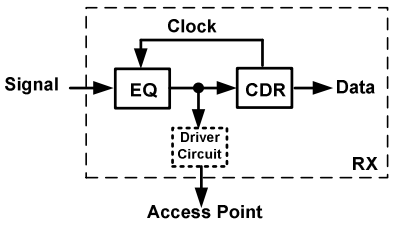

Figure 1: A receiver in an HSSL

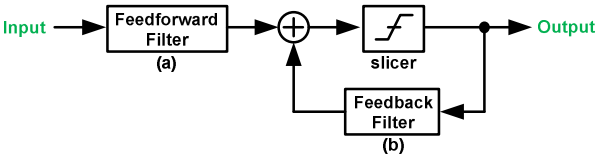

Figure 2: Receiver equalization architectures: (a) feedforward filter, and (b) feedback filter

II. Adaptive Equalizer Architectures

Receiver equalization can be realized using a feedforward filter, a feedback filter, or the combination of both (see Figure 2). A feedforward filter reduces pre-cursor ISI and a feedback filter mitigates post-cursor ISI. An equalizer that incorporates a feedforward filter only is called a feedforward equalizer (FFE). An equalizer with a feedback filter only or with both feedforward and feedback filters is called a decision feedback equalizer (DFE). In adaptive equalizers, the *weighting factors* (aka *tap coefficients*) of the filters are dynamically adjusted by an adaptation algorithm. The adaptation scheme is implemented in either an analog or a mixed-signal fashion. The former is called a continuous-time adaptive equalizer (CT-AEQ) and the latter is called a digitally-assisted adaptive equalizer (DA-AEQ).

A. Continuous-time adaptive equalizer

CT-AEQ does not require a sampling clock, so the equalizer functions independently of the CDR circuit. The block diagrams of a conventional and an enhanced CT-AEQ are shown in figures 3 and 4. To compensate for the high-frequency loss due to the transmission channel, the equalization filter either boosts the high frequency components or attenuates the low frequency components of the received input signal. The compensation gain of the equalization filter is adjusted by an adaptive servo loop. In conventional CT-AEQs [3]-[5], the compensation gains are determined based on the difference between the high frequency contents of the comparator's input and output signals. Although it has been successfully demonstrated in 0.13μm CMOS technology that this architecture achieved a performance of 10 Gb/s [5], it is, in practice, difficult to

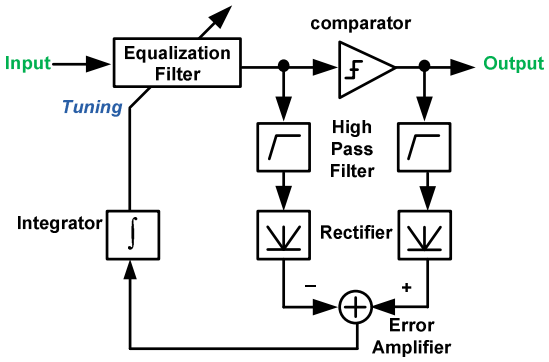

Figure 3: Block diagram of a conventional CT-AEQ

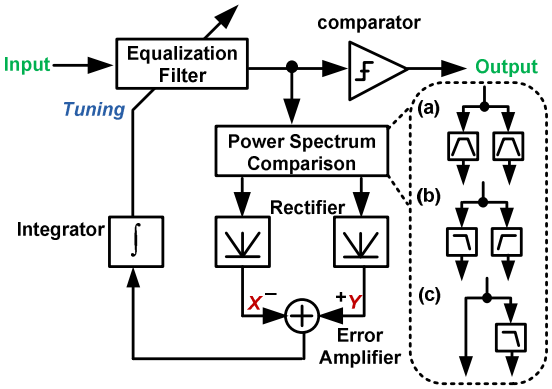

Figure 4: Block diagram of an enhanced CT-AEQ

design a comparator that can generate a clean waveform for comparison at very high frequencies. On the other hand, in enhanced CT-AEQs [6]-[8], the compensation gains of the equalization filter are controlled by the power difference between the two frequency ranges of the equalization filter's output signal. This power spectrum comparison has been implemented using two band-pass filters (BPFs) [6] (Figure 4(a)), a low-pass filter (LPF) and a high-pass filter (HPF) [7] (Figure 4(b)), and a LPF alone [8] (Figure 4(c)). Since there is no comparator in the feedback path, these enhanced CT-AEQs have achieved higher speeds with less power consumption in comparison to their conventional counterparts.

B. Digitally-assisted adaptive equalizer

Analog adaptation approaches suffer from the non-idealities of the analog components and noise. As technology scales, it becomes increasingly difficult to design high performance analog circuits. In addition, the area and power consumption of the analog circuits scale at a slower rate than do their digital counterparts. Therefore, designers have started to adopt the *digitally-assisted* design style [9] to reduce the analog design complexity. In this approach, a portion of the analog tasks are shifted to the digital domain. Recent successful designs following this

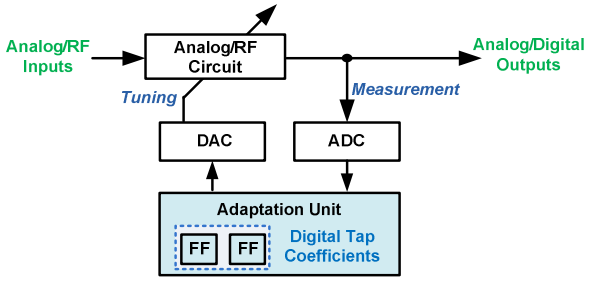

Figure 5: The conceptual diagram of a digitally-assisted design

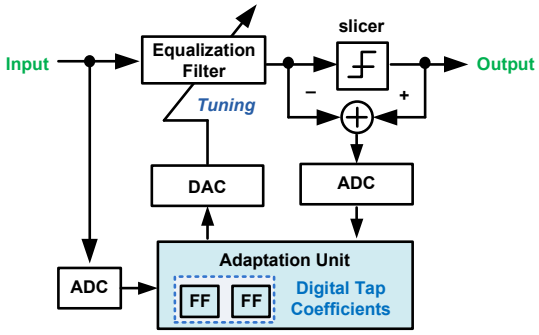

Figure 6: Block diagram of a digitally-assisted adaptive equalizer

style include ADCs [10]-[12], phase-lock loops [13], and RF transceivers [14]-[15].

The conceptual diagram of a digitally-assisted design is shown in Figure 5. Some aspects of the analog circuit's performance are captured and converted into digital data through analog-to-digital converters or simply through comparators. Such information is used as input to the digital adaptation unit that derives the digital tap coefficients based on an underlying digital adaptation algorithm. These digital tap coefficients are converted into analog voltage signals, which in turn adjust the analog circuit performance through the built-in tuning knobs.

The block diagram of a DA-AEQ [16]-[19] that adheres to the digitally-assisted design style is shown in Figure 6. The pure digital block is shown in blue. In comparison to the CT-AEQs in figures 3 and 4, the compensation gain of the equalization filter is adjusted by the tap coefficients from a digital adaptation unit, which has greater precision and will also scale better. Note that the adaptation unit needs only to run at a fraction of the signal data rate because the variations of the channel characteristics, if any, are usually very slow.

III. General Test Strategies For Equalizers

Several general test strategies that are based either on loopback testing of the HSSL or on-chip eye quality measurement have been developed. These strategies, useful for either characterizing or testing the equalizers, are generally independent of the equalizer architectures.

A. Loopback Testing

Loopback testing is a low-cost solution for testing multi-Gbps HSSLs. Since the transmitter and the receiver are configured to test each other, the demand for high-performance testers is relaxed. The transmitter and the receiver can be connected through various internal or external loopback configurations that enable the testing of different aspects of the device. Internal loopback testing can be conducted prior to packaging and is, thus, applicable to wafer probes. However, since internal loopback connections do not cover IO pads and external channel degradation, which are primary jitter contributors [20], external loopback is often necessary. It was concluded in [21] that a purely digital internal loopback configuration is useful for fault diagnosis while external loopback testing is necessary for production testing.

External loopback is a common testing practice in the industry [22]-[25] for serial links. This loopback is configured by connecting the transmitter and the receiver with a loopback element on the load board. To mimic the channel effect, the loopback element introduces additional jitter, which is fully characterized prior to loopback testing. The amount of injected jitter can be made adjustable to improve the test and characterization quality [20]. An extensive discussion on the ATE requirements for facilitating loopback testing can be found in [26].

Using either internal or external loopback, the transmitter and the receiver, along with the integrated equalizers in them, are tested as a single, end-to-end system. The well-known fault-masking problem – caused by testing multiple components together as a single unit (for example, a strong transmitter could mask a weak receiver) – could result in a non-trivial test escape of individual components. In addition, it is difficult to identify the fault location and fault type once a failure is detected in a loopback setup. Therefore, the loopback approach is not effective for testing equalizers.

B. On-chip eye-opening monitor

Several approaches based on on-chip monitors have been proposed to characterize the eye openings at the output of an equalizer. The horizontal axis of an eye diagram represents the unit interval (UI) and the vertical axis is the voltage value. The eye can be characterized by first setting the reference timing and voltage values. The eye-opening monitor circuitry proposed in [27] reports the horizontal eye opening at the equalizer output in the form of an analog voltage signal. The monitor circuitry in [28] only measures the vertical eye opening.

A two-dimensional eye-opening monitor, proposed in [29], reports the effective eye opening by capturing the data transition characteristics with respect to several rectangular masks. The vertical opening of the mask is defined by two reference voltages and the horizontal opening is set by two phases of the sampling clock. They defined the mask error rate (MER), which is the number of data transitions that fall inside a given mask. The effective eye opening is the aggregated result of the masks given a MER threshold (e.g., MER=0). Since the errors on the left and the right sides of the mask are counted separately, their approach can effectively capture asymmetric eye diagrams, which is a more realistic scenario.

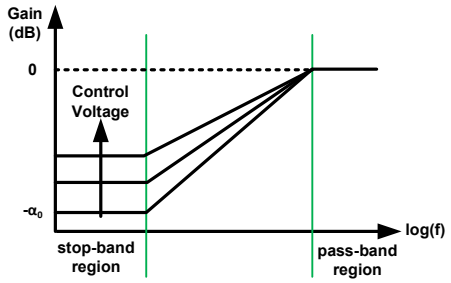

Figure 7: Frequency response of a tunable equalization filter [8]

An on-die waveform capture approach was proposed in [30] and its application to testing HSSL was reported in [31]. The on-chip oscilloscope measurement is made possible by sweeping the timing and voltage control and checking the error rate at each setting.

These on-chip monitors enable characterization and testing of the eye quality. Their output can be further used to automatically tune the equalizers' performance [27][29][32] in a closed-loop control configuration. For example, in [32], an on-chip ISI monitor is used to measure the response resulting from the channel and the equalizer on the fly. The measured channel response is then compared with the ideal response. The difference is then used by the control circuit to modify the equalizer parameters such that the deviation is minimized. In general, such self-tuning features incur non-trivial overhead that may not be acceptable in some applications.

IV. Testing Continuous-Time Adaptive Equalizers

The frequency response of a tunable equalization filter is shown in Figure 7. By adjusting the control voltage, this tunable filter can compensate for the channel loss up to α_0 dB, which is called the maximum compensation gain. The authors in [33] proposed a *two-tone testing* technique to detect the maximum compensation gain of an enhanced CT-AEQ. The test stimulus used is a two-sinusoidal-tone signal – one frequency of the two-tone signal, f_L, falls within the stop-band region and the other frequency, f_H, falls within the pass-band region. The root-mean-squared (RMS) value of the test response is measured at either point *X* or *Y* in Figure 4 with an RMS detector, which is the only DfT modification required for this test method.

Figure 8 illustrates the two-tone testing technique. The test stimulus with a fixed f_H magnitude and an increasing f_L magnitude is repeatedly applied, as shown in Figure 8(a). Such test stimuli mimic those signals with different relative

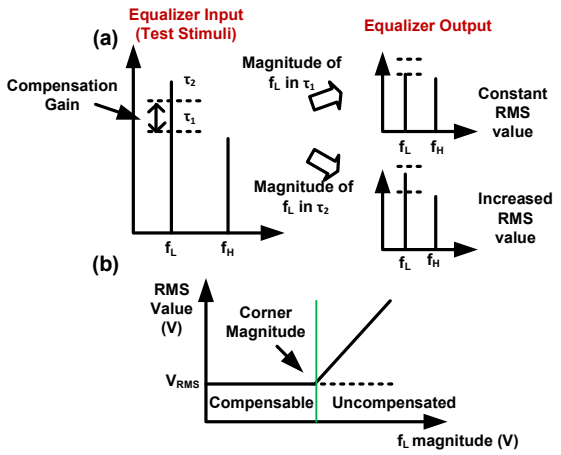

Figure 8: Illustration of the two-tone test technique [33]

high-frequency losses from the channel. If the relative magnitude difference of f_H and f_L is within the range of the maximum compensation gain, the RMS value of the equalizer output should remain a constant after the adaptation process converges. In contrast, if the magnitude difference is beyond the maximum compensation gain, the RMS value will be higher. The relationship between the output RMS value and the f_L's magnitude (with a fixed f_H magnitude) is shown in Figure 8(b), in which the corner magnitude of f_L reveals the information about the equalizer's maximum compensation gain. In practice, instead of a constant value, the RMS value increases as the f_L's magnitude increases – even in the compensable frequency range – because the equalization filter's gain slightly varies due to the change in the control voltage. However, the slope in the uncompensable frequency range is significantly greater than that in the compensable range. Thus, the corner magnitude and, in turn, the maximum compensation gain can be clearly identified in this RMS-vs-f_L magnitude plot.

The advantages of this testing technique include: 1) the test stimuli, which need not be stressed by different channels, can be easily generated and directly applied; 2) the test response is a DC signal and, thus, it can be easily measured; 3) the extra on-chip circuitry needed for supporting the technique incurs low area overhead and does not degrade the equalizer's performance.

V. Testing Digitally-Assisted Adaptive Equalizers

For DA-AEQs, we can employ the *digitally-assisted testing methodology* [34] for either go/no-go testing or for predicting circuit performance. This methodology yields similar or even better test quality at a lower cost and also is less intrusive compared to conventional testing methods. Methods using this testing principle have been successfully applied to characterize and test a DA-AEQ [35]-[37], characterize the VCO frequency [38], predict the post-calibration image-rejection ratio in an RF receiver [34], and

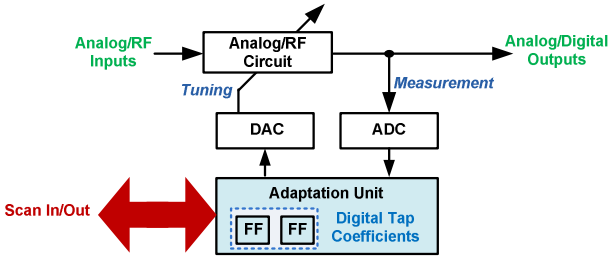

Figure 9: Digitally-assisted testing methodology [34]

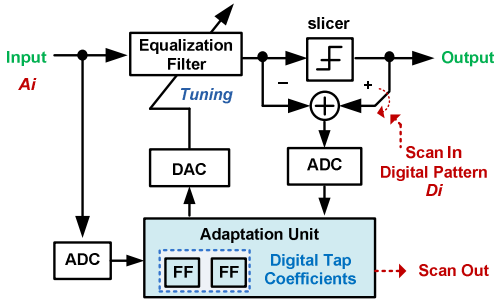

Figure 10: Testable design of a DA-AEQ [35]

predict the effective number of bits in a digitally-calibrated pipelined ADC [39]. In the following, we describe the principles of this testing methodology and its applications to characterizing and testing DA-AEQs.

A. Digitally-assisted analog testing

The conceptual diagram of the digitally-assisted analog testing methodology is shown in Figure 9. By controlling and observing the digital tap coefficients, the adaptation unit can provide digital accessibility to the analog/RF circuitry. We could, for example, apply pre-defined test stimuli from an arbitrary waveform generator (AWG) at the analog/RF input and analyze the convergence characteristics of the digital tap coefficients by observing them through scan. We could also stress the analog circuitry, with respect to different corners, by applying specific tap coefficient values through scan. Observing the circuit performance under such testing scenarios could characterize the equalizer and identify out-of-spec devices. Furthermore, we can control a subset of the digital tap coefficients using specific values and observe other coefficients for analysis and fault detection. In this method, the final values of the digital tap coefficients, after the adaptation process has converged, are considered as signatures for fault detection. To further enhance the fault detection capability, we can extract signatures from entire sequences of the tap-coefficient values during the adaptation process instead of simply using the final values. These signatures should contain more distinct information for differentiating the fault-free and the faulty circuits.

The DfT modifications required to support this testing methodology are only in the digital domain and are non-

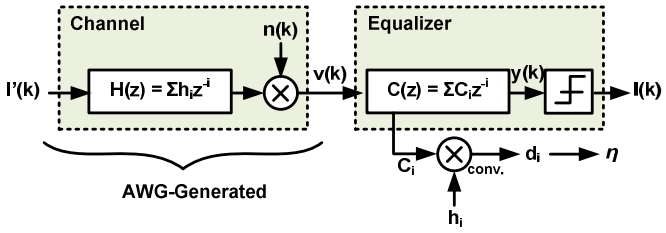

Figure 11: Model and concept of the digitally-assisted eye quality characterization method [35]

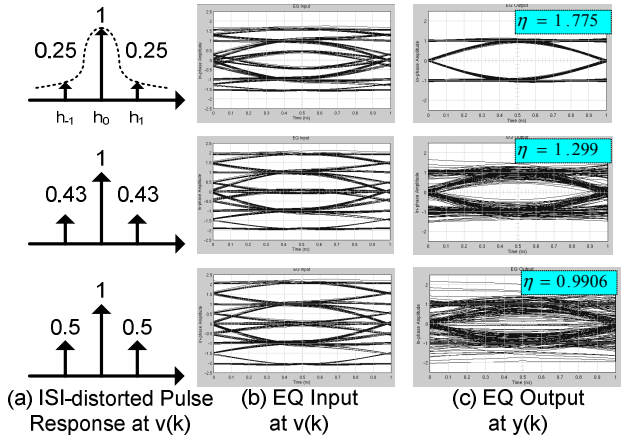

Figure 12: The eye diagrams and eye-opening index under various input stimuli [35]

invasive to the main signal path. The area overhead is very low and there is no performance degradation at all. In addition, cheaper digital test equipment is used in place of high precision analog testers. As the measurement is completely in the digital domain, it is much more repeatable and has greater noise immunity.

To support the application of the digitally-assisted test methodology to a DA-AEQ [35]-[37], two DfT modifications are needed (as shown in Figure 10). First, a scan structure and additional shadow registers are inserted so that the values of the tap coefficients can be controlled and observed through scan and can be captured without interfering with the adaptation process. In addition, the feedback signal into the adaption unit can be configured from either the CDR circuit or from external testers.

B. Digitally-assisted characterization

An eye quality characterization method based on analyzing the digital tap coefficients was proposed in [35]. The models and the concepts behind this method are shown in Figure 11. Based on the given ISI channel model $H(z) = \Sigma h_i z^{-i}$, where h_i's are the channel parameters, the AWG is programmed to generate and apply the ISI-distorted signal to the equalizer input for characterizing the equalizer's eye quality. If the change rate of the time-varying channel is relatively slow (which is often the case), the channel model parameters or h_i's can be modeled as constants for the characterization purpose. To test the equalizers under

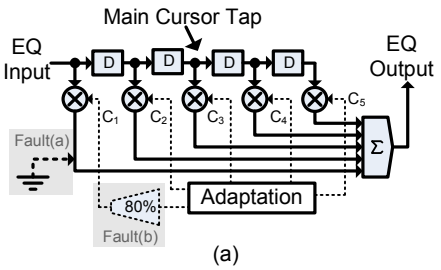

Figure 13: Fault detection example of a 5-tap DA-AEQ [35]

different channel characteristics, we can simply repeat the same characterization process with different ISI-distorted stimuli, each of which is with respect to a unique channel model. Under this assumption of slow-varying channel, the tap coefficients or C_i's in the adaptation unit will converge once the equalization is achieved. These final tap coefficients can be observed through scan by the ATE. Based on the channel parameters and the equalizer's tap coefficients, the DSP in the ATE constructs the combined equivalent model of the channel and the equalizer, by computing the convolution of the h_i's and C_i's. The combined model is expressed as $D(z) = \Sigma d_i z^{-i}$.

Based on the computed d_i's, an eye-opening index η defined in [40] is used to quantify the eye quality at the equalizer output without explicit access and measurement at the equalizer output:

$$\eta = \frac{2 \cdot \max|d_i|}{\sum_i |d_i|}$$

This eye-opening index η provides a quantitative measurement of the equalizer's performance. According to [40], the greater the η value, the more open the eye. If $\eta \leqq 1$, the eye at the equalizer output is considered closed, and the channel is not properly equalized as significant ISI still exists. If $1 < \eta \leqq 2$, the eye is open. Figure 12 illustrates exemplar eye diagrams and the corresponding eye-opening indices under various input stimuli.

C. Signature-based testing strategies

For production testing or debugging, we can configure the equalizer to break the feedback from the equalizer output as shown earlier in Figure 10. With this configuration, we can apply specific analog stimuli, A_i, at the equalizer's input, and corresponding digital stimuli, D_i, at the disconnected feedback point in Figure 10. In response to such stimuli, the tap coefficients of a fault-free device will converge to an expected set of values. Significant deviation from these fault-free values indicates the presence of defects or excessive variations. In [35] and [36], the tap coefficients *after* the adaptation process converges are scanned out and used for fault detection. These *steady-state* tap coefficients are referred to as *static signatures* of a DA-AEQ.

To illustrate this test strategy, consider a 5-tap feedforward equalizer shown in Figure 13. Two fault

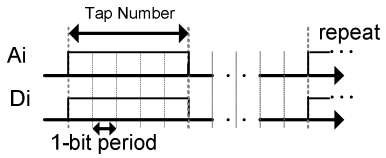

Figure 14: Test stimuli for the DA-AEQ in Figure 13 [35]

scenarios are shown to illustrate the fault detection capability of the static-signature-based testing method. This equalizer has two pre-cursor taps (with tap coefficients C_1 and C_2), one cursor tap (C_3), and two post-cursor taps (C_4 and C_5). In this illustration, we only consider single-fault scenarios. Fault (a) in Figure 13 is a broken pre-cursor tap (with coefficient C_1) that is always stuck-at 0. Fault (b) is a gain error of the DAC that occurred in the same precursor tap for which the DAC can only drive 80% of the expected coefficient value.

Figure 14 shows the test stimuli suggested in [35] for fault detection. The static signatures of the fault-free and the faulty circuits for faults (a) and (b) are shown in figures 15(a) and (b). If fault (a) is present, C_1 becomes 0, instead of 1, in the steady state. In addition, coefficients C_2 and C_5, after convergence, deviate significantly from the expected 0 value for the faulty circuit. If fault (b) is present, although the correct tap coefficient C_1 will be observed (i.e. $C_1 = 1$), the presence of other tap coefficients that are attempting to jointly and adaptively minimize the errors caused by the fault, would result in erroneous values after convergence. In response to the specific test stimuli used, shown in Figure 14, the fault-free and faulty C_2 and C_5 values are significantly different. These two simple examples illustrate the static-signature-based test strategy. Note that it is also possible to diagnose the fault location and the fault type [35] under the same configuration, but it would require the application of special diagnostic test stimuli.

While the types of test stimuli illustrated in Figure 14 can effectively detect most faults in FFEs, they fail to detect some of the hard-to-detect faults for complex DFEs [37]. To enhance fault detection, an alternative test pattern template, shown in Figure 16, was developed in [37]. For the analog stimuli A_i, instead of having a constant amplitude for a period of cycle count equal to the number of taps in the equalizer, each cycle i has a unique amplitude h_i. It was demonstrated empirically that such test stimuli stimulate the equalizer in a more dynamic fashion and they can detect some of the hard-to-detect faults missed by the types of stimuli shown in Figure 14.

It was also illustrated in [37] that the static signatures (i.e. the final tap coefficient values after the adaptation process converges) may fail to detect some faults. It was observed that for many of those missed faults, the tap coefficients have convergence characteristics distinct from those of the fault-free circuit. Therefore, instead of just examining the final values, periodically sampling and accumulating the tap coefficient during the adaptation process would enhance the fault detection capability [37].

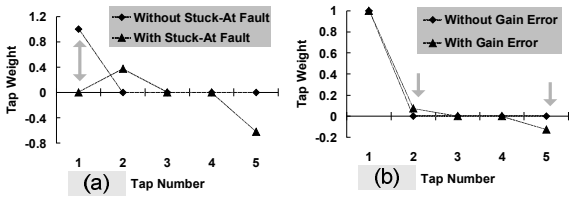

Figure 15: Static signature of Figure 13's faults (a) and (b) using test stimuli in Figure 14 [35]

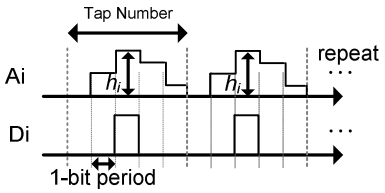

Figure 16: Test stimuli for the DA-AEQ in Figure 13 [37]

Such accumulated values are referred to as the *dynamic signatures*. Shadow registers need to be added to enable the observation and accumulation of the tap coefficients during the adaptation process without interruption. It has been shown in [37] that combining the use of both static and dynamic signatures results in the best test quality.

The signature values and their fault detection capabilities are highly dependent upon the test stimuli. The stimuli should be designed to maximize the signature differences between the fault-free and the faulty circuits. One potential optimization problem is to derive the best combination of h_i's for the test template shown in Figure 16 that can maximize the differences between the fault-free and the faulty signatures. An automatic test pattern generator can be developed based on this optimization problem.

VI. SUMMARY

This paper summarizes several strategies for testing the adaptive equalizer in a high-speed serial link. For general equalizers, on-die waveform capture or eye-opening monitors can be used to test the equalization quality. However, such a strategy incurs significant area overhead. For continuous-time adaptive equalizers, a two-tone testing method can be applied to test the equalizer's maximum compensation gain. For digitally-assisted adaptive equalizers, the equalization quality can be characterized by an eye-opening index. In addition, we can apply non-functional stimuli and observe digital tap coefficients as the signatures for fault detection. This digitally-assisted testing strategy incurs minor area overhead and helps reduce the test cost.

To further minimize the test costs, future strategies for testing adaptive equalizers should utilize existing on-chip resources and migrate the analog domain measurements to the cheaper and more robust digital domain. Because adaptive equalizer designs are increasingly using digitally-assisted styles, using the signature-based, digitally-assisted methods for both circuit characterization and production

testing are promising for both test quality improvement and cost reduction.

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