Gain and Equalization Adaptation to Optimize the Vertical Eye Opening in a Wireline Receiver

Dustin Dunwell and Anthony Chan Carusone
Department of Electrical and Computer Engineering
University of Toronto, Toronto, Ontario, Canada

***Abstract*—A strategy for the adaptation of an equalizer and variable gain amplifier is presented. Both control signals are generated by examining the probability density function (PDF) of the received data, which is obtained from the DC output of an additional analog sampler at the equalizer output. This technique works to minimize the spreading of the PDF of the received signal while adding only minimal complexity and power consumption to the receiver design. The technique is demonstrated in a wireline receiver fabricated in 65-nm CMOS technology. Measured results show that the adaptation scheme functions correctly over both coax and PCB channels of varying lengths and at speeds ranging from 2 to 10 Gb/s.**

I. Introduction

Frequency-dependent channel impairments such as dielectric loss and skin-effect can severely limit a wireline receiver's ability to operate at high-speeds. As a result, many receivers incorporate an analog front-end (AFE) which includes some form of gain-control and equalization to help compensate for these impairments. The ability to intelligently control the AFE blocks in a way that optimizes receiver speed, sensitivity, dynamic range and noise performance, is non-trivial. In particular, control signals for the variable-gain amplifier (VGA) and equalizer (EQ) should be generated automatically and should be able to adapt to a variety of channel conditions.

The EQ control signal can be generated by minimizing the difference between the high-frequency content of the EQ and slicer outputs [1]. While this technique can also include low-frequency gain control [2], the necessary analog filters can be difficult to design and can consume a great deal of chip area. Furthermore, this technique offers no guarantee that the resulting EQ control achieves optimal bit error rate (BER) performance.

In order to optimize the BER, it is necessary to monitor the eye opening at the slicer (or ADC) input. This can be performed by using additional slicers with either a variable decision threshold for vertical eye monitoring [3], variable sampling time for horizontal eye monitoring [4], or both variable threshold and sampling time for two-dimensional eye monitoring [5]. This technique is used to obtain complete eye opening data and BER contours in [6] and is shown in Fig. 1. By comparing the resulting BER to some target value, the adaptation algorithm is able to generate analog control signals for the taps of the decision feedback equalizer. This technique can be very slow to converge and requires a significant amount of additional hardware including a high-speed XOR gate and error counter as well as multiple clocks with finely tunable phases. It also does not incorporate any gain control into the AFE, limiting the dynamic range of the receiver.

This paper introduces a different technique for automatic adaptation of both the gain and equalizer control signals. Rather than targeting a specific minimum BER as in [6], this algorithm tightens the distribution of the received signal amplitude and centers it at a specific level to optimize the receiver's dynamic range. This technique requires only a single sampling phase at the center of the received eye and is therefore able to operate independently of the CDR.

It also requires only minimal hardware overhead as it does not use a high-speed XOR gate to count errors but instead uses only the DC output voltage of one additional comparator to determine the appropriate EQ and VGA control signals. These factors make this adaptation strategy attractive not only as an efficient means of optimizing AFE settings, but also as a way of quickly and easily detecting faults and predicting circuit performance in a production testing environment, which can otherwise be costly and time-consuming [7].

II. PDF-Based Adaptation

A sequence of random binary data can be represented by a random process X. If this data is generated by an ideal, noise-free binary transmitter and sampled at the baud rate, T_b, and at phase τ, corresponding to the midpoint of each bit then each sample is a random variable represented by

$$X_\tau(k) = X(kT_b + \tau) \tag{1}$$

where k is an integer. In the absence of noise or other non-idealities in the transmitter, $X_\tau(k)$ will be constrained to two

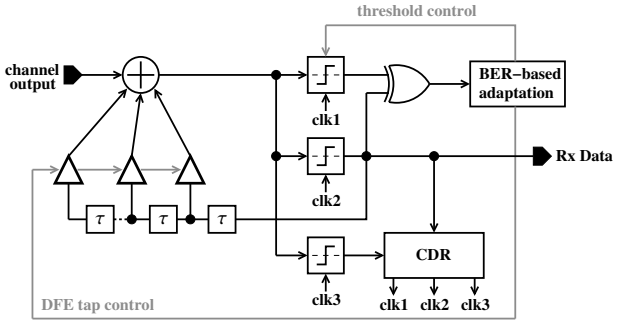

Fig. 1. Digital BER-based adaptation used to optimize DFE tap settings [6].

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possible states: logic high, V_H, and logic low, V_L, which are equally probable

$$P(X_\tau(k) = V_L) = P(X_\tau(k) = V_H) = 0.5 \quad (2)$$

and whose values are defined by the voltage swing constraints inherent to the transmitter.

The result is the transmitted eye diagram and the probability density function (PDF) of X_τ, denoted by $f_{X_\tau}(x)$, in Fig. 2(a). Here the PDF is confined to two impulse functions corresponding to V_H and V_L.

After passing through a channel, the received eye diagram will show intersymbol interference (ISI) in the form of jitter and a spreading of the received signal amplitudes due to the frequency-dependent losses of the channel, reflections at connection points, and bandlimited stages in the receiver's AFE. A new random variable, $Y_{\tau'}(k)$, is obtained by sampling the received data at a phase corresponding to the midpoint of each received bit, given by τ'. The PDF of this variable is given by $f_{Y_{\tau'}}(x)$ and is illustrated in Fig. 2(b).

The received data is no longer exclusively constrained to two specific voltage levels but is instead spread over a range of values by the introduced ISI and noise. Hence, the PDF of the received data is not represented by impulse functions, but is instead distributed around new high and low levels, V_{RH} and V_{RL}. A detailed derivation of $f_{Y_{\tau'}}(x)$ in terms of the transmitter and channel characteristics can be found in [8].

The premise of this work is to monitor the PDF of the received data and adjust gain and high-frequency peaking controls in an AFE to return it to the ideal PDF of the transmitted signal in Fig. 2(a).

A. Measuring the Received PDF

If a slicer's threshold voltage is moved away from the center of the received eye, the slicer will begin to generate errors. These errors can easily be detected by passing this slicer output, along with the fixed-threshold slicer output from the main data path, through an XOR gate. Counting the number of errors generated by each threshold step can be used to generate BER contours, which can then be used to select an optimum slicer threshold [9] or optimize equalizer tap coefficients [6].

In this work this process is simplified by observing that as the threshold voltage is swept, the DC output of the slicer,

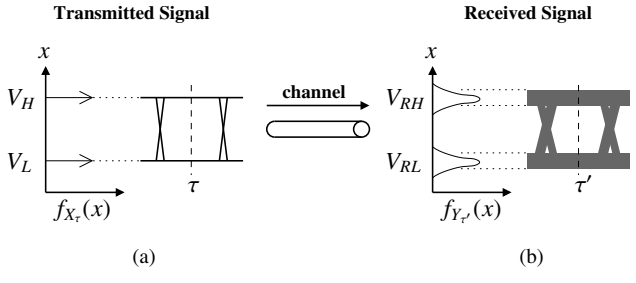

Fig. 2. A noiseless transmitted signal (a) experiences ISI in a frequency-dependent channel, which results in spreading of the PDF of the received signal (b).

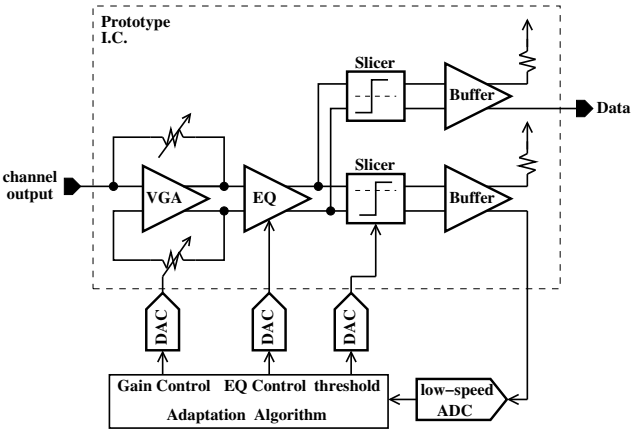

Fig. 3. A block diagram of the VGA and EQ adaptation performed in this work. The low-speed ADC digitizes the DC (average) output of the offset slicer. This information is used to minimize the spread in the received PDF and to appropriately center it. Measurements use off-chip ADC and DACs.

V_{out}, is proportional to the cumulative distribution function (CDF) of the input signal. Since the CDF of the received signal yields information equivalent to a BER contour, it is possible to replace the high-speed XOR gate and error counter with a simple low-pass filter. The test setup used to demonstrate this operation is shown in Fig. 3. The fabricated chip is a 10 Gb/s binary wireline receiver in 65-nm CMOS. The output of the variable-threshold slicer is taken off-chip where simple Matlab control logic was used to generate the gain, equalizer and threshold controls.

The received signal PDF is equal to the slope of the CDF obtained by sweeping the auxiliary sampler threshold, as illustrated in Fig. 4. The equalizer peaking is chosen to maximize the slope of the CDF (peak value of the PDF).

B. Equalizer's Effect on the PDF

The EQ implemented in this receiver is a linear, split-path equalizer similar to that introduced in [10], which creates high-frequency peaking by decreasing low-frequency gain. Simulation results show that the equalizer is capable of producing

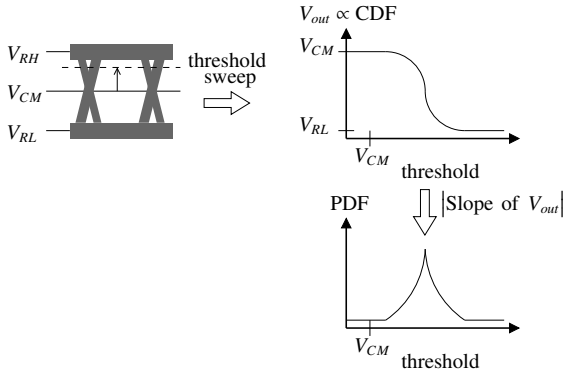

Fig. 4. The DC output of the slicer drops as V_{th} is increased. The magnitude of the slope of this decline is related to the PDF of the received data.

high-frequency peaking of up to 8 dB in 65-nm CMOS.

To illustrate the EQ adaptation, Fig. 5 shows measured results taken from a prototype binary receiver fabricated in 65-nm CMOS. In Fig. 5(a) the DC slicer output voltage is used to infer the percentage of time that the slicer spends at logic high (V_{RH}), which is equivalent to the CDF of the received random variable. As the threshold level is increased, this percentage increases from 50% when the threshold is in the center of the received eye, to 100% when the threshold is outside the eye.

When alternating data is transmitted, a sharp rise in the CDF is observed near a threshold level of 200 mV because there is no ISI present. Conversely, the presence of ISI with 2^7-1 PRBS data means a more gradual change is observed in the CDF. This effect is even more apparent in Fig. 5(b) where the PDFs of the two received patterns are compared.

The adaptation algorithm was tested when receiving a 2^7-1, 2 Gb/s PRBS signal, transmitted across a 10 m BNC coaxial cable. Fig. 6(a) shows the PDF of the logic high level of the received data for five different equalizer peaking settings. As the EQ control voltage V_{eq} is increased, the low-frequency content of the received signal is attenuated, meaning that the peak slope of V_{out} occurs at incrementally lower threshold levels. At the same time, the resulting emphasis of the high-frequency content helps to reduce ISI, narrowing the PDF of the received data and increasing its peak value. In this case, the adaptation algorithm selects V_{eq} = 0.65 V to be the best equalizer setting because it produces the highest peak in the PDF (i.e. the highest slope in the CDF).

Since adjusting the settings of a peaking EQ effects the signal amplitude, this adaptation is performed before the VGA adaptation, which is described in the following section.

C. VGA's Effect on the PDF

The VGA can help keep the signal amplitude within some specified range throughout the receiver signal path in order to ensure the best possible dynamic range in the AFE. Fortunately, the amplitude of the signal at the equalizer output can be readily observed using the additional slicer. As the gain of the AFE is increased or decreased, the received signal PDF is observed as described in the previouse section and its peak is used to indicate the signal amplitude. For the 65-nm CMOS receiver in this work, it was determined that the voltage swing of the equalizer output eye should not exceed 100 mV (peak-to-peak per side) in order to avoid distortion.

In this work, the VGA gain decreases as V_{gain} is increased [11]. From the measured results in Fig. 6(b) we see that the peak of the PDF shifts to higher voltages for higher preamplifier gain settings. In this case the adaptation algorithm chooses a V_{gain} setting of 1.2 V since this places the peak of the PDF as close as possible to the target value of 100 mV.

By continuously repeating the EQ and then VGA adaptation techniques, it is possible to maintain optimal settings for the AFE as channel conditions vary over time. Also, since both the equalization and gain control settings are determined from the same set of measured DC output voltages, no additional filters, slicers or other high-speed circuitry needs to be added to the receiver to perform the VGA adaptation.

III. Measurement Results

The fabricated receiver occupies approximately 0.23 mm^2 (excluding pad frame) and has a measured power consumption of 252 mA from a 1.2 V supply. The AFE accounts for 67.1 mA of this total, with the rest being used in the output drivers and current-mode logic of the digital back end. A die photo of the fabricated receiver is shown in Fig. 7. All measurements were made on-wafer and alignment of the clock and data signals was performed manually off-chip.

To demonstrate the robustness of the adaptation algorithm, measurements were made on a variety of channel types and lengths. Fig. 8 compares the measured loss of each channel to the equalizer peaking and preamplifier gain settings chosen by the adaptation algorithm. All tests were performed using length 2^7-1 PRBS data at a speed of 4 Gb/s for the PCB tests

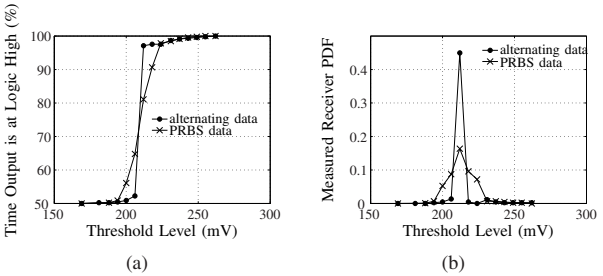

Fig. 5. Measured DC output voltage is proportional to (a) the percentage of time that the output spends at logic high. The slope of this curve is then used to create (b) the PDF of the the received signal.

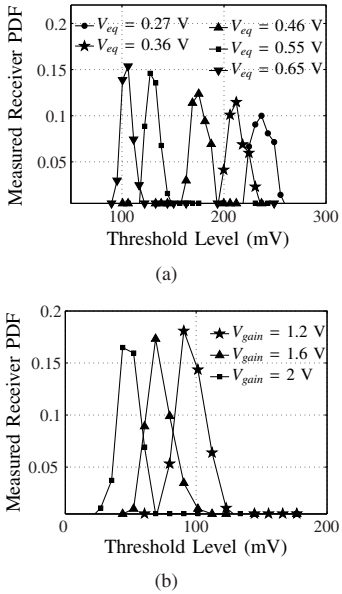

Fig. 6. Measurement results show that (a) increasing EQ peaking narrows the PDF and increases its peak value and that (b) increasing VGA gain moves this peak towards the target maximum threshold level of 100 mV.

and 10 Gb/s for the coaxial cable tests (with the exception of the 30 m cable, where the speed was reduced to 5 Gb/s to achieve an open received eye).

In both the PCB and coax cases, the adaptation algorithm responds to the increase in channel losses by increasing equalizer peaking and preamplifier gain. This intuitive result was further verified by examining the receiver's output eye diagram after adaptation had taken place. In all cases the resulting eyes showed error free operation. One example of such an eye is shown in Fig. 9 for a 10 Gb/s signal sent across a 10 m coaxial cable.

IV. Conclusion

The ability to generate and automatically adapt the control signals of a VGA and EQ in a receiver's front end is essential in order to maintain optimal receiver operation. The adaptation method presented in this work is able to generate these signals by adding only minimal hardware overhead to the receiver. By observing the DC output of a single additional slicer with variable decision threshold, a PDF of the received data is obtained, which contains the information necessary to intelligently adapt the control signals to a variety of channel conditions. By minimizing the spreading of the PDF caused by ISI and maximizing the amplitude of the received signal within the limits of linear operation, the adaptation scheme ensures that the vertical opening of the received eye is optimized.

To demonstrate its effectiveness, the technique was used to adapt the control settings of a binary receiver fabricated in 65-nm CMOS technology. Measured results show that the adaptation scheme operates correctly when used with a variety of channel types and lengths, and at speeds ranging from 2 to 10 Gb/s.

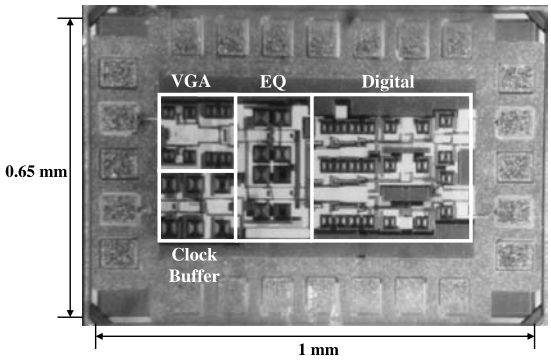

Fig. 7. Die photo of the receiver fabricated in 65-nm CMOS.

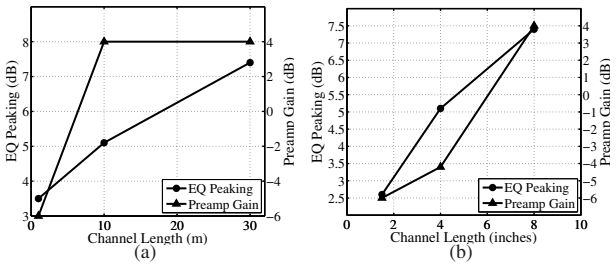

Fig. 8. Adaptation algorithm automatically increases equalizer peaking and preamplifier gain to compensate for increasing channel losses across (a) coaxial cables and (b) PCB traces.

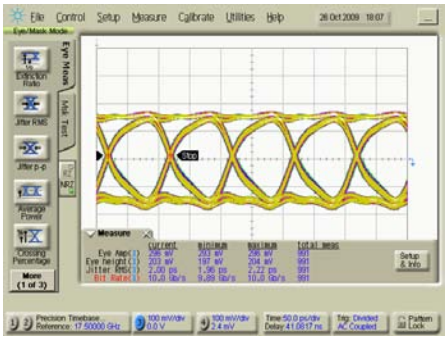

Fig. 9. Eye diagram of the receiver output after automatic adaptation when receiving 10 Gb/s data sent across a 10 m coaxial cable.

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