Test and Characterization of High-Speed Circuits

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Abstract: Test, validation and characterization of high-speed circuits is a becoming a complex issue due to increase in circuit marginality, higher fallout, and more complex test solutions. The issue is compounded by the complex interactions between packaged components; interconnect design and customer board designs. This session will address the challenges in characterizing high-speed circuits including PLLs and SERDES. It describes test methodologies to overcome those challenges using industrial test cases.

"Characterization Of The Digital PLLs On An 8-Core Microprocessor Using Electrical And Optical Techniques"
By: Kevin Stawiasz, Keith Jenkins, Peilin Song*, Franco Stellari, Jose Tierno, Alexander Rylakov and Daniel Friedman (IBM)

"Challenges in High Volume Manufacturing Test and System Correlation for High Speed IO"
By: Anne Meixner* (Intel Corporation)

"High-Speed SerDes Characterization"
By: Dongwoo Hong* and Matthew Isaacs (Broadcom)

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