External Loopback Testing on High Speed Serial Interface

Lee, Shen Shen
Altera Corporation (M) Sdn Bhd, Plot 6, Bayan Lepas Technoplex, Medan Bayan Lepas, Penang
E-mail: shslee@altera.com

Abstract

Testing for high speed links have been, and will continue to be, primarily based on checking their conformance to the specifications and performance testing due to the lack of industry analog fault models. However, with the increased diversity of features to support new transceiver protocols, specification testing on high speed serial interface (HSSI) is becoming increasingly difficult and costly. Techniques like design-for-testability (DFT) have been applied to overcome some of these challenges.

In this paper, the author presents case studies of one of the most common DFT techniques for HSSI testing, namely, external loopback. Firstly, the different flavors of loopback available in industry are briefly mentioned together with their usage. Next, the need for external loopback engagement in HSSI test strategy is described. This is then followed by the explanation of the external loopback circuitry on device-under-test (DUT) card and test methods for supporting HSSI buffer level testing that are implemented on transceiver based FPGA product. This paper also provides summary from silicon experiences and directions for future improvement.

Keywords

External loopback, HSSI, PMA, DFT, AC-coupling

1. Introduction

Digital testing is far more advanced compared to analog and mixed signal testing. This is generally contributed by the widespread acceptance of the stuck-at-fault model and output logic level monitoring as the primary paradigm. Analog and mixed signal testing on the other hand has no general-purpose DFT technique as comparable to digital's scan-based design and testing. Three main hurdles of this matter are lack of an industry accepted analog fault model, diversity of analog stimulus and response types and lack of synthesis and layout automation for analog functional design [1].

Today, specification or parameter-based high speed serial interface (HSSI) testing to meet DPM (defective parts per million) goals is common in the industry [2] [3]. Figure 1 illustrates the specification based strategy whereby the specification or parameter based data collected from production test is compared to design specification to pass or fail the device. A typical test list for HSSI could include duty-cycle distortion, bit error rate testing (BERT), receiver sensitivity testing, DC parameter testing and so on. However, direct measurements for these parameters in high-volume manufacturing (HVM) are usually very costly due to the need for sophisticated test equipment and long test time. This is not a preferred solution for companies to achieve the desired profitability and still deliver quality unit screening.

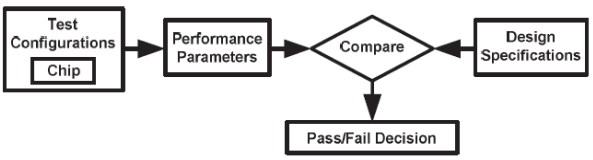

Figure 1: Specification-based test strategy.

Furthermore, according to ITRS 2011 roadmap, high frequency multiple Gbps/GHz I/O technology continues to show significant growth in speed and port count in computing, networking and as well as consumer applications, beyond its true serial communication origin [4]. In high volume computing and networking application, the Gbps/GHz interface is still keeping its exponential pace but with a reduced slope in logarithmic scale as shown in Figure 2. High port count aspect is contributed by the enablement of massive integration into large ASIC and SoC devices with the availability of low voltage CMOS technologies and low output voltage swings. Up to 200 pairs of 10Gbps backplane style SerDes are found in some applications, even though for a large percentage of applications, the port count will be limited to 32 or less. With the current trend of speed growth and port count increase, a cost efficient ATE or DFT solution that can concurrently test all serial ports is essential for production and clearly specification testing is out of the consideration due to long measurement time for the increased port count and requirement for expensive high speed channel pin card level integration support from ATE supplier [4].

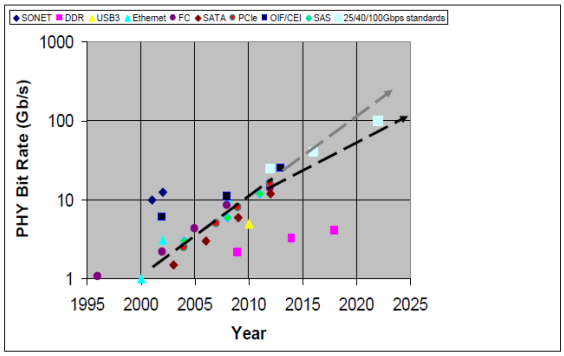

Figure 2: High speed interface trend.

Loopback testing is among the most popular test strategy for devices that incorporates both transmitters and receivers. This low-cost testing strategy incurs minor to no hardware overhead and alleviates the requirement of high-end AMS testers. Besides, it is capable to test all the high speed channels at the same time. However, as the entire

transceiver is tested as a single, end-to-end unit, the test quality might be compromised due to fault masking among interacting blocks [3]. This paper focuses on one of the most common DFT techniques for HSSI testing; namely, AC-coupled external loopback.

This paper is organized as follows. Section 2 describes briefly the different flavor of loopbacks available in industry together with their usage. The need of external loopback engagement, board setup and verification as well as buffer level test methodology are presented in Section 3. Silicon experiences learnt from the adoption of external loopback strategy on transceiver based FPGA product and directions for future improvement are described in Section 4. Section 5 provides the summary of what has been discussed in this paper.

2. Loopback connections and their usage

Loopback testing is a low-cost solution for testing HSSI as the transceiver pairs are configured to test each other thus the requirement for high-performance testers is alleviated. As shown in Figure 3 below, during the loopback testing, the DUT is configured into several configurations, each of which basically routes the output of one component of the pair (e.g., the transmitter) to the input of the other component of the pair (e.g., the receiver). There are three commonly used on-die loopback paths as depicted in Figure 3 which includes:

1. Parallel Loopback
2. Reverse Serial Diagnostic Loopback
3. Serial Loopback

Parallel loopback path is normally used to verify digital sub-components in the Physical Coding Sublayer (PCS) block without engaging the Physical Medium Attachment (PMA) block which consists of analog and mixed signal block. Reverse serial diagnostic loopback is used for device characterization with external instrument usage. As for serial loopback path, it is usually engaged in HVM tests. The serial loopback can be used for both wafer sort and packaged unit testing. This path is extremely useful when it comes to at-speed testing of the HSSI which utilizes the Pseudo Random Binary Sequence (PRBS) generator and verifier to perform system level test. However, this loopback does not work well for packaged unit tests as it masked off the signal integrity caused by the buffers and package trace. This is usually compensated by adding jitter guard band which is acquired from characterization bench correlation into the max frequency value obtained when running the HSSI at-speed.

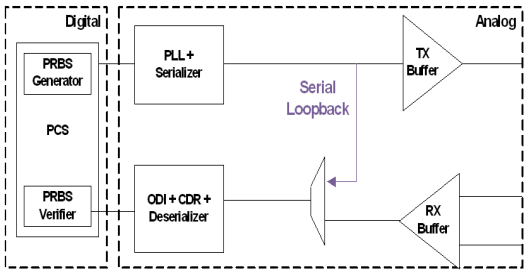

Figure 3: Loopback configuration.

The off-chip external loopback path shown in Figure 3 is configured in AC coupled mode. Although DC coupling is still common, AC coupling is becoming favored way to connect high frequency (HF) signals because it provides voltage ISOLATION to allow the transmitter and the receiver to each operate in their preferred voltage range [5]. Besides, AC coupling has been widely adopted in high speed I/O protocol such as PCI-E, Interlaken, GPON, CPRI, XAUI and the list continues. This paper focuses on the AC coupling external loopback strategy as it covers majority of the protocols available in the market.

3. External loopback test strategy

The following subsections are presented as follows. Section 3.1 describes the need to start external loopback strategy evaluation in our test strategy for buffer level testing. Section 3.2 provides brief description on the external loopback board setup and verification. Section 3.3 covers the test methodology for receiver and transmitter build-up circuitries such as AC JTAG board diagnostic test, the receiver sensitivity test, PCIE receiver detection test, PCIE signal detection test and pin leakage test for receiver and transmitter differential pins.

3.1. The need of external loopback engagement

Prior to external loopback engagement, performance and parameter based testing on HSSI are common in the industry. By referring to Figure 4, performance based testing such as at-speed testing of blocks before the transmitter and receiver buffer like clock data recovery (CDR), phase locked loop (PLL), high speed clock network, deserializer, serializer and so on are doable with the existence of serial loopback path in the HSSI circuitry. By engaging the PRBS generator and PRBS verifier in PCS block, system level test method can be executed across these blocks to extract the performance data for these blocks. Parameter based testing, on the other hand, is performed using DC parametric test method whereby parametric measurement unit (PMU) in automated test equipment (ATE) is heavily rely on. This test strategy looks into every sub-component in transmitter and receiver buffer block and performs necessary voltage or current measurement on these circuitries. Example of tests that are parameter based testing are transmitter's differential output voltage measurement, termination resistor measurement, minimum differential input voltage (VID) measurement and the list goes on. Both performance and parameter based testing are critical to ensure there is no circuitry defect and customer specification is being guaranteed.

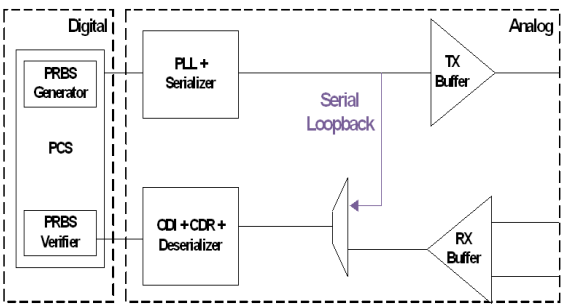

Figure 4: Serial loopback configuration.

By looking into these two strategies, performance based testing is capable of covering more blocks in a single test due to the engagement of system level test method. However, for parameter based testing, only a single sub-circuitry of the buffer can be targeted in one test, thus, more tests are required to cover the whole buffer alone. Furthermore, these tests usually have high test time due to extensive usage of PMU and are very sensitive to tester setup and PMU accuracy. System level test method is not possible for this buffer testing due to tester limitation whereby there is no built-in pattern generator and pattern verifier capability to drive and monitor the data off-chip. Along the same line, it is difficult for these parameter based tests to directly correlate with customer issues as the blocks are not being tested functionally but rather being targeted for stuck-at-testing.

External loopback is now a commonly used strategy in the test industry [2] whereby the transmitter is connected to receiver on board either through AC or DC coupled link. With this, it enables system level testing to be performed as one can engage the on-chip pattern generator and verifier. This also allows the buffer tests to run up to certain speed which depends on board design and is able to test all the high speed I/O at the same time. Unlike DC parametric testing, the AC components incorporated in the buffer can be stressed for testing when run at speed. Usage of PMU can also be kept at minimum as the driving or monitoring of signal is now handled on-chip with the data propagates from transmitter and back to receiver. Moreover, it also simplifies buffer test method as it reflects closer to customer application. This then provides our customers with a stronger confidence in our test screening quality since our test platform is similar with their usage and it also eases the correlation work on test with failures seen on customer setup. With all the advantages mentioned above, there is definitely a strong value to start exploring the usage of external loopback in our test environment.

3.2. External loopback board setup and verification

The DUT board is designed to include the external loopback connection as shown in Figure 5 below. For PCI-E protocol, AC coupling capacitor of a value between 75nF and 200nF can be used for AC-coupled link operation [6]. By placing an isolation resistor (eg 1~5 kOhm) that connects to tester connector provides a path to PMU engagement without affecting the high frequency pin [5]. This board setup includes two 100nF capacitors and four 1k Ohm resistors for each TX to RX external loopback connection. In the analysis described by this paper, the data rate is fixed to 2Gbps.

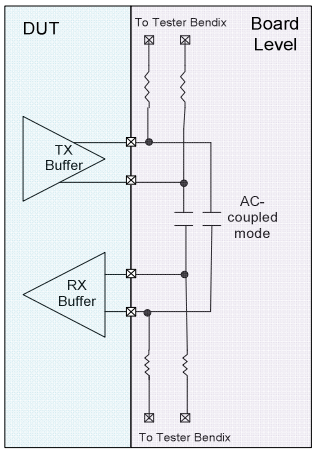

Figure 5: External loopback connection on DUT card.

Board verification has been conducted to ensure the loopback connectivity and components in place are working as what is expected. This is performed by sending a PRBS-9 pattern at 2Gbps with 300mV VOD (differential output voltage) from transmitter through the external loopback path. The signal node on the receiver pad is being observed and as shown in Figure 6, clean signals are monitored on receiver differential pins.

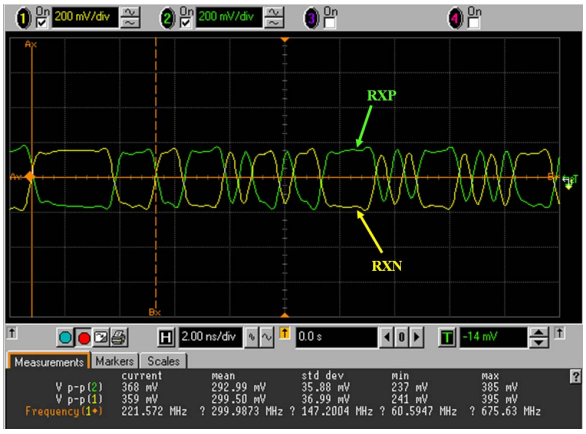

Figure 6: Signal scoping during board verification.

3.3. Buffer level test methods

3.3.1. Board diagnostic test using IEEE 1149.6 standard boundary scan

The IEEE 1149.6 Standard was developed to address the requirements of boundary-scan testing of AC-coupled, differential nets [7] [8]. While testing this feature functionally, it indirectly performs board diagnostic on the external loopback paths. This test is critical as it ensures the board to be in good condition before carrying out the production testing. Figure 7 shows the top level implementation of IEEE 1149.6 Standard on both transmitter and receiver.

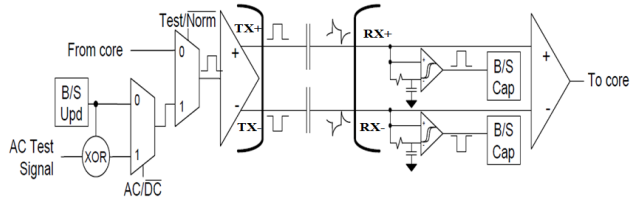

Figure 7: Implementation of 1149.6 standard.

The most critical part of the IEEE 1149.6 Standard is the test receiver circuitry that responsible for correctly detecting transmitted logic levels and edges. Figure 8 shows a basic block diagram of the test receiver that has both AC and DC capability [9]. The receiver supports the AC test capability and IEEE 1149.1 Standard level-detecting interconnect test (DC EXTEST) instruction. When configured in AC test capability, the receiver responds to the output of the low pass filter as shown in node B connection of Figure 8 below. While in DC capability, the circuitry turns off the transition detection and has the receiver responds to voltage levels (Vbias) by controlling the analog switch to DC mode.

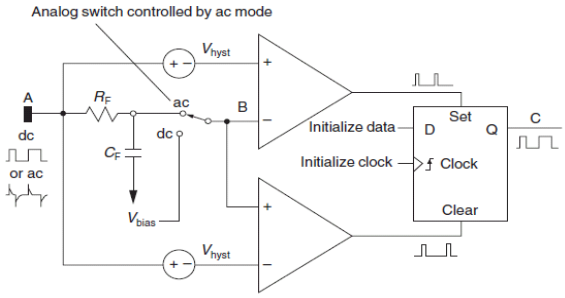

Figure 8: Test receiver.

When engaged in AC mode during EXTEST PULSE or EXTEST TRAIN instruction, the self-referencing hysteretic comparator is used to capture the signal transition. The comparator receives the test signal input and a delayed version of the test signal input that has passed through the low-pass filter. As when engaged in DC EXTEST instruction, the use of internal bias voltage, Vbias, sets the mission receiver's common mode point as a static reference for the test receivers. In the execution of these instructions, the comparator outputs set and clear the flip-flop on receipt of rising and failing edges.

These three instructions are called upon the boundary scan test run. DC EXTEST instruction is needed as it has the capability to filter out fault related to capacitor short which causes TX+ shorted to RX+ or TX- shorted to RX-. EXTEST PULSE and EXTEST TRAIN are pretty similar except that in EXTEST TRAIN instruction, the test logic generates data transition during every TCK failing edge while in run-test/idle state of JTAG tap state machine [9]. Both instructions are utilized for test coverage purposes and they are meant to detect any open faults between TX+ and RX+ or TX- and RX-.

3.3.2. Testing of receiver sensitivity

Receiver sensitivity testing scheme involves the usage of both the transmitter and receiver buffer as illustrated in Figure 9. This test is required to validate the minimum differential input voltage (VID) that the receiver can run and at the same time verify the transmitter for any stuck at fault along the data propagation path as well as its main driver's current sources. By changing the bias current in the transmitter buffer that generates the VOD, it modifies the input voltage level of the looped-back signal to receiver. The PRBS generator is utilized on the transmitter side to send PRBS data with a fixed VOD through the loopback path and the data received is validated by the PRBS verifier that resides in the receiver path. This fixed VOD value is based on the min VID specification supported by the receiver plus some margin that is based on empirical data collections to cater for the inaccuracy of the TX bias current, inaccuracy of termination resistors, IR drop along the external loopback path and so on.

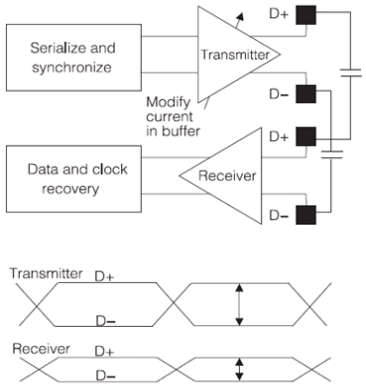

Figure 9: Receiver sensitivity testing.

3.3.3. Testing of detection modes

Receiver detection and signal threshold detection circuitry are legacy features of PCI-E protocol. These two are important features to test due to circuit sensitivity and requirement for system usage.

3.3.3.1. Receiver detection

The detect block in transmitter side is required to detect the presence or absence of a receiver at the other end of the link after coming out of reset or power-on. The feature exploits the fact that an un-terminated, ac-coupled transmission line will have a very different charge time when the line is terminated versus open. Each PCI-E transmitter, at the commencement of linkup, produces a low-frequency "ping" on each of the differential TX outputs. The transmitter includes a simple detection circuit to monitor the line response to this ping.

With no receiver attached, the edge rate (and amplitude) of the line change is much higher than when a receiver is present. Because the PCI-E specification has a defined range of coupling capacitance and the receiver termination, a distinct, detectable time constant range defines when a receiver is present or not [6]. Figure 10 depicts the pull-up charge up speed is fast due to the small RC decay time while Figure 11 shows the connected receiver on the other end and its charge up time that is significantly slower due to the presence of the termination resistance [10].

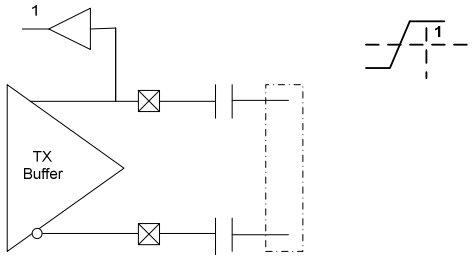

Figure 10: Response of RC time constant without a receiver attached.

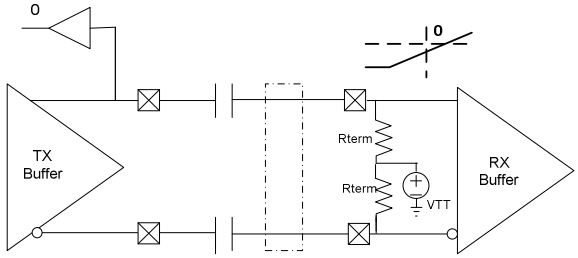

Figure 11: Response of RC time constant with a receiver attached.

With the integration of AC coupling external loopback on DUT card, the setup is already engaged as per what is needed by the feature, thus, by only controlling the RX termination, receiver absence and presence case can be tested. To emulate receiver absence case, RX termination is set to tri-state in the test and to emulate receiver presence case, the RX termination is enabled.

3.3.3.2 Signal threshold detection circuitry

This feature senses if the signal level presents at the receiver input is above or below the threshold voltage that is being specified. The detection circuitry has a hysteresis response that asserts the status signal only when a number of data pulses exceeding the threshold voltage are detected and de-asserts the status signal when the signal below the threshold voltage is detected for a number of recovered parallel clock cycles. This signal is useful in applications such as SATA and SAS for detecting out-of-band (OOB) signals.

To test this circuitry, two patterns are created to cover the assertion and de-assertion of the status signal. For the assertion of status signal testing, a data pattern with its VID sets higher than the threshold voltage specified is sent from the transmitter to the receiver through the external loopback path. This step asserts the status signal once it reaches the data pulses indicated by the hysteresis block. For the de-assertion of the status signal testing, the transmitter is powered down thus both the differential RX pins are biased to VCM value which is lower than the threshold voltage. After keeping the signal below threshold voltage for certain time per the requirement sets in the hysteresis circuitry, the status signal goes low. Figure 12 shows the top level implementation of the signal threshold detection circuitry.

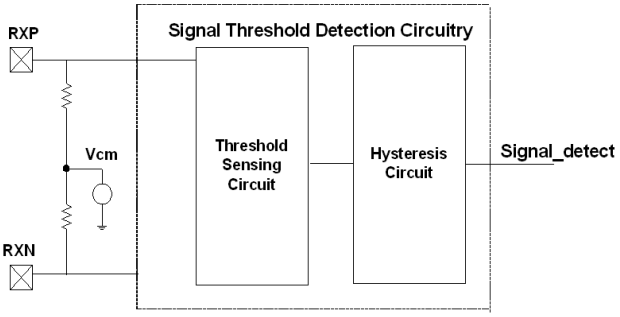

Figure 12: Signal threshold detection circuitry.

3.3.4. Pin leakage testing

With the availability of the PMU engagement through the isolation resistor as depicted in Figure 5, pin leakage to VCC and VSS can be conducted by driving the pins to either VCC or VSS using PMU and reading the leakage current measurement. Since the measurement is done through the 1KOhm isolation resistor, the leakage limit needs to take into account the effect of this isolation resistor in current reading. Table 1 shows an example of leakage measurement calculation with the 1KOhm resistor exists on the measurement path.

Table 1: Pin leakage measurement calculation with 1KOhm isolation resistor on DUT card

Vcc (V)	Leakage Current (uA)	R (Ohm)	R+1K (Ohm)	Leakage current through 1K Ohm Resistor Measurement (uA)
1	10	100,000	101,000.00	9.90
1	20	50,000	51,000.00	19.61
1	30	33,333	34,333.33	29.13
1	40	25,000	26,000.00	38.46
1	50	20,000	21,000.00	47.62

4. Silicon experiences and future direction

The biggest challenge in debugging the external loopback tests is fault identification. One needs to understand well the functionality of all the different blocks involved in external loopback strategy to be able to identify the problematic block. For example, receiver sensitivity test involves the engagement of transmitter buffer, PRBS generator, serializer, CDR and so on. Once this test fails, it requires significant debug time and ample circuitry knowledge to perform the fault localization. This is unlike the previous parameter based test strategy whereby the test setup concentrated on one sub-circuitry testing thus narrowed down the debug area.

The implementation of receiver sensitivity test and signal threshold detection test also pose some challenges whereby there is no systematic way to fix an accurate VOD value from the transmitter side for the receiver input to receive the right value of VID. The quality of the transmitted data is not

equal for all the channels mainly due to the transmitter driver bias current accuracy. Furthermore, the transmitted data is also further degraded as it passes through the external loopback path. This is the major reason why the limit is set based on empirical study. Along the same line, utilizing both the transmitter and receiver simultaneously in the external loopback configuration could cause test escape due to fault masking. For example, testing a strong transmitter and a weak receiver together as a single unit may result in test escape of weak receiver.

Board diagnostic test plays a crucial role as it helps to filter out any faulty components on board and ensures good quality of setup. This board diagnostic test needs to have a feature to be able to indicate the failing pin information and the fault that it is facing (e.g. open or capacitor shorts). This is to ease the operator or engineer to fix the board/setup issue quickly.

The tests described in the earlier section are incorporated into an FPGA product's test flow that supports 36 transceiver channels. The flow checkout is first performed on the engineering tester at both 25 °C and 105 °C on three good units. Good unit here means unit that passed the screening of the original production flow that does not incorporate external loopback. The flow is looped 20 times on each unit for each temperature and there is no test failure seen on the units. However, during the checkout, the author did encountered issues with the setup bring-up that causes board diagnostic test to fail and they are mainly caused by the quality of the contactor. With this issue resolved, there is no other failure encountered in regards to the tests.

The same flow is then used to perform on two production testers with handler. This is mainly to identify any potential issue with contact resistance when using handler for tester setup. Table 2 shows the checkout result from the production testers. The same 13 units that are being checkout in production tester A is rerun on production tester B to ensure that there is no setup independent issue. These 13 units are from a different lot as compared to the 104 units. The one unit that failed on tester B is failing the receiver sensitivity test and further debug showed that it is a genuine failure thus a valid reject unit.

Table 2: Flow checkout result on production testers.

Production Tester	# of Units	Checkout Status
A	13	Passed all units
B	13	Passed all units
B	104	1 unit failed

Test time analysis on these external loopback based tests is also conducted. By referring to Table 3 below, all tests except for pin leakage test have significant test time saving. Two main factors that contributed to this are the major reduction of PMU usage and adoption of functionality testing rather than DC parametric based testing. There is no test time saving for pin leakage test since the test is still utilizing the PMU usage.

Table 3: Test time analysis.

Test Type	Test Time Saving (%)
Board Diagnostic	44%
Receiver Sensitivity	85%
Receiver Detection	93%
Signal Threshold Detection	93%
Pin Leakage	0%

The external loopback strategy can be further expanded to run till to test the signal conditioning blocks such as decision feedback equalizer (DFE) and adaptive dispersion compensation engine (ADCE). With the assistant of on-die instrument, it is possible to verify the convergence of these equalizers to the targeting values [4].

5. Summary

The initial evaluation of external loopback strategy to cover the HSSI buffer level circuitry has been successfully verified in the production environment. Since this approach provides capability to test the buffer circuitry closer to customer application, it helps to correlate with customer failure faster and more effective. Besides, this simplifies the on-die DFT requirement and the parameter based testing usage is also minimized. Test cost can be kept down as the dependency on tester's PMU usage has also been significantly reduces. The evaluation performed shows that there is a huge test time saving on tests performed with external loopback as compared to the original parameter testing with three of the tests having more than 85% test time reduction. This exploration also provides test platform for future experiments such as testing of the signal conditioning blocks.

6. Acknowledgement

The author would like to acknowledge the HSSI team in Altera test development group for their contribution in external loopback implementation and its application in Altera production environment. A special thank is also addressed to Tze Sin Tan and Siang Leong Foo for their time and effort in reviewing this paper.

7. References

[1] S. Sunter, "EDA for analog DFT? - designers must get on the bus," IEEE International Test Conference, 2009.

[2] S. Abdennadher and S. A. Shaikh, "Practices in Mixed-Signal and RF IC Testing," IEEE Design and Test of Computers, July-Aug. 2007.

[3] K.-T. Cheng and H.-M. Chang, "Recent Advances in Analog, Mixed-Signal, and RF Testing," IPSJ Transactions on System LSI Design Methodology *(TSLDM)*, vol. 3, pp. 19-46, February 2010.

[4] International Technology Roadmap for Semiconductors, (ITRS 2011).

[5] S. Sunter, A. Roy, and J. Cote, "An Automated, Complete, Structural Test Solution for SERDES," IEEE International Test Conference, 2004.

[6] PCI SIG, "PCI Express Base Specifications Revision 1.1a", PCI SIG, 2003.

[7] B. Eklow, C. Barnhart, M. Ricchetti, T. Borroz, “IEEE 1149.6: A Practical Perspective,” IEEE International Test Conference, 2003.

[8] S. Vandivier, M. Wahl, and J. Rearick, "First IC Validation of IEEE Std. 1149.6," Proc. of IEEE International Test Conference, 2003, pp.632-639.

[9] B. Eklow, K. P. Parker, and C. F. Barnhart, “IEEE 1149.6: A boundary-scan standard for advanced digital networks,” IEEE Des. Test Comput., 20(5), 76–83, 2003.

[10] A. Meixner, A. Kakizawa, B. Provost, and S. Bedwani, "External Loopback Testing Experiences with High Speed Serial Interfaces,” IEEE International Test Conference, 2008.

[11] B. Provost and T. Huang, ‘‘AC IO Loopback Design for High Speed Microprocessor IO Test,’’ IEEE International Test Conference, 2004.