SERDES External Loopback Test Using Production Parametric-Test Hardware

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***Abstract*—External loopback testing is an industry standard test for serializer-deserializer (SERDES) interfaces, and it is used to test for at-speed defects in the analog transmission (TX) and reception (RX) buffers. The specific test involves sending pseudo-random bit sequence (PRBS) at high speed from the TX side, looping on the load-board and receiving on the RX side where the sequence is checked to calculate bit error rate (BER). To achieve parametric coverage on the buffers, it is required to have tester access at the SERDES pins. However, the on-board component populated for this tester access may lead to poor channel insertion and return loss due to reflections from these additional components. This, in turn, may lead to unacceptable BER at higher data rates. Consequently, it is a common practice to use one type of load-board for parametric/DC testing and another type for AC/at-speed testing.**

This paper describes a dedicated production load-board that is designed to achieve tester access on the SERDES pins using a resistor network. Using this load-board, external loopback could be operated successfully up to 20Gbps without sacrificing parametric test capability.

Keywords—SERDES; High-speed I/O; External loopback; analog AC test.

I. INTRODUCTION

High speed serial interfaces (HSSI) are common in most modern computing industry, data centers as well as communication systems. However, one of the key testing issues related to these interfaces is the difficulty of verifying the entire serial interfaces including the transmitter (TX) and receiver (RX) buffers. This issue can be addressed by high-speed external loopback test [1] [2]. However, production load-boards often require DC access to the HSSI TX and RX pins for parametric testing. When the TX and RX are operated in the external loopback configuration at higher data rates on the DC load-boards, users often run into signal integrity (SI) limitations that can result in higher than expected BER at the receiving channel [3] [4] [5]. This limitation stems primarily from poor channel insertion loss as well as return loss due to reflections resulting from on-board components populated for tester access of the SERDES pins. Both of these issues can be mitigated during the external loopback test by using a simpler load-board that does not have any DC access of the SERDES pins. However, this test strategy requires two test insertions, one for DC parametric test and another for the high speed external loopback test. This strategy increases the SERDES test time as well as hardware cost in addition to any logistic complication that may result from this dual test insertion strategy.

Several researchers have worked on enabling external loopback testing for high speed I/Os. However, most of them focused on improved design-for-test (DFT) features that would enable the external loopback. For example, authors in [3] [4] [6] have used high speed boundary scan registers (from IEEE 1149.1, IEEE1149.4, IEEE1149.6, *etc.*) to launch and capture bits at high speed. However, this JTAG testing is not meant to be run at the SERDES functional speeds. Other work has used built-in self-test (BIST) engines instead to achieve higher loopback frequencies [5] [7]. However, these approaches are still limited by the board trace and signal integrity issues that have been mentioned previously.

The work in this paper addresses this board trace and signal integrity issue by significantly improving the production load board design. In the past, traditionally the external loopback load boards have been designed using active components like relays to disconnect the DC parametric access during high speed testing. These designs are bulky and, as a result, harder to maintain in production environment. To mitigate this issue, the authors in [8] have proposed the use of inductors to provide DC access to high speed channels. An inductor acts as a short when DC voltage is applied thus enabling DC access on the high speed pins. However, resonance due to the capacitive component of an inductor at higher frequencies is worse than the resonance due to the capacitive component of a resistor (which is used in this work).

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This paper proposes a production load board design that can be used for both DC parametric tests as well as high-speed external loopback test (up to 20Gbps) to a SERDES in production test environment. As a result, this load-board design eliminates the need for a second test insertion during production test of a SERDES. To enable such capability, a load-board is designed to address two aspects. First, signal integrity issues on the load-board are addressed to enable the high-speed external loopback operation while keeping DC parametric access intact. Second, receiver signal conditioning blocks are utilized to compensate for the reflection and losses of the test structure on the load-board. This particular test load-board is designed to study 15+ structures for best channel performance. Optimal settings for the signal conditioning blocks like Continuous Time Linear Equalizer (CTLE), Variable Gain Amplifier (VGA), and Decision Feedback Equalizer (DFE) are finalized on the production load-board. Process-voltage-temperature (PVT) variation on silicon is addressed by engaging an adaptation engine to adjust the settings dynamically to minimize incorrect bit transmission.

The rest of the paper is organized as follows: Section 2 includes a discussion of the system-level architecture of a typical SERDES in our production designs and how external loopback can be enabled for this SERDES. Section 3 contains description of the load-board design and related challenges, while Section 4 summarizes the test structures studies for the load-board design. The channel characteristics of the external loopback trace on our production load-board design is also discussed in Section 4. Section 5 discusses how the settings for the available signal conditioning blocks are determined. Next, results of this work are included in Section 6. Finally, conclusions drawn from this work as well as future directions are discussed in Section 7.

II. System Level Block Diagram

Figure 1 shows a simplified block diagram of the SERDES under test. Specifically, parallel pseudo-random bit sequence (PRBS) is generated in the physical coding sub-layer (PCS). The serializer block then receives clock from the transmit-PLL, and it converts the parallel PRBS data into a serial bit-stream. This serial bit-stream is then sent out through the transmitter (TX). This data is ac-coupled to the receiver side. A resistor network is used to enable parametric access. Then, the RX receives the looped back serial data and feeds it forward to the clock-data recovery (CDR) unit and then to the deserializer block. The deserializer converts the serial bit stream back to parallel data, which is then checked out by the PRBS pattern verifier in the PCS for any erroneous bit. The RX includes the following signal conditioning blocks.

- Continuous Time Linear Equalizer (CTLE)
- Variable Gain Amplifier (VGA)
- Decision Feedback Equalizer (DFE)
- Adaptive Parametric Tuning Engine

All the above signal conditioning blocks are engaged to compensate for the channel loss during the external loopback testing used in this paper.

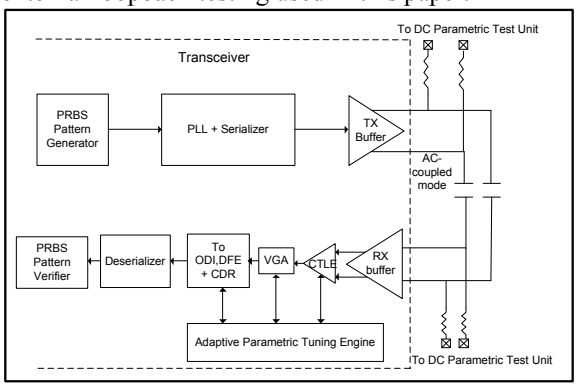

Fig. 1. System Level Block Diagram of a serializer-deserializer (SERDES) under test.

III. Load-board Design

Production load-boards have to meet certain physical constraint to ensure compatibility with the test systems they are used on. In this case, it is required to meet a certain thickness and have predetermined clearance on both top and bottom side. Also, the loss characteristic of the external loopback trace should be the same across all the channels. This is to ensure that all the channels on the device under test (DUT) are stressed identically. This means that all channels need to be routed in a similar fashion. A given transceiver device could have ~100 pairs of differential TX and RX pins. Hence there would be ~400 high speed signals to be routed in a limited space.

Another requirement on this load-board is that DC access to the tester should be available to avoid dual insertion testing. The DC access structure is needed to be optimized to be able to hit targeted data rate of 20 Gbps for external loopback trace.

Lastly, the external loopback trace should be designed in such a way that it is able to exercise the signal conditioning blocks like the CTLE and DFE. The trace lengths needs to be chosen in such a way that CTLE gain would be positioned in the center of its operating range. Also, DFE taps would be needed to compensate for the Inter-Symbol Interferance (ISI) in the link due to reflections. This would mean

deciding on dielectric material, microstrip and stripline length, and back drilling or sequential lamination process to optimize the discontinuity at via transitions. All the above constraints need to be met while ensuring manufacturability and cost budget.

Figure 2 below shows the layout view of the mock load-board with routing traces enabled on the left side. This load board already shows the component and trace congestion encountered when external loopback is enabled. This, in turn, also illustrates the complexity of a production load board design that that can enable external loopback test at high speed while maintaining all other production tests intact[1].

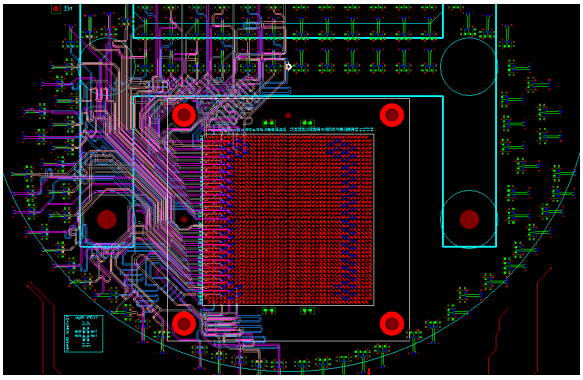

Fig. 2. Layout view of a mock load-board design that enables external loopback link with traces highlighted on the left side

IV. Test Structures

The following test structures shown in Table 1 are fabricated on the PCB to determine the characteristics of the DC access structure that would be used on the production load-board. They can be classified into two categories. The first category is the loopback structure. The five structures under this category are studied to determine the size of the on-board components and whether GND cut optimization was needed. The second category is the microstrip structure that is fabricated to quantify the loss characteristic of the 4 inch versus 8 inch trace length. This would help to choose optimum trace length on the production load-board that stresses the signal conditioning blocks on the unit under test as well meets the area budget.

Table I. Categories of Test Structure

Category	Description
Loopback Structure	Loopback with GND cuts and vias
	Loopback without GND cuts and vias
	Loopback with GND cuts and vias, extra pad
	Loopback without GND cuts and vias, extra pad
	Loopback without GND cuts and vias, extra pad,0201
Microstrip Structure	4 inch trace length
	8 inch trace length

Figure 3 shows a test-board that is designed with the structures indicated above. Description of these structures is included in the remainder of this Section.

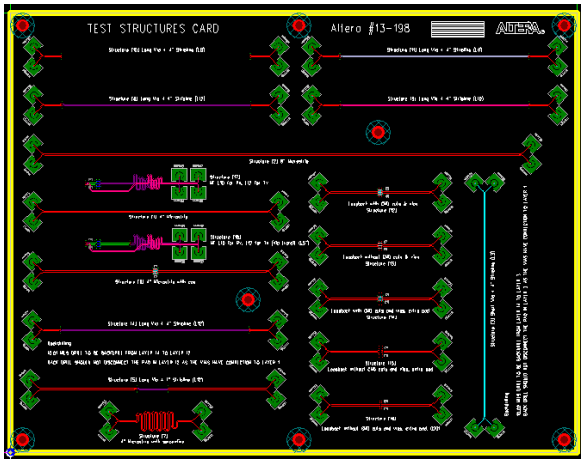

Fig. 3. Test structure Card

A. Loopback Structure

The circuit diagram for the loopback structure is as shown in Figure 4. Four 10KΩ resistors are used for tester access. High speed data is AC coupled from TX to RX side using 100nF capacitors. This loopback structure is built with GND cuts and vias as well as without GND cuts and vias. For ease of manufacturability, possibility of having an extra pad to populate the resistors is also studied. Two footprints of the extra pad are under consideration 0402 and 0201. Di-electric material used is FR4.

[1] The actual load-board design used in production test could not be shown in this paper due to propriety violation.

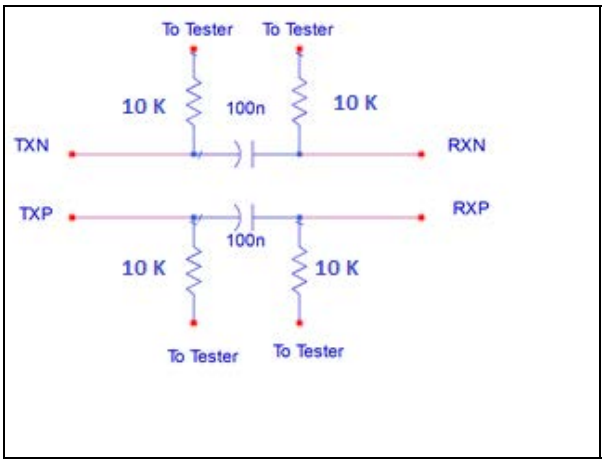

Fig. 4. Circuit Diagram for the loopback structure.

Figure 5 shows the insertion loss characteristics of the loopback structures. Loopback structure with GND cuts and vias and with the option of having an extra pad showed promising insertion loss characteristic at the data rate of interest. The steep loss occurs over 25GHz. For the loopback structure with GND cuts and vias and no extrapad, the insertion loss characteristic is better with steep loss occurring over 40GHz. However, having an extra pad is in general better for manufacturability and maintenance of the load-board in production environment, so we chose to go with the Loopback structure with GND pads and vias with an extra pad. The footprint of 0201 showed better insertion loss characteristic than the 0402 but again for manufacturability reasons 0402 footprint is better.

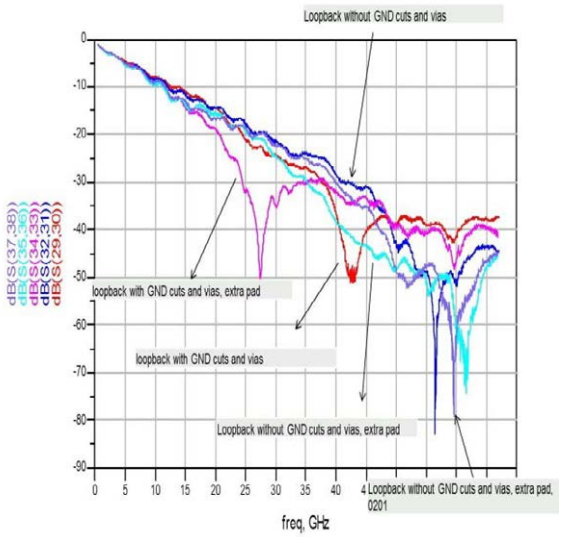

Fig. 5. Insertion Loss characteristic for the loopback structure.

B. Microstrip Structure

In order to determine the trace length that would be optimum for this load-board, one microstrip structure with 4 inch trace length and another with 8 inch trace was studied. De-embedding technique (similar to ones described in [9] [10]) is used here to remove the effect of cable and connectors from the raw measurement. Figures 6 and 7 show the loss characteristic of 4 inch and 8 inch microstrips, respectively.

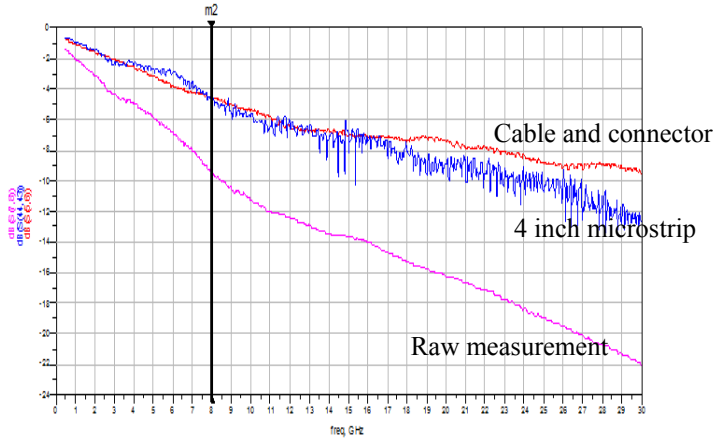

Fig. 6. Insertion Loss characteristic for the 4 inch microstrip

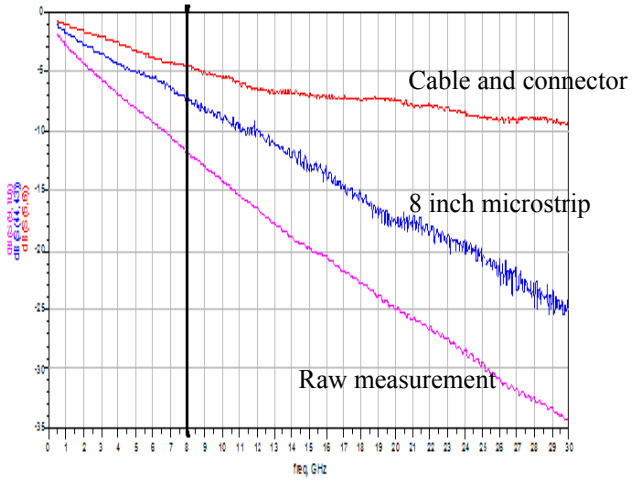

Fig. 7. Insertion Loss characteristic for the 8 inch microstrip

The insertion loss characteristic of 8 inch microstrip is close to what would be a reasonable stress condition for a given channel and trace length is picked to be very close to 8 inch for all the channels.

C. Channel Characteristic

After incorporating the test structure finalized from the section 4 into the production load-board, two channels are studied to benchmark the channel degradation due to 10KΩ resistor connected to the tester channel. Figures 8 and 9 compare the insertion losses and the return losses of one channel (referred to as Ch#1 in this paper) that is populated with the 10KΩ resistor and another channel (referred to as Ch#2 in this paper) that does not include the 10KΩ resistor, respectively.

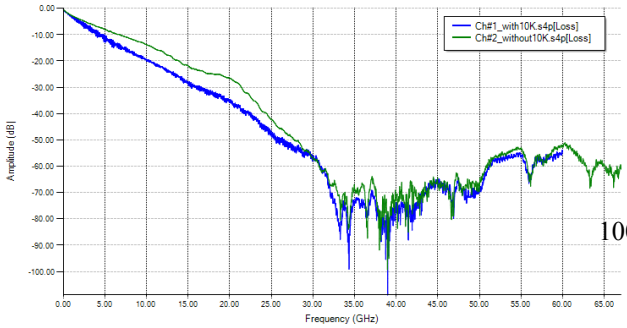

Fig. 8. Insertion loss comparison of a channel populated with 10KΩ resistor (shown as Ch#1 in blue) and another channel without the 10KΩ resistor (shown as Ch#2 in green).

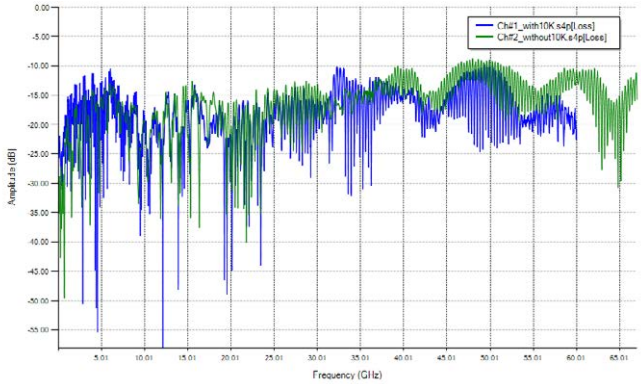

Fig. 9. Return loss comparison of a channel populated with 10KΩ resistor (shown as Ch#1 in blue) and another channel without the 10KΩ resistor (shown as Ch#2 in green).

Note that at a lower data rate up to 5Gbps, the insertion loss of Ch#1 configuration and Ch#2 configuration is comparable and are around -5dB. However, at higher data rates, Ch#1 has more insertion loss compared to Ch#2. Also, the return loss for Ch#2 configuration is better as compared to Ch#1 configuration since the former has no stubs connected to the tester channel. However, in Section 6, when these two channels are compared, both are observed to work up to 20Gbps with acceptable BER.

Time-domain reflectometry (TDR) is used to reports any discontinuity in the high speed data transmission for Ch#2 configuration. Figure 10 shows the TDR measurement of the above channel. The vertical axis indicates 5 Ohm per division. ~20 Ohm differential discontinuity at the loopback structure is seen. Measurement TDR edge rate is ~25 pS. This indicates a significant amount of energy will be reflected back. Hence, it becomes increasingly important for the signal conditioning blocks to compensate for the channel impairment.

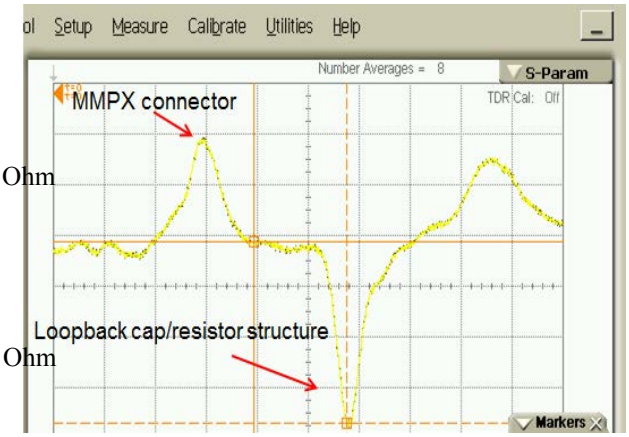

Fig. 10. TDR measurement of Ch#2

V. Using Signal Conditioning Blocks

During the exploratory phase, the load-board was modified to bring the TX eye out to the scope for a link with Ch#2 configuration (without the 10KΩ resistors in Figure 2). The coupling capacitors to the RX pins were also removed for this measurement. Figure 11 shows the eye measurement with this configuration. The blue and yellow signals in Figure 5 represent the single ended TXP and TXN over differential pair. Between both these signals, minimum eye height of 212mV and minimum eye width of 154ps is measured at 5Gbps. In other words, good eye opening is observed at this data rate.

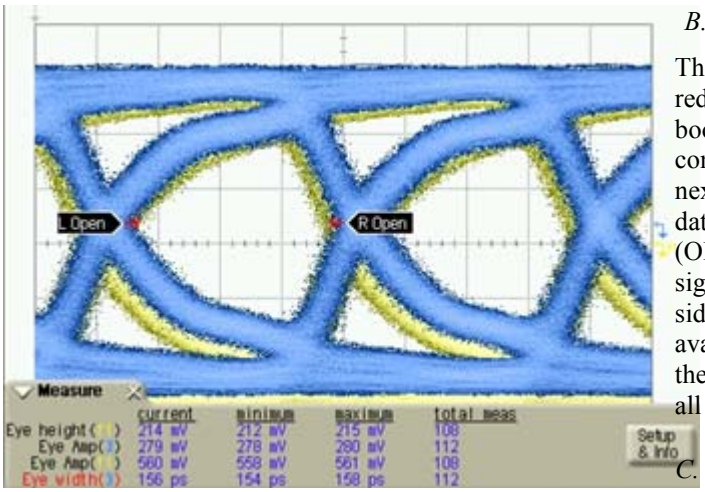

Fig. 11. Eye opening of the external loopback link at 5 Gbps.

However, the eye closes rapidly as data rate is increased beyond 5Gbps; and it closed completely when data rate exceeds 10Gbps. Hence the signal conditioning blocks at the RX side need to be engaged to open the eye.

The remainder of this section is used to discuss how the setting of various signal conditioning blocks is determined to compensate for the channel impairment. More details regarding each of these blocks is available in [11].

A. Continuous Time Linear Equalizer (CTLE)

The first signal conditioning block used to minimize BER is CTLE. The goal of CLTE is to amplify the signal that is attenuated due to channel characteristics by compensating for the low pass characteristics of the channel. This paper uses the CTLE block with fixed DC gain and sweeps the AC gain setting across PVT corners to identify the most optimal settings for acceptable BER from the external loopback link. It is important to ascertain the optimal equalization level from CLTE since under as well as over equalization of the loopback signal may result in higher than acceptable BER.

We also explored two bandwidth settings of the CTLE, namely full bandwidth and medium bandwidth. The full bandwidth CTLE setting provides AC gain centered at 6.25 GHz, while the medium bandwidth setting provides AC gain centered at 3.125 GHz. Therefore, depending on the channel insertion loss and the amount of compensation required at the selected test data rate, the appropriate bandwidth setting for CTLE is picked.

B. Variable Gain Amplifier (VGA)

The next signal conditioning block that is used to reduce the return loss is VGA. This block not only boosts the signal amplitude, but is also ensures a constant voltage swing before the data is fed to the next set of blocks for sampling, which are the clock-data recovery circuit (CDR), on-die instrumentation (ODI), and decision feedback equalizer (DFE). This signal flow is also illustrated in Figure 1 on the RX side. In this work, the VGA is set to have highest available bandwidth setting with medium gain since these settings are found to be the most optimal across all PVT corners.

C. Decision Feedback Equalizer (DFE)

Using only CTLE and VGA, good signal integrity can be achieved below data rates of 5Gbps. However, when the data rate is above 5Gbps, the BER of the external loopback link is no longer observed to be below the acceptable level when only CTLE and VGA is in use. Consequently, a third signal conditioning block, namely DFE, is used to improve the signal integrity of the external loopback link. The decision feedback equalizer (DFE) is a specialized signal conditioning block that amplifies the high frequency component of a signal, but does not amplify its noise content. By doing so, DFE removes the post-cursor Inter Symbol Interference (ISI) of the bit received previously from the current bit and, in turn, improves the Bit Error Rate (BER).

Figure 11 shows the general relationship between the tap settings of DFE with respect to data rate. As shown, in Figure 12, higher tap weight is necessary at higher data rate. However, DFE has several taps, and the specific weight for each tap is derived adaptively depending on the loss characteristics of the external loopback link.

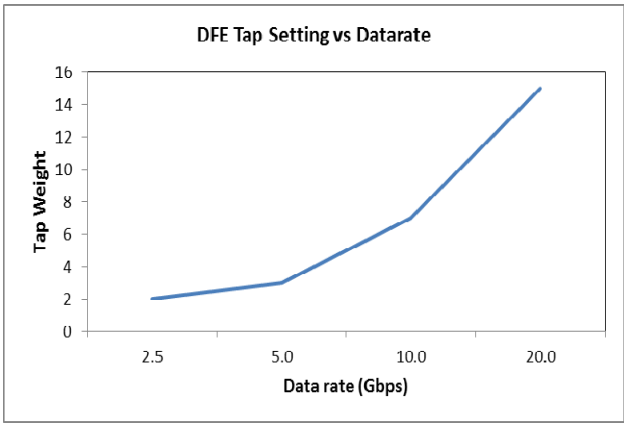

Fig. 12. DFE Tap weight with respect to external loopback data rate.

VI. RESULTS

Finally, when the new load board design is used along with the optimal settings of the signal conditioning blocks (derived as described in Section 5), successful external loopback is observed up to data rates of 20Gbps. However, different CTLE and DFE settings are required at different data rates; meaning, their settings are data-rate dependent. Table 2 shows the CTLE and DFE settings that are found to be working for both Ch#1 and Ch#2 configurations across all PVT corners for few example data rates explored in this work.

Table II. Signal conditioning blocks used for a given data rate

Data rate	Signal conditioning block settings
2.5Gbps	▪ CTLE – Medium bandwidth ▪ DFE – Not used
5Gbps	▪ CTLE –Medium bandwidth ▪ DFE – Not used
10Gbps	▪ CTLE –Full bandwidth ▪ DFE – Adaptive DFE
20Gbps	▪ CTLE –Full bandwidth ▪ DFE – Adaptive DFE

Note that both channel Ch#1 and Ch#2 configurations are able to support data rates up to 20 Gbps. Hence, adding the resistor network for DC parametric access did not incur any penalty on the performance of the external loopback link. It is also important to note that the load board design and the signal conditioning block settings discussed in this paper has been successfully deployed in high-volume production testing of our most recent product to verify the maximum operating frequency of the SERDES block.

VII. CONCLUSION

This paper explores a novel production load-board design that can support external loopback testing of the SERDES block along with all other necessary tests. It also discusses settings for the signal conditioning blocks in the design. Finally, it observed that only when a novel load-board design is used along with optimal signal conditioning settings, high data rates of up to 20Gbps can be tested by the external loopback link; meaning, each alone cannot support this high data rate.

In future, the high-volume test data will be analyzed to determine the silicon units that uniquely fail at these high data rates, but pass all other tests including the high speed internal loopback tests. These failing units may provide additional clue into TX and RX buffer issues that cannot be tested by the internal loopback tests.

ACKNOWLEDGEMENTS

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