External Loopback Testing Experiences with High Speed Serial Interfaces

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Abstract

Data eye margin test used in conjunction with loopback configuration has become a popular Design for Test (DFT) based test method for high speed links. This paper summarizes the DFT circuitry and test methods for supporting high speed serial interfaces (e.g. S-ATA,). The challenges of no-touch test methods in an external loopback environment are discussed. We close with a summary of our manufacturing experiences and directions for future improvement.

1. The Need for External Loopback and IO DFT Test Support

The drive to higher bandwidth interfaces in computing devices (e.g. PCI Express™) has resulted in the adoption of high speed serial interfaces (HSIO) similar to those found in communication devices. However, the test practices from communications products have not been embraced in computer device testing. The following characteristics have led to a different test strategy:

1. High signal counts- communication devices have a few lanes, while computer devices can have 16 to 100 lanes, or even 500 lanes;
2. Higher production volume (millions of units per year)- results in higher sensitivity to manufacturing test time and costs;
3. Lower average selling price- hence, greater cost sensitivity;
4. System channels of 4"-20" copper traces on printed circuit board- impacts jitter test requirements.

With the challenges of keeping test costs down and testing HSIOs, DFT based methods have been pursued. Data eye margining tests have been adopted by companies, usually facilitated by on-die or off-die loopback. By relaying upon eye margining test methods and additional DFT test methods as noted in [3], computer products have ignored the communications style of testing which involves expensive ATE equipment for jitter testing and requires long test times.

As noted in a description of AC IO Loopback [1], Intel engineers had already begun efforts to develop extensions that can be used for HSIO high volume manufacturing (HVM) testing. Our success with timing margining on the Intel Front Side Bus™ (FSB, gave us confidence in applying this technique to new interfaces including: S-ATA™, PCI Express™, Direct Memory Interface (DMI), Fully Buffered DIMM™ (FBD). Applying margining concept to the voltage domain was a natural extension from what system designers commonly do for characterization. Previous work on pin leakage can also be applied to these interfaces. Finally, the investment in Intel® Interconnect BIST (Intel® IBIST) [4] permitted more complex test patterns.

This paper will focus on overall manufacturing test methods applied for products using external loopback and will include basic descriptions of implementations and share silicon experiences. The remainder of this paper will start off discussing loopback design options and basic test requirements. The next section spells out timing margin and voltage margin test options. The options for leakage testing are then described. This is followed by sections which address test of data clock recovery (DCR) circuitry and special functions like link and squelch detection. A summary of test pattern generation, capture and control implementations is then provided. The final sections of the paper address silicon experiences, improvements and future directions.

2. Loopback Connections and Test Requirements

Loopback connections, depicted in Figure 1 include:

1. Analog Near-End
2. Digital Near-End
3. Analog Far-End
4. Digital Far-End

HVN test uses near-end loopbacks, while far-end loopbacks are used for device characterization with an instrument or within a system between two components (e.g. INTEL® IBIST). Initially analog near end loopback had two options: on-die- ANEELB1

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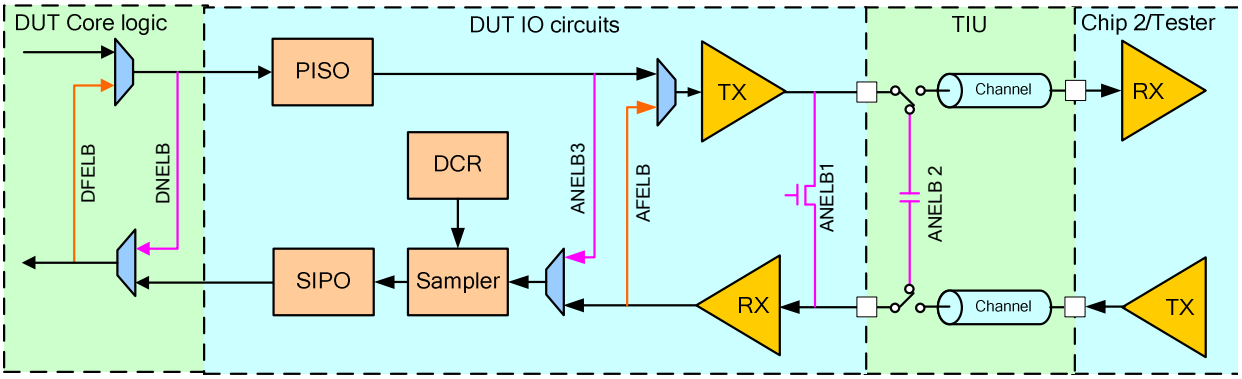

Figure 1 Loopback paths on HSIO

or on the test load board- ANELB2 (note relays are optional). The on-die analog near end loopback from TX pad to RX pad can used for wafer sort without probing. On-die loopback doesn't work for packaged unit tests due to the signal integrity issues caused by the package trace. At higher data rates, the performance impact of the on-die connections becomes significant. The first generation specs could manage the performance impact of ANELB1. With the second generation specs a compromise was made by creating a loopback (ANELB3) after the sensitive driver and receiver circuitry that still stress the sampler and DCR circuits. This enables an at speed test at wafer sort for most of the physical layer. In the products discussed in this paper used ANELB3.

DFT and test requirements to support HSIO test in a loopback configuration include:

- Pattern generation and received pattern checking
- Timing Margining
- Voltage margining
- Data Clock Recovery (DCR) circuitry testing
- Pin leakage test
- Special modes testing
- Structural test of compensation circuitry

Additional DFX (X=Test, Debug Validation) hooks may be supported for board level test (e.g. XOR or Boundary Scan), silicon debug and silicon validation. This paper will only focus on manufacturing test usage.

In considering loopback design on the load board, there exist trade-offs between test methods and design. First, some interfaces have an unequal number of TX and RX lanes e.g. FBD™. To execute a loopback test, one can design extra TX or RX lanes on the DUT. Alternatively, one can add relays to the loopbacks to enable full connectivity with a second pass of tests. On our products we have observed both options used. Even with symmetric TX/RX lanes one can choose to use an ATE's DC parametric test capability via direct connection and then use external loopback for the at speed testing. In this case relays are used to change the configuration based upon test methods. Careful consideration of signal integrity issues must be made; best practices like stubless design are recommended [3]. Note, there may be load board area constraints which limit how many loopback configurations can be made. Figure 2 a-c illustrates configurations that could be used on TX to RX connection of an HSIO.

Figure 2 Three External Loopback Configurations

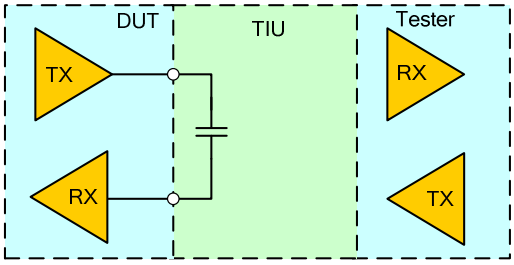

Figure 2a) External loopback

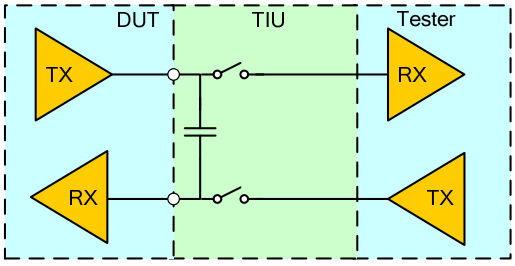

Figure 2b) Always loopback with relays

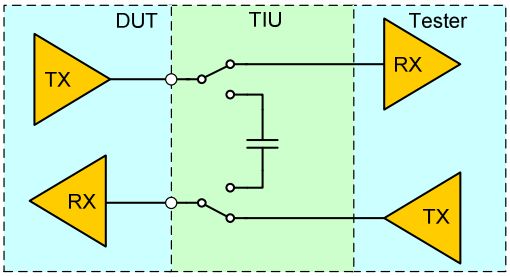

Figure 2c) Loopback with relays

3. Timing Margining Test Methods

A timing margining test assesses the data eye width [1], [3], [7], and pass/fail determination is based upon the minimum width. In our previous work with Intel FSB™, we made this assessment over a signal group. With HSIO interfaces, we make the assessment per lane. We determine the pass/fail criterion via empirical study as the published specification does not account for differences between the load board and system channels. Te load board data eye is larger in both time and voltage than the system data eye.

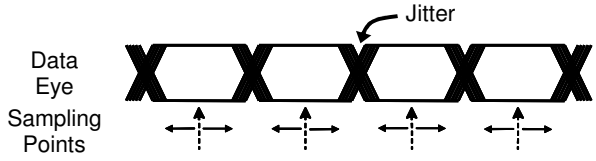

Figure 3 Data Eye Timing Margining

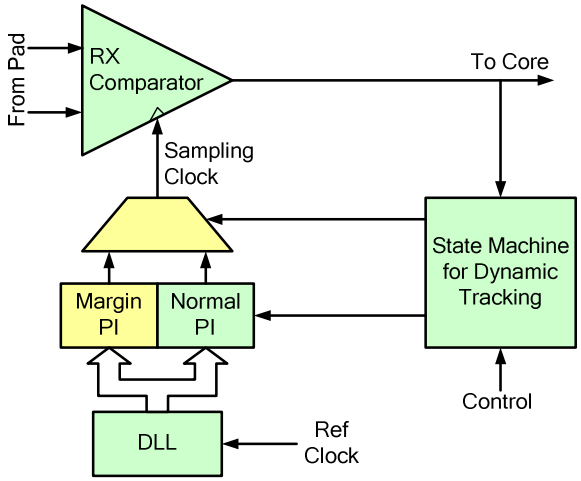

Figure 4 Timing Margining with a Margin PI

Figure 3 illustrates a timing margining test. Ideally, the RX strobe would be centered in the data eye, and the right/left margin would be ½ UI (Unit Interval, ideal data eye width) each. In reality, jitter, circuit non-idealities, setup/hold time, trace length mismatch and clock recovery inaccuracy causes the margins to be reduced and unequal. By moving the sampling points in both directions, one executes a timing margining test. The test can be structured to search until a pattern mismatch is detected or to move to a pre-determined point. Pass/fail is then determined.

Reuse of physical layer training circuitry results in a low DFT area cost. For each HSIO type, the exact implementation will vary due to data clock recovery (DCR) design differences and designer's options. An over-sampled DCR timing margining differs from one reusing a DCR based upon phase interpolation. Figure 4 shows a one timing margining implementation using a RX Phase Interpolator (PI). For this implementation the designer chose a supplemental PI (identified as margin PI) to enable timing margining without disrupting the tracking data obtained during training. Some designers were not concerned about the tracking during the test mode. They chose to directly offset the PI trained valued.

With TX Phase select, the driver timing is shifted by muxing a different driving clock signal, already available for the RX. Finally overriding the trained value is available for debug and validation purposes and could be used as a back-up for manufacturing test.

Table 1 provides the timing margining implementation, range and resolution available for the HSIO circuits employed in our products.

Table 1: Timing Margining Implementations

Interface	DCR type and methods	Range, Resolution
S-ATA	Over-sampled: TX phase Select	2 UI, 1/8 UI
PCI Express	PI based: Supplemental or offset	2 UI, 1/32 UI
DMI	PI base: Supplemental	2 UI, 1/32 UI
FBD	PI Based: Offset	2UI, 1/32 UI

4. Voltage Margining Test Methods

Voltage margining schemes involve reuse of TX or RX circuitry and hence are tied to specific circuit implementations. The main approaches can be divided in two ways: offset-based and common-mode based. Table 2 summarizes these approaches and gives a qualitative assessment on process, voltage, temperature (PVT) tolerance, range and resolution.

We should note that most limitations highlighted in the table can be attributed to reuse of normal mode circuits. While adequate for their design purpose, these do not always translate well into a test usage model with respect to range or resolution. Hence, the limitations noted are not fundamental limitations of the techniques. At the end of the paper we discuss possible mitigations to improve reuse. The rest of this section discusses each test method.

Figure 5 illustrates an RX method which tests the perceived RX data eye height by manipulating the voltage offset of a variable offset comparator (VOC), [3], [9]. Empirical data collection sets the pass/fail limits. Some drawbacks of this approach include: taking the circuitry out of prescribed common-mode range, inadequate range and non-linearity at the range ends. The last drawback can greatly impact the robustness of the test method.

Table 2: Voltage Margining Strategies

Name	Range Resolution	Resulting Data Eye Impact
Rx Comparator Offset	Range designed value – amount reserved for Vt mismatch Resolution 2-5 mV	Actively move trip point of RX comparator by offsetting the trimmed value. Good PVT on resolution.
Rx Common Mode offset	Range on order of 300 mV. Resolution 20-25 mV	Move Common-mode by changing value provided by Band-gap reference. Excellent PVT
Tx I-Comp	Usable range usually 10% lower than target. Typically 4 bits to control	Reduce driver current strength results in smaller eye. PVT impact- same code will result in different value
Tx/Rx R-Comp	Usable range usually 10% lower than target. Typically 4 bits for control	Lowering termination resistance results in smaller eye. PVT impact- same code will result in different value

Another RX option is offsetting the common-mode as shown in Figure 6. The DFT implementation permits shifting the D+ signal's common-mode independent of the D- signal. A band-gap reference provides the bias resulting in excellent PVT tolerance. However, a key drawback is resolution which can result in overkill or underkill.

The final test method involves changing the compensated values for TX or RX circuitry. Transmitter driver strength changes are possible by changing current bias, number of devices or termination resistor value. The impact is a reduced data eye as illustrated in Figure 7. It should be noted it also results in a change in common-mode. The RX termination can also be changed. When changing the TX/RX termination values one must consider the signal integrity impact of mismatched termination which would also impact the data eye width.

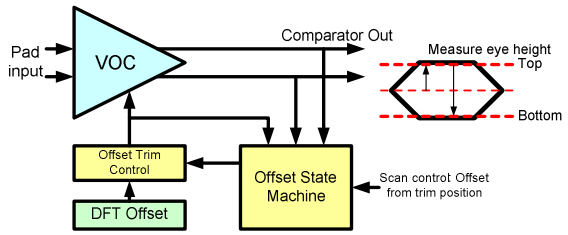

Figure 5: Voltage margining via Offset

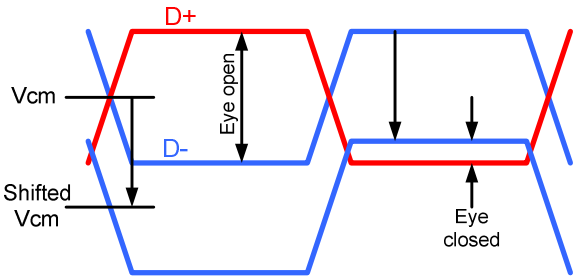

Figure 6 Voltage margining via Common Mode shift

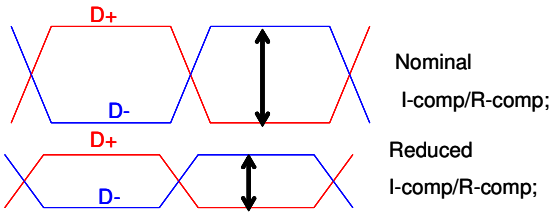

Figure 7 Voltage margining with I-comp/R-comp

TX voltage output and RX voltage input tests are traditionally done separately, thus allowing a direct comparison to published electrical specs. With a loopback connection, these two parameters are tied together. Therefore the test method challenge to separate out TX vs RX defects exists. One can run two tests: first, no TX degradation, second, with TX degradation. With our first generation of HSIO we have often found it difficult to measure the full strength of the TX at the RX due to DFT method limitations. This is partially because load board interconnect

delivers a larger TX data eye than the system board. One can create a degraded eye by having a longer trace or an active component that could degrade the connection [16], [17]. However, load board area limits may inhibit meeting the RX minimum data eye for devices which have a large number of HSIO lanes. In practice, this means we need to combine TX and RX DFT to execute a voltage margining test in loopback.

5. Test Coverage for Data Clock Recovery (DCR) Circuitry

All the HSIOs discussed rely upon an embedded clock assumption; therefore they include DCR circuitry in their receiver design. In communication products jitter injection is the traditional means of providing test for coverage for the DCR and other physical layer digital circuitry (e.g. FIFO buffers) [18] [19]. A simple loopback test even with timing margining will not provide adequate test coverage because the TX and RX use the same clock. Hence one needs specific DFT based test methods to use during loopback to guarantee DCR performance [3].

The options available are circuit architecture specific, so a brief description of two architectures is given prior to describing the test methods. One is an over sampled architecture in which the data is sampled multiple times and during the initial training an initial sample is chosen. As there may be a drift in clock phase, a continual checking for best sample is executed. Another implementation uses a phase interpolator to mix different clock phases provided by a delayed lock loop (DLL). Initial link training determines the best sampling point. To accommodate phase drift either a continual checking of edge and data samples or periodic retraining is done. Two test methods used in our products will be described; TX phase select test is with over-sampling DCRs and a mutual PI test when two PI's are used in the DCR.

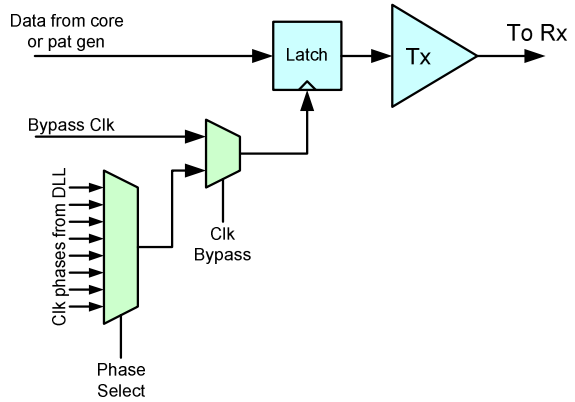

Figure 8 TX Phase Select implementation

The TX phase select test changes the TX phase by incremental steps while the RX phase remains same see Figure 8. This test mode is used in conjunction with the full-speed loop-back mode. The TX signal delivered to the receiver will be shifted, thus allowing more of the DCR logic to be tested at high-speed. Actively changing the TX phase select during loopback operation permits a test approaching a traditional jitter test. This is possible if the necessary controls are available. Unfortunately, the implementations in the first generation HSIO used software control to change settings which didn't change the phase fast enough, we discuss this further in improvements section.

Depending upon the DCR design there may be one or two phase interpolators (PIs). The latter permits mutual PI testing. The concept is to use one PI output to sample the other. Designers added a comparison latch and separate control of each PI's settings to permit a self check. Using a D-Flop we simply shift the value of the clk. A defect in one interpolator causing an abnormal delay will cause Q to switch from 0 to 1.

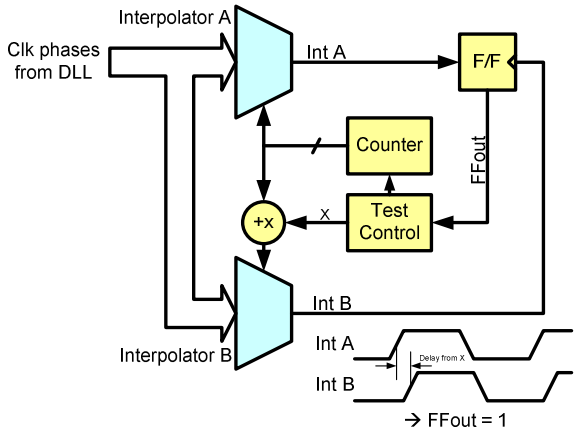

Figure 9 TX Mutual Phase Interpolator Test

6. Pin Leakage Test

Our first products had implemented loopback as depicted in Figure 2(a); hence, we required a no-touch test method. The method of choice was based upon a RC Decay method as described in [11], [12]. For illustration, leakage to VSS, the steps consist of:

a. Write a 1 to the pin under test
b. Remove all leakage path sources
c. Wait an empirically determined time
d. Sample the value on the pin
e. If value changed to 0 then fail

For pin leakage PCI Express™ presented an additional challenge due to the AC coupling. Therefore the designers added by-pass circuitry the for the on-die capacitor. Figure 10 describes the DFT circuitry on the

PCI Express RX analog front end (AFE) [15]. A local comparator is used to compare the node under test to the Vcm value programmed via a band-gap reference. With this implementation each node must be tested separately for leakage to Vss and Vcc. Similar circuitry can be found in the TX AFE. Additional logic circuitry XORs the results from all pins and then sends the results to an external pin. This permits the ATE to control the sampling rate at a resolution of 10 ns. This test can be done at wafer and unit level test; naturally they require different test limits because of differing capacitance loads.

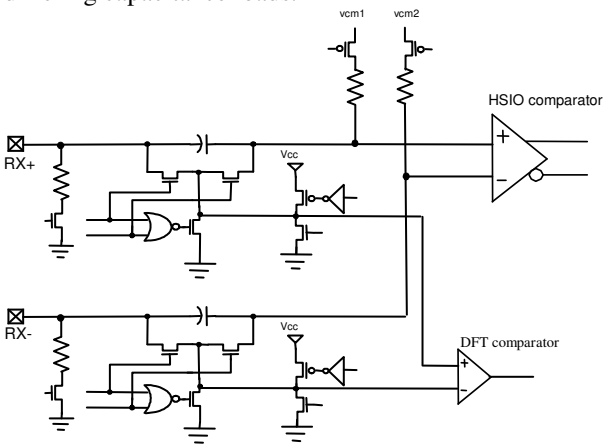

Figure 10 DFT to support leakage test on PCI Express™ RX

7. Testing of Detection Modes

HSIOs have detection modes to permit transition from active to power down states (squelch) and to check link presence during training. These can be important features to test due to circuit sensitivity and requirement for system usage. For illustration purposes this section describes two tests used for PCI Express™: card detect and squelch detect.

The TX card detect circuit determines the presence of an add-in card. Figure 11 shows that the pull-up charge up speed is fast due to the small RC decay time.

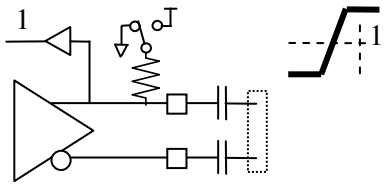

Figure 11 No Add-in card

Figure 12 depicts the connected add-in card. The charge up speed is significantly slower due to the termination resistance.

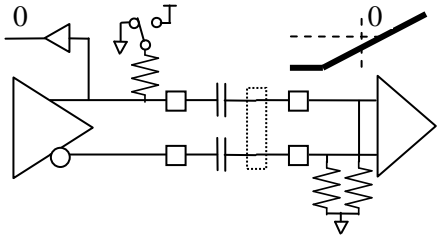

Figure 12 Add-in card present

On the HVM load board the TX and RX are connected via AC coupled capacitors for high speed loopback test. To test the card detect circuitry, DFT disconnects the RX termination to emulate the no card condition as shown in Figure 13. This also provides coverage for RX pin leakage to Vss; which turned out to be an important collateral coverage.

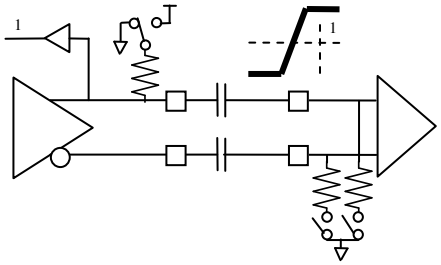

Figure 13 HVM test set-up for card detect

Squelch (SQ) detect circuitry on RX pins identifies the TX power save mode. As illustrated in Figure 14, when the perceived signal height is less than 65mV differential p-p (peak to peak), the TX is in squelch mode. When the signal is more than >175mV differ p-p, then the TX is out of squelch.

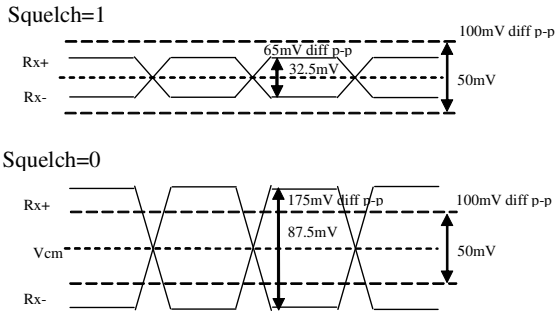

Figure 14 PCI Express Gen1 Squelch Spec

The squelch voltage design targets the value between 65mV and 175mV diff p-p. In the presence of Fab process variation, the actual voltage may be less than 65mV, i.e. out of spec. With a loopback connection,

the ATE can not apply a Vil/Vih test. However, even with a direct ATE connection (see Figure 2 b/c), the pin electronics may be unable drive the required small voltage accurately. Consider a tester accuracy spec for Vil/Vih with resolution 0f 10mV and minimum difference of Vih – Vil >100mV. Currently production test can use two DFT based solutions:

1. Use the DFT that generates multiple bias reference voltages.
2. Use TX to RX loopback with driver eye height change capability.

The second solution has been discussed in Section 3, we explain the first solution below.

In normal squelch circuit operation, the offset is set -100mV (Figure 15 blue line), so ideally output would be as follows:

- TX diff>100mV → Sq=0
- TX diff<100mV → Sq=1

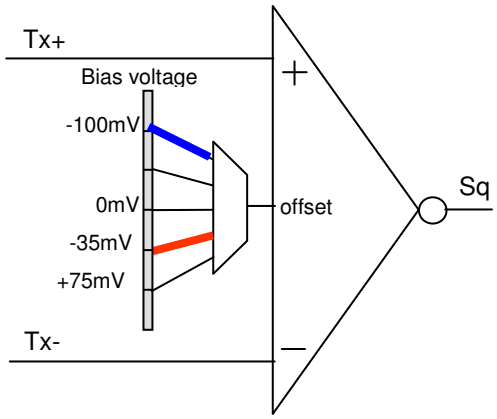

Figure 15 Squelch circuit diagram

When a large offset exists such that it violates the spec (Sq=1 at <65mV) the result is as follows:

- TX diff>60mV → Sq=0
- TX diff<60mV → Sq=1

To implement a DC Squelch test we use DFT to set a different bias, (Figure 15 red line), and test as follows:

1. Set TX diff=0 (Tx+=Tx-)
2. Set offset -35mV (100-65mV margin to spec)
3. Check Sq output:
   - Sq=1, "pass" = sense amp offset < 35mV
   - Sq=0, "fail" = sense amp offset > 35mV

From our silicon experiences, while we observed the absolute bias voltages had some accuracy errors the relative voltages proved to be quite accurate and it is the difference that matters in this test method.

8. Pattern Generation, Capture and Test Control

A backbone to all the test methods described in the previous sections is on-die pattern generation and capture and the test control. While some designers implemented Intel® IBIST [4], others chose to reuse existing pattern capability such as the PCI Express™ CMM (Compliance Mode Module). Other designers implemented their own local pattern generation and compare circuitry. Table 3 summarizes the various implementations used by HSIO interfaces found in our products. The trade-offs in implementation are silicon area and the amount of effort in pre-silicon validation for the more complex designs. The products which chose the Intel® IBIST did so for system validation purposes and because they had more stringent specs.

Table 3: Pattern Generation/Capture Capability

Pattern generator	Pattern Depth	Pattern Modes	Capture Modes
Intel® IBIST	128 bits	Default Programmed Single Burst PRBS[1] Conintuous	Stop on first fail Count fails Sticky bit failure
CMM	10 bits x 4	Fixed pattern Singe burst Continuous	Stop on first fail Sticky bit failure
Local	64 bits	Single Burst Continuous	Stop on first fail Count fails Sticky bit failure

The other aspect of test method implementation is test mode control. Some products use only registers to control settings and observe test results. Writing and reading control settings and results via either JTAG or other another test interface can be done.

9. Silicon Experiences

In planning IO DFT based test methods to support external loopback, engineering teams executed pre-silicon validation in the form of logic and transistor level simulation. These activities helped prepare for silicon arrival and identified methodology changes. The final proof though is in the silicon. For this section we share debug, characterization and implementation challenges, and manufacturing test fallout data.

A challenge in debugging external loopback test is observability and overall design health. The product

[1] Pseudo Random Bit Sequence

teams who invested in an HVM debug board without the loopback had an easier time debugging pattern issues. The cause of pattern issues included: the boundary between the control logic and analog circuitry not working as expected, signal integrity issues- i.e. expecting on-die loopback to work on a unit, and incorrect test methodology applied.

Due to the reliance upon on-die features making measurements, characterization of range and resolution over PVT becomes essential to implementing a solid test methodology. Silicon design validation activities planned for the interface will cover basic debug needs. For setting HVM test limits one wants to extend the characterization over a wide range of devices. Considering the test methodologies discussed in this paper the following features would be characterized:

- All codes of impedance termination on TX and RX,
- All codes of TX driver I-compensation,
- All codes of variable offset comparator,
- All settings of common-mode provided by band gap reference,
- All phases of a DLL,
- All settings of a Phase Interpolator,
- All settings of an Over-sampled DCR,
- Pin leakage to Vcc and Vss and correlated with the no-touch methods.

To execute the characterization it is important to have appropriate observation points for circuitry that is not normally visible; for instance consider the DCR circuitry. While observing every single lane's DCR output may not be feasible; at least one direct observation of an DCR permits understanding its linearity. This understanding is vital to a repeatable timing margining test. Early implementations of phase interpolators exhibited some non-linearity. While the average step-size proved adequate for the design purpose, the non-linearity made it challenging to develop a robust test method. Some products chose to not implement timing margining due to concerns of overkill, others managed despite some yield loss

The implementation of voltage margining suffered from engineers choosing the TX I/R-comp based methods which have the least amount of PVT tolerance. Hence after the first generation of products, many products added relays to their loopback design to permit ATE DC based test for input and output levels. Even ATE's have limits for levels testing; as noted earlier, the squelch detection test had to use DFT to implement.

At least one initial product could not get a no-touch leakage methodology operational on PCIExpress™. Luckily the card detect test provided coverage for RX pin leakage to Vss; which turned out to be the leakage measurement with the highest fallout.

We share manufacturing test results on four chipset products. These products did not fully apply all the DFT based test methods discussed in this paper. In addition, they all implemented a termination leg check test, in which resistor value is structurally tested. The products used either a 130 nm or 90 nm process, and can be described as follows:

- Product A, 130 nm: South Bridge- USB2.0™, S-ATA™, PCIExpress™, DMI; used relays;
- Product B, 130 nm: server North Bridge FSB, FBD™, PCIExpress™; no relays;
- Product C 90 nm: desktop North Bridge- FSB, DDRII, PCIExpress™, DMI; used relays;
- Product D 90 nm: mobile North Bridge- FSB, DDRII, PCIExpress™, DMI; used relays;

The manufacturing fallout data is for unit level test which is after a Burn-in step. For presenting the data in a meaningful format without revealing true yield numbers the fallout is represented as a percent of overall fallout. Sample size numbers were on order of 200K to 1 million units. The data for products B-D was collected from the same time frame and product A was from a different time frame. Table 4 shows the breakdown for memory, logic, misc., IO fallout. In general for chipsets the IO fallout is on par with the logic fallout. However, for products C and D this is not the case and can be contributed to increased fallout to HSIO tests in product D.

Table 4 Relative HVM fallout, %

Product	Logic	Memory	Misc.	IO
A,130 nm	37.91	4.63	19.03	38.44
B,130 nm	25.68	1.07	26.50	46.75
C, 90 nm	63.04	9.25	11.05	16.66
D, 90 nm	13.93	5.10	24.22	56.74

HSIO fallout can be found in Table 5, note all HSIO fallout is included together and is not normalized for the different number of HSIO lanes. In addition not all IO received the same test content and this may skew the results. Two terms used in the table require definition. N/A means this test was not run; No data means the data combined all IO results and hence could not separate out the HSIO fallout.

Table 5 HSIO Relative HVM Fallout, %

Test	A	B	C	D
Loopback	9.60	10.69	2.97	4.35
DCR	0.36	N/A	N/A	N/A
Timing Margin	N/A	0.09	N/A	N/A
Voltage Margin	N/A	3.48	N/A	N/A
DC Levels	0.15	N/A	No data	No data
Term Leg check	N/A	0.20	0.23	0.39
Leakage NTL/DC	N/A/ 0.59	2.15/ N/A	0.08/ 0.36	4.28/ 2.64
Squelch detect	N/A	N/A	2.93	30.28
Card/Link Detect	N/A	6.11	0.01	1.88
Total	10.71	22.72	6.57	43.81

In three out of four products the loopback test contributed to most of the fallout. Products C and D had relays on a subset of its external loopbacks; hence leakage test results are reported for both methods. As product D is a mobile version of product C the significant increase in fallout to leakage, squelch and card detect tests can be explained. With a lower Vcc the variation of Vt for matched devices increases would significantly impact any differential amplifier, such as squelch and card detect diff amps. For the NTL testing, the increase can be due to the diff amp variation and that the leakage may have increased with the lower Vcc. Only product B implemented data eye margining tests and it is very interesting to note more fallout for the voltage margining test. This can be contributed to using the TX I/R-comp methodology by setting all units to the lowest possible setting. As this ignores the process skew for each unit, overkill is most likely for this particular test. One can over come this with a change in test program described in the next section.

10. Improvements and Future Directions

Our silicon experiences provide grist for improvements in implementation and guidance for investment in on-die automation and consider alternative test methods which reduce test program implementation effort. The following list captures these areas for improvement:

- Careful automation of data eye margining tests
- Alternative no-touch leakage test methodologies
- Improving voltage margining techniques
- Providing DFT to support DC levels testing

Initial products implemented a no-touch leakage methodology; however, engineers found it cumbersome to do the correlation every time the process shift resulted in significant changes in pin leakage. This often led to yield excursions that needed a quick response. In some cases, the next iteration of a product added relays to the load board to enable the more familiar ATE based test. This initial experience has also motivated exploring alternative DFT approaches. One such method builds on previously published work [13]; the test approach is based upon noting a change in a DC Bias and using an on-die comparator to determine pass/fail limits. Another idea uses an on-die analog test bus and DFT to provide a means for an ATE channel to test each pin in a serial fashion.

Combined need for more interface bandwith and lower power will result in more sophisticated equalization schemes. In some future TX circuit designs full coefficient control for an FIR equalization technique is possible and this permits a means of changing the TX data eye with increased resolution and maintaining the common-mode voltage. The I/R-comp based schemes suffer from changing the common-mode and lower PVT tolerance. As noted previously this method can have overkill. By providing a lookup table for compensation codes per process skew, a fail flow could be added to permit recovery of good parts. This same technique could deal with PI non-linearity. In both instances, additional DUT information is needed for a successful fail flow. The PI timing margining test would need to know the trained position for the failing lane(s) and use this data to more accurately assess the eye width. The I/R comp voltage test would use the compensated value to determine position on the process curve; adjustment for code setting could then be made. For RX comparator offset variation, a minor change to the design can provide more range for the test method by sacrificing the resolution. For instance, doubling the range would results in changing from 1-2 mV increments to 5-7 mV increments. We believe this reduction in resolution is well worth the extension in test range.

Another option implemented in products is to use software control for test mode. While this saves design

area, it does have a draw back in that updates are slow. The ability to automate the test algorithm for searches and providing results can be extremely advantageous. A state machine or a counter can be used to advance through timing increments, voltage offsets, or compensation values.

Increasing cost pressures indicate that our reliance upon DFT based methods will continue to grow. ATE pin electronics for high performance interfaces are the highest cost adder to a test platform. With a shift to a System on a Chip (SOC) architecture and time to market standardization of test interfaces to HSIO will be essential to successfully bringing a product to market. The products discussed in this used uniquely three different means of communicating test access via different internal buses or messaging structures. Hence no sharing of test vectors or programs is possible. Having the same test interface to an IO block has the potential to reduce test program development.

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