12Gbps SerDes Jitter Tolerance BIST in Production Loopback Testing with Enhanced Spread Spectrum Clock Generation Circuit

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Abstract:

We designed and tested an on-chip BIST test for high speed SerDes devices. Jitter Tolerance testing is a critical way to stress the SerDes receivers. A jitter free loopback test hardly represents the real application environment. We implemented a jitter injection technique to precisely injecting the amount of in-band and out-of-band jitter to effectively testing receiver clock and data recovery circuits (CDR). Because out-of-band jitter is more effective in stressing the CDR, it is critical to generate jitter frequency that is higher than the receiver CDR loop bandwidth. Both the jitter frequency and amplitude can be programmed digitally in this BIST implementation. And more importantly, it does NOT require any external instrument for calibration. As a result, overall production test coverage is enhanced without additional test cost and tester instrument calibration hardware.

1. Introduction:

The evolvement of backplanes from bus-based architectures to fabric/mesh-based architectures has fueled rapid deployment of multi-gigabit serializer and de-serializer (SerDes) devices. The serializer does not transmit a dedicated clock signal. Instead the deserializer needs to have the capability to lock to the received data signal, extract the clock/timing information, retime/resample the received signal with the recovered clock, and make correct detections of the intended transmitted signal. As a result, the two key circuit blocks in the receiver are the clock and data recovery (CDR) and the equalizers (EQ). The CDR extracts the timing information and keeps the data latch staying in the center of the data eye. The EQ reshapes the signal such that logic one is correctly distinguished from logic zero.

In addition, because of the leading edge speed of the SerDes devices, the serial data rates under test are generally faster than what the tester can support. So in many cases, looping back the Tx to Rx for a self test is used. However, a jitter free loopback test hardly represents the real application environment.

This Built-In-Self-Test (BIST) for the CDR circuit is designed in particular for production test using Automated Test Equipments (ATE). The industry recognized method of exercising the CDR circuit is through the compliance jitter tolerance (CJT) test. Jitter is defined as deviation of an actual signal edge from the ideal position, which has many contributing components (i.e. DCD, ISI, PJ, RJ and etc…). The periodic jitter (PJ), also referred to as the sinusoidal jitter (SJ), is commonly used in jitter tolerance tests by modulating the signal before it reaches receiver inputs. Two parameters that define the PJ are the jitter amplitude and the jitter frequency. The CDR circuit reacts differently to different PJ frequencies. When the PJ frequency is low and within the bandwidth of the CDR, the CDR could track the jitter and move along with the jittery signal edges. In that case, the recovered clock stays in the center of the data eye. However when the PJ frequency goes higher than the CDR tracking band, the jitter cut into the timing recovery margin for the CDR. That is why the out-of-band jitter is an effective way to test CDR tolerance margins.

USB Super Speed Electrical Compliance Methodology, Revision 0.5

Table 6. Input jitter requirements for Rx tolerance testing

Symbol	Parameter	Value	Units	Notes
f1	Tolerance corner	4.9	MHz	1,2,3,5
J_{Rj}	Random Jitter	0.0121	UI rms	1,2,3,4
$J_{Rj\_p\text{-}p}$	Random Jitter peak- peak at 10^{-10}	0.154	UI p-p	1,2,3,4
J_{Pj_500kHZ}	Sinusoidal Jitter	2.265	UI p-p	1,2,3,4
J_{Pj_1Mhz}	Sinusoidal Jitter	1.132	UI p-p	1,2,3,4
J_{Pj_2MHz}	Sinusoidal Jitter	0.566	UI p-p	1,2,3,4
J_{Pj_f1}	Sinusoidal Jitter	0.232	UI p-p	1,2,3,4
J_{Pj_50MHz}	Sinusoidal Jitter	0.232	UI p-p	1,2,3,4
V_full_swing	Transition bit differential voltage swing	0.75	V p-p	1,2,3,5
V_EQ_level	Non transition bit voltage (equalization)	-3	dB	1,2,3,5

Notes:

1. All parameters are measured at TP1 Figure 10.
2. Due to time limitations at compliance testing, only a subset of frequencies can be tested. However, the Rx is required to tolerate Pj at all frequencies between the compliance test points.
3. During the Rx tolerance test, SSC is generated by test equipment and present at all times. Each J_{Pj} source is then added and tested to the specification limit one at a time.
4. Specified for a budgeted BER of 10^{-10}.
5. All specified values in this table were extracted from tables 6-19 of the USB 3.0 Specification. In case of conflict, the values in the USB 3.0 Specification supersede those contained in this row.

Figure 1 USB 3.0 electrical compliance test methodology.

Precision PJ generation has been an important component of electrical compliance test methodology on many serial data communication standards. For example, Figure 1 shows USB Super Speed (USB 3.0) compliance test requirements.

978-1-4799-0859-2/13/$31.00 ©2013 IEEE

Despite the importance of jitter testing, test methods and equipments targeted for volume production ATE applications are not widely available. This is partially attributed to the fact that the leading edge SerDes development has outpaced the tracking capability for many testing equipments including ATE. Therefore, the need exists for jitter tolerance test on ATE. It is also a prerequisite for any ATE tests to be cost effective and time efficient for high volume production.

Conventional ATE testing is typically internal and external loopback tests. Although the printed circuit board (PCB) traces used in loopback create some ISI type of jitter, but it is hardly a rigorous CDR stress test. Although one can tune the PCB trace as cable equivalent filters to stress the Rx properly. [1] It is hard to control or even quantify the amount of ISI generated through these PCB traces. And because the layout constrain, it may not be possible to tune the traces length for large number of SerDes ports on the same PCB. Therefore, loopback functional test alone is inadequate for CDR test coverage. As a result, the devices with marginal performance can escape from production test and cause system failures for the customers. Such problems are very difficult to debug once in a system and the replacement cost is extremely high.

The lab characterization can provide a more comprehensive test of the CDR performance with proper jitter injection. [2] An example of jitter tolerance test setup is shown for XFI 10G in Figure 2. This lab setup costs over $300K. Apparently, this setup involves expensive test equipments and requires constant supervision of experienced engineers. It might be feasible for a small sample sized characterization, but not feasible for high volume production test. To achieve an aggressive low defect rate required by some customers, we still rely on DFT innovations.

A few BIST or BOST jitter tolerances techniques have been reported. In [3] [4], the amount of jitter tolerance injection is limited by external PCB and voltage offset induced DCD. This technique requires calibration, but the author can use on-chip jitter measurement capability to properly calibrate the jitter injection. In this method the jitter tolerance measurement is deduced from the internal CDR timing margin instead of a direct sweep of jitter injection. In [5], higher amount of jitter tolerance injection has been achieved through directly modulating the PLL. This made a smooth sweep of jitter input possible, but the PLL modulation limited this technique in generating higher frequency jitter to stress the CDR. Other BOST solutions use delay line modulation to add jitter [6] [7], which can achieve much higher frequency but not feasible for a low overhead BIST case. There was other DFT technique to inject jitter using phase interpolator or timing vernier reported in [8] [9]. They use phase select, which was limited by slow software control rate at the time of publication. In this publication, we present a jitter injection solution that can generate much higher bandwidth jitter, smooth sine wave modulation and no need for offset calibration. [10]

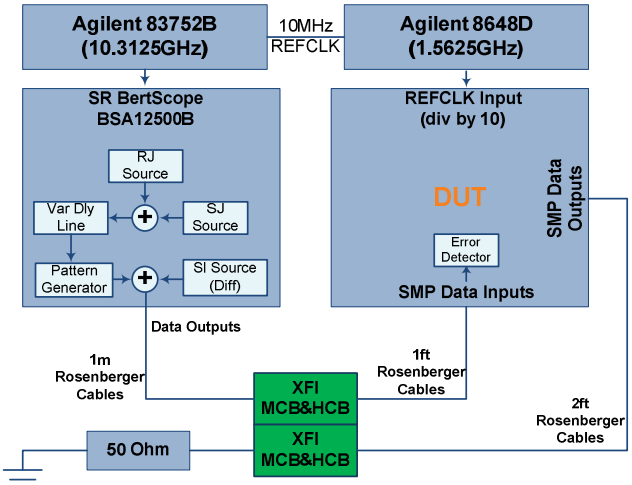

Figure 2 Jitter tolerance test lab characterization setup for XFI 10G.

2. Jitter Tolerance BIST with Enhanced SSC circuit

2.1 Design requirements for using SSC generator for jitter injection

In this publication we will present our patent pending DFT implementation for conducting jitter tolerance test in production loopback mode. We utilized an on-chip circuit to generate the jitter needed for jitter tolerance testing. On the production test ATE board, it looks like just a clean external loopback with no add-on circuit at all. Since it can be easily integrated with other functional tests, our method makes jitter tolerance test practical for high volume production test.

Our goal is to provide a precise, at speed, and yet low cost solution for jitter tolerance test, so the DFT overhead needs to be very low. All the jitter generation and calibration is on the silicon leveraged from existing circuit, instead of dedicated circuits for testing. In this case, we leveraged the circuit for supporting the SSC (Spread Spectrum Clocking) for this DFT needs.

In order to use this DFT as a self contained BIST, it is essential to avoid the needs for external calibration. We achieved that by making the jitter injection function fully synthesized and controlled digitally. This digital approach also simplified the test automation process. In addition, it can be applied on a wide range of ATE platforms because of its tester independent nature.

2.2 Design implementation - a Numerical Control Oscilator (NCO) based SSC design

Theoretically, we can generate precision periodic jitter (PJ) on-chip with precisely controlled frequency offset only in an controlled duration of time. That will introduce phase movement as jitter for this test. However, modulating the transmitter clock beyond receiver tracking frequency is not as straight forward. In most applications, the Tx design has aggressive low jitter design target. Therefore the clock generation PLL's priority is the loop stability factor. The loop bandwidth is controlled much lower than its receiver counterpart. In other words, if the transmitter allows a higher bandwidth needed to stress the receiver in test, the transmitter clock stability is compromised and hence producing higher jitter from Tx. That is the reason why no one would use this bluntly just for DFT. Only low frequency modulation is required on the transmit side such as the spread spectrum clocking (SSC). The SSC is a requirement for many SerDes industry standards like SAS and SATA. However, the SSC modulation is merely in the low 30~100KHz range, where the CDR will have absolutely no issue to track. That makes it harmless to the receiver. So we can NOT rely on this slow modulation to stress the CDR effectively in test.

In this application, our SSC circuit is capable to modulate the clock with more than 100MHz bandwidth. That is enough to generate jitter out of the receiver loop bandwidth. Not every SSC design can achieve that. Some of the SSC designs actively modulates the PLL divider ratios to generate the SSC frequency profile, but dynamically changing the PLL divider is too slow to generate the required out-of-band jitter frequency. We worked around this issue with a high bandwidth modulation NCO design. In this design, the frequency adder is separated from the main VCO feedback loop as illustrated in Figure 3. In this way, the modulation bandwidth is not compromised by stability factor requirement. This new NCO design balanced the two contradicting design requirements (i.e. the higher modulation bandwidth needed for adding jitter in test mode, and the PLL stability to suppress Tx jitter in mission mode).

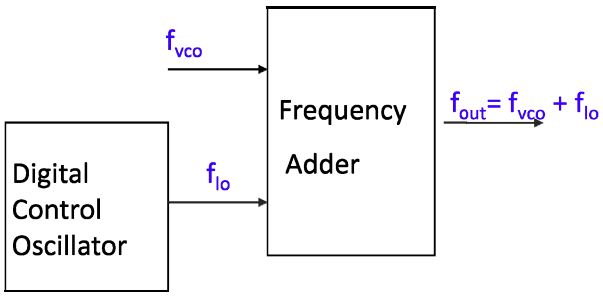

Figure 3 NCO design for SSC generation

In normal SSC mode as shown in Figure 4, a triangle frequency modulation is used. The SSC profile is digitally controlled to ramp up and down in small steps to achieve this.

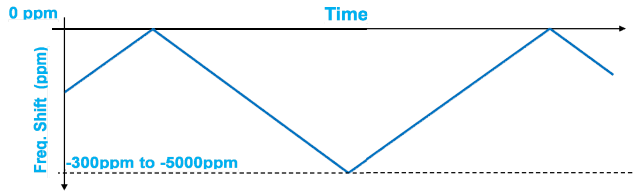

Figure 4 Normal SSC mode with triangle frequency modulation profile

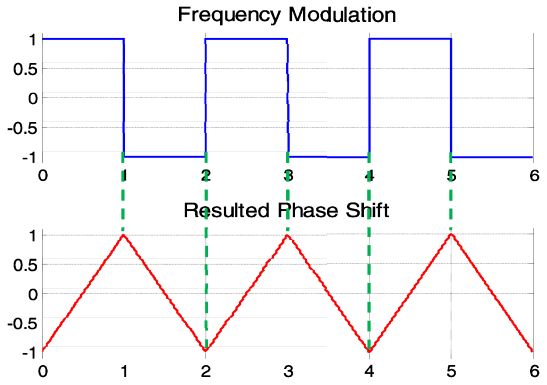

Figure 5 Toggle mode for SSC is used to generate jitter injection

When we use the SSC generator in test mode for periodic jitter injection, as shown in Figure 5, the SSC clock frequency are programmed to toggle between two fixed frequencies ($\mathbf{f}_{max}$ and $\mathbf{f}_{min}$), the duration of each frequency is also precisely controlled. This results in a digitally controlled phase error accumulation from the frequency offset and duration of such offset, as shown in Figure 6. We can obtain the desired PJ frequency from 3MHz to 150MHz. Jitter amplitude is also programmable from 0 to a full UI.

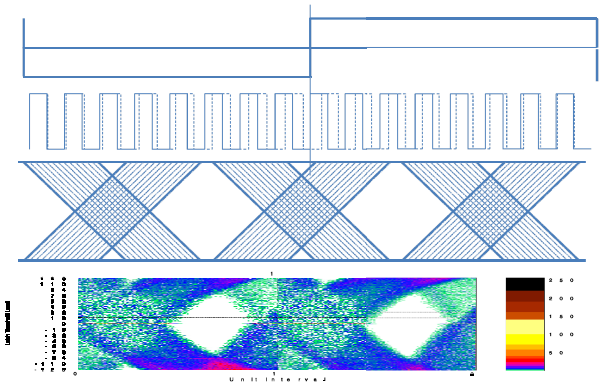

Figure 6 Phase error accumulation over the cycles with the programmed frequency offsets. When overlaying each period in a eye diagram format, the amount of jitter injected is illustrated.

The mathematical model for this phase error accumulation is derived below. If we define the frequency offset between maximum frequency ($\mathbf{f}_{max}$) and minimum frequency ($\mathbf{f}_{min}$) in part per million (ppm) as $ofst_{ppm}$, the frequency of transmitter signal is F_{baud}, the frequency offset of the jittered signal F_{offset_PJ} can be defined as:

$$F_{offset\_PJ} = F_{baud} \times \frac{ofst_{ppm}}{10^6},$$

From the derivative of phase, we obtain the angular frequency offset (rad/s):

$$\frac{d\Theta}{dt} = \omega_{offset\_PJ} = F_{offset\_PJ} \times 2\pi.rad$$

$$\frac{d\Theta}{dt} = F_{baud} \times \frac{ofst_{ppm}}{10^6} \times 2\pi.rad$$

Integrate the above equations and then we have the phase in rad, where F_{PJ} is the frequency of PJ injected:

$$\Theta = F_{baud} \times \frac{ofst_{ppm}}{10^6} \times 2\pi.rad \int_0^{T_{PJ}} dt$$

$$\Theta = F_{baud} \times \frac{ofst_{ppm}}{10^6} \times \frac{2\pi.rad}{2 \times F_{PJ}}$$

$$\Theta = \frac{ofst_{ppm} \times F_{baud}}{2 \times 10^6 \times F_{PJ}} \times 2\pi.rad$$

Converting the phase to PJ, where UI_{pp} is the peak-to-peak unit interval:

$$PJ = \frac{\Theta}{2\pi.rad} \times UI_{pp} = \frac{ofst_{ppm} \times F_{baud}}{2 \times 10^6 \times F_{PJ}} \times UI_{pp}$$

$$PJ_{in\_UI} = \frac{ofst_{ppm} \times F_{baud}}{2 \times 10^6 \times F_{PJ}}$$

This is the mathematical model for the periodic jitter injected in this DFT mode with square wave frequency modulation.

In standard compliance lab test, the sinusoidal jitter profile is common used. So we have implemented sinusoidal modulation profile to avoid any potential correlation issue with common lab instruments.

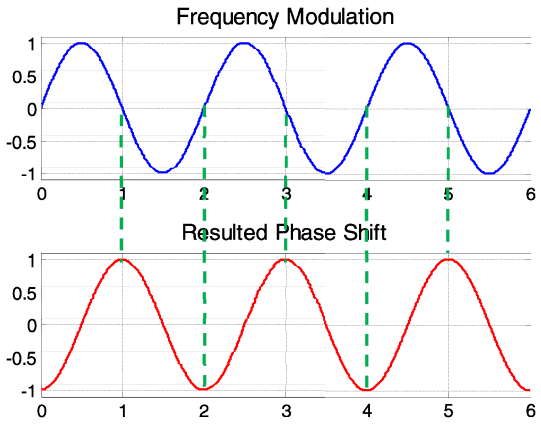

Figure 7 Sinusoidal Jitter injection is implemented using a sine DAC for frequency modulation.

For sinusoidal frequency modulation, again we can define the maximum frequency offset between $\mathbf{f}_{max}$ and $\mathbf{f}_{min}$ in part per million as $ofst_{ppm}$, the frequency of transmitter signal is F_{baud}, the frequency offset of the jittered signal F_{offset_PJ} can be defined as:

$$F_{offset\_max} = F_{baud} \times \frac{ofst_{ppm}}{10^6}$$

$$F_{offset\_SJ} = F_{offset\_max} \times \sin(2\pi \times f_{SJ} \times t)$$

$$F_{offset\_SJ} = F_{baud} \times \frac{ofst_{ppm}}{10^6} \times \sin(2\pi \times f_{SJ} \times t)$$

Where f_{SJ} is the frequency of modulation, which is also the frequency of resulted SJ. From the derivative of phase, we obtain the angular frequency offset (rad/s):

$$\frac{d\Theta}{dt} = \omega_{offset\_PJ} = F_{offset\_SJ} \times 2\pi.rad$$

$$\frac{d\Theta}{dt} = F_{baud} \times \frac{ofst_{ppm}}{10^6} \times \sin(2\pi \times f_{SJ} \times t) \times 2\pi.rad$$

Integrate the above equations and then we have the phase in rad:

$$\Theta = \frac{F_{baud} \times ofst_{ppm}}{10^6} \times 2\pi.rad \int \sin(2\pi \times f_{SJ} \times t) dt$$

$$\Theta = \frac{F_{baud} \times ofst_{ppm}}{2\pi \times f_{SJ} \times 10^6} \times 2\pi.rad \times \cos(2\pi \times f_{SJ} \times t)$$

Converting the phase to SJ, with respect to the peak-to-peak unit interval UI_{pp}:

$$SJ = \frac{\Theta}{2\pi.rad} \times UI_{pp}$$

$$SJ = \frac{ofst_{ppm} \times F_{baud}}{2\pi \times 10^6 \times f_{SJ}} \times \cos(2\pi \times f_{SJ} \times t) \times UI_{pp}$$

Consider the fact cosine wave is a phase shifted sine wave, we can derive the amplitude of the sinusoidal jitter:

$$SJ = \frac{A_{SJ}}{2} \times \sin(2\pi \times f_{SJ} \times t)$$

$$A_{SJ}(UI) = \frac{ofst_{ppm} \times F_{baud}}{\pi \times 10^6 \times f_{SJ}}$$

The following plots illustrate SJ injection obtained from measurements from real silicon. Figure 8 shows the SJ generated with a fixed 25MHz square wave modulation, when we programmed the SSC frequency offset from 0ppm to 17000ppm using digital control logic. The measurement results aligned in a very linear curve for the amount of jitter injected. The silicon data highly correlates with the mathematical model, but at high modulation PPM a slight diverge from model is observed. This conversion error is resulted from the band-limited distortion of squared modulation waveform. As shown in Figure 8, the jitter error is about 4ps as 1UI of jitter injected at 6Gbps.

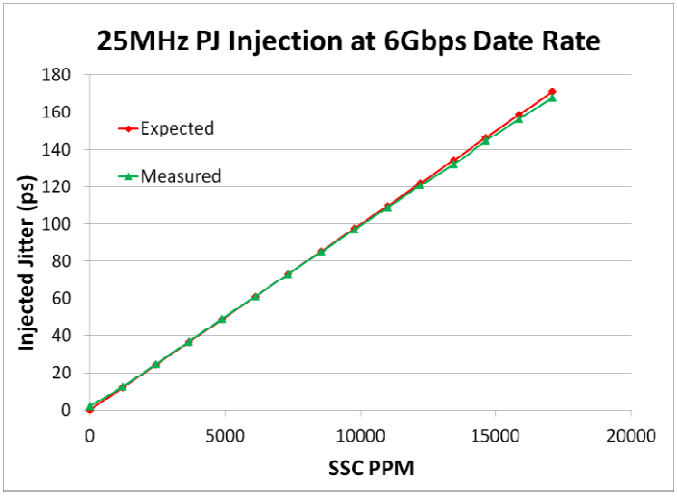

Figure 8 At a fixed jitter frequency, a sweep of frequency offset generates a linearly increasing jitter amplitude. For jitter amplitude above 120ps, slight error will happen due to the waveform distortion at high frequency modulation rate.

The mathematical model above showed the two variables digitally control the jitter injection amount – frequency offset and its duration. The NCO based design inherently bounded the frequency offset accuracy to the digital control oscillator's resolution. The duration in time of this frequency offset is also controlled digitally, in terms of maximum allowed phase movement accumulations over precise number of clock cycles. The end result is a very predictable accumulative phase movement, which is directly translated to a very repeatable jitter inject amplitude from device to device. This important design feature eliminated the need for external calibration of the actual jitter amplitude.

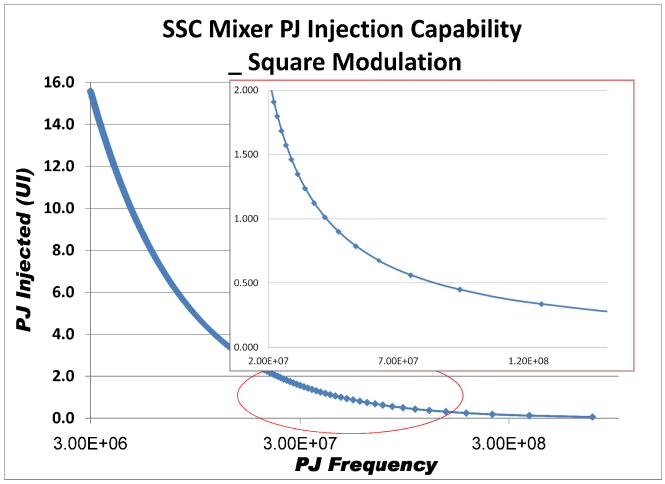

Figure 9 Illustration of Injected SJ frequency and amplitude capability with SSC toggle approach.

Next, we demonstrate a sinusoidal modulation profile can be achieve with the same precision. In this case, the ppm offset frequency changed from a square wave to a sine wave as a modulation waveform. The jitter amplitude is still the integral or accumulation of the phase movement. As shown in Figure 9, we can generate 1.4UI worth of SJ at 30MHz, and 0.8UI worth of SJ at 50MHz. This is more than enough for test 12Gbps SAS CDR with high enough out-of-band SJ frequency, and large enough jitter amplitude.

3. Accuracy Verification Data for the Jitter Injection with the SSC Design

In this section, we will discuss test setup to verify jitter injection frequency and amplitude accuracy. Even though theoretically we do NOT need to calibrate the on-chip jitter injection, it is still necessary to verify the resulted jitter profile, to make sure that we have accomplished our design target. We used a flexible setup in test hardware design, where the device under test (DUT) transmitter and receiver have the option to be connected to a loopback path, or an external real-time sampling scope (Tektronix DSA72004) for validating jitter performance, as shown in Figure 10.

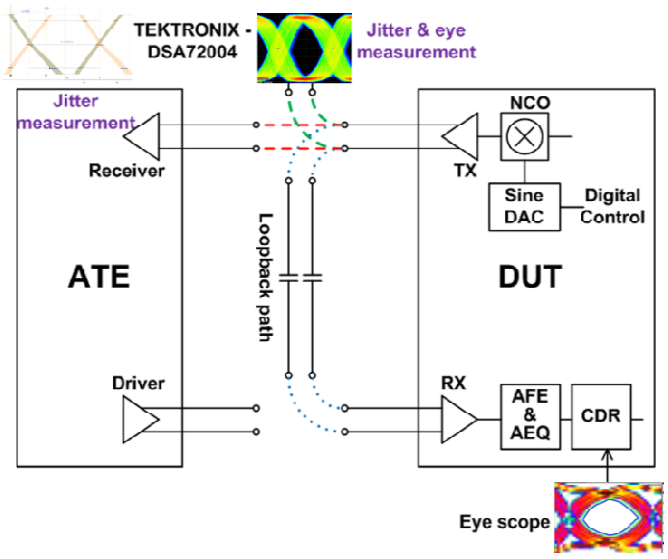

Figure 10 Flexible test hardware provides the capability to verify injected jitter in different ways while support production test.

We used an external realtime sampling scope to illustrate the real silicon results to confirm the frequency offset accuracy and duration control resolution is adequate. In Figure 11, 12Gbps signals with SJ frequency of 15MHz and 31.25MHz at different jitter magnitude are displayed. The jitter frequency and amplitude measurements match very well with the theoretical calculation, the result was very repeatable in multiple loop-run with power on reset. In the test setup, we used double transition clock pattern to minimize other jitter components in this SJ verification.

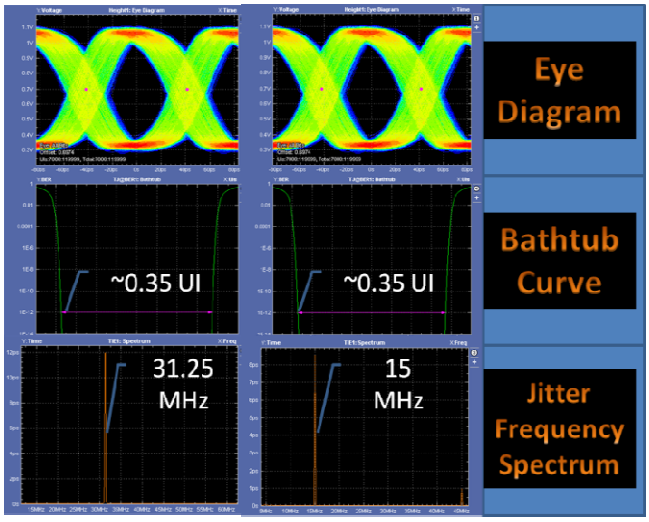

Figure 11 Realtime scope view of SJ injected signal, correlates very well with expected jitter magnitude and frequency.

Realtime oscilloscope is capable of measuring jitter very accurately, but time consuming if we have to measure a large number of settings. By using ATE high speed test equipment, we can also systematically verify the jitter amplitude profile without using an external oscilloscope. By driving an un-jittered clock pattern from DUT, without the presence of data dependent jitter (DDJ) and inter-symbol interference (ISI), we assume ATE measured total jitter (TJ_{Total}) equal to the combination of random jitter (RJ), duty cycle distortion (DCD) jitter and device intrinsic PJ (PJ_{DUT}), we define this as total intrinsic jitter ($TJ_{Intrinsic}$).

$$TJ_{Intrinsic} = RJ + DCD + PJ_{DUT}$$

With the same device, same data pattern and same test back plane, we then add controlled amount of PJ. If we assume $TJ_{Intrinsic}$ stay the same, with jitter injected, the TJ measured will grow linearly as injected PJ_{Inj}.

$$TJ_{Total} = RJ + DCD + PJ_{DUT} + PJ_{Inj}$$

$$TJ_{Total} = TJ_{Intrinsic} + PJ_{Inj}$$

Therefore, we can depend on the TJ measurements from ATE high speed equipment, and normalize to injected SJ amplitude by subtracting the calibrated intrinsic jitter. The test setup displayed in Figure 10 provides the feasibility of correlating injected jitter with automated ATE measurement at different jitter frequency and devices from different process corner. Figure 12 shows the correlation between normalized SJ amplitude and theoretical calculation. The small variation is a result of ATE measurement noise floor. The oscilloscope capture shows better repeatability. Benefiting from single-tone Sine modulation waveform which contains less high frequency harmonic components as in square wave modulations, the jitter error at higher jitter amplitude shows an improvement in Figure 8.

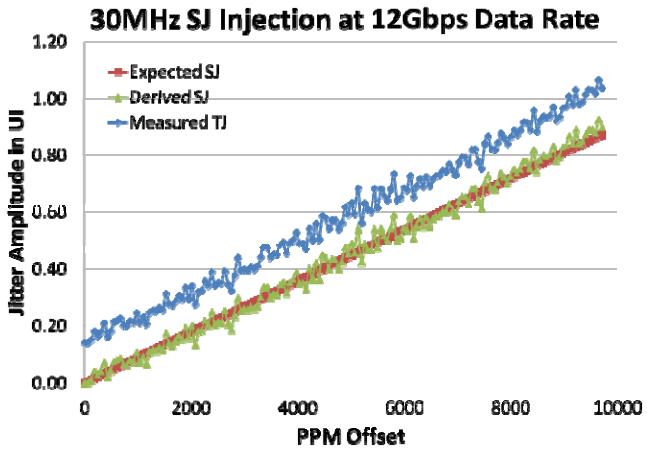

Figure 12 ATE measured jitter correlated to the theoretical values

4. Jitter tolerance test in production and its application for CDR setting optimization

The next step of verification of this technique is to apply the BIST in loopback mode. We took advantage of the ability to sweep the PJ frequencies, and plot out the jitter tolerance level v.s. PJ frequency. Figure 13 shows a sweep of different PJ frequency points to illustrate that our NCO based SSC design actually reach beyond the out-of-band jitter range for effective receiver CDR stressing. The result illustrated an expected curve with a clear transition around the receiver tracking band of a few MHz. Below the CDR tracking bandwidth, a large amount low frequency jitter (i.e. >=1UI) is still not enough to stress the receiver. When the jitter frequency reaches beyond the receiver tracking band, the jitter tolerance curve became flat, indicating CDR no longer tracking the fast phase movement.

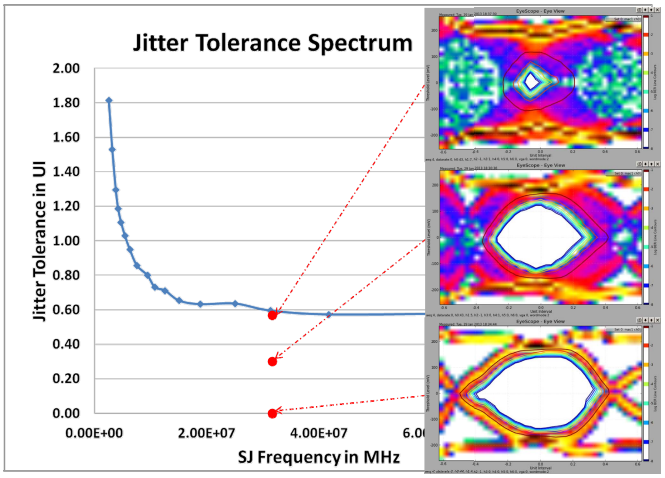

Figure 13 Jitter tolerance test results at various injected PJ frequencies at 12Gbps. As expected, out of band jitter produced a relative flat jitter tolerance profiles when CDR loses the ability to keep track of the high frequency jitter.

Taking advantage of the relatively fast loopback test approach, we can achieve faster CDR setting optimization and reduce the validation workload traditionally can only be done with bench instruments. Fig. 14 illustrate the jitter tolerance spectrums with different CDR loop settings, the data series in green is a result from the best settings, which achieved best jitter tolerance performance, and more balanced CDR tracking capability to low frequency and high frequency noise. The other 3 non-optimal loop settings yielded in lower jitter tolerance performance.

The internal Rx "eye scope" is built in Rx eye monitor tool. We captured Rx internal eye diagrams under 4 different settings to help visualize the actual Rx jitter timing margin. In Figure 14, with the same amount of jitter injected, the eye scopes indicate significant difference in eye opening under these 4 CDR settings. The different levels of eye opening indicate the difference of CDR tracking capability under the same injected jitter condition (i.e. a 0.3UI 25MHz SJ). This clearly shown the bottom setting will make the device failing without margin, while the top one with a lot of room to tolerate even more jitter coming in. Without the built in SSC jitter injection capability like that, ATE test with loopback will show all 3 settings above as all "passing". Now with this capability, we can provide constructive setting optimization with quantifiable margin analysis.

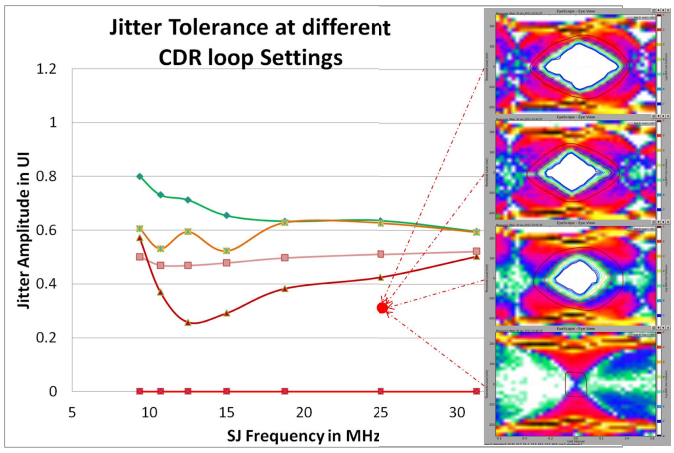

Figure 14 Loopback based jitter tolerance sweep provides relative fast approach to optimize CDR settings for better and more balanced tracking efficiency

4. Conclusions:

We demonstrated the effectiveness of our enhanced SSC based jitter tolerance test in loopback mode. This enables us to produce robust jitter tolerance test in the most cost effective fashion. The important distinguishable advantages for this technique is that we do NOT need any external instruments or elaborate calibration schemes. Because of these unique attributes, this technique is independent to the tester platform choice.

The limitation of this technique is using only one type of jitter (PJ) to stress the CDR. Even though it is very efficient in stressing the receiver, but the real application environment with a combination of different jitter types can NOT be directly emulated. For example, the ISI type of jitter result from bandwidth limited transmission media is another type of jitter can stress the receiver CDR differently.

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